# EFM32 Wonder Gecko Family
# EFM32WG Data Sheet

## The EFM32 Wonder Gecko MCUs are the world's most energy-friendly microcontrollers.

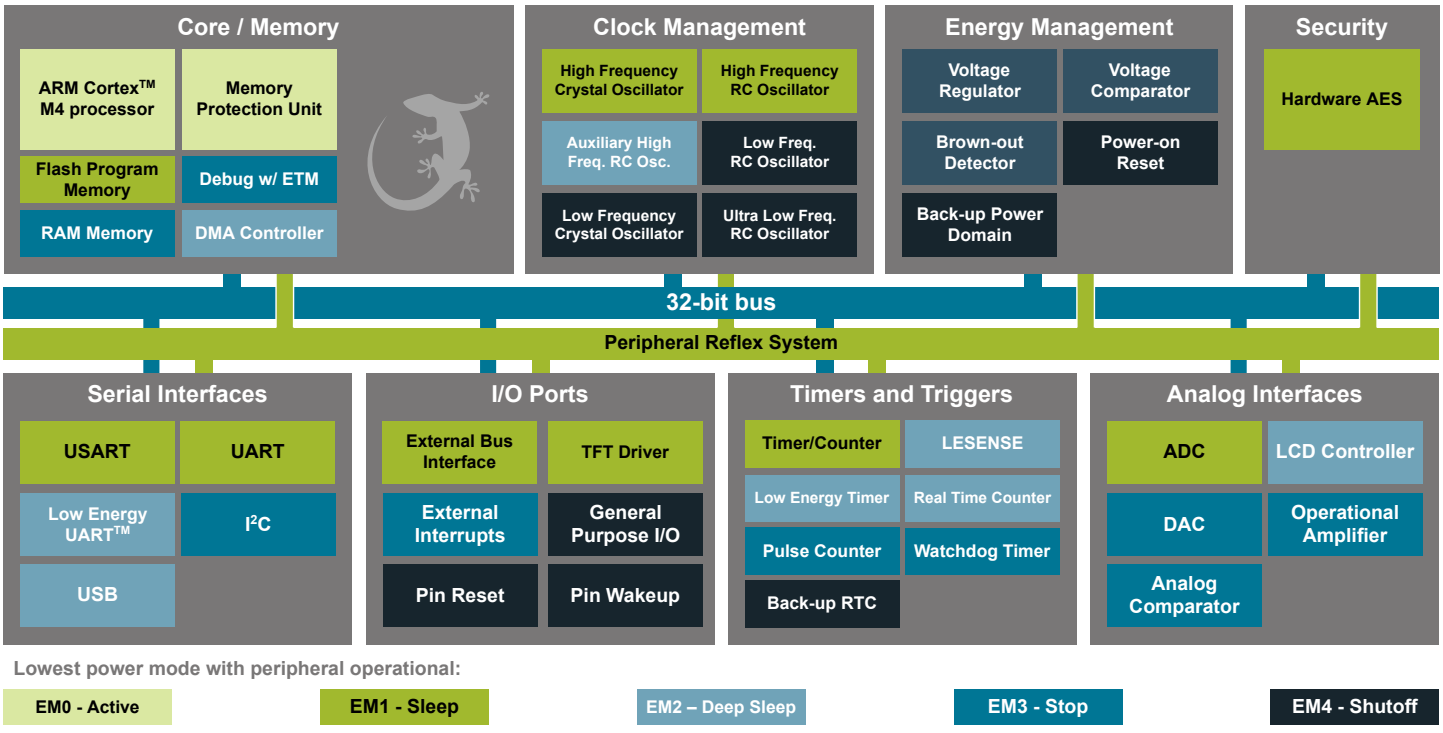
The EFM32WG offers unmatched performance and ultra low power consumption in both active and sleep modes. EFM32WG devices consume as little as 0.65 µA in Stop mode and 211 µA/MHz in Run mode. It also features autonomous peripherals, high overall chip and analog integration, and the performance of the industry standard 32-bit ARM Cortex-M4 with Floating-Point Unit (FPU) processor, making it perfect for battery-powered systems and systems with high-performance, low-energy requirements.

EFM32WG applications include the following:

- Energy, gas, water and smart metering
- Health and fitness applications
- Smart accessories
- Alarm and security systems
- Industrial and home automation

**KEY FEATURES**

- ARM Cortex-M4 with Floating-Point Unit (FPU) at 48 MHz
- Ultra low power operation
  - 0.65 µA current in Stop (EM3), with brown-out detection and RAM retention
  - 63 µA/MHz in EM1
  - 211 µA/MHz in Run mode (EM0)
- Fast wake-up time of 2 µs
- Hardware cryptography (AES)
- Up to 256 kB of Flash and 32 kB of RAM



# 1. Feature List

- ARM Cortex-M4 CPU platform
  - High Performance 32-bit processor @ up to 48 MHz
  - DSP instruction support and floating-point unit
  - Memory Protection Unit
- Flexible Energy Management System
  - 20 nA @ 3 V Shutoff Mode
  - 0.4 µA @ 3 V Shutoff Mode with RTC
  - 0.65 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.95 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 63 µA/MHz @ 3 V Sleep Mode
  - 211 µA/MHz @ 3 V Run Mode, with code executed from flash
- 256/128/64 kB Flash
- 32 kB RAM
- Up to 93 General Purpose I/O pins
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- 12 Channel DMA Controller
- 12 Channel Peripheral Reflex System (PRS) for autonomous inter- peripheral signaling
- Hardware AES with 128/256-bit keys in 54/75 cycles
- Timers/Counters
  - 4× 16-bit Timer/Counter
    - 4×3 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 16-bit Low Energy Timer
  - 1× 24-bit Real-Time Counter and 1× 32-bit Real-Time Counter
  - 3× 16/8-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- Integrated LCD Controller for up to 8×36 segments
  - Voltage boost, adjustable contrast and autonomous animation
- Backup Power Domain
  - RTC and retention registers in a separate power domain, available in all energy modes
  - Operation from backup battery when main power drains out
- External Bus Interface for up to 4x256 MB of external memory mapped space
  - TFT Controller with Direct Drive
- Communication interfaces
  - Up to 3× Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
  - 2× Universal Asynchronous Receiver/Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2× $I^2C$ Interface with SMBus support
    - Address recognition in Stop Mode
  - Universal Serial Bus (USB) with Host & OTG support
    - Fully USB 2.0 compliant
    - On-chip PHY and embedded 5V to 3.3V regulator

- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 8 single ended channels/4 differential channels
    - On-chip temperature sensor
  - 12-bit 500 ksamples/s Digital to Analog Converter
  - 2× Analog Comparator
    - Capacitive sensing with up to 16 inputs
  - 3× Operational Amplifier
    - 6.1 MHz GBW, Rail-to-rail, Programmable Gain
  - Supply Voltage Comparator
- Low Energy Sensor Interface (LESENSE)
  - Autonomous sensor monitoring in Deep Sleep Mode
  - Wide range of sensors supported, including LC sensors and capacitive buttons
- Ultra efficient Power-on Reset and Brown-Out Detector
- Debug Interface
  - 2-pin Serial Wire Debug interface
    - 1-pin Serial Wire Viewer
  - Embedded Trace Module v3.5 (ETM)
- Pre-Programmed USB/UART Bootloader
- Temperature range -40 to 85 ºC
- Single power supply 1.98 to 3.8 V
- Packages:
  - BGA112
  - BGA120
  - LQFP100
  - TQFP64
  - QFN64

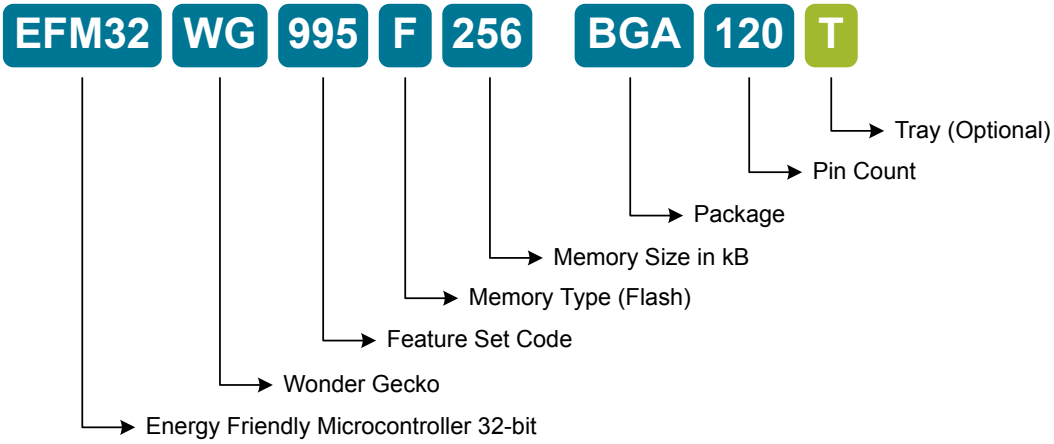
## 2. Ordering Information

The following table shows the available EFM32WG devices.

**Table 2.1. Ordering Information**

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32WG230F64-QFN64 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG230F128-QFN64 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG230F256-QFN64 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG232F64-QFP64 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG232F128-QFP64 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG232F256-QFP64 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG280F64-QFP100 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG280F128-QFP100 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG280F256-QFP100 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG290F64-BGA112 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG290F128-BGA112 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG290F256-BGA112 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG295F64-BGA120 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG295F128-BGA120 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG295F256-BGA120 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG330F64-QFN64 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG330F128-QFN64 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG330F256-QFN64 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG332F64-QFP64 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG332F128-QFP64 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG332F256-QFP64 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG360F64G-A-CSP81 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | CSP81 |
| EFM32WG360F128G-A-CSP81 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | CSP81 |
| EFM32WG360F256G-A-CSP81 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | CSP81 |
| EFM32WG380F64-QFP100 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG380F128-QFP100 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG380F256-QFP100 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG390F64-BGA112 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG390F128-BGA112 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG390F256-BGA112 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG395F64-BGA120 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG395F128-BGA120 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32WG395F256-BGA120 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG840F64-QFN64 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG840F128-QFN64 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG840F256-QFN64 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG842F64-QFP64 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG842F128-QFP64 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG842F256-QFP64 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG880F64-QFP100 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG880F128-QFP100 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG880F256-QFP100 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG890F64-BGA112 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG890F128-BGA112 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG890F256-BGA112 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG895F64-BGA120 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG895F128-BGA120 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG895F256-BGA120 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG900F256G-A-D1I | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | Wafer |
| EFM32WG940F64-QFN64 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG940F128-QFN64 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG940F256-QFN64 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32WG942F64-QFP64 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG942F128-QFP64 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG942F256-QFP64 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32WG980F64-QFP100 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG980F128-QFP100 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG980F256-QFP100 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG990F64-BGA112 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG990F128-BGA112 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG990F256-BGA112 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32WG995F64-BGA120 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG995F128-BGA120 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG995F256-BGA120 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |


EFM32
WG
995
F
256
BGA
120
T
Tray (Optional)
Pin Count
Package
Memory Size in kB
Memory Type (Flash)
Feature Set Code
Wonder Gecko
Energy Friendly Microcontroller 32-bit

Adding the suffix 'T' to the part number (e.g. EFM32WG995F256-BGA120T) denotes tray packaging.

Visit http://www.silabs.com for information on global distributors and representatives.

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# 3. System Summary

## 3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M4 with Floating-Point Unit (FPU), innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32WG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32WG devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32WG Reference Manual.

A block diagram of the EFM32WG is shown in the following figure.

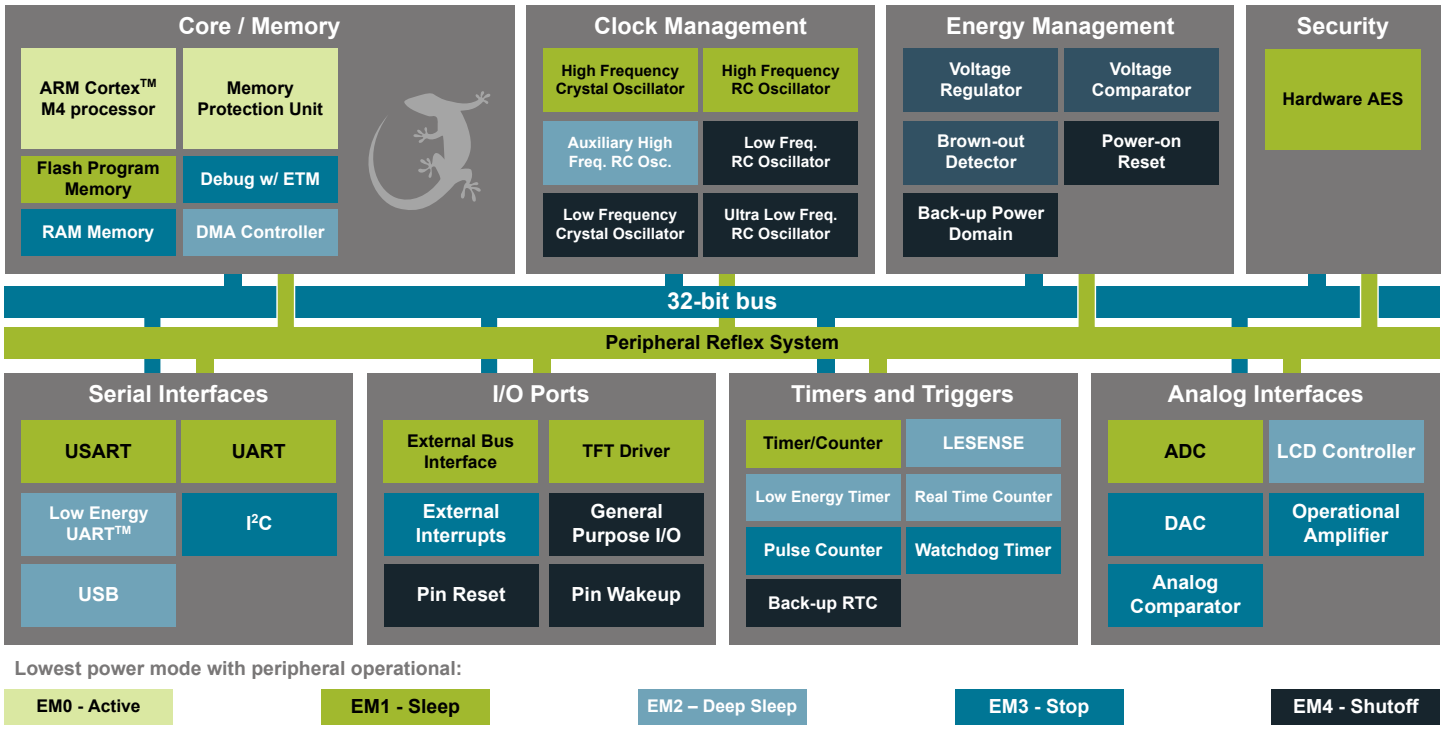



**Figure 3.1. Block Diagram**

### 3.1.1 ARM Cortex-M4 Core

The ARM Cortex-M4 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M4 is described in detail in EFM32WG Reference Manual.

### 3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

### 3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32WG microcontroller. The flash memory is readable and writable from both the Cortex-M4 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

### 3.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32WG.

### 3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32WG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32WG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 3.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M4. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

### 3.1.11 TFT Direct Drive

The EBI contains a TFT controller which can drive a TFT via a 565 RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

### 3.1.12 Universal Serial Bus Controller (USB)

The USB is a full-speed USB 2.0 compliant OTG host/device controller. The USB can be used in Device, On-the-go (OTG) Dual Role Device or Host-only configuration. In OTG mode the USB supports both Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The device supports both fullspeed (12MBit/s) and low speed (1.5MBit/s) operation. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes all OTG features, except for the voltage booster for supplying 5V to VBUS when operating as host.

### 3.1.13 Inter-Integrated Circuit Interface (I2C)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the $I^2C$ module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

### 3.1.14 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 Smart-Cards, IrDA and I2S devices.

### 3.1.15 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0042 is pre-programmed in the device at factory. The bootloader enables users to program the EFM32 through a UART or a USB CDC class virtual UART without the need for a debugger. The autobaud feature, interface and commands are described further in the application note.

### 3.1.16 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

### 3.1.17 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/ s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

### 3.1.18 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse- Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

### 3.1.19 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 3.1.20 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

### 3.1.21 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

### 3.1.22 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 3.1.23 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 3.1.24 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 3.1.25 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

### 3.1.26 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single-ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

### 3.1.27 Operational Amplifier (OPAMP)

The EFM32WG features up to 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single-ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

### 3.1.28 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE™), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

### 3.1.29 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32WG to keep track of time and retain data, even if the main power source should drain out.

### 3.1.30 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 3.1.31 General Purpose Input/Output (GPIO)

In the EFM32WG, there are up to 93 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

### 3.1.32 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

## 3.2 Configuration Summary

### 3.2.1 EFM32WG230

The features of the EFM32WG230 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.1. EFM32WG230 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |

| Module | Configuration | Pin Connections |
|---|---|---|
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 56 pins | Available pins are shown in 5.1.3 GPIO Pinout Overview |

### 3.2.2 EFM32WG232

The features of the EFM32WG232 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.2. EFM32WG232 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |

| Module | Configuration | Pin Connections |
|---|---|---|
| AES | Full configuration | NA |
| GPIO | 53 pins | Available pins are shown in 5.2.3 GPIO Pinout Overview |

### 3.2.3 EFM32WG280

The features of the EFM32WG280 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.3. EFM32WG280 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 85 pins | Available pins are shown in 5.3.3 GPIO Pinout Overview |

### 3.2.4 EFM32WG290

The features of the EFM32WG290 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.4. EFM32WG290 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 90 pins | Available pins are shown in 5.4.3 GPIO Pinout Overview |

### 3.2.5 EFM32WG295

The features of the EFM32WG295 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.5. EFM32WG295 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 93 pins | Available pins are shown in 5.5.3 GPIO Pinout Overview |

### 3.2.6 EFM32WG330

The features of the EFM32WG330 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.6. EFM32WG330 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[3:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |

| Module | Configuration | Pin Connections |
|---|---|---|
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 53 pins | Available pins are shown in 5.6.3 GPIO Pinout Overview |

### 3.2.7 EFM32WG332

The features of the EFM32WG332 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.7. EFM32WG332 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[3:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |

| Module | Configuration | Pin Connections |
|---|---|---|
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 50 pins | Available pins are shown in 5.7.3 GPIO Pinout Overview |

### 3.2.8 EFM32WG360

The features of the EFM32WG360 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.8. EFM32WG360 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |

| Module | Configuration | Pin Connections |
|---|---|---|
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 65 pins | Available pins are shown in 5.8.3 GPIO Pinout Overview |

### 3.2.9 EFM32WG380

The features of the EFM32WG380 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.9. EFM32WG380 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| ACMP1 | Full configuration | ACMP1_CH[3:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 83 pins | Available pins are shown in 5.9.3 GPIO Pinout Overview |

### 3.2.10 EFM32WG390

The features of the EFM32WG390 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.10. EFM32WG390 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| ACMP1 | Full configuration | ACMP1_CH[3:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 86 pins | Available pins are shown in 5.10.3 GPIO Pinout Overview |

### 3.2.11 EFM32WG395

The features of the EFM32WG395 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.11. EFM32WG395 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 93 pins | Available pins are shown in 5.11.3 GPIO Pinout Overview |

### 3.2.12 EFM32WG840

The features of the EFM32WG840 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.12. EFM32WG840 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:4], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |

| Module | Configuration | Pin Connections |
|---|---|---|
| AES | Full configuration | NA |
| GPIO | 56 pins | Available pins are shown in 5.12.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[19:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.13 EFM32WG842

The features of the EFM32WG842 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.13. EFM32WG842 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:4], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |

| Module | Configuration | Pin Connections |
|---|---|---|
| AES | Full configuration | NA |
| GPIO | 53 pins | Available pins are shown in 5.13.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[17:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.14 EFM32WG880

The features of the EFM32WG880 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.14. EFM32WG880 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 85 pins | Available pins are shown in 5.14.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.15 EFM32WG890

The features of the EFM32WG890 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.15. EFM32WG890 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 90 pins | Available pins are shown in 5.15.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.16 EFM32WG895

The features of the EFM32WG895 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.16. EFM32WG895 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 93 pins | Available pins are shown in Table 4.3 (p. 70) |
| LCD | Full configuration | LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.17 EFM32WG900

The features of the EFM32WG900 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.17. EFM32WG900 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NAND-WEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 93 pins | Available pins are shown in 5.17.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.18 EFM32WG940

The features of the EFM32WG940 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.18. EFM32WG940 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |

| Module | Configuration | Pin Connections |
|---|---|---|
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 53 pins | Available pins are shown in 5.18.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[17:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.19 EFM32WG942

The features of the EFM32WG942 is a subset of the feature set described in the EFM32WG Reference Manual. The following table device specific implementation of the features.

**Table 3.19. EFM32WG942 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |

| Module | Configuration | Pin Connections |
|---|---|---|
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 50 pins | Available pins are shown in 5.19.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[15:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.20 EFM32WG980

The features of the EFM32WG980 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.20. EFM32WG980 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| ACMP1 | Full configuration | ACMP1_CH[3:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 81 pins | Available pins are shown in 5.20.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[33:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.21 EFM32WG990

The features of the EFM32WG990 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.21. EFM32WG990 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| ACMP1 | Full configuration | ACMP1_CH[3:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 86 pins | Available pins are shown in 5.21.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[33:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.2.22 EFM32WG995

The features of the EFM32WG995 is a subset of the feature set described in the EFM32WG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.22. EFM32WG995 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 93 pins | Available pins are shown in 5.22.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

### 3.3 Memory Map

The EFM32WG memory map is shown in the following figure, with RAM and Flash sizes for the largest memory configuration.

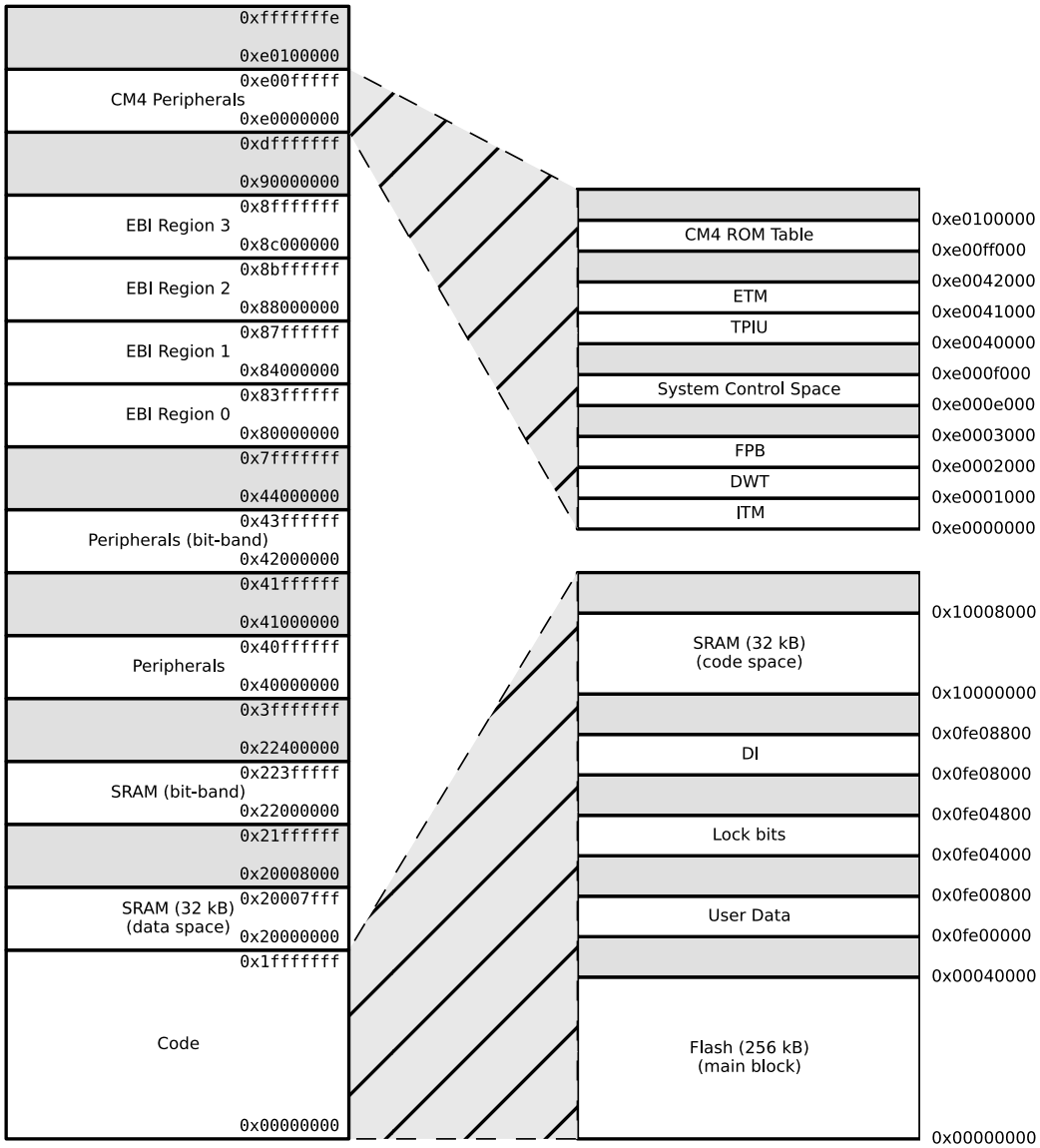



**Figure 3.2. System Address Space with Core and Code Space Listing**

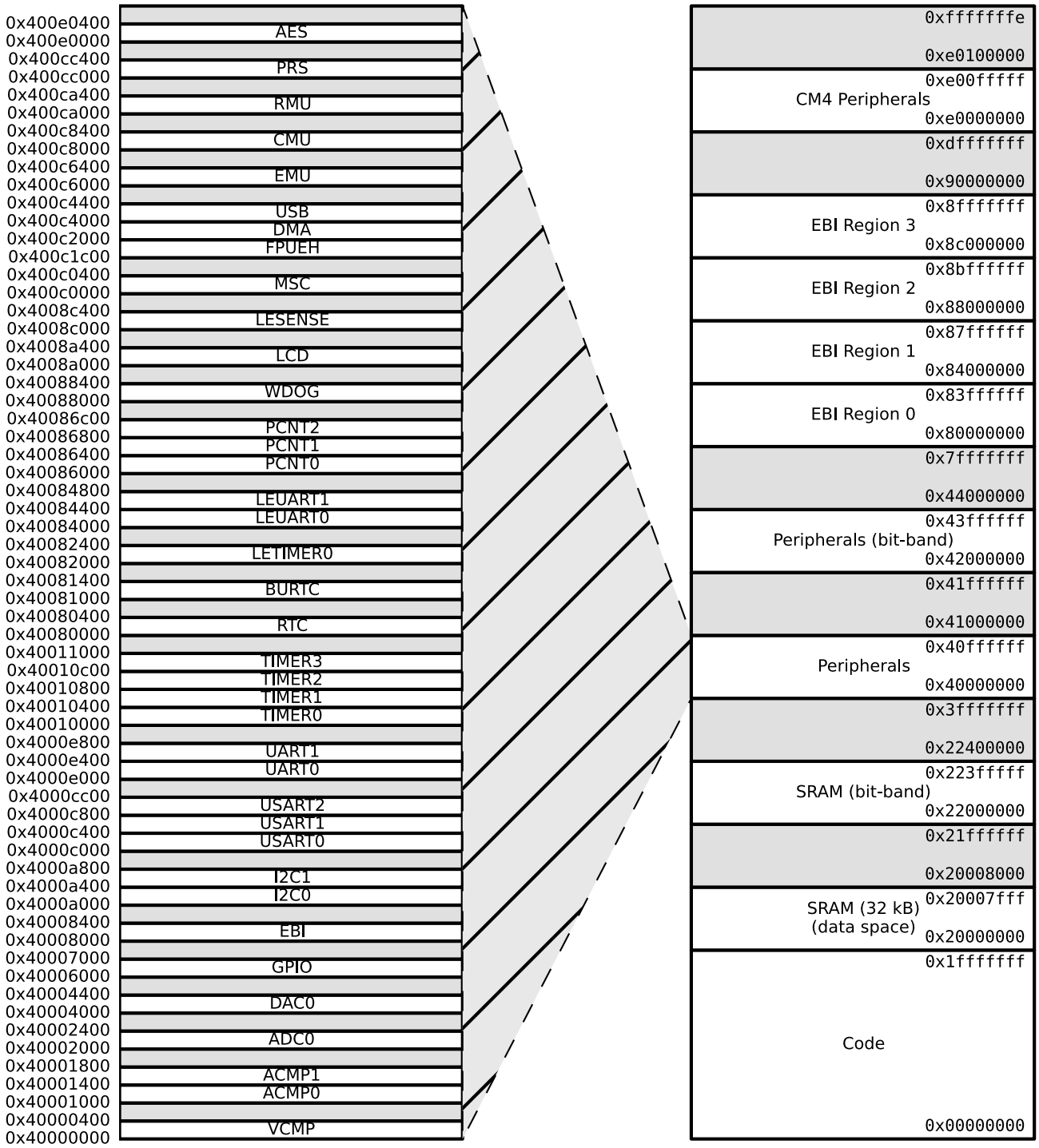



**Figure 3.3. System Address Space with Peripheral Listing**

# 4. Electrical Characteristics

## 4.1 Test Conditions

### 4.1.1 Typical Values

The typical data are based on $T_{AMB}$=25°C and $V_{DD}$=3.0 V, as defined in 4.3 General Operating Conditions, unless otherwise specified.

### 4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in 4.3 General Operating Conditions, unless otherwise specified.

## 4.2 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

**Table 4.1. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -40 | — | 150 | °C |
| Maximum soldering temperature | $T_S$ | Latest IPC/JEDEC J-STD-020 Standard | — | — | 260 | °C |
| External main supply voltage | $V_{DDMAX}$ | | 0 | — | 3.8 | V |
| Voltage on any I/O pin | $V_{IOPIN}$ | | -0.3 | — | $V_{DD}$+0.3 | V |
| Current per I/O pin (sink) | $I_{IOMAX_SINK}$ | | — | — | 100 | mA |
| Current per I/O pin (source) | $I_{IOMAX_SOURCE}$ | | — | — | -100 | mA |

## 4.3 General Operating Conditions

**Table 4.2. General Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ambient temperature range | $T_{AMB}$ | -40 | — | 85 | °C |
| Operating supply voltage | $V_{DDOP}$ | 1.98 | — | 3.8 | V |
| Internal APB clock frequency | $f_{APB}$ | — | — | 48 | MHz |
| Internal AHB clock frequency | $f_{AHB}$ | — | — | 48 | MHz |

### 4.4 Backup Supply Domain

**Table 4.3. Backup Supply Domain**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Backup supply voltage range | $V_{BU_VIN}$ | | 1.8 | — | 3.8 | V |
| PWRRES resistor | $R_{PWRRES}$ | EMU_PWRCONF_PWRRES = RES0 | 4234 | 4485 | 4786 | Ω |
| | | EMU_PWRCONF_PWRRES = RES1 | 2208 | 2363 | 2528 | Ω |
| | | EMU_PWRCONF_PWRRES = RES2 | 1166 | 1297 | 1433 | Ω |
| | | EMU_PWRCONF_PWRRES = RES3 | 295 | 344 | 399 | Ω |
| Output impedance between BU_VIN and BU_VOUT [1] | $R_{BU_VOUT}$ | EMU_PWRCONF_VOUTSTRONG = 1, EMU_PWRCONF_VOUTMED = 0, EMU_PWRCONF_VOUTWEAK = 0 | 49 | 63 | 80 | Ω |
| | | EMU_PWRCONF_VOUTSTRONG = 0, EMU_PWRCONF_VOUTMED = 1, EMU_PWRCONF_VOUTWEAK = 0 | 522 | 670 | 844 | Ω |
| | | EMU_PWRCONF_VOUTSTRONG = 0, EMU_PWRCONF_VOUTMED = 0, EMU_PWRCONF_VOUTWEAK = 1 | 5161 | 6743 | 7853 | Ω |
| Supply current | $I_{BU_VIN}$ | BU_VIN not powering backup domain | — | 3.4 | 6.5 | nA |
| | | BU_VIN powering backup domain | — | 197 | 1050 | nA |

**Note:**
1. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

## 4.5 Current Consumption

**Table 4.4. Current Consumption**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz) | $I_{EM0}$ | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 211 | 225 | µA/MHz |
| | | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 211 | 230 | µA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 212 | 220 | µA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 213 | 223 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 214 | 224 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 215 | 226 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 216 | 231 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 217 | 237 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 218 | 239 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 219 | 239 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 224 | 245 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 224 | 258 | µA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 257 | 285 | µA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 261 | 293 | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| EM1 current (Production test condition = 14 MHz) | $I_{EM1}$ | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 63 | 75 | µA/MHz |
| | | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 65 | 76 | µA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 64 | 75 | µA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 65 | 77 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 65 | 76 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 66 | 78 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 67 | 79 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 68 | 82 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 68 | 81 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 70 | 83 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 74 | 87 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 76 | 89 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 106 | 120 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 112 | 129 | µA/MHz |
| EM2 current | $I_{EM2}$ | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 0.95[1] | 1.7[1] | µA |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 3.0[1] | 4.0[1] | µA |
| EM3 current | $I_{EM3}$ | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 0.65 | 1.3 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 2.65 | 4.0 | µA |
| EM4 current | $I_{EM4}$ | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | — | 0.020 | 0.055 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | — | 0.44 | 0.90 | µA |

**Note:**
1. Using backup RTC.

### 4.5.1 EM1 Current Consumption

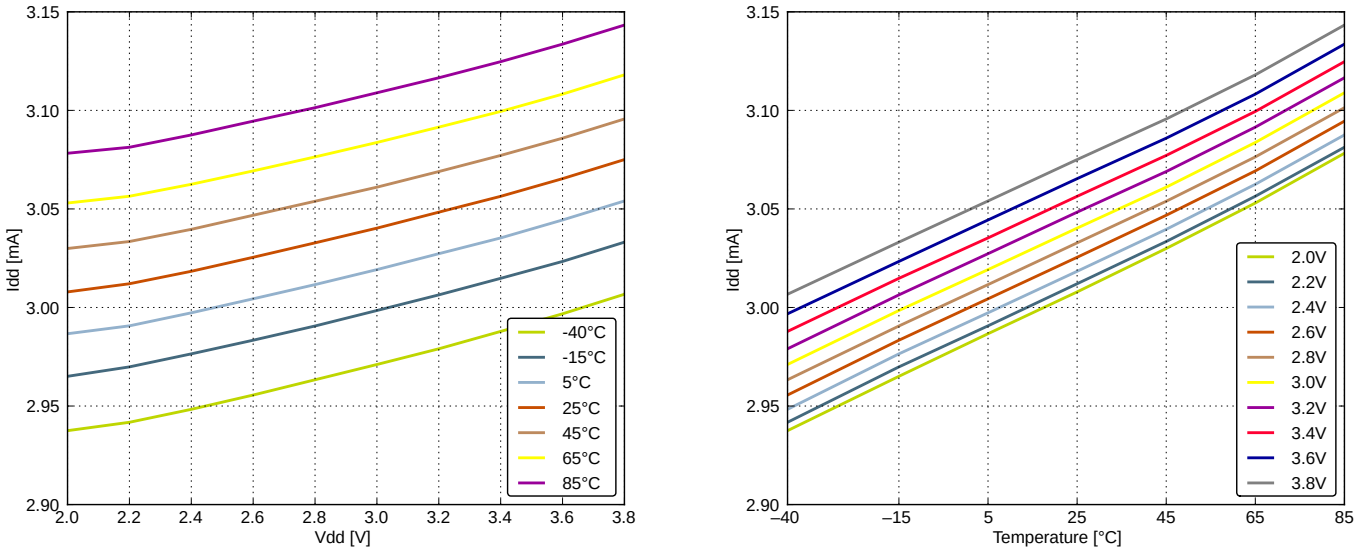



**Figure 4.1. EM1 Current consumption with all peripheral clocks disabled and HFXO running at 48 MHz**

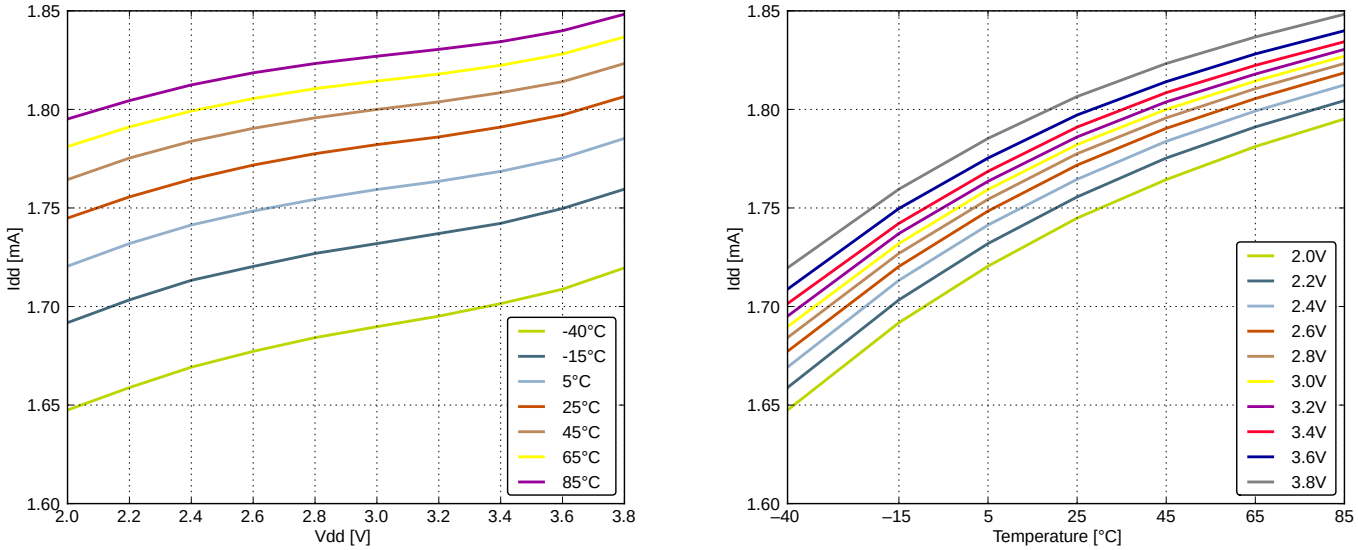



**Figure 4.2. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 28 MHz**

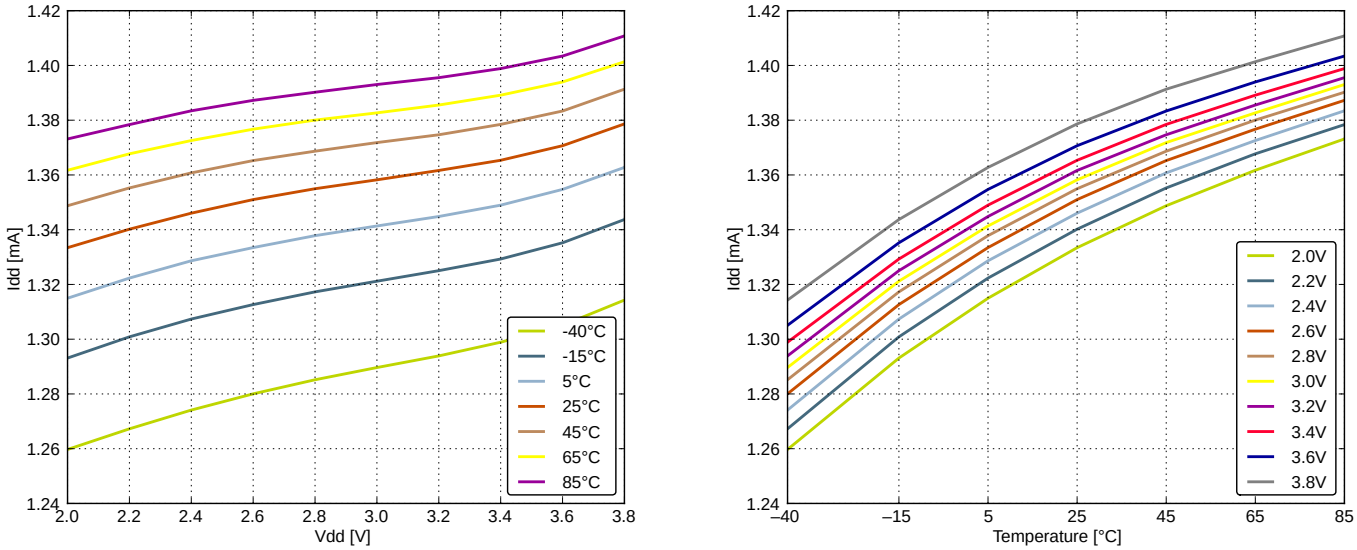



**Figure 4.3. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 21 MHz**

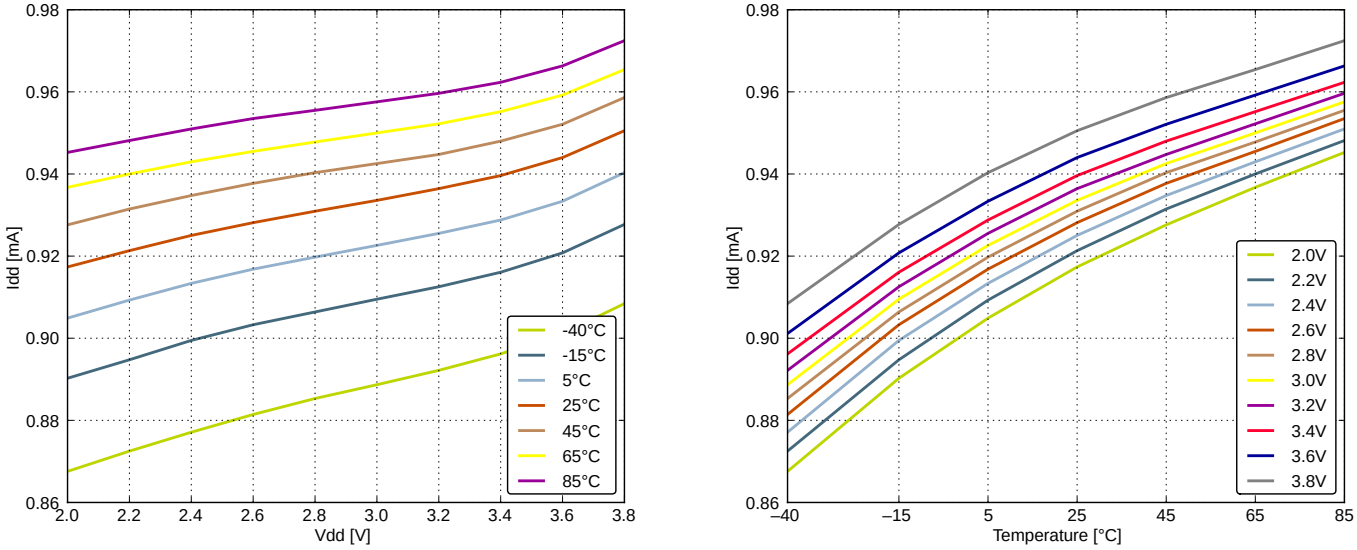



**Figure 4.4. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 14 MHz**

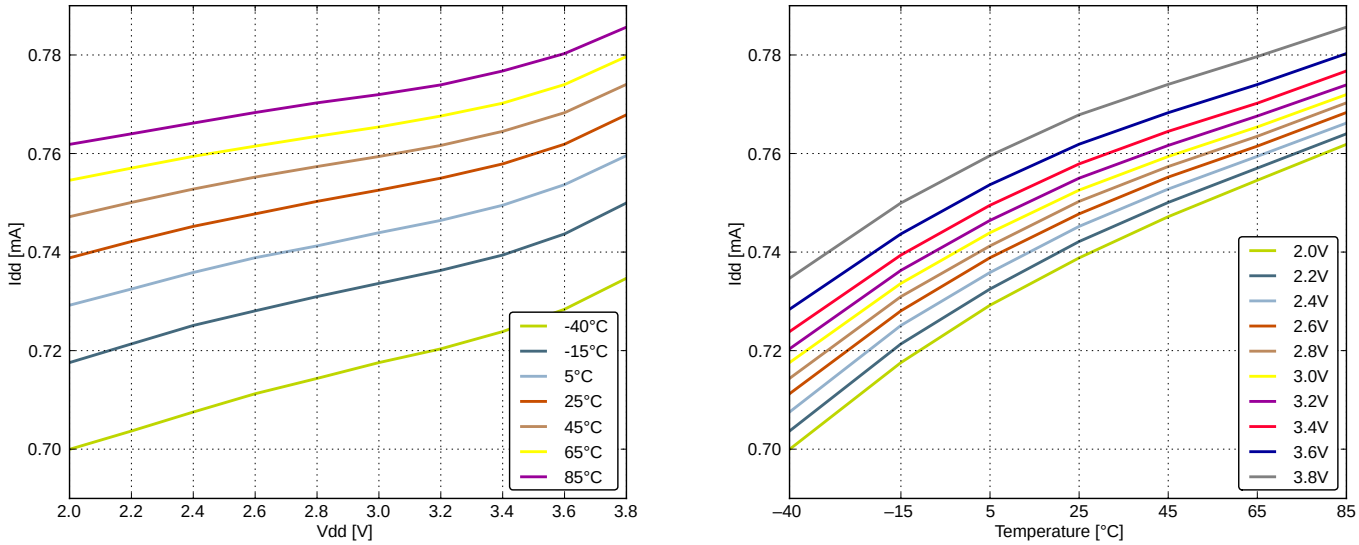



**Figure 4.5. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 11 MHz**

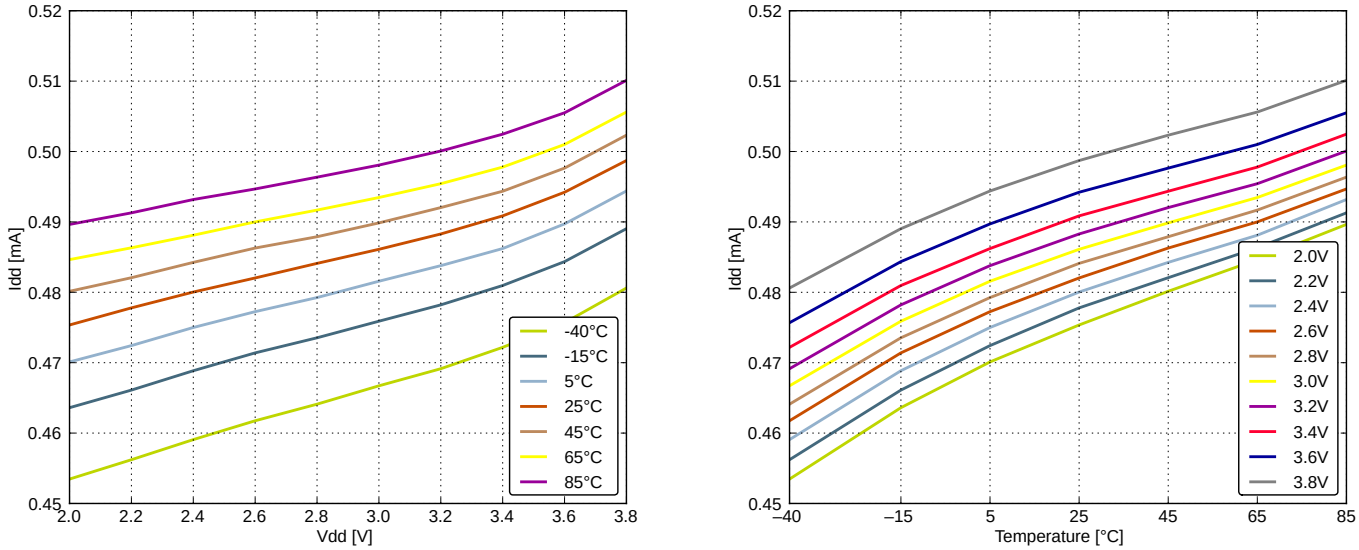
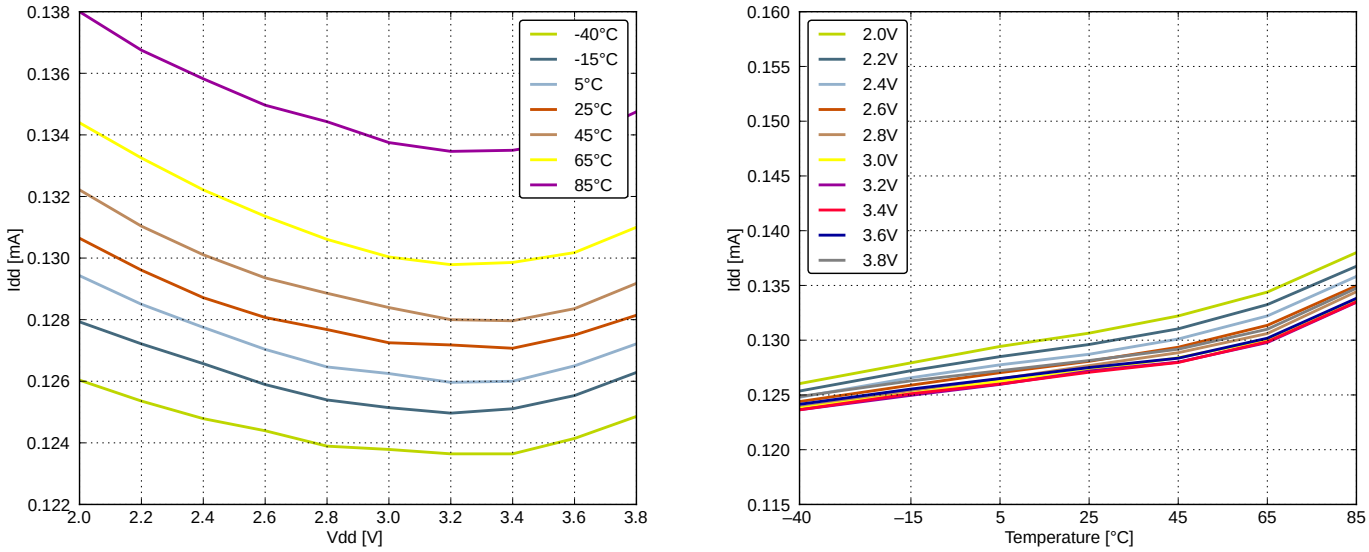



**Figure 4.6. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 6.6 MHz**




### 4.5.2 EM2 Current Consumption

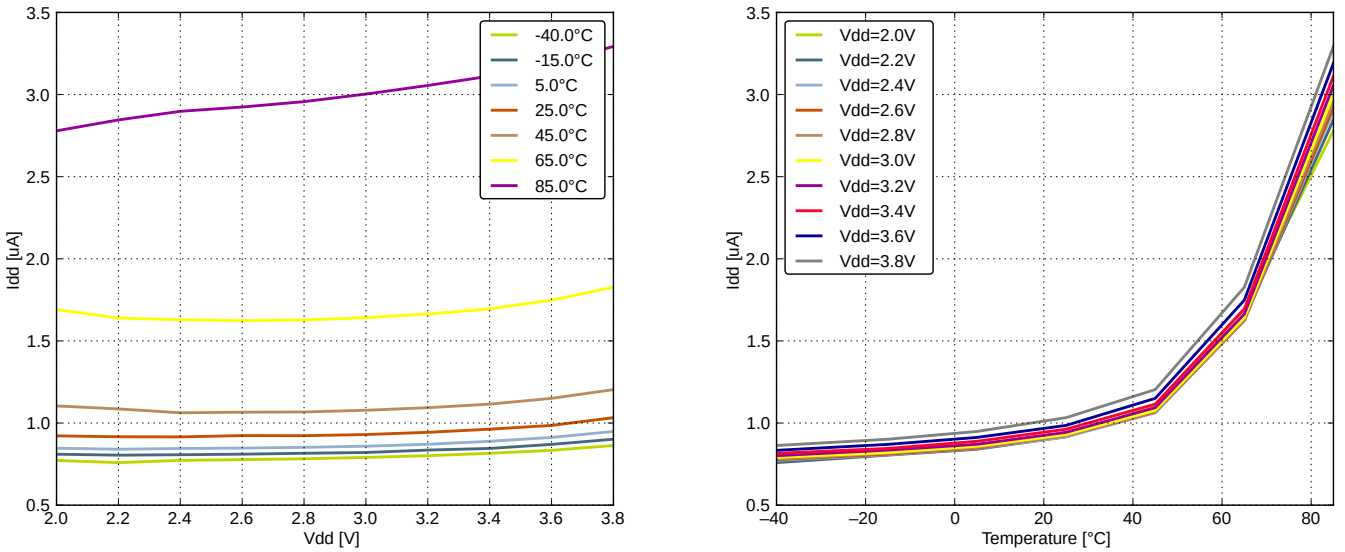



**Figure 4.7. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO**

### 4.5.3 EM3 Current Consumption

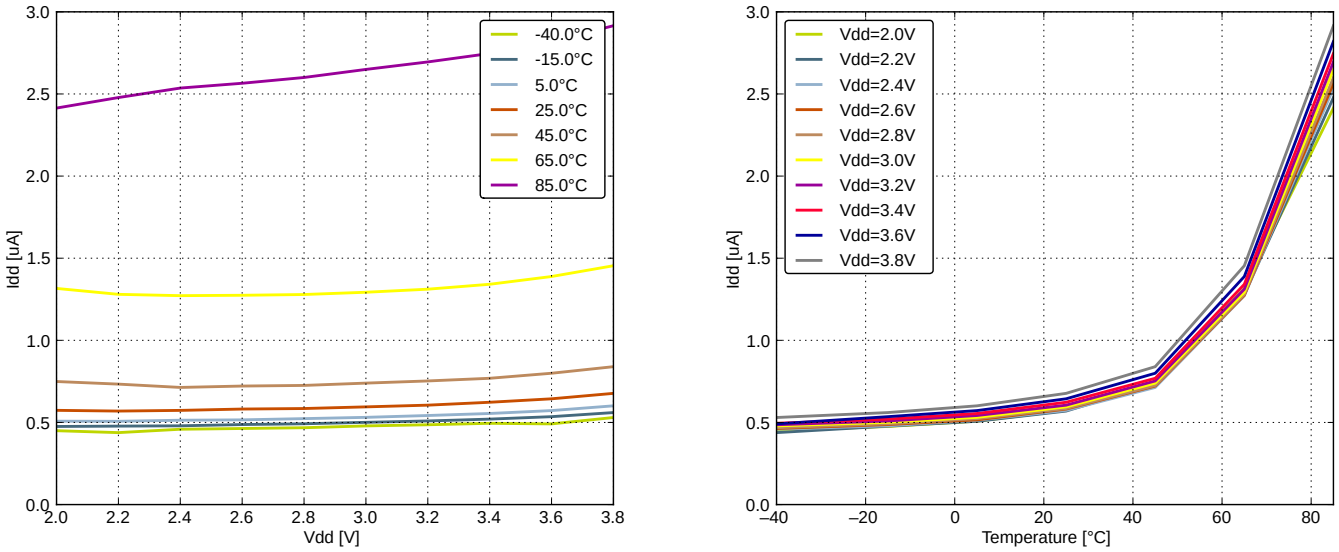



**Figure 4.8. EM3 Current Consumption**

### 4.5.4 EM4 Current Consumption

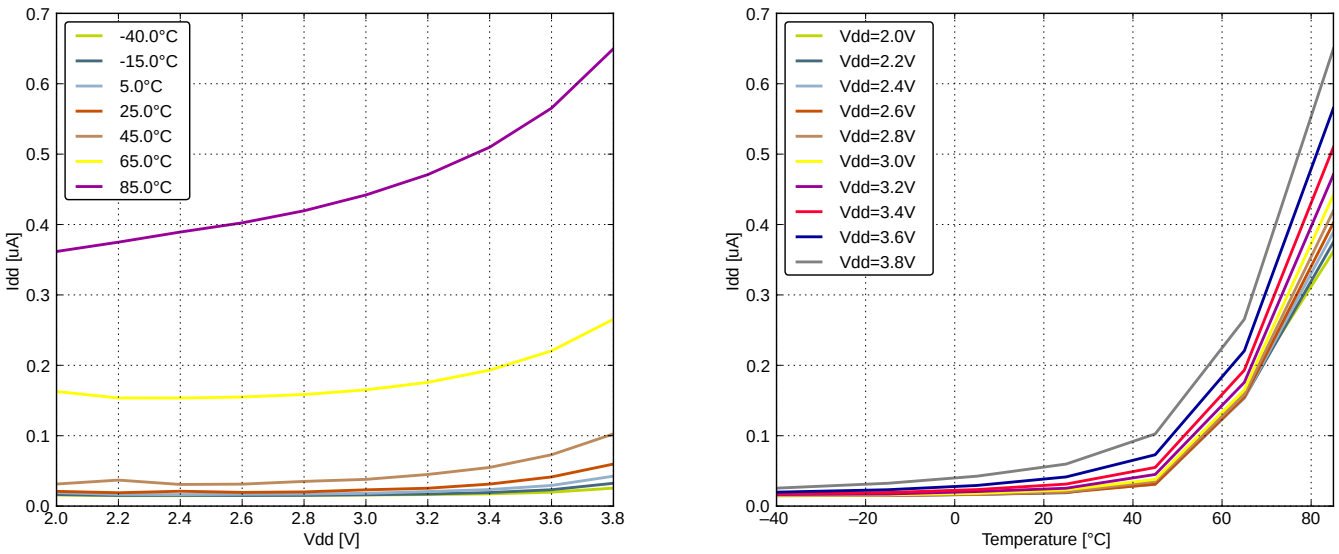



**Figure 4.9. EM4 Current Consumption**

### 4.6 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

**Table 4.5. Energy Modes Transitions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transition time from EM1 to EM0 | $t_{EM10}$ | — | 0 | — | HFCORECLK cycles |
| Transition time from EM2 to EM0 | $t_{EM20}$ | — | 2 | — | µs |
| Transition time from EM3 to EM0 | $t_{EM30}$ | — | 2 | — | µs |
| Transition time from EM4 to EM0 | $t_{EM40}$ | — | 163 | — | µs |

### 4.7 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, *AN0002 EFM32 Hardware Design Considerations*.

**Table 4.6. Power Management**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BOD threshold on falling external supply voltage | $V_{BODextthr-}$ | | 1.74 | — | 1.96 | V |
| BOD threshold on rising external supply voltage | $V_{BODextthr+}$ | | — | 1.85 | 1.98 | V |
| Power-on Reset (POR) threshold on rising external supply voltage | $V_{PORthr+}$ | | — | — | 1.98 | V |
| Delay from reset is released until program execution starts | $t_{RESET}$ | Applies to Power-on Reset, Brown-out Reset and pin reset. | — | 163 | — | µs |
| Voltage regulator decoupling capacitor. | $C_{DECOUPLE}$ | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | — | 1 | — | µF |
| USB voltage regulator out decoupling capacitor. | $C_{USB_VREGO}$ | X5R capacitor recommended. Apply between USB_VREGO pin and GROUND | — | 1 | — | µF |
| USB voltage regulator in decoupling capacitor. | $C_{USB_VREGI}$ | X5R capacitor recommended. Apply between USB_VREGI pin and GROUND | — | 4.7 | — | µF |

## 4.8 Flash

**Table 4.7. Flash**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Flash erase cycles before failure | $EC_{FLASH}$ | | 20000 | — | — | cycles |
| Flash word write cycles between erase | $WWC_{FLASH}$ | | — | — | 2[1] | cycles |
| Flash data retention | $RET_{FLASH}$ | $T_{AMB}$<150 °C | 10000 | — | — | h |
| | | $T_{AMB}$<85 °C | 10 | — | — | years |
| | | $T_{AMB}$<70 °C | 20 | — | — | years |
| Word (32-bit) programming time | $t_{W_PROG}$ | | 20 | — | — | µs |
| Page erase time[2] | $t_{PERASE}$ | | 20.7 | 22.0 | 24.8 | ms |
| Device erase time[3] | $t_{DERASE}$ | | 41.8 | 45.0 | 49.2 | ms |
| Erase current | $I_{ERASE}$ | | — | — | 7[4] | mA |
| Write current | $I_{WRITE}$ | | — | — | 7[4] | mA |
| Supply voltage during flash erase and write | $V_{FLASH}$ | | 1.98 | — | 3.8 | V |

**Note:**

1. There is a maximum of two writes to the same word between each erase due to a physical limitation of the flash. No bit should be written to ‘0’ more than once between erases. To write a word twice between erases, any bit written to ‘0’ by the first write should be written to ‘1’ by the second write. This preserves the specified flash write/erase endurance and does not change the ‘0’ written by the first write.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.
4. Measured at 25 °C.

## 4.9 General Purpose Input Output

**Table 4.8. GPIO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IOIL}$ | | — | — | 0.30×$V_{DD}$ | V |
| Input high voltage | $V_{IOIH}$ | | 0.70×$V_{DD}$ | — | — | V |
| Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | $V_{IOOH}$ | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | 0.80×$V_{DD}$ | — | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | 0.90×$V_{DD}$ | — | V |
| | | Sourcing 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | — | 0.85×$V_{DD}$ | — | V |
| | | Sourcing 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | — | 0.90×$V_{DD}$ | — | V |
| | | Sourcing 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | 0.75×$V_{DD}$ | — | — | V |
| | | Sourcing 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | 0.85×$V_{DD}$ | — | — | V |
| | | Sourcing 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | 0.60×$V_{DD}$ | — | — | V |
| | | Sourcing 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | 0.80×$V_{DD}$ | — | — | V |
| Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | $V_{IOOL}$ | Sinking 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | 0.20×$V_{DD}$ | — | V |
| | | Sinking 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | 0.10×$V_{DD}$ | — | V |
| | | Sinking 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | — | 0.10×$V_{DD}$ | — | V |
| | | Sinking 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | — | 0.05×$V_{DD}$ | — | V |
| | | Sinking 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | — | — | 0.30×$V_{DD}$ | V |
| | | Sinking 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | — | — | 0.20×$V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | — | — | 0.35×$V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | — | — | 0.25×$V_{DD}$ | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{IOLEAK}$ | VSS < Vin < VDD; pin configured as input or disabled, pullup and pull-down are disabled | -40 | ±0.1 | 40 | nA |
| I/O pin pull-up resistor | $R_{PU}$ | | — | 40 | — | kΩ |
| I/O pin pull-down resistor | $R_{PD}$ | | — | 40 | — | kΩ |
| Internal ESD series resistor | $R_{IOESD}$ | | — | 200 | — | Ω |
| Pulse width of pulses to be removed by the glitch suppression filter | $t_{IO-GLITCH}$ | | 10 | — | 50 | ns |
| Output fall time | $t_{IOOF}$ | GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L$=12.5-25pF. | 20+0.1×$C_L$ | — | 250 | ns |
| | | GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L$=350-600pF | 20+0.1×$C_L$ | — | 250 | ns |
| I/O pin hysteresis ($V_{IOTHR+}$ - $V_{IOTHR-}$) | $V_{IOHYST}$ | $V_{DD}$ = 1.98 - 3.8 V | 0.10×$V_{DD}$ | — | — | V |

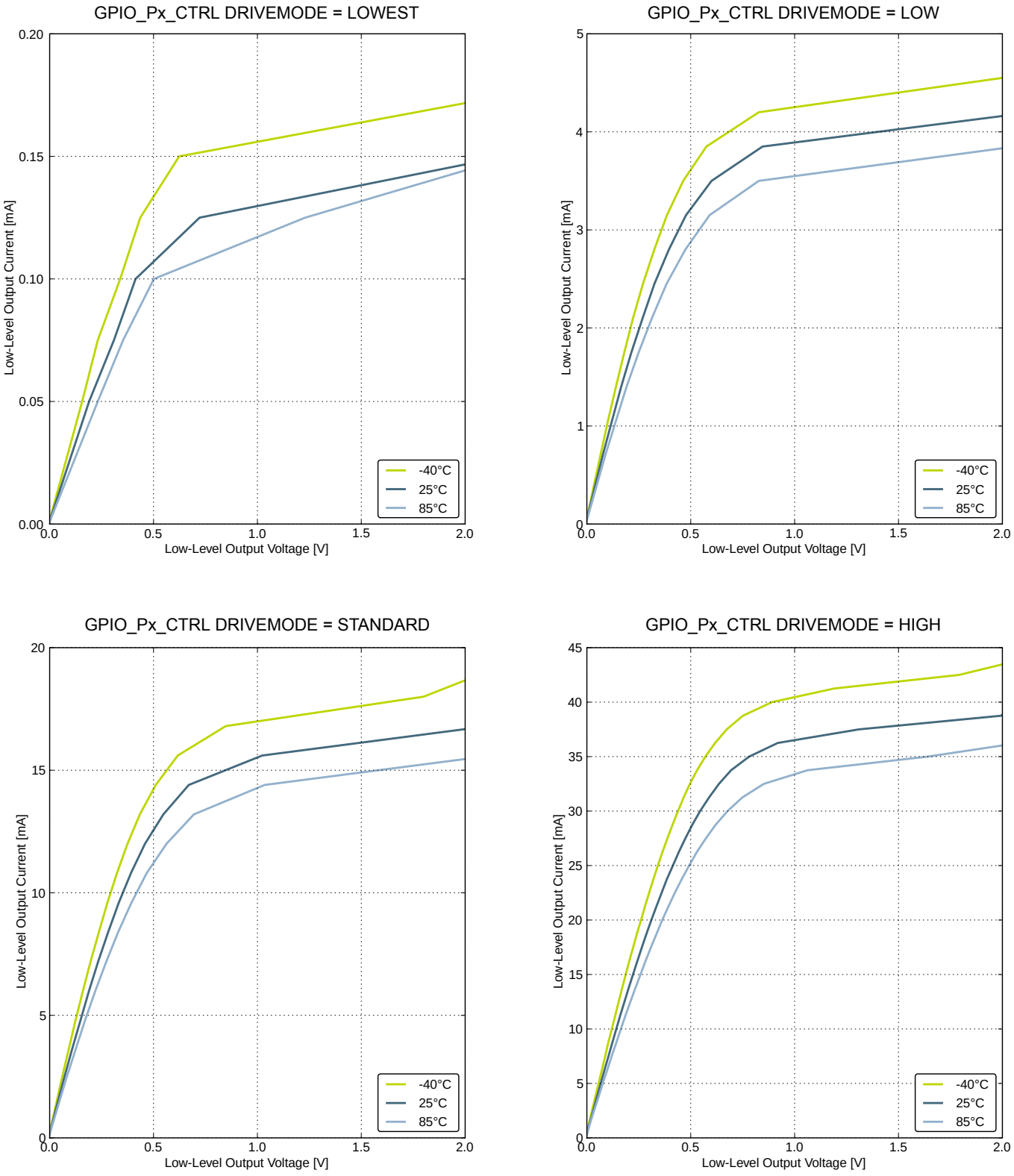



**Figure 4.10. Typical Low-Level Output Current, 2V Supply Voltage**

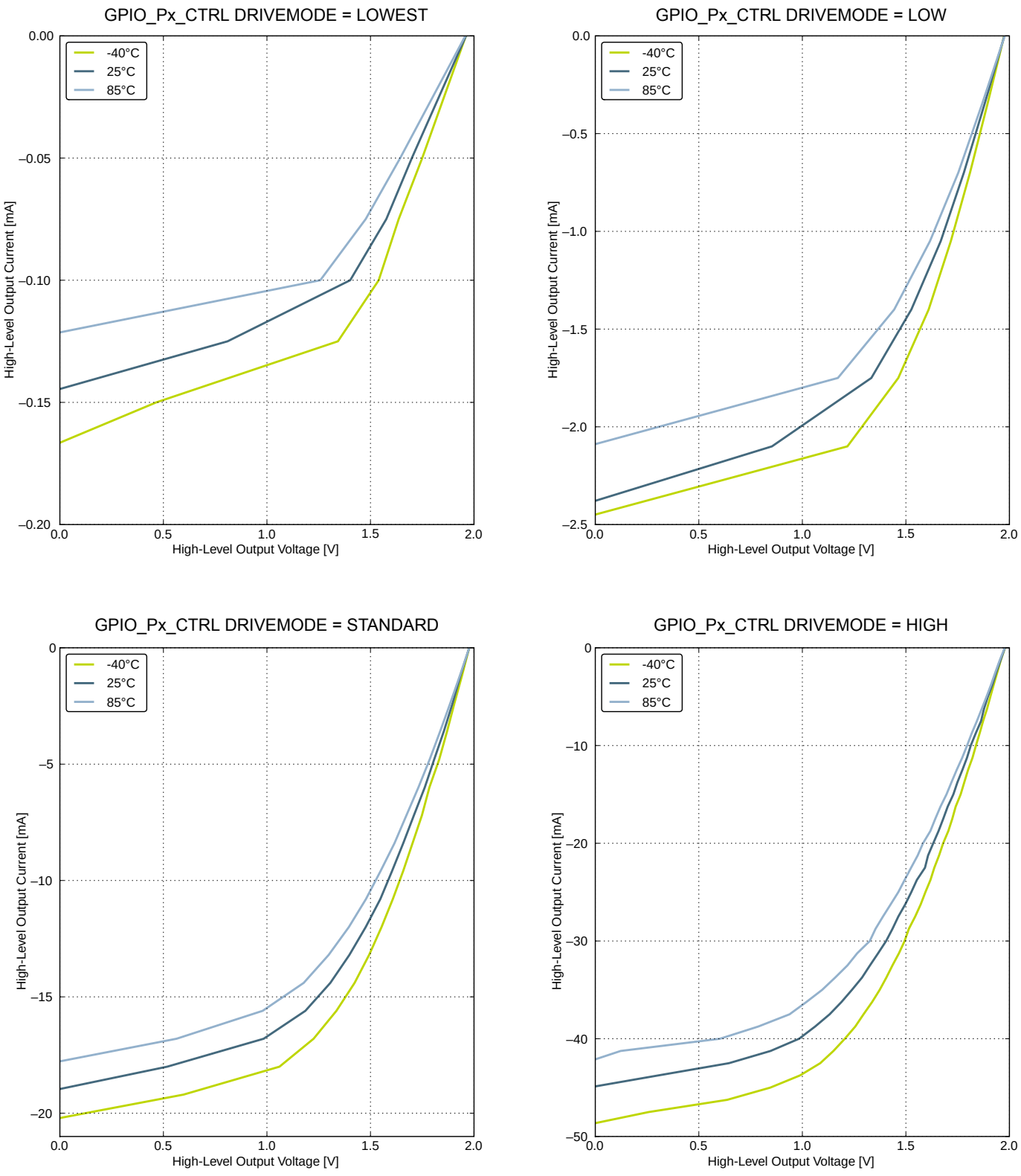



**Figure 4.11. Typical High-Level Output Current, 2 V Supply Voltage**

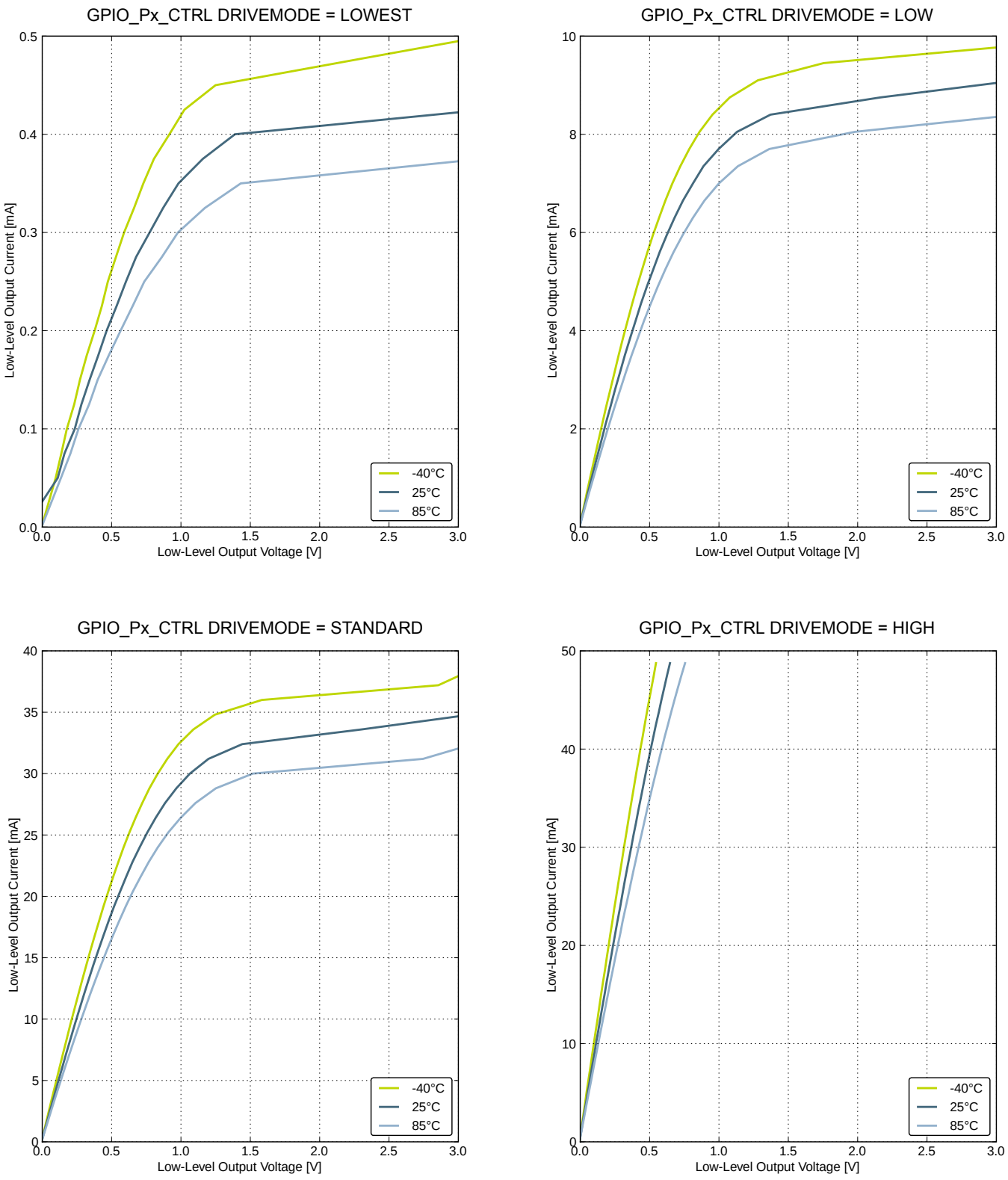



**Figure 4.12. Typical Low-Level Output Current, 3 V Supply Voltage**

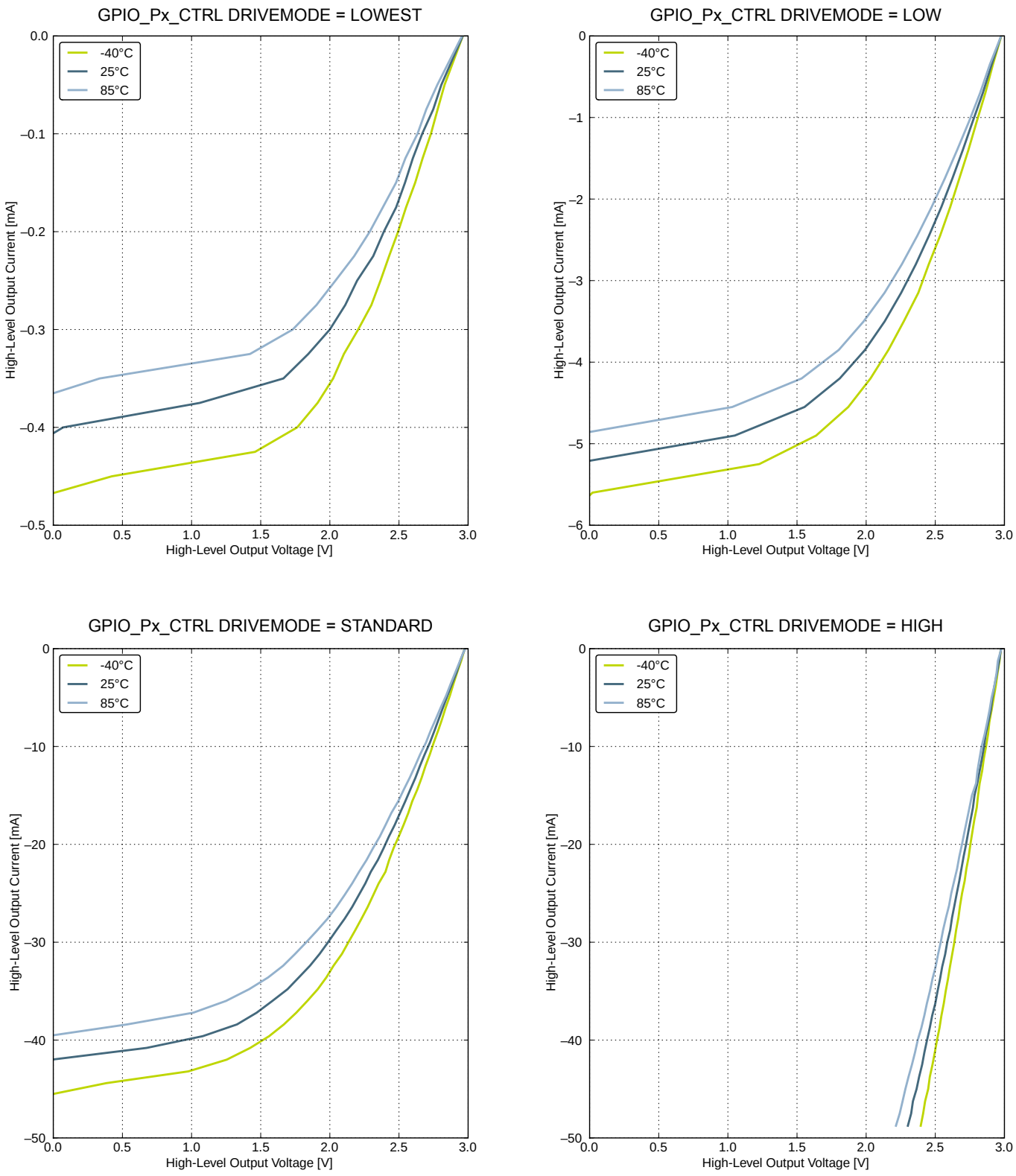



**Figure 4.13. Typical High-Level Output Current, 3 V Supply Voltage**

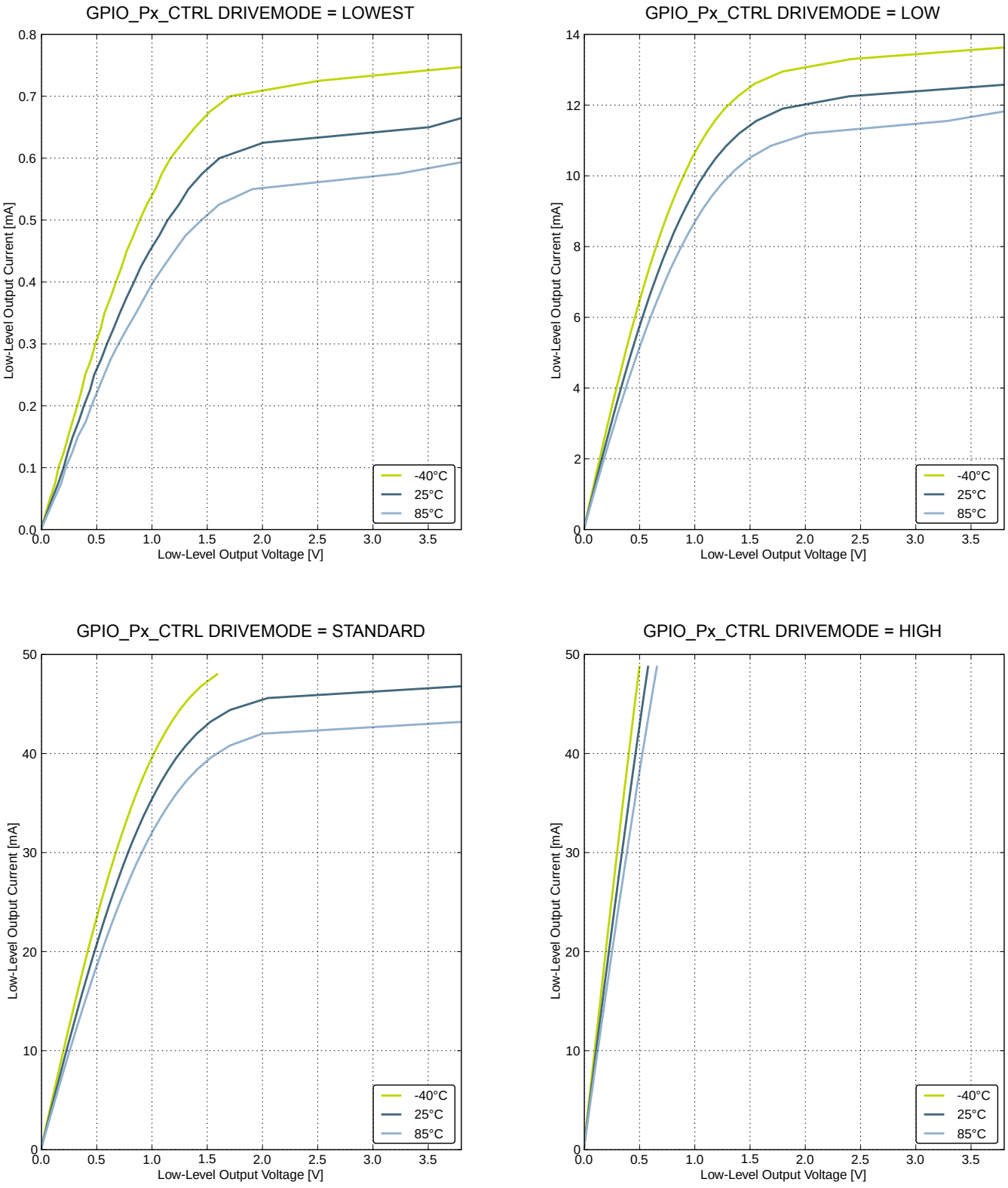



**Figure 4.14. Typical Low-Level Output Current, 3.8 V Supply Voltage**

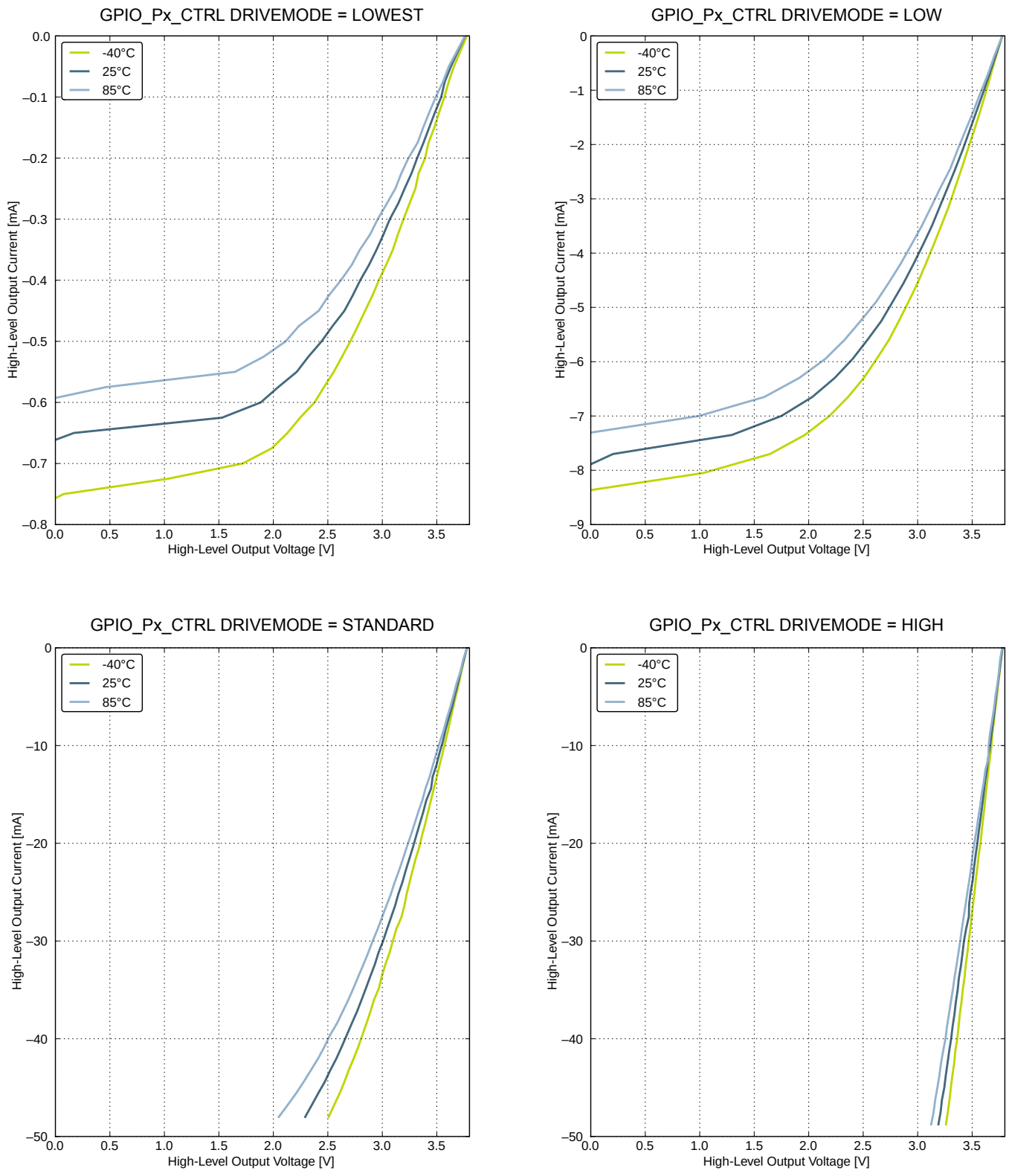



**Figure 4.15. Typical High-Level Output Current, 3.8 V Supply Voltage**

## 4.10 Oscillators

### 4.10.1 LFXO

**Table 4.9. LFXO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supported nominal crystal frequency | $f_{LFXO}$ | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{LFXO}$ | | — | 30 | 120 | kΩ |
| Supported crystal external load range | $C_{LFXOL}$ | | X[1] | — | 25 | pF |
| Current consumption for core and buffer after startup. | $I_{LFXO}$ | ESR=30 kΩ, $C_L$=10 pF, LFXOBOOST in CMU_CTRL is 1 | — | 190 | — | nA |
| Start- up time. | $t_{LFXO}$ | ESR=30 kΩ, CL=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1 | — | 400 | — | ms |

**Note:**
1. See Minimum Load Capacitance ($C_{LFXOL}$) Requirement For Safe Crystal Startup in Configurator in Simplicity Studio.

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note *AN0016 EFM32 Oscillator Design Consideration*.

### 4.10.2 HFXO

**Table 4.10. HFXO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supported nominal crystal Frequency | $f_{HFXO}$ | | 4 | — | 48 | MHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{HFXO}$ | Crystal frequency 48 MHz | — | — | 50 | Ω |
| | | Crystal frequency 32 MHz | — | 30 | 60 | Ω |
| | | Crystal frequency 4 MHz | — | 400 | 1500 | Ω |
| The transconductance of the HFXO input transistor at crystal startup | $g_{mHFXO}$ | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | — | — | mS |
| Supported crystal external load range | $C_{HFXOL}$ | | 5 | — | 25 | pF |
| Current consumption for HFXO after startup | $I_{HFXO}$ | 4 MHz: ESR=400 Ω, $C_L$=20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 85 | — | µA |
| | | 32 MHz: ESR=30 Ω, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 165 | — | µA |
| Startup time | $t_{HFXO}$ | 32 MHz: ESR=30 Ω, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 400 | — | µs |

### 4.10.3 LFRCO

**Table 4.11. LFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{LFRCO}$ | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 31.29 | 32.768 | 34.28 | kHz |
| | | Over full supply and temperature range | 26.0 | 32.768 | 46.2 | kHz |
| Startup time not including software calibration | $t_{LFRCO}$ | | — | 150 | — | µs |
| Current consumption | $I_{LFRCO}$ | | — | 300 | — | nA |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{LFRCO}$ | | — | 1.5 | — | % |
| Voltage drift | $V_{DRIFT}$ | | — | -123291 | — | ppm/V |
| Temperature drift | $T_{DRIFT}$ | | — | 610 | — | ppm/°C |

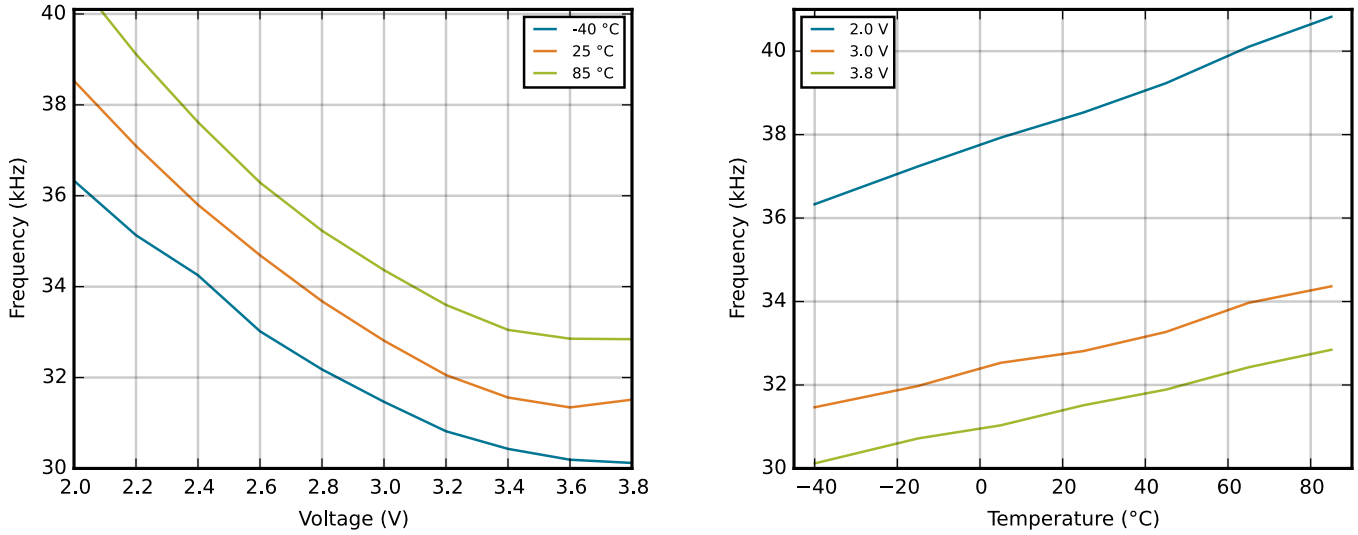



**Figure 4.16. Calibrated LFRCO Frequency vs Temperature and Supply Voltage**

### 4.10.4 HFRCO

**Table 4.12. HFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency, all packages except CSP, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | $f_{HFRCO}$ | $f_{HFRCO}$ = 28 MHz | 27.5 | 28.0 | 28.5 | MHz |
| | | $f_{HFRCO}$ = 21 MHz | 20.6 | 21.0 | 21.4 | MHz |
| | | $f_{HFRCO}$ = 14 MHz | 13.7 | 14.0 | 14.3 | MHz |
| | | $f_{HFRCO}$ = 11 MHz | 10.8 | 11.0 | 11.2 | MHz |
| | | $f_{HFRCO}$ = 6.6 MHz | 6.48[1] | 6.6[1] | 6.72[1] | MHz |
| | | $f_{HFRCO}$ = 1.2 MHz | 1.15[2] | 1.2[2] | 1.25[2] | MHz |
| Oscillation frequency, all packages except CSP, over full supply and temperature range | $f_{HFRCO}$ | $f_{HFRCO}$ = 28 MHz | 24.9 | 28.0 | 31.1 | MHz |
| | | $f_{HFRCO}$ = 21 MHz | 18.8 | 21.0 | 23.3 | MHz |
| | | $f_{HFRCO}$ = 14 MHz | 12.4 | 14.0 | 15.6 | MHz |
| | | $f_{HFRCO}$ = 11 MHz | 9.9 | 11.0 | 12.2 | MHz |
| | | $f_{HFRCO}$ = 6.6 MHz | 5.9[1] | 6.6[1] | 7.4[1] | MHz |
| | | $f_{HFRCO}$ = 1.2 MHz | 0.8[2] | 1.2[2] | 1.6[2] | MHz |
| Oscillation frequency, CSP devices, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | $f_{HFRCO}$ | $f_{HFRCO}$ = 28 MHz | — | 28.0 | — | MHz |
| | | $f_{HFRCO}$ = 21 MHz | — | 21.0 | — | MHz |
| | | $f_{HFRCO}$ = 14 MHz | — | 14.0 | — | MHz |
| | | $f_{HFRCO}$ = 11 MHz | — | 11.0 | — | MHz |
| | | $f_{HFRCO}$ = 6.6 MHz | — | 6.6[1] | — | MHz |
| | | $f_{HFRCO}$ = 1.2 MHz | — | 1.2[2] | — | MHz |
| Oscillation frequency, CSP devices, over full supply and temperature range | $f_{HFRCO}$ | $f_{HFRCO}$ = 28 MHz | — | 28.0 | — | MHz |
| | | $f_{HFRCO}$ = 21 MHz | — | 21.0 | — | MHz |
| | | $f_{HFRCO}$ = 14 MHz | — | 14.0 | — | MHz |
| | | $f_{HFRCO}$ = 11 MHz | — | 11.0 | — | MHz |
| | | $f_{HFRCO}$ = 6.6 MHz | — | 6.6[1] | — | MHz |
| | | $f_{HFRCO}$ = 1.2 MHz | — | 1.2[2] | — | MHz |
| Settling time after start-up | $t_{HFRCO_settling}$ | $f_{HFRCO}$ = 14 MHz | — | 0.6 | — | Cycles |
| Current consumption | $I_{HFRCO}$ | $f_{HFRCO}$ = 28 MHz | — | 165 | 215 | µA |
| | | $f_{HFRCO}$ = 21 MHz | — | 134 | 175 | µA |
| | | $f_{HFRCO}$ = 14 MHz | — | 106 | 140 | µA |
| | | $f_{HFRCO}$ = 11 MHz | — | 94 | 125 | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | — | 77 | 105 | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | — | 25 | 40 | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Voltage drift | $V_{HFRCO_DRIFT}$ | $f_{HFRCO}$ = 28 MHz | — | 10768 | — | ppm/V |
| | | $f_{HFRCO}$ = 21 MHz | — | 8939 | — | ppm/V |
| | | $f_{HFRCO}$ = 14 MHz | — | 8040 | — | ppm/V |
| | | $f_{HFRCO}$ = 11 MHz | — | 7719 | — | ppm/V |
| | | $f_{HFRCO}$ = 6.6 MHz | — | 8491 | — | ppm/V |
| | | $f_{HFRCO}$ = 1.2 MHz | — | -124035 | — | ppm/V |
| Temperature drift | $T_{HFRCO_DRIFT}$ | $f_{HFRCO}$ = 28 MHz | — | 91 | — | ppm/°C |
| | | $f_{HFRCO}$ = 21 MHz | — | 88 | — | ppm/°C |
| | | $f_{HFRCO}$ = 14 MHz | — | 43 | — | ppm/°C |
| | | $f_{HFRCO}$ = 11 MHz | — | 50 | — | ppm/°C |
| | | $f_{HFRCO}$ = 6.6 MHz | — | -50 | — | ppm/°C |
| | | $f_{HFRCO}$ = 1.2 MHz | — | 83 | — | ppm/°C |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{HFRCO}$ | | — | 0.3[3] | — | % |

**Note:**

1. For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.
2. For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.
3. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

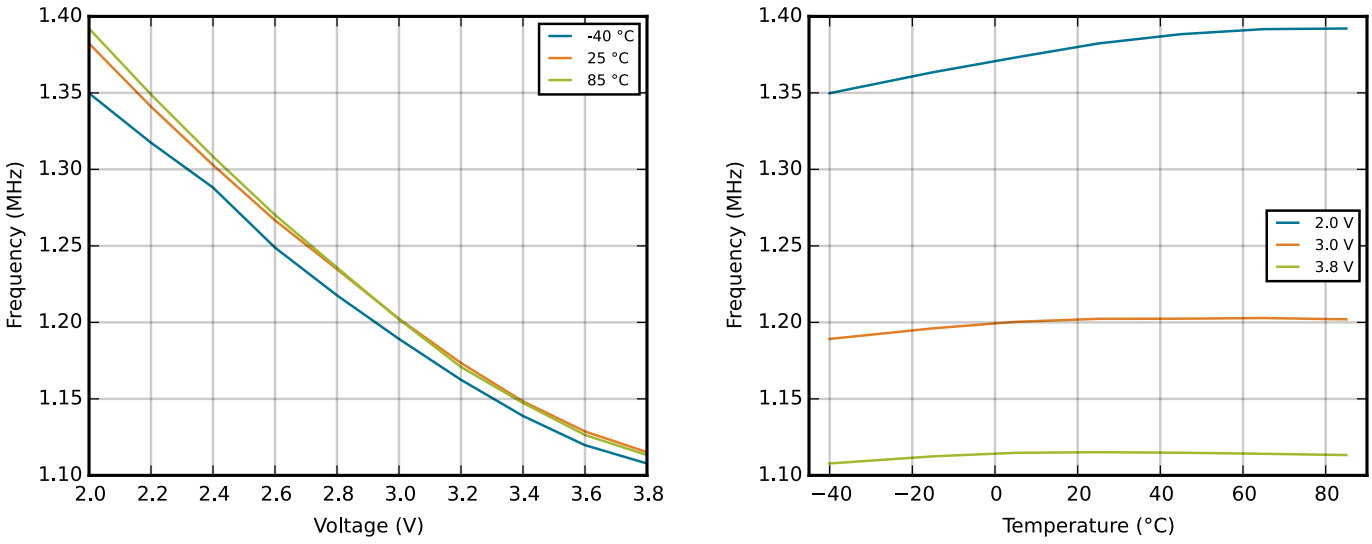



**Figure 4.17. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature**

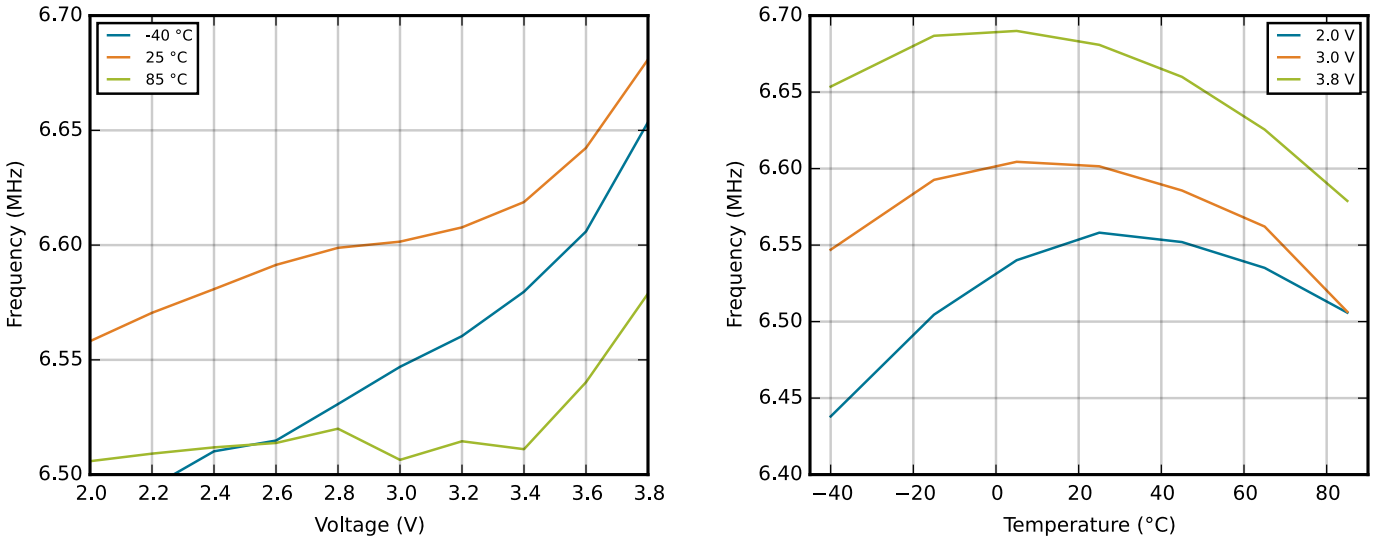



**Figure 4.18. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature**

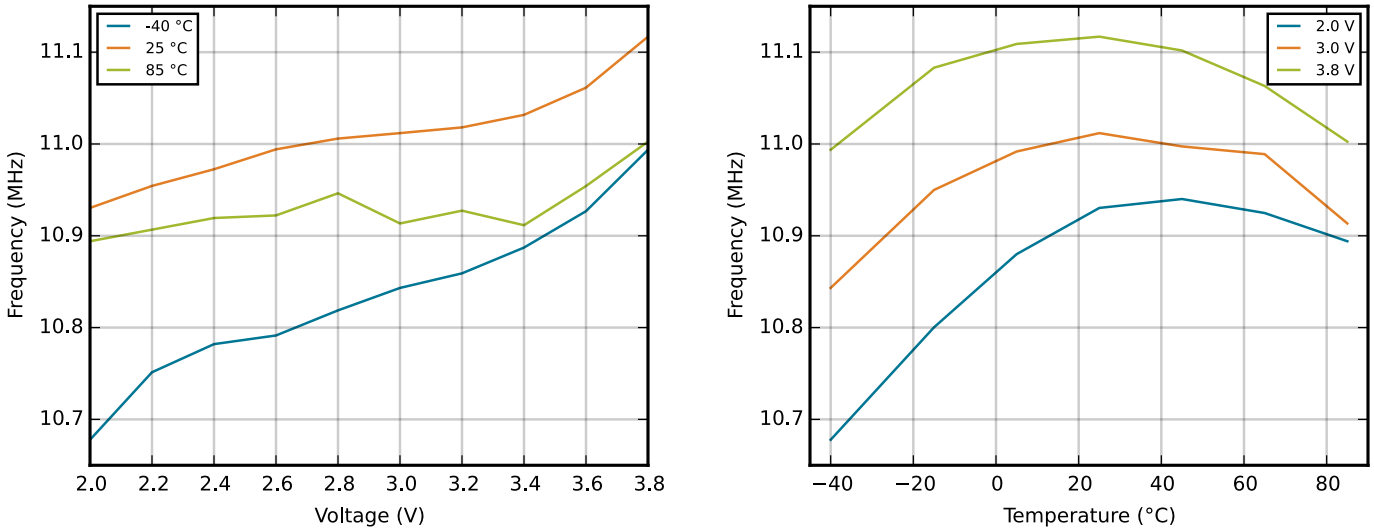



**Figure 4.19. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**

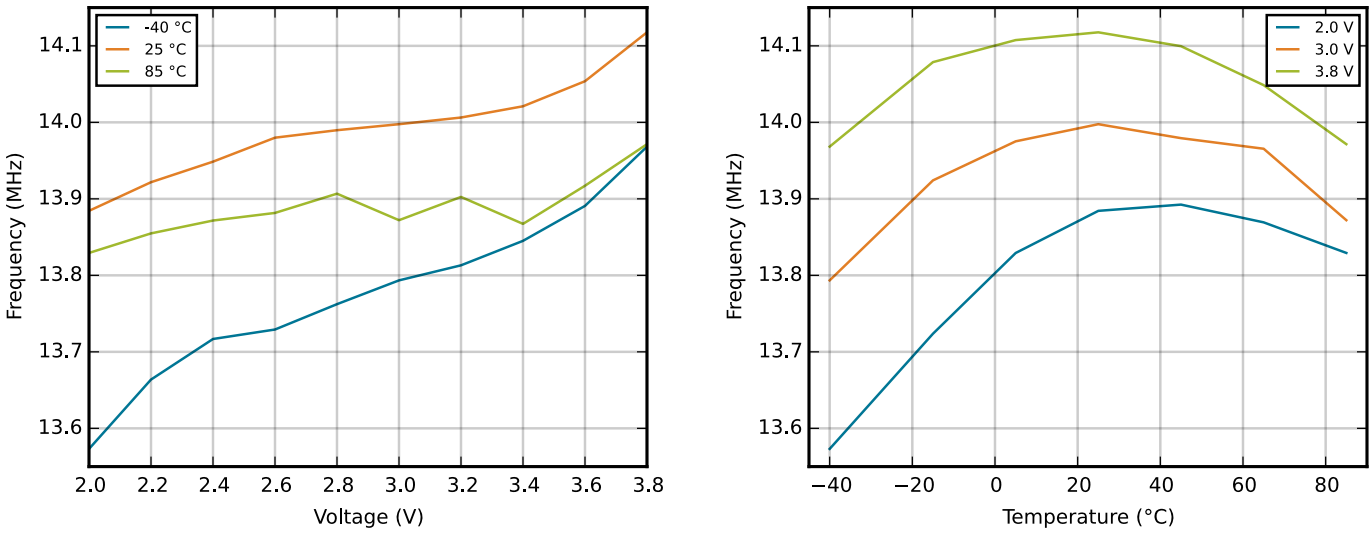



**Figure 4.20. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature**

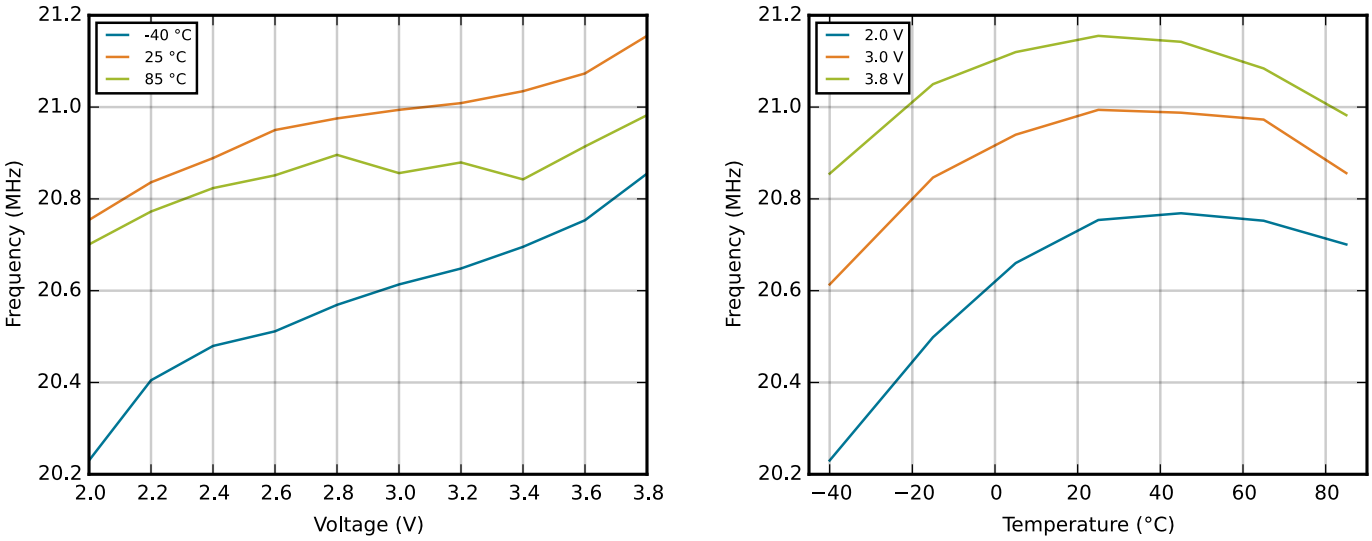



**Figure 4.21. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature**

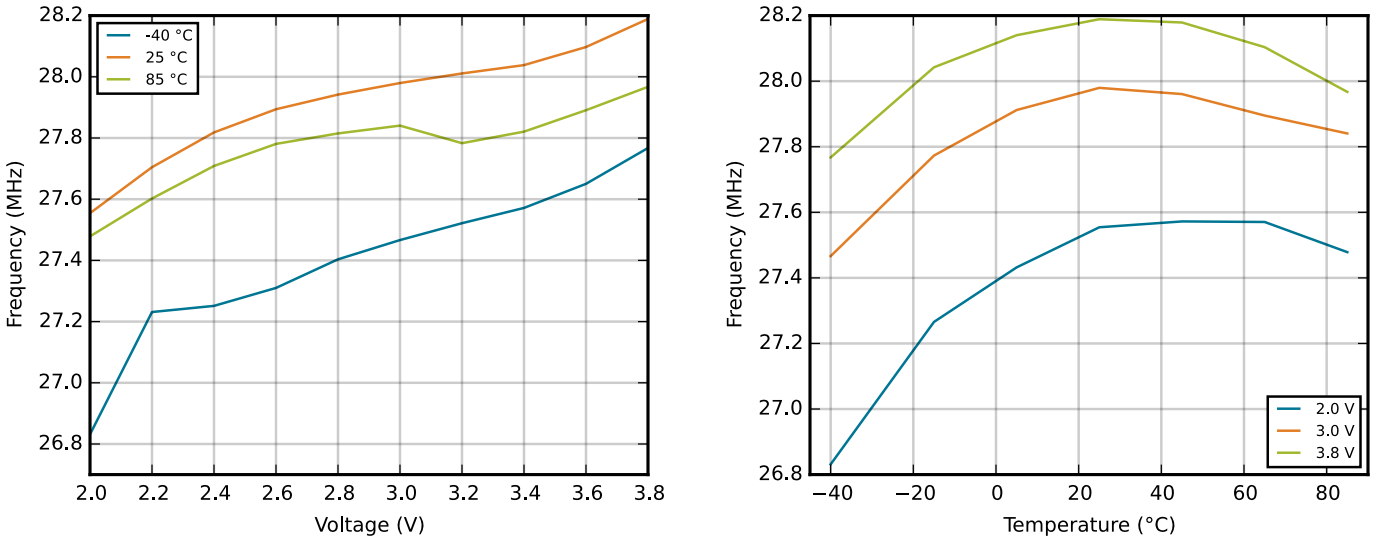



**Figure 4.22. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature**

### 4.10.5 AUXHFRCO

**Table 4.13. AUXHFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency, all packages except CSP, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | $f_{AUXHFRCO}$ | $f_{AUXHFRCO}$ = 28 MHz | 27.5 | 28.0 | 28.5 | MHz |
| | | $f_{AUXHFRCO}$ = 21 MHz | 20.6 | 21.0 | 21.4 | MHz |
| | | $f_{AUXHFRCO}$ = 14 MHz | 13.7 | 14.0 | 14.3 | MHz |
| | | $f_{AUXHFRCO}$ = 11 MHz | 10.8 | 11.0 | 11.2 | MHz |
| | | $f_{AUXHFRCO}$ = 6.6 MHz | 6.48[1] | 6.60[1] | 6.72[1] | MHz |
| | | $f_{AUXHFRCO}$ = 1.2 MHz | 1.15[2] | 1.20[2] | 1.25[2] | MHz |
| Oscillation frequency, CSP devices, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | $f_{AUXHFRCO}$ | $f_{AUXHFRCO}$ = 28 MHz | — | 28.0 | — | MHz |
| | | $f_{AUXHFRCO}$ = 21 MHz | — | 21.0 | — | MHz |
| | | $f_{AUXHFRCO}$ = 14 MHz | — | 14.0 | — | MHz |
| | | $f_{AUXHFRCO}$ = 11 MHz | — | 11.0 | — | MHz |
| | | $f_{AUXHFRCO}$ = 6.6 MHz | — | 6.60[1] | — | MHz |
| | | $f_{AUXHFRCO}$ = 1.2 MHz | — | 1.20[2] | — | MHz |
| Settling time after start-up | $t_{AUXHFRCO_settling}$ | $f_{AUXHFRCO}$ = 14 MHz | — | 0.6 | — | Cycles |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{AUXHFRCO}$ | | — | 0.3[3] | — | % |

**Note:**

1. For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.
2. For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.
3. The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

### 4.10.6 ULFRCO

**Table 4.14. ULFRCO**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{ULFRCO}$ | 25°C, 3V | 0.7 | — | 1.75 | kHz |
| Temperature coefficient | $TC_{ULFRCO}$ | | — | 0.05 | — | %/°C |
| Supply voltage coefficient | $VC_{ULFRCO}$ | | — | -18.2 | — | %/V |

## 4.11 Analog Digital Converter (ADC)

**Table 4.15. ADC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{ADCIN}$ | Single ended | 0 | — | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | — | $V_{REF}/2$ | V |
| Input range of external reference voltage, single ended and differential | $V_{ADCREFIN}$ | | 1.25 | — | $V_{DD}$ | V |
| Input range of external negative reference voltage on channel 7 | $V_{ADCREFIN_CH7}$ | See $V_{ADCREFIN}$ | 0 | — | $V_{DD}$ - 1.1 | V |
| Input range of external positive reference voltage on channel 6 | $V_{ADCREFIN_CH6}$ | See $V_{ADCREFIN}$ | 0.625 | — | $V_{DD}$ | V |
| Common mode input range | $V_{ADCCMIN}$ | | 0 | — | $V_{DD}$ | V |
| Input current | $I_{ADCIN}$ | 2 pF sampling capacitors | — | <100 | — | nA |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | | — | 65 | — | dB |
| Average active current | $I_{ADC}$ | 1 MSamples/s, 12 bit, external reference | — | 351 [1] | — | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00 | — | 67 [1] | — | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01 | — | 63 [1] | — | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10 | — | 64 [1] | — | µA |
| Input capacitance | $C_{ADCIN}$ | | — | 2 | — | pF |
| Input ON resistance | $R_{ADCIN}$ | | 1 | — | — | MΩ |
| Input RC filter resistance | $R_{ADCFILT}$ | | — | 10 | — | kΩ |
| Input RC filter/decoupling capacitance | $C_{ADCFILT}$ | | — | 250 | — | fF |
| Input bias current | $I_{ADCBIASIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| Input offset current | $I_{ADCOFFSETIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| ADC Clock Frequency | $f_{ADCCLK}$ | | — | — | 13 | MHz |
| Conversion time | $t_{ADCCONV}$ | 6 bit | 7 | — | — | ADCCLK Cycles |
| | | 8 bit | 11 | — | — | ADCCLK Cycles |
| | | 12 bit | 13 | — | — | ADCCLK Cycles |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Acquisition time | $t_{ADCACQ}$ | Programmable | 1 | — | 256 | ADCCLK Cycles |
| Required acquisition time for VDD/3 reference | $t_{ADCACQVDD3}$ | | 2 | — | — | µs |
| Startup time of reference generator and ADC core | $t_{ADCSTART}$ | NORMAL mode | — | 5 | — | µs |
| | | KEEPADCWARM mode | — | 1 | — | µs |
| Signal-to-Noise Ratio (SNR) | $SNR_{ADC}$ | 1 MSamples/s, 12 bit, single ended, internal 1.25 V reference | — | 59 | — | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5 V reference | — | 63 | — | dB |
| | | 1 MSamples/s, 12 bit, single ended, VDD reference | — | 65 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference | — | 60 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference | — | 65 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference | — | 54 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, VDD reference | — | 67 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 2xVDD reference | — | 69 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25 V reference | — | 62 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5 V reference | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, VDD reference | — | 67 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 5 V reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, VDD reference | 63 | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 2xVDD reference | — | 70 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal-to-Noise And Distortion Ratio (SINAD) | $SINAD_{ADC}$ | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | — | 58 | — | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5 V reference | — | 62 | — | dB |
| | | 1 MSamples/s, 12 bit, single ended, VDD reference | — | 64 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference | — | 60 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference | — | 64 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference | — | 54 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, VDD reference | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 2xVDD reference | — | 68 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25 V reference | — | 61 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5 V reference | — | 65 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, VDD reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, VDD reference | 62 | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 2xVDD reference | — | 69 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious-Free Dynamic Range (SFDR) | $SFDR_{ADC}$ | 1 MSamples/s, 12 bit, single ended, internal 1.25 V reference | — | 64 | — | dBc |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5 V reference | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, single ended, VDD reference | — | 73 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference | — | 66 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference | — | 77 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, VDD reference | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, 2xVDD reference | — | 75 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference | — | 69 | — | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25 V reference | — | 75 | — | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5 V reference | — | 75 | — | dBc |
| | | 200 kSamples/s, 12 bit, single ended, VDD reference | — | 76 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5 V reference | — | 78 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, VDD reference | 68 | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2xVDD reference | — | 79 | — | dBc |
| Offset voltage | $V_{ADCOFFSET}$ | After calibration, single ended | -3.5 | 0.3 | 3 | mV |
| | | After calibration, differential | — | 0.3 | — | mV |
| Thermometer output gradient | $TGRAD_{ADCTH}$ | | — | -1.92 | — | mV/°C |
| | | | — | -6.3 | — | ADC Codes/°C |
| Differential non-linearity (DNL) | $DNL_{ADC}$ | $V_{DD}$= 3.0 V, external 2.5V reference | -1 | ±0.7 | 4 | LSB |
| Integral non-linearity (INL), End point method | $INL_{ADC}$ | $V_{DD}$= 3.0 V, external 2.5V reference | — | ±1.2 | ±3 | LSB |
| Missing codes | $MC_{ADC}$ | | 11.999 [2] | 12 | — | bits |
| Gain error drift | $GAIN_{ED}$ | 1.25 V reference | — | 0.01 [3] | 0.033 [4] | %/°C |
| | | 2.5 V reference | — | 0.01 [3] | 0.03 [4] | %/°C |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset error drift | $OFFSET_{ED}$ | 1.25 V reference | — | 0.2 [3] | 0.7 [4] | LSB/°C |
| | | 2.5 V reference | — | 0.2 [3] | 0.62 [4] | LSB/°C |
| VREF voltage | $V_{REF}$ | 1.25 V reference | 1.2 | 1.25 | 1.3 | V |
| | | 2.5 V reference | 2.4 | 2.5 | 2.6 | V |
| VREF voltage drift | $V_{REF_VDRIFT}$ | 1.25 V reference | -12.4 | 2.9 | 18.2 | mV/V |
| | | 2.5 V reference, VDD > 2.5 V | -24.6 | 5.7 | 35.2 | mV/V |
| VREF temperature drift | $V_{REF_TDRIFT}$ | 1.25 V reference | -132 | 272 | 677 | µV/°C |
| | | 2.5 V reference | -231 | 545 | 1271 | µV/°C |
| VREF current consumption | $I_{VREF}$ | 1.25 V reference | — | 67 | 114 | µA |
| | | 2.5 V reference | — | 55 | 82 | µA |
| ADC and DAC VREF matching | $V_{REF_MATCH}$ | 1.25 V reference | — | 99.85 | — | % |
| | | 2.5 V reference | — | 100.01 | — | % |

**Note:**

1. Includes required contribution from the voltage reference.
2. On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value inthe set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonicat all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is-missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scalein-put for chips that have the missing code issue.
3. Typical numbers given by abs(Mean) / (85 - 25).
4. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in the following two figures.

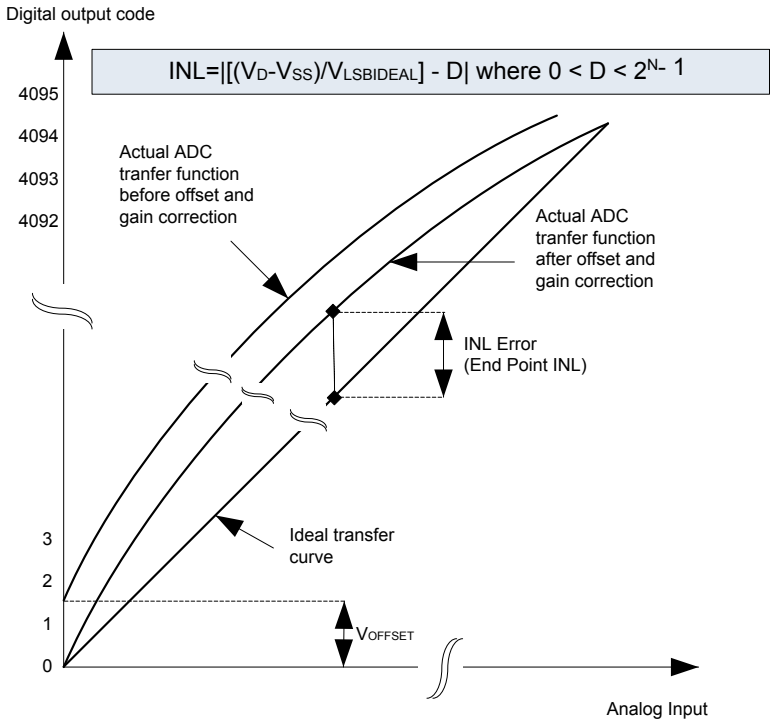



**Figure 4.23. Integral Non-Linearity (INL)**

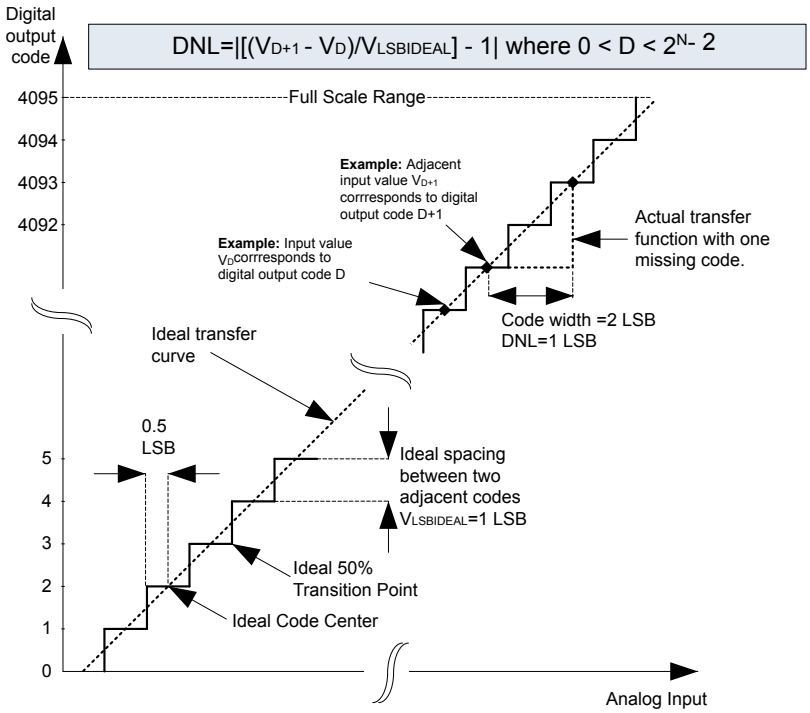



**Figure 4.24. Differential Non-Linearity (DNL)**

### 4.11.1 Typical Performance

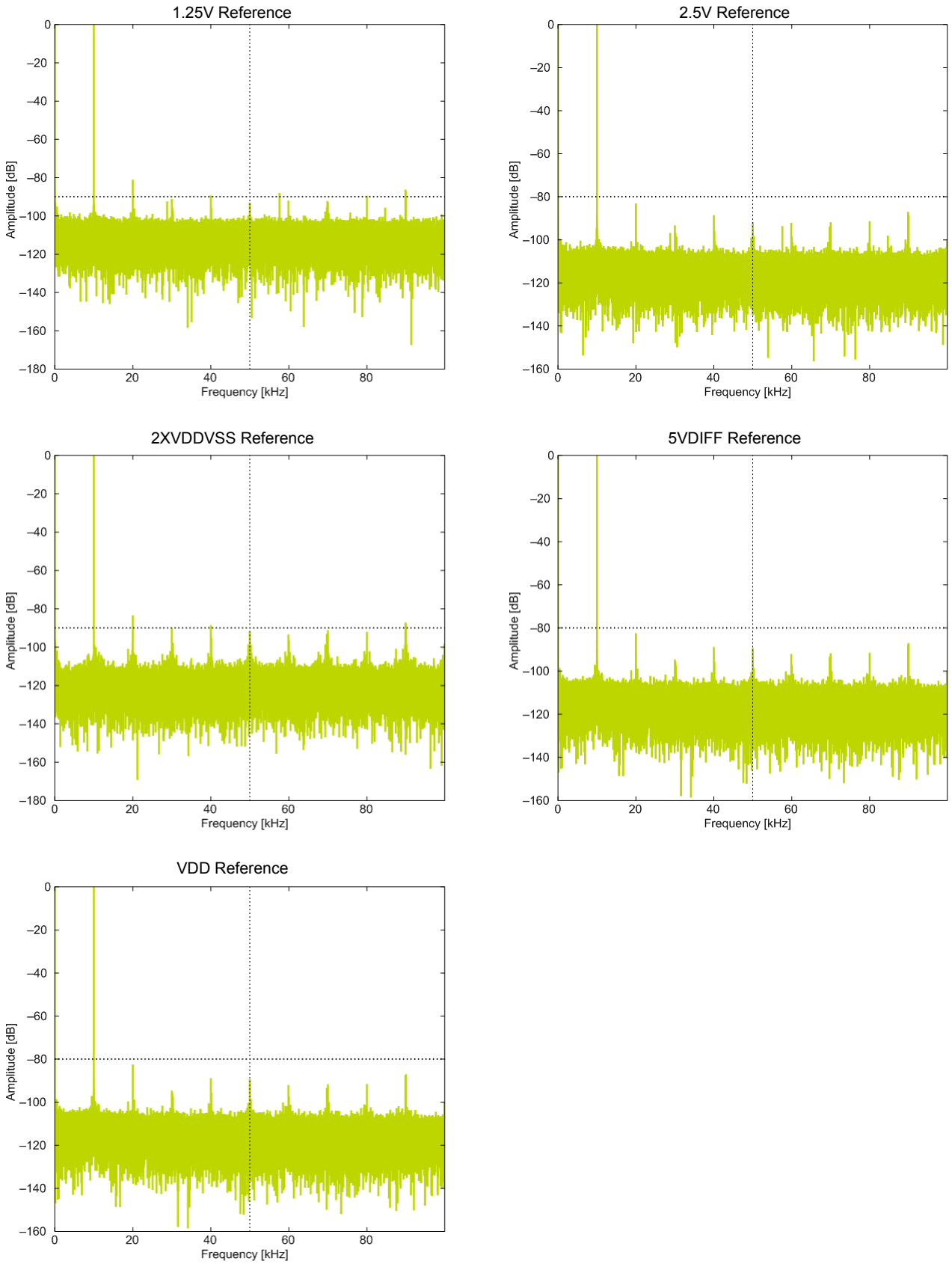



**Figure 4.25. ADC Frequency Spectrum, VDD = 3 V, Temp = 25 °C**

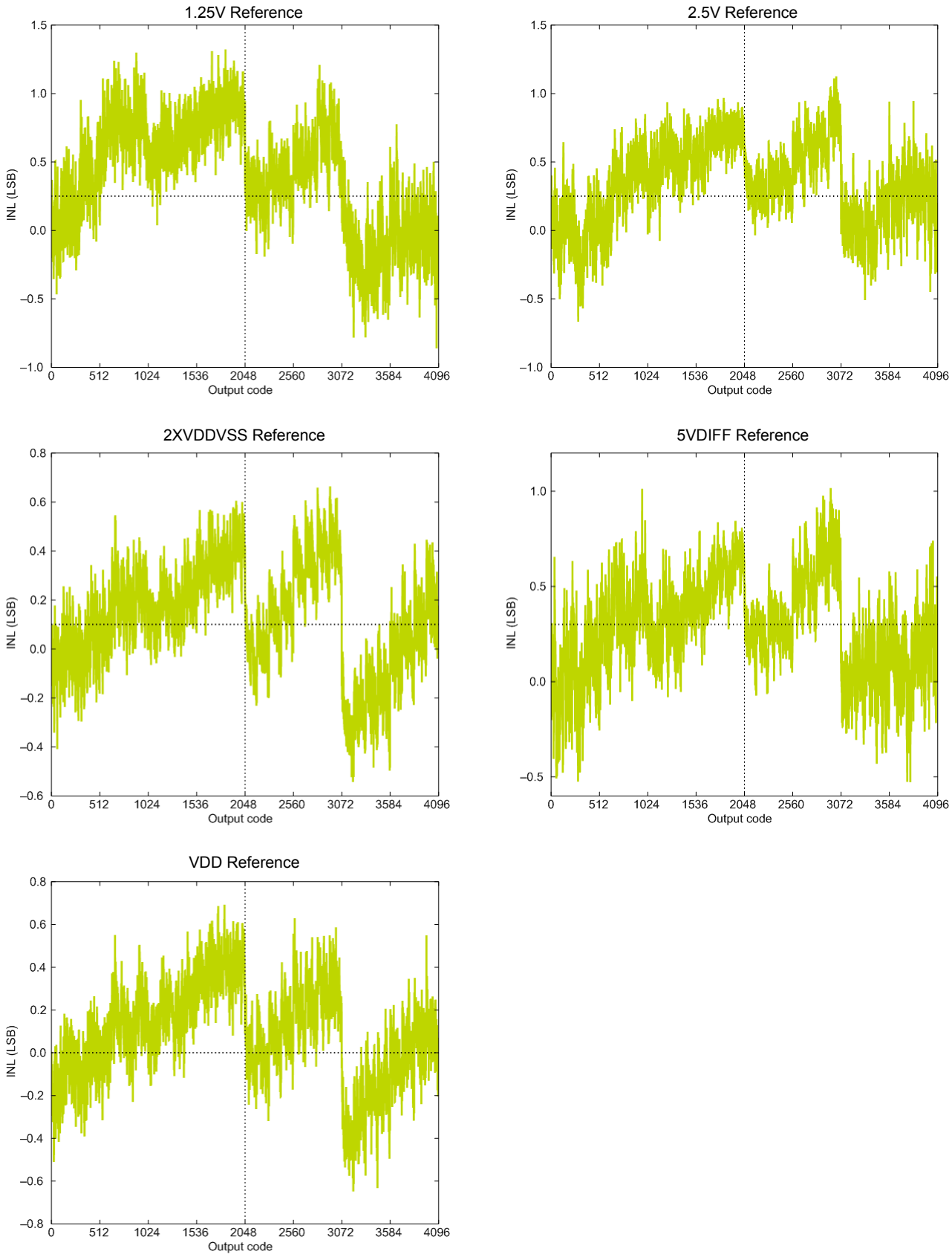



**Figure 4.26. ADC Integral Linearity Error vs Code, VDD = 3 V, Temp = 25 °C**

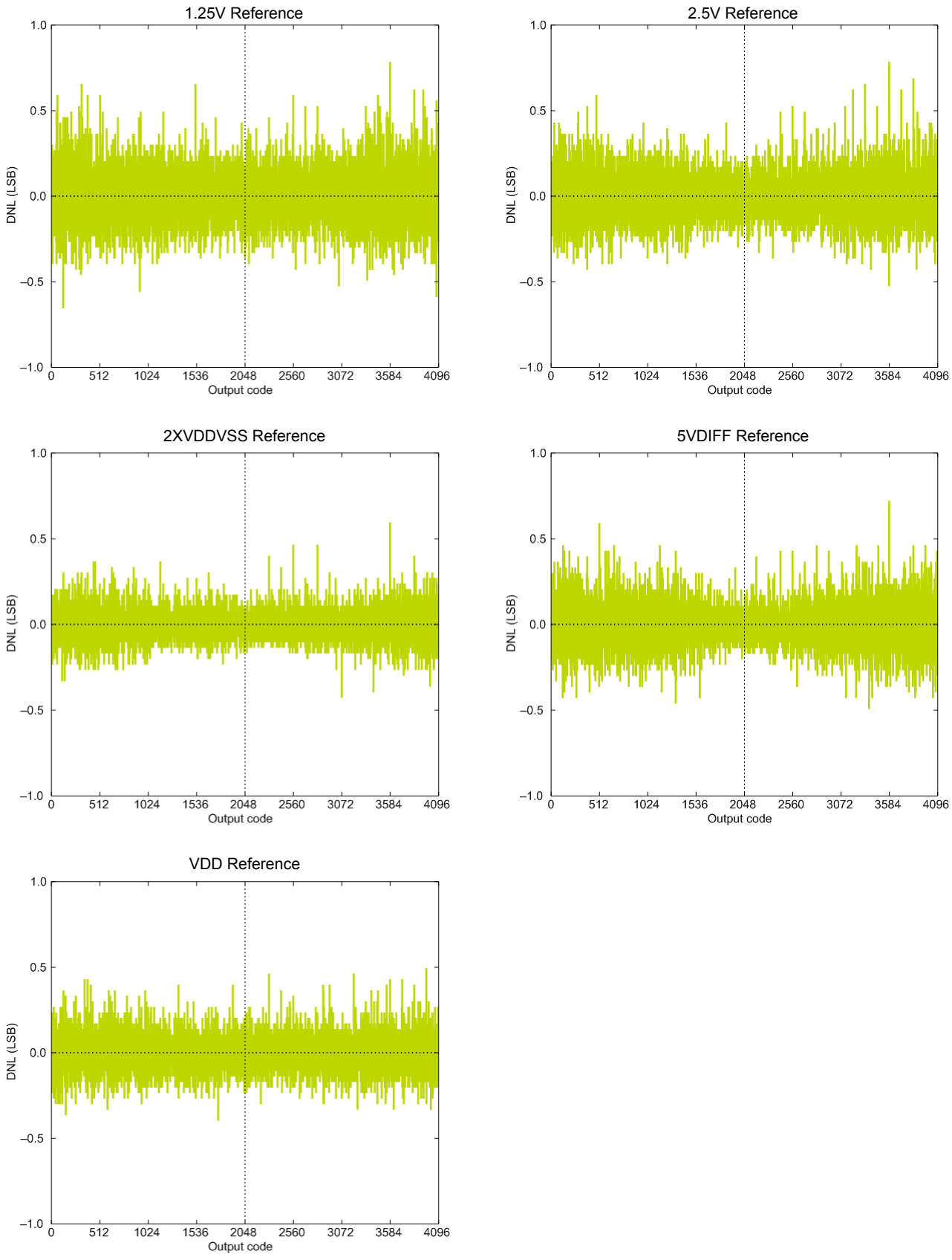



**Figure 4.27. ADC Differential Linearity Error vs Code, VDD = 3 V, Temp = 25 °C**

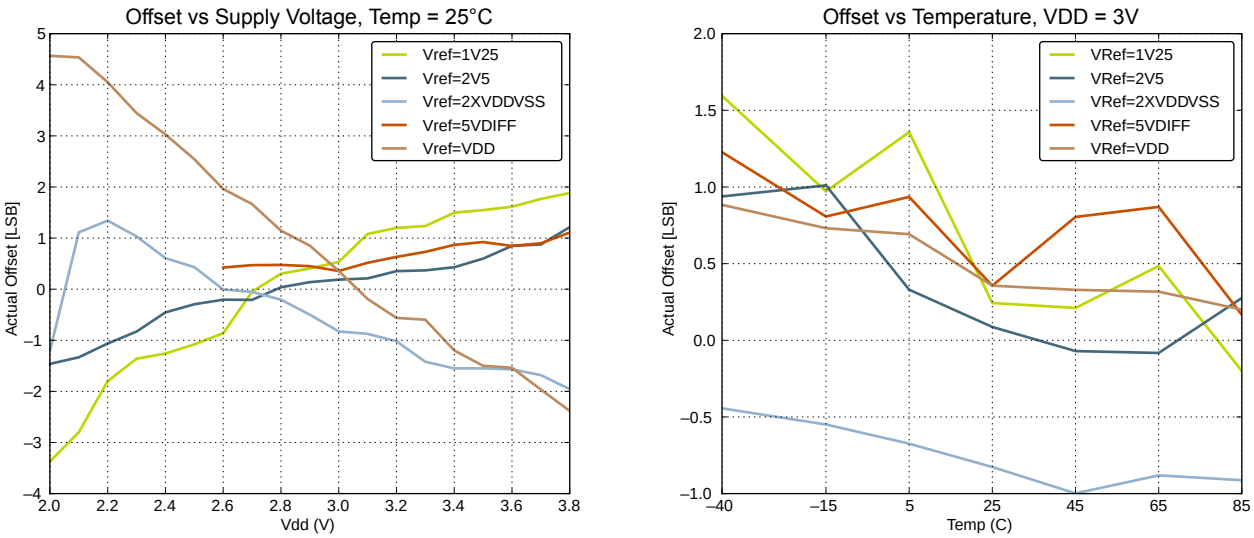



**Figure 4.28. ADC Absolute Offset, Common Mode = VDD/2**

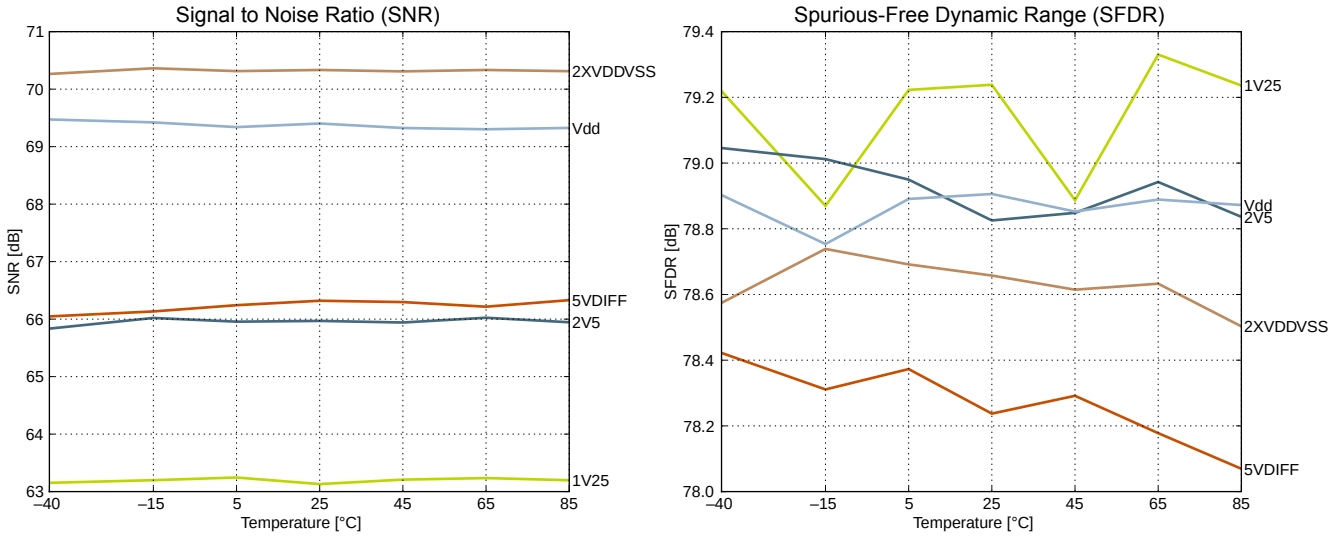



**Figure 4.29. ADC Dynamic Performance vs Temperature for all ADC References, VDD = 3 V**

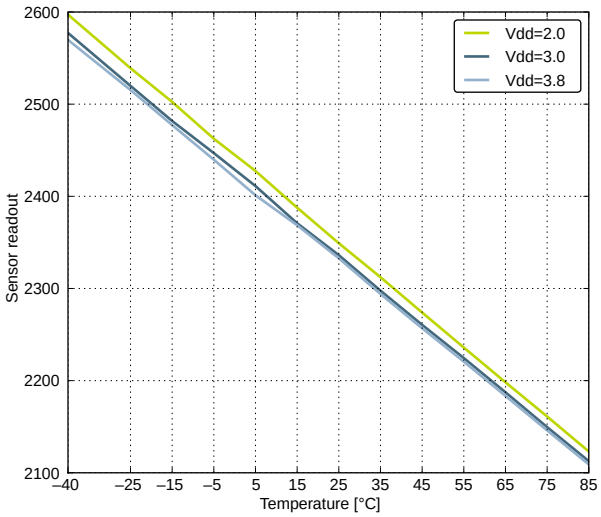



**Figure 4.30. ADC Temperature Sensor Readout**

### 4.12 Digital Analog Converter (DAC)

**Table 4.16. DAC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage range | $V_{DACOUT}$ | VDD voltage reference, single ended | 0 | — | $V_{DD}$ | V |
| | | VDD voltage reference, differential | $-V_{DD}$ | — | $V_{DD}$ | V |
| Output common mode voltage range | $V_{DACCM}$ | | 0 | — | $V_{DD}$ | V |
| Average active current | $I_{DAC}$ | 500 kSamples/s, 12-bit, internal 1.25 V reference, Continuous Mode | — | 400[1] | — | µA |
| | | 100 kSamples/s, 12-bit, internal 1.25 V reference, Sample/Hold Mode | — | 200[1] | — | µA |
| | | 1 kSamples/s 12-bit, internal 1.25 V reference, Sample/Off Mode | — | 17[1] | — | µA |
| Sample rate | $SR_{DAC}$ | | — | — | 500 | ksamples/s |
| DAC clock frequency | $f_{DAC}$ | Continuous Mode | — | — | 1000 | kHz |
| | | Sample/Hold Mode | — | — | 250 | kHz |
| | | Sample/Off Mode | — | — | 250 | kHz |
| Clock cycles per conversion | $CYC_{DACCONV}$ | | — | 2 | — | cycles |
| Conversion time | $t_{DACCONV}$ | | 2 | — | — | µs |
| Settling time | $t_{DACSETTLE}$ | | — | 5 | — | µs |
| Signal-to-Noise Ratio (SNR) | $SNR_{DAC}$ | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 59 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | — | 59 | — | dB |
| Signal-to-Noise plus Distortion Ratio (SNDR) | $SNDR_{DAC}$ | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 57 | — | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 54 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 56 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 53 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | — | 55 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious-Free Dynamic Range (SFDR) | $SFDR_{DAC}$ | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 62 | — | dBc |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 56 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 61 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 55 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | — | 60 | — | dBc |
| Offset voltage, all packages except CSP | $V_{DACOFFSET}$ | After calibration, single ended | — | 2 | 9 | mV |
| | | After calibration, differential | — | 2 | — | mV |
| Offset voltage, CSP devices | $V_{DACOFFSET}$ | After calibration, single ended | — | 2 | — | mV |
| | | After calibration, differential | — | 2 | — | mV |
| Differential non-linearity | $DNL_{DAC}$ | | — | ±1 | — | LSB |
| Integral non-linearity | $INL_{DAC}$ | | — | ±5 | — | LSB |
| No missing codes | $MC_{DAC}$ | | — | 12 | — | bits |
| Load current | $I_{LOAD_DC}$ | | — | — | 11 | mA |
| VREF voltage | $V_{REF}$ | 1.25 V reference | 1.2 | 1.25 | 1.3 | V |
| | | 2.5 V reference | 2.4 | 2.5 | 2.6 | V |
| VREF voltage drift | $V_{REF_VDRIFT}$ | 1.25 V reference | -12.4 | 2.3 | 18.2 | mV/V |
| | | 2.5 V reference, VDD > 2.5 V | -24.6 | 5.3 | 35.2 | mV/V |
| VREF temperature drift | $V_{REF_TDRIFT}$ | 1.25 V reference | -132 | 242 | 677 | µV/°C |
| | | 2.5 V reference | -231 | 507 | 1271 | µV/°C |
| VREF current consumption | $I_{VREF}$ | 1.25 V reference | — | 67 | 114 | µA |
| | | 2.5 V reference | — | 55 | 72 | µA |
| ADC and DAC VREF matching | $V_{REF_MATCH}$ | 1.25 V reference | — | 99.85 | — | % |
| | | 2.5 V reference | — | 100.01 | — | % |

**Note:**

1. Measured with a static input code and no loading on the output. Includes required contribution from the voltage reference.

## 4.13 Operational Amplifier (OPAMP)

**Table 4.17. OPAMP**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active Current | $I_{OPAMP}$ | (OPA2)BIASPROG=0xF,(OPA2)HALF-BIAS=0x0, Unity Gain | — | 370 | 460 | µA |
| | | (OPA2)BIASPROG=0x7,(OPA2)HALF-BIAS=0x1, Unity Gain | — | 95 | 135 | µA |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1, Unity Gain | — | 13 | 25 | µA |
| | | (OPA2)BIASPROG=0x4,(OPA2)HALF-BIAS=0x1, UnityGain | — | 63 | 87 | µA |
| | | (OPA0)BIASPROG=0x0,(OPA0)HALF-BIAS=0x1, UnityGain | — | 18 | 27 | µA |
| | | (OPA0)BIASPROG=0x4,(OPA0)HALF-BIAS=0x1, UnityGain | — | 68 | 96 | µA |
| | | (OPA1)BIASPROG=0x0,(OPA1)HALF-BIAS=0x1, UnityGain | — | 18 | 27 | µA |
| | | (OPA1)BIASPROG=0x4,(OPA1)HALF-BIAS=0x1, UnityGain | — | 67 | 96 | µA |
| Open Loop Gain | $G_{OL}$ | (OPA2)BIASPROG=0xF,(OPA2)HALF-BIAS=0x0 | — | 101 | — | dB |
| | | (OPA2)BIASPROG=0x7,(OPA2)HALF-BIAS=0x1 | — | 98 | — | dB |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1 | — | 91 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Gain Bandwidth Product | $GBW_{OPAMP}$ | (OPA0)BIASPROG=0x0,(OPA0)HALFBIAS=0x1, DC bias = 0.3 V | — | 0.393[1] | — | MHz |
| | | (OPA0)BIASPROG=0x0,(OPA0)HALFBIAS=0x1, DC bias = 1 V | — | 0.487[1] | — | MHz |
| | | (OPA0)BIASPROG=0x0,(OPA0)HALFBIAS=0x1, DC bias = 2 V | — | 0.392[1] | — | MHz |
| | | (OPA0)BIASPROG=0x0,(OPA0)HALFBIAS=0x1, DC bias = 2.7 V | — | 0.318[1] | — | MHz |
| | | (OPA0)BIASPROG=0x4,(OPA0)HALFBIAS=0x1, DC bias = 0.3 V | — | 1.595[1] | — | MHz |
| | | (OPA0)BIASPROG=0x4,(OPA0)HALFBIAS=0x1, DC bias = 1 V | — | 2.661[1] | — | MHz |
| | | (OPA0)BIASPROG=0x4,(OPA0)HALFBIAS=0x1, DC bias = 2 V | — | 2.566[1] | — | MHz |
| | | (OPA0)BIASPROG=0x4,(OPA0)HALFBIAS=0x1, DC bias = 2.7 V | — | 1.787[1] | — | MHz |
| | | (OPA1)BIASPROG=0x0,(OPA1)HALFBIAS=0x1, DC bias = 0.3 V | — | 0.460[1] | — | MHz |
| | | (OPA1)BIASPROG=0x0,(OPA1)HALFBIAS=0x1, DC bias = 1 V | — | 0.447[1] | — | MHz |
| | | (OPA1)BIASPROG=0x0,(OPA1)HALFBIAS=0x1, DC bias = 2 V | — | 0.372[1] | — | MHz |
| | | (OPA1)BIASPROG=0x0,(OPA1)HALFBIAS=0x1, DC bias = 2.7 V | — | 0.295[1] | — | MHz |
| | | (OPA1)BIASPROG=0x4,(OPA1)HALFBIAS=0x1, DC bias = 0.3 V | — | 1.890[1] | — | MHz |
| | | (OPA1)BIASPROG=0x4,(OPA1)HALFBIAS=0x1, DC bias = 1 V | — | 2.849[1] | — | MHz |
| | | (OPA1)BIASPROG=0x4,(OPA1)HALFBIAS=0x1, DC bias = 2 V | — | 2.561[1] | — | MHz |
| | | (OPA1)BIASPROG=0x4,(OPA1)HALFBIAS=0x1, DC bias = 2.7 V | — | 1.705[1] | — | MHz |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALFBIAS=0x1, DC bias = 0.3 V | — | 0.339[1] | — | MHz |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALFBIAS=0x1, DC bias = 1 V | — | 0.432[1] | — | MHz |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALFBIAS=0x1, DC bias = 2 V | — | 0.347[1] | — | MHz |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALFBIAS=0x1, DC bias = 2.7 V | — | 0.286[1] | — | MHz |
| | | (OPA2)BIASPROG=0x4,(OPA2)HALFBIAS=0x1, DC bias = 0.3 V | — | 1.271[1] | — | MHz |
| | | (OPA2)BIASPROG=0x4,(OPA2)HALFBIAS=0x1, DC bias = 1 V | — | 1.429[1] | — | MHz |
| | | (OPA2)BIASPROG=0x4,(OPA2)HALFBIAS=0x1, DC bias = 2 V | — | 1.283[1] | — | MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Gain Bandwidth Product | $GBW_{OPAMP}$ | (OPA2)BIASPROG=0x4,(OPA2)HALF-BIAS=0x1, DC bias = 2.7 V | — | 1.136[1] | — | MHz |
| | | (OPA2)BIASPROG=0xF,(OPA2)HALF-BIAS=0x0, DC bias = 1.5 V | — | 6.1[2] | — | MHz |
| | | (OPA2)BIASPROG=0x7,(OPA2)HALF-BIAS=0x1, DC bias = 1.5 V | — | 1.8[2] | — | MHz |
| Phase Margin | $PM_{OPAMP}$ | (OPA2)BIASPROG=0xF,(OPA2)HALF-BIAS=0x0, $C_L$=75 pF | — | 64 | — | ° |
| | | (OPA2)BIASPROG=0x7,(OPA2)HALF-BIAS=0x1, $C_L$=75 pF | — | 58 | — | ° |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1, $C_L$=75 pF | — | 58 | — | ° |
| Input Resistance | $R_{INPUT}$ | | — | 100 | — | MΩ |
| Load Resistance | $R_{LOAD}$ | | 200 | — | — | Ω |
| DC Load Current | $I_{LOAD_DC}$ | | — | — | 11 | mA |
| Input Voltage | $V_{INPUT}$ | OPAxHCMDIS=0 | $V_{SS}$ | — | $V_{DD}$ | V |
| | | OPAxHCMDIS=1 | $V_{SS}$ | — | $V_{DD}$-1.2 | V |
| Output Voltage | $V_{OUTPUT}$ | | $V_{SS}$ | — | $V_{DD}$ | V |
| Input Offset Voltage, all packages except CSP | $V_{OFFSET}$ | (OPA0) Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | -13 | 0 | 11 | mV |
| | | (OPA1) Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | -13 | 0.1 | 11 | mV |
| | | (OPA2) Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | -13 | 0 | 11 | mV |
| | | (OPA2) Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$-1.2,OPAxHCMDIS=1 | — | 1 | — | mV |
| Input Offset Voltage, CSP devices | $V_{OFFSET}$ | (OPA0) Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | — | 0 | — | mV |
| | | (OPA1) Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | — | 0.1 | — | mV |
| | | (OPA2) Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | -13 | 0 | 11 | mV |
| | | (OPA2) Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$-1.2,OPAxHCMDIS=1 | — | 1 | — | mV |
| Input Offset Voltage Drift | $V_{OFFSET_DRIFT}$ | | — | — | 0.02 | mV/°C |
| Input bias current | $I_{OPAMPBIASIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| Input offset current | $I_{OPAMPOFFSETI}$ | VSS < VIN < VDD | -40 | — | 40 | nA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Slew Rate | $SR_{OPAMP}$ | (OPA2)BIASPROG=0xF,(OPA2)HALF-BIAS=0x0, 70 pF load Rising (Simulated at 25 C and VDD=3 V) | — | 3.2 | — | V/µs |
| | | (OPA2)BIASPROG=0x7,(OPA2)HALF-BIAS=0x1, 70 pF load, Rising (Simulated at 25 Cand VDD=3 V) | — | 0.8 | — | V/µs |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1, 70 pF load, Rising | — | 178 | — | V/µs |
| | | (OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1, 70 pF load, Falling | — | 198 | — | V/µs |
| | | (OPA2)BIASPROG=0x4,(OPA2)HALF-BIAS=0x1, 70 pF load, Rising | — | 969 | — | V/µs |
| | | (OPA2)BIASPROG=0x4,(OPA2)HALF-BIAS=0x1, 70 pF load, Falling | — | 969 | — | V/µs |
| | | (OPA1)BIASPROG=0x0,(OPA1)HALF-BIAS=0x1, 70 pF load, Rising | — | 166 | — | V/µs |
| | | (OPA1)BIASPROG=0x0,(OPA1)HALF-BIAS=0x1, 70 pF load, Falling | — | 180 | — | V/µs |
| | | (OPA1)BIASPROG=0x4,(OPA1)HALF-BIAS=0x1, 70 pF load, Rising | — | 918 | — | V/µs |
| | | (OPA1)BIASPROG=0x4,(OPA1)HALF-BIAS=0x1, 70 pF load, Falling | — | 937 | — | V/µs |
| | | (OPA0)BIASPROG=0x0,(OPA0)HALF-BIAS=0x1, 70 pF load, Rising | — | 173 | — | V/µs |
| | | (OPA0)BIASPROG=0x0,(OPA0)HALF-BIAS=0x1, 70 pF load, Falling | — | 191 | — | V/µs |
| | | (OPA0)BIASPROG=0x4,(OPA0)HALF-BIAS=0x1, 70 pF load, Rising | — | 935 | — | V/µs |
| | | (OPA0)BIASPROG=0x4,(OPA0)HALF-BIAS=0x1, 70 pF load, Falling | — | 950 | — | V/µs |
| Voltage Noise | $N_{OPAMP}$ | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0 | — | 101 | — | $\mu V_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1 | — | 141 | — | $\mu V_{RMS}$ |
| | | Vout=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | — | 196 | — | $\mu V_{RMS}$ |
| | | Vout=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1 | — | 229 | — | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCM-DIS=0 | — | 1230 | — | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCM-DIS=1 | — | 2130 | — | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCM-DIS=0 | — | 1630 | — | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCM-DIS=1 | — | 2590 | — | $\mu V_{RMS}$ |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Measured with 70 pF load capacitance, 25 ºC, and 3 V, using a 100 mV p-p amplitude on the input signal.
2. Simulated with 70 pF load capacitance, 25 ºC, and 3 V, using a 1 mV p-p amplitude on the input signal.

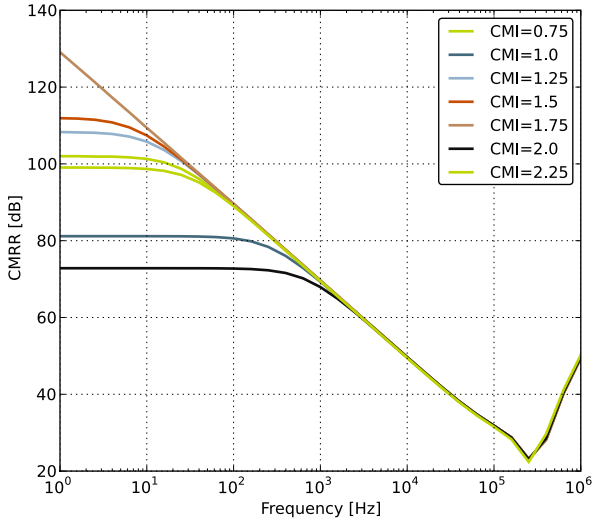



**Figure 4.31. OPAMP Common Mode Rejection Ratio**

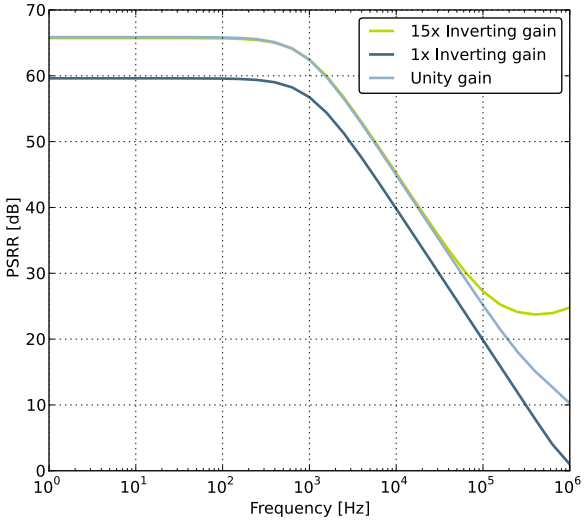



**Figure 4.32. OPAMP Positive Power Supply Rejection Ratio**

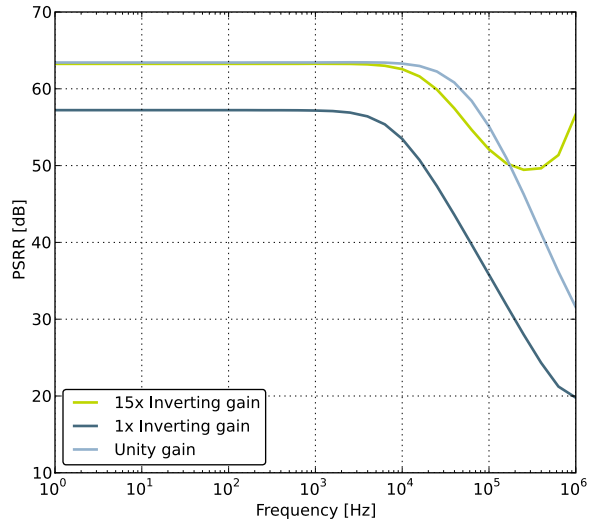



**Figure 4.33. OPAMP Negative Power Supply Rejection Ratio**

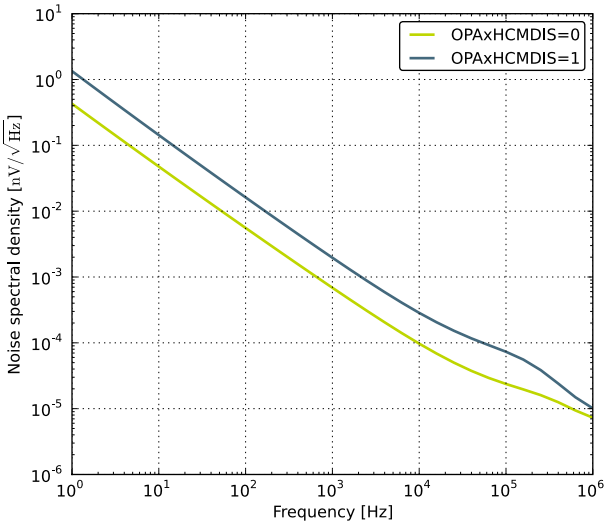



**Figure 4.34. OPAMP Voltage Noise Spectral Density(Unity Gain) $V_{out}$=1V**

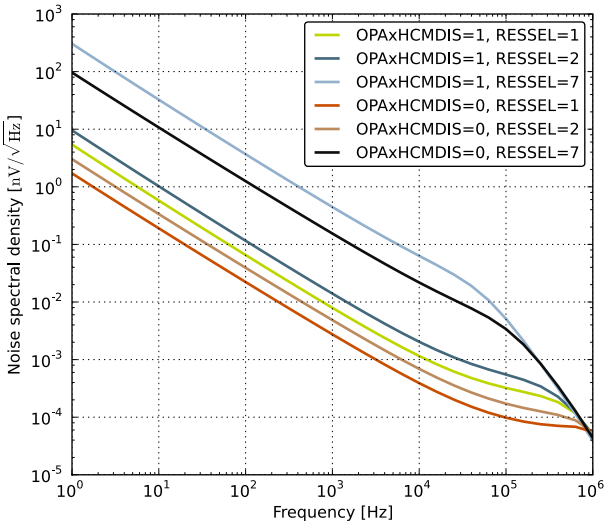



**Figure 4.35. OPAMP Voltage Noise Spectral Density(Non-Unity Gain)**

### 4.14 Analog Comparator (ACMP)

**Table 4.18. ACMP**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{ACMPIN}$ | | 0 | — | $V_{DD}$ | V |
| Input bias current | $I_{ACMPBIASIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| Input offset current | $I_{ACMPOFFSETIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| ACMP Common Mode voltage range | $V_{ACMPCM}$ | | 0 | — | $V_{DD}$ | V |
| Active current | $I_{ACMP}$ | BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register | — | 0.1[1] | 0.4[1] | µA |
| | | BIASPROG=0b1111, FULLBIAS= 0 and HALFBIAS=0 in ACMPn_CTRL register | — | 2.87[1] | 15[1] | µA |
| | | BIASPROG=0b1111, FULLBIAS= 1 and HALFBIAS=0 in ACMPn_CTRL register | — | 195[1] | 520[1] | µA |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1 in ACMPn_CTRL register | — | 0.8[1] | 2.2[1] | µA |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1 in-ACMPn_CTRL register | — | 2.7[1] | 8.1[1] | µA |
| Current consumption of internal voltage reference | $I_{ACMPREF}$ | Internal voltage reference off. Using external voltage reference | — | 0 | — | µA |
| | | Internal voltage reference | — | 5 | — | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Negative response time | $t_{RESPONSE_N}$ | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=0 | — | 353 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=1 | — | 547 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=2 | — | 578 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=3 | — | 627 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=4 | — | 670 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=5 | — | 741 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=6 | — | 811 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=7 | — | 926 | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Negative response time | $t_{RESPONSE_N}$ | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=0 | — | 843 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=1 | — | 1499 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=2 | — | 1590 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=3 | — | 1746 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=4 | — | 1876 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=5 | — | 2104 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=6 | — | 2323 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=7 | — | 2691 | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Positive response time | $t_{RESPONSE_P}$ | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=0 | — | 451 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=1 | — | 643 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=2 | — | 679 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=3 | — | 725 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=4 | — | 761 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=5 | — | 826 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=6 | — | 909 | — | ns |
| | | BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=7 | — | 1021 | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Positive response time | $t_{RESPONSE_P}$ | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=0 | — | 1014 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=1 | — | 1671 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=2 | — | 1786 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=3 | — | 1933 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=4 | — | 2046 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=5 | — | 2262 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=6 | — | 2531 | — | ns |
| | | BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=7 | — | 2907 | — | ns |
| Offset voltage | $V_{ACMPOFFSET}$ | BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | -12 | 0 | 12 | mV |
| | | BIASPROG= 0b0100, FULLBIAS=0, HALFBIAS=1, and LPREF=0 in ACMPn_CTRL register | -14.4 | 0.4 | 14.8 | mV |
| | | BIASPROG= 0b1111, FULLBIAS=0, HALFBIAS=1, and LPREF=0 in ACMPn_CTRL register | -13.3 | 0.3 | 13.2 | mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Negative hysteresis | $V_{ACMPHYST_N}$ | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=0 | -0.3 | 1.2 | 4.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=1 | -18.0 | -12.2 | -4.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=2 | -25.0 | -17.6 | -9.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=3 | -33.0 | -22.8 | -13.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=4 | -40.0 | -27.8 | -16.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=5 | -46.0 | -33.4 | -21.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=6 | -56.0 | -39.9 | -25.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=7 | -65.0 | -46.4 | -29.0 | mV |
| Positive hysteresis | $V_{ACMPHYST_P}$ | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=0 | -0.3 | 1.2 | 4.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=1 | 4.0 | 12.2 | 21.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=2 | 9.0 | 17.1 | 25.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=3 | 13.0 | 22.3 | 33.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=4 | 17.0 | 28.2 | 42.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=5 | 20.0 | 34.0 | 49.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=6 | 25.0 | 39.8 | 58.0 | mV |
| | | BIASPROG=0b1111, FULL-BIAS=0, HALF-BIAS=1,LPREF=0, HYSTSEL=7 | 29.4 | 46.4 | 68.0 | mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Capacitive Sense Internal Resistance | $R_{CSRES}$ | CSRESSEL=0b00 in ACMPn_INPUTSEL | — | 39 | — | kΩ |
| | | CSRESSEL=0b01 in ACMPn_INPUTSEL | — | 71 | — | kΩ |
| | | CSRESSEL=0b10 in ACMPn_INPUTSEL | — | 104 | — | kΩ |
| | | CSRESSEL=0b11 in ACMPn_INPUTSEL | — | 136 | — | kΩ |
| Startup time | $t_{ACMPSTART}$ | | — | — | 10 | µs |
| VDD_SCALED input accuracy | $V_{VDDSCALED}$ | VDD_SCALED=9,BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1, HYSTSEL=0, LPREF=0 | — | -10.8 | — | mV |
| | | VDD_SCALED=9,BIASPROG=0b0000, FULLBIAS=0, HALFBIAS=1, HYSTSEL=0, LPREF=1 | — | 1.3 | — | mV |

**Note:**
1. Reference current not included.

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in in the following equation. $I_{ACMPREF}$ is zero if an external voltage reference is used.

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

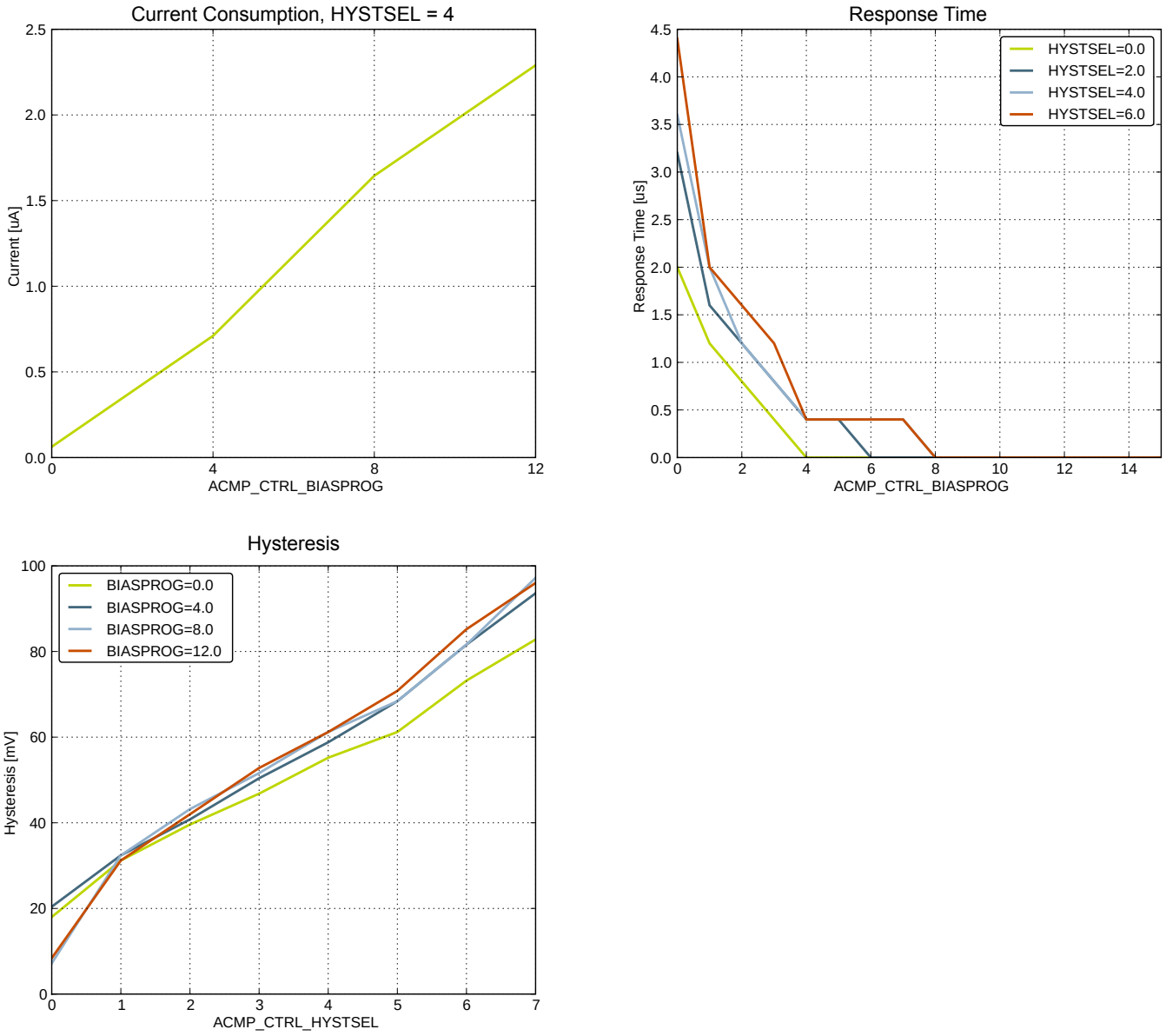



**Figure 4.36. ACMP Characteristics, Vdd = 3 V, Temp = 25 °C, FULLBIAS = 0, HALFBIAS = 1**

### 4.15 Voltage Comparator (VCMP)

**Table 4.19. VCMP**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{VCMPIN}$ | | — | $V_{DD}$ | — | V |
| VCMP Common Mode voltage range | $V_{VCMPCM}$ | | — | $V_{DD}$ | — | V |
| Active current | $I_{VCMP}$ | BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register | — | 0.3[1] | 0.6[1] | µA |
| | | BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0. | — | 22[1] | 35[1] | µA |
| Startup time reference generator | $t_{VCMPREF}$ | NORMAL | — | 10 | — | µs |
| Offset voltage | $V_{VCMPOFFSET}$ | Single ended | — | 10 | — | mV |
| | | Differential | — | 10 | — | mV |
| Negative hysteresis | $V_{VCMPHYST_N}$ | BIASPROG=0b0000, HALFBIAS=1, LPREF=1 | -46.6 | -15.6 | 11.4 | mV |
| Positive hysteresis | $V_{VCMPHYST_P}$ | BIASPROG=0b0000, HALFBIAS=1, LPREF=1 | -7.5 | 23.4 | 46.6 | mV |
| Hysteresis delta | $V_{VCMPHYST_DELTA}$ | BIASPROG=0b0000, HALFBIAS=1, LPREF=1 | 4.2 | 35.2 | 70.0 | mV |
| Startup time | $t_{VCMPSTART}$ | | — | — | 10 | µs |
| Negative response time | $t_{RESPONSE_N}$ | BIASPROG=0b0000, HALFBIAS=1, LPREF=1, HYSTSEL=0 | — | 372.3 | — | µs |
| Positive response time | $t_{RESPONSE_P}$ | BIASPROG=0b0000, HALFBIAS=1, LPREF=1, HYSTSEL=0 | — | 865.7 | — | µs |

**Note:**
1. Includes required contribution from the voltage reference.

The $V_{DD}$ trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{DD\ Trigger\ Level} = 1.667V + 0.034 \times TRIGLEVEL$$

### 4.16 EBI

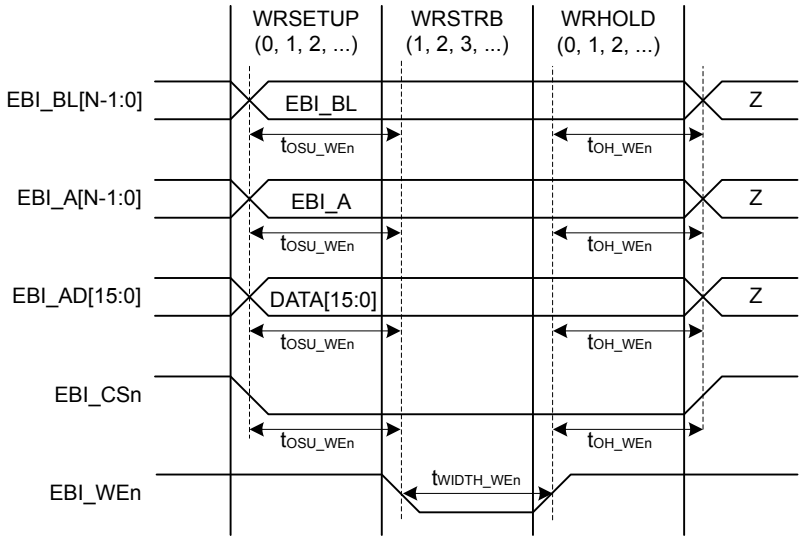



**Figure 4.37. EBI Write Enable Timing**

**Table 4.20. EBI Write Enable Timing**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output hold time, from trailing EBI_WEn/EBI_NAND-WEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | $t_{OH_WEn}$ [1 2 3 4] | -6.00 + (WRHOLD × $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn/EBI_NANDWEn edge | $t_{OSU_WEn}$ [1 2 3 4 5] | -14.00 + (WRSETUP × $t_{HFCORECLK}$) | — | — | ns |
| EBI_WEn/EBI_NANDWEn pulse width | $t_{WIDTH_WEn}$ [1 2 3 4 5] | -7.00 + ((WRSTRB + 1) × $t_{HFCORECLK}$) | — | — | ns |

**Note:**

1. Applies for all addressing modes (figure only shows D16 addressing mode)
2. Applies for both EBI_WEn and EBI_NANWEn (figure only shows EBI_WEn)
3. Applies for all polarities (figure only shows active low signals)
4. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)
5. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of $t_{WIDTH_WEn}$ and increases the length of $t_{OSU_WEn}$ by 1/2 × $t_{HFCLKNODIV}$.

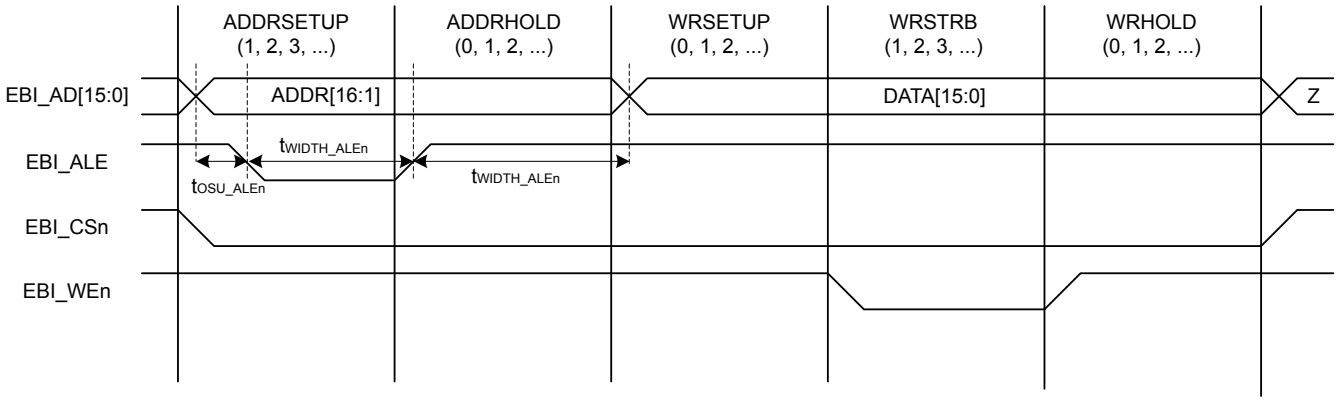



**Figure 4.38. EBI Address Latch Enable Related Output Timing**

**Table 4.21. EBI Address Latch Enable Related Output Timing**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output hold time, from trailing EBI_ALE edge to EBI_AD invalid | $t_{OH_ALEn}$ [1 2 3 4] | -6.00 + (WRHOLD[5] × $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, from EBI_AD valid to leading EBI_ALE edge | $t_{OSU_ALEn}$ [1 2 4] | -13.00 + (0 × $t_{HFCORECLK}$) | — | — | ns |
| EBI_ALEn pulse width | $t_{WIDTH_ALEn}$ [1 2 3 4] | -7.00 + ((ADDRSETUP + 1) × $t_{HFCORECLK}$) | — | — | ns |

**Note:**

1. Applies to addressing modes D8A24ALE and D16A16ALE (figure only shows D16A16ALE)
2. Applies for all polarities (figure only shows active low signals)
3. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALE can be moved to the left by setting HALFALE=1. This decreases the length of $t_{WIDTH_ALEn}$ and increases the length of $t_{OH_ALEn}$ by $t_{HFCORECLK}$ - 1/2 × $t_{HFCLKNODIV}$.
4. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)
5. Figure only shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

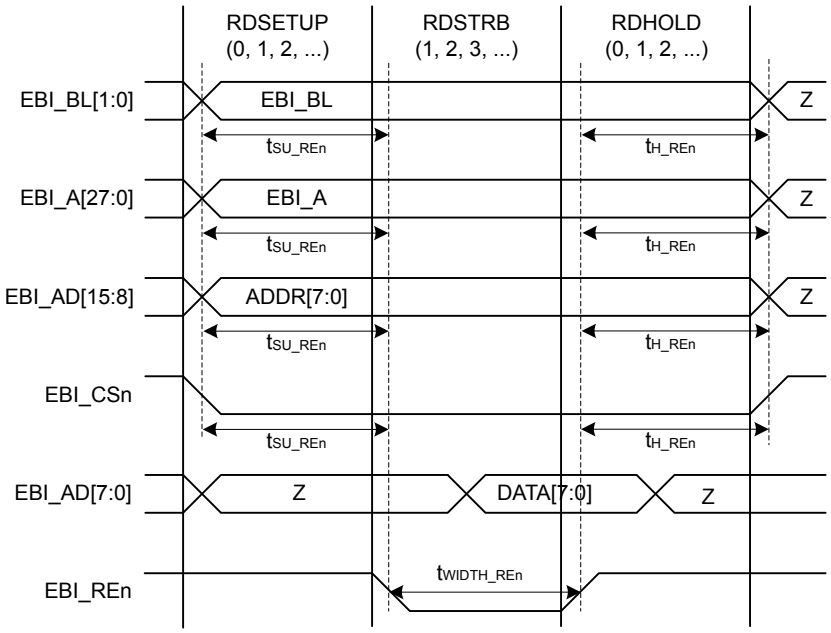



**Figure 4.39. EBI Read Enable Related Output Timing**

**Table 4.22. EBI Read Enable Related Output Timing**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output hold time, from trailing EBI_REn/EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | $t_{OH_REn}$ [1 2 3 4] | -10.00 + (RDHOLD × $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn/ EBI_NANDREn edge | $t_{OSU_REn}$ [1 2 3 4 5] | -10.00 + (RDSETUP × $t_{HFCORECLK}$) | — | — | ns |
| EBI_REn pulse width | $t_{WIDTH_REn}$ [1 2 3 4 5 6] | -9.00 + ((RDSTRB + 1) × $t_{HFCORECLK}$) | — | — | ns |

**Note:**

1. Applies for all addressing modes (figure only shows D8A8. Output timing for EBI_AD only applies to multiplexed addressing modes D8A24ALE and D16A16ALE)
2. Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)
3. Applies for all polarities (figure only shows active low signals)
4. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)
5. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of $t_{WIDTH_REn}$ and increases the length of $t_{OSU_REn}$ by 1/2 × $t_{HFCLKNODIV}$.
6. When page mode is used, RDSTRB is replaced by RDPA for page hits.

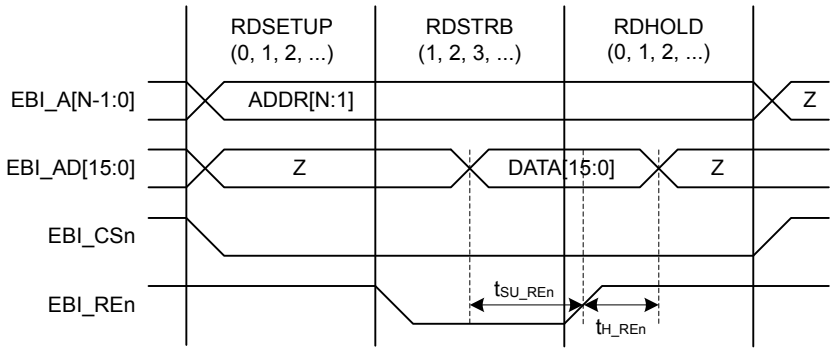



**Figure 4.40. EBI Read Enable Related Timing Requirements**

**Table 4.23. EBI Read Enable Related Timing Requirements**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Setup time, from EBI_AD valid to trailing EBI_REn edge | $t_{SU_REn}$ [1 2 3 4] | 37 | — | — | ns |
| Hold time, from trailing EBI_REn edge to EBI_AD invalid | $t_{H_REn}$ [1 2 3 4] | -1 | — | — | ns |

**Note:**

1. Applies for all addressing modes (figure only shows D16A8).
2. Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)
3. Applies for all polarities (figure only shows active low signals)
4. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

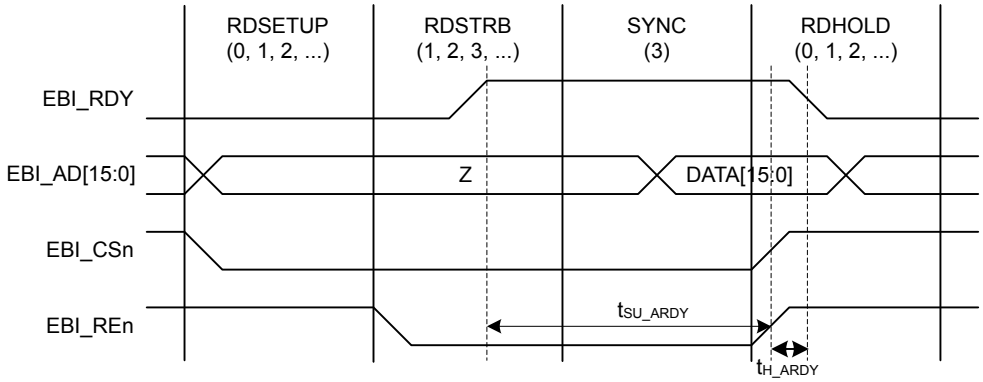



**Figure 4.41. EBI Ready/Wait Related Timing Requirements**

**Table 4.24. EBI Ready/Wait Related Timing Requirements**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge | $t_{SU_ARDY}$ [1 2 3 4] | 37 + (3 × $t_{HFCORECLK}$) | — | — | ns |
| Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid | $t_{H_ARDY}$ [1 2 3 4] | -1 + (3 × $t_{HFCORECLK}$) | — | — | ns |

**Note:**

1. Applies for all addressing modes (figure only shows D16A8.)
2. Applies for EBI_REn, EBI_WEn (figure only shows EBI_REn)
3. Applies for all polarities (figure only shows active low signals)
4. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

### 4.17 LCD

**Table 4.25. LCD**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frame rate | $f_{LCDFR}$ | | 30 | — | 200 | Hz |
| Number of segments supported | $NUM_{SEG}$ | | — | 36×8 | — | seg |
| LCD supply voltage range | $V_{LCD}$ | Internal boost circuit enabled | 2.0 | — | 3.8 | V |
| Steady state current consumption. | $I_{LCD}$ | Display disconnected, static mode, framerate 32 Hz, all segments on. | — | 250 | — | nA |
| | | Display disconnected, quad-ruplex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register. | — | 550 | — | nA |
| Steady state Current contribution of internal boost. | $I_{LCDBOOST}$ | Internal voltage boost off | — | 0 | — | µA |
| | | Internal voltage boost on, boosting from 2.2 V to 3.0 V. | — | 8.4 | — | µA |
| Boost Voltage | $V_{BOOST}$ | VBLEV of LCD_DISPCTRL register to LEVEL0 | — | 3.02 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL1 | — | 3.15 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL2 | — | 3.28 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL3 | — | 3.41 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL4 | — | 3.54 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL5 | — | 3.67 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL6 | — | 3.73 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL7 | — | 3.74 | — | V |

The total LCD current is given by the following equation. $I_{LCDBOOST}$ is zero if internal boost is off.

$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST}$

### 4.18 I2C

**Table 4.26. I2C Standard-mode (Sm)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | — | 100[1] | kHz |
| SCL clock low time | $t_{LOW}$ | 4.7 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | 4.0 | — | — | µs |
| SDA set-up time | $t_{SU,DAT}$ | 250 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | 3450[2,3] | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 4.7 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 4.0 | — | — | µs |
| STOP condition set-up time | $t_{SU,STO}$ | 4.0 | — | — | µs |
| Bus free time between a STOP and a START condition | $t_{BUF}$ | 4.7 | — | — | µs |

**Note:**
1. For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32WG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 4).

**Table 4.27. I2C Fast-mode (Fm)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | | 400[1] | kHz |
| SCL clock low time | $t_{LOW}$ | 1.3 | | | µs |
| SCL clock high time | $t_{HIGH}$ | 0.6 | | | µs |
| SDA set-up time | $t_{SU,DAT}$ | 100 | | | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | | 900[2,3] | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.6 | | | µs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.6 | | | µs |
| STOP condition set-up time | $t_{SU,STO}$ | 0.6 | | | µs |
| Bus free time between a STOP and a START condition | $t_{BUF}$ | 1.3 | | | µs |

**Note:**
1. For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32WG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 4).

**Table 4.28. I2C Fast-mode Plus (Fm+)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | | 1000[1] | kHz |
| SCL clock low time | $t_{LOW}$ | 0.5 | | | µs |
| SCL clock high time | $t_{HIGH}$ | 0.26 | | | µs |
| SDA set-up time | $t_{SU,DAT}$ | 50 | | | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | | | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.26 | | | µs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.26 | | | µs |
| STOP condition set-up time | $t_{SU,STO}$ | 0.26 | | | µs |
| Bus free time between a STOP and a START condition | $t_{BUF}$ | 0.5 | | | µs |

**Note:**
1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32WG Reference Manual.

### 4.19 USART SPI

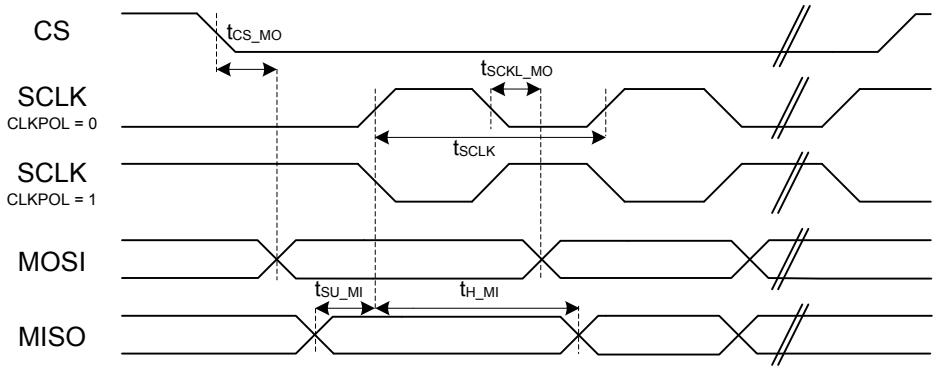



**Figure 4.42. SPI Master Timing**

**Table 4.29. SPI Master Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period | $t_{SCLK}$ [1] [2] | | 2 × $t_{HFPERCLK}$ | — | — | ns |
| CS to MOSI | $t_{CS_MO}$ [1] [2] | | -2.00 | — | 2.00 | ns |
| SCLK to MOSI | $t_{SCLK_MO}$ [1] [2] | | -1.00 | — | 3.00 | ns |
| MISO setup time | $t_{SU_MI}$ [1] [2] | IOVDD = 3.0 V | 36.00 | — | — | ns |
| MISO hold time | $t_{H_MI}$ [1] [2] | | -6.00 | — | — | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

**Table 4.30. SPI Master Timing with SSSEARLY and SMSDELAY**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period | $t_{SCLK}$ [1] [2] | | 2 × $t_{HFPERCLK}$ | — | — | ns |
| CS to MOSI | $t_{CS_MO}$ [1] [2] | | -2.00 | — | 2.00 | ns |
| SCLK to MOSI | $t_{SCLK_MO}$ [1] [2] | | -1.00 | — | 3.00 | ns |
| MISO setup time | $t_{SU_MI}$ [1] [2] | IOVDD = 3.0 V | -32.00 | — | — | ns |
| MISO hold time | $t_{H_MI}$ [1] [2] | | 63.00 | — | — | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

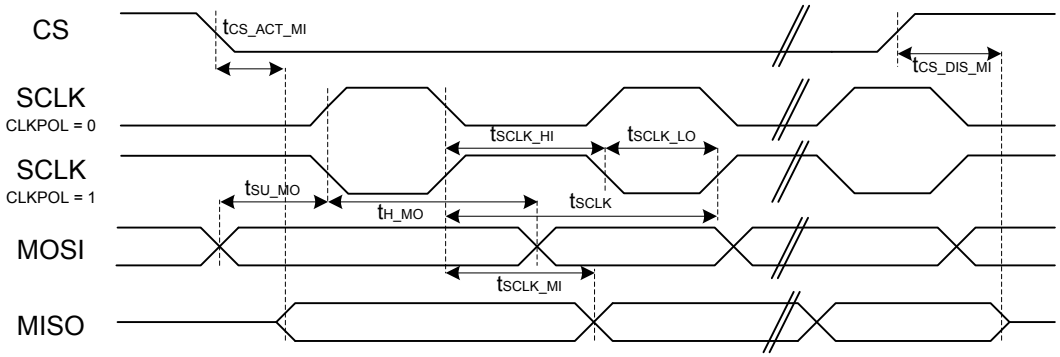



**Figure 4.43. SPI Master Timing**

**Table 4.31. SPI Slave Timing**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCKL period | $t_{SCLK_sl}$ [1] [2] | 6 × $t_{HFPERCLK}$ | — | — | ns |
| SCLK high period | $t_{SCLK_hi}$ [1] [2] | 3 × $t_{HFPERCLK}$ | — | — | ns |
| SCLK low period | $t_{SCLK_lo}$ [1] [2] | 3 × $t_{HFPERCLK}$ | — | — | ns |
| CS active to MISO | $t_{CS_ACT_MI}$ [1] [2] | 5.00 | — | 35.00 | ns |
| CS disable to MISO high-impedance | $t_{CS_DIS_MI}$ [1] [2] | 5.00 | — | 35.00 | ns |
| MOSI setup time | $t_{SU_MO}$ [1] [2] | 5.00 | — | — | ns |
| MOSI hold time | $t_{H_MO}$ [1] [2] | 2 + 2 × $t_{HFPERCLK}$ | — | — | ns |
| SCLK to MISO | $t_{SCLK_MI}$ [1] [2] | 7 + $t_{HFPERCLK}$ | — | 42 + 2 × $t_{HFPERCLK}$ | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

**Table 4.32. SPI Slave Timing with SSSEARLY and SMSDELAY**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCKL period | $t_{SCLK_sl}$ [1] [2] | 6 × $t_{HFPERCLK}$ | — | — | ns |
| SCLK high period | $t_{SCLK_hi}$ [1] [2] | 3 × $t_{HFPERCLK}$ | — | — | ns |
| SCLK low period | $t_{SCLK_lo}$ [1] [2] | 3 × $t_{HFPERCLK}$ | — | — | ns |
| CS active to MISO | $t_{CS_ACT_MI}$ [1] [2] | 5.00 | — | 35.00 | ns |
| CS disable to MISO | $t_{CS_DIS_MI}$ [1] [2] | 5.00 | — | 35.00 | ns |
| MOSI setup time | $t_{SU_MO}$ [1] [2] | 5.00 | — | — | ns |
| MOSI hold time | $t_{H_MO}$ [1] [2] | 2 + 2 × $t_{HFPERCLK}$ | — | — | ns |

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCLK to MISO | $t_{SCLK_MI}$ [1] [2] | -264 + $t_{HFPERCLK}$ | — | -234 + 2 × $t_{HFPERCLK}$ | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

### 4.20 Digital Peripherals

**Table 4.33. Digital Peripherals**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| USART current | $I_{USART}$ | USART idle current, clock enabled | — | 4.0 | — | µA/MHz |
| UART current | $I_{UART}$ | UART idle current, clock enabled | — | 3.8 | — | µA/MHz |
| LEUART current | $I_{LEUART}$ | LEUART idle current, clock enabled | — | 194.0 | — | nA |
| I2C current | $I_{I2C}$ | I2C idle current, clock enabled | — | 7.6 | — | µA/MHz |
| TIMER current | $I_{TIMER}$ | TIMER_0 idle current, clock enabled | — | 6.5 | — | µA/MHz |
| LETIMER current | $I_{LETIMER}$ | LETIMER idle current, clock enabled | — | 85.8 | — | nA |
| PCNT current | $I_{PCNT}$ | PCNT idle current, clock enabled | — | 91.4 | — | nA |
| RTC current | $I_{RTC}$ | RTC idle current, clock enabled | — | 54.6 | — | nA |
| LCD current | $I_{LCD}$ | LCD idle current, clock enabled | — | 72.7 | — | nA |
| AES current | $I_{AES}$ | AES idle current, clock enabled | — | 1.8 | — | µA/MHz |
| GPIO current | $I_{GPIO}$ | GPIO idle current, clock enabled | — | 3.4 | — | µA/MHz |
| EBI current | $I_{EBI}$ | EBI idle current, clock enabled | — | 6.5 | — | µA/MHz |
| PRS current | $I_{PRS}$ | PRS idle current | — | 3.9 | — | µA/MHz |
| DMA current | $I_{DMA}$ | Clock enable | — | 10.9 | — | µA/MHz |
| LE Peripheral Interface Clock current | $I_{LFCLK}$ | Using LFXO, LFA clock tree | — | 12.2 | — | µA/MHz |
| | | Using LFXO, LFB clock tree | — | 4.3 | — | µA/MHz |

# 5. Pin Definitions

**Note:** Please refer to the application note *AN0002 EFM32 Hardware Design Considerations* for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32WG.

## 5.1 EFM32WG230 (QFN64)

### 5.1.1 Pinout

The EFM32WG230 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

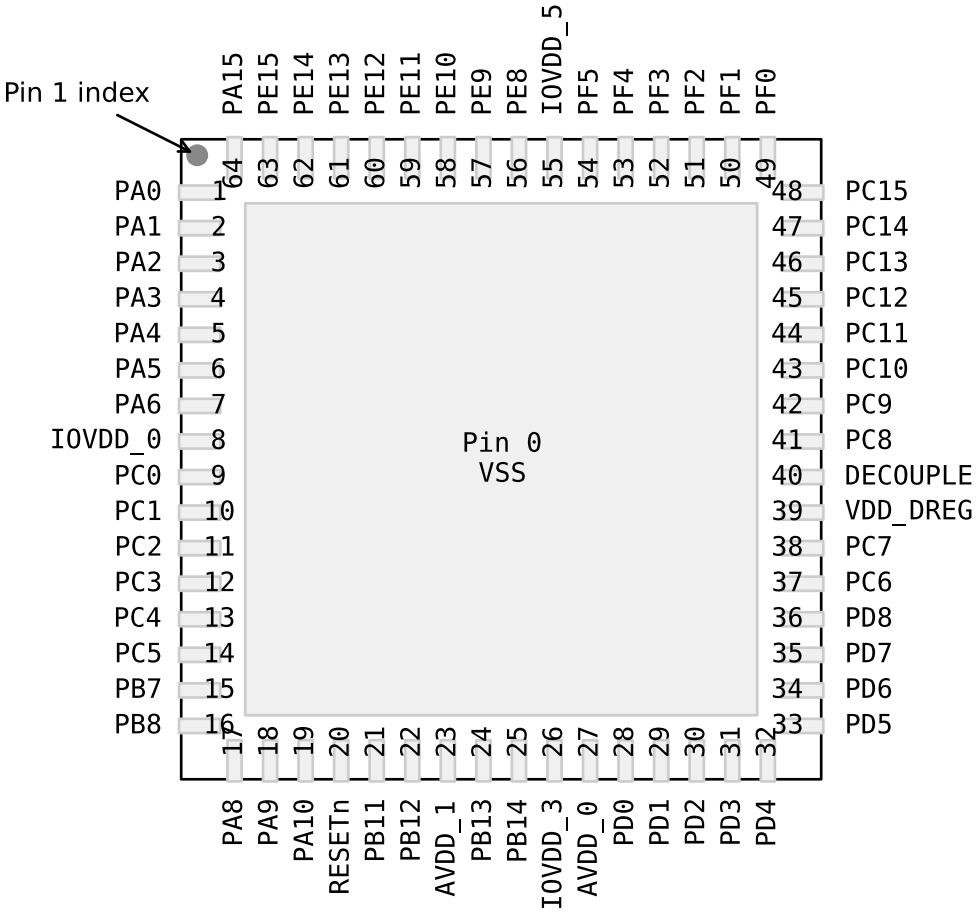



**Figure 5.1. EFM32WG230 Pinout (top view, not to scale)**

**Table 5.1. Device Pinout**

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| 4 | PA3 | | TIM0_CDTI0 #0 | | LES_ALTEX2 #0 ETM_TD1 #3 |
| 5 | PA4 | | TIM0_CDTI1 #0 | | LES_ALTEX3 #0 ETM_TD2 #3 |
| 6 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| 7 | PA6 | | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 10 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 11 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 12 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 13 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA8 | | TIM2_CC0 #0 | | |
| 18 | PA9 | | TIM2_CC1 #0 | | |
| 19 | PA10 | | TIM2_CC2 #0 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 22 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 42 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 43 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| 45 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | CMU_CLK0 #1 LES_CH12 #0 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 46 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 47 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 48 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 49 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 51 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | PF3 | | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| 53 | PF4 | | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| 54 | PF5 | | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 57 | PE9 | | PCNT2_S1IN #1 | | |
| 58 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 60 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 61 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 62 | PE14 | | TIM3_CC0 #0 | LEU0_TX #2 | |
| 63 | PE15 | | TIM3_CC1 #0 | LEU0_RX #2 | |
| 64 | PA15 | | TIM3_CC2 #0 | | |

### 5.1.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.2. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM3_CC2 | PA15 | | | | | | | Timer 3 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.1.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG230 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.3. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | — | — | — | — | PA10 | PA9 | PA8 | — | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PA12 | PB11 | — | — | PB8 | PB7 | — | — | — | — | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | — | — | — | — | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.1.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG230 is shown in the following figure.

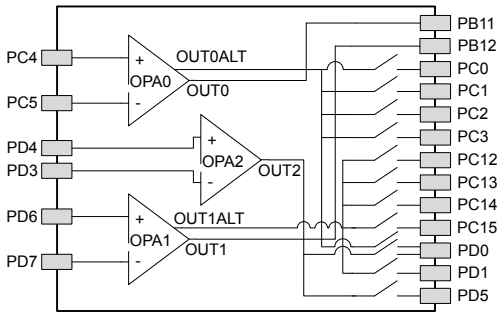



**Figure 5.2. Opamp Pinout**

## 5.2 EFM32WG232 (TQFP64)

### 5.2.1 Pinout

The EFM32WG232 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

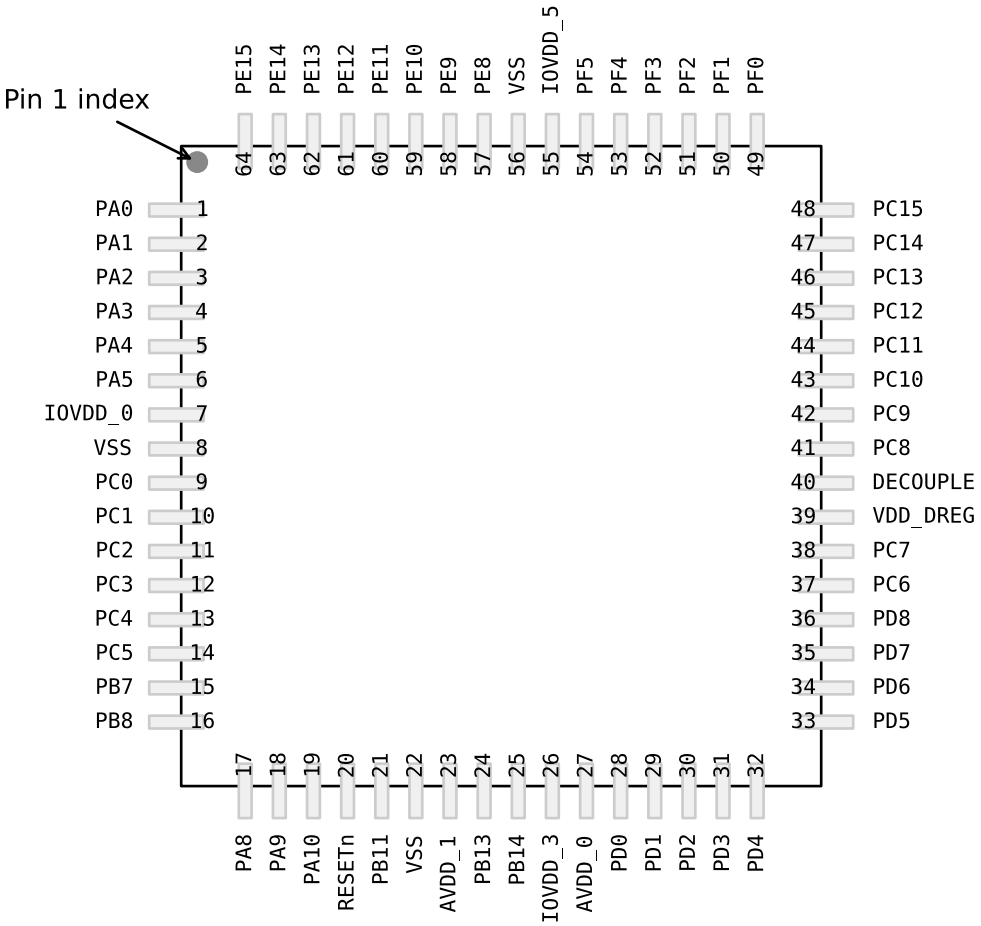



**Figure 5.3. EFM32WG232 Pinout (top view, not to scale)**

**Table 5.4. Device Pinout**

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PA3 | | TIM0_CDTI0 #0 | | LES_ALTEX2 #0 ETM_TD1 #3 |
| 5 | PA4 | | TIM0_CDTI1 #0 | | LES_ALTEX3 #0 ETM_TD2 #3 |
| 6 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 10 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 11 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 12 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 13 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA8 | | TIM2_CC0 #0 | | |
| 18 | PA9 | | TIM2_CC1 #0 | | |
| 19 | PA10 | | TIM2_CC2 #0 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 42 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 43 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| 45 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | CMU_CLK0 #1 LES_CH12 #0 |
| 46 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 47 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 48 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 49 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 51 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | PF3 | | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| 53 | PF4 | | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| 54 | PF5 | | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 58 | PE9 | | PCNT2_S1IN #1 | | |
| 59 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 60 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 61 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 62 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 63 | PE14 | | TIM3_CC0 #0 | LEU0_TX #2 | |
| 64 | PE15 | | TIM3_CC1 #0 | LEU0_RX #2 | |

### 5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.5. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LEU1_RX | PC7 | | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.2.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG232 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.6. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | — | — | — | — | — | PA10 | PA9 | PA8 | — | — | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | — | PB11 | — | — | PB8 | PB7 | — | — | — | — | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | — | — | — | — | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.2.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG232 is shown in the following figure.

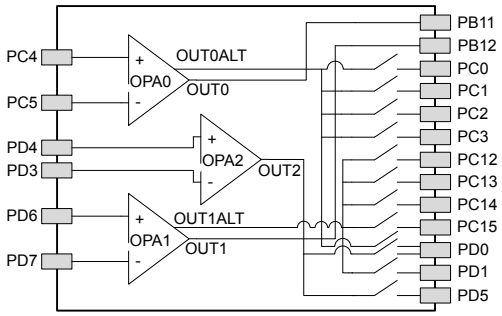



**Figure 5.4. Opamp Pinout**

### 5.3 EFM32WG280 (LQFP100)

#### 5.3.1 Pinout

The EFM32WG280 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

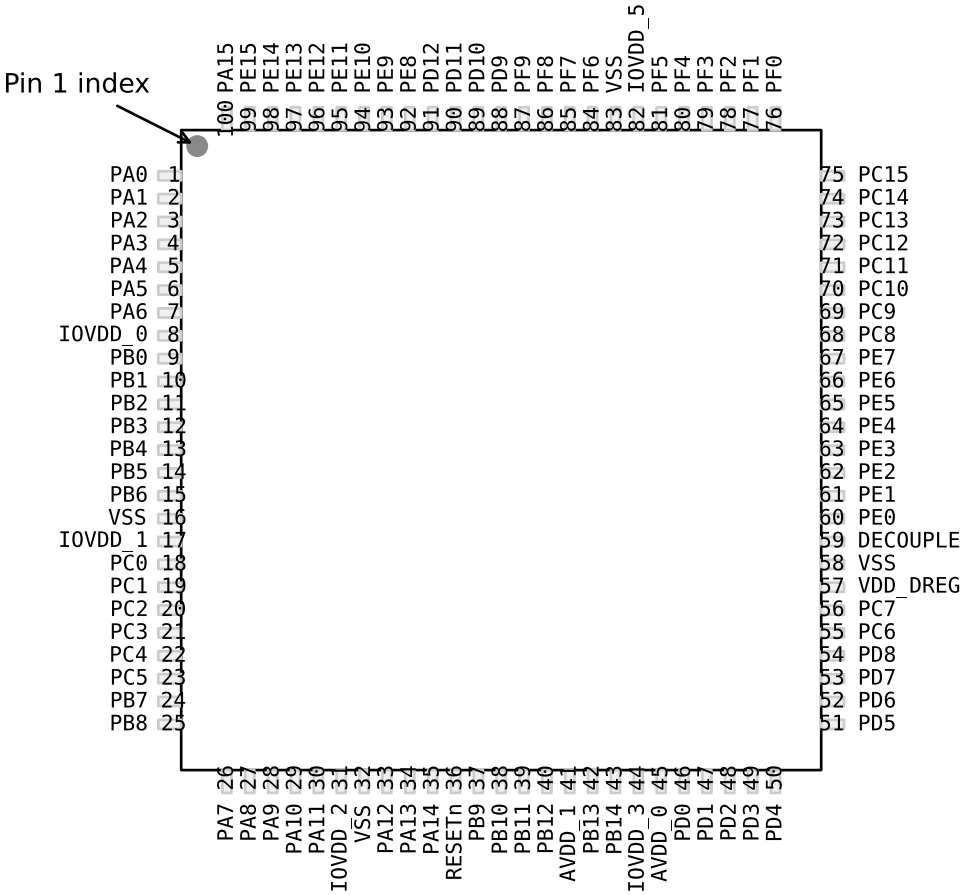



**Figure 5.5. EFM32WG280 Pinout (top view, not to scale)**

**Table 5.7. Device Pinout**

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| 2 | PA1 | | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| 10 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| 11 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| 12 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| 15 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 19 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 20 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 21 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 22 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 23 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 24 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 26 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| 27 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| 28 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| 29 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| 30 | PA11 | | EBI_HSNC #0/1/2 | | | |
| 31 | IOVDD_2 | Digital IO power supply 2. | | | | |
| 32 | VSS | Ground. | | | | |
| 33 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| 34 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| 35 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| 36 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| 37 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| 38 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| 39 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 40 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 41 | AVDD_1 | Analog power supply 1. | | | | |
| 42 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| 43 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| 44 | IOVDD_3 | Digital IO power supply 3. | | | | |
| 45 | AVDD_0 | Analog power supply 0. | | | | |
| 46 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 47 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 48 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| 49 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 50 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 51 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 52 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 53 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 54 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| 55 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 56 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 57 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| 58 | VSS | Ground. | | | | |
| 59 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| 60 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1 PCNT0_S0IN #1 | U0_TX #1 I2C1_SDA #2 | |
| 61 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1 PCNT0_S1IN #1 | U0_RX #1 I2C1_SCL #2 | |
| 62 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| 63 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| 64 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| 65 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| 66 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| 67 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| 68 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 69 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 70 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 71 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 72 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| 73 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| 74 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| 75 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| 76 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 77 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 78 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 79 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| 80 | PF4 | | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| 81 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| 87 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |
| 88 | PD9 | | EBI_CS0 #0/1/2 | | | |
| 89 | PD10 | | EBI_CS1 #0/1/2 | | | |
| 90 | PD11 | | EBI_CS2 #0/1/2 | | | |
| 91 | PD12 | | EBI_CS3 #0/1/2 | | | |
| 92 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 93 | PE9 | | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| 94 | PE10 | | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 95 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 96 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |
| 97 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| 98 | PE14 | | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 99 | PE15 | | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 100 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |

### 5.3.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.8. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG280 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.9. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.3.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG280 is shown in the following figure.

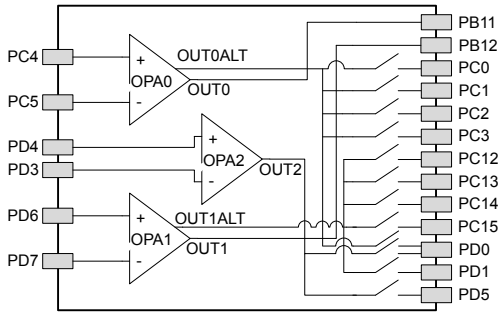



**Figure 5.6. Opamp Pinout**

## 5.4 EFM32WG290 (BGA112)

### 5.4.1 Pinout

The EFM32WG290 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

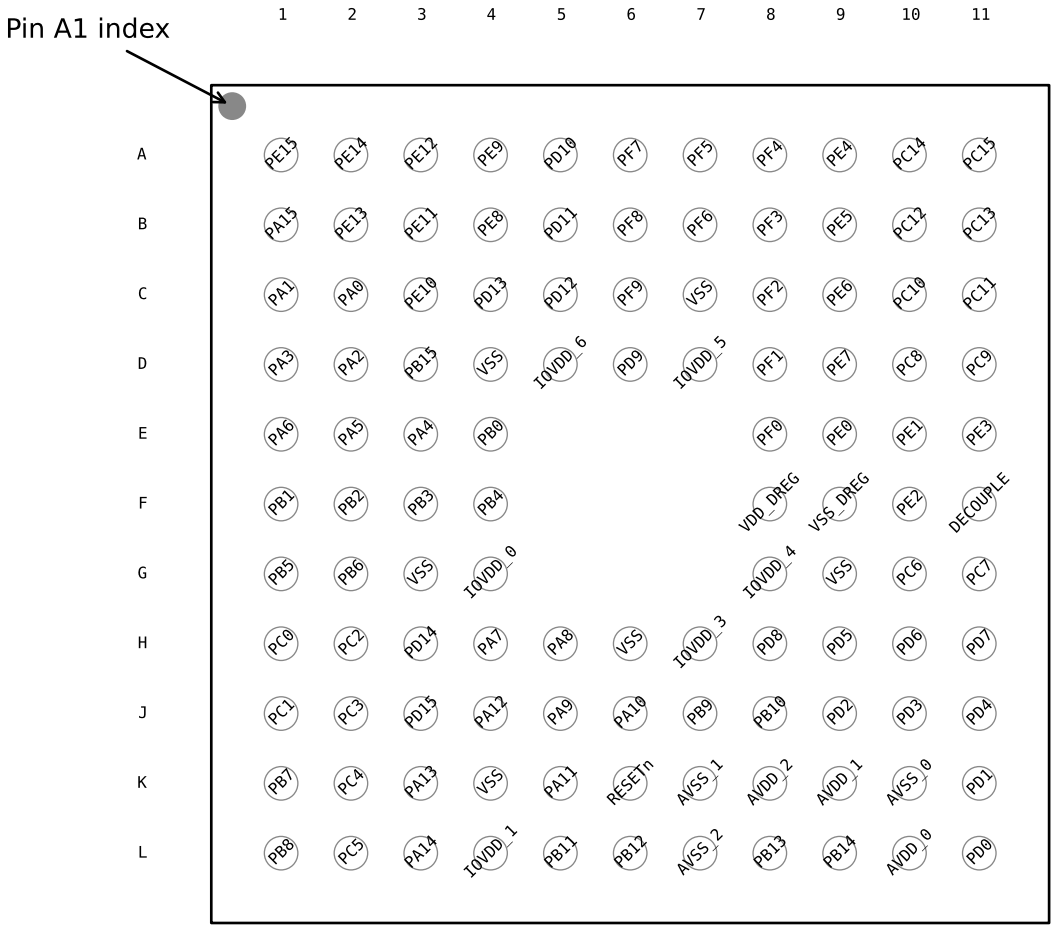



**Figure 5.7. EFM32WG290 Pinout (top view, not to scale)**

**Table 5.10. Device Pinout**

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| A3 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A4 | PE9 | | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD10 | | EBI_CS1 #0/1/2 | | | |
| A6 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A7 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| A8 | PF4 | | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| A9 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| A10 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| A11 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| B1 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| B3 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| B4 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD11 | | EBI_CS2 #0/1/2 | | | |
| B6 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B7 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B8 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| B9 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| B10 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| B11 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| C1 | PA1 | | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| C2 | PA0 | | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| C3 | PE10 | | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |
| C5 | PD12 | | EBI_CS3 #0/1/2 | | | |
| C6 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C7 | VSS | Ground. | | | | |
| C8 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| C9 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| C10 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| C11 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| D1 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| D2 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D4 | VSS | Ground. | | | | |
| D5 | IOVDD_6 | Digital IO power supply 6. | | | | |
| D6 | PD9 | | EBI_CS0 #0/1/2 | | | |
| D7 | IOVDD_5 | Digital IO power supply 5. | | | | |
| D8 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| D9 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| D10 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| D11 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| E1 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| E2 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| E3 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| E4 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| E8 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| E9 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| E10 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| E11 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| F1 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F2 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F3 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| F4 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| F8 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| F9 | VSS_DREG | Ground for on-chip voltage regulator. | | | | |
| F10 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| F11 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| G1 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| G2 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |
| G3 | VSS | Ground. | | | | |
| G4 | IOVDD_0 | Digital IO power supply 0. | | | | |
| G8 | IOVDD_4 | Digital IO power supply 4. | | | | |
| G9 | VSS | Ground. | | | | |
| G10 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| G11 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| H1 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| H2 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| H5 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| H9 | PD5 | ADC0_CH5<br>OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| H10 | PD6 | ADC0_CH6<br>DAC0_P1 /<br>OPAMP_P1 | | TIM1_CC0 #4 LE-<br>TIM0_OUT0 #0<br>PCNT0_S0IN #3 | US1_RX #2<br>I2C0_SDA #1 | LES_ALTEX0 #0<br>ACMP0_O #2<br>ETM_TD0 #0 |
| H11 | PD7 | ADC0_CH7<br>DAC0_N1 /<br>OPAMP_N1 | | TIM1_CC1 #4 LE-<br>TIM0_OUT1 #0<br>PCNT0_S1IN #3 | US1_TX #2<br>I2C0_SCL #1 | CMU_CLK0 #2<br>LES_ALTEX1 #0<br>ACMP1_O #2<br>ETM_TCLK #0 |
| J1 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| J2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| J3 | PD15 | | | | I2C0_SCL #3 | |
| J4 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| J5 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| J6 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| J7 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| J8 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| J9 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| J10 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| J11 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| K1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| K2 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| K3 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| K4 | VSS | Ground. | | | | |
| K5 | PA11 | | EBI_HSNC #0/1/2 | | | |
| K6 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |
| K11 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| L2 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| L3 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| L6 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| L9 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |
| L11 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |

### 5.4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.11. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG290 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.12. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.4.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG290 is shown in the following figure.

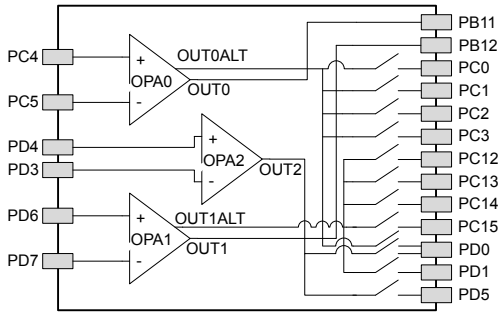



**Figure 5.8. Opamp Pinout**

## 5.5 EFM32WG295 (BGA120)

### 5.5.1 Pinout

The EFM32WG295 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

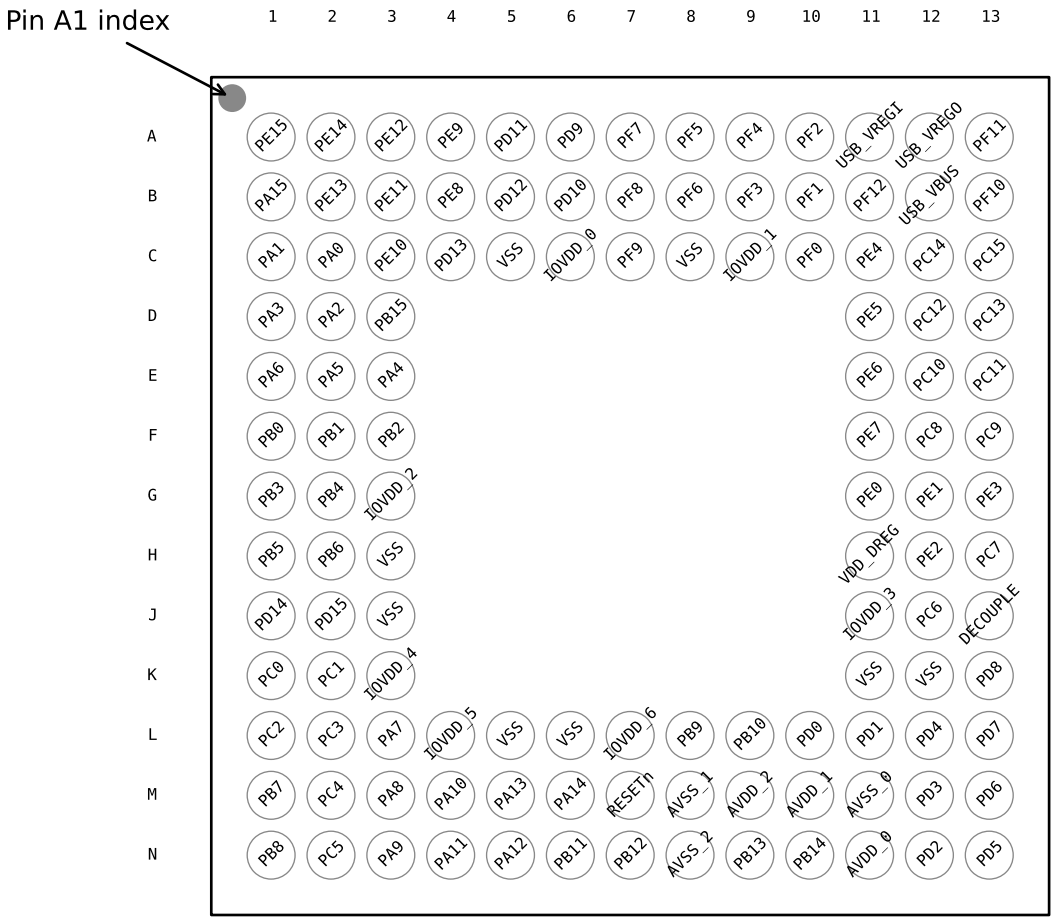



**Figure 5.9. EFM32WG295 Pinout (top view, not to scale)**

**Table 5.13. Device Pinout**

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| A3 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A4 | PE9 | | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD11 | | EBI_CS2 #0/1/2 | | | |
| A6 | PD9 | | EBI_CS0 #0/1/2 | | | |
| A7 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A8 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| A9 | PF4 | | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| A10 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| A11 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | | |
| A12 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| A13 | PF11 | | | | U1_RX #1 | |
| B1 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| B3 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| B4 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD12 | | EBI_CS3 #0/1/2 | | | |
| B6 | PD10 | | EBI_CS1 #0/1/2 | | | |
| B7 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B8 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B9 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1<br>ETM_TD3 #1 |
| B10 | PF1 | | | TIM0_CC1 #5 LE-<br>TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO<br>#0/1/2/3<br>GPIO_EM4WU3 |
| B11 | PF12 | | | | | |
| B12 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| B13 | PF10 | | | | U1_TX #1 | |
| C1 | PA1 | | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| C2 | PA0 | | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| C3 | PE10 | | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |
| C5 | VSS | Ground. | | | | |
| C6 | IOVDD_0 | Digital IO power supply 0. | | | | |
| C7 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C8 | VSS | Ground. | | | | |
| C9 | IOVDD_1 | Digital IO power supply 1. | | | | |
| C10 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| C11 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| C12 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| C13 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| D1 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0 ETM_TD1 #3 |
| D2 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D11 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| D12 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| D13 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| E1 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| E2 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| E3 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0 ETM_TD2 #3 |
| E11 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| E12 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| E13 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| F1 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| F2 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F3 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F11 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| F12 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| F13 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| G1 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| G2 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| G3 | IOVDD_2 | Digital IO power supply 2. | | | | |
| G11 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| G12 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| G13 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| H1 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| H2 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |
| H3 | VSS | Ground. | | | | |
| H11 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| H12 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| H13 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| J1 | PD14 | | | | I2C0_SDA #3 | |
| J2 | PD15 | | | | I2C0_SCL #3 | |
| J3 | VSS | Ground. | | | | |
| J11 | IOVDD_3 | Digital IO power supply 3. | | | | |
| J12 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| J13 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| K1 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| K2 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| K3 | IOVDD_4 | Digital IO power supply 4. | | | | |
| K11 | VSS | Ground. | | | | |
| K12 | VSS | Ground. | | | | |
| K13 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| L1 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| L2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| L3 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| L4 | IOVDD_5 | Digital IO power supply 5. | | | | |
| L5 | VSS | Ground. | | | | |
| L6 | VSS | Ground. | | | | |
| L7 | IOVDD_6 | Digital IO power supply 6. | | | | |
| L8 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| L9 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| L10 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| L11 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L12 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| L13 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| M1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| M2 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| M3 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| M4 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| M5 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| M6 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| M7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| M8 | AVSS_1 | Analog ground 1. | | | | |
| M9 | AVDD_2 | Analog power supply 2. | | | | |
| M10 | AVDD_1 | Analog power supply 1. | | | | |
| M11 | AVSS_0 | Analog ground 0. | | | | |
| M12 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| M13 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| N1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| N2 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| N3 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| N4 | PA11 | | EBI_HSNC #0/1/2 | | | |
| N5 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| N6 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| N7 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| N8 | AVSS_2 | Analog ground 2. | | | | |
| N9 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| N10 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| N11 | AVDD_0 | Analog power supply 0. | | | | |
| N12 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| N13 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |

### 5.5.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.14. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG295 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.15. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.5.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG295 is shown in the following figure.

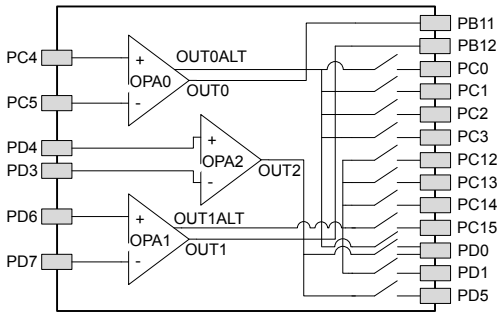



**Figure 5.10. Opamp Pinout**

## 5.6 EFM32WG330 (QFN64)

### 5.6.1 Pinout

The EFM32WG330 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

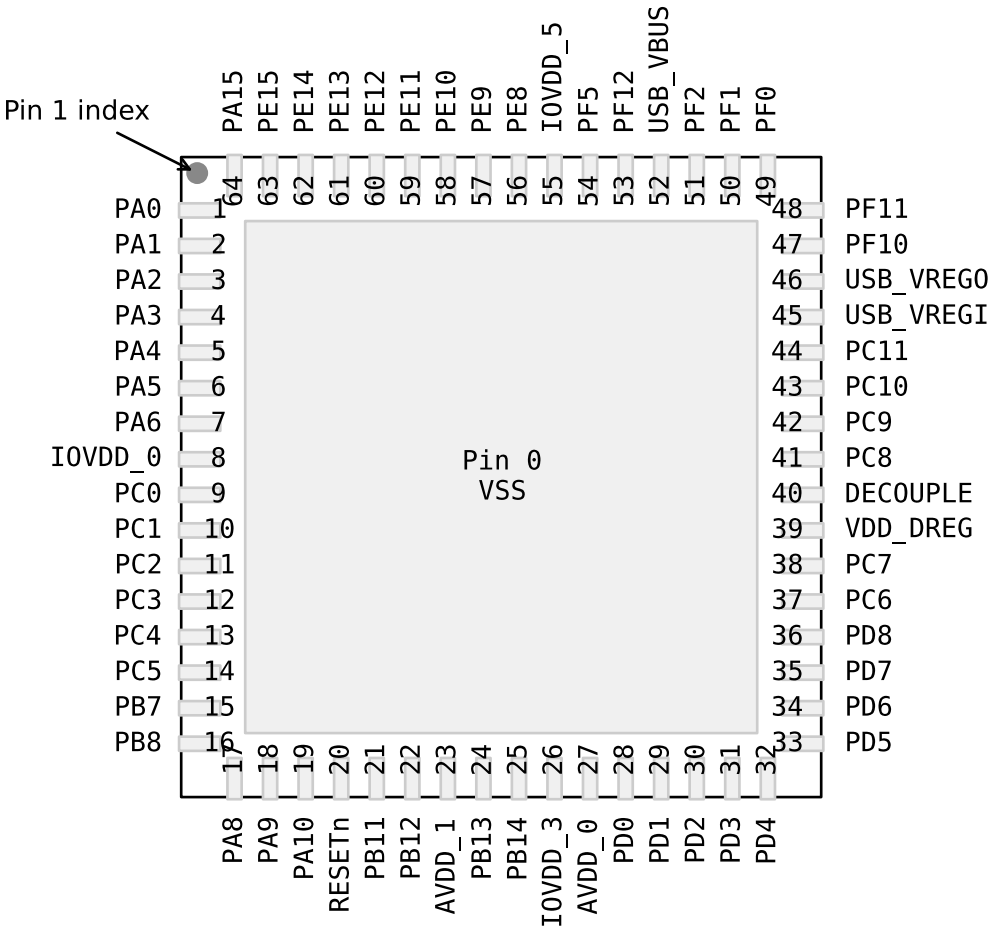



**Figure 5.11. EFM32WG330 Pinout (top view, not to scale)**

**Table 5.16. Device Pinout**

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | | TIM0_CDTI0 #0 | | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | | TIM0_CDTI1 #0 | | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5 US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0 PRS_CH2<br>#0 |
| 10 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5 US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0 PRS_CH3<br>#0 |
| 11 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 12 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 13 | PC4 | ACMP0_CH4<br>DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-<br>TIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA<br>#0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5<br>DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL<br>#0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK<br>#0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA8 | | TIM2_CC0 #0 | | |
| 18 | PA9 | | TIM2_CC1 #0 | | |
| 19 | PA10 | | TIM2_CC2 #0 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 /<br>OPAMP_OUT0 | TIM1_CC2 #3 LE-<br>TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 22 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX<br>#1 | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 42 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 43 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| 45 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | |
| 46 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | |
| 47 | PF10 | | | USB_DM | |
| 48 | PF11 | | | USB_DP | |
| 49 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 51 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| 52 | USB_VBUS | USB 5.0 V VBUS input. | | | |
| 53 | PF12 | | | USB_ID | |
| 54 | PF5 | | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 57 | PE9 | | PCNT2_S1IN #1 | | |
| 58 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| 60 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |
| 61 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| 62 | PE14 | | TIM3_CC0 #0 | LEU0_TX #2 | |
| 63 | PE15 | | TIM3_CC1 #0 | LEU0_RX #2 | |
| 64 | PA15 | | TIM3_CC2 #0 | | |

### 5.6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.17. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | | | | | | | Timer 3 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.6.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG330 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.18. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | — | — | — | — | PA10 | PA9 | PA8 | — | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | — | — | PB8 | PB7 | — | — | — | — | — | — | — |
| Port C | — | — | — | — | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | — | — | — | — | — | — | — | — |
| Port F | — | — | — | PF12 | PF11 | PF10 | — | — | — | — | PF5 | — | — | PF2 | PF1 | PF0 |

### 5.6.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG330 is shown in the following figure.

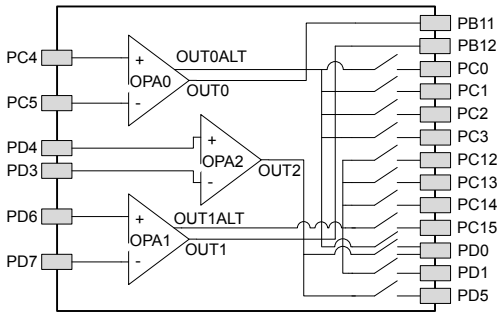



**Figure 5.12. Opamp Pinout**

### 5.7 EFM32WG332 (TQFP64)

#### 5.7.1 Pinout

The EFM32WG332 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

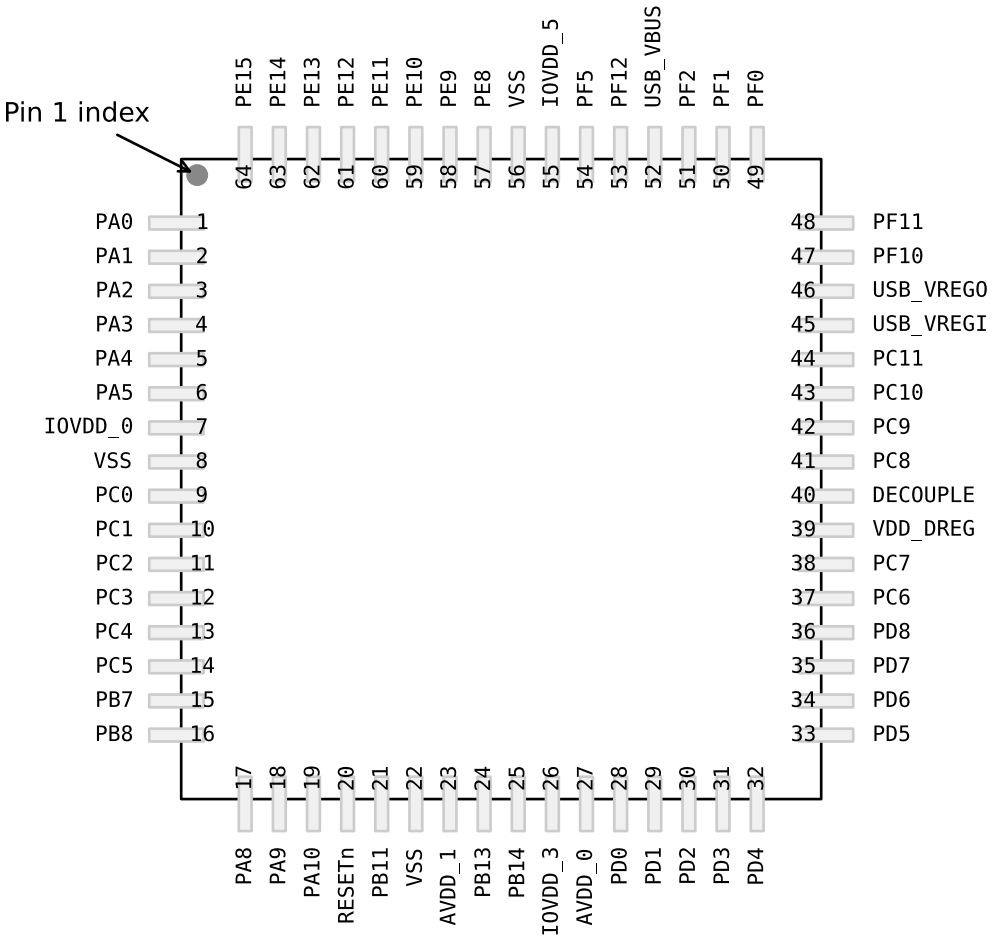



**Figure 5.13. EFM32WG332 Pinout (top view, not to scale)**

**Table 5.19. Device Pinout**

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PA3 | | TIM0_CDTI0 #0 | | LES_ALTEX2 #0 ETM_TD1 #3 |
| 5 | PA4 | | TIM0_CDTI1 #0 | | LES_ALTEX3 #0 ETM_TD2 #3 |
| 6 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 10 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 11 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 12 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 13 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA8 | | TIM2_CC0 #0 | | |
| 18 | PA9 | | TIM2_CC1 #0 | | |
| 19 | PA10 | | TIM2_CC2 #0 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 42 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 43 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| 45 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | |
| 46 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | |
| 47 | PF10 | | | USB_DM | |
| 48 | PF11 | | | USB_DP | |
| 49 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 51 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 52 | USB_VBUS | USB 5.0 V VBUS input. | | | |
| 53 | PF12 | | | USB_ID | |
| 54 | PF5 | | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 58 | PE9 | | PCNT2_S1IN #1 | | |
| 59 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 60 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 61 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 62 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 63 | PE14 | | TIM3_CC0 #0 | LEU0_TX #2 | |
| 64 | PE15 | | TIM3_CC1 #0 | LEU0_RX #2 | |

### 5.7.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.20. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PCNT1_S0IN | PC4 | | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| US0_CLK | PE12 | | PC9 | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.7.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG332 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.21. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | - | - | - | - | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | - | - | - | - | - | - | - | - |
| Port F | - | - | - | PF12 | PF11 | PF10 | - | - | - | - | PF5 | - | - | PF2 | PF1 | PF0 |

### 5.7.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG332 is shown in the following figure.

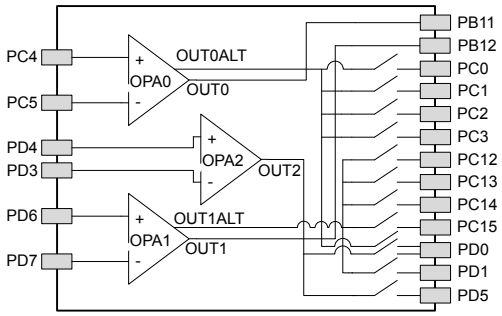



**Figure 5.14. Opamp Pinout**

### 5.8 EFM32WG360 (CSP81)

#### 5.8.1 Pinout

The EFM32WG360 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

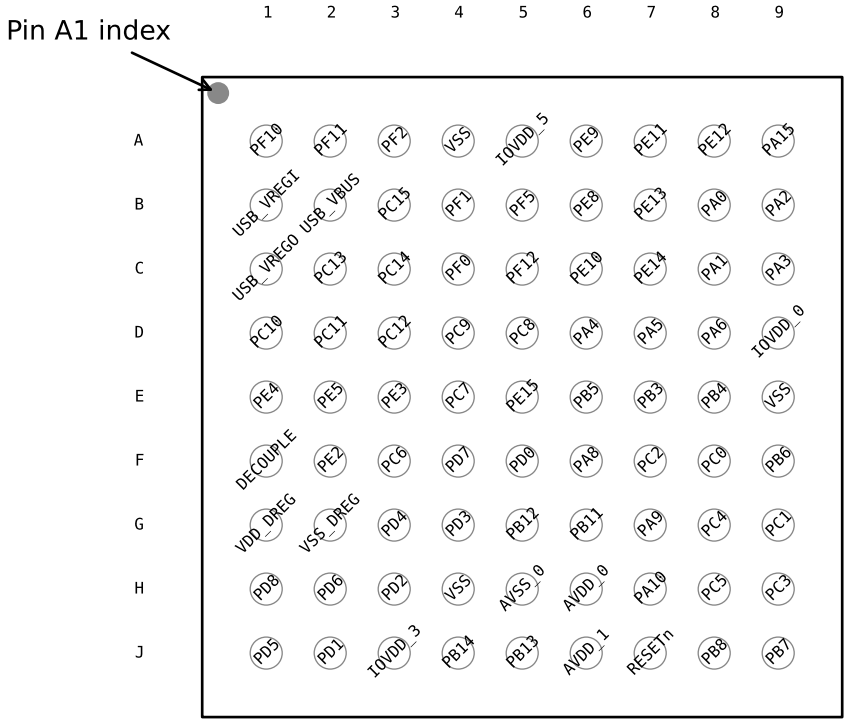



**Figure 5.15. EFM32WG360 Pinout (top view, not to scale)**

**Table 5.22. Device Pinout**

| CSP81 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| A1 | PF10 | | | U1_TX #1 USB_DM | |
| A2 | PF11 | | | U1_RX #1 USB_DP | |
| A3 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |

| CSP81 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| A4 | VSS | Ground. | | | |
| A5 | IOVDD_5 | Digital IO power supply 5. | | | |
| A6 | PE9 | | PCNT2_S1IN #1 | | |
| A7 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| A8 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| A9 | PA15 | | TIM3_CC2 #0 | | |
| B1 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | |
| B2 | USB_VBUS | USB 5.0 V VBUS input. | | | |
| B3 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| B4 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| B5 | PF5 | | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| B6 | PE8 | | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B7 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| B8 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| B9 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| C1 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | |
| C2 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| C3 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| C4 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| C5 | PF12 | | | USB_ID | |
| C6 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C7 | PE14 | | TIM3_CC0 #0 | LEU0_TX #2 | |
| C8 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| C9 | PA3 | | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0 ETM_TD1 #3 |
| D1 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| D2 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |

| CSP81 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| D3 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| D4 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| D5 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| D6 | PA4 | | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0 ETM_TD2 #3 |
| D7 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| D8 | PA6 | | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| D9 | IOVDD_0 | Digital IO power supply 0. | | | |
| E1 | PE4 | | | US0_CS #1 | |
| E2 | PE5 | | | US0_CLK #1 | |
| E3 | PE3 | BU_STAT | | U1_RX #3 | ACMP1_O #1 |
| E4 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| E5 | PE15 | | TIM3_CC1 #0 | LEU0_RX #2 | |
| E6 | PB5 | | | US2_CLK #1 | |
| E7 | PB3 | | PCNT1_S0IN #1 | US2_TX #1 | |
| E8 | PB4 | | PCNT1_S1IN #1 | US2_RX #1 | |
| E9 | VSS | Ground. | | | |
| F1 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C^{DECOUPLE}$ is required at this pin. | | | |
| F2 | PE2 | BU_VOUT | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| F3 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| F4 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| F5 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| F6 | PA8 | | TIM2_CC0 #0 | | |
| F7 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| F8 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| F9 | PB6 | | | US2_CS #1 | |

| CSP81 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| G1 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| G2 | VSS_DREG | Ground for on-chip voltage regulator. | | | |
| G3 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| G4 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| G5 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| G6 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| G7 | PA9 | | TIM2_CC1 #0 | | |
| G8 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| G9 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| H1 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| H2 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| H3 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| H4 | VSS | Ground. | | | |
| H5 | AVSS_0 | Analog ground 0. | | | |
| H6 | AVDD_0 | Analog power supply 0. | | | |
| H7 | PA10 | | TIM2_CC2 #0 | | |
| H8 | PC5 | ACMP0_CH5 DAC0_N0 / PD6OPAMP_N0 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| H9 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| J1 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| J2 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| J3 | IOVDD_3 | Digital IO power supply 3. | | | |
| J4 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| J5 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| J6 | AVDD_1 | Analog power supply 1. | | | |
| J7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |

| CSP81 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| J8 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| J9 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |

### 5.8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.23. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | | PC13 | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | | PC14 | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM2_CC2 | PA10 | | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | | | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | | | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.8.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG360 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.24. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | - | - | - | - | PA10 | PA9 | PA8 | - | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | PB12 | PB11 | - | - | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | - | - | - |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | - | - | PE5 | PE4 | PE3 | PE2 | - | - |
| Port F | - | - | - | PF12 | PF11 | PF10 | - | - | - | - | PF5 | - | - | PF2 | PF1 | PF0 |

### 5.8.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG360 is shown in the following figure.

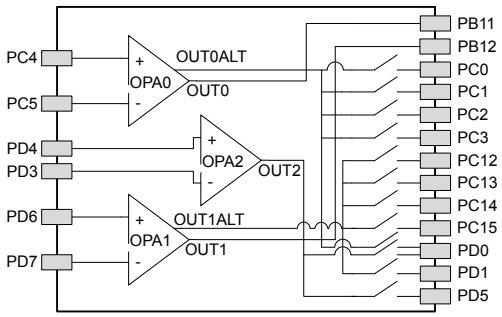



**Figure 5.16. Opamp Pinout**

### 5.9 EFM32WG380 (LQFP100)

#### 5.9.1 Pinout

The EFM32WG380 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

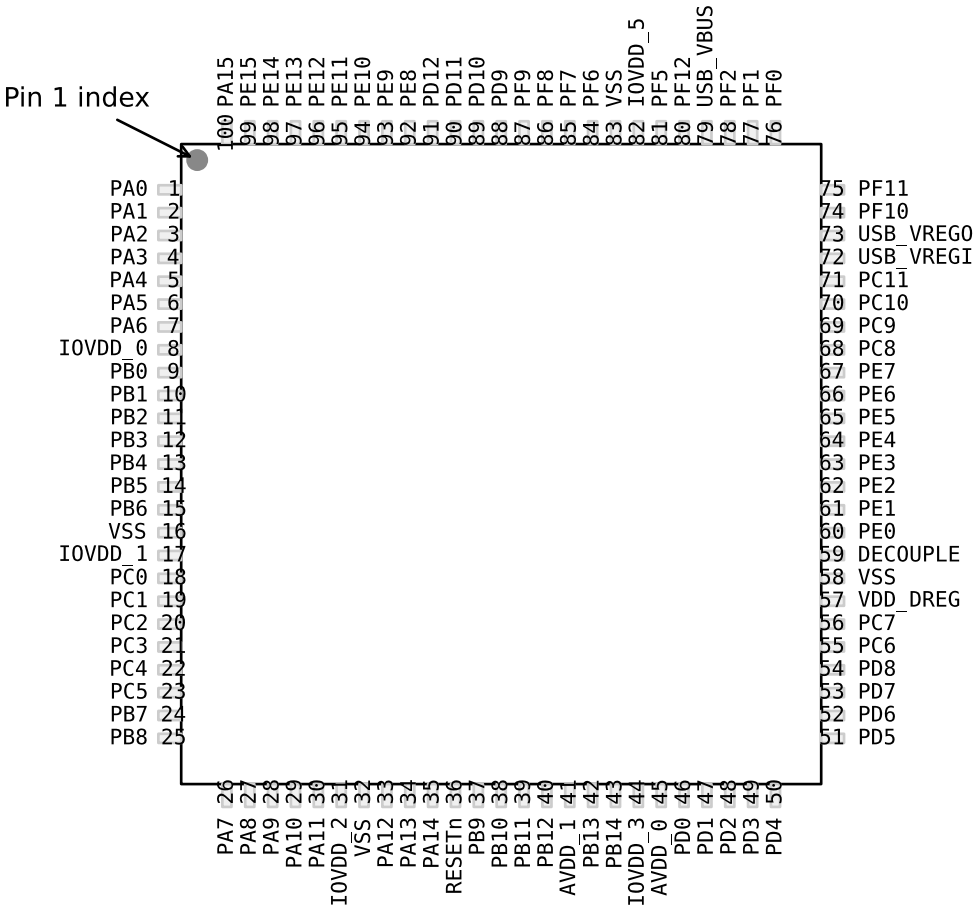



**Figure 5.17. EFM32WG380 Pinout (top view, not to scale)**

**Table 5.25. Device Pinout**

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| 2 | PA1 | | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| 10 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| 11 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| 12 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| 15 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 19 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 20 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 21 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 22 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 23 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 24 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 26 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| 27 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| 28 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| 29 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| 30 | PA11 | | EBI_HSNC #0/1/2 | | | |
| 31 | IOVDD_2 | Digital IO power supply 2. | | | | |
| 32 | VSS | Ground. | | | | |
| 33 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| 34 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| 35 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| 36 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| 37 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| 38 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| 39 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 40 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 41 | AVDD_1 | Analog power supply 1. | | | | |
| 42 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| 43 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| 44 | IOVDD_3 | Digital IO power supply 3. | | | | |
| 45 | AVDD_0 | Analog power supply 0. | | | | |
| 46 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 47 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 48 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| 49 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 50 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 51 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 52 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 53 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 54 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| 55 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 56 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 57 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| 58 | VSS | Ground. | | | | |
| 59 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| 60 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1 PCNT0_S0IN #1 | U0_TX #1 I2C1_SDA #2 | |
| 61 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1 PCNT0_S1IN #1 | U0_RX #1 I2C1_SCL #2 | |
| 62 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| 63 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| 64 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| 65 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| 66 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| 67 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| 68 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 69 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 70 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 71 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 72 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | | |
| 73 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| 74 | PF10 | | | | U1_TX #1 USB_DM | |
| 75 | PF11 | | | | U1_RX #1 USB_DP | |
| 76 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 77 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 78 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 79 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| 80 | PF12 | | | | USB_ID | |
| 81 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| 87 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |
| 88 | PD9 | | EBI_CS0 #0/1/2 | | | |
| 89 | PD10 | | EBI_CS1 #0/1/2 | | | |
| 90 | PD11 | | EBI_CS2 #0/1/2 | | | |
| 91 | PD12 | | EBI_CS3 #0/1/2 | | | |
| 92 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 93 | PE9 | | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| 94 | PE10 | | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 95 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 96 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 97 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 98 | PE14 | | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 99 | PE15 | | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 100 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |

### 5.9.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.26. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | | PF8 | | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | PB2 | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| U0_RX | PF7 | PE1 | PA4 | | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.9.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG380 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.27. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | — | — | — | — | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | — | — | PF2 | PF1 | PF0 |

### 5.9.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG380 is shown in the following figure.

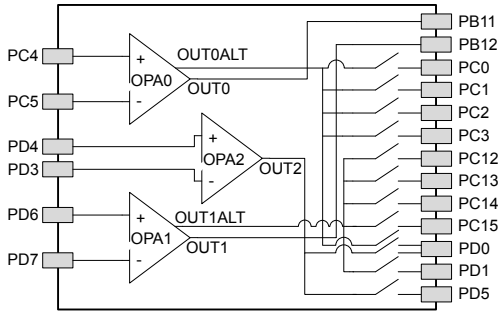



**Figure 5.18. Opamp Pinout**

### 5.10 EFM32WG390 (BGA112)

#### 5.10.1 Pinout

The EFM32WG390 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

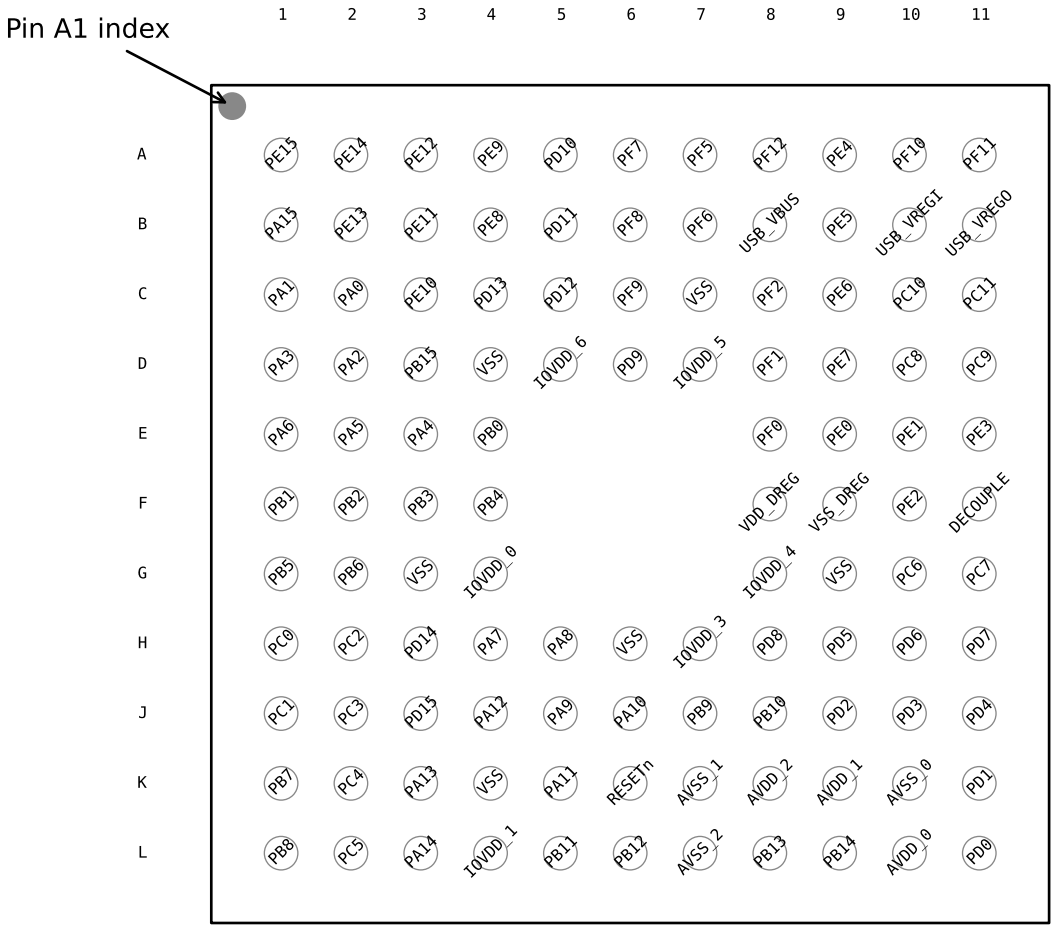



**Figure 5.19. EFM32WG390 Pinout (top view, not to scale)**

**Table 5.28. Device Pinout**

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| A3 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A4 | PE9 | | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD10 | | EBI_CS1 #0/1/2 | | | |
| A6 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A7 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| A8 | PF12 | | | | USB_ID | |
| A9 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| A10 | PF10 | | | | U1_TX #1 USB_DM | |
| A11 | PF11 | | | | U1_RX #1 USB_DP | |
| B1 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| B3 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| B4 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD11 | | EBI_CS2 #0/1/2 | | | |
| B6 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B7 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B8 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| B9 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| B10 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | | |
| B11 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| C1 | PA1 | | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| C2 | PA0 | | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| C3 | PE10 | | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |
| C5 | PD12 | | EBI_CS3 #0/1/2 | | | |
| C6 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |
| C7 | VSS | Ground. | | | | |
| C8 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| C9 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| C10 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| C11 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| D1 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| D2 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D4 | VSS | Ground. | | | | |
| D5 | IOVDD_6 | Digital IO power supply 6. | | | | |
| D6 | PD9 | | EBI_CS0 #0/1/2 | | | |
| D7 | IOVDD_5 | Digital IO power supply 5. | | | | |
| D8 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| D9 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| D10 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| D11 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| E1 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| E2 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| E3 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| E4 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| E8 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| E9 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| E10 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| E11 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| F1 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F2 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F3 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| F4 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| F8 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| F9 | VSS_DREG | Ground for on-chip voltage regulator. | | | | |
| F10 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| F11 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| G1 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| G2 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| G3 | VSS | Ground. | | | | |
| G4 | IOVDD_0 | Digital IO power supply 0. | | | | |
| G8 | IOVDD_4 | Digital IO power supply 4. | | | | |
| G9 | VSS | Ground. | | | | |
| G10 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| G11 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| H1 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| H2 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| H5 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| H9 | PD5 | ADC0_CH5<br>OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| H10 | PD6 | ADC0_CH6<br>DAC0_P1 /<br>OPAMP_P1 | | TIM1_CC0 #4 LE-<br>TIM0_OUT0 #0<br>PCNT0_S0IN #3 | US1_RX #2<br>I2C0_SDA #1 | LES_ALTEX0 #0<br>ACMP0_O #2<br>ETM_TD0 #0 |
| H11 | PD7 | ADC0_CH7<br>DAC0_N1 /<br>OPAMP_N1 | | TIM1_CC1 #4 LE-<br>TIM0_OUT1 #0<br>PCNT0_S1IN #3 | US1_TX #2<br>I2C0_SCL #1 | CMU_CLK0 #2<br>LES_ALTEX1 #0<br>ACMP1_O #2<br>ETM_TCLK #0 |
| J1 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| J2 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| J3 | PD15 | | | | I2C0_SCL #3 | |
| J4 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| J5 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| J6 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| J7 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| J8 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| J9 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0<br>US1_CLK #1 | DBG_SWO #3 |
| J10 | PD3 | ADC0_CH3<br>OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| J11 | PD4 | ADC0_CH4<br>OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| K1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| K2 | PC4 | ACMP0_CH4<br>DAC0_P0 /<br>OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-<br>TIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |
| K3 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| K4 | VSS | Ground. | | | | |
| K5 | PA11 | | EBI_HSNC #0/1/2 | | | |
| K6 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |
| K11 | PD1 | ADC0_CH1<br>DAC0_OUT1ALT<br>#4/<br>OPAMP_OUT1ALT | | TIM0_CC0 #3<br>PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| L2 | PC5 | ACMP0_CH5<br>DAC0_N0 /<br>OPAMP_N0 | EBI_NANDWEn<br>#0/1/2 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| L3 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OUT0 /<br>OPAMP_OUT0 | | TIM1_CC2 #3 LE-<br>TIM0_OUT0 #1 | I2C1_SDA #1 | |
| L6 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_P | | | US0_CLK #4/5<br>LEU0_TX #1 | |
| L9 | PB14 | HFXTAL_N | | | US0_CS #4/5<br>LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| L11 | PD0 | ADC0_CH0<br>DAC0_OUT0ALT #4/<br>OPAMP_OUT0ALT<br>OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |

### 5.10.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.29. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | | PF8 | | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | PB2 | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| U0_RX | PF7 | PE1 | PA4 | | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.10.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG390 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.30. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | — | — | — | — | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | — | — | PF2 | PF1 | PF0 |

### 5.10.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG390 is shown in the following figure.

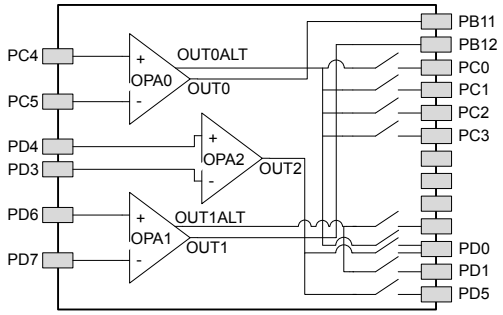



**Figure 5.20. Opamp Pinout**

## 5.11 EFM32WG395 (BGA120)

### 5.11.1 Pinout

The EFM32WG395 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

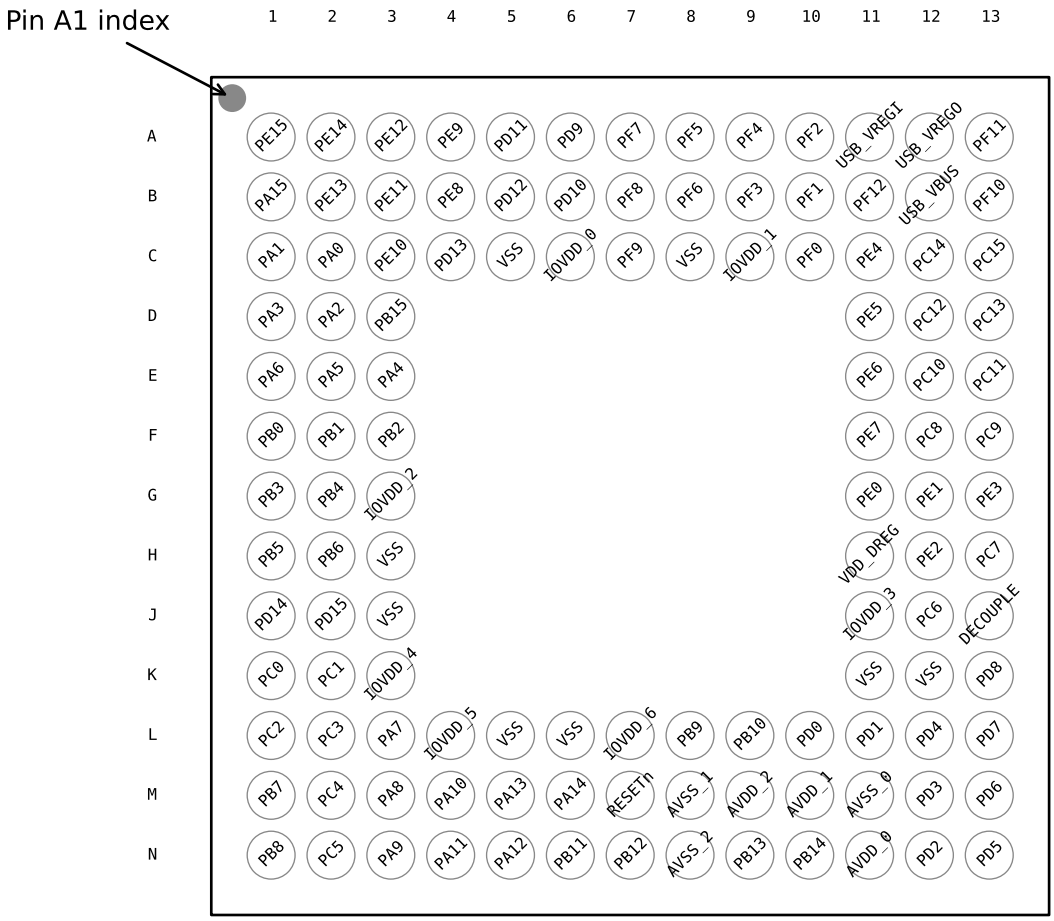



**Figure 5.21. EFM32WG395 Pinout (top view, not to scale)**

**Table 5.31. Device Pinout**

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| A3 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A4 | PE9 | | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD11 | | EBI_CS2 #0/1/2 | | | |
| A6 | PD9 | | EBI_CS0 #0/1/2 | | | |
| A7 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A8 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| A9 | PF4 | | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| A10 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| A11 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | | |
| A12 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| A13 | PF11 | | | | U1_RX #1 USB_DP | |
| B1 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| B3 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| B4 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD12 | | EBI_CS3 #0/1/2 | | | |
| B6 | PD10 | | EBI_CS1 #0/1/2 | | | |
| B7 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B8 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B9 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1<br>ETM_TD3 #1 |
| B10 | PF1 | | | TIM0_CC1 #5 LE-<br>TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO<br>#0/1/2/3<br>GPIO_EM4WU3 |
| B11 | PF12 | | | | USB_ID | |
| B12 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| B13 | PF10 | | | | U1_TX #1 USB_DM | |
| C1 | PA1 | | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| C2 | PA0 | | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| C3 | PE10 | | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |
| C5 | VSS | Ground. | | | | |
| C6 | IOVDD_0 | Digital IO power supply 0. | | | | |
| C7 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C8 | VSS | Ground. | | | | |
| C9 | IOVDD_1 | Digital IO power supply 1. | | | | |
| C10 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| C11 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| C12 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| C13 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| D1 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0 ETM_TD1 #3 |
| D2 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D11 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| D12 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| D13 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| E1 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| E2 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| E3 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0 ETM_TD2 #3 |
| E11 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| E12 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| E13 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| F1 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| F2 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F3 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F11 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| F12 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| F13 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| G1 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| G2 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| G3 | IOVDD_2 | Digital IO power supply 2. | | | | |
| G11 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| G12 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| G13 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| H1 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| H2 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |
| H3 | VSS | Ground. | | | | |
| H11 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| H12 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| H13 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| J1 | PD14 | | | | I2C0_SDA #3 | |
| J2 | PD15 | | | | I2C0_SCL #3 | |
| J3 | VSS | Ground. | | | | |
| J11 | IOVDD_3 | Digital IO power supply 3. | | | | |
| J12 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| J13 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| K1 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| K2 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| K3 | IOVDD_4 | Digital IO power supply 4. | | | | |
| K11 | VSS | Ground. | | | | |
| K12 | VSS | Ground. | | | | |
| K13 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| L1 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| L2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| L3 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| L4 | IOVDD_5 | Digital IO power supply 5. | | | | |
| L5 | VSS | Ground. | | | | |
| L6 | VSS | Ground. | | | | |
| L7 | IOVDD_6 | Digital IO power supply 6. | | | | |
| L8 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| L9 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| L10 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| L11 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L12 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| L13 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| M1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| M2 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| M3 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| M4 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| M5 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| M6 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| M7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| M8 | AVSS_1 | Analog ground 1. | | | | |
| M9 | AVDD_2 | Analog power supply 2. | | | | |
| M10 | AVDD_1 | Analog power supply 1. | | | | |
| M11 | AVSS_0 | Analog ground 0. | | | | |
| M12 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| M13 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| N1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| N2 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| N3 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| N4 | PA11 | | EBI_HSNC #0/1/2 | | | |
| N5 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| N6 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| N7 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| N8 | AVSS_2 | Analog ground 2. | | | | |
| N9 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| N10 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| N11 | AVDD_0 | Analog power supply 0. | | | | |
| N12 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| N13 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |

### 5.11.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.32. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_ VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_ VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_ VRE- GO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.11.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG395 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.33. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.11.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG395 is shown in the following figure.

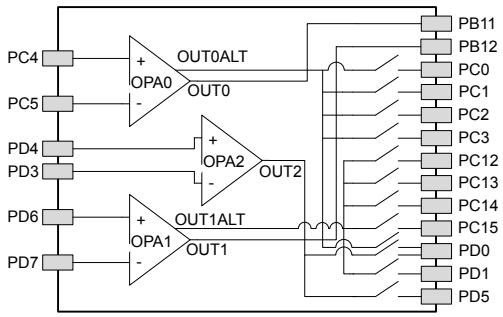



**Figure 5.22. Opamp Pinout**

### 5.12 EFM32WG840 (QFN64)

#### 5.12.1 Pinout

The EFM32WG840 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

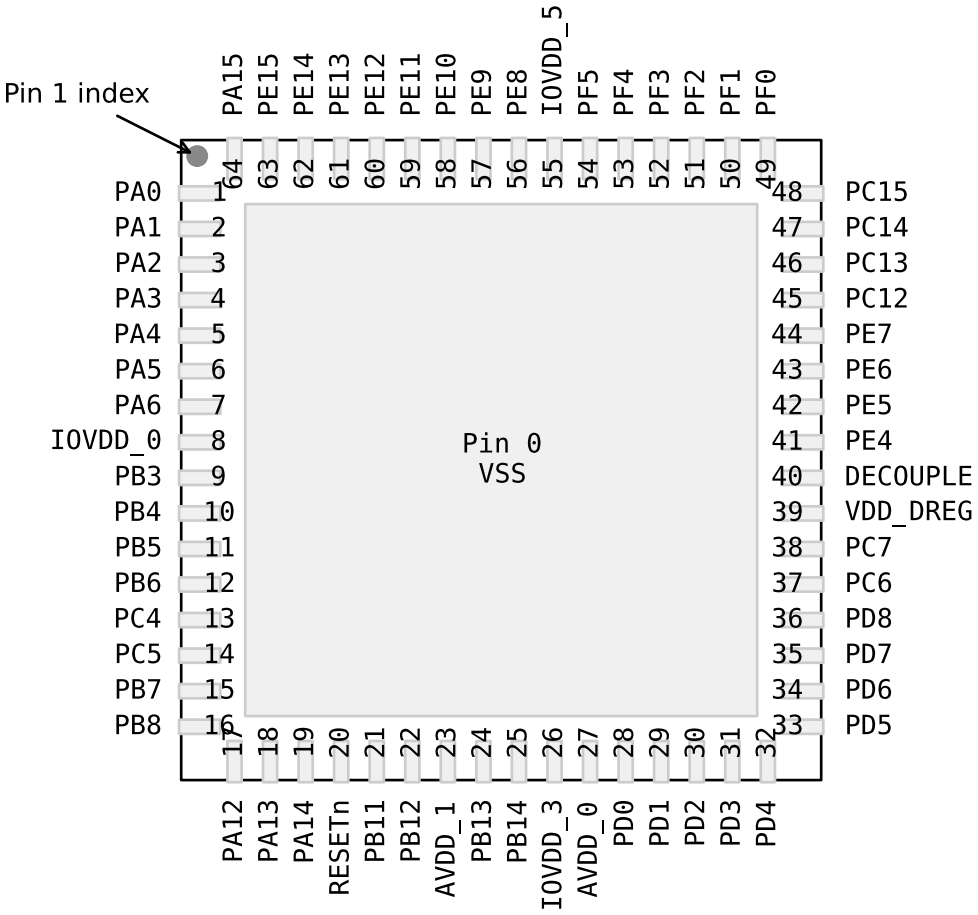



**Figure 5.23. EFM32WG840 Pinout (top view, not to scale)**

**Table 5.34. Device Pinout**

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | LCD_SEG16 | TIM0_CDTI0 #0 | | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | LCD_SEG17 | TIM0_CDTI1 #0 | | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | LCD_SEG19 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PB3 | LCD_SEG20/<br>LCD_COM4 | PCNT1_S0IN #1 | US2_TX #1 | |
| 10 | PB4 | LCD_SEG21/<br>LCD_COM5 | PCNT1_S1IN #1 | US2_RX #1 | |
| 11 | PB5 | LCD_SEG22/<br>LCD_COM6 | | US2_CLK #1 | |
| 12 | PB6 | LCD_SEG23/<br>LCD_COM7 | | US2_CS #1 | |
| 13 | PC4 | ACMP0_CH4<br>DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-<br>TIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA<br>#0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5<br>DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL<br>#0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK<br>#0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | TIM2_CC0 #1 | | |
| 18 | PA13 | LCD_BCAP_N | TIM2_CC1 #1 | | |
| 19 | PA14 | LCD_BEXT | TIM2_CC2 #1 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 /<br>OPAMP_OUT0 | TIM1_CC2 #3 LE-<br>TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 22 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX<br>#1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 45 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | CMU_CLK0 #1 LES_CH12 #0 |
| 46 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 47 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 48 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 49 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 50 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 51 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | PF3 | LCD_SEG1 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| 53 | PF4 | LCD_SEG2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| 54 | PF5 | LCD_SEG3 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | LCD_SEG4 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 57 | PE9 | LCD_SEG5 | PCNT2_S1IN #1 | | |
| 58 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 60 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 61 | PE13 | LCD_SEG9 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 62 | PE14 | LCD_SEG10 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 63 | PE15 | LCD_SEG11 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 64 | PA15 | LCD_SEG12 | TIM3_CC2 #0 | | |

### 5.12.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.35. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | | | | | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | | | | | | I2C1 Serial Clock Line input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | PA12 | | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | PA13 | | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | PA14 | | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | | | | | | | Timer 3 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | PE12 | PB8 | | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | PE13 | PB7 | | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.12.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG840 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.36. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | — | — | — | — | — | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | — | — | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | — | — | — | — | PC7 | PC6 | PC5 | PC4 | — | — | — | — |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.12.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG840 is shown in the following figure.

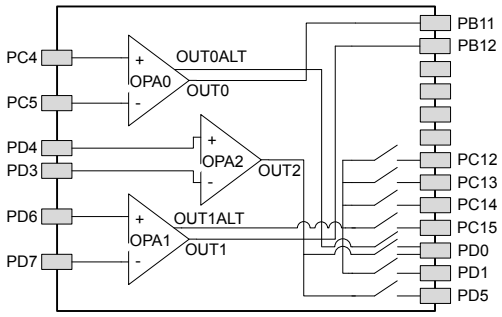



**Figure 5.24. Opamp Pinout**

### 5.13 EFM32WG842 (TQFP64)

#### 5.13.1 Pinout

The EFM32WG842 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

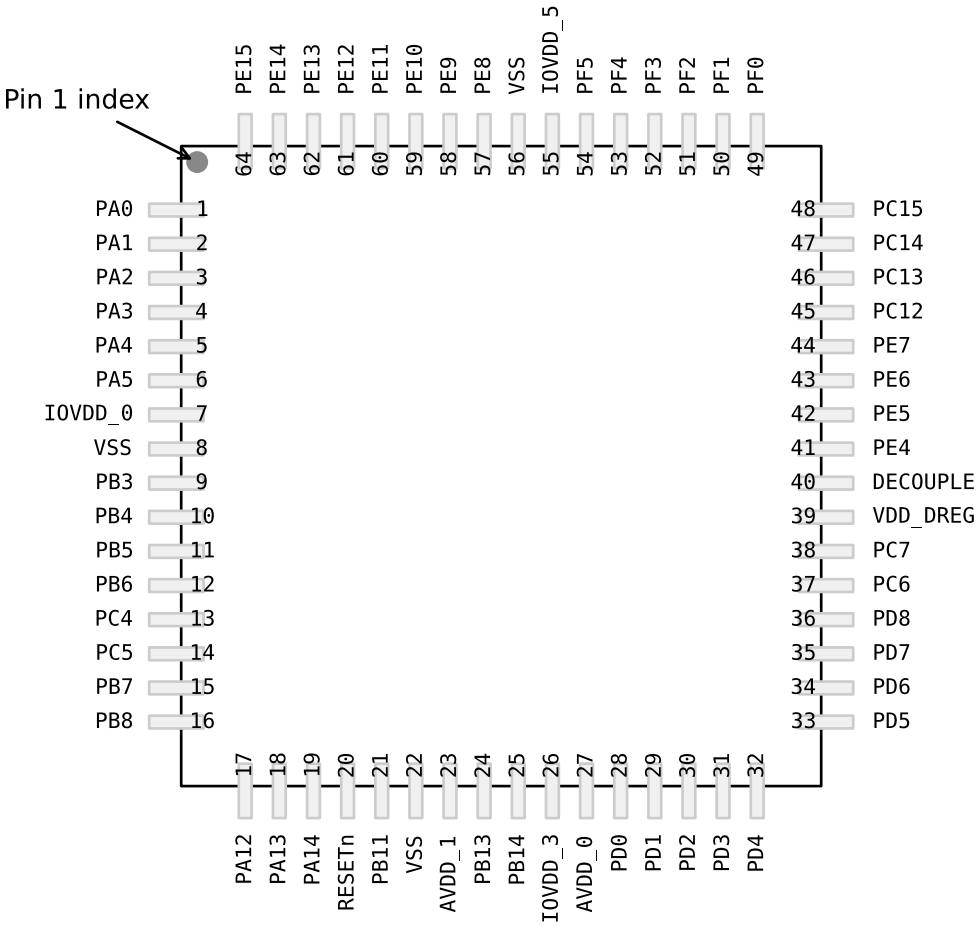



**Figure 5.25. EFM32WG842 Pinout (top view, not to scale)**

**Table 5.37. Device Pinout**

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PA3 | LCD_SEG16 | TIM0_CDTI0 #0 | | LES_ALTEX2 #0 ETM_TD1 #3 |
| 5 | PA4 | LCD_SEG17 | TIM0_CDTI1 #0 | | LES_ALTEX3 #0 ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PB3 | LCD_SEG20/ LCD_COM4 | PCNT1_S0IN #1 | US2_TX #1 | |
| 10 | PB4 | LCD_SEG21/ LCD_COM5 | PCNT1_S1IN #1 | US2_RX #1 | |
| 11 | PB5 | LCD_SEG22/ LCD_COM6 | | US2_CLK #1 | |
| 12 | PB6 | LCD_SEG23/ LCD_COM7 | | US2_CS #1 | |
| 13 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | TIM2_CC0 #1 | | |
| 18 | PA13 | LCD_BCAP_N | TIM2_CC1 #1 | | |
| 19 | PA14 | LCD_BEXT | TIM2_CC2 #1 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 45 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | CMU_CLK0 #1 LES_CH12 #0 |
| 46 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 47 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 48 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 49 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 51 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | PF3 | LCD_SEG1 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| 53 | PF4 | LCD_SEG2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| 54 | PF5 | LCD_SEG3 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | LCD_SEG4 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 58 | PE9 | LCD_SEG5 | PCNT2_S1IN #1 | | |
| 59 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 60 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 61 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 62 | PE13 | LCD_SEG9 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 63 | PE14 | LCD_SEG10 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 64 | PE15 | LCD_SEG11 | TIM3_CC1 #0 | LEU0_RX #2 | |

### 5.13.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.38. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | | | | | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | PA12 | | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | PA13 | | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | PA14 | | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| US0_CLK | PE12 | PE5 | | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | PC14 | PB14 | PB14 | | USART0 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US0_RX | PE11 | PE6 | | PE12 | PB8 | | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | PE13 | PB7 | | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.13.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG842 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.39. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | — | PA14 | PA13 | PA12 | — | — | — | — | — | — | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | — | PB11 | — | — | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | — | — | — | — | PC7 | PC6 | PC5 | PC4 | — | — | — | — |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.13.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG842 is shown in the following figure.

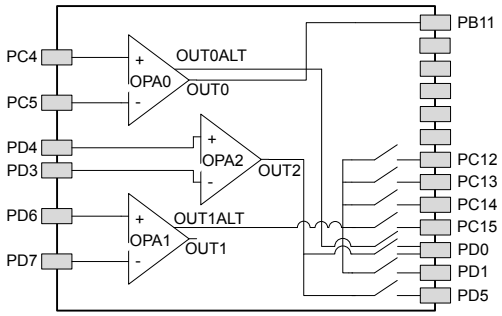



**Figure 5.26. Opamp Pinout**

### 5.14 EFM32WG880 (LQFP100)

#### 5.14.1 Pinout

The EFM32WG880 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

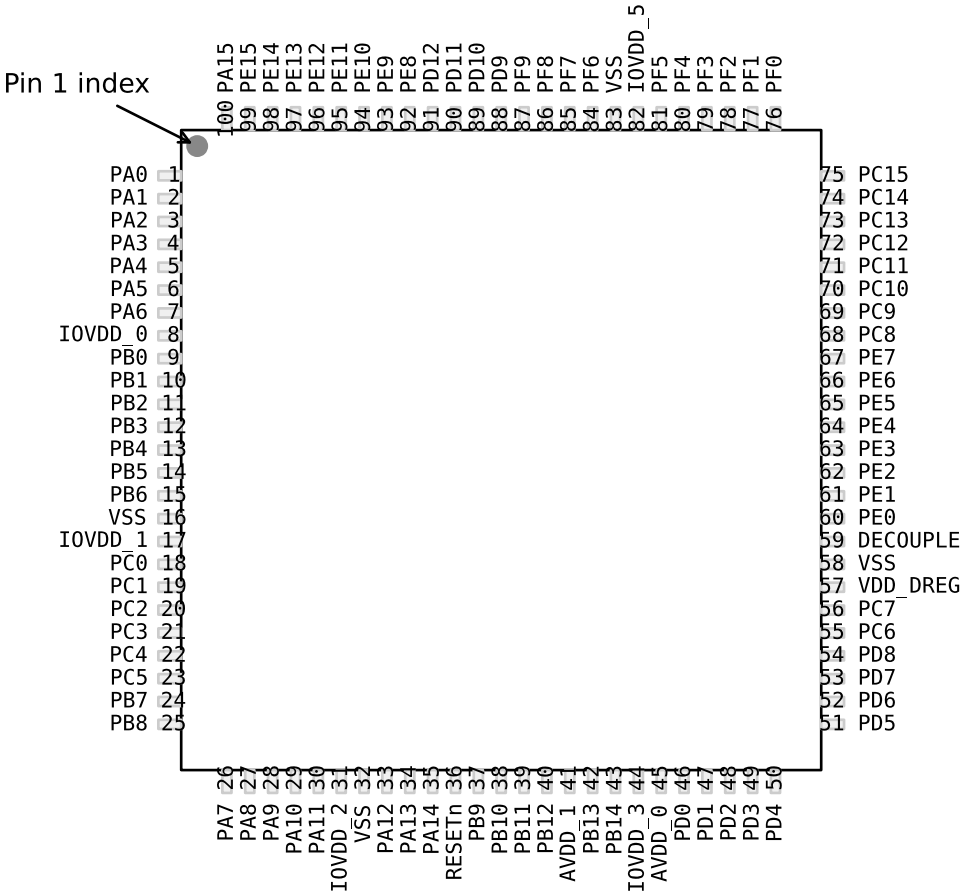



**Figure 5.27. EFM32WG880 Pinout (top view, not to scale)**

**Table 5.40. Device Pinout**

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | LCD_SEG16 | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | LCD_SEG17 | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | LCD_SEG19 | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | LCD_SEG32 | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| 10 | PB1 | LCD_SEG33 | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| 11 | PB2 | LCD_SEG34 | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| 12 | PB3 | LCD_SEG20/<br>LCD_COM4 | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | LCD_SEG21/<br>LCD_COM5 | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | LCD_SEG22/<br>LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| 15 | PB6 | LCD_SEG23/<br>LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 19 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 20 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 21 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 22 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 23 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 24 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 26 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| 27 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| 28 | PA9 | LCD_SEG37 | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| 29 | PA10 | LCD_SEG38 | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| 30 | PA11 | LCD_SEG39 | EBI_HSNC #0/1/2 | | | |
| 31 | IOVDD_2 | Digital IO power supply 2. | | | | |
| 32 | VSS | Ground. | | | | |
| 33 | PA12 | LCD_BCAP_P | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| 34 | PA13 | LCD_BCAP_N | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| 35 | PA14 | LCD_BEXT | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| 36 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| 37 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| 38 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| 39 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 40 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 41 | AVDD_1 | Analog power supply 1. | | | | |
| 42 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| 43 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| 44 | IOVDD_3 | Digital IO power supply 3. | | | | |
| 45 | AVDD_0 | Analog power supply 0. | | | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 46 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| 47 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 48 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| 49 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 50 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 51 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 52 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 53 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 54 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| 55 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 56 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 57 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| 58 | VSS | Ground. | | | | |
| 59 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| 60 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1 PCNT0_S0IN #1 | U0_TX #1 I2C1_SDA #2 | |
| 61 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1 PCNT0_S1IN #1 | U0_RX #1 I2C1_SCL #2 | |
| 62 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| 63 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| 64 | PE4 | LCD_COM0 | EBI_A11 #0/1/2 | | US0_CS #1 | |
| 65 | PE5 | LCD_COM1 | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| 66 | PE6 | LCD_COM2 | EBI_A13 #0/1/2 | | US0_RX #1 | |
| 67 | PE7 | LCD_COM3 | EBI_A14 #0/1/2 | | US0_TX #1 | |
| 68 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 69 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 70 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 71 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| 72 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| 73 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| 74 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| 75 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| 76 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 77 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 78 | PF2 | LCD_SEG0 | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 79 | PF3 | LCD_SEG1 | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| 80 | PF4 | LCD_SEG2 | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| 81 | PF5 | LCD_SEG3 | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | LCD_SEG24 | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | LCD_SEG25 | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | LCD_SEG26 | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| 87 | PF9 | LCD_SEG27 | EBI_REn #1 | | | ETM_TD0 #1 |
| 88 | PD9 | LCD_SEG28 | EBI_CS0 #0/1/2 | | | |
| 89 | PD10 | LCD_SEG29 | EBI_CS1 #0/1/2 | | | |
| 90 | PD11 | LCD_SEG30 | EBI_CS2 #0/1/2 | | | |
| 91 | PD12 | LCD_SEG31 | EBI_CS3 #0/1/2 | | | |
| 92 | PE8 | LCD_SEG4 | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 93 | PE9 | LCD_SEG5 | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| 94 | PE10 | LCD_SEG6 | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 95 | PE11 | LCD_SEG7 | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| 96 | PE12 | LCD_SEG8 | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |
| 97 | PE13 | LCD_SEG9 | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| 98 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 99 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 100 | PA15 | LCD_SEG12 | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |

### 5.14.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.41. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | PF6 | | | | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG30 | PD11 | | | | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.14.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG880 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.42. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.14.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG880 is shown in the following figure.

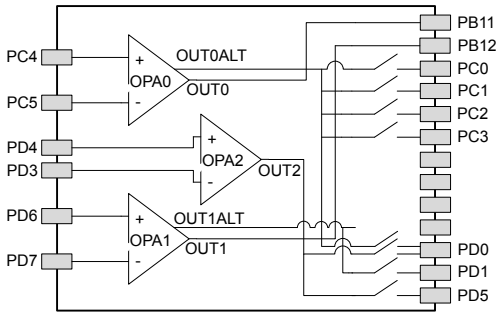



**Figure 5.28. Opamp Pinout**

## 5.15 EFM32WG890 (BGA112)

### 5.15.1 Pinout

The EFM32WG890 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

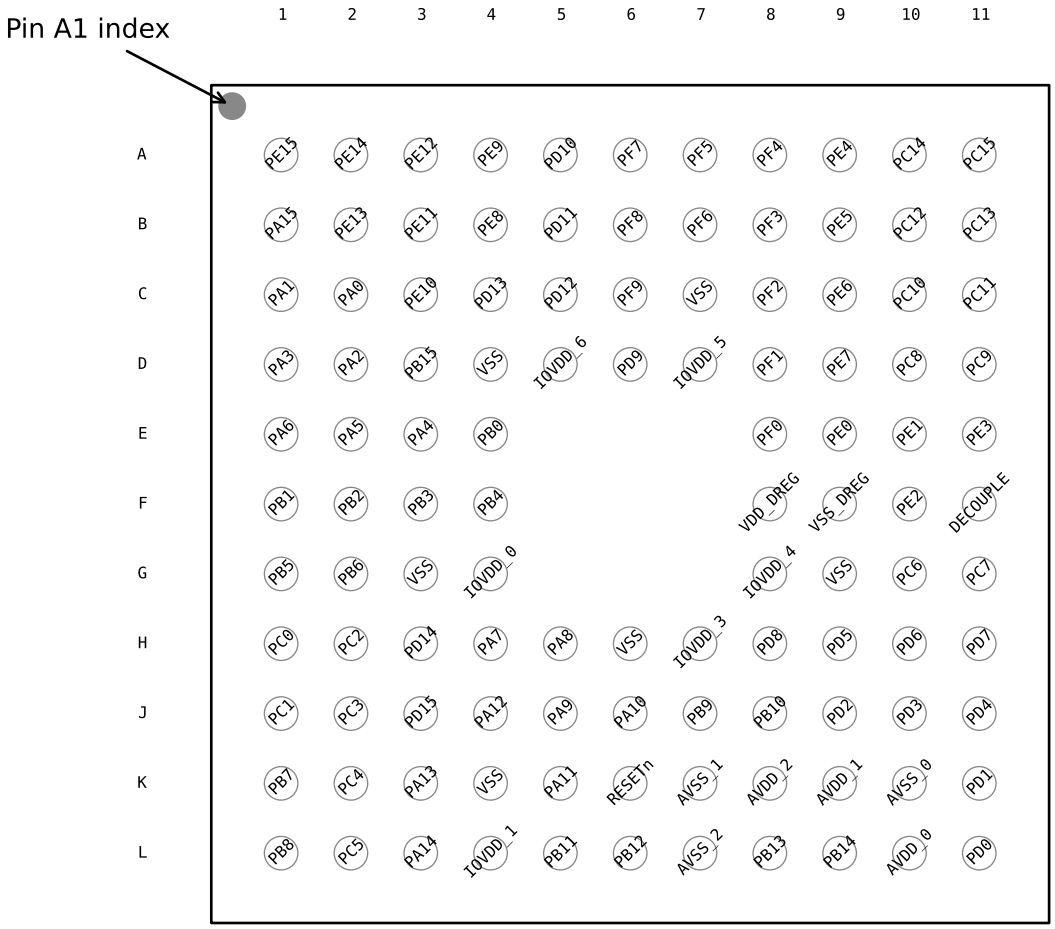



**Figure 5.29. EFM32WG890 Pinout (top view, not to scale)**

**Table 5.43. Device Pinout**

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| A3 | PE12 | LCD_SEG8 | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| A4 | PE9 | LCD_SEG5 | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD10 | LCD_SEG29 | EBI_CS1 #0/1/2 | | | |
| A6 | PF7 | LCD_SEG25 | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A7 | PF5 | LCD_SEG3 | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| A8 | PF4 | LCD_SEG2 | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| A9 | PE4 | LCD_COM0 | EBI_A11 #0/1/2 | | US0_CS #1 | |
| A10 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| A11 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| B1 | PA15 | LCD_SEG12 | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | LCD_SEG9 | EBI_AD05 #0/1/2 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| B3 | PE11 | LCD_SEG7 | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| B4 | PE8 | LCD_SEG4 | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD11 | LCD_SEG30 | EBI_CS2 #0/1/2 | | | |
| B6 | PF8 | LCD_SEG26 | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B7 | PF6 | LCD_SEG24 | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B8 | PF3 | LCD_SEG1 | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| B9 | PE5 | LCD_COM1 | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| B10 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| B11 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C1 | PA1 | LCD_SEG14 | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| C2 | PA0 | LCD_SEG13 | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| C3 | PE10 | LCD_SEG6 | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |
| C5 | PD12 | LCD_SEG31 | EBI_CS3 #0/1/2 | | | |
| C6 | PF9 | LCD_SEG27 | EBI_REn #1 | | | ETM_TD0 #1 |
| C7 | VSS | Ground. | | | | |
| C8 | PF2 | LCD_SEG0 | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| C9 | PE6 | LCD_COM2 | EBI_A13 #0/1/2 | | US0_RX #1 | |
| C10 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| C11 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| D1 | PA3 | LCD_SEG16 | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| D2 | PA2 | LCD_SEG15 | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D4 | VSS | Ground. | | | | |
| D5 | IOVDD_6 | Digital IO power supply 6. | | | | |
| D6 | PD9 | LCD_SEG28 | EBI_CS0 #0/1/2 | | | |
| D7 | IOVDD_5 | Digital IO power supply 5. | | | | |
| D8 | PF1 | | | TIM0_CC1 #5 LE-<br>TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO<br>#0/1/2/3<br>GPIO_EM4WU3 |
| D9 | PE7 | LCD_COM3 | EBI_A14 #0/1/2 | | US0_TX #1 | |
| D10 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| D11 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| E1 | PA6 | LCD_SEG19 | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| E2 | PA5 | LCD_SEG18 | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| E3 | PA4 | LCD_SEG17 | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| E4 | PB0 | LCD_SEG32 | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| E8 | PF0 | | | TIM0_CC0 #5 LE-<br>TIM0_OUT0 #2 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK<br>#0/1/2/3 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| E9 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| E10 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| E11 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| F1 | PB1 | LCD_SEG33 | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F2 | PB2 | LCD_SEG34 | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F3 | PB3 | LCD_SEG20/<br>LCD_COM4 | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| F4 | PB4 | LCD_SEG21/<br>LCD_COM5 | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| F8 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| F9 | VSS_DREG | Ground for on-chip voltage regulator. | | | | |
| F10 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| F11 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| G1 | PB5 | LCD_SEG22/<br>LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| G2 | PB6 | LCD_SEG23/<br>LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| G3 | VSS | Ground. | | | | |
| G4 | IOVDD_0 | Digital IO power supply 0. | | | | |
| G8 | IOVDD_4 | Digital IO power supply 4. | | | | |
| G9 | VSS | Ground. | | | | |
| G10 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| G11 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| H1 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| H2 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| H5 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| H9 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| H10 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| H11 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| J1 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| J2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| J3 | PD15 | | | | I2C0_SCL #3 | |
| J4 | PA12 | LCD_BCAP_P | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| J5 | PA9 | LCD_SEG37 | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| J6 | PA10 | LCD_SEG38 | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| J7 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| J8 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| J9 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| J10 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| J11 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| K1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| K2 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| K3 | PA13 | LCD_BCAP_N | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| K4 | VSS | Ground. | | | | |
| K5 | PA11 | LCD_SEG39 | EBI_HSNC #0/1/2 | | | |
| K6 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| K11 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| L2 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| L3 | PA14 | LCD_BEXT | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| L6 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| L9 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |
| L11 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |

### 5.15.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.44. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | PF6 | | | | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG30 | PD11 | | | | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.15.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG890 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.45. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.15.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG890 is shown in the following figure.

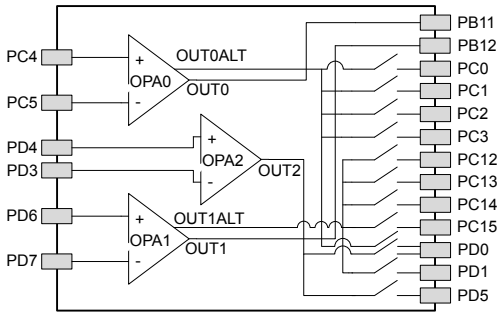



**Figure 5.30. Opamp Pinout**

### 5.16 EFM32WG895 (BGA120)

#### 5.16.1 Pinout

The EFM32WG895 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

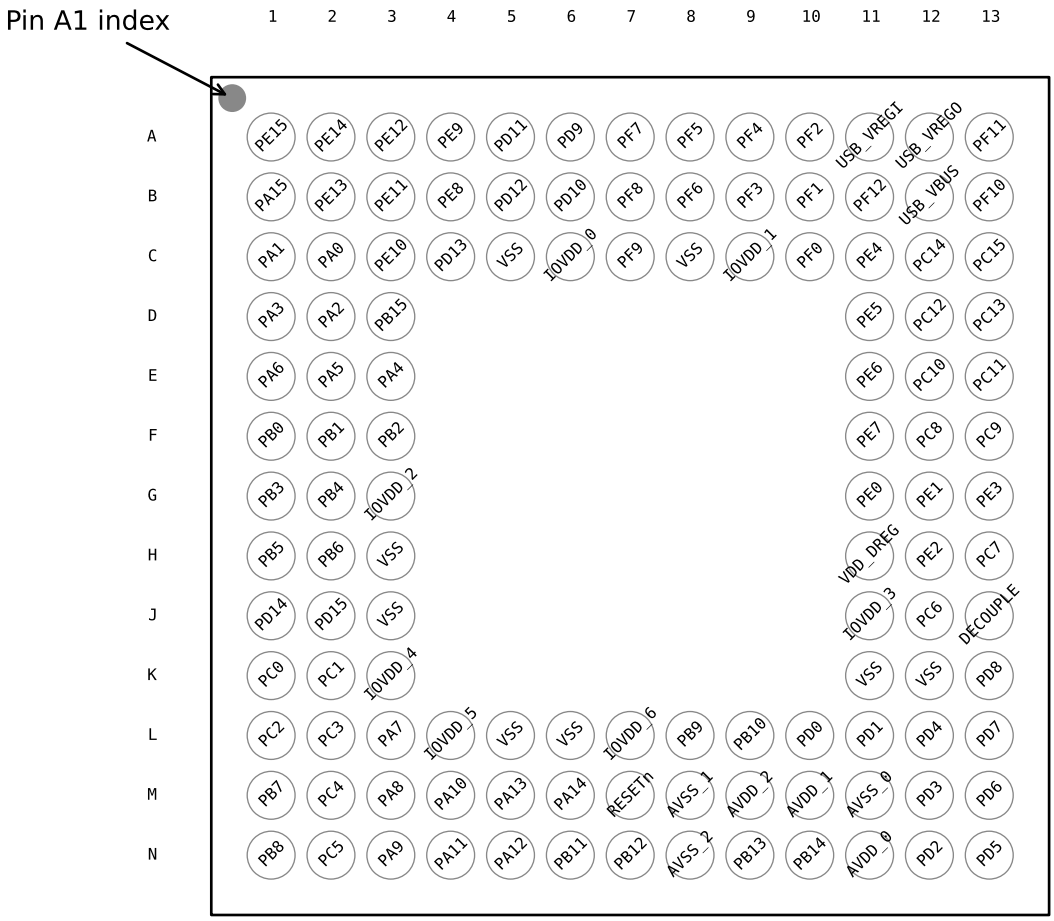



**Figure 5.31. EFM32WG895 Pinout (top view, not to scale)**

**Table 5.46. Device Pinout**

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| A3 | PE12 | LCD_SEG8 | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |
| A4 | PE9 | LCD_SEG5 | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD11 | LCD_SEG30 | EBI_CS2 #0/1/2 | | | |
| A6 | PD9 | LCD_SEG28 | EBI_CS0 #0/1/2 | | | |
| A7 | PF7 | LCD_SEG25 | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A8 | PF5 | LCD_SEG3 | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| A9 | PF4 | LCD_SEG2 | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| A10 | PF2 | LCD_SEG0 | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| A11 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | | |
| A12 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| A13 | PF11 | | | | U1_RX #1 | |
| B1 | PA15 | LCD_SEG12 | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | LCD_SEG9 | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| B3 | PE11 | LCD_SEG7 | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| B4 | PE8 | LCD_SEG4 | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD12 | LCD_SEG31 | EBI_CS3 #0/1/2 | | | |
| B6 | PD10 | LCD_SEG29 | EBI_CS1 #0/1/2 | | | |
| B7 | PF8 | LCD_SEG26 | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B8 | PF6 | LCD_SEG24 | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B9 | PF3 | LCD_SEG1 | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1<br>ETM_TD3 #1 |
| B10 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| B11 | PF12 | | | | | |
| B12 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| B13 | PF10 | | | | U1_TX #1 | |
| C1 | PA1 | LCD_SEG14 | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C2 | PA0 | LCD_SEG13 | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| C3 | PE10 | LCD_SEG6 | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |
| C5 | VSS | Ground. | | | | |
| C6 | IOVDD_0 | Digital IO power supply 0. | | | | |
| C7 | PF9 | LCD_SEG27 | EBI_REn #1 | | | ETM_TD0 #1 |
| C8 | VSS | Ground. | | | | |
| C9 | IOVDD_1 | Digital IO power supply 1. | | | | |
| C10 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| C11 | PE4 | LCD_COM0 | EBI_A11 #0/1/2 | | US0_CS #1 | |
| C12 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| C13 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| D1 | PA3 | LCD_SEG16 | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0 ETM_TD1 #3 |
| D2 | PA2 | LCD_SEG15 | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D11 | PE5 | LCD_COM1 | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| D12 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| D13 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| E1 | PA6 | LCD_SEG19 | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| E2 | PA5 | LCD_SEG18 | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| E3 | PA4 | LCD_SEG17 | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0 ETM_TD2 #3 |
| E11 | PE6 | LCD_COM2 | EBI_A13 #0/1/2 | | US0_RX #1 | |
| E12 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| E13 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| F1 | PB0 | LCD_SEG32 | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| F2 | PB1 | LCD_SEG33 | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F3 | PB2 | LCD_SEG34 | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F11 | PE7 | LCD_COM3 | EBI_A14 #0/1/2 | | US0_TX #1 | |
| F12 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| F13 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| G1 | PB3 | LCD_SEG20/<br>LCD_COM4 | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| G2 | PB4 | LCD_SEG21/<br>LCD_COM5 | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| G3 | IOVDD_2 | Digital IO power supply 2. | | | | |
| G11 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| G12 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| G13 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| H1 | PB5 | LCD_SEG22/<br>LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| H2 | PB6 | LCD_SEG23/<br>LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| H3 | VSS | Ground. | | | | |
| H11 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| H12 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| H13 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| J1 | PD14 | | | | I2C0_SDA #3 | |
| J2 | PD15 | | | | I2C0_SCL #3 | |
| J3 | VSS | Ground. | | | | |
| J11 | IOVDD_3 | Digital IO power supply 3. | | | | |
| J12 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| J13 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| K1 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| K2 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| K3 | IOVDD_4 | Digital IO power supply 4. | | | | |
| K11 | VSS | Ground. | | | | |
| K12 | VSS | Ground. | | | | |
| K13 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| L1 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| L2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| L3 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| L4 | IOVDD_5 | Digital IO power supply 5. | | | | |
| L5 | VSS | Ground. | | | | |
| L6 | VSS | Ground. | | | | |
| L7 | IOVDD_6 | Digital IO power supply 6. | | | | |
| L8 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| L9 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| L10 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| L11 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L12 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| L13 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| M1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| M2 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| M3 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| M4 | PA10 | LCD_SEG38 | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| M5 | PA13 | LCD_BCAP_N | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| M6 | PA14 | LCD_BEXT | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| M7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| M8 | AVSS_1 | Analog ground 1. | | | | |
| M9 | AVDD_2 | Analog power supply 2. | | | | |
| M10 | AVDD_1 | Analog power supply 1. | | | | |
| M11 | AVSS_0 | Analog ground 0. | | | | |
| M12 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| M13 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| N1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| N2 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| N3 | PA9 | LCD_SEG37 | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| N4 | PA11 | LCD_SEG39 | EBI_HSNC #0/1/2 | | | |
| N5 | PA12 | LCD_BCAP_P | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| N6 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| N7 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| N8 | AVSS_2 | Analog ground 2. | | | | |
| N9 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| N10 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| N11 | AVDD_0 | Analog power supply 0. | | | | |
| N12 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| N13 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |

### 5.16.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.47. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | PF6 | | | | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG25 | PF7 | | | | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG30 | PD11 | | | | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.16.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG895 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.48. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.16.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG895 is shown in the following figure.

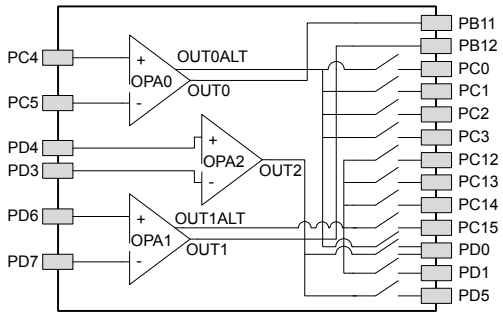



**Figure 5.32. Opamp Pinout**

## 5.17 EFM32WG900 (Wafer)

### 5.17.1 Padout

The EFM32WG900 padout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pad are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

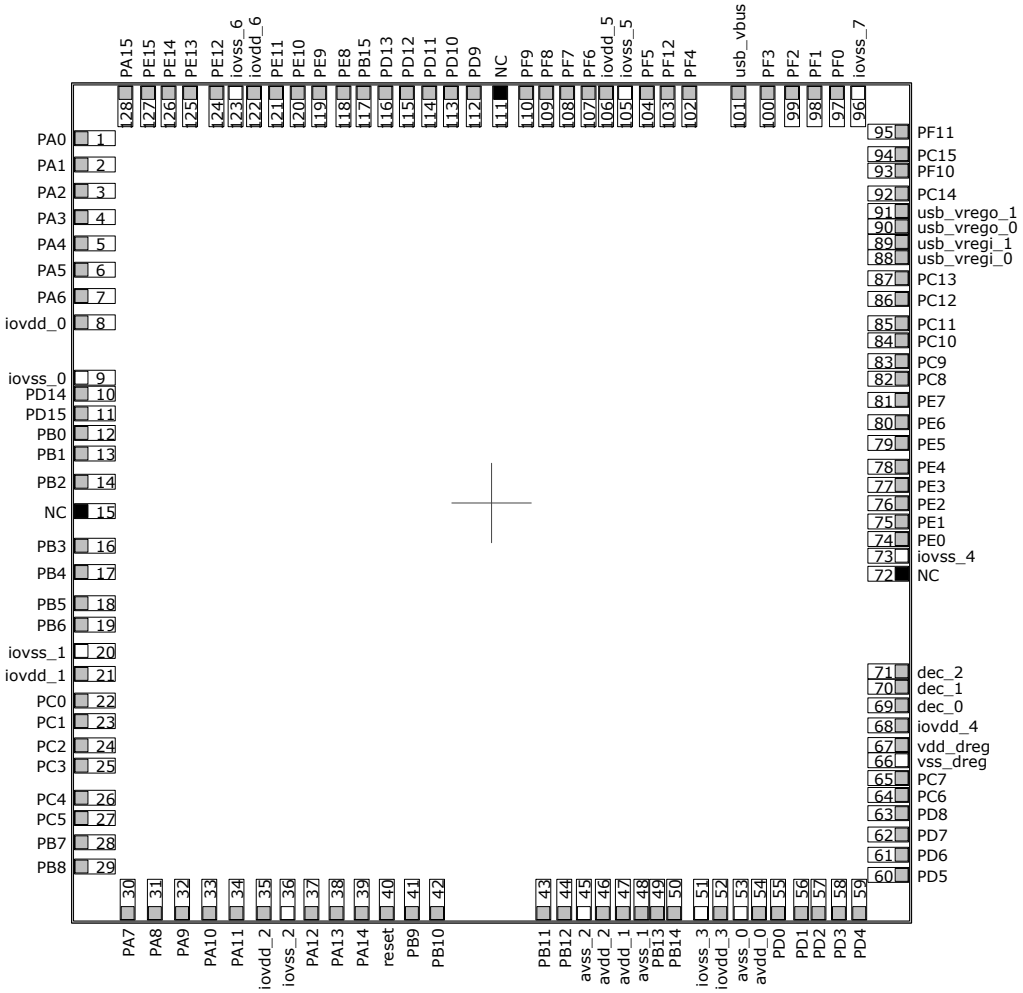



**Figure 5.33. EFM32WG900 Padout (top view, not to scale)**

**Table 5.49. Device Padout**

| Water Pads | | Pad Alternative Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pad # | Pad Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | LCD_SEG16 | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |

| Water Pads | | Pad Alternative Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pad # | Pad Name | Analog | EBI | Timers | Communication | Other |
| 5 | PA4 | LCD_SEG17 | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | LCD_SEG19 | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | IOVSS_0 | Digital IO ground 0. | | | | |
| 10 | PD14 | | | | I2C0_SDA #3 | |
| 11 | PD15 | | | | I2C0_SCL #3 | |
| 12 | PB0 | LCD_SEG32 | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| 13 | PB1 | LCD_SEG33 | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| 14 | PB2 | LCD_SEG34 | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| 15 | NC | Do not connect. | | | | |
| 16 | PB3 | LCD_SEG20/<br>LCD_COM4 | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| 17 | PB4 | LCD_SEG21/<br>LCD_COM5 | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| 18 | PB5 | LCD_SEG22/<br>LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| 19 | PB6 | LCD_SEG23/<br>LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| 20 | IOVSS_1 | Digital IO ground 1. | | | | |
| 21 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 22 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 23 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 24 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 25 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 26 | PC4 | ACMP0_CH4<br>DAC0_P0 /<br>OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4<br>LETIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |

| Water Pads | | Pad Alternative Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pad # | Pad Name | Analog | EBI | Timers | Communication | Other |
| 27 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 28 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 29 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 30 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| 31 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| 32 | PA9 | LCD_SEG37 | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| 33 | PA10 | LCD_SEG38 | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| 34 | PA11 | LCD_SEG39 | EBI_HSNC #0/1/2 | | | |
| 35 | IOVDD_2 | Digital IO power supply 2. | | | | |
| 36 | IOVSS_2 | Digital IO ground 2. | | | | |
| 37 | PA12 | LCD_BCAP_P | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| 38 | PA13 | LCD_BCAP_N | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| 39 | PA14 | LCD_BEXT | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| 40 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| 41 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| 42 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| 43 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 44 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 45 | AVSS_2 | Analog ground 2. | | | | |
| 46 | AVDD_2 | Analog power supply 2. | | | | |
| 47 | AVDD_1 | Analog power supply 1. | | | | |
| 48 | AVSS_1 | Analog ground 1. | | | | |
| 49 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| 50 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| 51 | IOVSS_3 | Digital IO ground 3. | | | | |
| 52 | IOVDD_3 | Digital IO power supply 3. | | | | |
| 53 | AVSS_0 | Analog ground 0. | | | | |
| 54 | AVDD_0 | Analog power supply 0. | | | | |

| Water Pads | | Pad Alternative Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pad # | Pad Name | Analog | EBI | Timers | Communication | Other |
| 55 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| 56 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 57 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| 58 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 59 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 60 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 61 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 62 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 63 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| 64 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 65 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 66 | VSS_DREG | Ground for on-chip voltage regulator. | | | | |
| 67 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| 68 | IOVDD_4 | Digital IO power supply 4. | | | | |
| 69 | DEC_0 | Decouple output for on-chip voltage regulator. | | | | |
| 70 | DEC_1 | Decouple output for on-chip voltage regulator. | | | | |
| 71 | DEC_2 | Decouple output for on-chip voltage regulator. | | | | |
| 72 | NC | Do not connect. | | | | |
| 73 | IOVSS_4 | Digital IO ground 4. | | | | |
| 74 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1 PCNT0_S0IN #1 | U0_TX #1 I2C1_SDA #2 | |
| 75 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1 PCNT0_S1IN #1 | U0_RX #1 I2C1_SCL #2 | |
| 76 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| 77 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| 78 | PE4 | LCD_COM0 | EBI_A11 #0/1/2 | | US0_CS #1 | |

| Water Pads | | Pad Alternative Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pad # | Pad Name | Analog | EBI | Timers | Communication | Other |
| 79 | PE5 | LCD_COM1 | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| 80 | PE6 | LCD_COM2 | EBI_A13 #0/1/2 | | US0_RX #1 | |
| 81 | PE7 | LCD_COM3 | EBI_A14 #0/1/2 | | US0_TX #1 | |
| 82 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 83 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| 84 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 85 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| 86 | PC12 | ACMP1_CH4<br>DAC0_OUT1ALT #0/<br>OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1<br>LES_CH12 #0 |
| 87 | PC13 | ACMP1_CH5<br>DAC0_OUT1ALT #1/<br>OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3<br>TIM1_CC0 #0<br>TIM1_CC2 #4<br>PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| 88 | USB_VREGI_0 | USB input to internal 3.3 V regulator. | | | | |
| 89 | USB_VREGI_1 | USB input to internal 3.3 V regulator. | | | | |
| 90 | USB_VREGO_0 | USB decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| 91 | USB_VREGO_1 | USB decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| 92 | PC14 | ACMP1_CH6<br>DAC0_OUT1ALT #2/<br>OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| 93 | PF10 | | | | U1_TX #1<br>USB_DM | |
| 94 | PC15 | ACMP1_CH7<br>DAC0_OUT1ALT #3/<br>OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3<br>TIM1_CC2 #0 | US0_CLK #3<br>U0_RX #3 | LES_CH15 #0<br>DBG_SWO #1 |
| 95 | PF11 | | | | U1_RX #1<br>USB_DP | |
| 96 | IOVSS_7 | Digital IO ground 7. | | | | |
| 97 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 98 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| 99 | PF2 | LCD_SEG0 | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| 100 | PF3 | LCD_SEG1 | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1<br>ETM_TD3 #1 |
| 101 | USB_VBUS | USB 5.0 V VBUS input. | | | | |

| Water Pads | | Pad Alternative Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pad # | Pad Name | Analog | EBI | Timers | Communication | Other |
| 102 | PF4 | LCD_SEG2 | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| 103 | PF12 | | | | USB_ID | |
| 104 | PF5 | LCD_SEG3 | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 105 | IOVSS_5 | Digital IO ground 5. | | | | |
| 106 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 107 | PF6 | LCD_SEG24 | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| 108 | PF7 | LCD_SEG25 | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| 109 | PF8 | LCD_SEG26 | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| 110 | PF9 | LCD_SEG27 | EBI_REn #1 | | | ETM_TD0 #1 |
| 111 | NC | Do not connect. | | | | |
| 112 | PD9 | LCD_SEG28 | EBI_CS0 #0/1/2 | | | |
| 113 | PD10 | LCD_SEG29 | EBI_CS1 #0/1/2 | | | |
| 114 | PD11 | LCD_SEG30 | EBI_CS2 #0/1/2 | | | |
| 115 | PD12 | LCD_SEG31 | EBI_CS3 #0/1/2 | | | |
| 116 | PD13 | | | | | ETM_TD1 #1 |
| 117 | PD15 | | | | | ETM_TD2 #1 |
| 118 | PE8 | LCD_SEG4 | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 119 | PE9 | LCD_SEG5 | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| 120 | PE10 | LCD_SEG6 | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 121 | PE11 | LCD_SEG7 | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| 122 | IOVDD_6 | Digital IO power supply 6. | | | | |
| 123 | IOVSS_6 | Digital IO ground 6. | | | | |
| 124 | PE12 | LCD_SEG8 | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |
| 125 | PE13 | LCD_SEG9 | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| 126 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 127 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 128 | PA15 | LCD_SEG12 | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |

### 5.17.2 Alternate Functionality Padout

A wide selection of alternate functionality is available for multiplexing to various pads. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the padout is shown in the column corresponding to LOCATION 0.

**Table 5.50. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0 / OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1 / OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| DAC0_P0 / OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1 / OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | PF6 | | | | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG30 | PD11 | | | | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.17.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG900 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.51. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.17.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG900 is shown in the following figure.

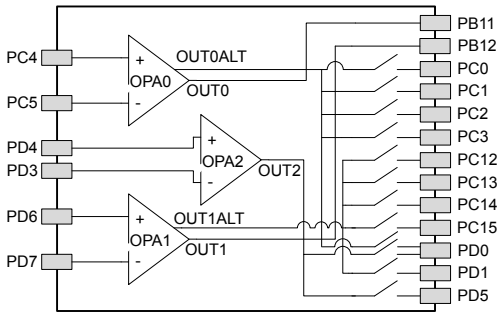



**Figure 5.34. Opamp Pinout**

### 5.18 EFM32WG940 (QFN64)

#### 5.18.1 Pinout

The EFM32WG940 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

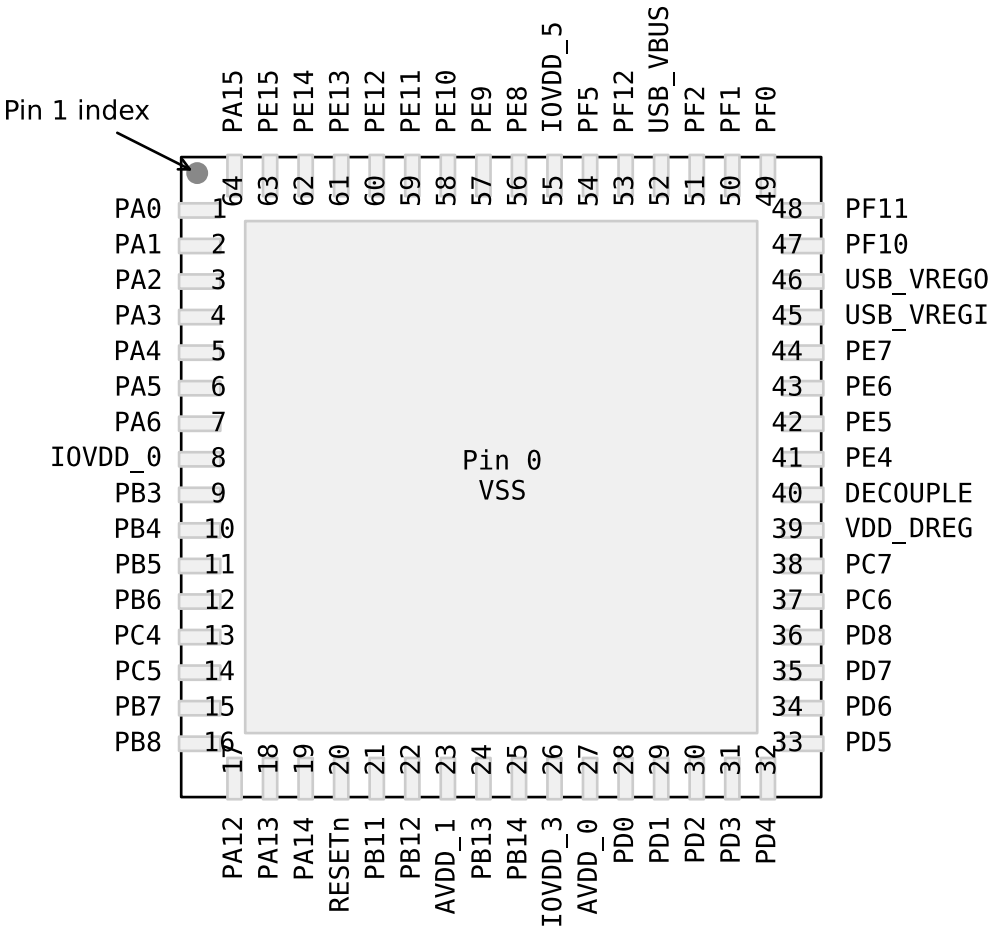



**Figure 5.35. EFM32WG940 Pinout (top view, not to scale)**

**Table 5.52. Device Pinout**

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| 4 | PA3 | LCD_SEG16 | TIM0_CDTI0 #0 | | LES_ALTEX2 #0 ETM_TD1 #3 |
| 5 | PA4 | LCD_SEG17 | TIM0_CDTI1 #0 | | LES_ALTEX3 #0 ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| 7 | PA6 | LCD_SEG19 | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PB3 | LCD_SEG20/ LCD_COM4 | PCNT1_S0IN #1 | US2_TX #1 | |
| 10 | PB4 | LCD_SEG21/ LCD_COM5 | PCNT1_S1IN #1 | US2_RX #1 | |
| 11 | PB5 | LCD_SEG22/ LCD_COM6 | | US2_CLK #1 | |
| 12 | PB6 | LCD_SEG23/ LCD_COM7 | | US2_CS #1 | |
| 13 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | TIM2_CC0 #1 | | |
| 18 | PA13 | LCD_BCAP_N | TIM2_CC1 #1 | | |
| 19 | PA14 | LCD_BEXT | TIM2_CC2 #1 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 22 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | LETIM0_OUT1 #1 | I2C1_SCL #1 | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 45 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | |
| 46 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | |
| 47 | PF10 | | | USB_DM | |
| 48 | PF11 | | | USB_DP | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 49 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 51 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | USB_VBUS | USB 5.0 V VBUS input. | | | |
| 53 | PF12 | | | USB_ID | |
| 54 | PF5 | LCD_SEG3 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | LCD_SEG4 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 57 | PE9 | LCD_SEG5 | PCNT2_S1IN #1 | | |
| 58 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 60 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 61 | PE13 | LCD_SEG9 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 62 | PE14 | LCD_SEG10 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 63 | PE15 | LCD_SEG11 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 64 | PA15 | LCD_SEG12 | TIM3_CC2 #0 | | |

### 5.18.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.53. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | | | | | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | | | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | PA12 | | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | PA13 | | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | PA14 | | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | | | | | | | Timer 3 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | PE12 | PB8 | | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US0_TX | PE10 | PE7 | | PE13 | PB7 | | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.18.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG940 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.54. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | — | — | — | — | — | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | — | — | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | — | — | — |
| Port C | — | — | — | — | — | — | — | — | PC7 | PC6 | PC5 | PC4 | — | — | — | — |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | — | — | — | — |
| Port F | — | — | — | PF12 | PF11 | PF10 | — | — | — | — | PF5 | — | — | PF2 | PF1 | PF0 |

### 5.18.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG940 is shown in the following figure.

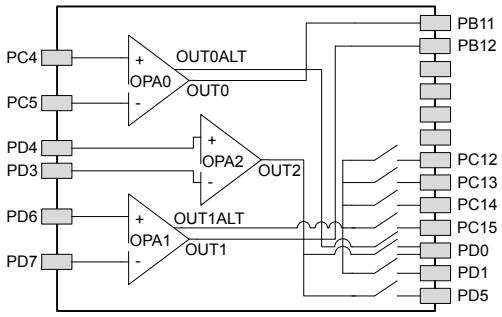



**Figure 5.36. Opamp Pinout**

### 5.19 EFM32WG942 (TQFP64)

#### 5.19.1 Pinout

The EFM32WG942 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

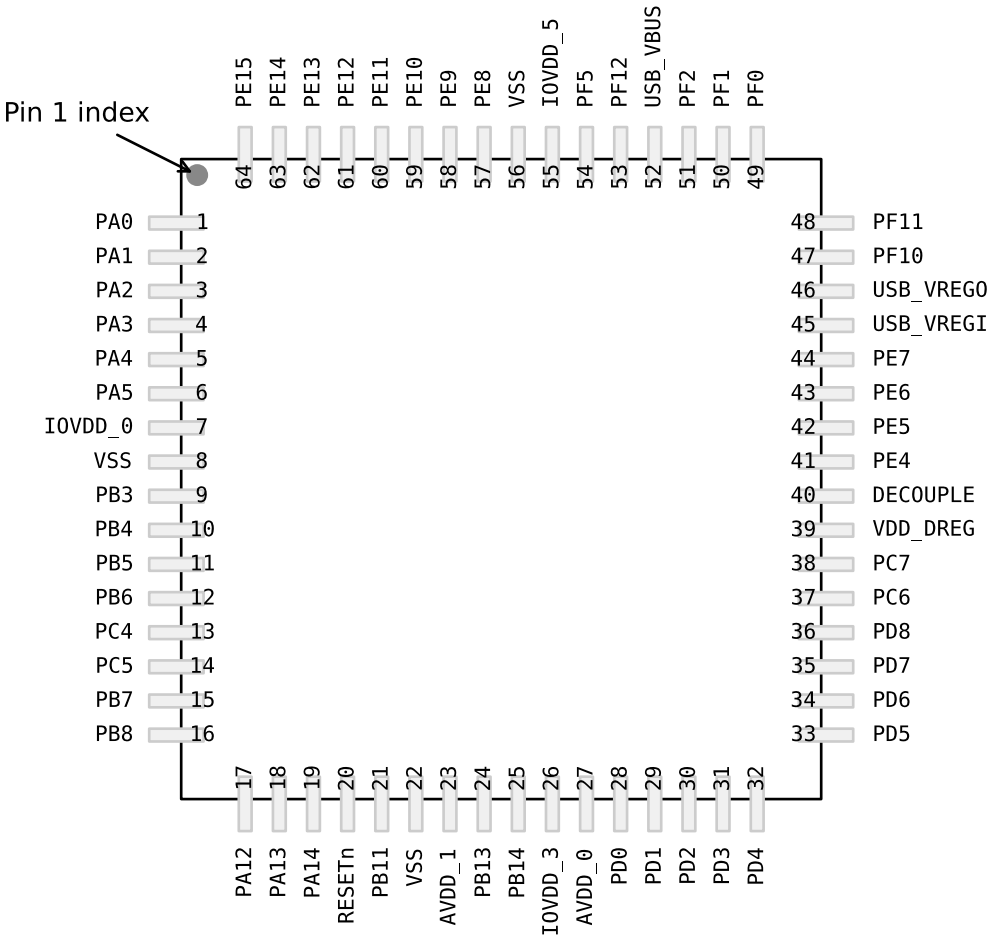



**Figure 5.37. EFM32WG942 Pinout (top view, not to scale)**

**Table 5.55. Device Pinout**

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PA3 | LCD_SEG16 | TIM0_CDTI0 #0 | | LES_ALTEX2 #0 ETM_TD1 #3 |
| 5 | PA4 | LCD_SEG17 | TIM0_CDTI1 #0 | | LES_ALTEX3 #0 ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PB3 | LCD_SEG20/ LCD_COM4 | PCNT1_S0IN #1 | US2_TX #1 | |
| 10 | PB4 | LCD_SEG21/ LCD_COM5 | PCNT1_S1IN #1 | US2_RX #1 | |
| 11 | PB5 | LCD_SEG22/ LCD_COM6 | | US2_CLK #1 | |
| 12 | PB6 | LCD_SEG23/ LCD_COM7 | | US2_CS #1 | |
| 13 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | TIM2_CC0 #1 | | |
| 18 | PA13 | LCD_BCAP_N | TIM2_CC1 #1 | | |
| 19 | PA14 | LCD_BEXT | TIM2_CC2 #1 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 45 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | |
| 46 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | |
| 47 | PF10 | | | USB_DM | |
| 48 | PF11 | | | USB_DP | |
| 49 | PF0 | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| 51 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | USB_VBUS | USB 5.0 V VBUS input. | | | |
| 53 | PF12 | | | USB_ID | |
| 54 | PF5 | LCD_SEG3 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | LCD_SEG4 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 58 | PE9 | LCD_SEG5 | PCNT2_S1IN #1 | | |
| 59 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 60 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 61 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 62 | PE13 | LCD_SEG9 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 63 | PE14 | LCD_SEG10 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 64 | PE15 | LCD_SEG11 | TIM3_CC1 #0 | LEU0_RX #2 | |

### 5.19.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.56. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | | | | | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | | | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | PA12 | | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | PA13 | | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | PA14 | | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| US0_CLK | PE12 | PE5 | | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | PE12 | PB8 | | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | PE13 | PB7 | | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_TX | | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.19.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG942 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.57. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | — | PA14 | PA13 | PA12 | — | — | — | — | — | — | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | — | PB11 | — | — | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | — | — | — |
| Port C | — | — | — | — | — | — | — | — | PC7 | PC6 | PC5 | PC4 | — | — | — | — |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | — | — | — | — |
| Port F | — | — | — | PF12 | PF11 | PF10 | — | — | — | — | PF5 | — | — | PF2 | PF1 | PF0 |

### 5.19.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG942 is shown in the following figure.

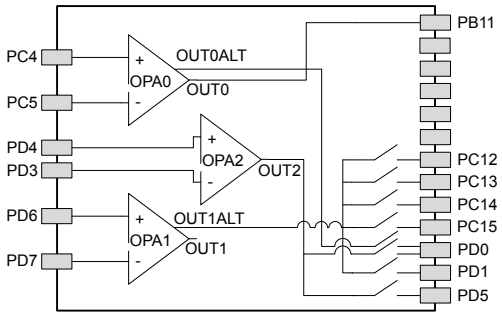



**Figure 5.38. Opamp Pinout**

### 5.20 EFM32WG980 (LQFP100)

#### 5.20.1 Pinout

The EFM32WG980 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

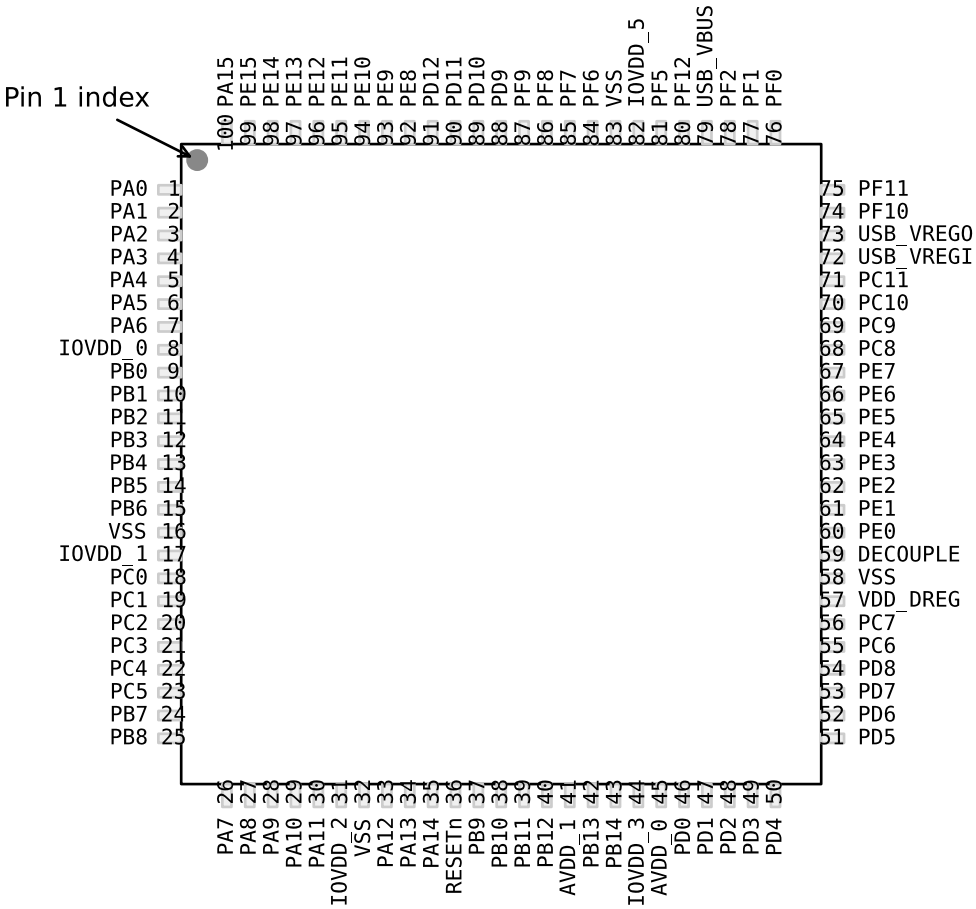



**Figure 5.39. EFM32WG980 Pinout (top view, not to scale)**

**Table 5.58. Device Pinout**

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | LCD_SEG16 | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | LCD_SEG17 | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | LCD_SEG19 | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | LCD_SEG32 | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| 10 | PB1 | LCD_SEG33 | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| 11 | PB2 | LCD_SEG34 | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| 12 | PB3 | LCD_SEG20/<br>LCD_COM4 | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | LCD_SEG21/<br>LCD_COM5 | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | LCD_SEG22/<br>LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| 15 | PB6 | LCD_SEG23/<br>LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 19 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 20 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 21 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 22 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 23 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 24 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 26 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| 27 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| 28 | PA9 | LCD_SEG37 | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| 29 | PA10 | LCD_SEG38 | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| 30 | PA11 | LCD_SEG39 | EBI_HSNC #0/1/2 | | | |
| 31 | IOVDD_2 | Digital IO power supply 2. | | | | |
| 32 | VSS | Ground. | | | | |
| 33 | PA12 | LCD_BCAP_P | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| 34 | PA13 | LCD_BCAP_N | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| 35 | PA14 | LCD_BEXT | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| 36 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| 37 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| 38 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| 39 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| 40 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 41 | AVDD_1 | Analog power supply 1. | | | | |
| 42 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| 43 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| 44 | IOVDD_3 | Digital IO power supply 3. | | | | |
| 45 | AVDD_0 | Analog power supply 0. | | | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 46 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| 47 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 48 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| 49 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 50 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 51 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 52 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| 53 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| 54 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| 55 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| 56 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| 57 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| 58 | VSS | Ground. | | | | |
| 59 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| 60 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1 PCNT0_S0IN #1 | U0_TX #1 I2C1_SDA #2 | |
| 61 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1 PCNT0_S1IN #1 | U0_RX #1 I2C1_SCL #2 | |
| 62 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| 63 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| 64 | PE4 | LCD_COM0 | EBI_A11 #0/1/2 | | US0_CS #1 | |
| 65 | PE5 | LCD_COM1 | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| 66 | PE6 | LCD_COM2 | EBI_A13 #0/1/2 | | US0_RX #1 | |
| 67 | PE7 | LCD_COM3 | EBI_A14 #0/1/2 | | US0_TX #1 | |
| 68 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 69 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| 70 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 71 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| 72 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | | |
| 73 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| 74 | PF10 | | | | U1_TX #1 USB_DM | |
| 75 | PF11 | | | | U1_RX #1 USB_DP | |
| 76 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 77 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| 78 | PF2 | LCD_SEG0 | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| 79 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| 80 | PF12 | | | | USB_ID | |
| 81 | PF5 | LCD_SEG3 | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | LCD_SEG24 | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | LCD_SEG25 | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | LCD_SEG26 | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| 87 | PF9 | LCD_SEG27 | EBI_REn #1 | | | ETM_TD0 #1 |
| 88 | PD9 | LCD_SEG28 | EBI_CS0 #0/1/2 | | | |
| 89 | PD10 | LCD_SEG29 | EBI_CS1 #0/1/2 | | | |
| 90 | PD11 | LCD_SEG30 | EBI_CS2 #0/1/2 | | | |
| 91 | PD12 | LCD_SEG31 | EBI_CS3 #0/1/2 | | | |
| 92 | PE8 | LCD_SEG4 | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 93 | PE9 | LCD_SEG5 | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| 94 | PE10 | LCD_SEG6 | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 95 | PE11 | LCD_SEG7 | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| 96 | PE12 | LCD_SEG8 | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 97 | PE13 | LCD_SEG9 | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| 98 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 99 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 100 | PA15 | LCD_SEG12 | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |

### 5.20.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.59. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | | PF8 | | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | PF6 | | | | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG28 | PD9 | | | | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG30 | PD11 | | | | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | PB2 | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.20.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG980 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.60. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | — | — | — | — | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | — | — | PF2 | PF1 | PF0 |

### 5.20.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG980 is shown in the following figure.

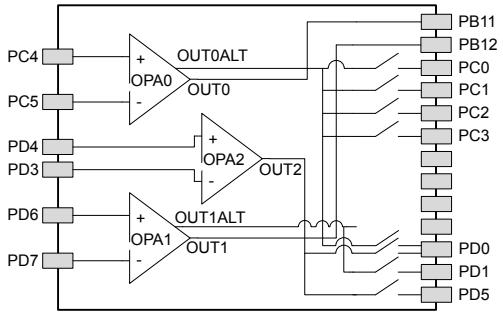



**Figure 5.40. Opamp Pinout**

## 5.21 EFM32WG990 (BGA112)

### 5.21.1 Pinout

The EFM32WG990 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

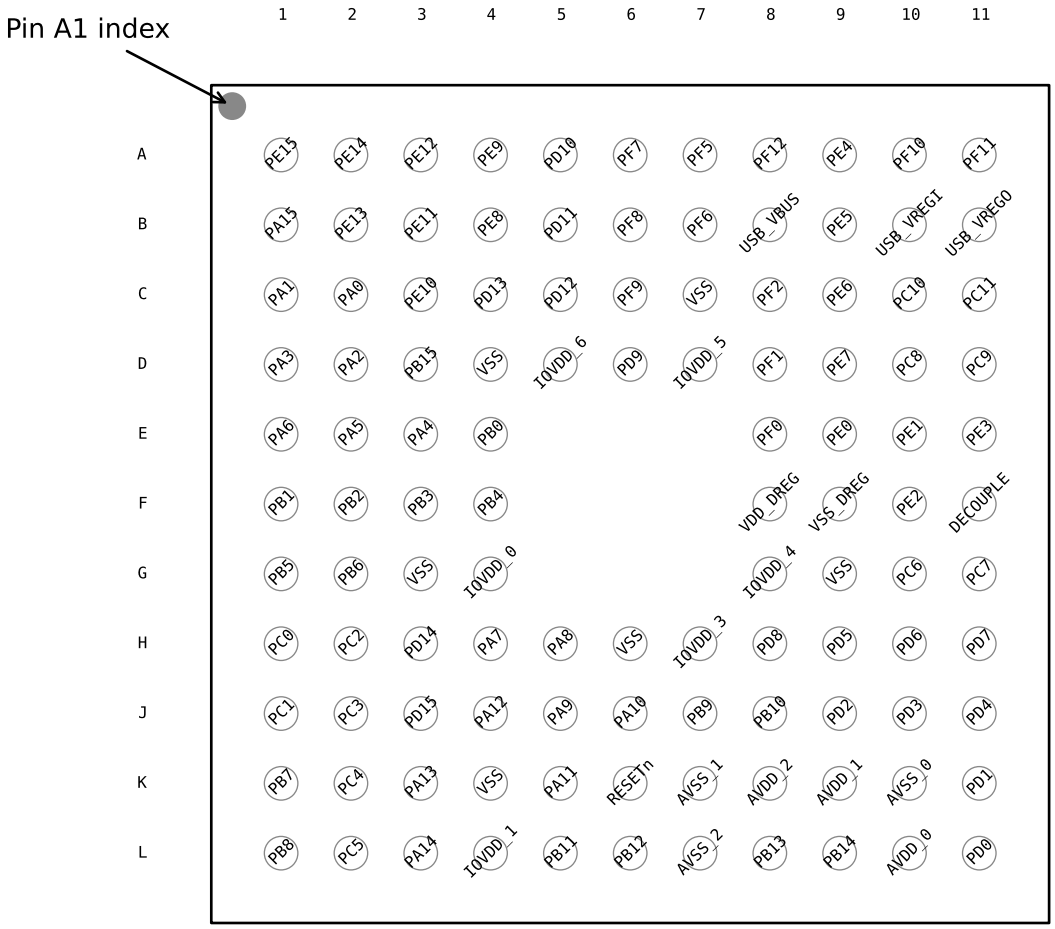



**Figure 5.41. EFM32WG990 Pinout (top view, not to scale)**

**Table 5.61. Device Pinout**

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| A3 | PE12 | LCD_SEG8 | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A4 | PE9 | LCD_SEG5 | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD10 | LCD_SEG29 | EBI_CS1 #0/1/2 | | | |
| A6 | PF7 | LCD_SEG25 | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A7 | PF5 | LCD_SEG3 | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| A8 | PF12 | | | | USB_ID | |
| A9 | PE4 | LCD_COM0 | EBI_A11 #0/1/2 | | US0_CS #1 | |
| A10 | PF10 | | | | U1_TX #1 USB_DM | |
| A11 | PF11 | | | | U1_RX #1 USB_DP | |
| B1 | PA15 | LCD_SEG12 | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | LCD_SEG9 | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| B3 | PE11 | LCD_SEG7 | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| B4 | PE8 | LCD_SEG4 | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD11 | LCD_SEG30 | EBI_CS2 #0/1/2 | | | |
| B6 | PF8 | LCD_SEG26 | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B7 | PF6 | LCD_SEG24 | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B8 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| B9 | PE5 | LCD_COM1 | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| B10 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | | |
| B11 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| C1 | PA1 | LCD_SEG14 | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| C2 | PA0 | LCD_SEG13 | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| C3 | PE10 | LCD_SEG6 | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |
| C5 | PD12 | LCD_SEG31 | EBI_CS3 #0/1/2 | | | |
| C6 | PF9 | LCD_SEG27 | EBI_REn #1 | | | ETM_TD0 #1 |
| C7 | VSS | Ground. | | | | |
| C8 | PF2 | LCD_SEG0 | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| C9 | PE6 | LCD_COM2 | EBI_A13 #0/1/2 | | US0_RX #1 | |
| C10 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| C11 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| D1 | PA3 | LCD_SEG16 | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| D2 | PA2 | LCD_SEG15 | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D4 | VSS | Ground. | | | | |
| D5 | IOVDD_6 | Digital IO power supply 6. | | | | |
| D6 | PD9 | LCD_SEG28 | EBI_CS0 #0/1/2 | | | |
| D7 | IOVDD_5 | Digital IO power supply 5. | | | | |
| D8 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| D9 | PE7 | LCD_COM3 | EBI_A14 #0/1/2 | | US0_TX #1 | |
| D10 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| D11 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| E1 | PA6 | LCD_SEG19 | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| E2 | PA5 | LCD_SEG18 | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| E3 | PA4 | LCD_SEG17 | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| E4 | PB0 | LCD_SEG32 | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| E8 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| E9 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| E10 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| E11 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| F1 | PB1 | LCD_SEG33 | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F2 | PB2 | LCD_SEG34 | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F3 | PB3 | LCD_SEG20/<br>LCD_COM4 | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| F4 | PB4 | LCD_SEG21/<br>LCD_COM5 | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| F8 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| F9 | VSS_DREG | Ground for on-chip voltage regulator. | | | | |
| F10 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| F11 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| G1 | PB5 | LCD_SEG22/<br>LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| G2 | PB6 | LCD_SEG23/ LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| G3 | VSS | Ground. | | | | |
| G4 | IOVDD_0 | Digital IO power supply 0. | | | | |
| G8 | IOVDD_4 | Digital IO power supply 4. | | | | |
| G9 | VSS | Ground. | | | | |
| G10 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| G11 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| H1 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| H2 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| H5 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| H9 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| H10 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| H11 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| J1 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| J2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| J3 | PD15 | | | | I2C0_SCL #3 | |
| J4 | PA12 | LCD_BCAP_P | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| J5 | PA9 | LCD_SEG37 | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| J6 | PA10 | LCD_SEG38 | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| J7 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| J8 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| J9 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0<br>US1_CLK #1 | DBG_SWO #3 |
| J10 | PD3 | ADC0_CH3<br>OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| J11 | PD4 | ADC0_CH4<br>OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| K1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| K2 | PC4 | ACMP0_CH4<br>DAC0_P0 /<br>OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-<br>TIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |
| K3 | PA13 | LCD_BCAP_N | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| K4 | VSS | Ground. | | | | |
| K5 | PA11 | LCD_SEG39 | EBI_HSNC #0/1/2 | | | |
| K6 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |
| K11 | PD1 | ADC0_CH1<br>DAC0_OUT1ALT<br>#4/<br>OPAMP_OUT1ALT | | TIM0_CC0 #3<br>PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| L2 | PC5 | ACMP0_CH5<br>DAC0_N0 /<br>OPAMP_N0 | EBI_NANDWEn<br>#0/1/2 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| L3 | PA14 | LCD_BEXT | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OUT0 /<br>OPAMP_OUT0 | | TIM1_CC2 #3 LE-<br>TIM0_OUT0 #1 | I2C1_SDA #1 | |
| L6 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_P | | | US0_CLK #4/5<br>LEU0_TX #1 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| L9 | PB14 | HFXTAL_N | | | US0_CS #4/5<br>LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |
| L11 | PD0 | ADC0_CH0<br>DAC0_OUT0ALT #4/<br>OPAMP_OUT0ALT<br>OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |

### 5.21.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.62. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | | PF8 | | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | PF6 | | | | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG28 | PD9 | | | | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG30 | PD11 | | | | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | PB2 | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.21.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG990 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.63. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | — | — | — | — | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | — | — | PF2 | PF1 | PF0 |

### 5.21.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG990 is shown in the following figure.

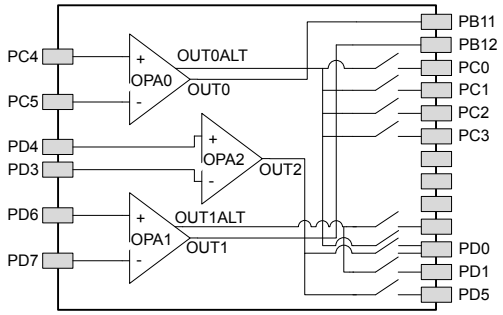



**Figure 5.42. Opamp Pinout**

## 5.22 EFM32WG995 (BGA120)

### 5.22.1 Pinout

The EFM32WG995 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

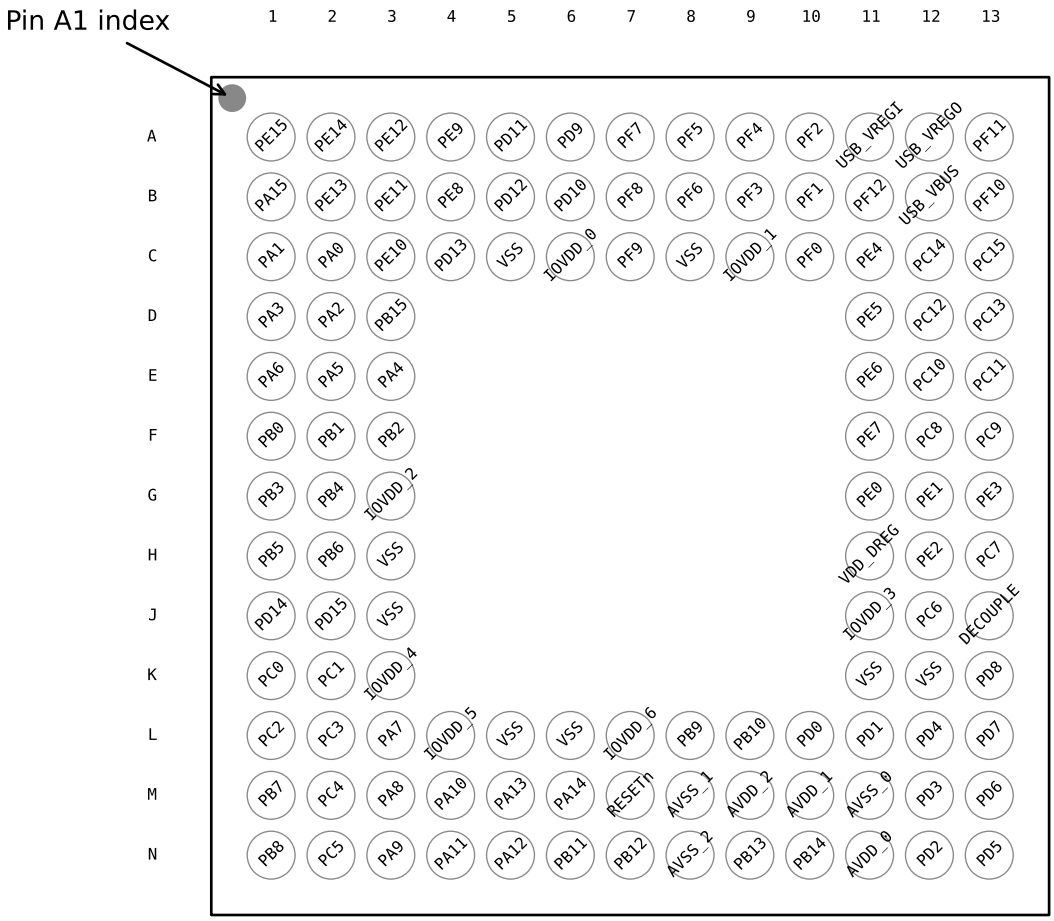



**Figure 5.43. EFM32WG995 Pinout (top view, not to scale)**

**Table 5.64. Device Pinout**

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| A3 | PE12 | LCD_SEG8 | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A4 | PE9 | LCD_SEG5 | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD11 | LCD_SEG30 | EBI_CS2 #0/1/2 | | | |
| A6 | PD9 | LCD_SEG28 | EBI_CS0 #0/1/2 | | | |
| A7 | PF7 | LCD_SEG25 | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A8 | PF5 | LCD_SEG3 | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| A9 | PF4 | LCD_SEG2 | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| A10 | PF2 | LCD_SEG0 | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| A11 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | | |
| A12 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | | |
| A13 | PF11 | | | | U1_RX #1 USB_DP | |
| B1 | PA15 | LCD_SEG12 | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | LCD_SEG9 | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| B3 | PE11 | LCD_SEG7 | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| B4 | PE8 | LCD_SEG4 | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD12 | LCD_SEG31 | EBI_CS3 #0/1/2 | | | |
| B6 | PD10 | LCD_SEG29 | EBI_CS1 #0/1/2 | | | |
| B7 | PF8 | LCD_SEG26 | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B8 | PF6 | LCD_SEG24 | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B9 | PF3 | LCD_SEG1 | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1<br>ETM_TD3 #1 |
| B10 | PF1 | | | TIM0_CC1 #5 LE-<br>TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO<br>#0/1/2/3<br>GPIO_EM4WU3 |
| B11 | PF12 | | | | USB_ID | |
| B12 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| B13 | PF10 | | | | U1_TX #1 USB_DM | |
| C1 | PA1 | LCD_SEG14 | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| C2 | PA0 | LCD_SEG13 | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| C3 | PE10 | LCD_SEG6 | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |
| C5 | VSS | Ground. | | | | |
| C6 | IOVDD_0 | Digital IO power supply 0. | | | | |
| C7 | PF9 | LCD_SEG27 | EBI_REn #1 | | | ETM_TD0 #1 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C8 | VSS | Ground. | | | | |
| C9 | IOVDD_1 | Digital IO power supply 1. | | | | |
| C10 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| C11 | PE4 | LCD_COM0 | EBI_A11 #0/1/2 | | US0_CS #1 | |
| C12 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| C13 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| D1 | PA3 | LCD_SEG16 | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0 ETM_TD1 #3 |
| D2 | PA2 | LCD_SEG15 | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D11 | PE5 | LCD_COM1 | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| D12 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| D13 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| E1 | PA6 | LCD_SEG19 | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| E2 | PA5 | LCD_SEG18 | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| E3 | PA4 | LCD_SEG17 | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0 ETM_TD2 #3 |
| E11 | PE6 | LCD_COM2 | EBI_A13 #0/1/2 | | US0_RX #1 | |
| E12 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| E13 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| F1 | PB0 | LCD_SEG32 | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| F2 | PB1 | LCD_SEG33 | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F3 | PB2 | LCD_SEG34 | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F11 | PE7 | LCD_COM3 | EBI_A14 #0/1/2 | | US0_TX #1 | |
| F12 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| F13 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| G1 | PB3 | LCD_SEG20/ LCD_COM4 | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| G2 | PB4 | LCD_SEG21/ LCD_COM5 | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| G3 | IOVDD_2 | Digital IO power supply 2. | | | | |
| G11 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1 PCNT0_S0IN #1 | U0_TX #1 I2C1_SDA #2 | |
| G12 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1 PCNT0_S1IN #1 | U0_RX #1 I2C1_SCL #2 | |
| G13 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| H1 | PB5 | LCD_SEG22/ LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| H2 | PB6 | LCD_SEG23/ LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| H3 | VSS | Ground. | | | | |
| H11 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| H12 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| H13 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| J1 | PD14 | | | | I2C0_SDA #3 | |
| J2 | PD15 | | | | I2C0_SCL #3 | |
| J3 | VSS | Ground. | | | | |
| J11 | IOVDD_3 | Digital IO power supply 3. | | | | |
| J12 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| J13 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| K1 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| K2 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| K3 | IOVDD_4 | Digital IO power supply 4. | | | | |
| K11 | VSS | Ground. | | | | |
| K12 | VSS | Ground. | | | | |
| K13 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| L1 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| L2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| L3 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| L4 | IOVDD_5 | Digital IO power supply 5. | | | | |
| L5 | VSS | Ground. | | | | |
| L6 | VSS | Ground. | | | | |
| L7 | IOVDD_6 | Digital IO power supply 6. | | | | |
| L8 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| L9 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| L10 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| L11 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L12 | PD4 | ADC0_CH4 OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| L13 | PD7 | ADC0_CH7 DAC0_N1 / OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| M1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| M2 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| M3 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| M4 | PA10 | LCD_SEG38 | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| M5 | PA13 | LCD_BCAP_N | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| M6 | PA14 | LCD_BEXT | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| M7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| M8 | AVSS_1 | Analog ground 1. | | | | |
| M9 | AVDD_2 | Analog power supply 2. | | | | |
| M10 | AVDD_1 | Analog power supply 1. | | | | |
| M11 | AVSS_0 | Analog ground 0. | | | | |
| M12 | PD3 | ADC0_CH3 OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| M13 | PD6 | ADC0_CH6 DAC0_P1 / OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| N1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| N2 | PC5 | ACMP0_CH5 DAC0_N0 / OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| N3 | PA9 | LCD_SEG37 | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| N4 | PA11 | LCD_SEG39 | EBI_HSNC #0/1/2 | | | |
| N5 | PA12 | LCD_BCAP_P | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| N6 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |
| N7 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| N8 | AVSS_2 | Analog ground 2. | | | | |
| N9 | PB13 | HFXTAL_P | | | US0_CLK #4/5 LEU0_TX #1 | |
| N10 | PB14 | HFXTAL_N | | | US0_CS #4/5 LEU0_RX #1 | |
| N11 | AVDD_0 | Analog power supply 0. | | | | |
| N12 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0 US1_CLK #1 | DBG_SWO #3 |
| N13 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |

### 5.22.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.65. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | PF6 | | | | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG25 | PF7 | | | | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG30 | PD11 | | | | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

### 5.22.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG995 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.66. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.22.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG995 is shown in the following figure.

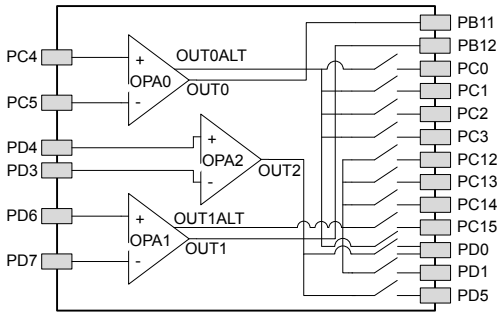



**Figure 5.44. Opamp Pinout**

# 6. BGA112 Package Specifications

## 6.1 BGA112 Package Dimensions

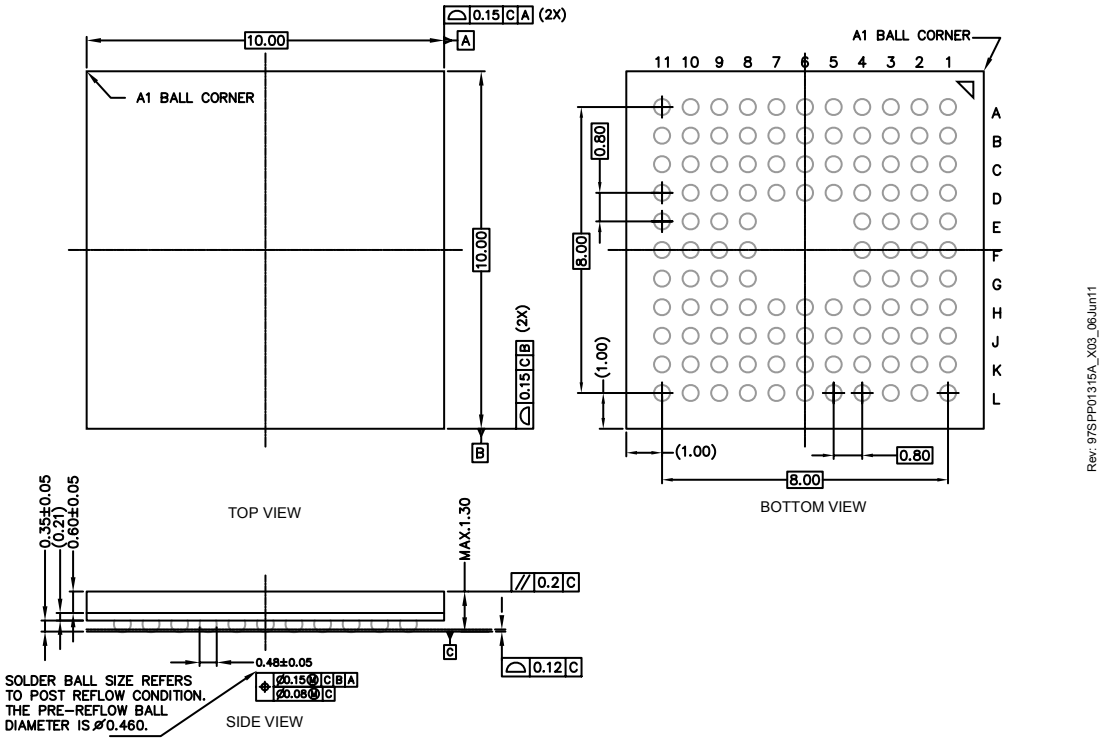



**Figure 6.1. BGA112**

**Note:**

1. The dimensions in parenthesis are reference.
2. Datum 'C' and seating plane are defined by the crown of the solder balls.
3. All dimensions are in millimeters.

### 6.2 BGA112 PCB Layout

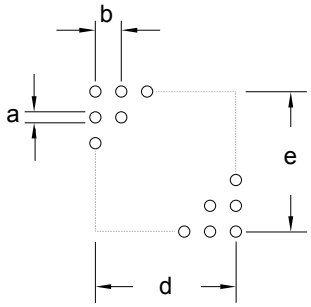



**Figure 6.2. BGA112 PCB Land Pattern**

**Table 6.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.35 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

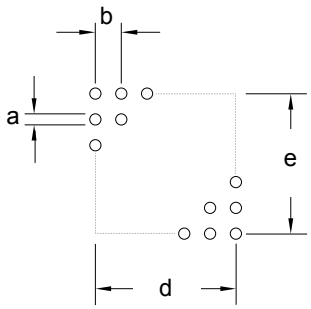



**Figure 6.3. BGA112 PCB Solder Mask**

**Table 6.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.48 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

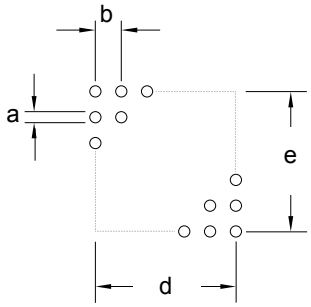



**Figure 6.4. BGA112 PCB Stencil Design**

**Table 6.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.33 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 6.3 BGA112 Package Marking

In the illustration below package fields and position are shown.

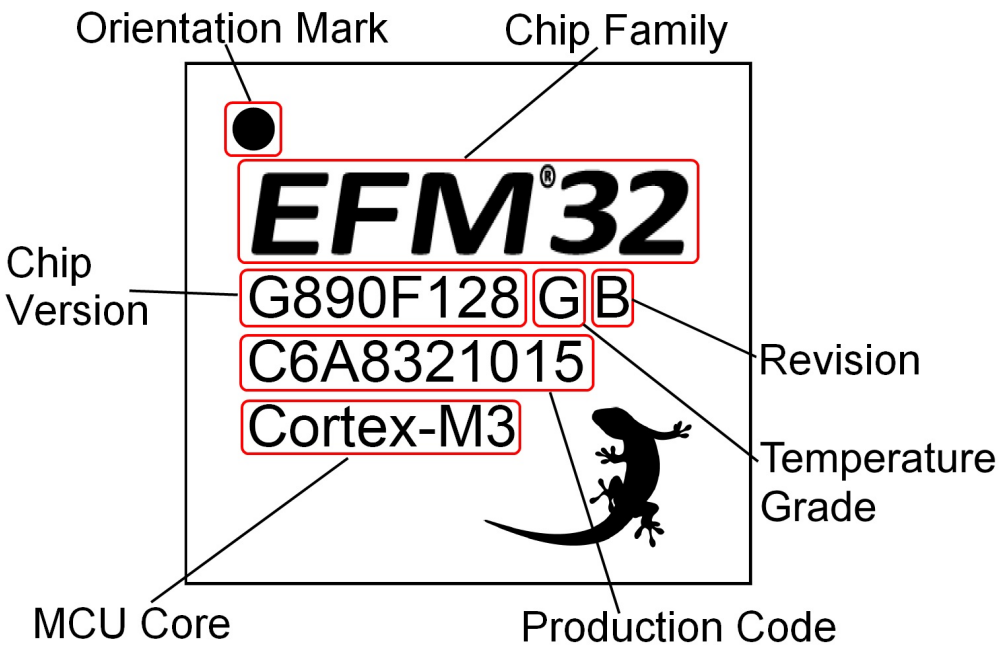



**Figure 6.5. Example Chip Marking (Top View)**

# 7. BGA120 Package Specifications

## 7.1 BGA120 Package Dimensions

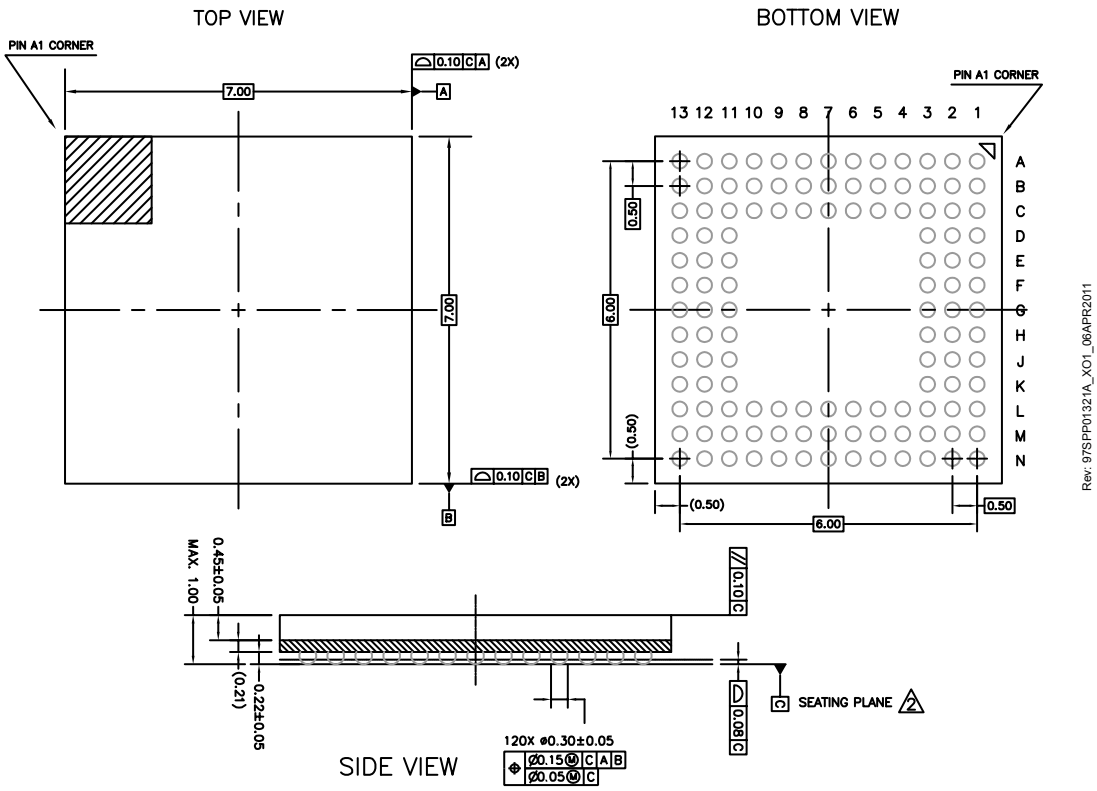



**Figure 7.1. BGA120**

**Note:**

1. The dimensions in parenthesis are reference.
2. Datum "C" and seating plane are defined by the crown of the soldier balls.
3. All dimensions are in millimeters.

### 7.2 BGA120 PCB Layout

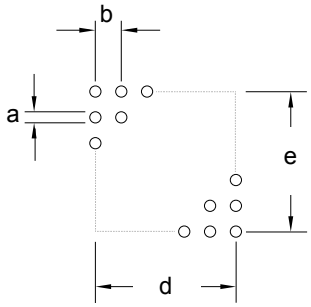



**Figure 7.2. BGA120 PCB Land Pattern**

**Table 7.1. BGA120 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.25 |
| b | 0.50 |
| d | 6.00 |
| e | 6.00 |

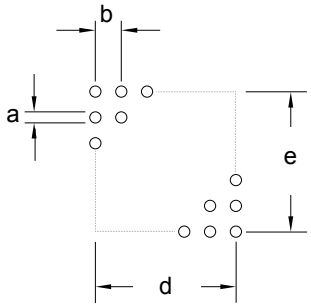



**Figure 7.3. BGA120 PCB Solder Mask**

**Table 7.2. BGA120 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.35 |
| b | 0.50 |
| d | 6.00 |
| e | 6.00 |

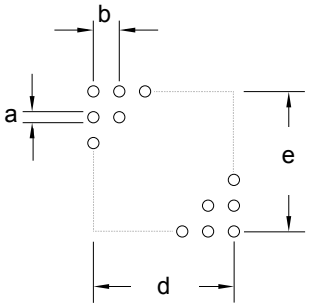



**Figure 7.4. BGA120 PCB Stencil Design**

**Table 7.3. BGA120 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.25 |
| b | 0.50 |
| d | 6.00 |
| e | 6.00 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 7.3 BGA120 Package Marking

In the illustration below package fields and position are shown.

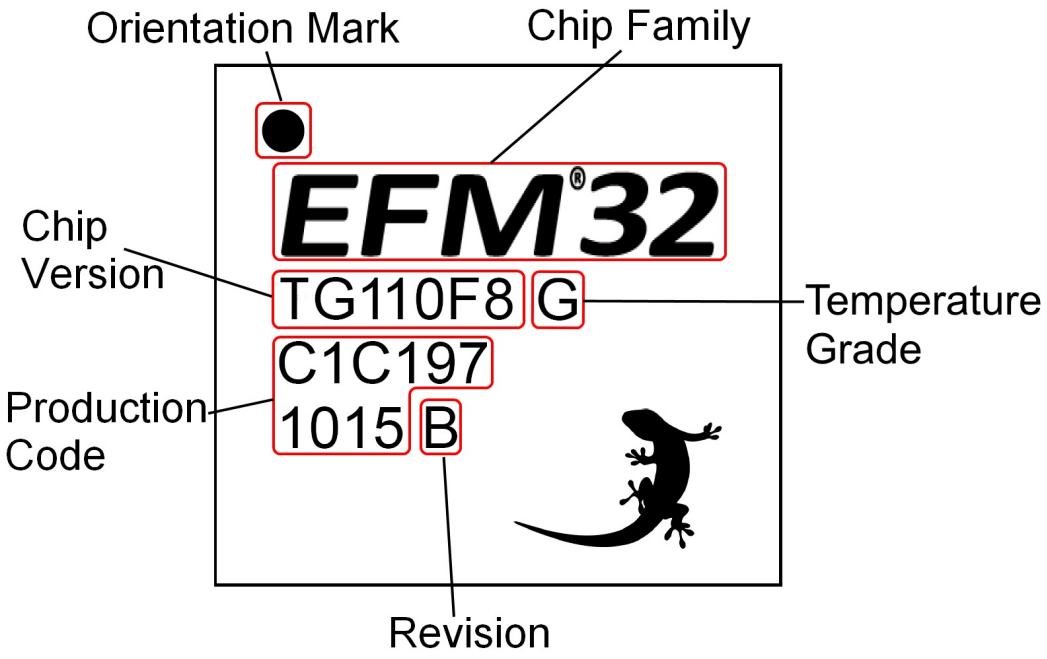



**Figure 7.5. Example Chip Marking (Top View)**

# 8. CSP81 Package Specifications

## 8.1 CSP81 Package Dimensions

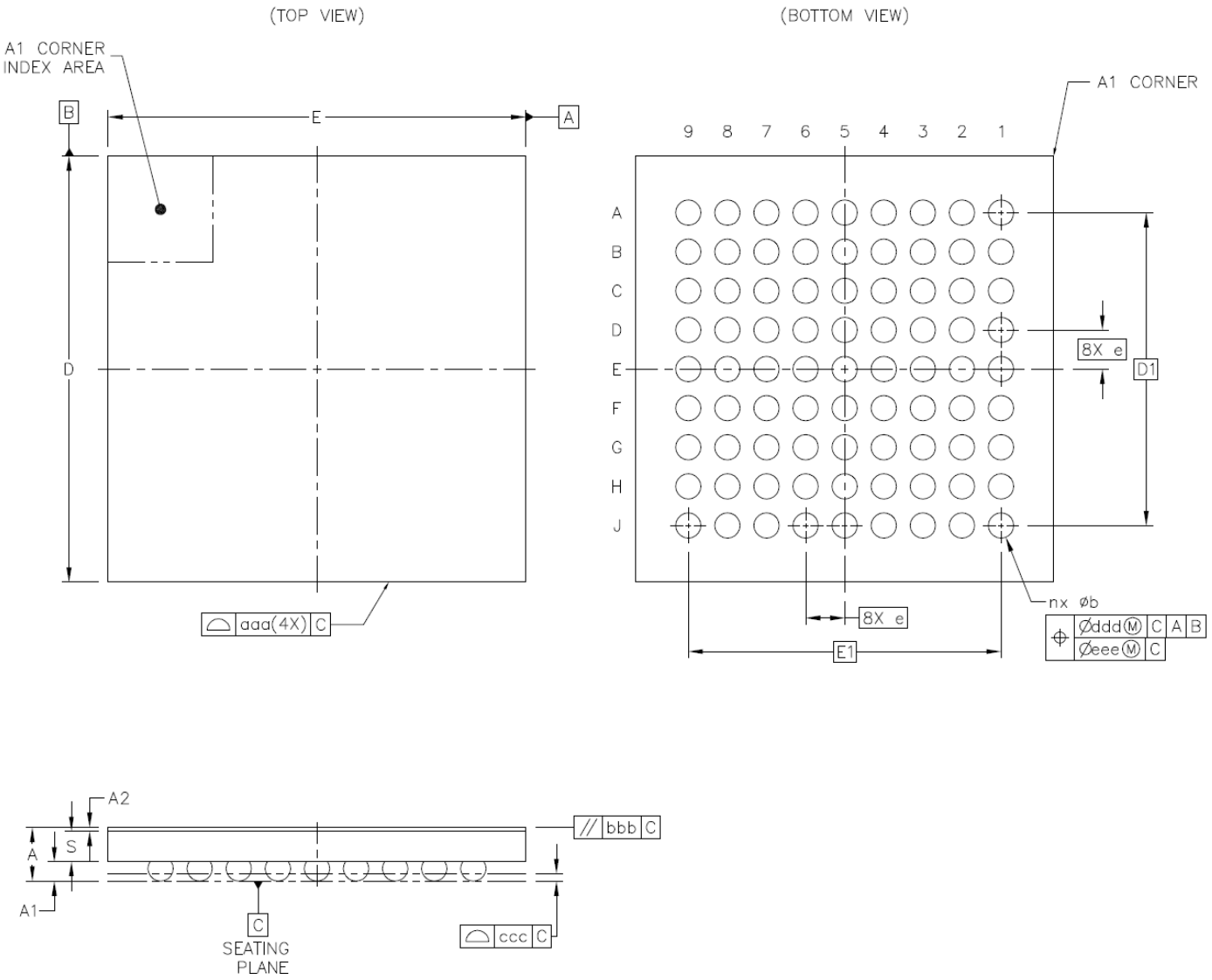



**Figure 8.1. CSP81**

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum “C” and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension “b” is measured at the maximum solder bump diameter, parallel to primary datum “C”.
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

**Table 8.1. CSP81 (Dimensions in mm)**

| Symbol | Min | Nom | Max |
|---|---|---|---|
| A | 0.491 | 0.55 | 0.609 |
| A1 | 0.17 | — | 0.23 |
| A2 | 0.036 | — | 0.044 |
| b | 0.23 | — | 0.29 |
| S | 0.3075 | 0.31 | 0.3125 |
| D | 4.355 BSC. | | |
| E | 4.275 BSC. | | |
| e | 0.40 BSC. | | |
| D1 | 3.20 BSC. | | |
| E1 | 3.20 BSC. | | |
| n | 81 | | |
| aaa | 0.05 | | |
| bbb | 0.10 | | |
| ccc | 0.075 | | |
| ddd | 0.15 | | |
| eee | 0.05 | | |

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 8.2 CSP81 PCB Layout

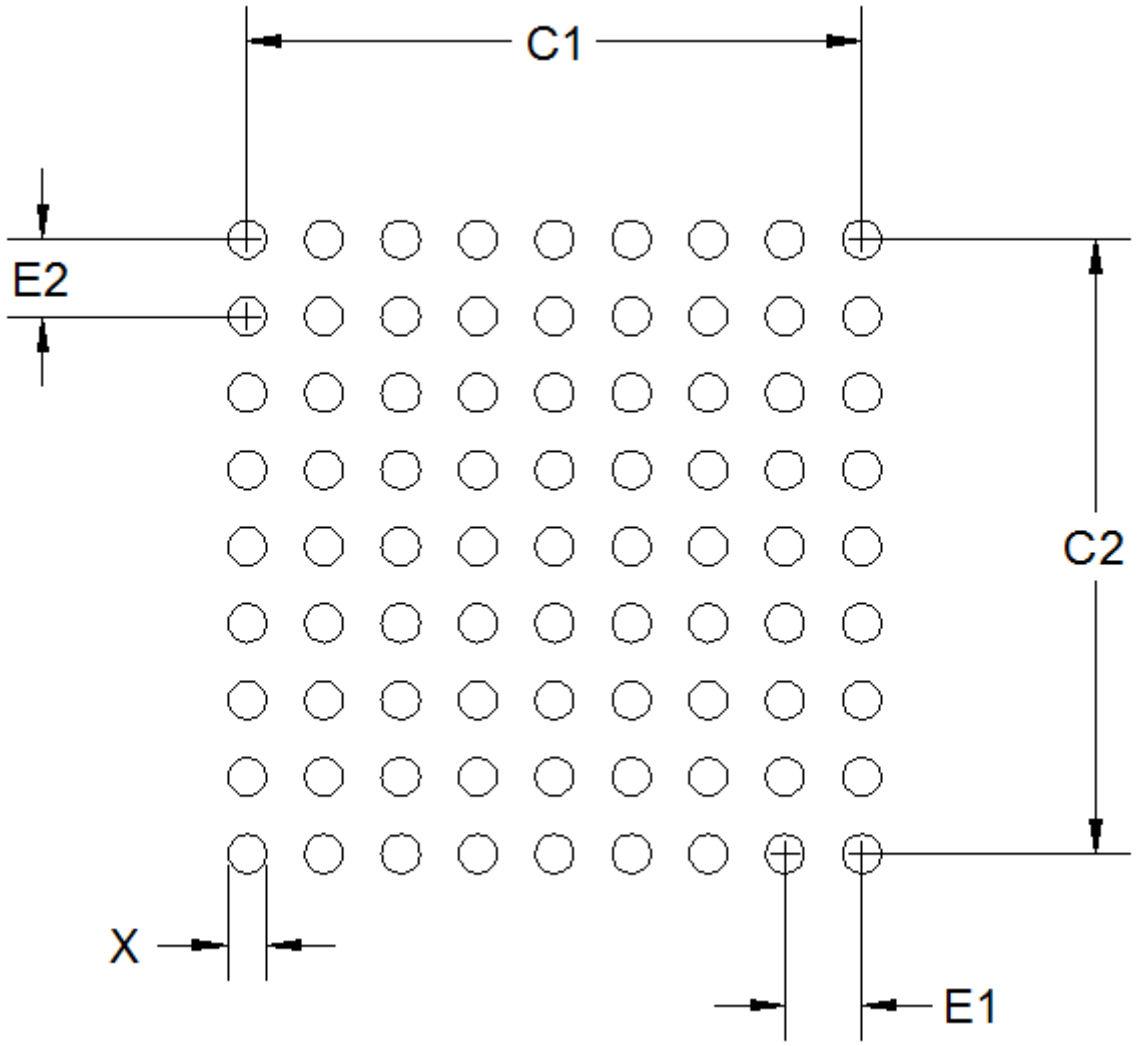



**Figure 8.2. CSP81 PCB Land Pattern**

**Table 8.2. CSP81 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| X | 0.20 |
| C1 | 3.20 |
| C2 | 3.20 |
| E1 | 0.40 |
| E2 | 0.40 |

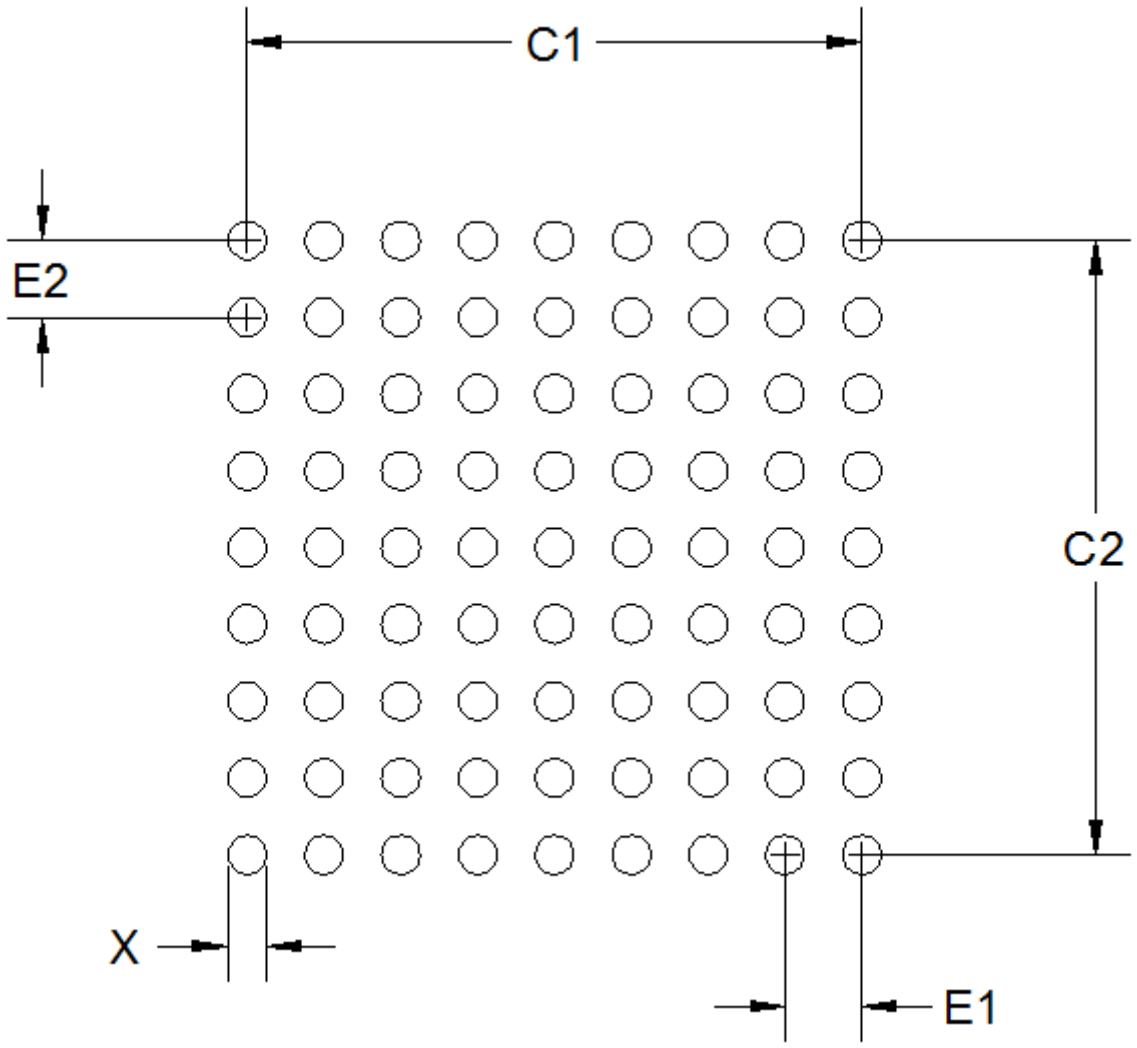



**Figure 8.3. CSP81 PCB Solder Mask**

**Table 8.3. CSP81 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| X | 0.26 |
| C1 | 3.20 |
| C2 | 3.20 |
| E1 | 0.40 |
| E2 | 0.40 |

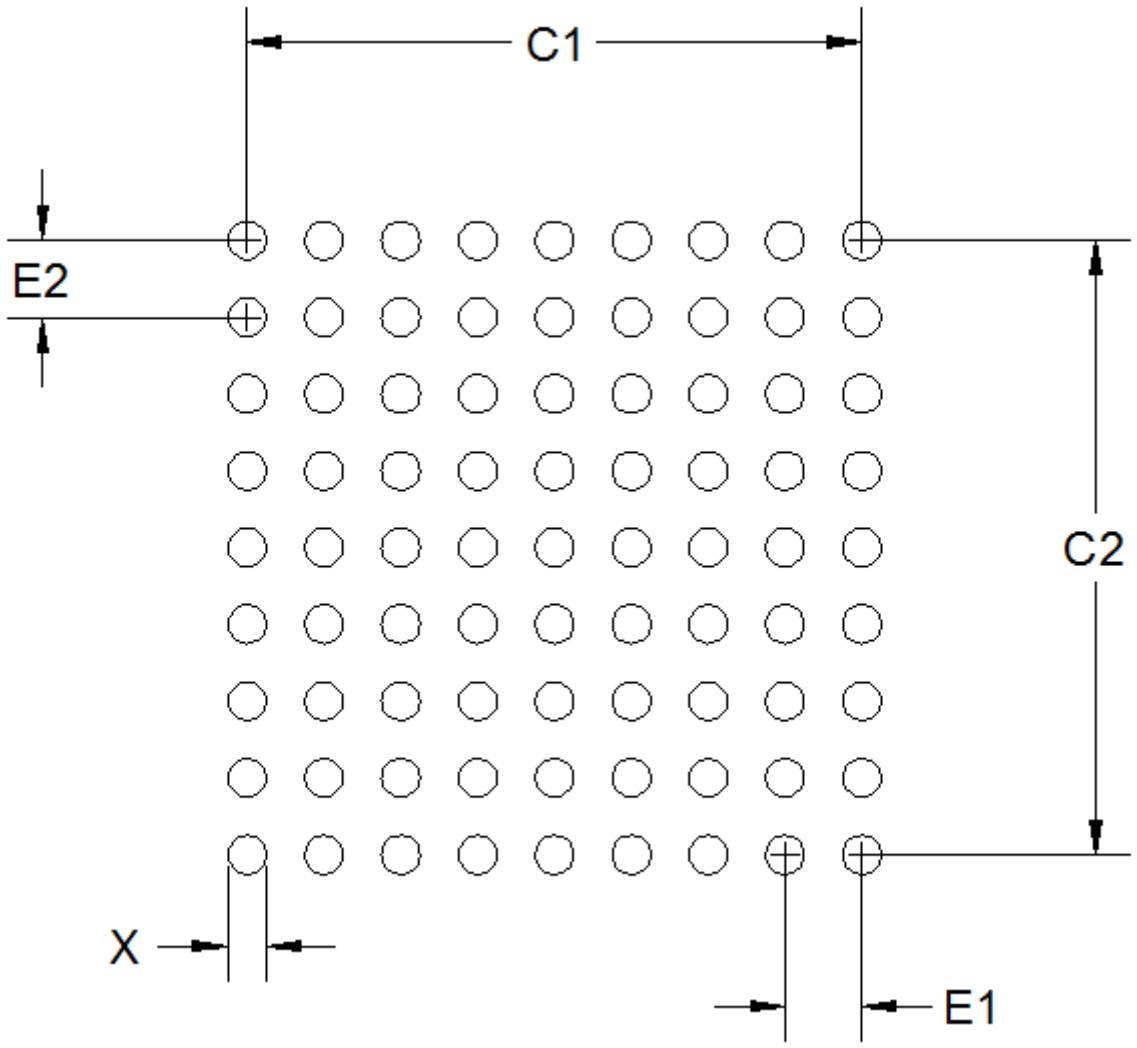



**Figure 8.4. CSP81 PCB Stencil Design**

**Table 8.4. CSP81 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| X | 0.20 |
| C1 | 3.20 |
| C2 | 3.20 |
| E1 | 0.40 |
| E2 | 0.40 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 8.3 CSP81 Package Marking

In the illustration below package fields and position are shown.

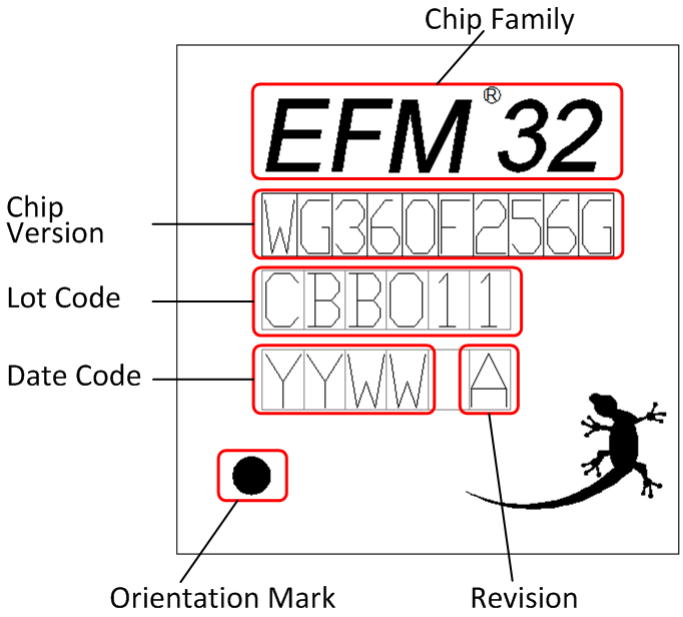



**Figure 8.5. Example Chip Marking (Top View)**

### 8.4 CSP81 Environmental

WLCSP devices can be handled and soldered using industry standard surface mount assembly techniques. However, because WLCSP devices are essentially a piece of silicon and are not encapsulated in plastic, they are susceptible to mechanical damage and may be sensitive to light. When WLCSPs must be used in an environment exposed to light, it may be necessary to cover the top and sides withan opaque material.

# 9. LQFP100 Package Specifications

## 9.1 LQFP100 Package Dimensions

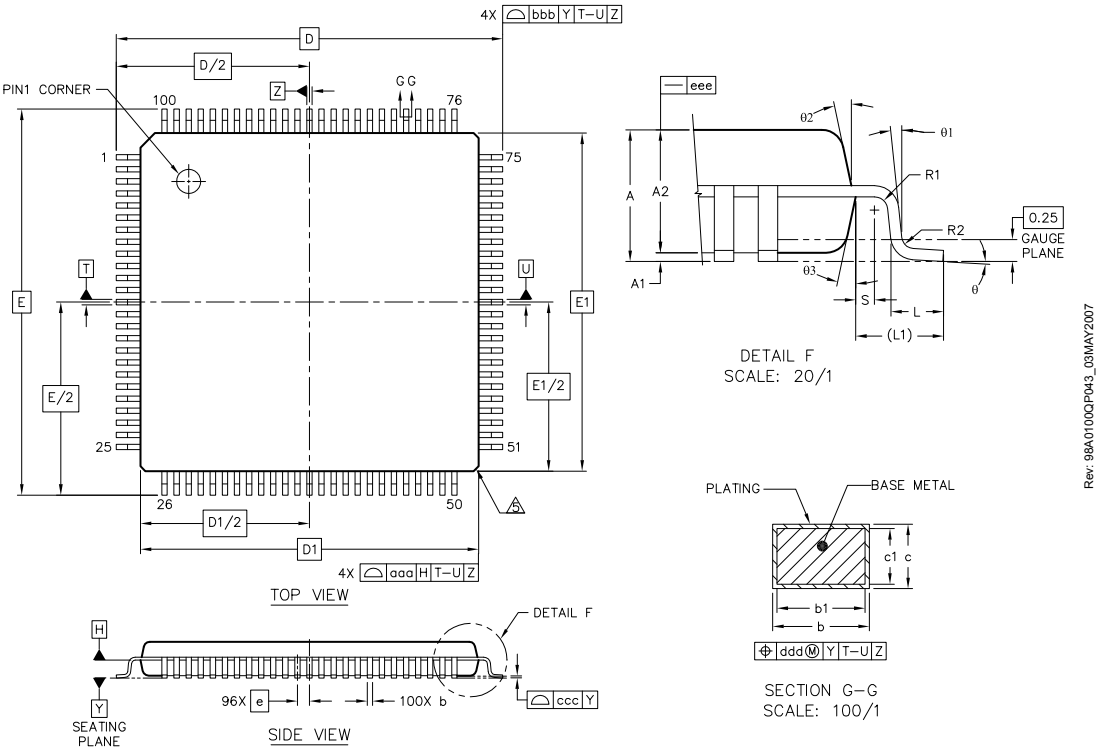



**Figure 9.1. LQFP100**

**Note:**

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
5. Exact shape of each corner is optional.

**Table 9.1. LQFP100 (Dimensions in mm)**

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| total thickness | | A | — | — | 1.6 |
| stand off | | A1 | 0.05 | — | 0.15 |
| mold thickness | | A2 | 1.35 | 1.4 | 1.45 |
| lead width (plating) | | b | 0.17 | 0.2 | 0.27 |
| lead width | | b1 | 0.17 | — | 0.23 |
| L/F thickness (plating) | | c | 0.09 | — | 0.2 |
| lead thickness | | c1 | 0.09 | — | 0.16 |
| | x | D | 16 BSC | | |
| | y | E | 16 BSC | | |
| body size | x | D1 | 14 BSC | | |
| | y | E1 | 14 BSC | | |
| lead pitch | | e | 0.5 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| footprint | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | — | — |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | — | — |
| | | R1 | 0.08 | — | 0.2 |
| | | S | 0.2 | — | — |
| package edge tolerance | | aaa | 0.2 | | |
| lead edge tolerance | | bbb | 0.2 | | |
| coplanarity | | ccc | 0.08 | | |
| lead offset | | ddd | 0.08 | | |
| mold flatness | | eee | 0.05 | | |

The LQFP100 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 9.2 LQFP100 PCB Layout

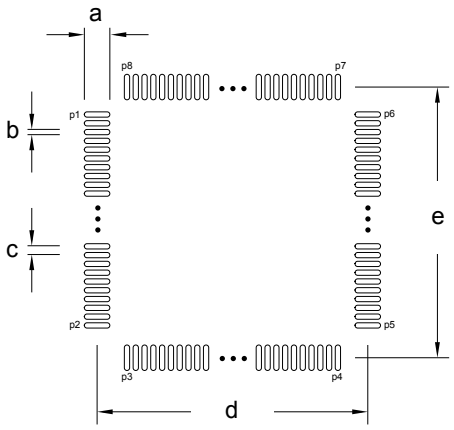



**Figure 9.2. LQFP100 PCB Land Pattern**

**Table 9.2. LQFP100 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 1.45 | P1 | 1 | P6 | 75 |
| b | 0.30 | P2 | 25 | P7 | 76 |
| c | 0.50 | P3 | 26 | P8 | 100 |
| d | 15.40 | P4 | 50 | | |
| e | 15.40 | P5 | 51 | | |

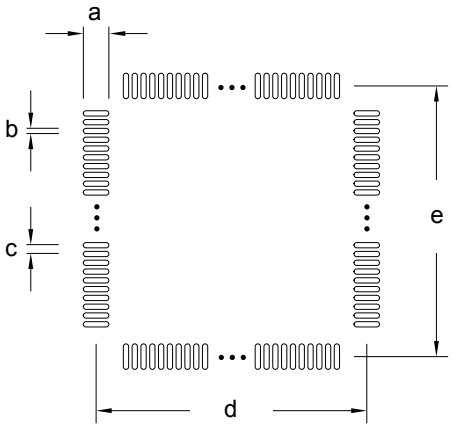



**Figure 9.3. LQFP100 PCB Solder Mask**

**Table 9.3. LQFP100 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 1.57 |
| b | 0.42 |
| c | 0.50 |
| d | 15.40 |
| e | 15.40 |

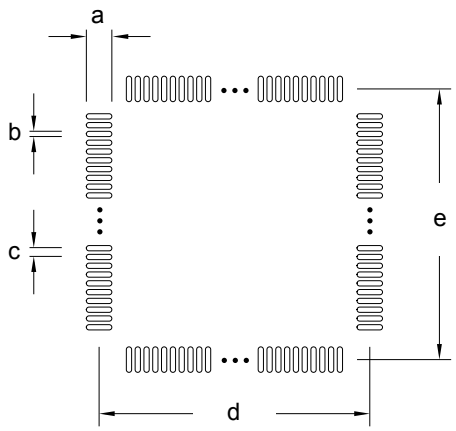



**Figure 9.4. LQFP100 PCB Stencil Design**

**Table 9.4. LQFP100 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 1.35 |
| b | 0.20 |
| c | 0.50 |
| d | 15.40 |
| e | 15.40 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 9.3 LQFP100 Package Marking

In the illustration below package fields and position are shown.

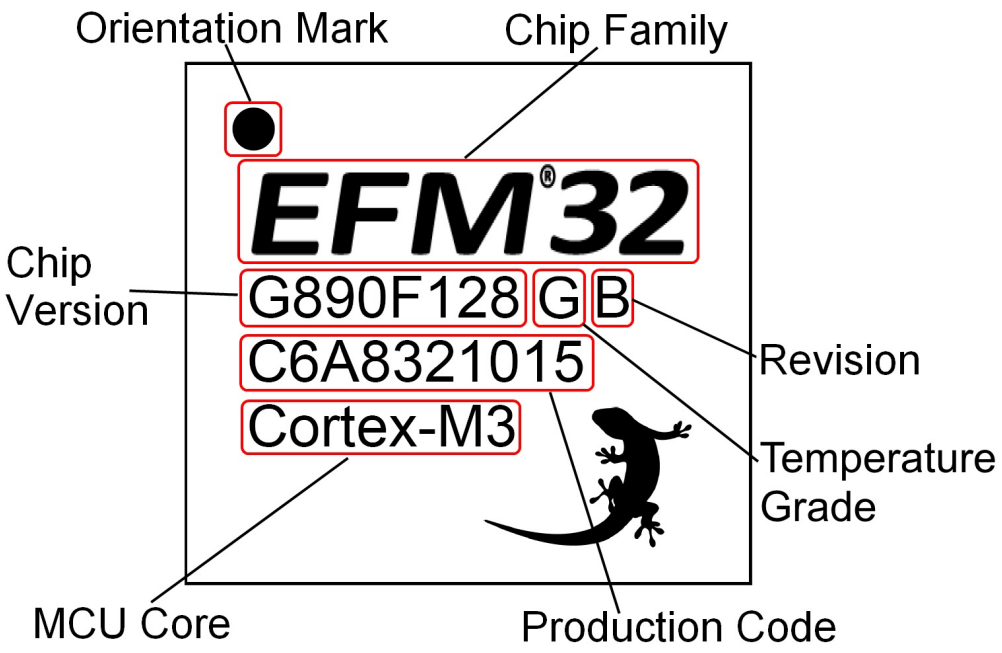



**Figure 9.5. Example Chip Marking (Top View)**

# 10. TQFP64 Package Specifications

## 10.1 TQFP64 Package Dimensions

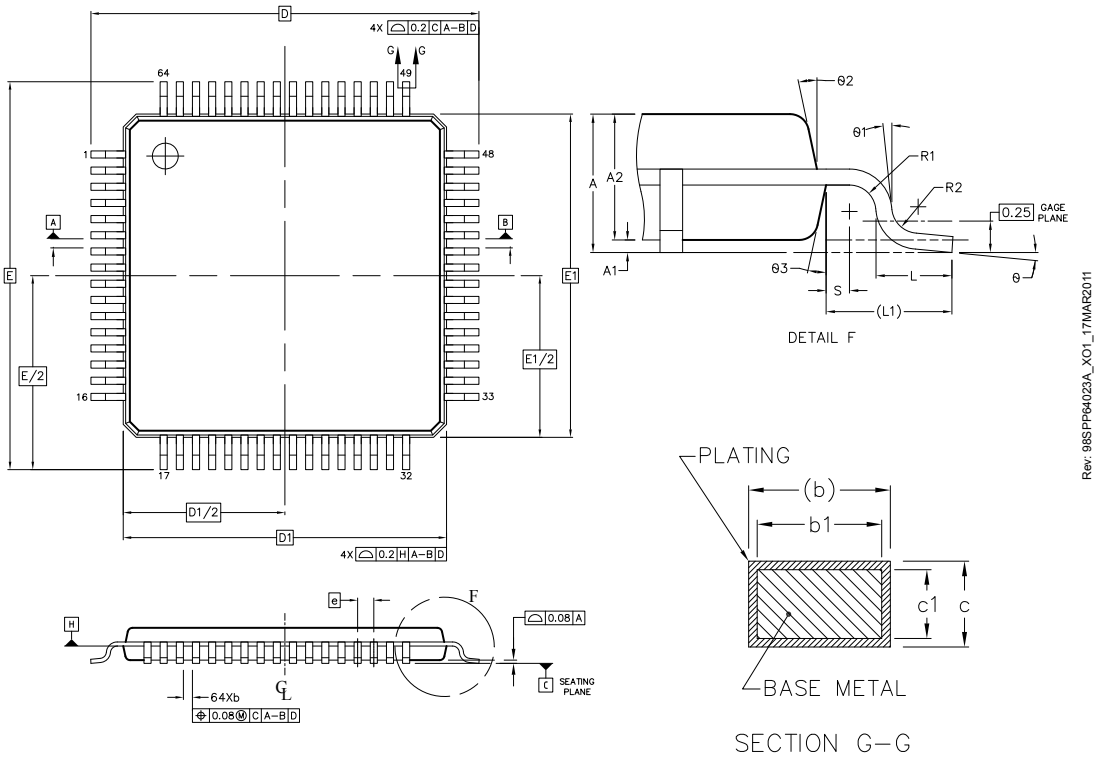



**Figure 10.1. TQFP64**

**Note:**

1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package body size.
3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.
4. To be determined at seating place 'C'.
5. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side. 'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
6. Detail of Pin 1 indicatifier are option all but must be located within the zone indicated.
7. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
8. Exact shape of each corner is optional.
9. These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. All dimensions are in millimeters.

**Table 10.1. QFP64 (Dimensions in mm)**

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|
| A | — | 1.10 | 1.20 | L1 | | — | |
| A1 | 0.05 | — | 0.15 | R1 | 0.08 | — | — |
| A2 | 0.95 | 1.00 | 1.05 | R2 | 0.08 | — | 0.20 |
| b | 0.17 | 0.22 | 0.27 | S | 0.20 | — | — |
| b1 | 0.17 | 0.20 | 0.23 | θ | 0° | 3.5° | 7° |
| c | 0.09 | — | 0.20 | θ1 | 0° | — | — |
| C1 | 0.09 | — | 0.16 | θ2 | 11° | 12° | 13° |
| D | 12.0 BSC | | | θ3 | 11° | 12° | 13° |
| D1 | 10.0 BSC | | | | | | |
| e | 0.50 BSC | | | | | | |
| E | 12.0 BSC | | | | | | |
| E1 | 10.0 BSC | | | | | | |
| L | 0.45 | 0.60 | 0.75 | | | | |

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 10.2 TQFP64 PCB Layout

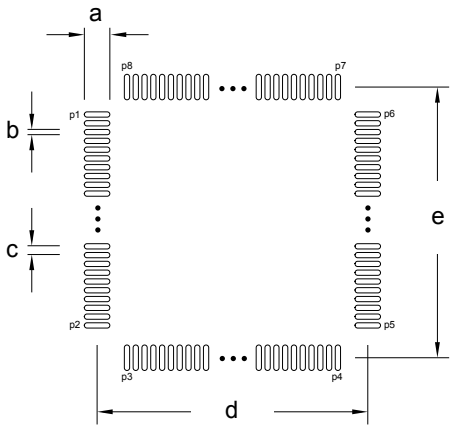



**Figure 10.2. TQFP64 PCB Land Pattern**

**Table 10.2. TQFP64 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 1.60 | P1 | 1 | P6 | 48 |
| b | 0.30 | P2 | 16 | P7 | 49 |
| c | 0.50 | P3 | 17 | P8 | 64 |
| d | 11.50 | P4 | 32 | | |
| e | 11.50 | P5 | 33 | | |

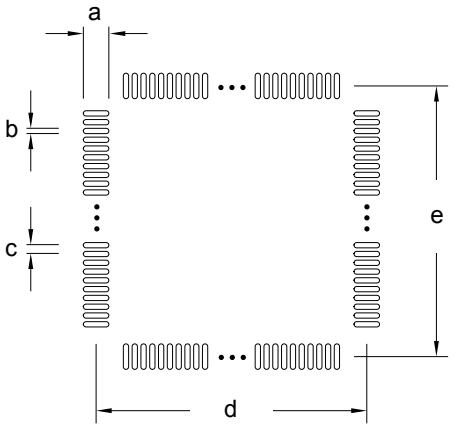



**Figure 10.3. TQFP64 PCB Solder Mask**

**Table 10.3. TQFP64 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 1.72 |
| b | 0.42 |
| c | 0.50 |
| d | 11.50 |
| e | 11.50 |

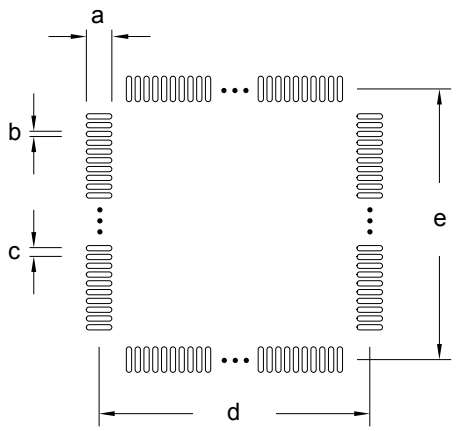



**Figure 10.4. TQFP64 PCB Stencil Design**

**Table 10.4. TQFP64 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 1.50 |
| b | 0.20 |
| c | 0.50 |
| d | 11.50 |
| e | 11.50 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 10.3 TQFP64 Package Marking

In the illustration below package fields and position are shown.

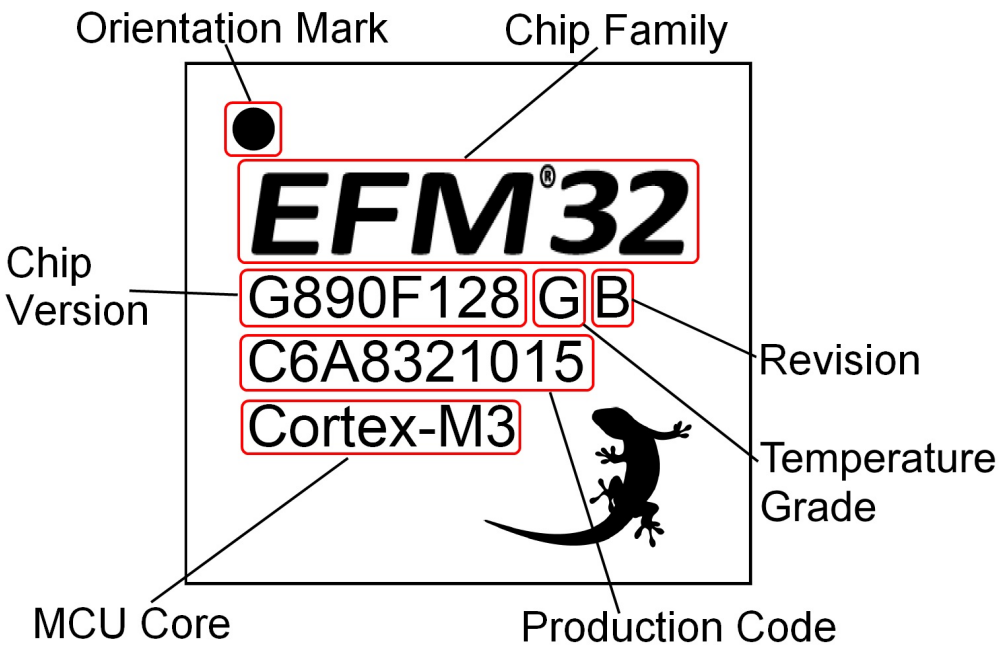



**Figure 10.5. Example Chip Marking (Top View)**

# 11. QFN64 Package Specifications

## 11.1 QFN64 Package Dimensions

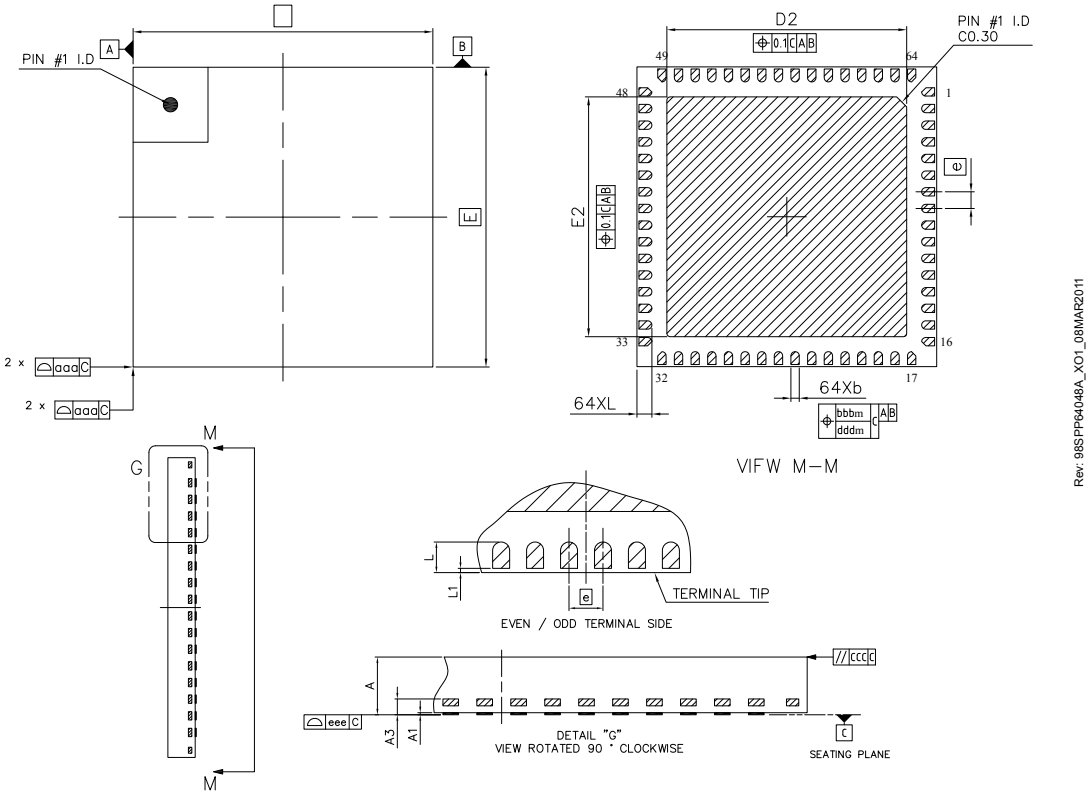



**Figure 11.1. QFN64**

**Note:**

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

**Table 11.1. QFN64 (Dimensions in mm)**

| Symbol | Min | Nom | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | — | 0.05 |
| A3 | | 0.203 REF | |
| b | 0.20 | 0.25 | 0.30 |
| D | | 9.00 BSC | |
| E | | 9.00 BSC | |
| D2 | 7.10 | 7.20 | 7.30 |
| E2 | 7.10 | 7.20 | 7.30 |
| e | | 0.50 BSC | |
| L | 0.40 | 0.45 | 0.50 |
| L1 | 0.00 | — | 0.10 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |

The QFN64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 11.2 QFN64 PCB Layout

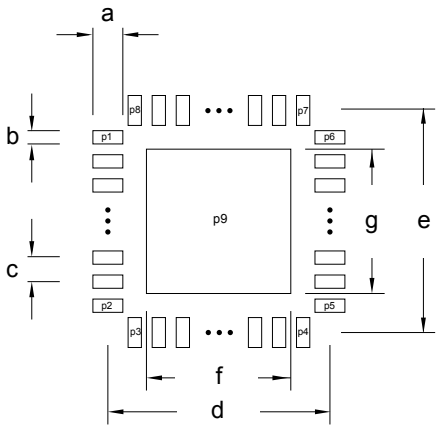



**Figure 11.2. QFN64 PCB Land Pattern**

**Table 11.2. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 0.85 | P1 | 1 | P8 | 64 |
| b | 0.30 | P2 | 16 | P9 | 0 |
| c | 0.50 | P3 | 17 | | |
| d | 8.90 | P4 | 32 | | |
| e | 8.90 | P5 | 33 | | |
| f | 7.20 | P6 | 48 | | |
| g | 7.20 | P7 | 49 | | |

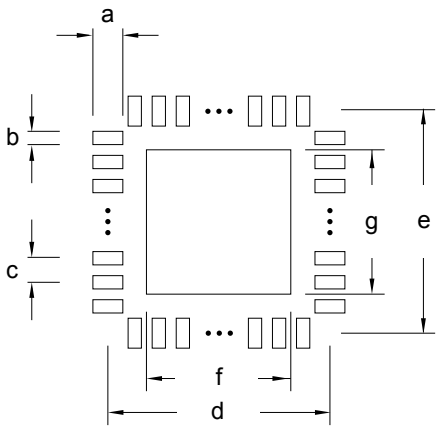



**Figure 11.3. QFN64 PCB Solder Mask**

**Table 11.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|---|---|---|---|
| a | 0.97 | e | 8.90 |
| b | 0.42 | f | 7.32 |
| c | 0.50 | g | 7.32 |

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|---|---|---|---|
| d | 8.90 | - | - |

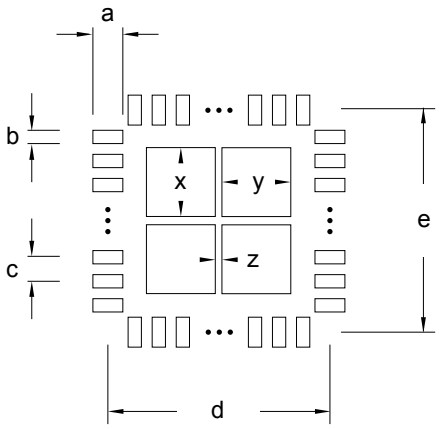



**Figure 11.4. QFN64 PCB Stencil Design**

**Table 11.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|---|---|---|---|
| a | 0.75 | e | 8.90 |
| b | 0.22 | x | 2.70 |
| c | 0.50 | y | 2.70 |
| d | 8.90 | z | 0.80 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 11.3 QFN64 Package Marking

In the illustration below package fields and position are shown.

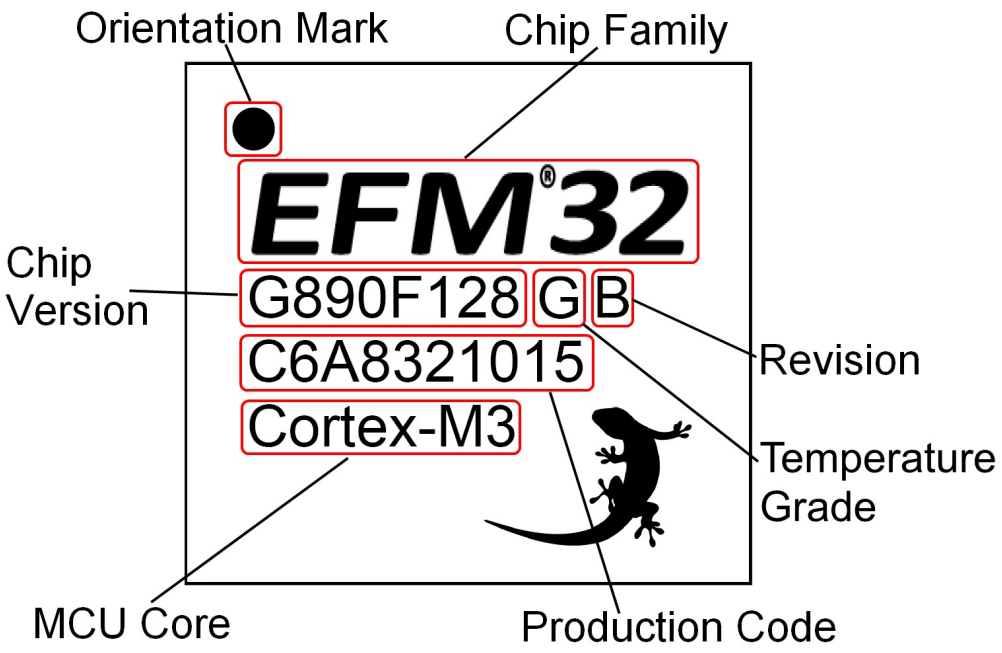



**Figure 11.5. Example Chip Marking (Top View)**

# 12. Wafer Specifications

## 12.1 Bonding Instructions

All pads should be bonded out, with the exception of the pads labeled “NC” and listed as “Do not connect” in Padout. Gold bond wires are recommended for these devices.

All three voltage regulator output decouple pads (DEC_0, DEC_1, DEC_2) must be bonded out and electrically connected on the PCB. In the packaged devices, these three pads are all bonded to a single DECOUPLE pin.

If the USB feature of EFM32WG900 will be used, all of the USB pads must be bonded out, and

- both USB_VREGO_0 and USB_VREGO_1 must be bonded out and electrically connected on the PCB. In the packaged devices, these two pads are both bonded to a single USB_VREGO pin.
- both USB_VREGI_0 and USB_VREGI_1 must be bonded out and electrically connected on the PCB. In the packaged devices, these two pads are both bonded to a single USB_VREGI pin.

## 12.2 Wafer Description

**Table 12.1. Wafer and Die Information**

| Parameter | Value |
|---|---|
| Device Family | EFM32WG (Wonder Gecko) |
| Wafer Diameter | 8 in |
| Die Dimensions (Outer edge of seal ring) | Contact sales for information |
| Wafer Thickness (No backgrind) | 725 µm ±15 µm (28.54 mil ±1 mil) |
| Wafer Identification | Notch |
| Scribe Street Width | 80 µm × 160 µm |
| Die Per Wafer[1] | Contact sales for information |
| Passivation | Standard |
| Wafer Packaging Detail | Wafer Jar |
| Bond Pad Dimensions | 65 µm (parallel to die edge) × 66 µm |
| Bond Pad Pitch Minimum | 76 µm |
| Maximum Processing Temperature | 250°C |
| Electronic Die Map Format | .txt |

**Note:**
1. This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).

### 12.2.1 Environmental

Bare silicon die are susceptible to mechanical damage and may be sensitive to light. When bare die must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

### 12.3 Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18 - 24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

### 12.4 Failure Analysis (FA) Guidelines

Certain conditions must be met for Silicon Laboratories to perform Failure Analysis on devices sold in wafer form.

- In order to conduct failure analysis on a device in a customer-provided package, Silicon Laboratories must be provided with die assembled in an industry standard package that is pin compatible with existing packages Silicon Laboratories offers for the device. Initial response time for FA requests that meet these requirements will follow the standard FA guidelines for packaged parts.
- If retest of the entire wafer is requested, Silicon Laboratories must be provided with the whole wafer. Silicon Laboratories cannot retest any wafers that have been sawed, diced, backgrind or are on tape. Initial response time for FA requests that meet these requirements will be 3 weeks.

# 13. Chip Revision, Solder Information, Errata

## 13.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

## 13.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

## 13.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

# 14. Revision History

### Revision 2.10

November, 2018

- 2. Ordering Information – Corrected QFN, QFP, and BGA ordering code errors introduced in datasheet v2.00. Corrected ordering code decoder.
- Table 3.6 EFM32WG330 Configuration Summary on page 29 - Corrected number of GPIOs.
- Table 3.18 EFM32WG940 Configuration Summary on page 53 - Corrected number of GPIOs.
- Corrected available ACMP0 and ACMP1 channels in the following Configuration Summary sections:
  - 3.2.6 EFM32WG330
  - 3.2.7 EFM32WG332
  - 3.2.9 EFM32WG380
  - 3.2.10 EFM32WG390
  - 3.2.12 EFM32WG840
  - 3.2.13 EFM32WG842
  - 3.2.18 EFM32WG940
  - 3.2.19 EFM32WG942
  - 3.2.20 EFM32WG980
  - 3.2.21 EFM32WG990
- Added 4.4 Backup Supply Domain.
- 4.8 Flash - Updated page erase time and device erase time and added footnotes.
- 11.2 QFN64 PCB Layout - Corrected pin number for symbol P9.

**Revision 2.00**

July, 2018

- Consolidated all EFM32WG data sheets:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG360
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG900
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- Added a Feature List section.
- 2. Ordering Information – Added ordering code decoder.
- 3.3 Memory Map – Separated the Memory Map into two figures – one for core and code space listing and one for peripheral listing.
- 4.2 Absolute Maximum Ratings – Updated preface. Removed the footnote about storage temperature and added max source/sink current per I/O pin.
- Environmental – Removed this section. Environmental specifications are available in the qualification report.
- 4.5 Current Consumption – Updated typical and added maximum current specifications for the highest energy mode, $I_{EM0}$.
- 4.8 Flash – Added word write cycles between erase ($WWC_{FLASH}$) specification.
- 4.9 General Purpose Input Output – Reduced maximum input leakage current ($I_{IOLEAK}$, max).
- 4.10.2 HFXO – Replaced “energyAware Designer” with “Configurator tool”.
- 4.10.3 LFRCO – Added (min, typ, max) specifications for oscillation frequency over full power supply and full temperature range. Also added typical voltage drift and temperature drift specs.
- 4.10.3 LFRCO – Updated graphs for calibrated LFRCO Frequency vs. Temperature and Supply Range, and also fixed y-axis unit [kHz].
- 4.10.4 HFRCO – Added specifications for oscillation frequency over full power supply and temperature range, added typical voltage drift and temperature drift specs at each frequency band, and removed the duty cycle spec ($DC_{HFRCO}$).
- 4.10.4 HFRCO – Updated all HFRCO graphs (various frequency bands).
- 4.10.5 AUXHFRCO – Updated test conditions for oscillation frequency.
- 4.10.5 AUXHFRCO – Removed the duty cycle spec for AUXHFRCO ($DC_{AUXHFRCO}$).

- 4.11 Analog Digital Converter (ADC) – Added footnote for average active current, updated conditions for INL and DNL. Added the following specs:
  - Input bias current ($I_{ADCBIASIN}$) – added max (source and sink).
  - Input offset current ($I_{ADCOFFSETIN}$) – added max (source and sink).
  - VREF output voltage ($V_{REF}$) – added min, typ, max.
  - VREF voltage drift ($V_{REF_VDRIFT)}$ – added min, typ, max.
  - VREF temperature drift ($V_{REF_TDRIFT}$) – added min, typ, max.
  - VREF current consumption ($I_{VREF}$) – added typ, max, replacing $I_{ADCREF}$.
  - ADC and DAC VREF matching ($V_{REF_MATCH}$) – added typical.
- 4.12 Digital Analog Converter (DAC) – Updated parameter description, test conditions, and footnote for average current ($I_{DAC)}$), and added the following new VREF specs at each voltage reference:
  - VREF output voltage ($V_{REF}$) – added min, typ, max.
  - VREF voltage drift ($V_{REF_VDRIFT}$) – added min, typ, max.
  - VREF temperature drift ($V_{REF_TDRIFT}$) – added min, typ, max.
  - VREF current consumption ($I_{VREF}$) – added typ, max.
  - ADC and DAC VREF matching ($V_{REF_MATCH}$) – added typical.
- 4.13 Operational Amplifier (OPAMP) – Removed note specifying that OPAMP specs stem from simulations, and added new specifications for the following:
  - Active Current ($I_{OPAMP}$) – new specifications at various (new) bias program settings.
  - Gain Bandwidth Product ($GBW_{OPAMP}$) – new (typ) specifications at new bias program settings and DC bias settings, and added footnotes.
  - Input Offset Voltage ($V_{OFFSET}$) – specified min, typ, max for Op Amps (OPA0-1).
  - Input Bias Current ($I_{OPAMPBIASIN}$) – new min and max specifications.
  - Input Offset Current ($I_{OPAMPOFF-SETIN}$) – new min and max specifications.
  - Slew Rate ($SR_{OPAMP}$) – new specifications at new bias program settings.
- 4.14 Analog Comparator (ACMP) – Added new specifications for the following:
  - Input Bias Current ($I_{ACMPBIASIN}$) – added min and max.
  - Input Offset Current ($I_{ACMPOFFSETIN}$) – added min and max.
  - Active Current ($I_{ACMP}$) – added two new condition settings and footnote.
  - Negative Response Time ($t_{RESPONSE_N}$) – added new specifications.
  - Positive Response Times ($t_{RESPONSE_P}$) – added new specifications.
  - Offset Voltage ($V_{ACMPOFFSET}$) – added specifications at new bias program settings.
  - ACMP Hysteresis ($V_{ACMPHYST}$) – added specifications for negative and positive hysteresis at various bias program settings.
  - VDD SCALED Input Accuracy ($V_{VDDSCALED}$) – added new specifications (typical).
- 4.15 Voltage Comparator (VCMP)– Added the following new specifications:
  - Footnote for active current, $I_{VCMP}$.
  - Negative hysteresis ($V_{VCMPHYST_N}$), replacing VCMP hysteresis.
  - Positive hysteresis ($V_{VCMPHYST_P}$), replacing VCMP hysteresis.
  - Hysteresis Delta ($V_{VCMPHYST_DELTA}$).
  - Negative Response Time ($t_{RESPONSE_N}$).
  - Positive Response Time ($t_{RESPONSE_P}$).
- 4.19 USART SPI – Corrected parameter descriptions for $t_{CS_DIS_MI}$.
- 4.20 Digital Peripherals – Added (typical) LE Peripheral Interface Clock Current ($I_{LFCLK}$) specifications with both the LFXO-LFA and LFXO-LFB clock trees.
- Removed MSL information (Moisture Sensitivity Level). Instead, MSL information can be found in the Qual report that is available on the Silicon Labs website.
- 6.1 BGA112 Package Dimensions – Removed statements regarding materials used.
- 7.1 BGA120 Package Dimensions – Removed statements regarding materials used.
- New formatting throughout.

**Revision 1.40**

June 13th, 2014

- This revision applies the following devices:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- Removed "Preliminary" markings.
- Corrected single power supply voltage minimum value from 1.85V to 1.98V.
- Added AUXHFRCO to blockdiagram and electrical characteristics.
- Updated current consumption data.
- Updated transition between energy modes data.
- Updated power management data.
- Updated GPIO data.
- Updated LFRCO, HFRCO and ULFRCO data.
- For devices with ADC, updated ADC data.
- For devices with DAC, updated DAC data.
- For devicse with OPAMP, updated OPAMP data.
- For devices with ACMP, updated ACMP data.
- For devices with VCMP, updated VCMP data.
- For devices with EBI, added EBI timing chapter.

**Revision 1.31**

November 21st, 2013

- This revision applies the following devices:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- Updated errata-link.
- Updated chip marking.
- Added link to Environmental and Quality information.
- For devices with DAC, re-added missing DAC-data.

**Revision 1.30**

September 30th, 2013

- This revision applies the following devices:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- Added I2C characterization data.
- Added SPI characterization data.
- Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.
- For devices with USB, added the USB bootloader information.
- Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.
- Updated the EM0 and EM1 current consumption numbers. Updated the the EM1 plots and removed the EM0 plots.
- For QFN64 packages, removed UART mentioned incorrectly in the QFN64 parts.
- Updated Environmental information.
- Updated trademark, disclaimer and contact information.
- Other minor corrections.

**Revision 1.20**

June 28th, 2013

- This revision applies the following devices:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- For BGA120 packages, corrected pinout top view figure.
- For all BGA pacakges, updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.
- Updated power requirements in the Power Management section.
- Removed minimum load capacitance figure and table. Added reference to application note.
- Other minor corrections.

March 16th, 2015

- This revision applies the following devices:
  - EFM32WG900
- Corrected pad numbers and the order of the pads in the padout table so that it matches the drawing.

**Revision 1.10**

May 6th, 2013

- This revision applies the following devices:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- Updated current consumption table and figures in Electrical characteristics section.
- Other minor corrections.

December 12th, 2014

- This revision applies the following devices:
  - EFM32WG900
- Added recommendation to use gold bond wire.

**Revision 1.00**

September 11th, 2012

- This revision applies the following devices:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- Updated the HFRCO 1 MHz band typical value to 1.2 MHz.
- Updated the HFRCO 7 MHz band typical value to 6.6 MHz.
- For BGA112 and BGA120 packages, corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

October 15th, 2014

- This revision applies the following devices:
  - EFM32WG360
  - EFM32WG900
- Initial release.

**Revision 0.95**

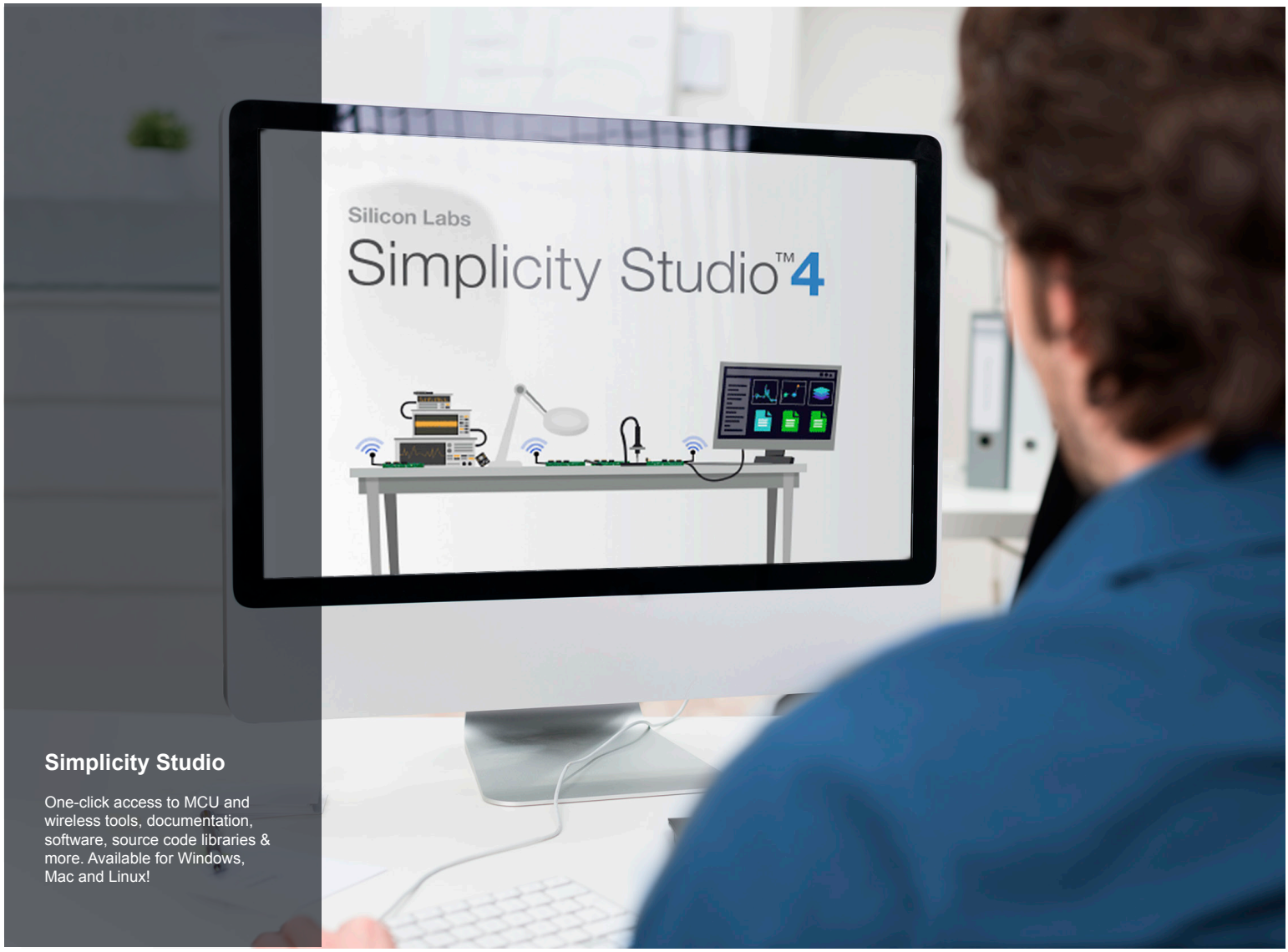
May 3rd, 2012

- This revision applies the following devices:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- Updated EM2/EM3 current consumption at 85°C.

**Revision 0.90**

February 27th, 2012

- This revision applies the following devices:
  - EFM32WG230
  - EFM32WG232
  - EFM32WG280
  - EFM32WG290
  - EFM32WG295
  - EFM32WG330
  - EFM32WG332
  - EFM32WG380
  - EFM32WG390
  - EFM32WG395
  - EFM32WG840
  - EFM32WG842
  - EFM32WG880
  - EFM32WG890
  - EFM32WG895
  - EFM32WG940
  - EFM32WG942
  - EFM32WG980
  - EFM32WG990
  - EFM32WG995
- Initial preliminary release.

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*ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703*

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