

## FEATURES

- Allows Safe Board Insertion and Removal from a Live Backplane
- System Reset Output with Programmable Delay
- Programmable Electronic Circuit Breaker
- User-Programmable Supply Voltage Power-Up Rate
- High Side Driver for an External N-Channel FET
- Controls Supply Voltages from 2.7V to 12V
- Undervoltage Lockout
- Soft Reset Input
- Glitch Filter on RESET
- Available in 8-Pin Narrow PDIP and SO Packages

## APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker

## DESCRIPTION

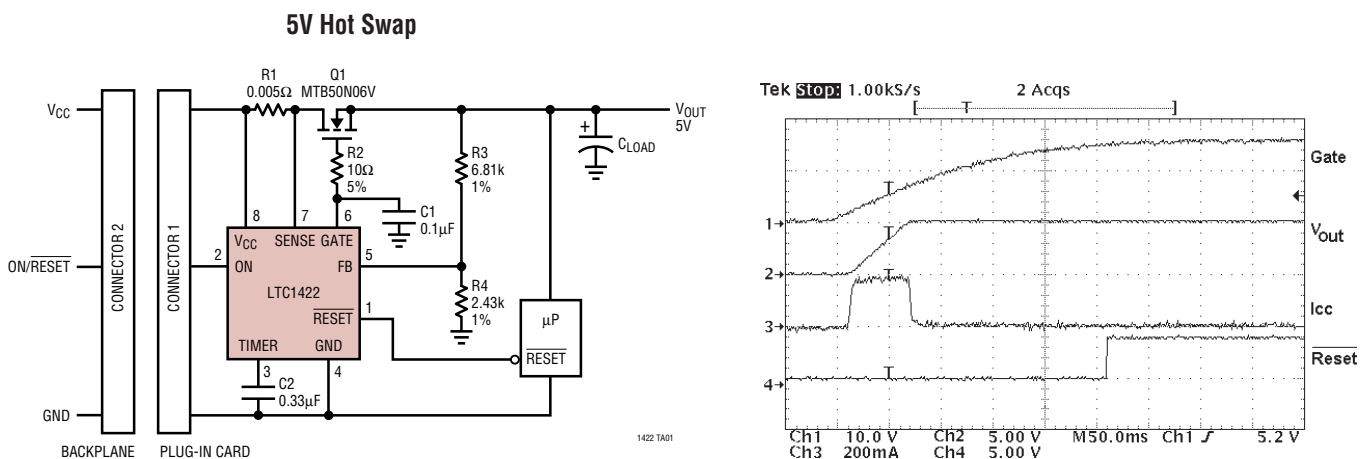
The LTC<sup>®</sup>1422 is an 8-pin Hot Swap<sup>™</sup> controller that allows a board to be safely inserted and removed from a live backplane. Using an external N-channel pass transistor, the board supply voltage can be ramped up at a programmable rate. A high side switch driver controls the N-channel gate for supply voltages ranging from 2.7V to 12V.

A programmable electronic circuit breaker protects against shorts. The  $\overline{\text{RESET}}$  output can be used to generate a system reset when the supply voltage falls below a programmable voltage. The ON pin can be used to cycle the board power or to generate a soft reset.

The LTC1422 is available in 8-pin PDIP and SO packages.

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 Hot Swap is a trademark of Linear Technology Corporation.

## TYPICAL APPLICATION

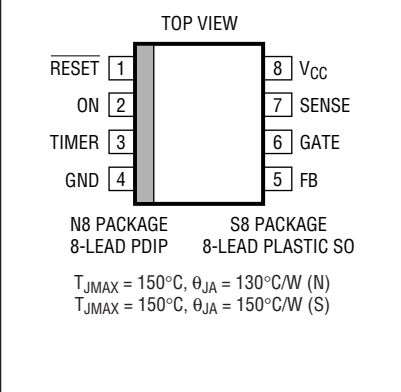


## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ( $V_{CC}$ )	13.2V
Input Voltage (TIMER, SENSE) ...	-0.3V to ( $V_{CC} + 0.3V$ )
Input Voltage (FB, ON)	-0.3V to 13.2V
Output Voltage ( $\overline{\text{RESET}}$ )	-0.3V to 20V
Output Voltage (GATE)	-0.3V to 20V
Operating Temperature Range	
LTC1422C	0°C to 70°C
LTC1422I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

## PACKAGE/ORDER INFORMATION

 <p>TOP VIEW</p> <p>RESET 1      8 <math>V_{CC}</math></p> <p>ON 2      7 SENSE</p> <p>TIMER 3      6 GATE</p> <p>GND 4      5 FB</p> <p>N8 PACKAGE      S8 PACKAGE</p> <p>8-LEAD PDIP      8-LEAD PLASTIC SO</p> <p><math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 130^{\circ}\text{C/W}</math> (N)</p> <p><math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 150^{\circ}\text{C/W}</math> (S)</p>	ORDER PART NUMBER
	<p>LTC1422CN8</p> <p>LTC1422CS8</p> <p>LTC1422IN8</p> <p>LTC1422IS8</p>
	S8 PART MARKING
	<p>1422</p> <p>1422I</p>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

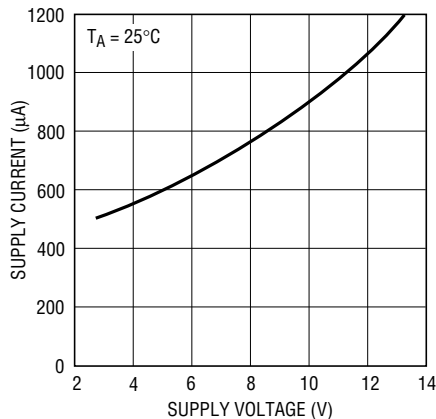
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{CC} = 5V$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>DC Characteristics</b>							
$I_{CC}$	$V_{CC}$ Supply Current	ON = $V_{CC}$	●		0.65	1.00	mA
$V_{LKO}$	$V_{CC}$ Undervoltage Lockout		●	2.40	2.47	2.55	V
$V_{LKH}$	$V_{CC}$ Undervoltage Lockout Hysteresis				120		mV
$V_{FB}$	FB Pin Voltage Threshold		●	1.220	1.232	1.244	V
$\Delta V_{FB}$	FB Pin Threshold Line Regulation	$3V \leq V_{CC} \leq 12V$	●		0.5	2.5	mV
$V_{FBHST}$	FB Pin Voltage Threshold Hysteresis				2.0		mV
$V_{TM}$	TIMER Pin Voltage Threshold		●	1.208	1.232	1.256	V
$\Delta V_{TM}$	TIMER Pin Threshold Line Regulation	$3V \leq V_{CC} \leq 12V$	●		2	15	mV
$V_{TMHST}$	TIMER Pin Voltage Threshold Hysteresis				45		mV
$I_{TM}$	TIMER Pin Current	Timer On, $GND \leq V_{TIMER} \leq 1.5V$ Timer Off, $V_{TIMER} = 1.5V$	●	-2.5	-2.0	-1.5	$\mu\text{A}$ mA
$V_{CB}$	Circuit Breaker Trip Voltage	$V_{CB} = (V_{CC} - V_{SENSE})$	●	44	50	64	mV
$I_{CP}$	GATE Pin Output Current	Charge Pump On, $V_{GATE} = GND$ Charge Pump Off, $V_{GATE} = V_{CC}$	●	-12	-10	-8	$\mu\text{A}$ mA
$\Delta V_{GATE}$	External N-Channel Gate Drive	$V_{GATE} - V_{CC}$	●	10	12	14	V
$V_{ONHI}$	ON Pin Threshold High		●	1.25	1.30	1.35	V
$V_{ONLO}$	ON Pin Threshold Low		●	1.20	1.23	1.26	V
$V_{ONHYST}$	ON Pin Hysteresis				80		mV
$V_{OL}$	Output Low Voltage	$\overline{\text{RESET}}$ , $I_O = 3\text{mA}$	●		0.14	0.4	V
$I_{PU}$	Logic Output Pull-Up Current	$\overline{\text{RESET}} = GND$			-12		$\mu\text{A}$
$t_{RST}$	Soft Reset Time		●	22	30	48	$\mu\text{s}$

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

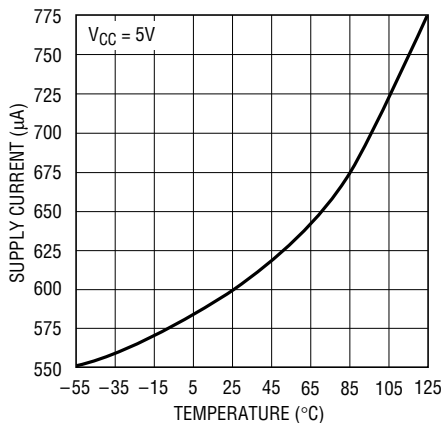
# TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current vs Supply Voltage**



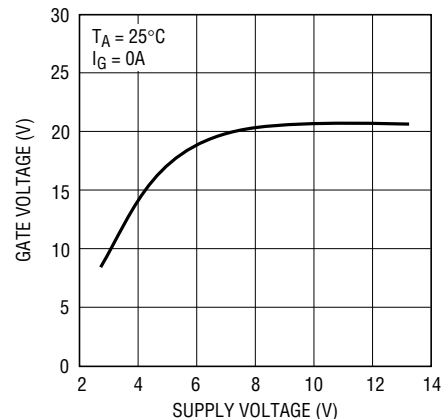
1422 G01

**Supply Current vs Temperature**



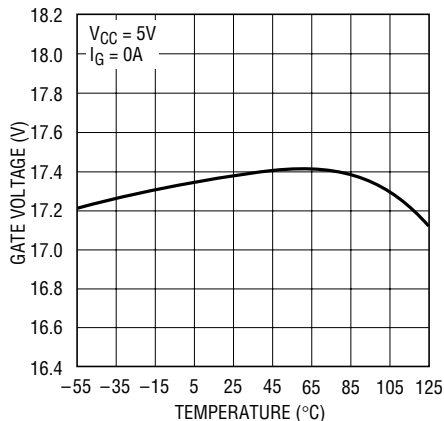
1422 G02

**Gate Voltage ( $V_{GATE}$ ) vs Supply Voltage**



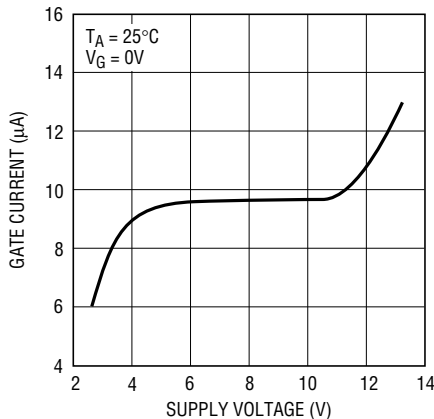
1422 G03

**Gate Voltage ( $V_{GATE}$ ) vs Temperature**



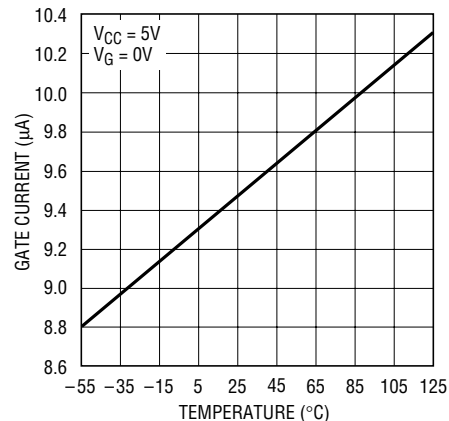
1422 G04

**Gate Current vs Supply Voltage**



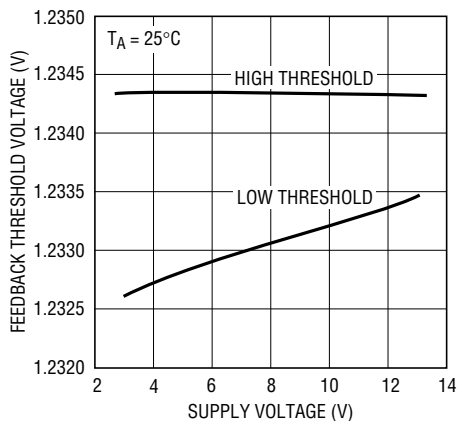
1422 G05

**Gate Current vs Temperature**



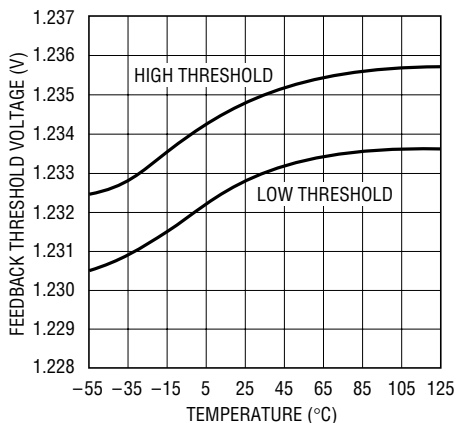
1422 G06

**Feedback Threshold Voltage vs Supply Voltage**



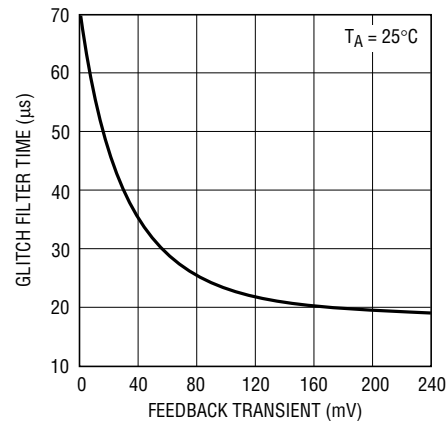
1422 G07

**Feedback Threshold Voltage vs Temperature**



1422 G08

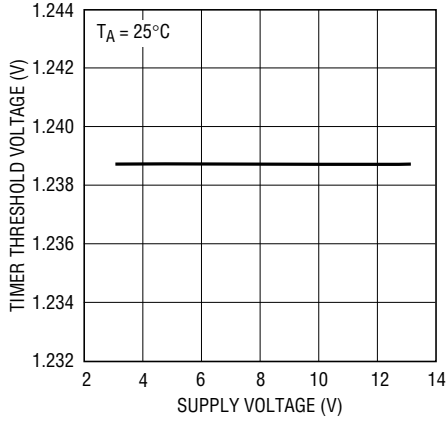
**Glitch Filter Time vs Feedback Transient**



1422 G09

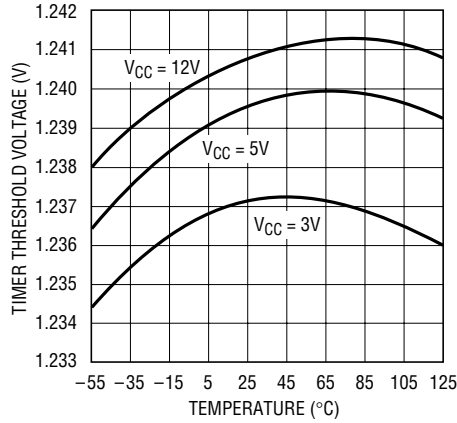
**TYPICAL PERFORMANCE CHARACTERISTICS**

**TIMER Threshold Voltage vs Supply Voltage**



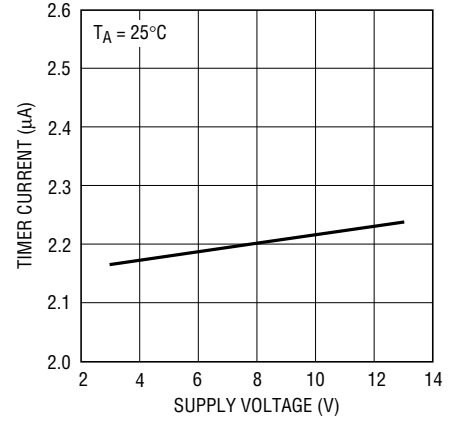
1422 G10

**TIMER Threshold Voltage vs Temperature**



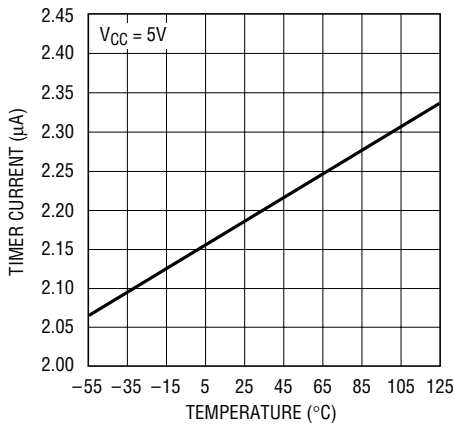
1422 G11

**TIMER Current vs Supply Voltage**



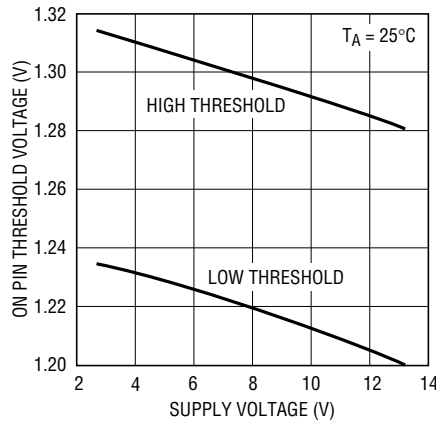
1422 G12

**TIMER Current vs Temperature**



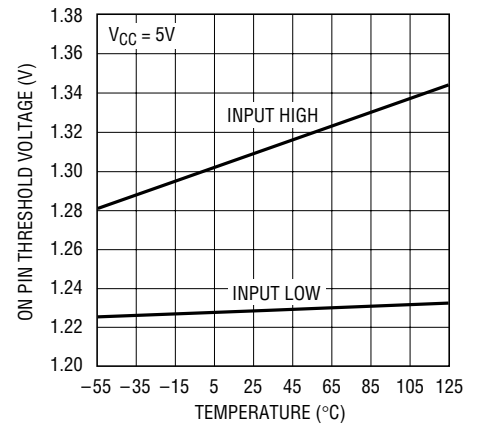
1422 G13

**ON Pin Threshold Voltage vs Supply Voltage**



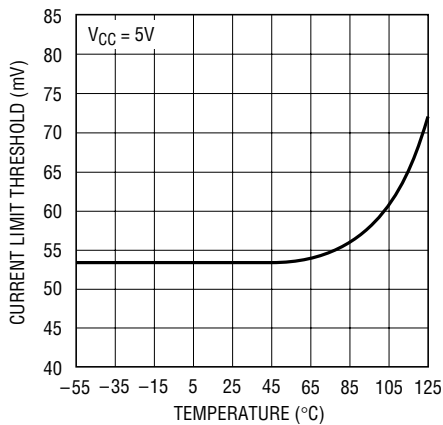
1422 G14

**ON Pin Threshold Voltage vs Temperature**



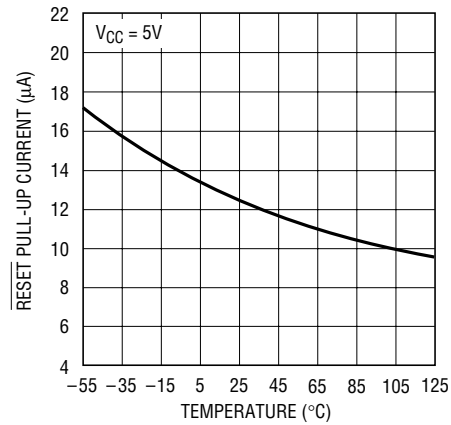
1422 G15

**Current Limit Threshold vs Temperature**



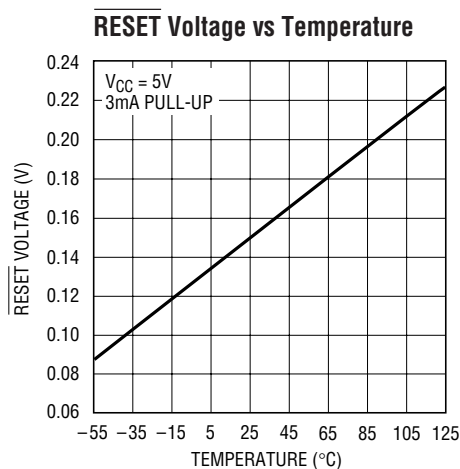
1422 G17

**RESET Pull-Up Current vs Temperature**

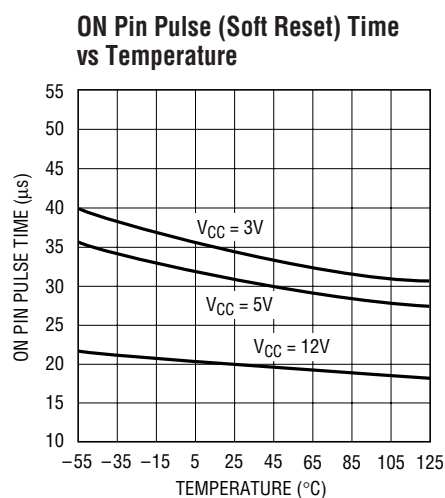


1422 G18

## TYPICAL PERFORMANCE CHARACTERISTICS



1422 G19



1422 G20

## PIN FUNCTIONS

**RESET (Pin 1)**: Open drain output to GND with a 12μA pull-up to V<sub>CC</sub>. This pin is pulled low when the voltage at the FB (Pin 5) goes below the FB pin threshold. The RESET pin will go high one timing cycle after the voltage at the FB pin goes above the FB pin threshold. An external pull-up resistor can be used to speed up the rising edge on the RESET pin or pull the pin to a voltage higher or lower than V<sub>CC</sub>.

**ON (Pin 2)**: Analog Input Pin. The threshold is set at 1.30V with 80mV hysteresis. When the ON pin is pulled high, the timer turns on for one cycle, then the charge pump turns on. When the ON pin is pulled low longer than 40μs, the GATE pin will be pulled low and remain off until the ON pin is pulled high.

If the ON pin is pulled low for less than 15μs a soft reset will occur. The charge pump remains on, and the RESET pin is pulled low for one timing cycle starting 30μs from the falling edge of the ON pin.

The ON pin is also used to reset the electronic circuit breaker. If the ON pin is cycled low and high following the trip of the circuit breaker, the circuit breaker is reset and a normal power-up sequence will occur.

**TIMER (Pin 3)**: Analog system timing generator pin. This pin is used to set the delay before the charge pump turns on after the ON pin goes high. It also sets the delay before the RESET pin goes high, after the output supply voltage is good, as sensed by the FB pin.

When the timer is off, an internal N-channel shorts the TIMER pin to ground. When the timer is turned on, a 2μA current from V<sub>CC</sub> is connected to the TIMER pin and the voltage starts to ramp up with a slope given by:  $dV/dt = 2\mu A/C_{TIMER}$ . When the voltage reaches the trip point (1.232V), the timer will be reset by pulling the TIMER pin back to ground. The timer period is given by:  $(1.232V \cdot C_{TIMER})/2\mu A$ .

**GND (Pin 4)**: Chip Ground.

**FB (Pin 5)**: Analog comparator input used to monitor the output supply voltage with an external resistive divider. When the voltage on the FB pin is lower than the 1.232V, the RESET pin will be pulled low. An internal filter helps prevent negative voltage glitches from triggering a reset. When the voltage on the FB pin rises above the trip point, the RESET pin will go high after one timing cycle.

## PIN FUNCTIONS

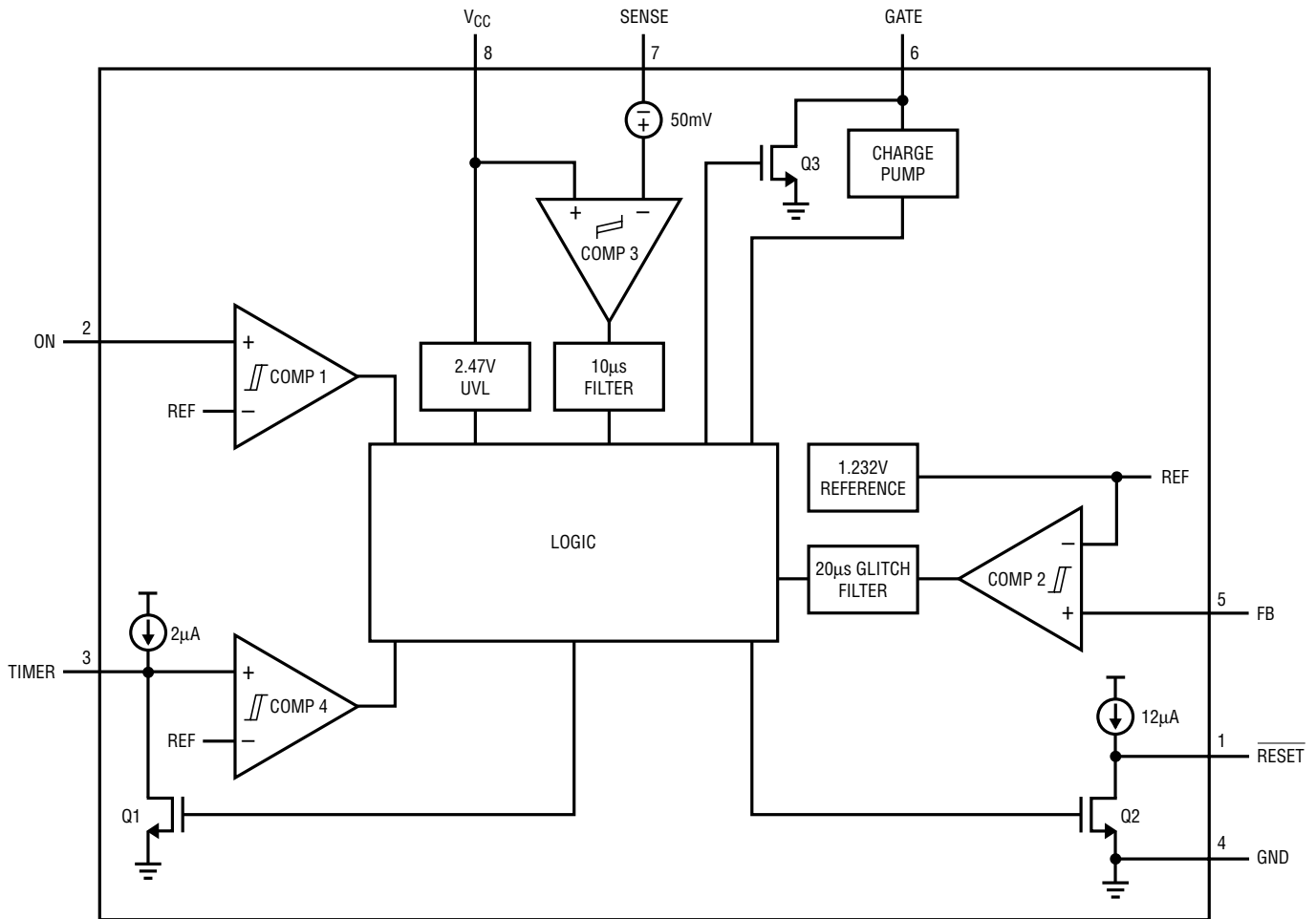
**GATE (Pin 6):** The high side gate drive for the external N-Channel. An internal charge pump guarantees at least 10V of gate drive when  $V_{CC}$  is 5V. The slope of the voltage rise or fall at the GATE is set by an external capacitor connected between GATE and GND, and the  $10\mu\text{A}$  charge pump output current. When the circuit breaker trips, the undervoltage lockout circuit monitoring  $V_{CC}$  trips, or the ON pin is pulled low for more than  $40\mu\text{s}$ , the GATE pin is immediately pulled to GND.

**SENSE (Pin 7) :** Circuit Breaker Set Pin. With a sense resistor placed in the supply path between  $V_{CC}$  and SENSE,

the circuit breaker will trip when the voltage across the resistor exceeds 50mV for more than  $10\mu\text{s}$ . If the circuit breaker trip current is set to twice the normal operating current, only 25mV is dropped across the sense resistor during normal operation. To disable the circuit breaker,  $V_{CC}$  and SENSE can be shorted together.

**$V_{CC}$  (Pin 8):** The positive supply input, ranging from 2.7V to 13.2V for normal operation.  $I_{CC}$  is typically 0.6mA. An undervoltage lockout circuit disables the chip until the voltage at  $V_{CC}$  is greater than 2.47V.

## BLOCK DIAGRAM



1422 BD

## APPLICATIONS INFORMATION

### Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors on the board can draw huge transient currents from the backplane power bus as they charge up. The transient currents can cause permanent damage to the connector pins and cause glitches on the system supply, causing other boards in the system to reset.

The LTC1422 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The chip also provides a system reset signal to indicate when board supply voltage drops below a programmable voltage.

### Power Supply Ramping

The onboard power supply is controlled by placing an external N-channel pass transistor in the power path (Figure 1). R1 provides current fault detection and R2 prevents high frequency oscillation. By ramping up the gate of the pass transistor at a controlled rate, the transient surge current ( $I = C \cdot dV/dt$ ) drawn from the main backplane supply can be limited to a safe value when the board makes connection.

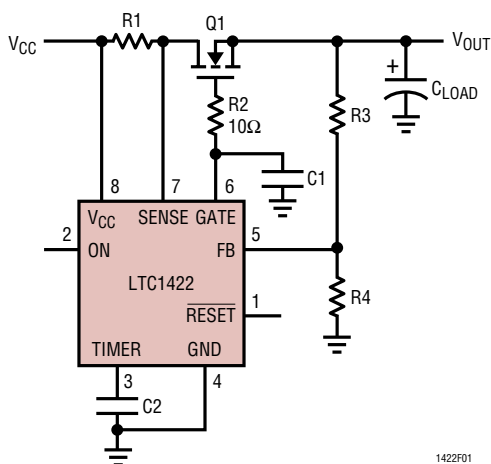


Figure 1. Supply Control Circuitry

When power is first applied to the chip, the gate of the N-channel (Pin 6) is pulled low. After the ON pin is held high for at least one timing cycle, the charge pump is turned on. The voltage at GATE begins to rise with a slope

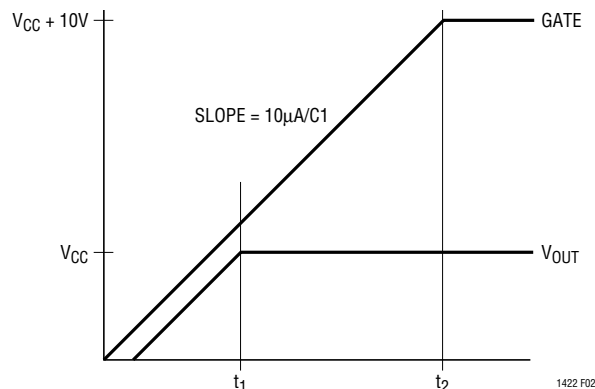


Figure 2. Supply Turn-On

equal to  $10\mu A/C1$  (Figure 2), where C1 is the external capacitor connected between the GATE pin and GND.

The ramp time for the supply is equal to:  $t = (V_{CC} \cdot C1) / 10\mu A$ . After the ON pin has been pulled low for more than  $40\mu s$ , the GATE is immediately pulled to GND.

### Voltage Monitor

The LTC1422 uses a 1.232V bandgap reference, precision voltage comparator and a resistive divider to monitor the output supply voltage (Figure 3).

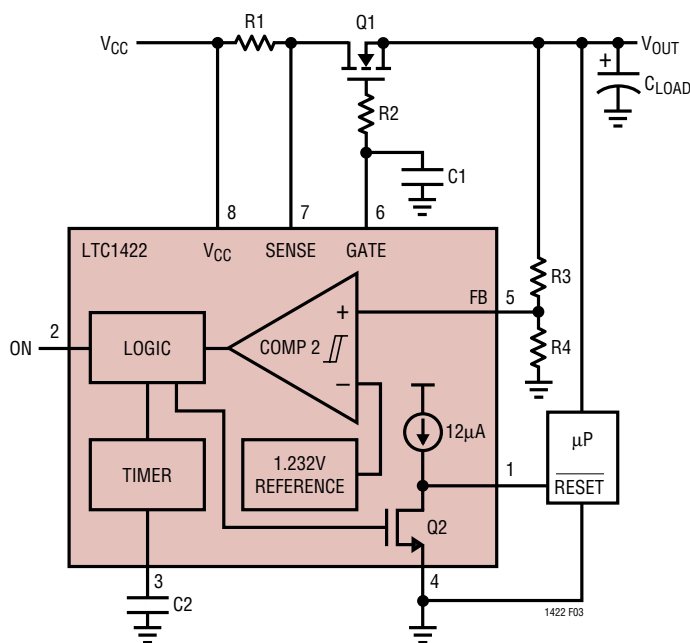


Figure 3. Supply Monitor Block Diagram

## APPLICATIONS INFORMATION

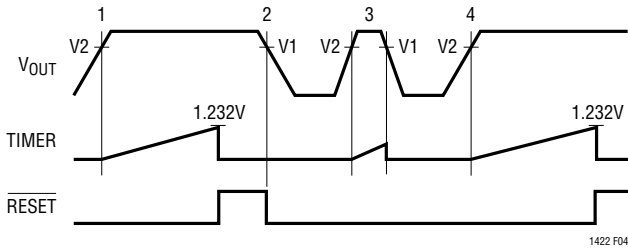


Figure 4. Supply Monitor Waveforms

When the voltage at the FB pin rises above its reset threshold (1.232V), the comparator COMP 2 output goes high, and a timing cycle starts (Figure 4, time points 1 and 4). After a complete timing cycle,  $\overline{\text{RESET}}$  is pulled high. The 12 $\mu\text{A}$  pull-up current source to  $V_{\text{CC}}$  on  $\overline{\text{RESET}}$  has a series diode so the pin can be pulled above  $V_{\text{CC}}$  by an external pull-up resistor without forcing current back into supply.

When the supply voltage at the FB pin drops below its reset threshold, the comparator COMP 2 output goes low. After passing through a glitch filter,  $\overline{\text{RESET}}$  is pulled low (time point 2). If the FB pin rises above the reset threshold for less than a timing cycle, the  $\overline{\text{RESET}}$  output will remain low (time point 3).

### Glitch Filter

The LTC1422 has a glitch filter to prevent  $\overline{\text{RESET}}$  from generating a system reset when there are transients on the FB pin. The filter is 20 $\mu\text{s}$  for large transients (greater than 150mV) and up to 80 $\mu\text{s}$  for small transients. The relationship between glitch filter time and the transient voltage is shown in Typical Performance curve: Glitch Filter Time vs Feedback Transient.

### Soft Reset

In some cases a system reset is desired without a power down. The ON pin can signal the  $\overline{\text{RESET}}$  pin to go low without turning off the external N-channel (a soft reset). This is accomplished by holding the ON pin low for only 15 $\mu\text{s}$  or less (Figure 5, time point 1). At about 30 $\mu\text{s}$  from the falling edge of the ON pin (time point 2) the  $\overline{\text{RESET}}$  pin goes low and stays low for one timing cycle.

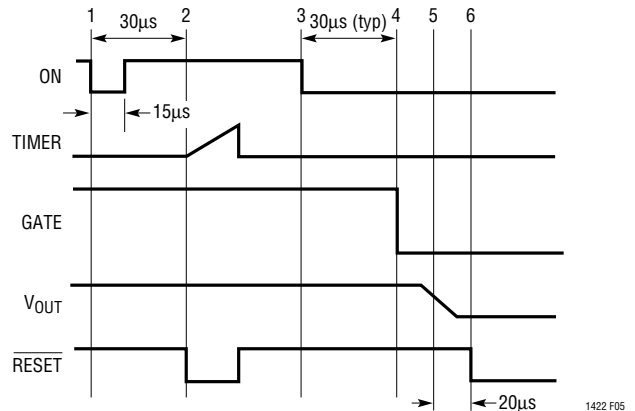


Figure 5. Soft Reset Waveforms

If the ON pin is held low for longer than 30 $\mu\text{s}$  (typ), the gate will turn off and the  $\overline{\text{RESET}}$  pin will eventually go low (time points 4, 5 and 6).

### Timer

The system timing for the LTC1422 is generated by the circuitry shown in Figure 6. The timer is used to set the turn-on delay after the ON pin goes high and the delay before the  $\overline{\text{RESET}}$  pin goes high after the output supply voltage is good as sensed by the FB pin.

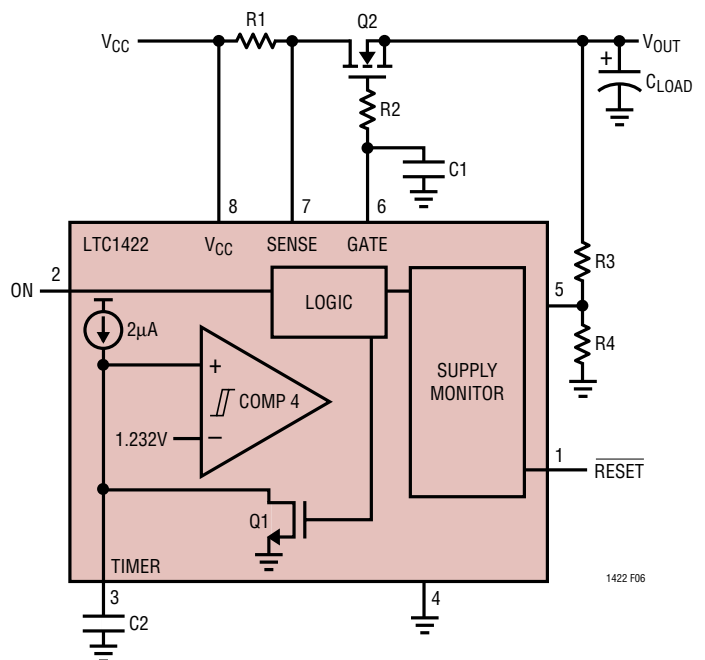


Figure 6. System Timing Block Diagram



## APPLICATIONS INFORMATION

When the timer is off, the internal N-channel Q1 shorts the TIMER pin to ground. When the timer is turned on, a  $2\mu\text{A}$  current from  $V_{\text{CC}}$  is connected to the TIMER pin and the voltage on the external capacitor C2 starts to ramp up with a slope given by:  $dV/dt = 2\mu\text{A}/C2$ . When the voltage reaches the trip point (1.232V), the timer will be reset by pulling the TIMER pin back to ground. The timer period is given by:  $(1.232\text{V} \cdot C2)/2\mu\text{A}$ . For a 200ms delay, use a  $0.33\mu\text{F}$  capacitor.

### Electronic Circuit Breaker

The LTC1422 features an electronic circuit breaker function that protects against short circuits or excessive currents on the supply. By placing a sense resistor between the supply input and SENSE pin, the circuit breaker will be tripped whenever the voltage across the sense resistor is greater than 50mV for more than  $10\mu\text{s}$ . When the circuit breaker trips, the GATE pin is immediately pulled to ground and the external N-channel is quickly turned off. When the ON pin is cycled off for greater than  $40\mu\text{s}$  and then on as shown in Figure 7, time point 7, the circuit breaker is reset and another timing cycle is started.

At the end of the timer cycle (time point 8), the charge pump will turn on again. If the circuit breaker feature is not required, the SENSE pin should be shorted to  $V_{\text{CC}}$ .

If more than  $10\mu\text{s}$  of response time is needed to reject supply noise, an external resistor and capacitor can be added to the sense circuit as shown in Figure 8.

### Connection Sense with ON Pin

The ON pin can be used to sense board connection to the backplane as shown in Figure 9.

Using staggered connection pins, ground mates first to discharge any static build up on the board, followed by the  $V_{\text{CC}}$  connection and all other pins. When  $V_{\text{CC}}$  makes connection, the bases of transistors Q3 and Q4 are pulled high turning them on and pulling the ON pin to ground. When the base connector pins of Q3 and Q4 finally mate to the backplane, the bases are shorted to ground. This turns off Q3 and Q4 and allows the ON pin to pull high and start a power-up cycle. The base connection pins of Q3 and Q4 should be located at opposite ends of the connector

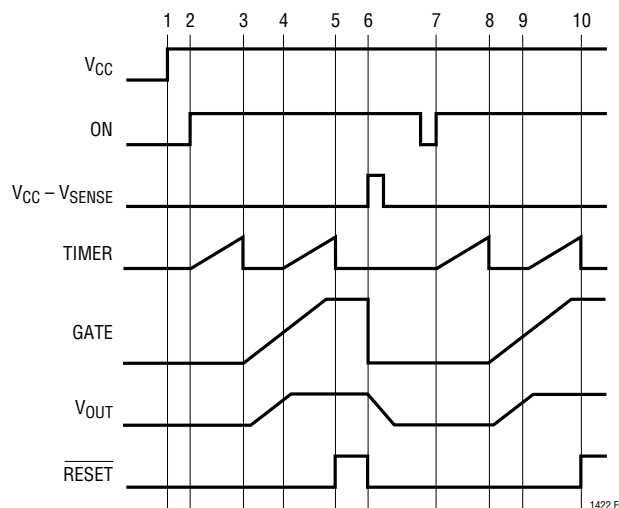


Figure 7. Current Fault Timing

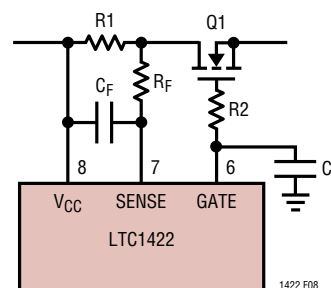


Figure 8. Extending the Short-Circuit Protection Delay

because most people will rock the board back and forth to get it seated properly.

A software-initiated power-down cycle can be started by momentarily turning on transistor Q2, which will pull the ON pin to ground. If the ON pin is held low for greater than  $40\mu\text{s}$ , the GATE pin is pulled to ground. If the low pulse on the ON pin is less than  $15\mu\text{s}$ , a soft reset is generated.

### Hot Swapping Two Supplies

With two external pass transistors, the LTC1422 can switch two supplies. In some cases, it is necessary to bring up the dominant supply first during power-up and ramp it down last during the power-down phase. The circuit in Figure 10 shows how to program two different delays for the pass transistors. The 5V supply is powered up first. R1

## APPLICATIONS INFORMATION

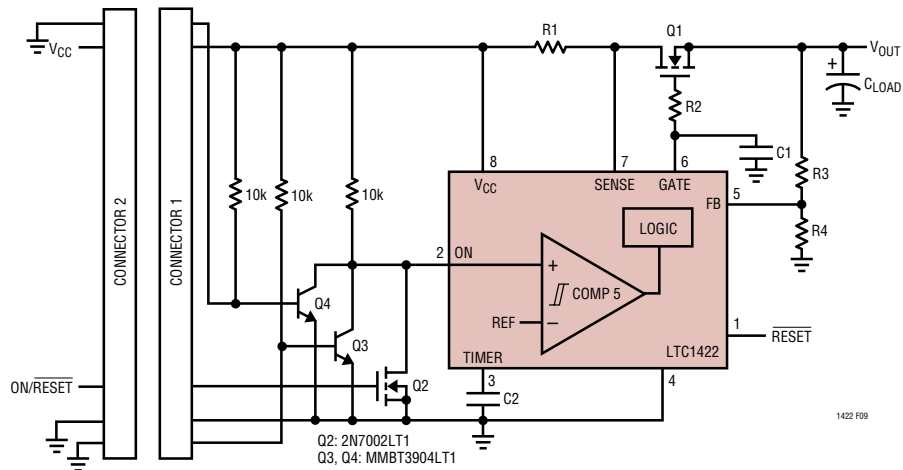


Figure 9. ON Pin Circuitry

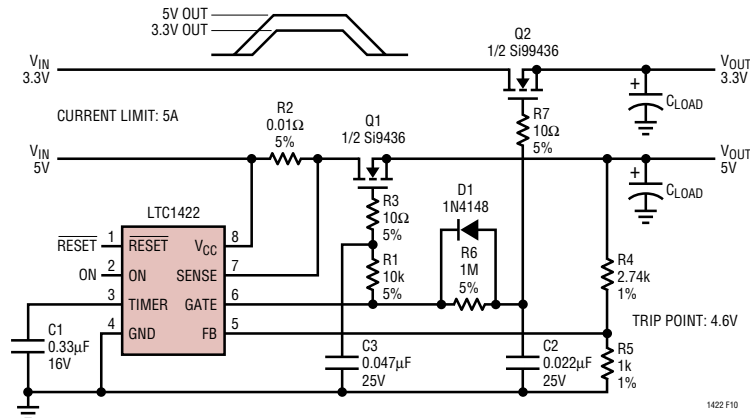


Figure 10. Switching 5V and 3.3V

and C3 are used to set the rise and fall delays on the 5V supply. Next, the 3.3V supply ramps up with a 20ms delay set by R6 and C2. On the falling edge, the 3.3V supply ramps down first because R6 is bypassed by the diode D1.

### Using the LTC1422 as a Linear Regulator

The LTC1422 can be used to Hot Swap the primary supply and generate a secondary low dropout regulated supply. Figure 11 shows how to switch a 5V supply and create a 3.3V supply using the reset comparator and one additional transistor. The FB pin is used to monitor the 3.3V output. When the voltage on the gate of Q2 increases, the 3.3V increases. At the 3.3V threshold, the reset comparator will trip. The RESET pin goes high which turns on Q3. This lowers the voltage on the gate of Q2. This feedback loop is compensated by the capacitor C1 and the resistors R6 and R7.

### Hot Swapping 48V DC/DC Module with Active Low On/Off Control Signal

Using a 7.5V Zener and a resistor, the LTC1422 can switch supplies much greater than the 12V  $V_{CC}$  pin rating. As shown in Figure 12, the switching FET Q1 is connected as a common source driver rather than the usual source follower used in previous applications. This allows the ground of the LTC1422 to sit at the negative terminal of the 48V input. The clamp circuit of R5 and D1 provides power to the LTC1422. The resistive divider R1 and R2 at the ON pin monitors the input supply. The switching FET Q1 is prevented from turning on until the input supply is at least 38V. Using the reset comparator to monitor the gate voltage allows the module to be turned on after the gate has reached a minimum level plus one timing cycle. A high voltage transistor Q2 is used to translate the RESET signal to the module On/Off input.



## APPLICATIONS INFORMATION

### Power N-Channel and Sense Resistor Selection

The decision of which external power N-Channel to use is dependent on its maximum current rating and the maximum allowed current times  $R_{DS(ON)}$  drop across the transistor. Table 1 lists some transistors that are available.

Table 2 lists some current sense resistors that can be used with the circuit breaker. Since this information is subject to change, please verify the part numbers with the manufacturer. Table 3 lists the web sites of several manufacturers.

**Table 1. N-Channel Selection Guide**

CURRENT LEVEL (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	MMDF3N02HD	Dual N-Channel SO-8 $R_{DS(ON)} = 0.1\Omega$	ON Semiconductor
2 to 5	MMSF5N02HD	Single N-Channel SO-8 $R_{DS(ON)} = 0.025\Omega$	ON Semiconductor
5 to 10	MTB50N06V	Single N-Channel DD Pak $R_{DS(ON)} = 0.028\Omega$	ON Semiconductor
10 to 20	MTB75N05HD	Single N-Channel DD Pak $R_{DS(ON)} = 0.0095\Omega$	ON Semiconductor

**Table 2. Sense Resistor Selection Guide**

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LR120601R050	0.05 $\Omega$ 0.25W 1% Resistor	IRC-TT
2A	LR120601R025	0.025 $\Omega$ 0.25W 1% Resistor	IRC-TT
2.5A	LR120601R020	0.02 $\Omega$ 0.25W 1% Resistor	IRC-TT
3.3A	WSL2512R015F	0.015 $\Omega$ 1W 1% Resistor	Vishay-Dale
5A	LR120601R010	0.01 $\Omega$ 0.25W 1% Resistor	IRC-TT
10A	WSR2R005F	0.005 $\Omega$ 2W 1% Resistor	Vishay-Dale

**Table 3. Manufacturers' Web Sites**

MANUFACTURER	WEB SITE
TEMIC Semiconductor	<a href="http://www.temic.com">www.temic.com</a>
International Rectifier	<a href="http://www.irf.com">www.irf.com</a>
ON Semiconductor	<a href="http://www.onsemiconductor.com">www.onsemiconductor.com</a>
Harris Semiconductor	<a href="http://www.semi.harris.com">www.semi.harris.com</a>
IRC-TT	<a href="http://www.irctt.com">www.irctt.com</a>
Vishay-Dale	<a href="http://www.vishay.com">www.vishay.com</a>

# APPLICATIONS INFORMATION

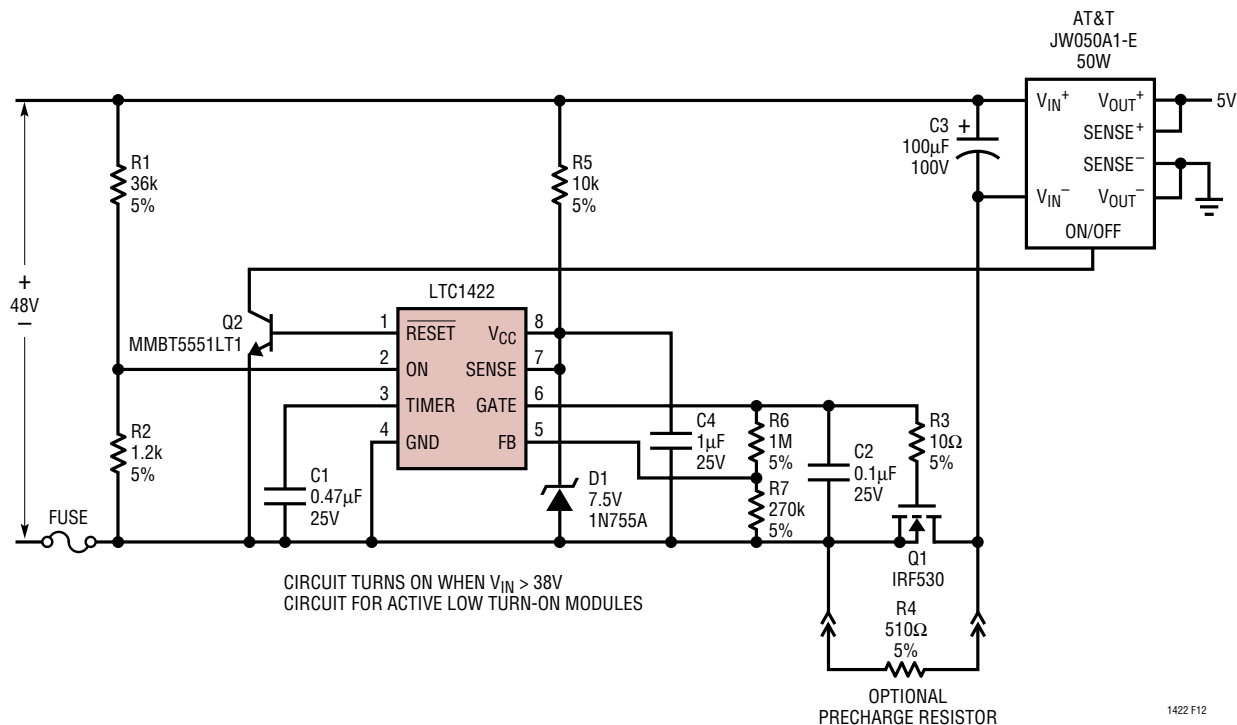


Figure 12. Switching 48V to an AT&T Module

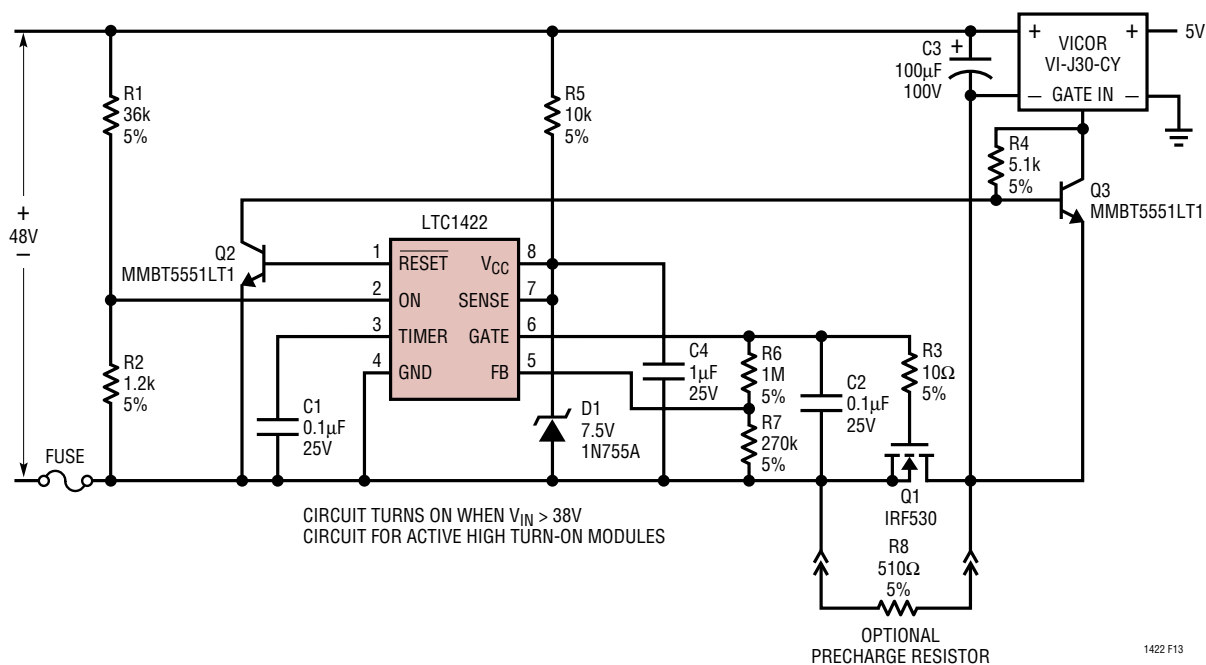


Figure 13. Switching 48V to a Vicor Module



# APPLICATIONS INFORMATION

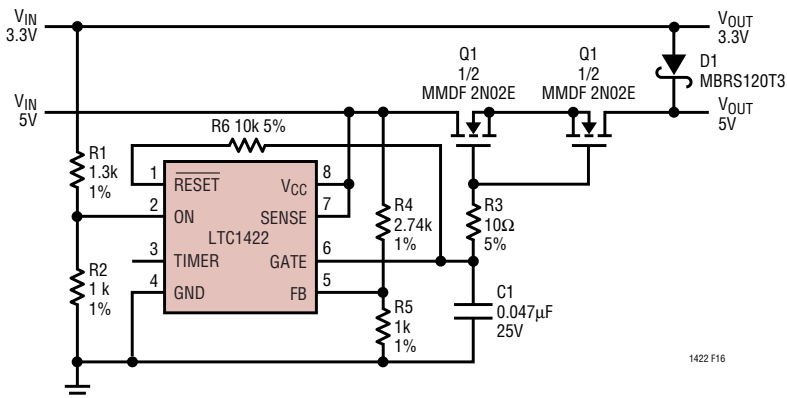
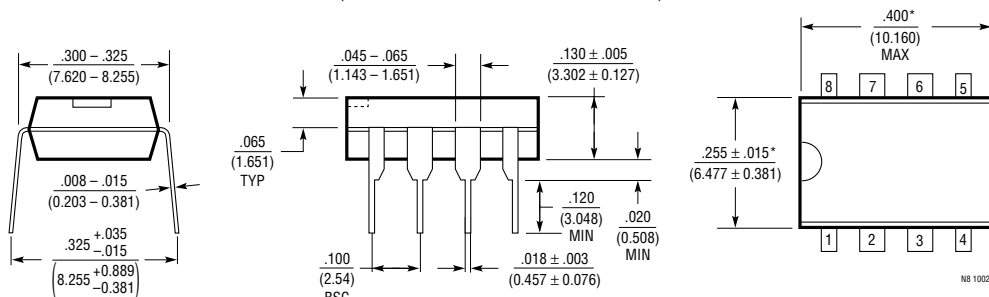


Figure 16. Power Supply Sequencer

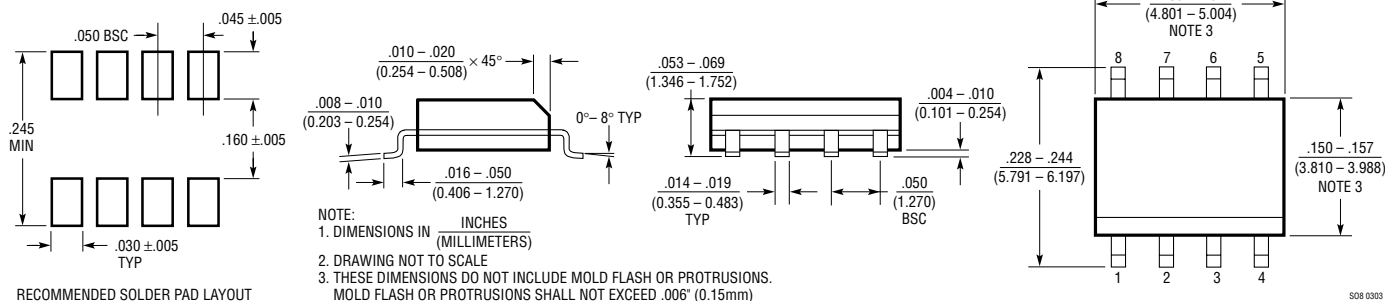
# PACKAGE DESCRIPTION

## N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



NOTE:  
1. DIMENSIONS ARE INCHES / MILLIMETERS  
\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

## S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:  
1. DIMENSIONS IN INCHES / (MILLIMETERS)  
2. DRAWING NOT TO SCALE  
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

## TYPICAL APPLICATION

### Current Sensing with 48V Applications

In the LTC1422, the SENSE pin threshold is 50mV below the  $V_{CC}$  pin. Typically, the current sense resistor is connected to the  $V_{CC}$  pin, but in 48V applications the sense resistor is connected to the negative terminal of the 48V supply. The circuit in Figure 17 translates the current in the sense resistor to a resistor connected to the LTC1422 SENSE pin.

The voltage drop across the current sense resistor  $R_{SENSE}$  is proportional to the load current  $I_{LOAD}$ . The voltage drop across  $R_{SENSE}$  is buffered by the op amp follower and is forced on  $R_{MIRROR}$ .

The mirror current can be described as:  $I_{MIRROR} = I_{LOAD} \cdot R_{SENSE} / R_{MIRROR}$ . The mirror current flows through the trip resistor  $R_{TRIP}$ . When the mirror current generates 50mV across  $R_{TRIP}$ , the LTC1422 will latch the GATE pin low ( $50mV = I_{MIRROR} \cdot R_{TRIP} = I_{LOAD} \cdot R_{SENSE} / R_{MIRROR} \cdot R_{TRIP}$ ). This example uses a 48V input but this translation circuit can be used anywhere the current sense resistor is not tied to  $V_{CC}$ .

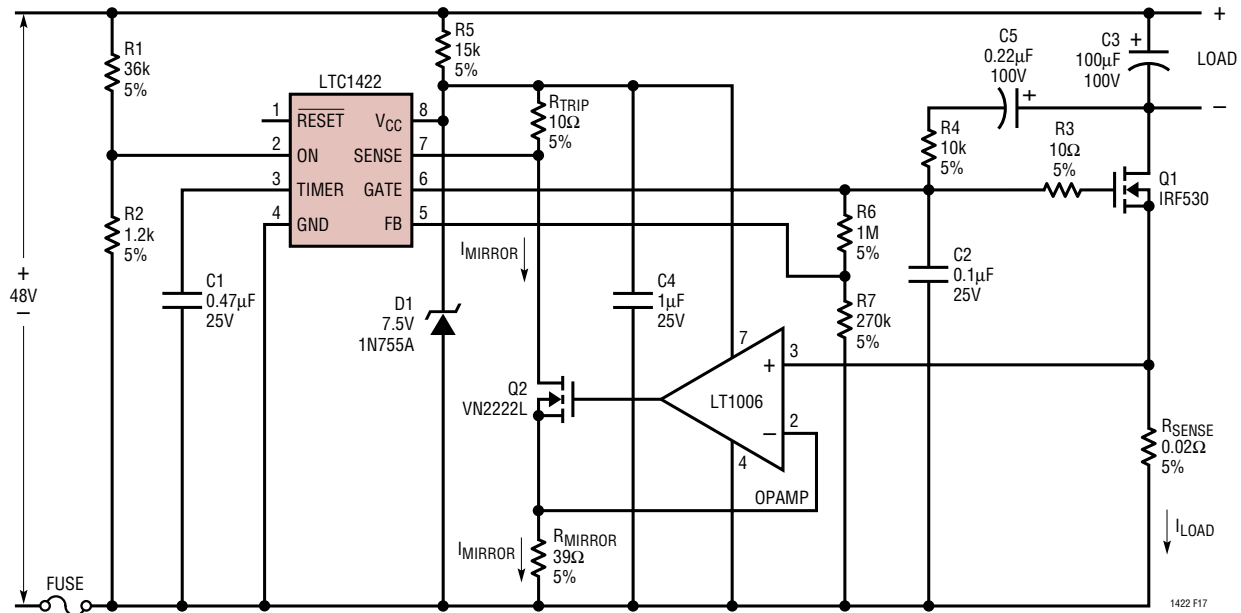


Figure 17. Switching 48V with Current Sensing

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Hot Swap Controller	24-Pin Multiple Supplies
LT1640L/LT1640H	Negative Voltage Hot Swap Controller in SO-8	Operates from -10V to -80V
LT1641	High Voltage Hot Swap Controller in SO-8	Operates from 9V to 80V
LT1642	Fault Protected Hot Swap Controller	Operates Up to 16.5V, Protected to 33V
LTC1643L/LTC1643H	PCI-Bus Hot Swap Controller	3.3V, 5V and ±12V in Narrow 16-Pin SSOP
LT1645	2-Channel Hot Swap Controller	Operates from 1.2V to 12V, Power Sequencing
LTC1647	Dual Hot Swap Controller in SO-8 or SSOP-16	Two ON Pins, Operates from 2.7V to 16.5V



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- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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