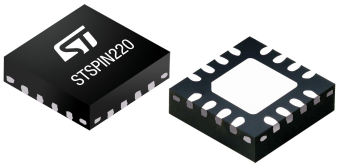
# STSPIN220

Datasheet

## Low voltage stepper motor driver




VFQFPN 3 X 3 X 1.0 (16-pin)

## Features

- Operating voltage: from 1.8 to 10 V
- Maximum output current: 1.3 $A_{rms}$
- $R_{DS(ON)}$ HS + LS = 0.4 Ω typ.
- Microstepping up to 1/256$^{th}$ of a step
- Current control with programmable off-time
- Full protection set
  - Non-dissipative overcurrent protection
  - Short-circuit protection
  - Thermal shutdown
- Energy saving and long battery life with standby consumption less than 80 nA

## Applications

Battery-powered stepper motor applications such as:

- Pop-up camera control for smartphones
- Point of sale (POS) devices
- Portable printers
- PC peripherals and accessories
- Robotics
- Toys
- Reflex cameras

| Product status link |
|---|
| STSPIN220 |

| Product summary | |
|---|---|
| **Order code** | STSPIN220 |
| **Package** | VFQFPN 3x3x1.0 16L |
| **Packing** | Tape & reel |

## Description

The STSPIN220 is a stepper motor driver which integrates, in a small VFQFPN 3 x 3 x 1.0 mm package, both control logic and a low $R_{DS\ (on)}$ power stage.

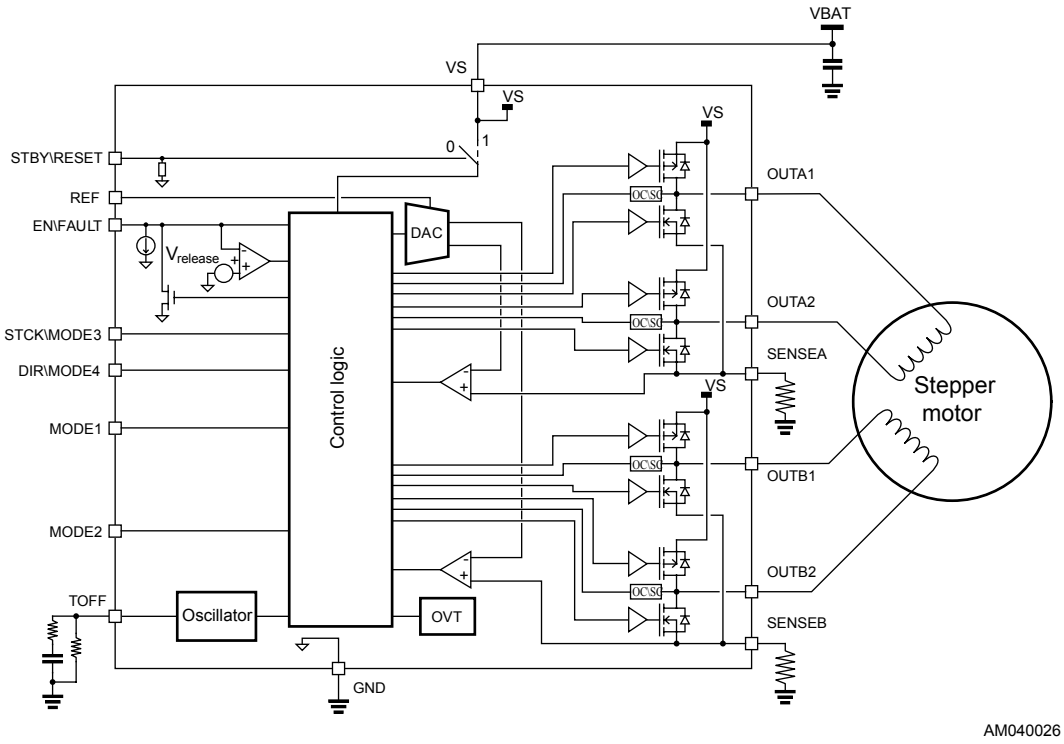
The integrated controller implements PWM current control with fixed OFF time and a microstepping resolution up to 1/256$^{th}$ of a step.

The device is designed to operate in battery-powered scenarios and can be forced into a zero-consumption state, allowing a significant increase in battery life.

The device offers a complete set of protection features including overcurrent, overtemperature and short-circuit protection.

# 1 Block diagram

Figure 2. **Block diagram**



# 2 Electrical data

## 2.1 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Test condition | Value | Unit |
|---|---|---|---|---|
| $V_S$ | Supply voltage | | -0.3 to 11 | V |
| $V_{IN}$ | Logic input voltage | | -0.3 to 5.5 | V |
| $V_{OUT}$ - $V_{SENSE}$ | Output-to-sense voltage drop | | Up to 12 | V |
| $V_S$ - $V_{OUT}$ | Supply-to-output voltage drop | | Up to 12 | V |
| $V_{SENSE}$ | Sense pin voltage | | -1 to 1 | V |
| $V_{REF}$ | Reference voltage input | | -0.3 to 1 | V |
| $I_{OUT,RMS}$ | Continuous power stage output current (each bridge) | | 1.3 | $A_{rms}$ |
| $T_{j,OP}$ | Operative junction temperature | | -40 to 150 | °C |
| $T_{j,STG}$ | Storage junction temperature | | -55 to 150 | °C |

## 2.2 Recommended operating conditions

**Table 2. Recommended operating conditions**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_S$ | Supply voltage | | 1.8 | | 10 | V |
| $V_{IN}$ | Logic input voltage | | 0 | | 5 | V |
| $V_{REF}$ | Reference voltage input | | 0.1 | | 0.5 | V |
| $t_{INw}$ | Logic inputs positive/negative pulse width | | 300 | | | ns |

## 2.3 Thermal data

**Table 3. Thermal data**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th\ (JA)}$ | Junction to ambient thermal resistance | Natural convection, according to JESD51-2a (1) | 57.1 | °C/W |
| $R_{thJCtop}$ | Junction to case thermal resistance (top side) | Simulation with cold plate on package top | 67.3 | °C/W |
| $R_{thJCbot}$ | Junction to case thermal resistance (bottom side) | Simulation with cold plate on exposed pad | 9.1 | °C/W |
| $R_{thJB}$ | Junction to board thermal resistance | According to JESD51-8(1) | 23.3 | °C/W |
| $\Psi_{JT}$ | Junction to top characterization | According to JESD51-2a(1) | 3.3 | °C/W |
| $\Psi_{JB}$ | Junction to board characterization | According to JESD51-2a(1) | 22.6 | °C/W |

1. *Simulated on a 21.2x21.2 mm board, 2s2p 1 Oz copper and four 300 µm vias below exposed pad.*

## 2.4 ESD protection

Table 4. **ESD protection ratings**

| Symbol | Parameter | Test condition | Class | Value | Unit |
|---|---|---|---|---|---|
| HBM | Human body model | Conforming to ANSI/ESDA/JEDEC JS-001-2014 | H2 | 2 | kV |
| CDM | Charge device model | Conforming to ANSI/ESDA/JEDEC JS-002-2014 | C2a | 500 | V |

# 3 Electrical characteristics

Test conditions: $V_S$ = 5 V, $T_j$ = 25 °C unless otherwise specified.

**Table 5. Electrical characteristics**

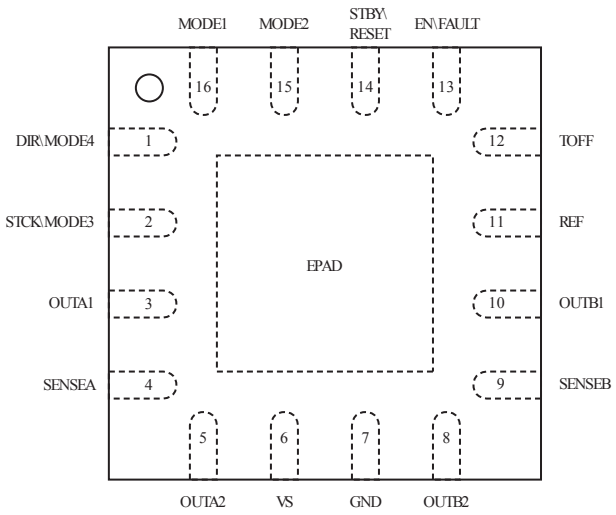
| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{Sth\ (ON)}$ | $V_S$ turn-on voltage | $V_S$ rising from 0 V | 1.45 | 1.65 | 1.79 | V |
| $V_{Sth\ (OFF)}$ | $V_S$ turn-off voltage | $V_S$ falling from 5 V | 1.3 | 1.45 | 1.65 | V |
| $V_{Sth\ (HYS)}$ | $V_S$ hysteresis voltage | | | 180 | | mV |
| $I_S$ | $V_S$ supply current | No commutations<br>EN = '0'<br>$R_{OFF}$ = 160 kΩ | | 960 | 1300 | µA |
| | | No commutations<br>EN = '1'<br>$R_{OFF}$ = 160 kΩ | | 1500 | 1950 | µA |
| $I_{S,STBY}$ | $V_S$ standby current | STBY = 0 V | | 10 | 80 | nA |
| $V_{STBYL}$ | Standby low logic level input voltage | | | | 0.9 | V |
| $V_{STBYH}$ | Standby high logic level input voltage | | 1.48 | | | V |
| **Power stage** | | | | | | |
| $R_{DS\ (ON)\ HS+LS}$ | Total ON resistance HS + LS | $V_S$ = 10 V,<br>$I_{OUT}$ = 1.3 A | | 0.4 | 0.65 | Ω |
| | | $V_S$ = 10 V,<br>$I_{OUT}$ = 1.3 A,<br>$T_j$ = 125 °C (1) | | 0.53 | 0.87 | |
| | | $V_S$ = 3 V,<br>$I_{OUT}$ = 0.4 A | | 0.53 | 0.8 | |
| $I_{DSS}$ | Leakage current | OUTx = $V_S$ | | | 1 | µA |
| | | OUTx = GND | - 1 | | | |
| $V_{DF}$ | Freewheeling diode forward voltage | $I_D$ = 1.3 A | | 0.9 | | V |
| $t_{rise}$ | Rise time | $V_S$ = 10 V;<br>unloaded outputs | | 10 | | ns |
| $t_{fall}$ | Fall time | $V_S$ = 10 V;<br>unloaded outputs | | 10 | | ns |
| $t_{DT}$ | Dead time | | | 50 | | ns |
| **Current control** | | | | | | |

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{SNS,OFFSET}$ | Sensing offset | $V_{REF}$ = 0.5 V;<br>Internal reference 20% $V_{REF}$ | -15 | | +15 | mV |
| $t_{OFF}$ | Total OFF time | $R_{OFF}$ = 10 kΩ | | 9 | | µs |
| | | $R_{OFF}$ = 160 kΩ | | 125 | | µs |
| $\Delta f_{OSC}$ | Internal oscillator precision ($f_{OSC}/f_{OSC,ID}$) | $R_{OFF}$ = 20 kΩ | -20% | | +20% | |
| $t_{OFF,jitter}$ | Total OFF time jittering | $R_{OFF}$ = 10 kΩ | | | 2% | |
| $t_{OFF,SLOW}$ | Slow decay time | | | 5/8 × $t_{OFF}$ | | µs |
| $t_{OFF,FAST}$ | Fast decay time | | | 3/8 × $t_{OFF}$ | | µs |
| **Logic IOs** | | | | | | |
| $V_{IH}$ | High logic level input voltage | | 1.6 | | | V |
| $V_{IL}$ | Low logic level input voltage | | | | 0.6 | V |
| $V_{RELEASE}$ | FAULT open drain release voltage | | | | 0.4 | V |
| $V_{OL}$ | EN Low logic level output voltage | $I_{EN}$ = 4 mA | | | 0.4 | V |
| $R_{STBY}$ | STBY pull-down resistance | | | 36 | | kΩ |
| $I_{PDEN}$ | EN pull-down current | | | 10.5 | | µA |
| $t_{ENd}$ | EN input propagation delay | From EN falling edge to OUT high impedance | | 55 | | ns |
| $t_{MODEho}$ | MODEx input hold time | From STBY edge, see Figure 6 | 100 | | | µs |
| $t_{MODEsu}$ | MODEx input setup time | From STBY edge, see Figure 6 | 1 | | | µs |
| $t_{DIRh}$ | DIR input hold time | From STCK rising edge, see Figure 5 | 100 | | | ns |
| $t_{DIRsu}$ | DIR input setup time | From STCK rising edge, see Figure 5 | 100 | | | ns |
| $t_{STCKH}$ | STCK high time | See Figure 5 | 100 | | | ns |
| $t_{STCKL}$ | STCK low time | See Figure 5 | 100 | | | ns |
| $f_{STCK}$ | STCK inputs frequency | See Figure 5 | | | 1 | MHz |
| **Protections** | | | | | | |
| $T_{jSD}$ | Thermal shutdown threshold | | | 160 | | °C |
| $T_{jSD,Hyst}$ | Thermal shutdown hysteresis | | | 40 | | °C |
| $I_{OC}$ | Overcurrent threshold | See Figure 15. Power stage resistance versus temperature | | 2 | | A |

1. *Based on characterization data on a limited number of samples, not tested during production.*

# 4 Pin description

Figure 3. **Pin connection (top view)**




**Note:** The exposed pad must be connected to ground.

Table 6. **Pin description**

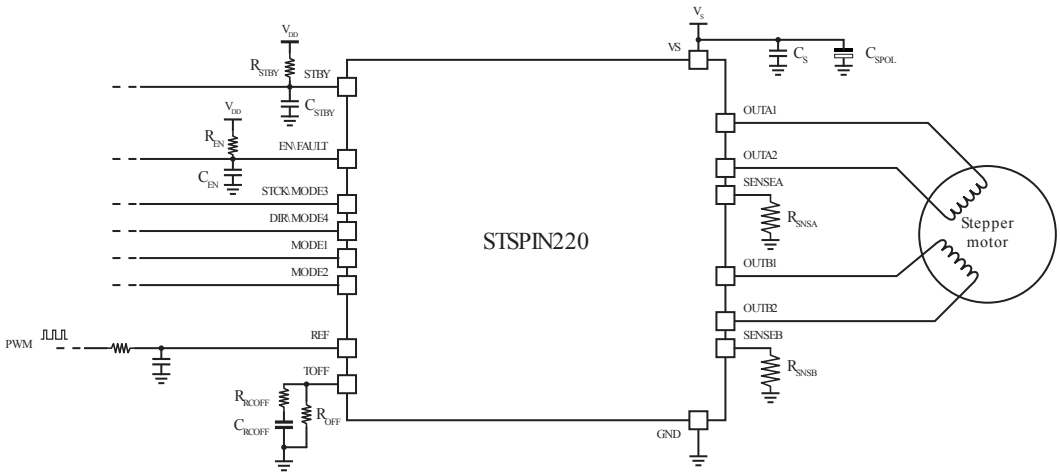
| N. | Name | Type | Function |
|---|---|---|---|
| 1 | DIR\MODE4 | Logic input | Direction input, Step mode selection input 4. |
| 2 | STCK\MODE3 | Logic input | Step clock input, Step mode selection input 3. |
| 3 | OUTA1 | Power output | Power bridge output side A1. |
| 4 | SENSEA | Power output | Sense output of the bridge A. |
| 5 | OUTA2 | Power output | Power bridge output side A2. |
| 6 | VS | Supply | Device supply voltage. |
| 7, EPAD | GND | Ground | Device ground. |
| 8 | OUTB2 | Power output | Power bridge output side B2. |
| 9 | SENSEB | Power output | Sense output of the bridge B. |
| 10 | OUTB1 | Power output | Power bridge output side B1. |
| 11 | REF | Analog input | Reference voltage for the PWM current control circuitry. |
| 12 | TOFF | Analog input | Internal oscillator frequency adjustment. |
| 13 | EN\FAULT | Logic input\Open drain output | This is the power stage enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs. |
| 14 | STBY\RESET | Logic input | When forced low, the device is forced into low consumption mode. |
| 15 | MODE2 | Logic input | Step mode selection input 2. |
| 16 | MODE1 | Logic input | Step mode selection input 1. |

# 5 Typical application

**Table 7. Typical application values**

| Name | Value |
|---|---|
| $C_S$ | 2.2 µF / 16V |
| $C_{SPOL}$ | 22 µF / 16V |
| $R_{SNSA}$, $R_{SNSB}$ | 330 mΩ / 1W |
| $C_{EN}$ | 10 nF / 6.3V |
| $R_{EN}$ | 18 kΩ |
| $C_{STBY}$ | 1 nF / 6.3V |
| $R_{STBY}$ | 18 kΩ |
| $C_{OFF}$ | 22 nF |
| $R_{COFF}$ | 1 kΩ |
| $R_{OFF}$ | 47 kΩ ($t_{OFF} \cong$ 37 µs) |

**Figure 4. Typical application schematic**



# 6 Functional description

The STSPIN220 is a stepper motor driver integrating a microstepping sequencer (up to 1/256$^{th}$ of a step), two PWM current controllers and a power stage composed of two fully-protected full-bridges.

## 6.1 Standby and power-up

The device provides a low consumption mode which is set forcing the STBY\RESET input below the $V_{STBYL}$ threshold.

When the device is in standby status, the power stage is disabled (outputs are in high impedance) and the supply to the integrated control circuitry is cut off. When the device exits the standby status, all of the control circuitry is reset to power-up condition.

At power-up, power-down and when leaving the standby condition, the EN/FAULT pin is forced low until the internal circuitry stabilize.

## 6.2 Microstepping sequencer

The value of the MODEx inputs is latched at power-up and when the device exits the STBY condition. After this, the input value is unimportant and the MODE3 and MODE4 inputs start operating as step-clock and direction input.

The only exception is the MODE1 = MODE2 = LOW condition; in this case the system is forced into full-step mode. The previous condition is restored as soon as the MODE1 and MODE2 inputs switch to a different combination.

An example of mode selection is shown in Figure 5. STCK and DIR timing.

At each STCK rising edge, the sequencer of the device is increased (DIR input high) or decreased (DIR input low) of a module selected through the MODEx inputs as listed in Table 8. Step mode selection through MODEx inputs.

The sequencer is a 10-bit counter that sets the reference value of the PWM current controller and the direction of the current for both of the H bridges.

**Table 8. Step mode selection through MODEx inputs**

| MODE3 (STCK) | MODE4 (DIR) | MODE1 | MODE2 | Step mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | **Full-step** |
| 0 | 0 | 0 | 1 | 1/32$^{nd}$ step |
| 0 | 0 | 1 | 0 | 1/128$^{th}$ step |
| 0 | 0 | 1 | 1 | 1/256$^{th}$ step |
| 0 | 1 | 0 | 0 | **Full-step - 1/32$^{nd}$ step** (1) |
| 0 | 1 | 0 | 1 | 1/4$^{th}$ step |
| 0 | 1 | 1 | 0 | 1/256$^{th}$ step |
| 0 | 1 | 1 | 1 | 1/64$^{th}$ step |
| 1 | 0 | 0 | 0 | **Full-step - 1/128$^{nd}$ step** (1) |
| 1 | 0 | 0 | 1 | 1/256$^{th}$ step |
| 1 | 0 | 1 | 0 | 1/2 step |
| 1 | 0 | 1 | 1 | 1/8$^{th}$ step |
| 1 | 1 | 0 | 0 | **Full-step - 1/256$^{th}$ step** (1) |
| 1 | 1 | 0 | 1 | 1/64$^{th}$ step |

| MODE3 (STCK) | MODE4 (DIR) | MODE1 | MODE2 | Step mode |
|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 1/8th step |
| 1 | 1 | 1 | 1 | 1/16th step |

1. *This driving mode is automatically bypassed by the MODE1 = MODE2 = 0 if it is kept after the device quit the standby condition.*

**Figure 5. STCK and DIR timing**

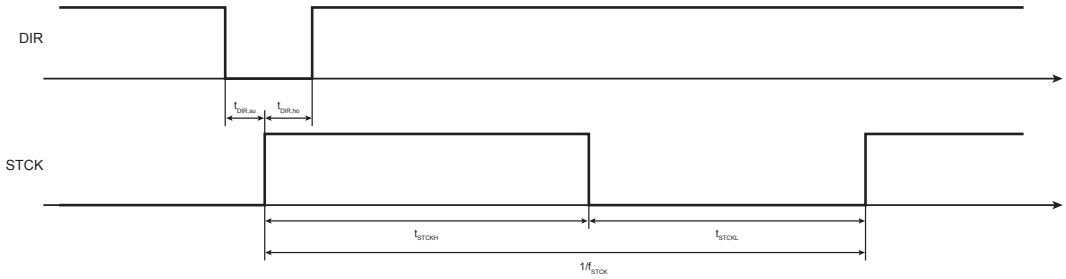
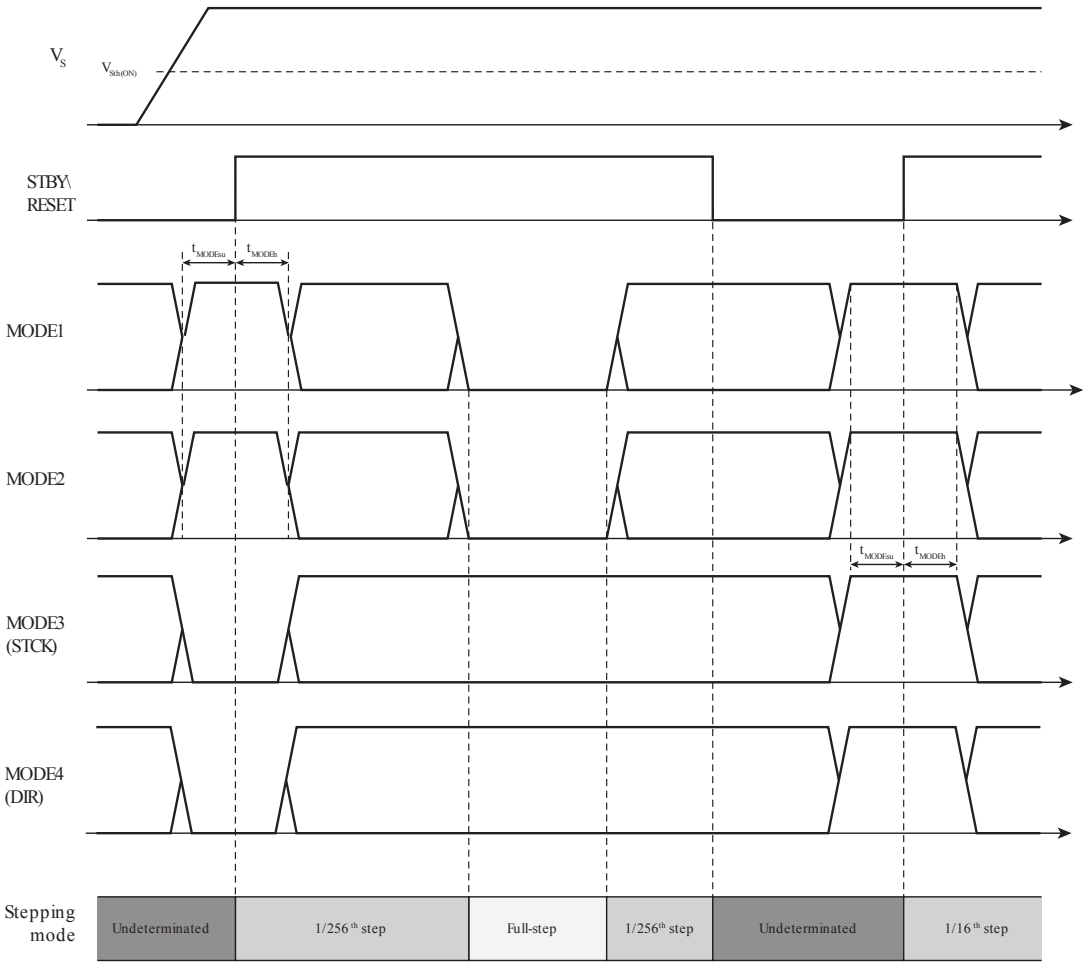



**Figure 6. Mode selection example**




When the full-step mode is set, the reference value of the PWM current controller and the direction of the current for both H bridges as listed in Table 8. Step mode selection through MODEx inputs.

**Table 9. Target reference and current direction according to sequencer value (full-step mode)**

| Sequencer value | | | | | | | | | | Phase A | | Phase B | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | Reference voltage | Current direction | Reference voltage | Current direction |
| 0 | 0 | X | X | X | X | X | X | X | X | 100% × $V_{REF}$ | A1 → A2 | 100% × $V_{REF}$ | B1 → B2 |
| 0 | 1 | X | X | X | X | X | X | X | X | 100% × $V_{REF}$ | A1 → A2 | 100% × $V_{REF}$ | B1 ← B2 |
| 1 | 0 | X | X | X | X | X | X | X | X | 100% × $V_{REF}$ | A1 ← A2 | 100% × $V_{REF}$ | B1 ← B2 |
| 1 | 1 | X | X | X | X | X | X | X | X | 100% × $V_{REF}$ | A1 ← A2 | 100% × $V_{REF}$ | B1 → B2 |

When the step mode is different from the full-step mode the values listed in Table 10. Target reference and current direction according to sequencer value (not full-step mode) are used.

**Table 10. Target reference and current direction according to sequencer value (not full-step mode)**

| Sequencer value | | | | | | | | | | Phase A | | Phase B | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | Reference voltage | Current direction | Reference voltage | Current direction |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Zero (power bridge disabled) | - | 100% × $V_{REF}$ | B1 → B2 |
| 0 | 0 | N | | | | | | | | Sin(N/256 × π/2) × $V_{REF}$ | A1 → A2 | Cos(N/256 × π/2) × $V_{REF}$ | B1 → B2 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 100% × $V_{REF}$ | A1 → A2 | Zero (power bridge disabled) | - |
| 0 | 1 | N | | | | | | | | Sin(π/2 + N/256 × π/2) × $V_{REF}$ | A1 → A2 | Cos(π/2 + N/256 × π/2) × $V_{REF}$ | B1 ← B2 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Zero (power bridge disabled) | - | 100% × $V_{REF}$ | B1 ← B2 |
| 1 | 0 | N | | | | | | | | Sin(N/256 × π/2) × $V_{REF}$ | A1 ← A2 | Cos(N/256 × π/2) × $V_{REF}$ | B1 ← B2 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 100% × $V_{REF}$ | A1 ← A2 | Zero (power bridge disabled) | - |
| 1 | 1 | N | | | | | | | | Sin(π/2 + N/256 × π/2) × $V_{REF}$ | A1 ← A2 | Cos(π/2 + N/256 × π/2) × $V_{REF}$ | B1 → B2 |

The following table shows the target reference and sequencer values for 1/2-, 1/4- and 1/8-step operation. Higher microstepping resolutions follow the same pattern. The reset state (home state) for all stepping mode is entered at power-up or when the device exits the standby status.

**Table 11. Example**

| 1/2 step | 1/4 step | 1/8 step | VREF phase A | VREF phase B | Sequencer value |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 0% | 100% | 0000000000 home state |
| | | 2 | 19.509% | 98.079% | 0000100000 |
| | 2 | 3 | 38.268% | 92.388% | 0001000000 |
| | | 4 | 55.557% | 83.147% | 0001100000 |

| 1/2 step | 1/4 step | 1/8 step | VREF phase A | VREF phase B | Sequencer value |
|---|---|---|---|---|---|
| 2 | 3 | 5 | 70.711% | 70.711% | 0010000000 |
| | | 6 | 83.147% | 55.557% | 0010100000 |
| | 4 | 7 | 92.388% | 19.509% | 0011100000 |
| | | 8 | 98.079% | 19.509% | 0011100000 |
| 3 | 5 | 9 | 100% | 0% | 0100000000 |
| | | 10 | 98.079% | -19.509% | 0100100000 |
| | 6 | 11 | 92.388% | -38.268% | 0101000000 |
| | | 12 | 83.147% | -55.557% | 0101100000 |
| 4 | 7 | 13 | 70.711% | -70.711% | 0110000000 |
| | | 14 | 55.557% | -83.147% | 0110100000 |
| | 8 | 15 | 38.268% | -92.388% | 0111000000 |
| | | 16 | 19.509% | -98.079% | 1000100000 |
| 5 | 9 | 17 | 0% | 100% | 1000000000 |
| | | 18 | -19.509% | -98.079% | 1000100000 |
| | 10 | 19 | -38.268% | -92.388% | 1001000000 |
| | | 20 | -55.557% | -83.147% | 1001100000 |
| 6 | 11 | 21 | -70.711% | -70.711% | 1010000000 |
| | | 22 | -83.147% | -55.557% | 1010100000 |
| | 12 | 23 | -92.388% | -38.268% | 1011000000 |
| | | 24 | -98.079% | -19.509% | 1011100000 |
| 7 | 13 | 25 | -100% | 0% | 1100000000 |
| | | 26 | -98.079% | 19.509% | 1100100000 |
| | 14 | 27 | -92.388% | 38.268% | 1101000000 |
| | | 28 | -83.147% | 55.557% | 1101100000 |
| 8 | 15 | 29 | -70.711% | 70.711% | 1110000000 |
| | | 30 | -55.557% | 83.147% | 1110100000 |
| | 16 | 31 | -38.268% | 92.388% | 1111000000 |
| | | 32 | -19.509% | 98.079% | 1111100000 |

*Note: The positive number means that the output current is flowing from OUTx1 to OUTx2, vice versa for a negative value.*

## 6.3 PWM current control

The device implements two independent PWM current controllers, one for each full bridge.

The voltage of the sense pins ($V_{SENSEA}$ and $V_{SENSEB}$) is compared to the respective internal reference generated based on the sequencer value (see Table 9. Target reference and current direction according to sequencer value (full-step mode) and Table 10. Target reference and current direction according to sequencer value (not full-step mode)).

When $V_{SENSEX} > V_{REFX}$, the integrated comparator is triggered, the OFF time counter is started and the decay sequence is performed.

The decay sequence starts turning on both the low sides of the full bridge. When $5/8^{ths}$ of the programmed OFF time ($t_{OFF,SLOW}$) has expired, the decay sequence performs a quasi-synchronous fast decay.

**Table 12. ON, slow decay and fast decay states**

| Current direction[1] | ON | Slow decay | Fast decay (quasi-synch) |
|---|---|---|---|
| Zero (power bridge disabled) | HSX1 = OFF<br>LSX1 = OFF<br>HSX2 = OFF<br>LSX2 = OFF | HSX1 = OFF<br>LSX1 = OFF<br>HSX2 = OFF<br>LSX2 = OFF | HSX1 = OFF<br>LSX1 = OFF<br>HSX2 = OFF<br>LSX2 = OFF |
| X1 → X2 | **HSX1 = ON**<br>LSX1 = OFF<br>HSX2 = OFF<br>**LSX2 = ON** | HSX1 = OFF<br>**LSX1 = ON**<br>HSX2 = OFF<br>**LSX2 = ON** | HSX1 = OFF<br>**LSX1 = ON**<br>HSX2 = OFF<br>LSX2 = OFF |
| X1 ← X2 | HSX1 = OFF<br>**LSX1 = ON**<br>**HSX2 = ON**<br>LSX2 = OFF | HSX1 = OFF<br>**LSX1 = ON**<br>HSX2 = OFF<br>**LSX2 = ON** | HSX1 = OFF<br>LSX1 = OFF<br>HSX2 = OFF<br>**LSX2 = ON** |

1. *The current direction is set according to Table 9. Table 9 and Table 9. Target reference and current direction according to sequencer value (full-step mode) Table 10. Target reference and current direction according to sequencer value (not full-step mode) .*

The reference voltage value, $V_{REF}$, must be selected according to the load current target value (peak value) and sense resistor value.

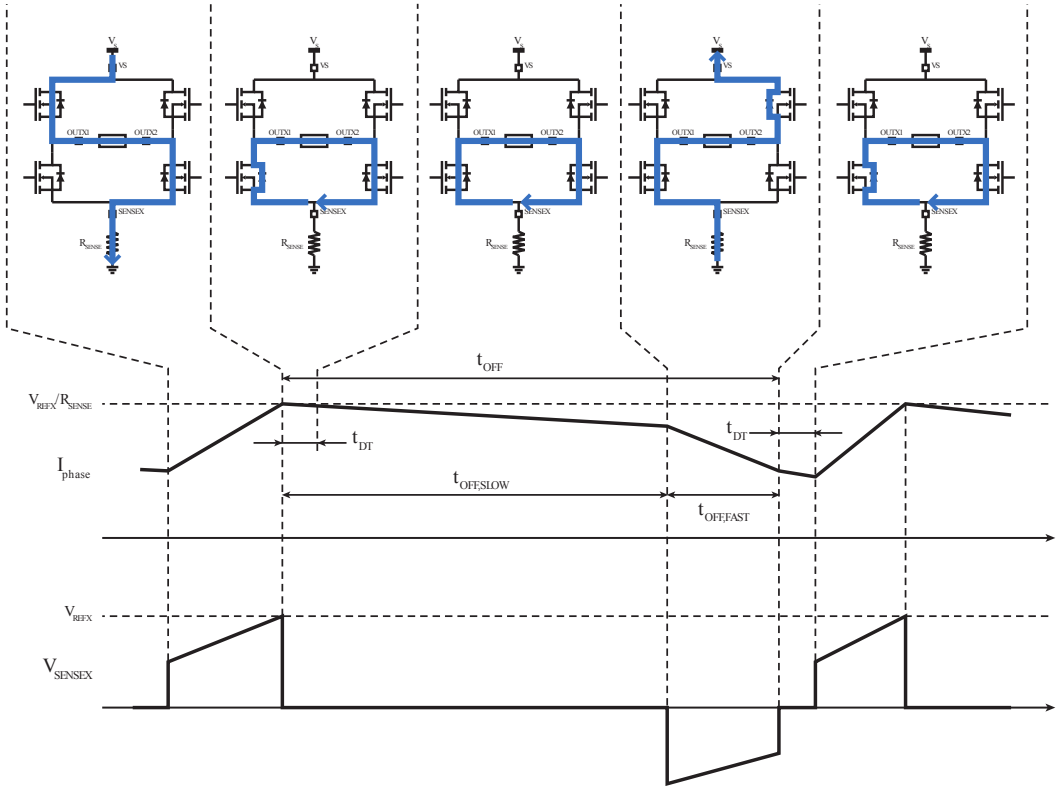
**Equation 1**

$$V_{REF} = R_{SNSx} \cdot I_{LOAD,peak}$$

In choosing the sense resistor value, two main issues must be taken into account:

- The sense resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during current recirculation. For this reason the resistance of this component should be kept low (using multiple resistors in parallel will help to obtain the required power rating with standard resistors).
- The lower the $R_{SNSx}$ value, the higher the peak current error due to noise on the $V_{REF}$ pin and the input offset of the current sense comparator. Values of $R_{SNSx}$ that are too low must be avoided.

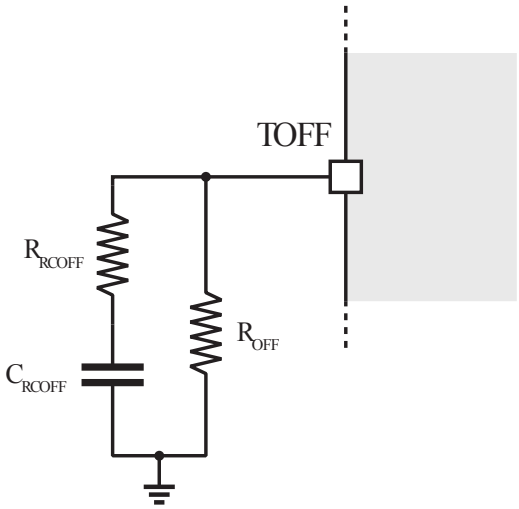
Figure 7. **PWM current control sequence**




### 6.3.1 OFF time adjustment

The total OFF time (slow decay + fast decay) is adjusted through an external resistor connected between the TOFF pin and ground, as shown in Figure 7. PWM current control sequence. A small RC series must be inserted in parallel with the regulator resistor in order to increase the stability of the regulation circuit according to Table 12. ON, slow decay and fast decay states indications.

Figure 8. **OFF time regulation circuit**

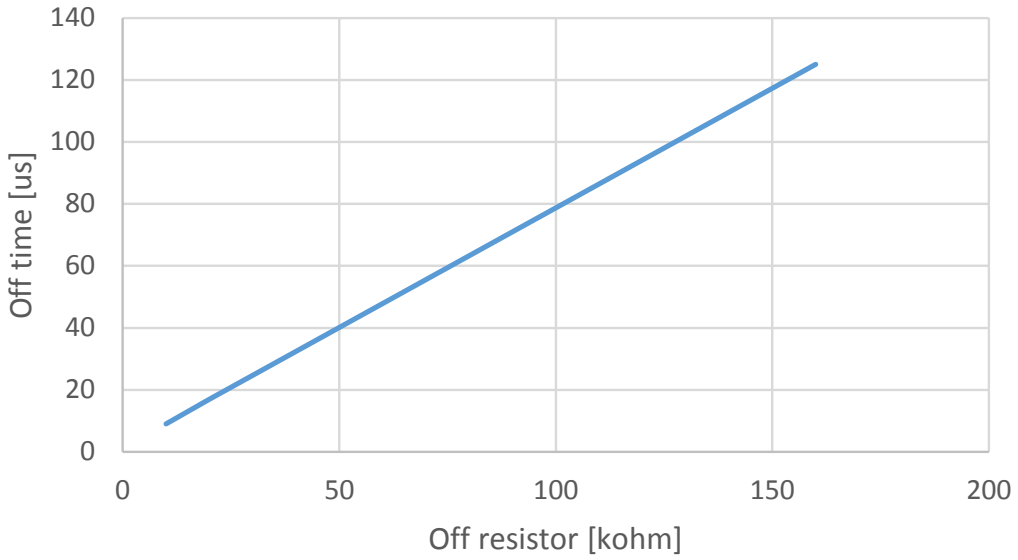


The relationship between the OFF time and the external resistor value is shown in Figure 8. OFF time regulation circuit. The value typically ranges from 10 µs to 150 µs.

**Table 13. Recommended $R_{RCOFF}$ and $C_{RCOFF}$ values according to $R_{OFF}$**

| $R_{OFF}$ | $R_{RCOFF}$ | $C_{RCOFF}$ |
|---|---|---|
| 10 kΩ ≤ $R_{OFF}$ < 82 kΩ | 1 kΩ | 22 nF |
| 82 kΩ ≤ $R_{OFF}$ ≤ 160 kΩ | 2.2 kΩ | 22 nF |

**Figure 9. OFF time vs. $R_{OFF}$ value**



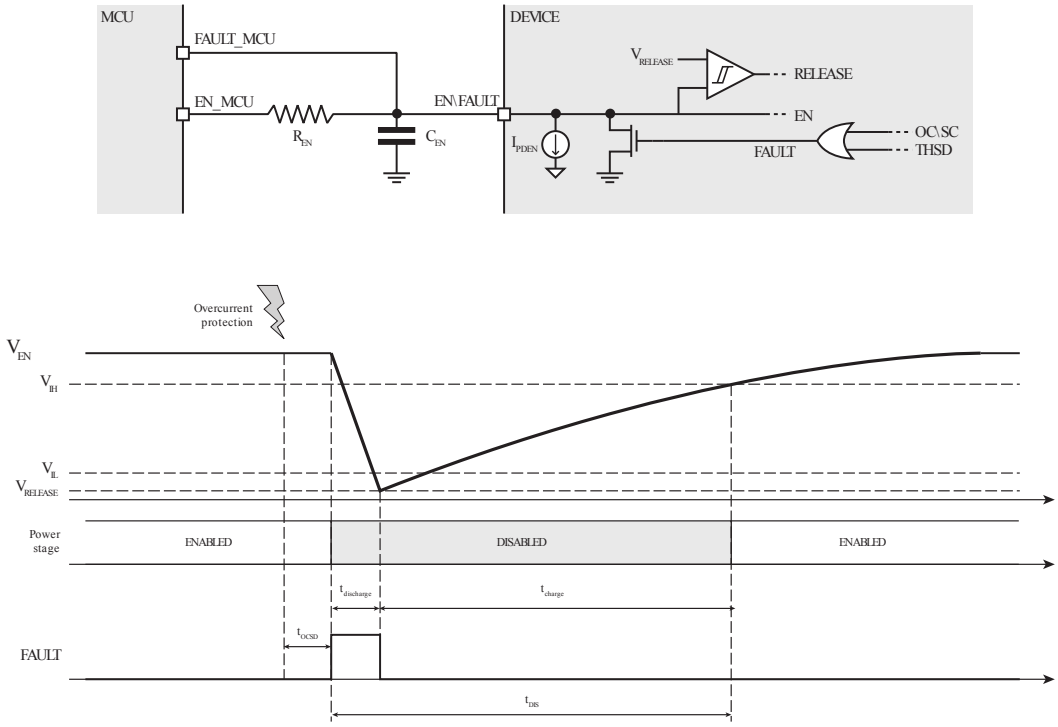

## 6.4 Overcurrent and short-circuit protection

The device embeds circuitry protecting each power output against the overload and short circuit conditions (short-circuit to ground, short-circuit to VS and short-circuit between outputs).

When the overcurrent or short-circuit protection is triggered, the power stage is disabled and the EN\FAULT input is forced low through the integrated open-drain MOSFET discharging the external $C_{EN}$ capacitor (refer to Figure 10. Overcurrent and short-circuit protection management).

The power stage is kept disabled and the open-drain MOSFET is kept ON until the EN\FAULT input falls below the $V_{RELEASE}$ threshold, then the $C_{EN}$ capacitor is charged through the external $R_{EN}$ resistor.

**Figure 10. Overcurrent and short-circuit protection management**




The total disable time after an overcurrent event can be set sizing properly the external network connected to the EN\FAULT pin (refer to Figure 10. Overcurrent and short-circuit protection management):

**Equation 2**

$$t_{DIS} = t_{discharge} + t_{charge}$$

But $t_{charge}$ is normally much higher than $t_{discharge}$, thus we can consider the following:

**Equation 3**

$$t_{DIS} \cong R_{EN} \cdot C_{EN} \cdot ln \frac{(V_{DD} - R_{EN} \cdot I_{PDEN}) - V_{RELEASE}}{(V_{DD} - R_{EN} \cdot I_{PDEN}) - V_{IH}}$$

where $V_{DD}$ is the pull-up voltage of the $R_{EN}$ resistor.

Figure 11. **Disable time versus $R_{EN}$ and $C_{EN}$ values ($V_{DD}$ = 3.3 V)**

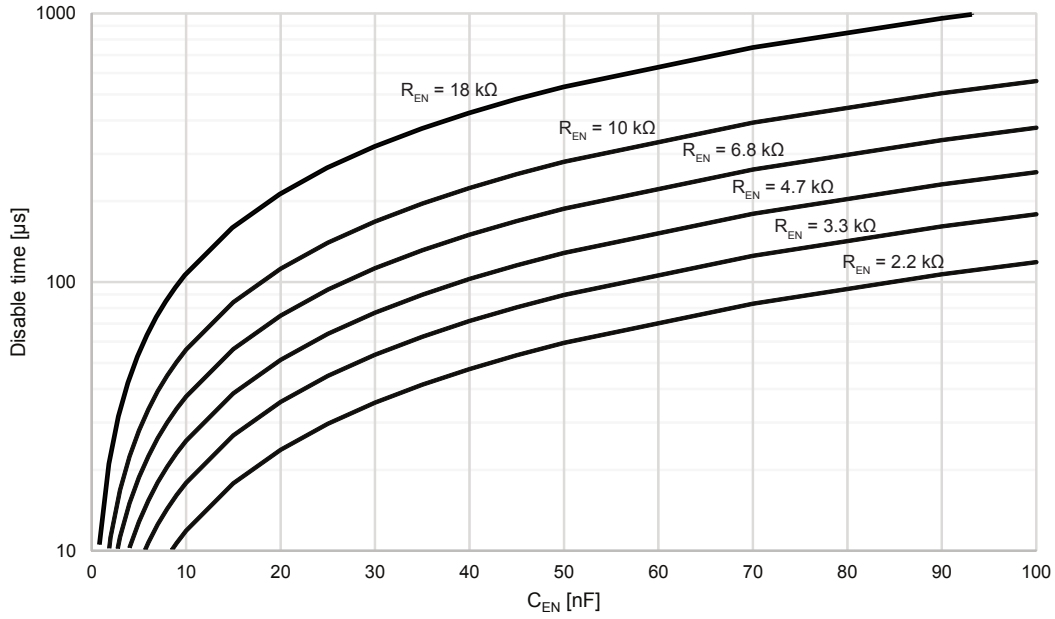
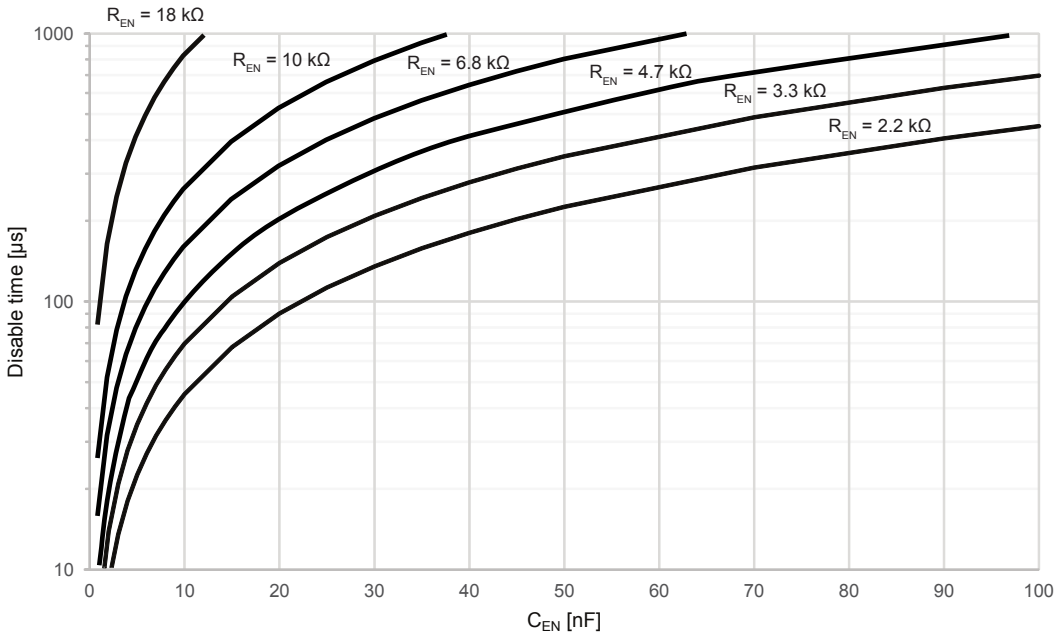



Figure 12. **Disable time versus $R_{EN}$ and $C_{EN}$ values ($V_{DD}$ = 1.8 V)**



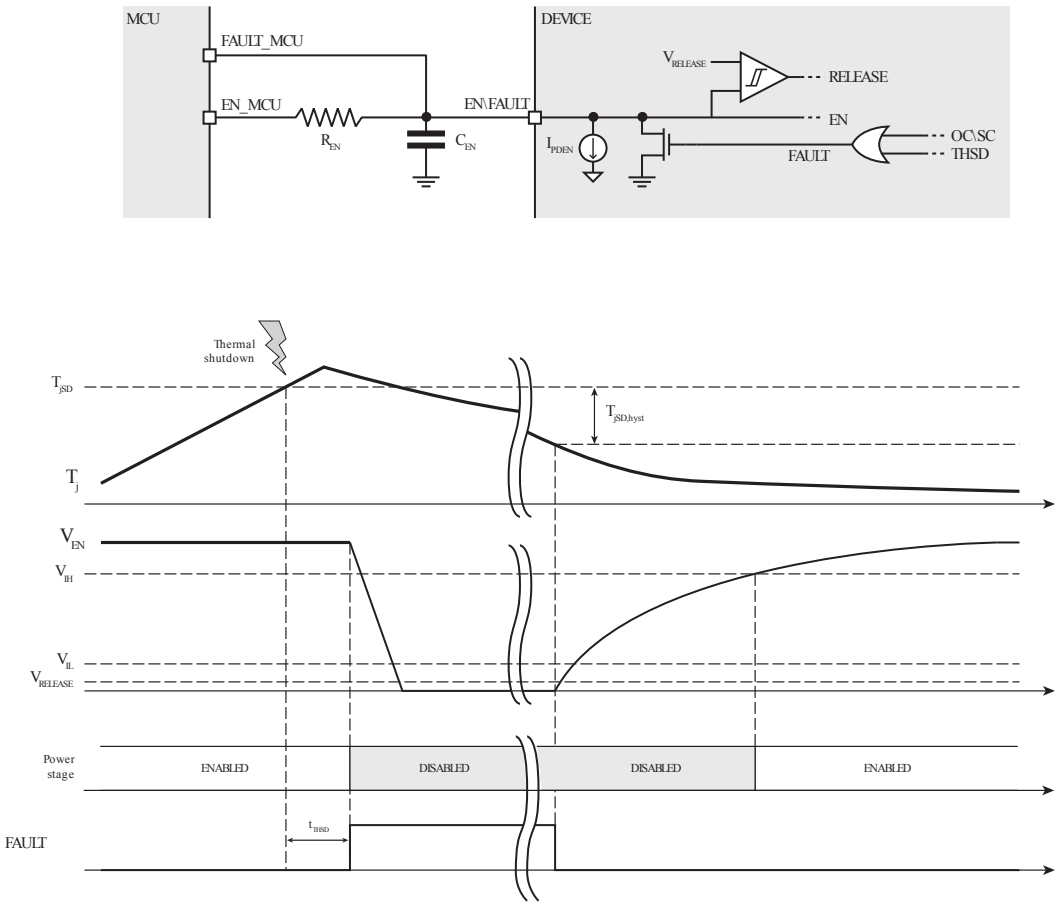

## 6.5 Thermal shutdown

The device embeds circuitry protecting it from the overtemperature conditions.

When the thermal shutdown temperature is reached, the power stage is disabled and the EN\FAULT input is forced low through the integrated open-drain MOSFET (refer to Figure 13. Thermal shutdown management).

The protection and the EN\FAULT output are released when the IC temperature returns below a safe operating value ($T_{jSD}$ - $T_{jSD,Hyst}$).

**Figure 13. Thermal shutdown management**



# 7 Graphs

Figure 14. **Power stage resistance versus supply voltage**

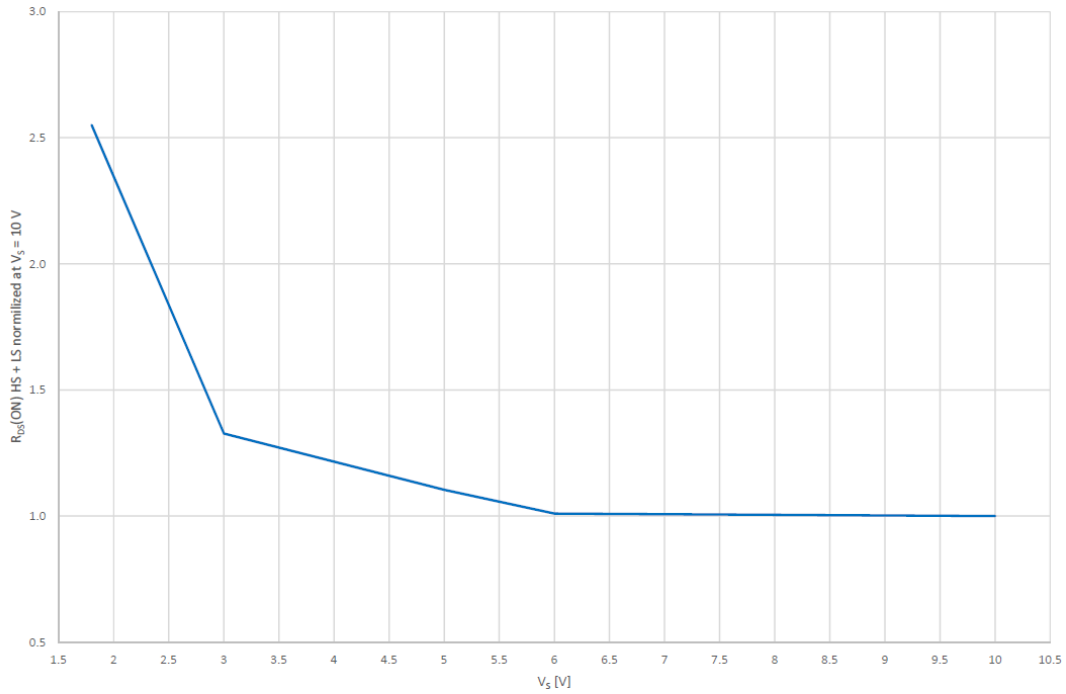



Figure 15. **Power stage resistance versus temperature**

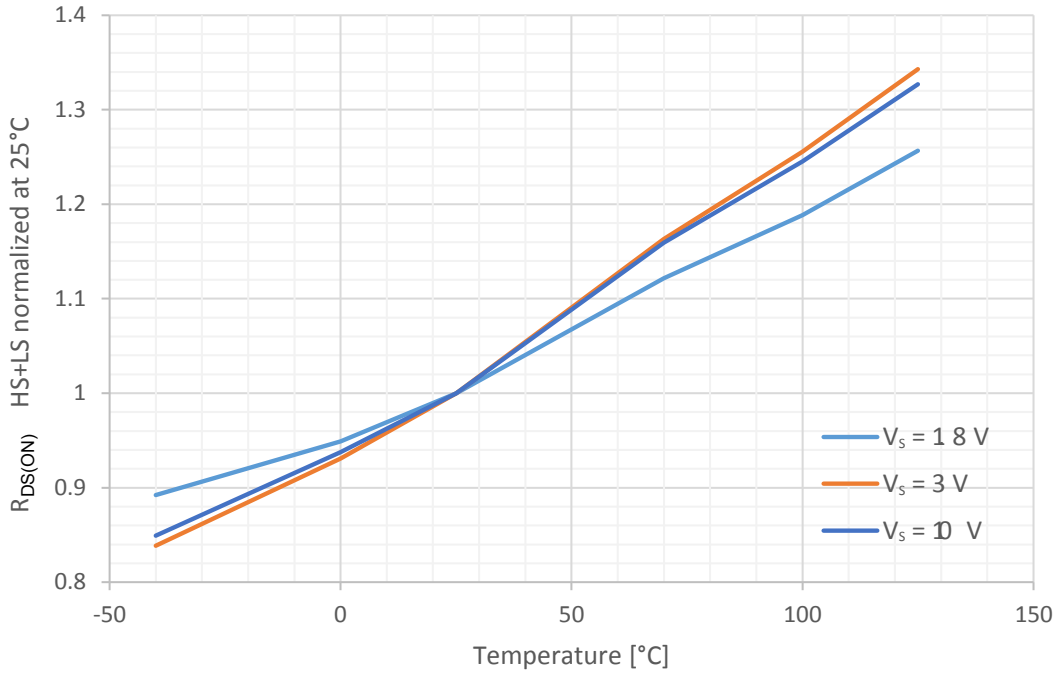
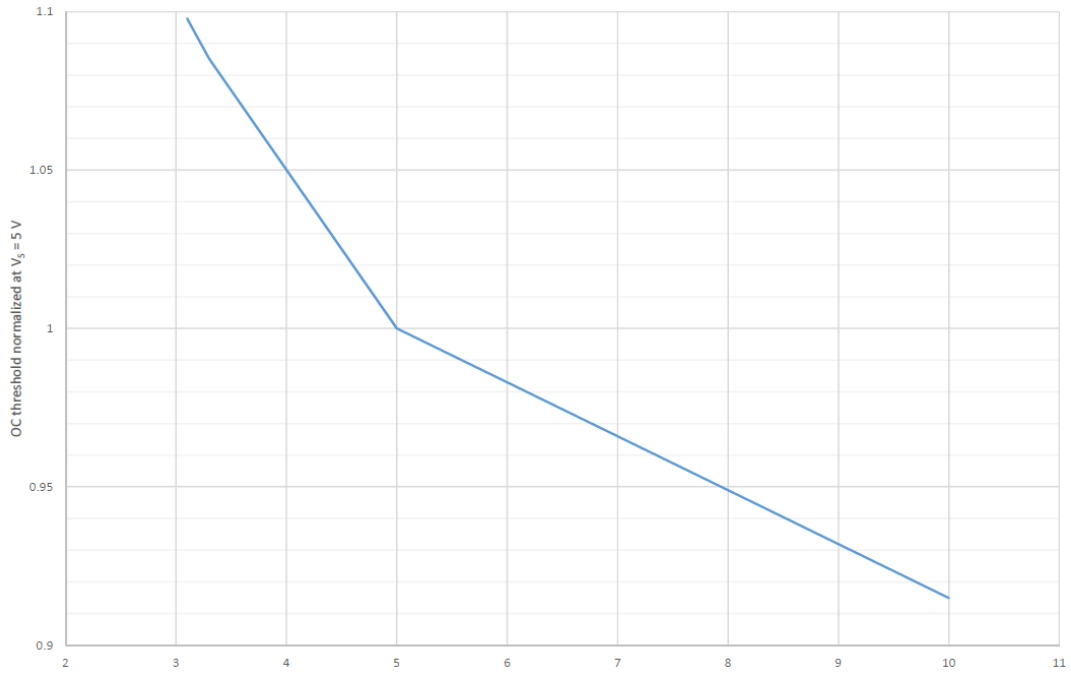


Figure 16. **Overcurrent threshold versus supply voltage**



# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 8.1 VFQFPN 3x3x1.0 16L package information

**Figure 17. VFQFPN 3x3x1.0 16L package outline**

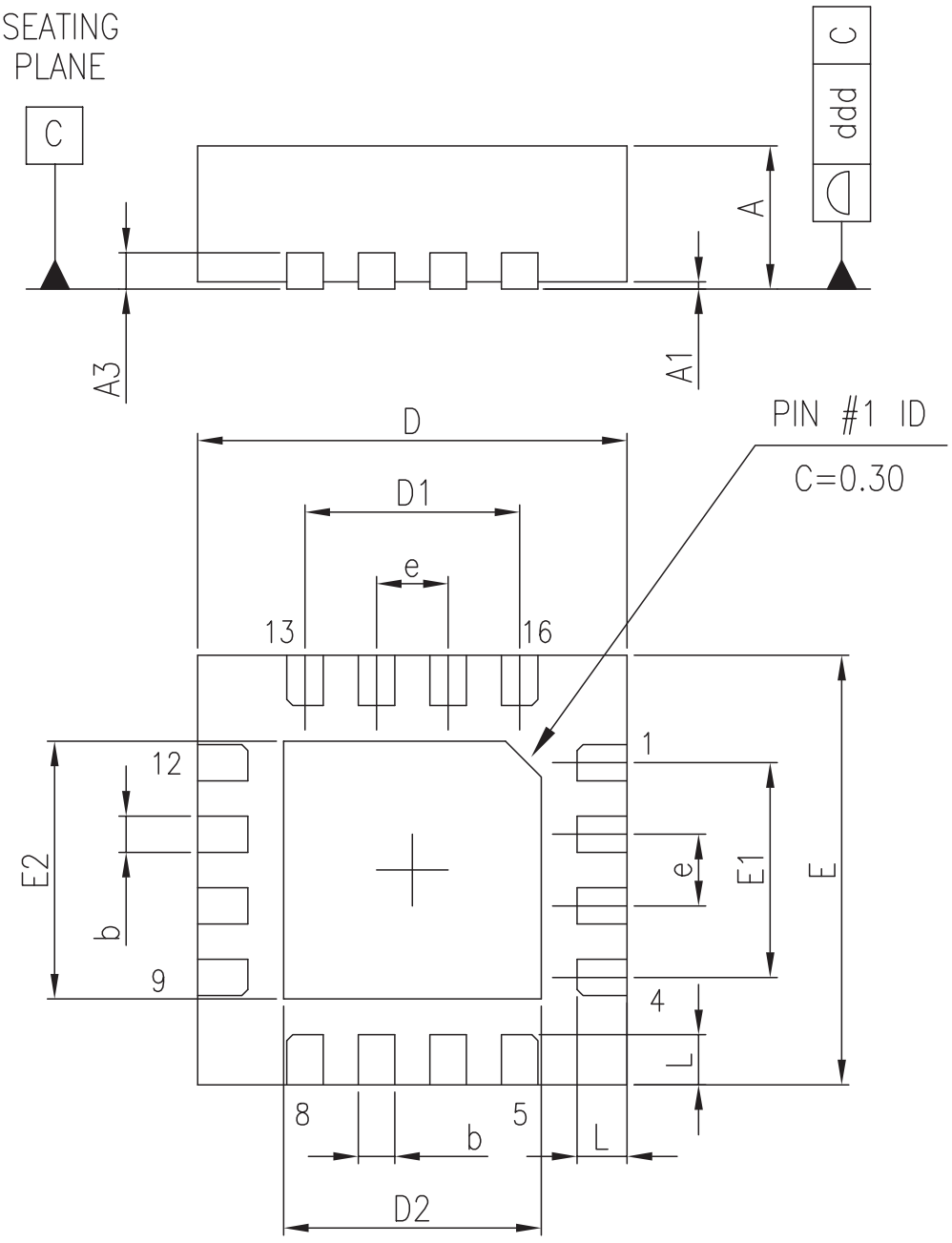
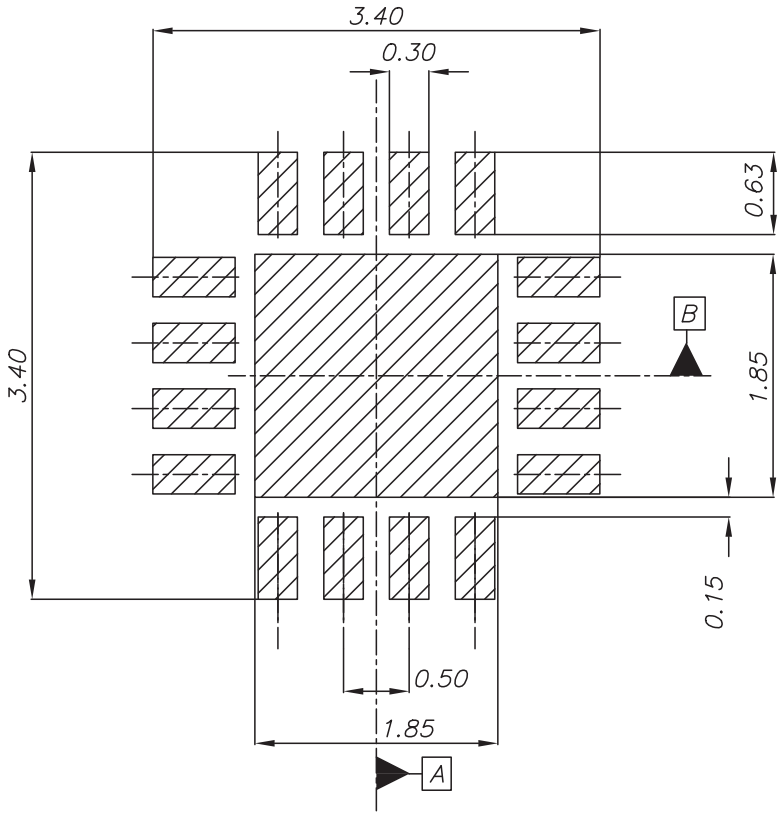


**Table 14. VFQFPN 3x3x1.0 16L package mechanical data**

| Symbol | Dimensions (mm) | | | |
|---|---|---|---|---|
| | Min. | Typ. | Max. | Notes |
| A | 0.80 | 0.90 | 1.00 | (1) (2) |
| A1 | | 0.02 | 0.05 | |
| A3 | | 0.20 | | |
| b | 0.18 | 0.25 | 0.30 | |
| D | 2.9 | 3.00 | 3.1 | |
| D1 | | 1.50 | | |
| D2 | 1.70 | 1.80 | 1.90 | |
| E | 2.9 | 3.00 | 3.1 | |
| E1 | | 1.50 | | |
| E2 | 1.70 | 1.80 | 1.90 | |
| e | 0.45 | 0.50 | 0.55 | |
| L | 0.30 | 0.40 | 0.50 | |
| ddd | | | 0.08 | |

1. *VFQFPN stands for "thermally-enhanced very thin fine pitch quad package, no lead". Very thin: 0.80 < A ≤ 1.00 mm / Fine pitch: e < 1.00 mm. The pin 1 identifier must be present on the top surface of the package as an indentation mark or other feature of the package body.*
2. *The chamfer of lead n 1,4,5,8,9,12,13,16 is 0.042 mm in both, x and y direction, with 45°.s*

**Figure 18. VFQFPN 3x3x1.0 16L recommended footprint**



# Revision history

Table 15. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 06-May-2016 | 1 | Initial release. |
| 30-Jun-2016 | 2 | - Updated document status to Datasheet - production data on page 1.<br>- Updated Table 1 (changed Max. value of VS from 12 to 11) and Table 7 (changed $t_{OFF}$ value from ≅47 µs to ≅37 µs). |
| 28-Nov-2016 | 3 | - Updated Figure 1 in Section 1 Block diagram (replaced by new figure).<br>- Updated Table 2 in Section 2.2 Recommended operating conditions (added $t_{INw}$ symbol).<br>- Updated Table 3 in Section 2.3 Thermal data(replaced by new table).<br>- Updated Table 8 in Section 6.2 Microstepping sequencer [removed "Sequencer module (binary)" column].<br>- Added Table 11 in Section 6.2 Microstepping sequencer.<br>- Updated Table 13 in (updated title).<br>- Updated Figure 13 in (replaced by new figure).<br>- Minor modifications throughout document. |
| 21-Mar-2019 | 4 | Updated Section 8.1 VFQFPN 3x3x1.0 16L package information |

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