

LTM4630A

Dual 18A or Single 36A μModule Regulator

DESCRIPTION

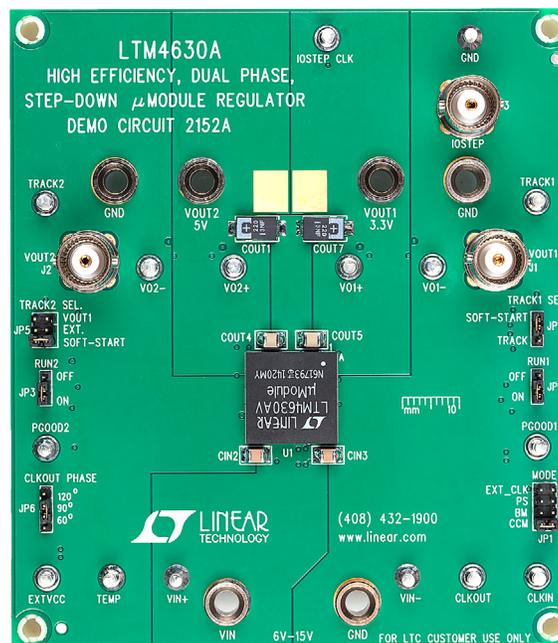
Demonstration circuit 2152A features the **LTM[®]4630AEV**, the high efficiency, high density, dual 18A, switch mode step-down power module regulator. The input voltage is from 6V to 15V. The output voltage is programmable from 0.6V to 5.3V. DC2152A can deliver up to 18A maximum in each channel. $\pm 3\%$ transient accuracy can be achieved with 25% load step. As explained in the data sheet, output current derating is necessary for certain V_{IN} , V_{OUT} , and thermal conditions. The board operates in continuous conduction mode in heavy load conditions. For high efficiency at low load currents, the MODE jumper (JP1) selects pulse-skipping mode for noise sensitive applications or Burst-Mode[®] in less noise sensitive applications. Two outputs can be connected in parallel for a single 36A output solution with optional jumper resistors. The board

allows the user to program how its output ramps up and down through the TRACK/SS pin. The output can be set up to either coincidentally or ratio-metrically track with another supply's output. Remote output voltage sensing is available for improved output voltage regulation at the load point. These features and the availability of the LTM4630AEV in a compact 16mm \times 16mm \times 4.41mm LGA package make it ideal for use in many high-density point-of-load regulation applications. The LTM4630A data sheet must be read in conjunction with this demo manual for working on or modifying the demo circuit DC2152A.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2152A>

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BOARD PHOTO



DEMO MANUAL DC2152A

PERFORMANCE SUMMARY Specifications are at $T_A = 25^\circ\text{C}$

| PARAMETER | CONDITIONS/NOTES | VALUE |
|---|--|---|
| Input Voltage Range | | 6V ~ 15V |
| Output Voltage V_{OUT1} | $V_{IN} = 6\sim 15\text{V}$, $I_{OUT1} = 0\sim 18\text{A}$, JP1: CCM | $3.3\text{V} \pm 1.5\%$ (3.2505V ~ 3.3495V) |
| Output Voltage V_{OUT2} | $V_{IN} = 6\sim 15\text{V}$, $I_{OUT2} = 0\sim 18\text{A}$, JP1: CCM | $5.0\text{V} \pm 1.5\%$ (4.925V ~ 5.075V) |
| Per-Channel Maximum Continuous Output Current | Derating is Necessary for Certain V_{IN} , V_{OUT} and Thermal Conditions, See Data Sheet for Detail | 18A |
| Default Operating Frequency | | 600kHz |
| Resistor programmable Frequency Range | | 250kHz – 780kHz |
| External Clock Sync. Frequency Range | | 400kHz – 780kHz |
| Efficiency of Channel 1 | $V_{IN} = 12\text{V}$, $V_{OUT1} = 3.3\text{V}$, $I_{OUT1} = 18\text{A}$, $f_{SW} = 600\text{kHz}$ | 93.4% See Figure 2 |
| Efficiency of Channel 2 | $V_{IN} = 12\text{V}$, $V_{OUT2} = 5.0\text{V}$, $I_{OUT2} = 18\text{A}$, $f_{SW} = 600\text{kHz}$ | 95.4% See Figure 3 |
| Load Transient of Channel 1 | $V_{IN} = 12\text{V}$, $V_{OUT1} = 3.3\text{V}$, $I_{STEP} = 9\sim 13.5\text{A}$ | See Figure 4 |
| Load Transient of Channel 2 | $V_{IN} = 12\text{V}$, $V_{OUT2} = 5.0\text{V}$, $I_{STEP} = 9\sim 13.5\text{A}$ | See Figure 5 |

QUICK START PROCEDURE

Demonstration circuit DC2152A is easy to set up to evaluate the performance of the LTM4630AEV. Please refer to Figure 1 for proper measurement setup and follow the procedure below:

- Place jumpers in the following positions for a typical application:

| JP1 | JP2 | JP3 | JP4 | JP5 | JP6 |
|------|------|------|-------------|-------------|--------------|
| MODE | RUN1 | RUN2 | TRACK1 SEL. | TRACK2 SEL. | CLKOUT PHASE |
| CCM | ON | ON | SOFT-START | SOFT-START | 90° |

- With power off, connect the input power supply, load and meters as shown in Figure 1. Preset the load to 0A and V_{IN} supply to 12V.
- Turn on the power supply at the input. The output voltage in channel 1 should be $3.3\text{V} \pm 1.5\%$ (3.2505V ~ 3.3495V) and the output voltage in channel 2 should be $5.0\text{V} \pm 1.5\%$ (4.925V ~ 5.075V).
- Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, output voltage ripple, efficiency and other parameters. Output ripple should be measured at J1 and J2 with BNC cables. 50 Ω termination should be set on the oscilloscope or BNC cables.

- (Optional) For optional load transient test, apply an adjustable pulse signal between “IOSTEP CLK” and “GND” test point. Pulse amplitude (3V~3.5V) sets the load step current amplitude. The output transient current can be monitored at the BNC connector J3 (15mV/A). The pulse signal should have very small duty cycle (< 10%) to limit the thermal stress on the transient load circuit. Switch the jumper resistors R34 or R35 (on the backside of boards) to apply load transient on channel 1 or channel 2 correspondingly.
- (Optional) LTM4630A can be synchronized to an external clock signal. Place the JP1 jumper on EXT_CLK and apply a clock signal (0~5V, square wave) on the “CLKIN” test point.
- (Optional) The outputs of LTM4630A can track another supply. The jumpers JP4 and JP5 allow choosing soft-start or output tracking. If tracking external voltage is selected, the corresponding test points, “TRACK1” and “TRACK2”, need to be connected to a valid voltage signal.
- (Optional) LTM4630A can be configured for a 2-phase single output at up to 36A on DC2152A. Install 0 Ω resistors on R14,R17,R28,R39 and remove R7,R19. Output voltage is set by R25 based on equation $V_{OUT} = 0.6\text{V}(1+60.4\text{k}/\text{R}25)$.

QUICK START PROCEDURE

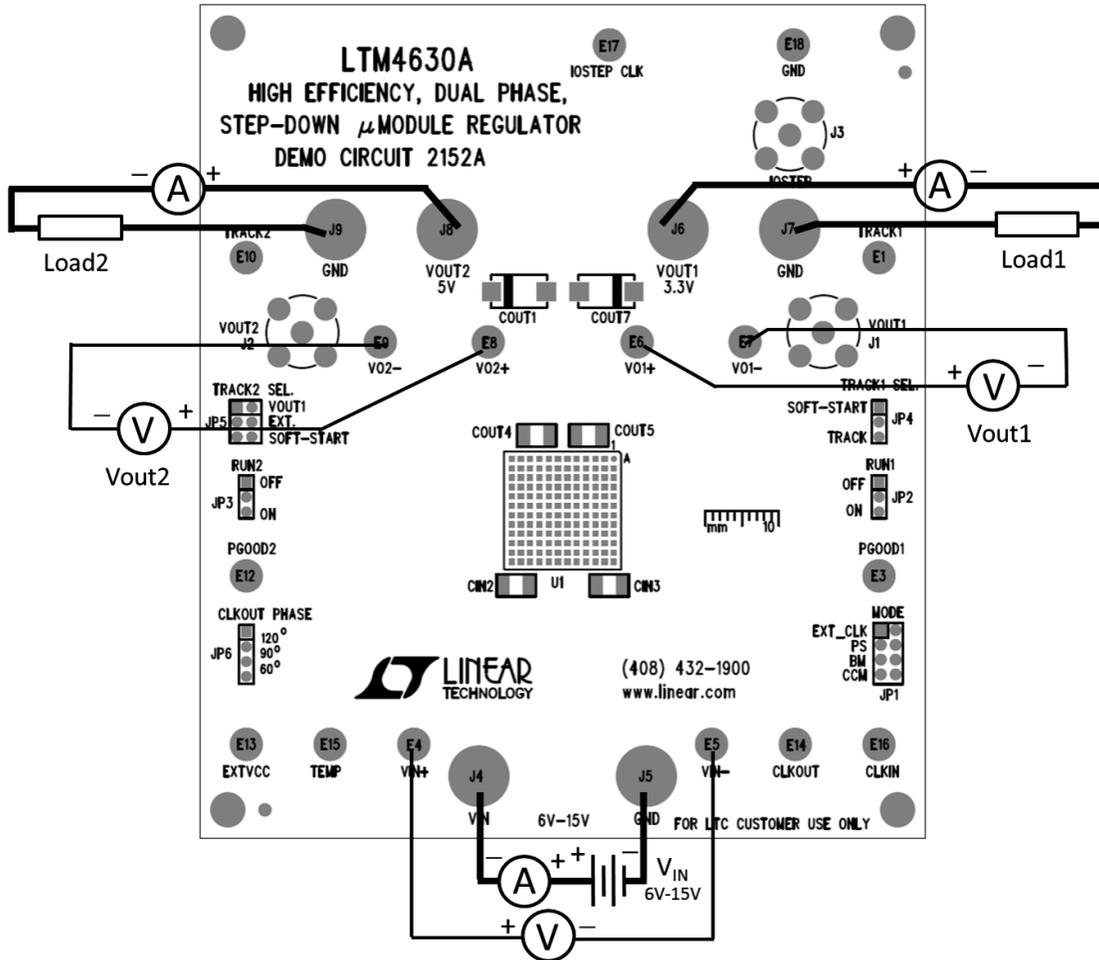


Figure 1. Test Setup of DC2152A

QUICK START PROCEDURE

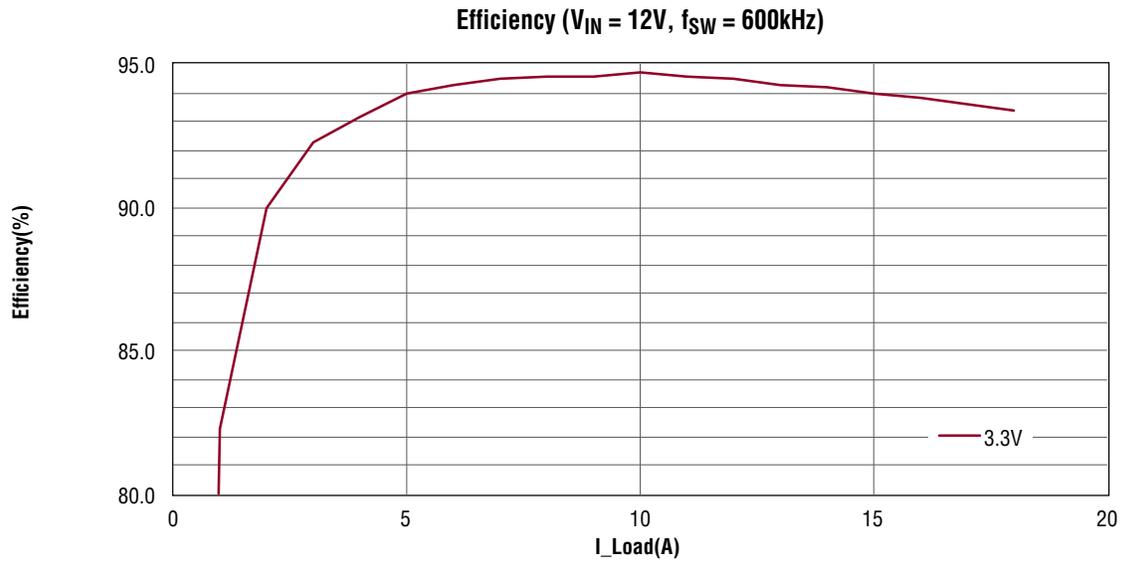


Figure 2. Measured Efficiency on Channel 1 ($V_{OUT1} = 3.3V, f_{SW} = 600kHz$, Channel 2 Disabled)

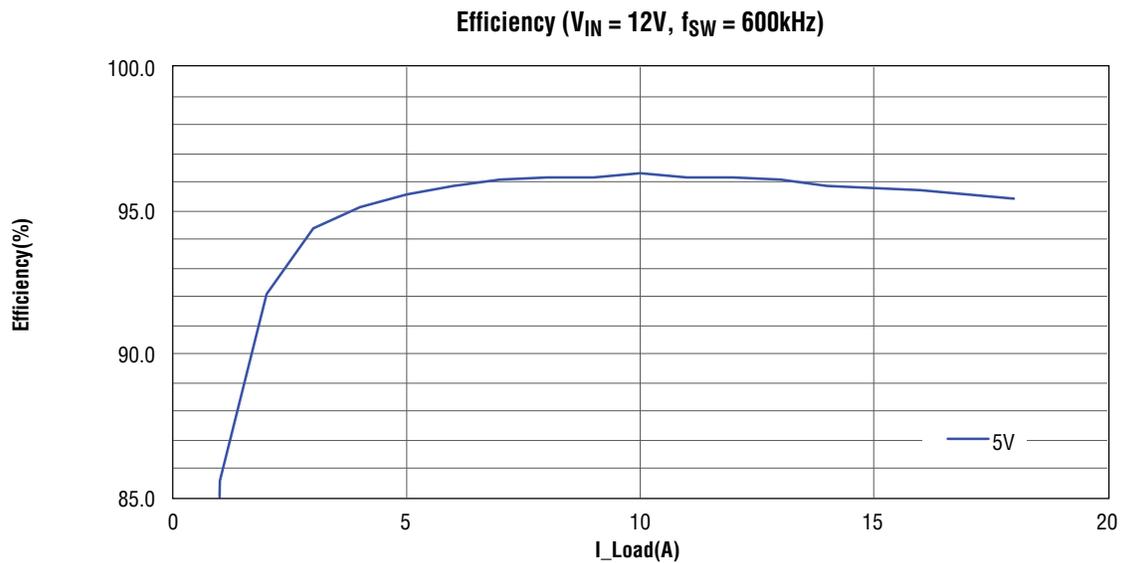


Figure 3. Measured Efficiency on Channel 2 ($V_{OUT2} = 5.0V, f_{SW} = 600kHz$, Channel 1 Disabled)

QUICK START PROCEDURE

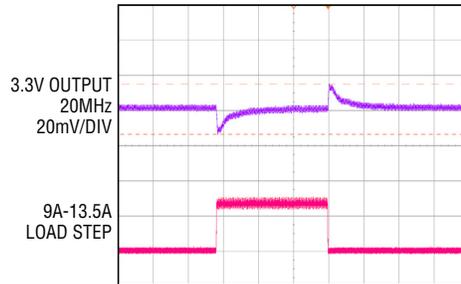


Figure 4. Measured Channel 1, 9A-13.5A Load Transient ($V_{IN} = 12V$, $V_{OUT1} = 3.3V$)

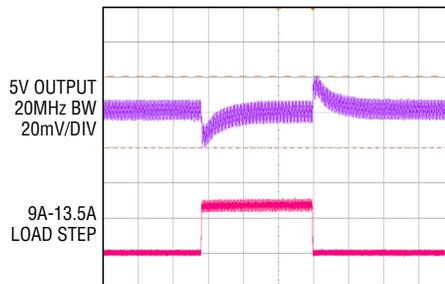


Figure 5. Measured Channel 2, 9A-13.5A Load Transient ($V_{IN} = 12V$, $V_{OUT2} = 5.0V$)

QUICK START PROCEDURE

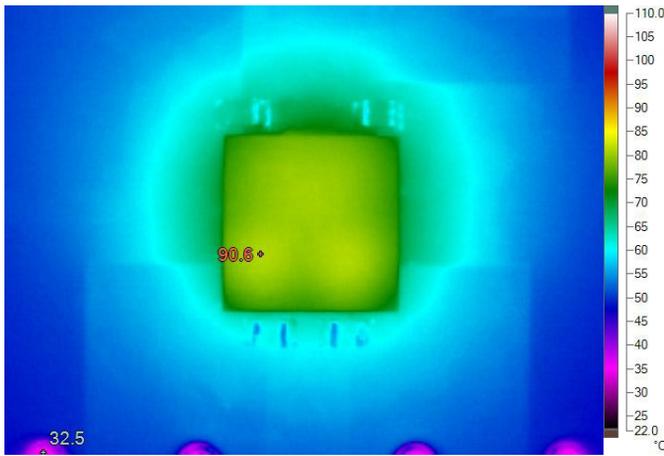


Figure 6. Thermal Capture at 12V_{IN}, 3.3V_{OUT1} at 14A and 5V_{OUT2} at 14A (T_A = 25°C, No Forced Airflow and No Heat Sink)

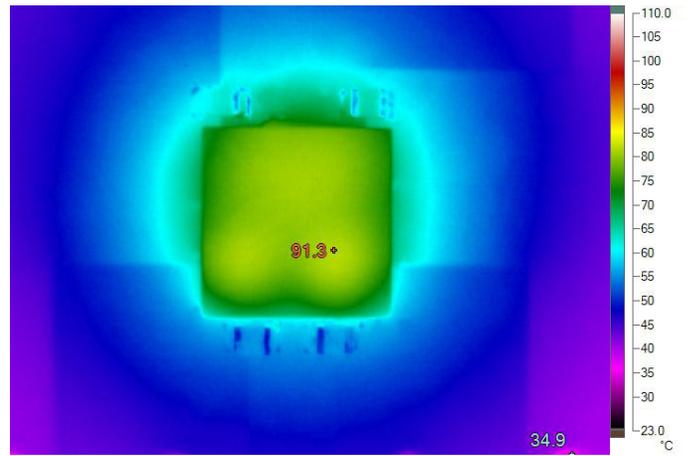


Figure 7. Thermal Capture at 12V_{IN}, 3.3V_{OUT1} at 17A and 5V_{OUT2} at 17A (T_A = 25°C, 200LFM Airflow and No Heat Sink)

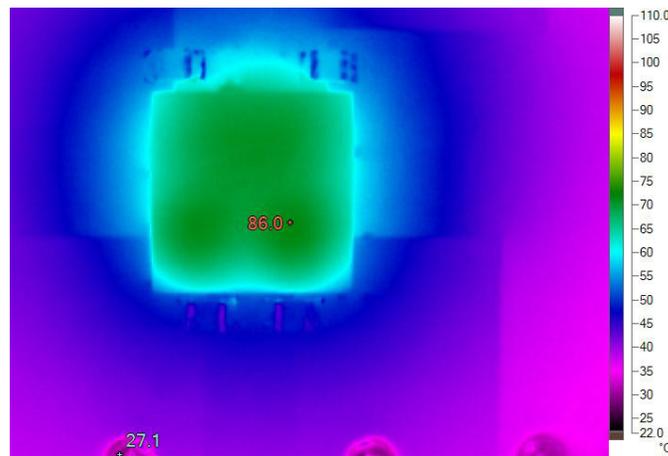


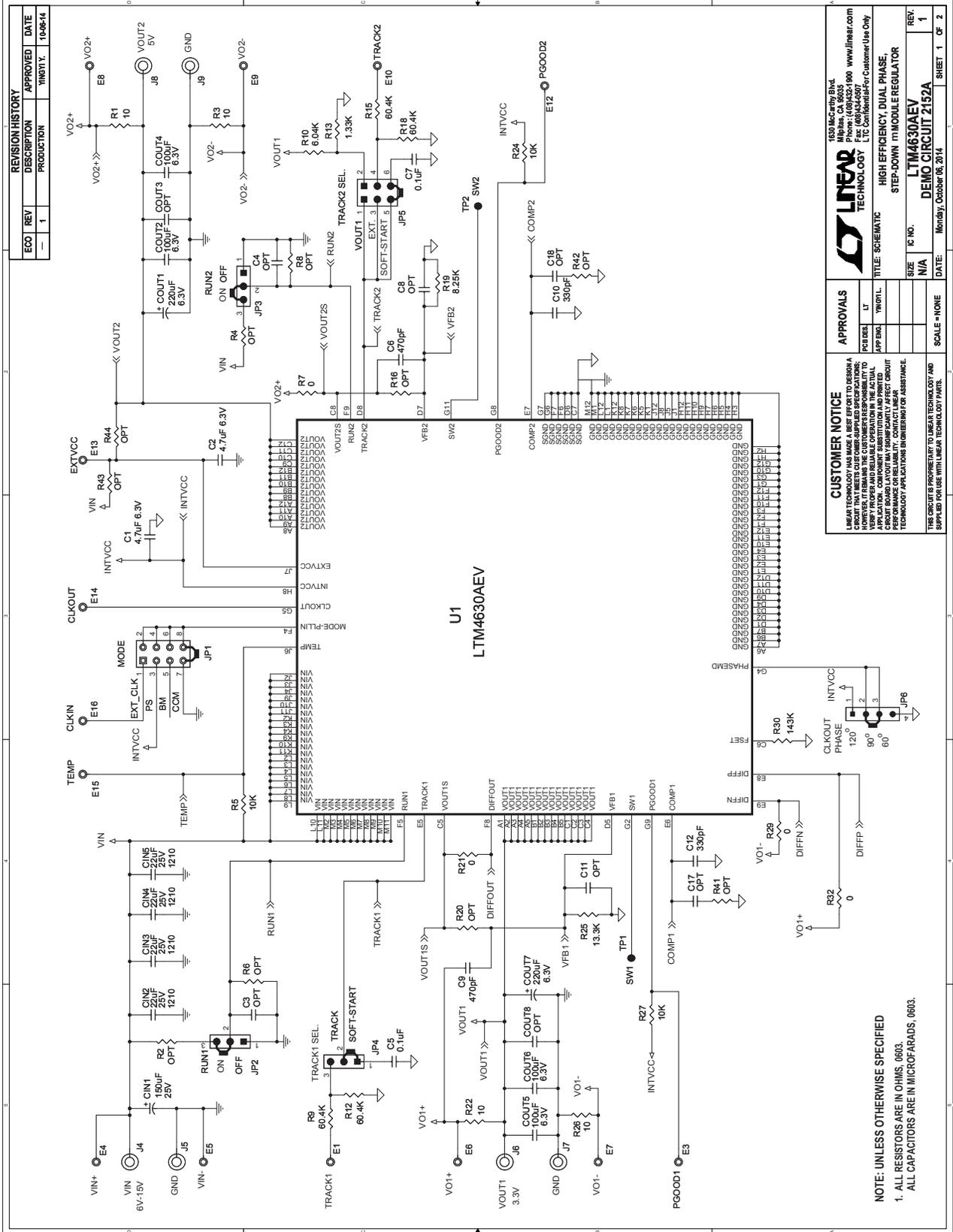
Figure 8. Thermal Capture at 12V_{IN}, 3.3V_{OUT1} at 18A and 5V_{OUT2} at 18A (T_A = 25°C, 400LFM Airflow and No Heat Sink)

PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|---|-----|---|-------------------------------------|-----------------------------------|
| Required Circuit Components | | | | |
| 1 | 1 | CIN1 | Cap., 150µF, 25V, Aluminum Electr., | SUN ELECT., 25CE150AX |
| 2 | 4 | CIN2, CIN3, CIN4, CIN5 | Cap., X5R, 22µF, 25V, 10%, 1210 | MURATA, GRM32ER61E226KE15L |
| 3 | 2 | COUT1, COUT7 | Cap., 220µF, 6.3V, POSCAP 7343 | PANASONIC, 6TPF220M5L |
| 4 | 4 | COUT2, COUT4, COUT5, COUT6 | Cap., X5R, 100µF, 6.3V, 20%, 1210 | AVX, 12106D107MAT2A |
| 5 | 2 | C1, C2 | Cap., X5R, 4.7µF, 6.3V, 10%, 0603 | AVX, 06036D475KAT2A |
| 6 | 2 | C5, C7 | Cap., X5R, 0.1µF, 25V, 10%, 0603 | AVX, 06033D104KAT |
| 7 | 2 | C6, C9 | Cap., X7R, 470pF, 100V, 10%, 0603 | AVX, 06031C471KAT2A |
| 8 | 2 | C10, C12 | Cap., X7R, 330pF, 100V, 10%, 0603 | AVX, 06031C331KAT2A |
| 9 | 2 | C13, C14 | Cap., X7R, 1µF, 10V, 10%, 0805 | AVX, 0805ZC105KAT2A |
| 10 | 2 | C15, C16 | Cap., X7R, 1µF, 10V, 10%, 0603 | AVX, 0603ZC105KAT2A |
| 11 | 1 | Q1 | XSTR,SUD50N04-8M8P-4GE3 MOSFET | VISHAY SUD50N04-8M8P-4GE3 |
| 12 | 4 | R1, R3, R22, R26 | Res., Chip, 10, 1%, 0603 | VISHAY, CRCW060310R0FKEA |
| 13 | 4 | R5, R24, R27, R36 | Res., Chip, 10k, 1%, 0603 | VISHAY, CRCW060310K0FKEA |
| 14 | 4 | R9, R12, R15, R18 | Res., Chip, 60.4k, 1%, 0603 | VISHAY, CRCW060360K4FKEA |
| 15 | 1 | R10 | Res., Chip, 6.04k, 1%, 0603 | VISHAY, CRCW06036K04FKEA |
| 16 | 1 | R13 | Res., Chip, 1.33k, 1%, 0603 | VISHAY, CRCW06031K33FKEA |
| 17 | 1 | R19 | Res., Chip, 8.25k, 1%, 0603 | VISHAY, CRCW06038K25FKEA |
| 18 | 1 | R25 | Res., Chip, 13.3k, 1%, 0603 | VISHAY, CRCW060313K3FKEA |
| 19 | 1 | R30 | Res., Chip, 143k, 1%, 0603 | VISHAY, CRCW06031431KFKEA |
| 20 | 1 | R37 | Res., Chip, 0.015Ω, 2W, 2512 | VISHAY, WSL2512R0150FEA |
| 21 | 1 | U1 | LTM4630AEV 15 × 15 × 4.41-LGA | LINEAR TECH., LTM4630AEV#PBF |
| Additional Demo Board Circuit Components | | | | |
| 1 | 0 | COUT3, COUT8, | OPT, 1210 | OPT |
| 2 | 0 | C3, C4, C8, C11, C17, C18 | OPT, 0603 | OPT |
| 3 | 0 | R2, R4, R6, R8, R11, R14, R16, R17, R20, R23, R28, R31, R33, R39, R40, R41, R42, R43, R44 | OPT, 0603 | OPT |
| 4 | 4 | R7, R21, R29, R32 | Res., Chip, 0, 1%, 0603 | VISHAY, CRCW06030000Z0EA |
| 5 | 1 | R34 | Res., Chip, 0Ω, 0.5W, 2010 | VISHAY, CRCW20100000Z0EF |
| 6 | 0 | R35 | OPT, 2010 | OPT |
| 7 | 0 | R38 | OPT, 2512 | OPT |
| Hardware: For Demo Board Only | | | | |
| 1 | 16 | E1, E3-E10, E12-E18 | TESTPOINT, TURRET, .094" pbf | MILL-MAX, 2501-2-00-80-00-00-07-0 |
| 2 | 3 | J1, J2, J3 | CONN, BNC, 5 PINS | CONNEX, 112404 |
| 3 | 6 | J4-J9 | JACK BANANA | KEYSTONE, 575-4 |
| 4 | 1 | JP1 | HEADER, 2 × 4 0.079 DOUBLE ROW | SULLINS, NRPN042PAEN-RC |
| 5 | 3 | JP2, JP3, JP4 | HEADER, 1 × 3 0.079 SINGLE ROW | SULLINS, NRPN031PAEN-RC |
| 6 | 1 | JP5 | HEADER, 2 × 3 0.079 DOUBLE ROW | SULLINS, NRPN032PAEN-RC |
| 7 | 1 | JP6 | HEADER, 1 × 4 0.079 SINGLE ROW | SULLINS, NRPN041PAEN-RC |
| 8 | 6 | XJP1-XJP6 | SHUNT, .079" CENTER | SAMTEC, 2SN-BK-G |
| 9 | 4 | (STAND-OFF) | STAND-OFF, NYLON 0.50" | KEYSTONE, 8833(SNAP ON) |

DEMO MANUAL DC2152A

SCHEMATIC DIAGRAM



| REVISION HISTORY | | | |
|------------------|-----|-------------|----------|
| ECO | REV | DESCRIPTION | DATE |
| - | 1 | PRODUCTION | 10-08-14 |


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APPROVALS
 DESIGNER: LT
 APPRVL: YH07L

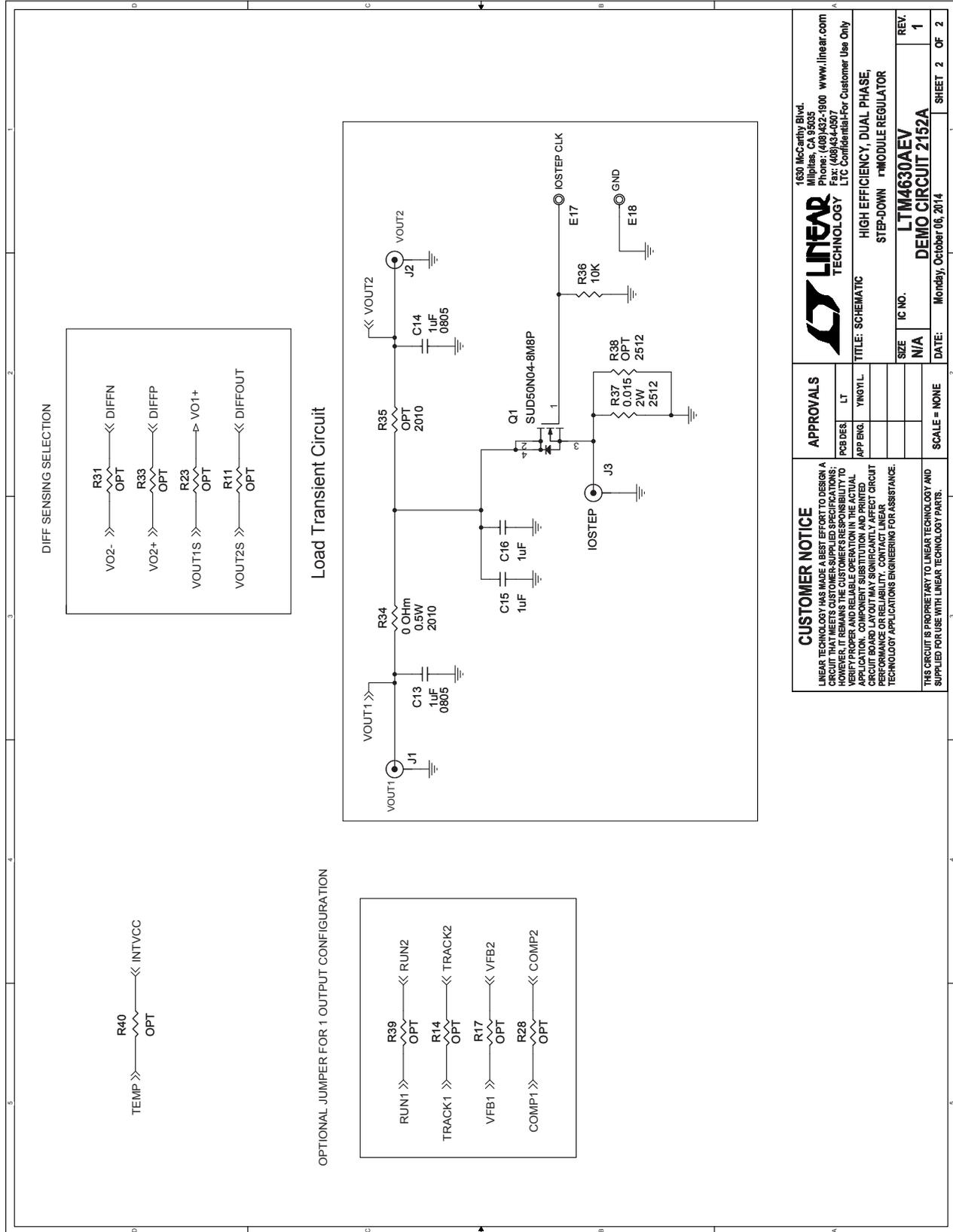
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TITLE: SCHEMATIC
HIGH EFFICIENCY DUAL PHASE
STEP-DOWN IN-MODULE REGULATOR
LTM4630AEV
DEMO CIRCUIT 2152A

SIZE: N/A I.C. NO.: LTM4630AEV
 DATE: Monday, October 06, 2014 REV: 1
 SCALE: NONE SHEET 1 OF 2

SCHEMATIC DIAGRAM



DEMO MANUAL DC2152A

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