Single/Dual Band RF Power Controllers

FEATURES

- **Dual Band RF Power Amplifier Control (LTC1757A-2)**
- **Improved Internal Schottky Diode Detector**
- **Wide Input Frequency Range: 850MHz to 2GHz**
- **Autozero Cancels Initial Offsets and Temperature Dependent Offset Errors**
- **Wide V_{IN} Range of 2.7V to 6V Allows Direct Connection to Battery**
- RF Output Power Set by External DAC
- Fast Acquire After Transmit Enable
- Internal Frequency Compensation
- Rail-to-Rail Power Control Outputs
- RF PA Supply Current Limiting
- Battery Overvoltage Protection
- Power Control Signal Overvoltage Protection
- Low Operating Current: 1mA
- Very Low Shutdown Current: <1µA
- Available in a 8-Pin MSOP Package (LTC1757A-1) and 10-Pin MSOP (LTC1757A-2)

APPLICATIONS

- Single/Dual Band GSM Cellular Telephones
- PCS Devices
- Wireless Data Modems
- TDMA Cellular Telephones

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DESCRIPTION

The LTC®1757A-2 is a dual band RF power controller for RF power amplifiers operating in the 850MHz to 2GHz range. The LTC1757A is pin compatible with the LTC1757 but has improved RF detection range. The input voltage range is optimized for operation from a single lithium-ion cell or 3× NiMH. Several functions required for RF power control and protection are integrated in one small 10-pin MSOP package, thereby minimizing PCB area.

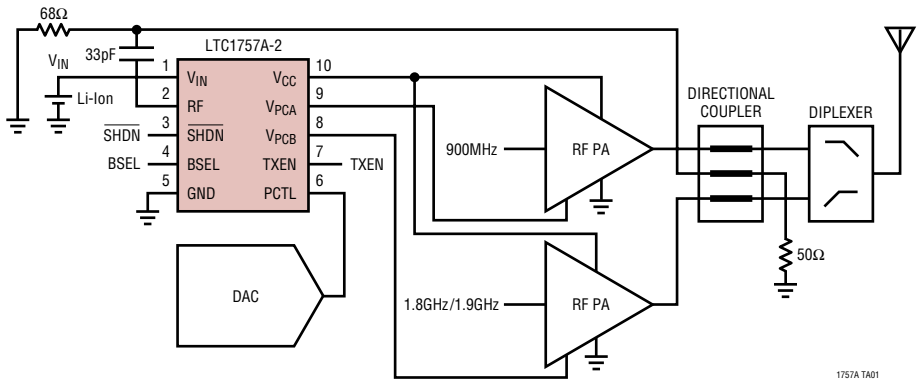
The LTC1757A-1 is a single output RF power controller that is identical in performance to the LTC1757A-2 except that one output (V_{PCA}) is provided. The LTC1757A-1 can be used to drive a single RF channel or dual channel module with integral multiplexer. This part is available in an 8-pin MSOP package.

RF power is controlled by driving the RF amplifier power control pins and sensing the resultant RF output power via a directional coupler. The RF sense voltage is peak detected using an on-chip Schottky diode. This detected voltage is compared to the DAC voltage at the PCTL pin to control the output power. The RF power amplifier is protected against high supply voltage and current and high power control pin voltages.

Internal and external offsets are cancelled over temperature by an autozero control loop, allowing accurate low power programming. The shutdown feature disables the part and reduces the supply current to <1µA.

TYPICAL APPLICATION

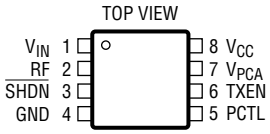
LTC1757A-2 Dual Band Cellular Telephone Transmitter



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} to GND ..... –0.3V to 6.5V
V_{PCA}, V_{PCB} Voltage ..... –0.3V to 3V
PCTL Voltage ..... –0.3V to (V_{IN} + 0.3V)
RF Voltage ..... (V_{IN} – 2.2V) to 7V
I_{VCC}, Continuous 1A
I_{VCC}, 12.5% Duty Cycle 2.5A
$\overline{SHDN}$, TXEN, BSEL
Voltage to GND ..... –0.3V to (V_{IN} + 0.3V)
$I_{VPCA/B}$, 25% Duty Cycle 20mA
Operating Temperature Range
(Note 2) ..... –30°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Junction Temperature ..... 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

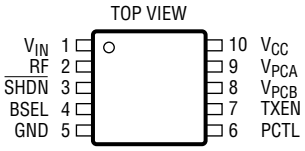
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC1757A-1EMS8
MS8 PART MARKING
LTPL



MS10 PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC1757A-2EMS
MS10 PART MARKING
LTPM

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, $\overline{SHDN}$ = TXEN = HI, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage	(Note 7)	●	2.7		6	V
I_{VIN} Shutdown Current	$\overline{SHDN}$ = LO, TXEN = LO, BSEL = LO	●			1	µA
I_{VIN} Autozero Current	$\overline{SHDN}$ = HI, TXEN = LO	●		0.9	1.5	mA
I_{VIN} Operating Current	$\overline{SHDN}$ = HI, TXEN = HI, I_{VPCA} = I_{VPCB} = 0mA, $V_{PCA/B}$ = HI	●		1	1.6	mA
I_{VCC} Current Limit				2.2		A
V_{IN} to V_{CC} Resistance	$\overline{SHDN}$ = LO, TXEN = LO			90	150	mΩ
$V_{PCA/B}$ V_{OL}	TXEN = HI, Open Loop, PCTL = –100mV	●		0	0.1	V
$V_{PCA/B}$ Dropout Voltage	I_{LOAD} = 5.5mA, V_{IN} = 2.7V	●			V_{IN} – 0.28	V
$V_{PCA/B}$ Voltage Clamp	R_{LOAD} = 400Ω	●	2.7	2.85	3.0	V
$V_{PCA/B}$ Output Current	$V_{PCA/B}$ = 2.4V, V_{IN} = 2.7V	●	5.5	9		mA
$V_{PCA/B}$ Enable Time	V_{PCTL} = 2V Step, C_{LOAD} = 100pF (Note 5)			200		ns
$V_{PCA/B}$ Bandwidth	C_{LOAD} = 100pF, R_{LOAD} = 400Ω (Note 9)	●	250	400	550	kHz
$V_{PCA/B}$ Load Capacitance	(Note 6)				100	pF
$V_{PCA/B}$ Slew Rate	V_{PCTL} = 2V Step, C_{LOAD} = 100pF (Note 3)		1.5	3		V/µs
$V_{PCA/B}$ Droop	V_{IN} = 2.7V, V_{PCTL} = 2V Step			±10		µV/ms
$V_{PCA/B}$ TXEN Start Voltage	Open Loop, TXEN Low to High, C_{LOAD} = 100pF (Note 10)		400	550	700	mV
$\overline{SHDN}$ Input Threshold	V_{IN} = 2.7V to 6V, TXEN = LO	●	0.35		1.4	V
TXEN, BSEL Input Threshold	V_{IN} = 2.7V to 4.7V	●	0.35		1.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, $\overline{SHDN}$ = TXEN = HI, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$, TXEN, BSEL Input Current	$\overline{SHDN}$, TXEN or BSEL = 3.6V	●	10	30	50	µA
PCTL Input Voltage Control Range	V_{IN} = 2.7V to 4.7V, R_{LOAD} = 400Ω	●	0		2	V
PCTL Input Voltage Range	V_{IN} = 3V, R_{LOAD} = 400Ω (Note 8)	●			2.4	V
PCTL Input Resistance	$\overline{SHDN}$ = LO, TXEN = LO	●	50	100	150	kΩ
PCTL Input Filter				1.25		MHz
Autozero Range	V_{IN} = 2.7V, R_{LOAD} = 400Ω (Note 4)	●			400	mV
Autozero Settling Time (t_S)	Shutdown to Enable (Autozero), V_{IN} = 2.7V (Note 11)	●			50	µs
RF Input Frequency Range	(Note 6)	●	850		2000	MHz
RF Input Power Range	900MHz (Note 6) 1800MHz (Note 6)		–24 –22		16 16	dBm dBm
RF DC Input Resistance	Referenced to V_{IN}, $\overline{SHDN}$ = LO, TXEN = LO	●	100	185	300	Ω
V_{IN} Overvoltage Range	$V_{PCA/B}$ < 0.5V, R_{LOAD} = 400Ω	●	4.8	5.0	5.4	V
BSEL Timing	t_1, Setup Time Prior to TXEN Asserted High t_2, Hold Time After TXEN is Asserted Low			200 200		ns ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1757A-1 and LTC1757A-2 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –30°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Slew rate is measured open loop. The slew time at V_{PCA} or V_{PCB} is measured between 1V and 2V.

Note 4: Maximum DAC zero-scale offset voltage that can be applied to PCTL.

Note 5: This is the time from TXEN rising edge 50% switch point to $V_{PCA/B}$ = 1V.

Note 6: Guaranteed by design. This parameter is not production tested.

Note 7: For V_{IN} voltages greater than 4.7V, V_{PCA}/V_{PCB} are set low by the overvoltage shutdown.

Note 8: Includes maximum DAC offset voltage and maximum control voltage.

Note 9: Bandwidth is calculated using the 10% to 90% rise time equation:

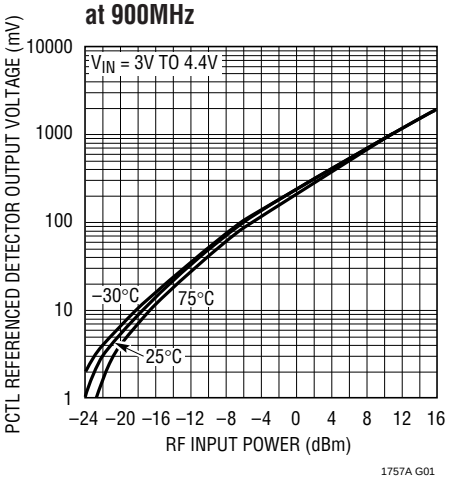
BW = 0.35/rise time

Note 10: Measured 1µs after TXEN = HI.

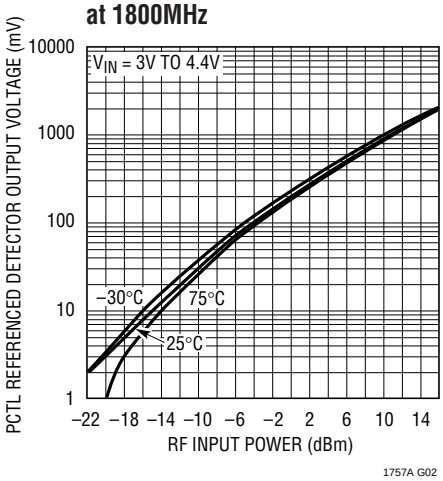
Note 11: 50% switch point, $\overline{SHDN}$ HI = V_{IN}, TXEN HI = V_{IN}.

TYPICAL PERFORMANCE CHARACTERISTICS

RF Detector Characteristics at 900MHz



RF Detector Characteristics at 1800MHz



PIN FUNCTIONS (LTC1757A-2/LTC1757A-1)

V_{IN} (Pin 1): Input Supply Voltage, 2.7V to 6V. V_{IN} should be bypassed with 0.1µF and 100pF ceramic capacitors. Used as return for RF 185Ω termination.

RF (Pin 2): RF Feedback Voltage from the Directional Coupler. Referenced to V_{IN}. A coupling capacitor of 33pF must be used to connect to the ground referenced directional coupler. The frequency range is 850MHz to 2000MHz. This pin has an internal 185Ω termination, an internal Schottky diode detector and peak detector capacitor.

SHDN (Pin 3): Shutdown Input. A logic low on the $\overline{SHDN}$ pin places the part in shutdown mode. A logic high places the part in autozero when TXEN is low. $\overline{SHDN}$ has an internal 150k pull-down resistor to ensure that the part is in shutdown when the drivers are in a three-state condition.

BSEL (Pin 4): (LTC1757A-2 Only) Selects V_{PCA} when low and V_{PCB} when high. This input has an internal 150k resistor to ground.

GND (Pin 5/Pin 4): System Ground.

PCTL (Pin 6/Pin 5): Analog Input. The external power control DAC drives this input. The amplifier servos the RF power until the RF detected signal equals the DAC signal. The input resistance is typically 100k.

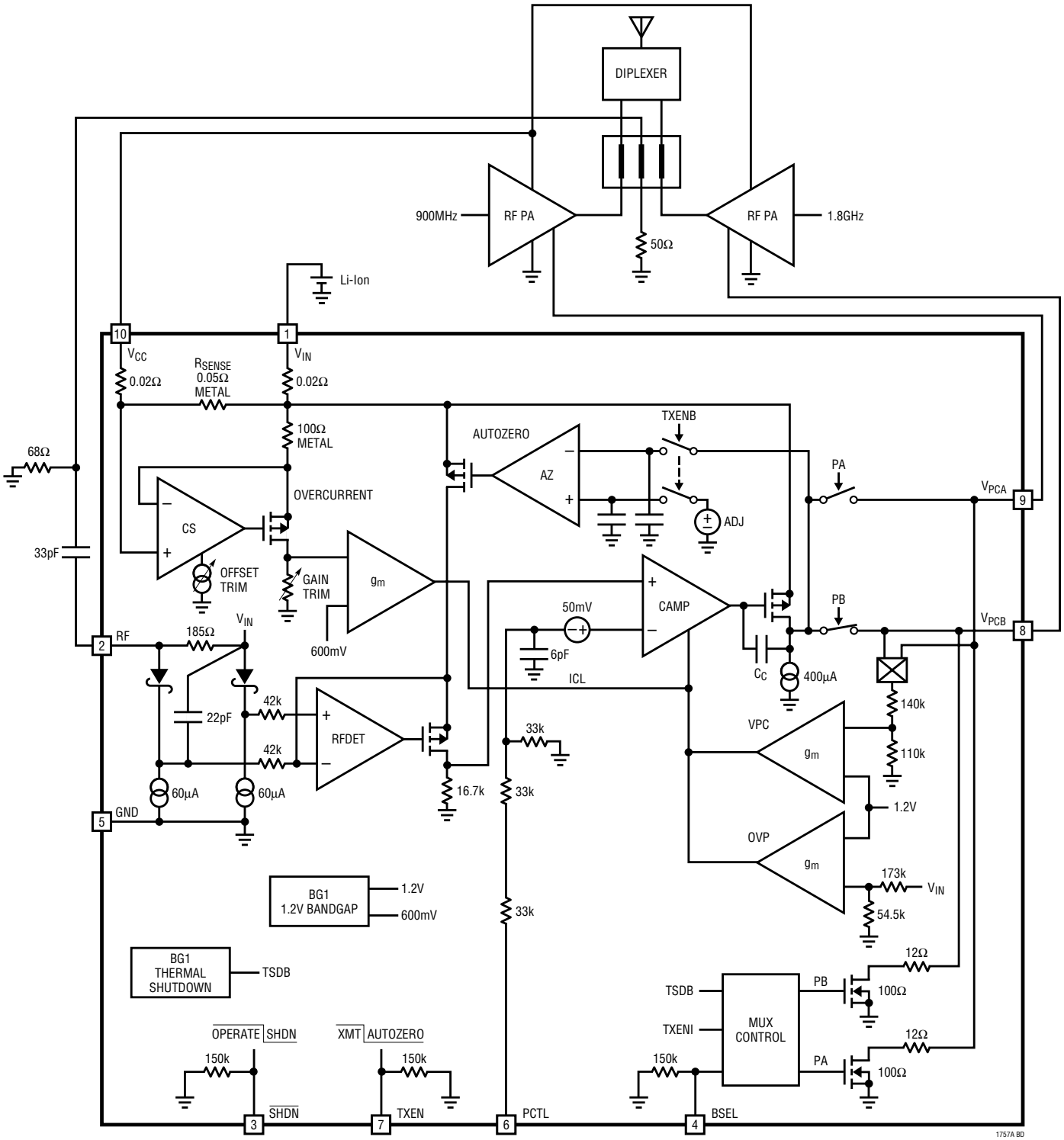
TXEN (Pin 7/Pin 6): Transmit Enable Input. A logic high enables the control amplifier. When TXEN is low and $\overline{SHDN}$ is high the part is in the autozero mode. This input has an internal 150k resistor to ground.

V_{PCB} (Pin 8): (LTC1757A-2 Only) Power Control Voltage Output. This pin drives an external RF power amplifier power control pin. The maximum load capacitance is 100pF. The output is capable of rail-to-rail swings at low load currents. Selected when BSEL is high.

V_{PCA} (Pin 9/Pin 7): Power Control Voltage Output. This pin drives an external RF power amplifier power control pin. The maximum load capacitance is 100pF. The output is capable of rail-to-rail swings at low load currents. Selected when BSEL is low (LTC1757A-2 only).

V_{CC} (Pin 10/Pin 8): RF Power Amplifier Supply. This pin has an internal 0.050Ω sense resistor between V_{IN} and V_{CC} that senses the RF power amplifier supply current to detect overcurrent conditions.

BLOCK DIAGRAM (LTC1757A-2)



APPLICATIONS INFORMATION

Operation

The LTC1757A-2 dual band RF power control amplifier integrates several functions to provide RF power control over two frequencies ranging from 850MHz to 2GHz. The device also prevents damage to the RF power amplifier due to overvoltage or overcurrent conditions. These functions include an internally compensated power control amplifier to control the RF output power, an autozero section to cancel internal and external voltage offsets, a sense amplifier with an internal sense resistor to limit the maximum RF power amplifier current, an RF Schottky diode peak detector and amplifier to convert the RF feedback signal to DC, a $V_{PCA/B}$ overvoltage clamp, a V_{IN} overvoltage detector, a bandgap reference, a thermal shutdown circuit and a multiplexer to switch the control amplifier output to either V_{PCA} or V_{PCB}.

Band Selection

The LTC1757A-2 is designed for dual band operation. The BSEL pin will select output V_{PCA} when low and output V_{PCB} when high. For example, V_{PCA} could be used to drive a 900MHz channel and V_{PCB} a 1.8GHz/1.9GHz channel. BSEL must be established before the part is enabled. The LTC1757A-1 can be used to drive a single RF channel or dual channel module with integral multiplexer.

Control Amplifier

The control amplifier supplies the power control voltage to the RF power amplifier. A portion (typically –19dB for low frequencies and –14dB for high frequencies) of the RF output signal is sampled, via a directional coupler, to close the gain control loop. When a DAC signal is applied to PCTL, the amplifier quickly servos V_{PCA} or V_{PCB} positive until the detected feedback voltage applied to the RF pin matches the voltage at PCTL. This feedback loop provides accurate RF power control. V_{PCA} or V_{PCB} are capable of driving a 5.5mA load current and 100pF load capacitor.

RF Detector

The internal RF Schottky diode peak detector and amplifier converts the RF feedback voltage from the directional coupler to a low frequency voltage. This voltage is compared to the DAC voltage at the PCTL pin by the control amplifier to close the RF power control loop. The RF pin input resistance is typically 185Ω and the frequency range of this pin is 850MHz to 2000MHz. The detector demonstrates excellent efficiency and linearity over a wide range of input power. The Schottky detector is biased at about 60μA and drives an on-chip peak detector capacitor of 22pF.

Autozero

An autozero system is included to improve power programming accuracy over temperature. This section cancels internal offsets associated with the Schottky diode detector and control amplifier. External offsets associated with the DAC driving the PCTL pin are also cancelled. Offset drift due to temperature is cancelled between each burst by the autozero system. The maximum offset allowed at the DAC output is limited to 400mV. Autozeroing is performed when the part is in autozero mode ($\overline{SHDN}$ = high, TXEN = low). When the part is enabled (TXEN = high, $\overline{SHDN}$ = high) the autozero capacitors are held and the V_{PCA} or V_{PCB} pin is connected to the control amplifier output. The hold droop voltage of typically 10μV/ms provides for accurate offset cancellation over the 1/8 duty cycle associated with the GSM protocol as well as multislot protocals. The part must be in the autozero mode for at least 50μs for autozero to settle to the correct value.

Protection Features

The RF power amplifier is overcurrent protected by an internal sense amplifier. The sense amplifier measures the voltage across an internal 0.050Ω resistor to determine the RF power amplifier current. V_{PCA} or V_{PCB} is lowered as this supply current exceeds 2.2A, thereby regulating the current to about 2.25A. The regulated current limit is temperature compensated. The 0.050Ω resistor and the current limit feature can be removed by connecting the PA directly to V_{IN}.

The RF power amplifier control voltage pins are overvoltage protected. The V_{PC} overvoltage clamp regulates V_{PCA} or V_{PCB} to 2.85V when the gain and PCTL input combination attempts to exceed this voltage.

The RF power amplifier is protected against excessive input supply voltages. The V_{IN} overvoltage detector starts

APPLICATIONS INFORMATION

to reduce V_{PCA} or V_{PCB} when V_{IN} exceeds 5V. V_{PCA} or V_{PCB} will be reduced to 0V as V_{IN} continues to increase by about 200mV. This gain control voltage reduction lowers the RF output power eventually reducing it to zero.

The internal thermal shutdown circuit will disable the LTC1757A-2 if the junction temperature exceeds approximately 150°C. The part will be enabled when the temperature falls below 140°C.

Modes of Operation

The LTC1757A-2 supports three operating modes: shutdown, autozero and enable.

In shutdown mode ($\overline{SHDN}$ = Low) the part is disabled and supply currents will be reduced to <1µA. V_{PCA} and V_{PCB} will be connected to ground via 100Ω switches.

In autozero mode ($\overline{SHDN}$ = High, TXEN = Low) V_{PCA} and V_{PCB} will remain connected to ground and the part will be in the autozero mode. The part must remain in autozero for at least 50µs to allow for the autozero circuit to settle.

In enable mode ($\overline{SHDN}$ = High, TXEN = High) the control loop and protection functions will be operational. When TXEN is switched high, acquisition will begin. The control amplifier will start to ramp the control voltage to the RF power amplifier. The RF amplifier will then start to turn on.

The feedback voltage from the directional coupler and the output power will be detected by the LTC1757A-2 at the RF pin. The loop closes and the amplifier output tracks the DAC voltage ramping at PCTL. The RF power output will then follow the programmed power profile from the DAC.

MODE	$\overline{SHDN}$	TXEN	OPERATION
Shutdown	Low	Low	Disabled
Autozero	High	Low	Autozero
Enable	High	High	Power Control

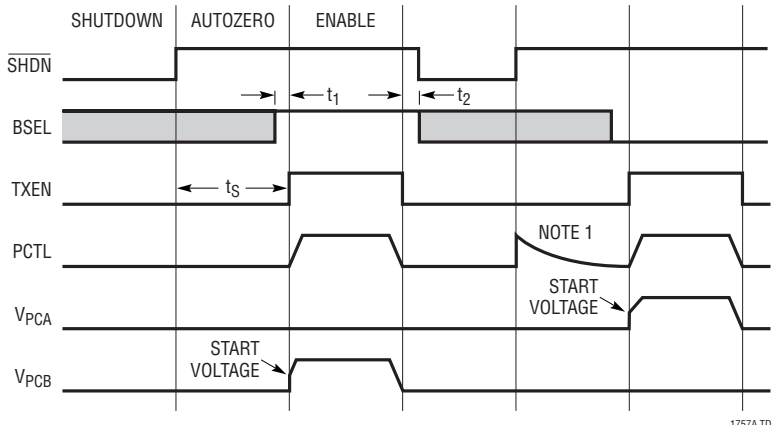
LTC1757A-1 Description

The LTC1757A-1 is identical in performance to the LTC1757A-2 except that only one control output (V_{PCA}) is available. The LTC1757A-1 can drive a single RF channel in the 850MHz to 2GHz range or a dual RF channel module with an internal multiplexer. Several manufacturers offer dual RF channel modules with an internal multiplexer.

General Layout Considerations

The LTC1757A-1/LTC1757A-2 should be placed near the directional coupler. The feedback signal line to the RF pin should be a 50Ω transmission line with a 68Ω termination. If short-circuit protection is used, bypass capacitors are required at V_{CC}.

LTC1757A-2 Timing Diagram



t_S: AUTOZERO SETTLING TIME, 50µs MINIMUM
t_1: BSEL CHANGE PRIOR TO TXEN, 200ns TYPICAL
t_2: BSEL CHANGE AFTER TXEN, 200ns TYPICAL

NOTE 1: THE EXTERNAL DAC DRIVING THE PCTL PIN CAN BE ENABLED DURING AUTOZERO. THE AUTOZERO SYSTEM WILL CANCEL THE DAC TRANSIENT. THE DAC MUST BE SETTLED TO AN OFFSET ≤400mV BEFORE TXEN IS ASSERTED HIGH.

APPLICATIONS INFORMATION

External Termination

The LTC1757A has an internal 185Ω termination resistor at the RF pin. If a directional coupler is used, it is recommended that an external 68Ω termination resistor be connected between the RF coupling capacitor (33pF), and ground at the side connected to the directional coupler. If the termination is placed at the LTC1757A RF pin, then the 68Ω resistor must be connected to V_{IN} since the detector is referenced to V_{IN}. Termination components should be placed adjacent to the LTC1757A.

Power Ramp Profiles

The external voltage gain associated with the RF channel can vary significantly between RF power amplifier types. The LTC1757A frequency compensation has been optimized to be stable with several different power amplifiers and manufacturers. This frequency compensation generally defines the loop dynamics that impact the power/time response and possibly (slow loops) the power ramp sidebands. The LTC1757A operates open loop until an RF voltage appears at the RF pin, at which time the loop closes and the output power follows the DAC profile. The RF power amplifier will require a certain control voltage level (threshold) before an RF output signal is produced. The LTC1757A $V_{PCA/B}$ outputs must quickly rise to this threshold voltage in order to meet the power/time profile. To reduce this time, the LTC1757A starts at 550mV. However, at very low power levels the PCTL input signal is small, and the $V_{PCA/B}$ outputs may take several microseconds to reach the RF power amplifier threshold voltage. To reduce this time, it may be necessary to apply a positive pulse at the start of the ramp to quickly bring the $V_{PCA/B}$ outputs to the threshold voltage. This can generally be achieved with DAC programming. The magnitude of the pulse is dependent on the RF amplifier characteristics.

Power ramp sidebands and power/time are also a factor when ramping to zero power. For RF amplifiers requiring high control voltages, it may be necessary to further adjust the DAC ramp profile. When the power is ramped down the loop will eventually open at power levels below the LTC1757A detector threshold. The LTC1757A will then go open loop and the output voltage at V_{PCA} or V_{PCB} will stop

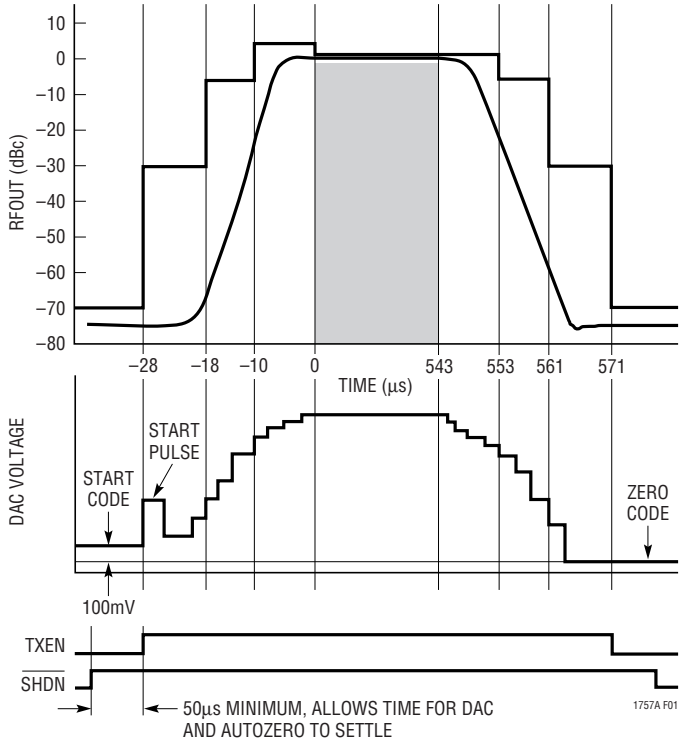


Figure 1. LTC1757A Ramp Timing

APPLICATIONS INFORMATION

falling. If this voltage is high enough to produce RF output power, the power/time or power ramp sidebands may not meet specification. This problem can be avoided by starting the DAC ramp from 100mV (Figure 1). At the end of the cycle, the DAC can be ramped down to 0mV. This applies a negative signal to the LTC1757A thereby ensuring that the $V_{PCA/B}$ outputs will ramp to 0V. The 100mV ramp step must be applied at least 4µs before TXEN is asserted high to allow for the auto zero to cancel the step. Slow DAC rise times due to filtering will extend this time by the additional RC time constants.

Another factor that affects power ramp sidebands is the DAC signal to PCTL. The bandwidth of the LTC1757A is not low enough to adequately filter out steps associated with the DAC. If the baseband chip does not have an internal filter, it is recommended that a 2-stage external filter be placed between the DAC output and the PCTL pin. Resistor values should be kept below 2k since the PCTL input resistance is 100k. A typical filter scheme is shown in Figure 2.

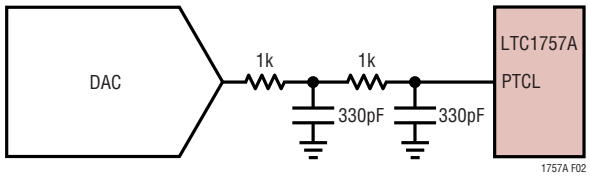


Figure 2

RF Input Voltage Levels

The LTC1757A detects peak RF voltage levels. The maximum peak RF voltage level is 2V corresponding to 16dBm in a 50Ω system. The RF signal is normally supplied via a directional coupler. The directional coupler loss for the low band is typically 19dB and for the high band 14dB. The high band generally requires a 5dB lower minimum power level and to keep the minimum RF detector voltage levels similar between both bands, the directional coupler loss is adjusted accordingly.

The maximum RF input voltage or power restriction must be considered when determining coupler loss requirements. If the RF power at the directional coupler is increased due to losses after the coupler, the increased power levels must not result in excessive RF voltages at the RF pin. If 2dB is lost after the directional coupler, then the directional coupler loss should be increased by 2dB. For example, if the maximum output requirement is 30dBm, but 32dBm is required at the directional coupler, then the coupler loss should be at least 16dB. Excessive coupler loss will degrade low power performance due to lower Schottky detector efficiencies. If the directional coupler loss cannot be easily adjusted a resistor network can be used as shown in Figure 3.

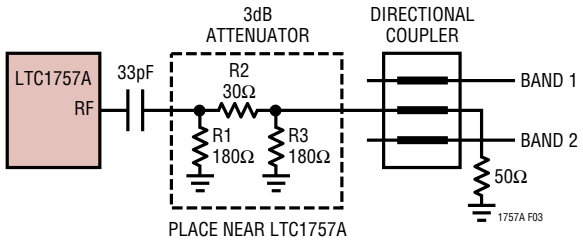


Figure 3

Demo Board

The LTC1757A has a demo board available upon request. The demo board has a 900MHz and an 1800MHz RF channel controlled by the LTC1757A. Timing signals for TXEN are generated on the board using a 13MHz crystal reference. The PCTL power control pin is driven by a 10-bit DAC and the DAC profile can be loaded via a serial port. The serial port data is stored in a flash memory, which is capable of storing eight ramp profiles. The board is supplied preloaded with four GSM power profiles and four DCS power profiles covering the entire power range. External timing signals can be used in place of the internal crystal controlled timing. A variety of RF power amplifier channels are available.

LTC1757A Control Loop Stability

The LTC1757A provides a stable control loop for several RF power amplifier models from different manufacturers over a wide range of frequencies, output power levels and V_{SWR} conditions. However, there are several factors that can improve or degrade loop frequency stability.

APPLICATIONS INFORMATION

1) The additional voltage gain supplied by the RF power amplifier increases the loop gain raising poles normally below the 0dB axis. The extra voltage gain can vary significantly over input/output power ranges, frequency, power supply, temperature and manufacturer. RF power amplifier gain control transfer functions are often not available and must be generated by the user. Loop oscillations are most likely to occur in the midpower range where the external voltage gain associated with the RF power amplifier typically peaks. It is useful to measure the oscillation or ringing frequency to determine whether it corresponds to the expected loop bandwidth and thus is due to high gain bandwidth.

2) Loop voltage losses supplied by the directional coupler will improve phase margin. The larger the directional coupler loss the more stable the loop will become. However, larger losses reduce the RF signal to the LTC1757A and detector performance may be degraded at low power levels. (See RF Detector Characteristics.)

3) Additional poles within the loop due to filtering or the turn-on response of the RF power amplifier can degrade the phase margin if these pole frequencies are near the effective loop bandwidth frequency. Generally loops using RF power amplifiers with fast turn-on times have more phase margin. Extra filtering below 16MHz should never be placed within the control loop, as this will only degrade phase margin.

4) Control loop instability can also be due to open loop issues. RF power amplifiers should first be characterized in an open loop configuration to ensure self oscillation is not present. Self-oscillation is often related to poor power supply decoupling, ground loops, coupling due to poor layout and extreme V_{SWR} conditions. The oscillation frequency is generally in the 100kHz to 10MHz range. Power supply related oscillation suppression requires large value ceramic decoupling capacitors placed close to the RF power amp supply pins. The range of decoupling capacitor values is typically 1nF to 3.3µF.

5) Poor layout techniques associated with the directional coupler area may result in high frequency signals bypassing the coupler. This could result in stability problems due to the reduction in the coupler loss.

Determining External Loop Voltage Gain and Bandwidth

The external loop voltage gain contributed by the RF channel and directional coupler network should be measured in a closed loop configuration. A voltage step is applied to PCTL and the change in V_{PCA} (or V_{PCB}) is measured. The detected voltage is 0.85 • PCTL and the external voltage gain contributed by the RF power amplifier and directional coupler network is $0.85 \bullet \Delta V_{PCTL}/\Delta V_{VPCA}$. Measuring voltage gain in the closed loop configuration accounts for the nonlinear detector gain that is dependent on RF input voltage and frequency as well as RF channel gain peaking.

The LTC1757A unity gain bandwidth specified in the data sheet assumes that the net voltage gain contributed by the RF power amplifier and directional coupler is unity. The bandwidth is calculated by measuring the rise time between 10% and 90% of the voltage change at V_{PCA} or V_{PCB} for a small step in voltage applied to PCTL.

$$BW1 = 0.35/\text{rise time}$$

The LTC1757A control amplifier unity gain bandwidth (BW1) is typically 400kHz. The phase margin of the control amplifier is typically 86°.

For example to determine the external RF channel loop voltage gain with the loop closed, apply a 100mV step to PCTL from 300mV to 400mV. V_{PCA} (or V_{PCB}) will increase to supply enough feedback voltage to the RF pin to cancel this 100mV step which would be the required detected voltage of 85mV. V_{PCA} changed from 1.498V to 1.540V to create the RF output power change required. The net external voltage gain contributed by the RF power amplifier and directional coupler network can be calculated by dividing the 85mV change at the RF pin by the 42mV change at the V_{PCA} pin. The net external voltage gain would then be approximately 2. The loop bandwidth extends to 2 • BW1. If BW1 is 400kHz, the loop bandwidth increases to approximately 800kHz. The phase margin can be determined from Figure 4. Repeat the above voltage gain measurement over the full power and frequency range.

APPLICATIONS INFORMATION

External pole frequencies within the loop may further reduce phase margin. The phase margin degradation, due to external and internal pole combinations, is difficult to determine since complex poles are present. Gain peaking may occur, resulting in higher bandwidth and lower phase margin than predicted from the open loop Bode plot. A low frequency AC SPICE model of the LTC1757A power controller is included to better determine pole and zero interactions. The user can apply external gains and poles to determine bandwidth and phase margin. DC, transient and RF information cannot be extracted from the present model. The model is suitable for external gain evaluations up to 6×. The 1.25MHz PCTL input filter limits the bandwidth, therefore, the RF input is used in the model.

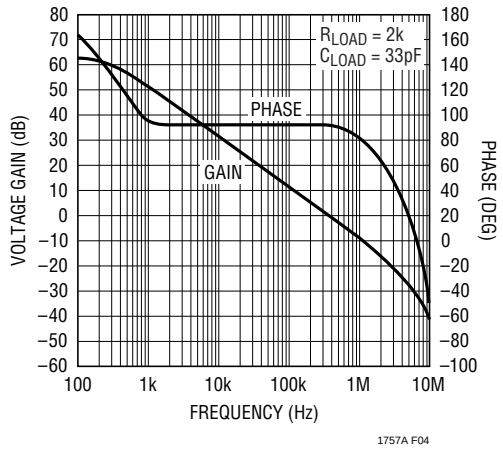


Figure 4. Measured Open Loop Gain and Phase

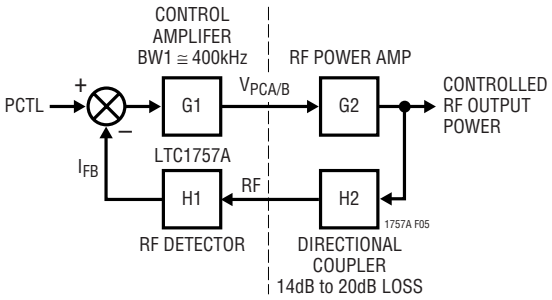


Figure 5. Closed Loop Block Diagram

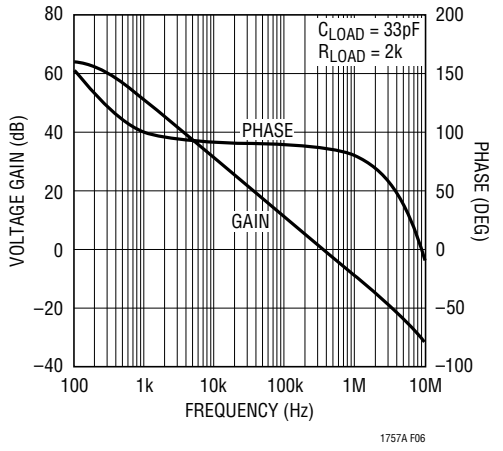


Figure 6. SPICE Model Open Loop Gain and Phase Characteristics from RF to V_{PCA}

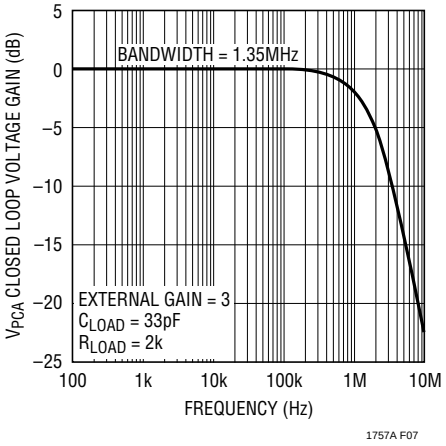


Figure 7. SPICE Model Closed Loop Voltage Gain

APPLICATIONS INFORMATION

```
*LTC1757A Low Frequency AC Spice Model*
GIN1 ND2 0 ND1 IFB 59E-6
GX3 ND6 0 0 ND4 1E-6
GX4 ND7 0 0 ND6 1E-6
GX1 ND3 0 0 ND2 1E-6
GX2 ND4 0 0 ND3 1E-6
GX5 ND10 0 0 ND9 1E-6
GX8 ND14 0 0 ND12 1E-6
GX7 ND12 0 0 ND11 1E-6
GX6 ND11 0 0 ND10 1E-6
GXFB IFB 0 0 ND14 23.53E-6
EX1 ND8 0 0 ND7 1
RPCTL2 ND1 0 33.75E3
RO1 ND2 0 85E6
RX3 ND6 0 1E6
RX4 ND7 0 1E6
RPCTL1 PCTL ND1 67.5E3
RX1 ND3 0 1E6
RX2 ND4 ND5 1E6
RSD RF ND9 500
RX5 ND10 0 1E6
RT RF 0 200
RX8 ND14 0 1E6
RX7 ND12 ND13 1E6
RX6 ND11 0 1E6
R9 ND8 ND8A 100
R9A ND8A VPCA 20
RLOAD VPCA 0 2E3
RFB1 IFB 0 16.75E3
CPCTL1 ND1 0 5.8E-12
CX3 ND6 0 1.2E-15
CX4 ND7 0 3.6E-15
CC1 ND2 0 10E-12
CX1 ND3 0 1.4E-15
CX5 ND10 0 10E-15
CX6 ND11 0 1.2E-15
CLOAD VPCA 0 33E-12
CLINT ND8A 0 37E-12
CLINTA VPCA 0 18E-12
CFB1 IFB 0 1E-12
CP ND9 0 22E-12
LX2 ND5 0 17E-3
LX7 ND13 0 7E-3
**Closed loop connections, comment-out VPCTLO, VRF, Adjust EFB gain to reflect external gain, currently set at 3X**
*EFB RF 0 VPCA VIN 3
*VIN VIN 0 DC 0 AC 1
*VPCTLO PCTL 0 DC 0
**Open loop connections, comment-out EFB, VIN and VPCTLO**
VPCTLO PCTL 0 DC 0
VRF RF 0 DC 0 AC 1
**Add AC statement and print statement as required**
.AC DEC 50 100 1E7
.END
```

Figure 8. LTC1757A Low Frequency AC SPICE Model

APPLICATIONS INFORMATION

This model (Figure 8) is being supplied to LTC users as an aid to circuit designs. While the model reflects reasonably close similarity to corresponding devices in low frequency AC performance terms, its use is not suggested as a replacement for breadboarding. Simulation should be used as a forerunner or a supplement to traditional lab testing.

Users should note very carefully the following factors regarding this model: Model performance in general will reflect typical baseline specs for a given device, and certain aspects of performance may not be modeled fully. While reasonable care has been taken in the preparation, we cannot be responsible for correct application on any and all computer systems. Model users are hereby notified that these models are supplied "as is", with no direct or implied responsibility on the part of LTC for their operation within a customer circuit or system. Further, Linear Technology Corporation reserves the right to change these models without prior notice.

In all cases, the current data sheet information is your final design guideline, and is the only performance guarantee.

For further technical information, refer to individual device data sheets. Your feedback and suggestions on this model is appreciated.

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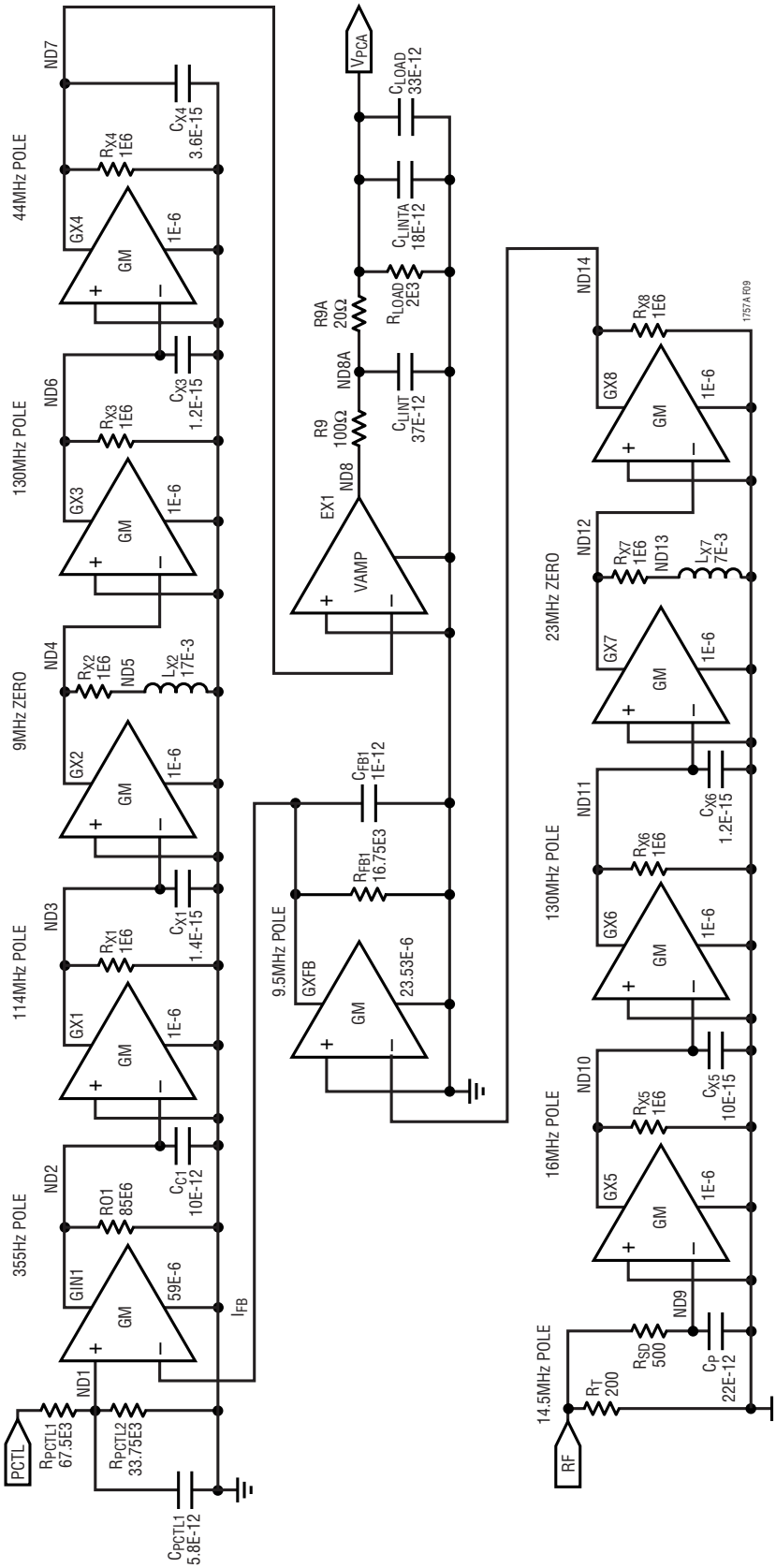
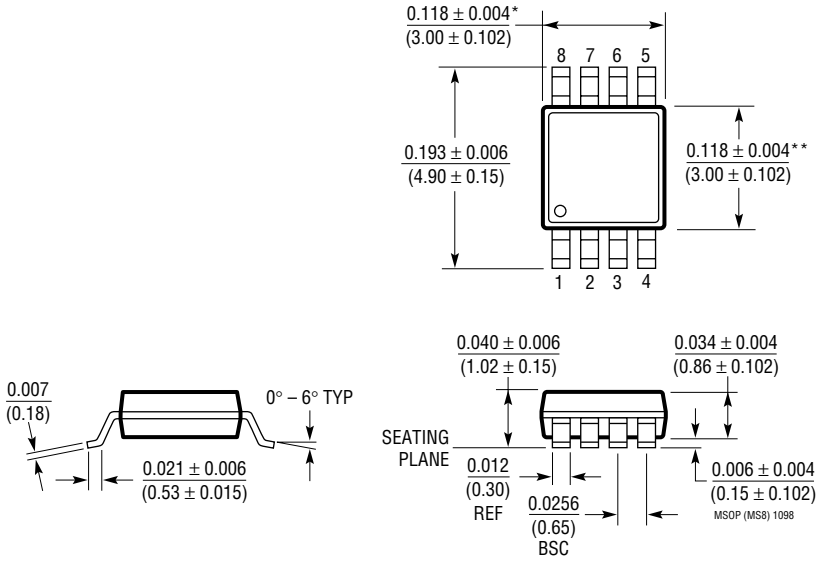


Figure 9. LTC1757A Low Frequency AC Model

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

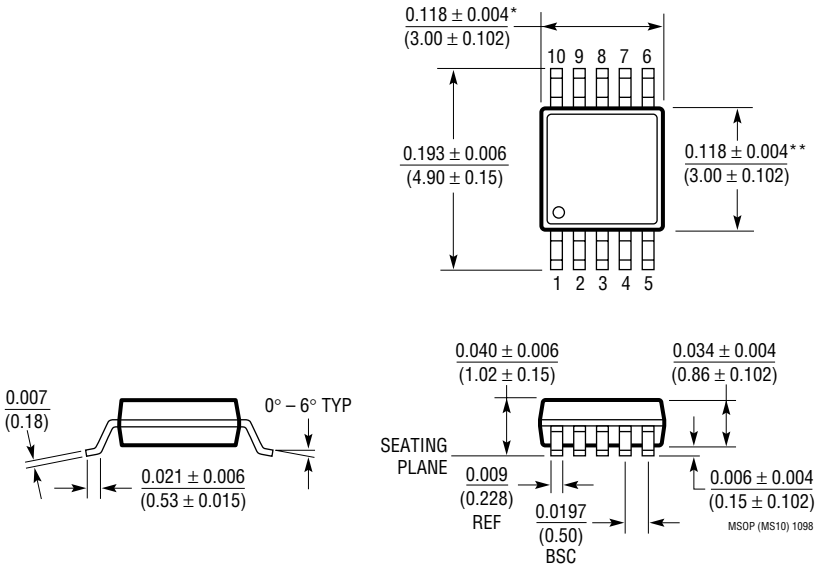
MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

MS10 Package
10-Lead Plastic MSOP
(LTC DWG # 05-08-1661)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

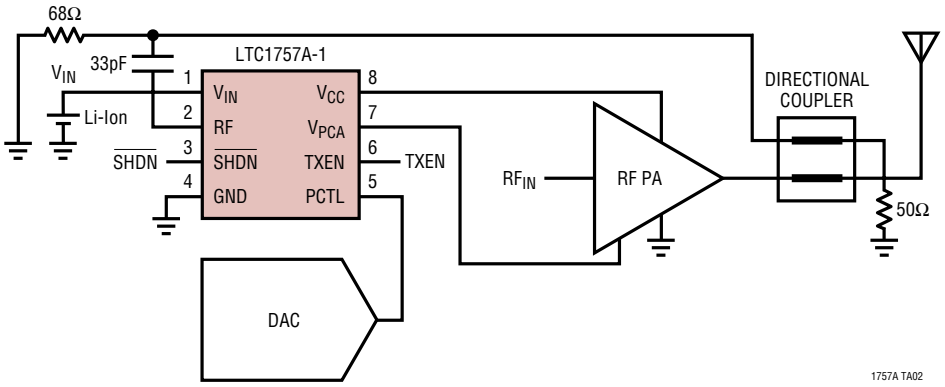
** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

LINEAR TECHNOLOGY

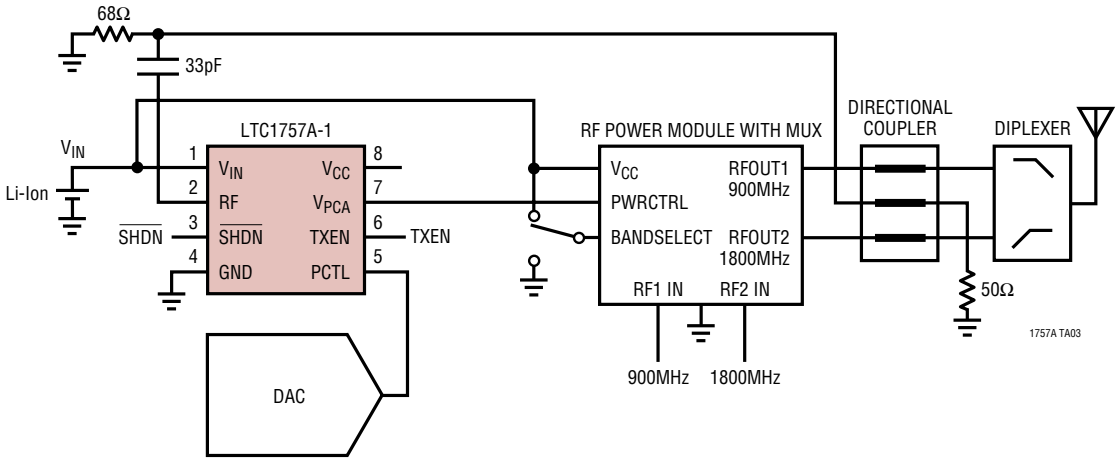
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TYPICAL APPLICATION

Single Band Cellular Telephone Transmitter



Using the LTC1757A-1 in a Dual Band Cellular Telephone Transmitter Without Current Limiting



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1261	Regulated Inductorless Voltage Inverter	Regulated –5V from 3V, REG Pin Indicates Regulation, Up to 15mA, Micropower
LTC1550/LTC1551	Low Noise Inductorless Voltage Inverter	Regulated Output, <1mV$_{P-P}$ Ripple, 900kHz
LTC1555L-1.8	SIM Card Power Supply and Level Translator	Buck/Boost Charge Pump Generates 1.8V, 3V or 5V; 30µA Quiescent Current; 2.6V ≤ V_{IN} ≤ 6V
LTC1682	Doubler Charge Pump with Low Noise Linear Regulator	1.8V ≤ V_{IN} ≤ 4.4V; Low Noise 60µV_{RMS} (100kHz BW); Ideal for backlighting
LTC1731	Li-Ion Linear Battery Charger	Small, Thin 8-Pin MSOP, Trickle Charge, EOC Indicator, 1% Accuracy
LTC3200/LTC3200-5	Low Noise, Regulated Charge Pump	2MHz Constant Frequency, I_{OUT} = 100mA, 2.7V ≤ V_{IN} ≤ 4.5V, SOT-23 and MSOP Packages

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