TDA19988

Low power, 150 MHz pixel rate HDMI 1.4a transmitter with 3 × 8-bit video inputs, HDCP and CEC support

Rev. 3 — 21 July 2011 Product data sheet

1. General description

TDA19988 is a very low power and very small size High-Definition Multimedia Interface (HDMI) 1.4a transmitter. It is backward compatible DVI 1.0 and can be connected to any DVI 1.0 or HDMI sink.

This device is primarily intended for mobile applications like Digital Video Camera (DVC), Digital Still Camera (DSC), Portable Multimedia Player (PMP), Mobile Phone and Ultra-Mobile Personal Computer (UM PC), new PC tablet and MID where size and power are key for battery autonomy.

This device is also targeting STB HDMI output applications. This part replaces previous TDA9981 Transmitters with increased features and better performances.

It allows mixing 3 × 8-bit RGB or YCbCr video stream at pixel rate up to 165 MHz together with S/PDIF or I^{2}S-bus audio streams at audio sampling rate up to 192 kHz.

In order to be compatible with most applications, TDA19988 integrates a full programmable input formatter and color space conversion block. The video input formats accepted are YCbCr 4 : 4 : 4 (up to 3 × 8-bit), YCbCr 4 : 2 : 2 semi-planar (up to 2 × 12-bit) and YCbCr 4 : 2 : 2 compliant with ITU656 (up to 1 × 12-bit). In case of ITU656-like format, the input pixel clock can be made active on one (SDR mode) or both edges (DDR mode).

TDA19988AHN and TDA19988AET only include a HDCP 1.4 compliant cipher block. The HDCP keys are stored internally in a non-volatile OTP memory for maximum security.

This device provides additional embedded features like CEC (Consumer Electronic Control). CEC is a single bidirectional bus that transmits CEC commands (like Standby from remote control) over the home appliance network connected through this bus. This eliminates the need of any additional device to handle this feature thus improving BOM (Bill Of Materials) of the whole system and enabling the connected devices (CEC enabled) to be controlled by only one remote control.

TDA19988 supports xvYCC HDMI 1.4a feature.

It can be switched to very low power Standby or Sleep modes to save power when HDMI is not used.

TDA19988 embeds I^{2}C-bus master interface for DDC-bus communication to read EDID and to manage HDCP (TDA19988AHN and TDA19988AET only).

This device can be controlled or configured via I^{2}C-bus interface.

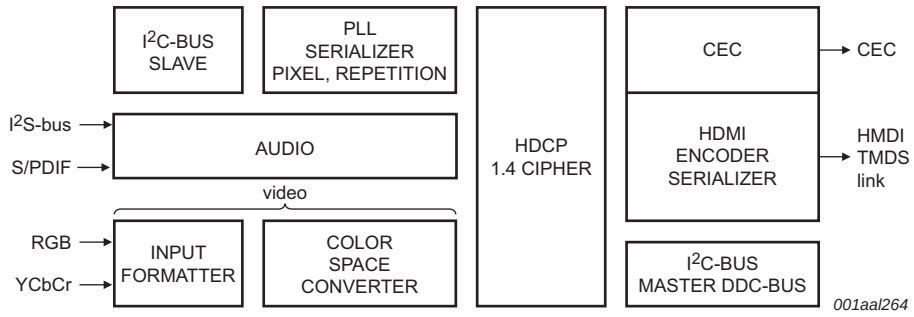

Fig 1. TDA19988 high-level block diagram

2. Features and benefits

- Compliance:
  - DVI 1.0
  - HDMI 1.4a
  - EIA/CEA-861B
  - CEC (HDMI 1.4a)
  - HDCP 1.4 (TDA19988AHN and TDA19988AET only)
- Video:
  - xvYCC HDMI 1.4a feature
  - Video formats with a pixel rate up to 165 MHz:
    RGB 4 : 4 : 4
    YCbCr 4 : 4 : 4
    YCbCr 4 : 2 : 2 semi-planar
    YCbCr 4 : 2 : 2 ITU656
  - 3D:
    Frame Packing: 720p at 50/60 Hz, 1080i at 50/60 Hz, 1080p at 24/30 Hz
    Side-by-Side (Half): 720p at 50/60 Hz, 1080i at 50/60 Hz, 1080p at 50/60 Hz
    Top-and-Bottom: 720p at 50/60 Hz, 1080i at 50/60 Hz, 1080p at 50/60 Hz
  - Maximum resolution:
    1080p at 50/60 Hz for TV
    1600 × 1200 at 60 Hz for PC (UXGA60)
    720p/1080i at 50/60 Hz in ITU656
  - Programmable color space converter:
    RGB to YCbCr
    YCbCr to RGB
  - Programmable input formatter and upsampler/interpolator allow input of any of the 4 : 4 : 4, 4 : 2 : 2 semi-planar, 4 : 2 : 2 ITU656-like formats
  - Horizontal synchronization, vertical synchronization and Data Enable (DE) inputs or VREF, HREF and FREF could be used for input data synchronization
  - In ITU656, pixel clock input can be single or dual edges (selectable by I2C-bus)
  - Repetition of video samples as required by HDMI specification
- Audio:

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- 4 × I²S-bus or one S/PDIF; audio data rate up to 192 kHz (depending on video format and on package)
- Deals with multiple levels of HDCP (TDA19988AHN and TDA19988AET only) receivers and repeaters
- Internal SHA-1 calculation
- System operation:
  - Master DDC-bus interface for EDID read
  - Controllable via I²C-bus
  - Hot Plug Detect (HPD) and receiver detection (RxSense)
- High performance power management:
  - Standby mode: 18 μW typical
  - Operation mode: 55 mW 720p 24 Hz
- Package:
  - TFBGA64, size 4.5 mm × 4.5 mm × 0.95 mm
  - HVQFN64, size 9 mm × 9 mm × 0.85 mm
- Power management:
  - External voltage supplies 1.8 V
  - Low power
  - Flexible power modes
- Miscellaneous:
  - POR (Power-On Reset)
  - Audio and video inputs LV-CMOS 1.8 V compatible and LV-CMOS 3.3 V tolerant
  - 250 MHz to 1.5 GHz TMDS transmitter operation

3. Applications

- Digital Video Camera (DVC)
- Digital Still Camera (DSC)
- Portable Multimedia Player (PMP)
- Ultra-Mobile Personal Computer (UM PC)
- YCbCr or RGB high-speed video digitizer
- Blu-ray disc player
- AVR and HDMI splitter
- MID/tablet
- Media box
- Mobile Phone
- Home theater amplifier
- STB

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TDA19988AET/C1	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls	SOT962-3

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Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
TDA19988BET/C1	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls; without HDCP	SOT962-3
TDA19988AHN/C1	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-4
TDA19988BHN/C1	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm; without HDCP	SOT804-4

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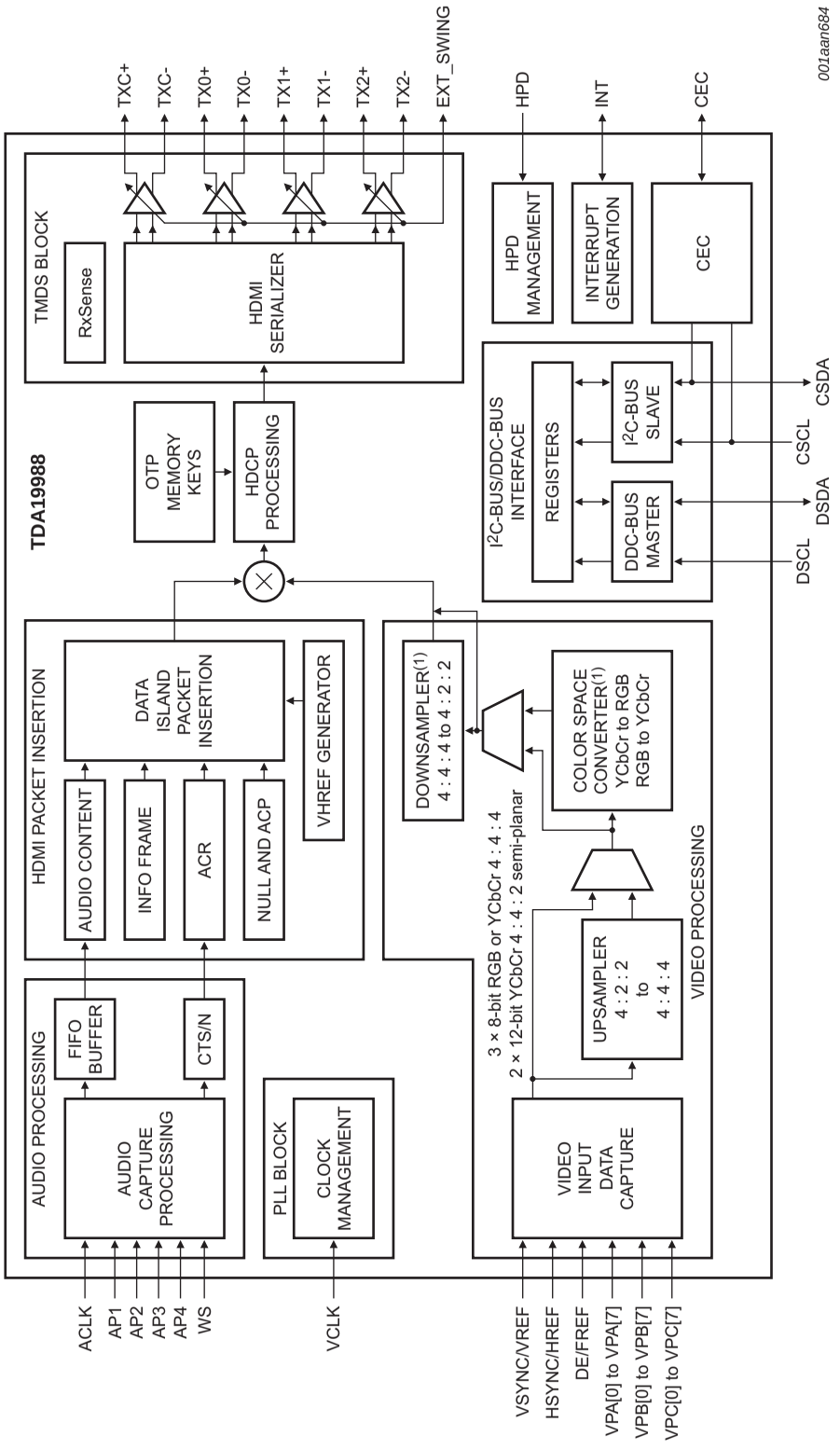
5. Block diagram



(1) The color space converter can be bypassed.
The device (TDA19988AHN and TDA19988AET only) can handle HDCP based on 1.4 features.

Fig 2. TDA19988 Block diagram

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6. Pinning information

6.1 Pinning

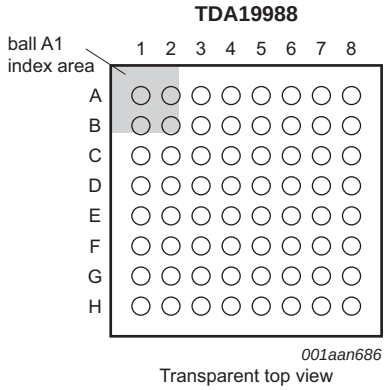

Fig 3. Pin configuration (TFBGA64)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
ACLK	H5	I	audio clock input
AP0	G5	I	audio port 0 input
AP1	F5	I	audio port 1 input
AP2	G6	I	audio port 2 input
OSC_IN/AP3	H6	I	input connected to the external oscillator circuit or external clock source/audio port 3 input
HPD	E6	I	hot plug detect; 5 V tolerant
EXT_SWING	E7	O	TMDS output swing adjustment; place resistor (R_{EXT_SWING} = 10 kΩ ± 1 %) between this pin and analog ground.
DSDA	F6	I/O	DDC-bus data input/output; 5 V tolerant
DSCL	F7	I	DDC-bus clock input; 5 V tolerant
VCLK	D4	I	input video pixel clock
HSYNC/HREF	F4	I	input horizontal synchronization or reference input
VSYNC/VREF	G4	I	input vertical synchronization or reference input
DE/FREF	H4	I	data enable or field reference input
CSCL	B5	I	I^2C-bus clock input; 1.8 V to 3.3 V tolerant
CSDA	A5	I/O	I^2C-bus data input/output; 1.8 V to 3.3 V tolerant
INT	B6	I/O	interrupt HDMI output (open-drain); this pin is used as Dual function pin selectable through I^2C-bus. In calibration mode only this pin is used as input for 10 ms ± 1 % calibration pulse. In operation mode this pin is used to warn the external microprocessor that a special event has occurred for HDMI or CEC

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Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
TX0–	E8	O	negative data channel 0 for TMDS output
TX0+	D8	O	positive data channel 0 for TMDS output
TX1–	C8	O	negative data channel 1 for TMDS output
TX1+	B8	O	positive data channel 1 for TMDS output
TX2–	A7	O	negative data channel 2 for TMDS output
TX2+	A6	O	positive data channel 2 for TMDS output
TXC–	G8	O	negative clock channel for TMDS output
TXC+	F8	O	positive clock channel for TMDS output
CEC	H7	I/O	CEC connection (open-drain) to HDMI connector
VPA[0]	C1	I	video port A input bit 0 (LSB)
VPA[1]	B1	I	video port A input bit 1
VPA[2]	B2	I	video port A input bit 2
VPA[3]	A2	I	video port A input bit 3
VPA[4]	B3	I	video port A input bit 4
VPA[5]	A3	I	video port A input bit 5
VPA[6]	B4	I	video port A input bit 6
VPA[7]	A4	I	video port A input bit 7 (MSB)
VPB[0]	E3	I	video port B input bit 0 (LSB)
VPB[1]	E2	I	video port B input bit 1
VPB[2]	E1	I	video port B input bit 2
VPB[3]	D1	I	video port B input bit 3
VPB[4]	D2	I	video port B input bit 4
VPB[5]	D3	I	video port B input bit 5
VPB[6]	C2	I	video port B input bit 6
VPB[7]	C3	I	video port B input bit 7 (MSB)
VPC[0]	H3	I	video port C input bit 0 (LSB)
VPC[1]	H2	I	video port C input bit 1
VPC[2]	G3	I	video port C input bit 2
VPC[3]	G2	I	video port C input bit 3
VPC[4]	G1	I	video port C input bit 4
VPC[5]	F1	I	video port C input bit 5
VPC[6]	F2	I	video port C input bit 6
VPC[7]	F3	I	video port C input bit 7 (MSB)
$V_{DDA(TMDS)(1V8)}$	A8, C7	P	TMDS analog supply voltage (1.8 V)
$V_{DDD(IO)(1V8)}$	E4	P	I/O digital supply voltage (1.8 V)
$V_{DDA(PLL)(1V8)}$	C6	P	PLL analog supply voltage (1.8 V), this PLL provides the clock for the serializer
$V_{DDA(1V8)}$	G7, H8	P	analog supply voltage (1.8 V), is used for the serializer and miscellaneous blocks
V_{DDDC}	E5, D5	P	core digital supply voltage (1.8 V)

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Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
V_{SSD}	B7, C4, C5, H1	G	digital ground supply voltage, is used for digital core and I/O
V_{SSA}	D6, D7	G	analog ground supply voltage, is used for PLL, serializer and transmitter
n.c.	A1		not connected

[1] P = power supply, G = ground, I = input, O = output.

6.3 Pinning

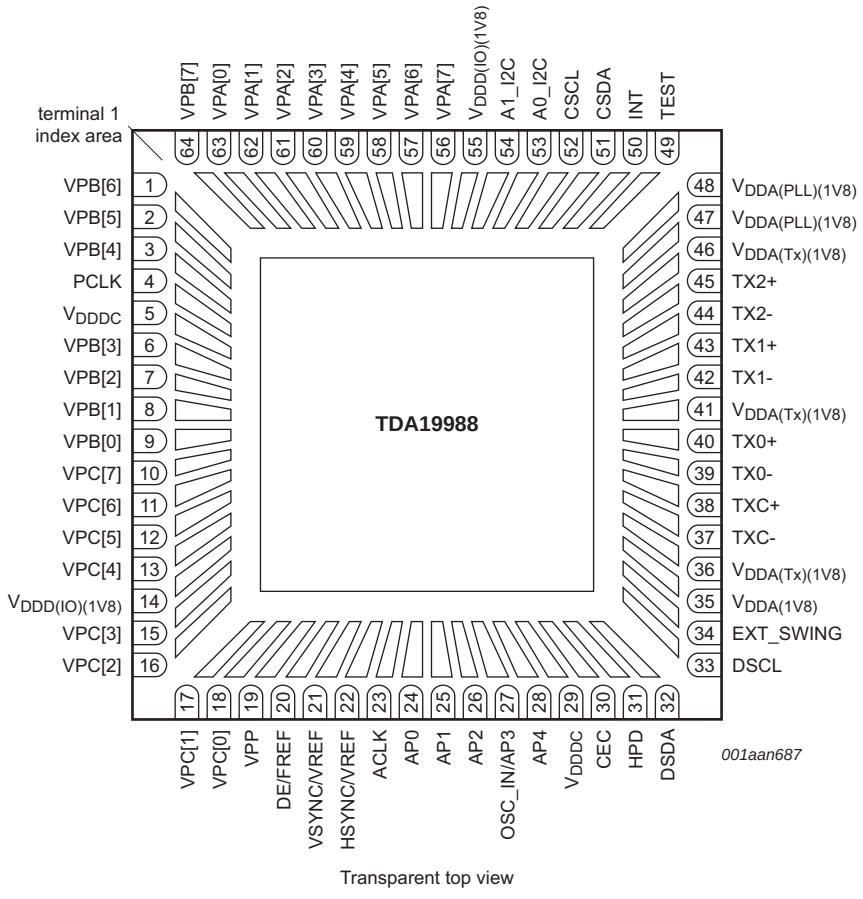

Fig 4. Pin configuration (HVQFN64)

6.4 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
VPB[6]	1	I	video port B input bit 6
VPB[5]	2	I	video port B input bit 5
VPB[4]	3	I	video port B input bit 4

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Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
PCLK	4	I	input video pixel clock
V_{DDDC}	5	P	core digital supply voltage (1.8 V)
VPB[3]	6	I	video port B input bit 3
VPB[2]	7	I	video port B input bit 2
VPB[1]	8	I	video port B input bit 1
VPB[0]	9	I	video port B input bit 0 (LSB)
VPC[7]	10	I	video port C input bit 7 (MSB)
VPC[6]	11	I	video port C input bit 6
VPC[5]	12	I	video port C input bit 5
VPC[4]	13	I	video port C input bit 4
$V_{DDD(IO)(1V8)}$	14	P	I/O digital supply voltage (1.8 V)
VPC[3]	15	I	video port C input bit 3
VPC[2]	16	I	video port C input bit 2
VPC[1]	17	I	video port C input bit 1
VPC[0]	18	I	video port C input bit 0 LSB)
VPP	19		to be connected to GND
DE/FREF	20	I	data enable or field reference input
VSYNC/VREF	21	I	input vertical synchronization or reference input
HSYNC/HREF	22	I	input horizontal synchronization or reference input
ACLK	23	I	audio clock input
AP0	24	I	audio port 0 input
AP1	25	I	audio port 1 input
AP2	26	I	audio port 2 input
OSC_IN/AP3	27	I	input connected to the external oscillator circuit or external clock source/audio port 3 input
AP4	28	I	audio port 4 input
V_{DDDC}	29	P	core digital supply voltage (1.8 V)
CEC	30	I/O	CEC connection (open-drain) to HDMI connector
HPD	31	I	hot plug detect; 5 V tolerant
DSDA	32	I/O	DDC-bus data input/output; 5 V tolerant
DSCL	33	I	DDC-bus clock input; 5 V tolerant
EXT_SWING	34	O	TMDS output swing adjustment; place resistor (R_{EXT_SWING} = 10 kΩ ± 1 %) between this pin and analog ground.
$V_{DDA(1V8)}$	35	P	analog supply voltage (1.8 V), is used for parallel-to-serial shift register and miscellaneous blocks
$V_{DDA(Tx)(1V8)}$	36	P	Tx analog supply voltage (1.8 V)
TXC–	37	O	negative clock channel for TMDS output
TXC+	38	O	positive clock channel for TMDS output
TX0–	39	O	negative data channel 0 for TMDS output
TX0+	40	O	positive data channel 0 for TMDS output
$V_{DDA(Tx)(1V8)}$	41	P	Tx analog supply voltage (1.8 V)

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Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
TX1–	42	O	negative data channel 1 for TMDS output
TX1+	43	O	positive data channel 1 for TMDS output
TX2–	44	O	negative data channel 2 for TMDS output
TX2+	45	O	positive data channel 2 for TMDS output
$V_{DDA(Tx)(1V8)}$	46	P	Tx analog supply voltage (1.8 V)
$V_{DDA(PLL)(1V8)}$	47	P	PLL analog supply voltage (1.8 V), this PLL provides the clock for the serializer
$V_{DDA(PLL)(1V8)}$	48	P	PLL analog supply voltage (1.8 V), this PLL provides the clock for the serializer
TEST	49		to be connected to GND
INT	50	I/O	interrupt HDMI output (open-drain); this pin is used as Dual function pin selectable through I^2C-bus. In calibration mode only this pin is used as input for 10 ms ± 1 % calibration pulse. In operation mode this pin is used to warn the external microprocessor that a special event has occurred for HDMI or CEC
CSDA	51	I/O	I^2C-bus data input/output; 1.8 V to 3.3 V tolerant
CSCL	52	I	I^2C-bus clock input; 1.8 V to 3.3 V tolerant
A0_I2C	53	I	I^2C-bus address LSB bit 0
A1_I2C	54	I	I^2C-bus address LSB bit 1
$V_{DDD(IO)(1V8)}$	55	P	I/O digital supply voltage (1.8 V)
VPA[7]	56	I	video port A input bit 7 (MSB)
VPA[6]	57	I	video port A input bit 6
VPA[5]	58	I	video port A input bit 5
VPA[4]	59	I	video port A input bit 4)
VPA[3]	60	I	video port A input bit 3
VPA[2]	61	I	video port A input bit 2
VPA[1]	62	I	video port A input bit 1
VPA[0]	63	I	video port A input bit 0 (LSB)
VPB[7]	64	I	video port B input bit 7 (MSB)
Exposed die pad	-	G	exposed die pad; must be connected to ground

[1] P = power supply, G = ground, I = input, O = output.

7. Functional description

TDA19988 is designed to convert digital data (video and audio) provided by Set-Top Boxes (STB), Digital Video Camera (DVC), Digital Still Camera (DSC), Portable Multimedia Player (PMP) or DVD into an HDMI output, connected to HDMI or DVI input of a TV.

The video data input formats are:

- RGB 4 : 4 : 4
- YCbCr 4 : 4 : 4

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- YCbCr 4 : 2 : 2 semi-planar
- YCbCr 4 : 2 : 2 ITU656-like

TDA19988 is able to output HDMI with the formats:

- RGB 4 : 4 : 4
- YCbCr 4 : 4 : 4
- YCbCr 4 : 2 : 2

It can also handle audio formats:

- four I^2S-bus lanes
- one S/PDIF lane

TDA19988 is also designed to support CEC protocol. For more details about CEC, refer to *HDMI specification 1.4a*.

7.1 System clock

The system clock section has a PLL serializer.

It is a system clock generator which enables the stream produced by the encoder to be transmitted on the HDMI data channel at ten times, or above, the sampling rate.

7.2 Video input formatter

7.2.1 Description

TDA19988 has three video input ports VPA[0] to VPA[7], VPB[0] to VPB[7] and VPC[0] to VPC[7].

TDA19988 can accept any of the following video input modes (see Table 7):

- RGB, with 8-bit for each component
- YCbCr 4 : 4 : 4, with 8-bit for each component
- YCbCr 4 : 2 : 2 semi-planar, with up to 12-bit for each component (YCbCr)
- YCbCr 4 : 2 : 2 ITU656, with up to 12-bit data depth

TDA19988 can be set to latch data at either rising or falling edge, or both.

7.2.2 Internal assignment

All video interfaces can be affected according to application requirements by swapping or allocating the 24-input VP ports to internal 24-video bus by block of 4-bit.

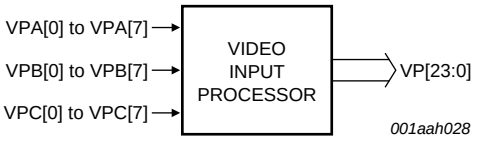

Fig 5. Internal assignment of VP[23:0]

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Table 4. Internal assignment

Internal assignment				
Internal port	**RGB**	**YCbCr 4 : 4 : 4**	**YCbCr 4 : 2 : 2 semi-planar**	**YCbCr 4 : 2 : 2 ITU656**
VP[23]	G[7]	Y[7]	Y[11]	YCbCr[11]
VP[22]	G[6]	Y[6]	Y[10]	YCbCr[10]
VP[21]	G[5]	Y[5]	Y[9]	YCbCr[9]
VP[20]	G[4]	Y[4]	Y[8]	YCbCr[8]
VP[19]	G[3]	Y[3]	Y[7]	YCbCr[7]
VP[18]	G[2]	Y[2]	Y[6]	YCbCr[6]
VP[17]	G[1]	Y[1]	Y[5]	YCbCr[5]
VP[16]	G[0]	Y[0]	Y[4]	YCbCr[4]
VP[15]	B[7]	Cb[7]	Y[3]	YCbCr[3]
VP[14]	B[6]	Cb[6]	Y[2]	YCbCr[2]
VP[13]	B[5]	Cb[5]	Y[1]	YCbCr[1]
VP[12]	B[4]	Cb[4]	Y[0]	YCbCr[0]
VP[11]	B[3]	Cb[3]	CbCr[11]	
VP[10]	B[2]	Cb[2]	CbCr[10]	
VP[9]	B[1]	Cb[1]	CbCr[9]	
VP[8]	B[0]	Cb[0]	CbCr[8]	
VP[7]	R[7]	Cr[7]	CbCr[7]	
VP[6]	R[6]	Cr[6]	CbCr[6]	
VP[5]	R[5]	Cr[5]	CbCr[5]	
VP[4]	R[4]	Cr[4]	CbCr[4]	
VP[3]	R[3]	Cr[3]	CbCr[3]	
VP[2]	R[2]	Cr[2]	CbCr[2]	
VP[1]	R[1]	Cr[1]	CbCr[1]	
VP[0]	R[0]	Cr[0]	CbCr[0]	

The device can swap and invert incoming video data using I^2C-bus registers VIP_CNTRL_0, VIP_CNTRL_1 and VIP_CNTRL_2 to match the expectation of the video processing block.

Table 5 shows the behavior of SWAP_A[2:0] of VIP_CNTRL_0 register, whose function is to map the 4 MSBs VP[23:20] to incoming video port

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Table 5. Video input swap to VP[23:20]

External assignment		SWAP_A[2:0] selector value	Internal assignment								
Pin number[1]	Pin name		Internal port	RGB	YCbCr 4 : 4 : 4	YCbCr 4 : 2 : 2 semi-planar		YCbCr 4 : 2 : 2 ITU656			
F3	VPC[7]	000b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
F2	VPC[6]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
F1	VPC[5]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
G1	VPC[4]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
G2	VPC[3]	001b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
G3	VPC[2]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
H2	VPC[1]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
H3	VPC[0]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
C3	VPB[7]	010b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
C2	VPB[6]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
D3	VPB[5]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
D2	VPB[4]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
D1	VPB[3]	011b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
E1	VPB[2]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
E2	VPB[1]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
E3	VPB[0]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
A4	VPA[7]	100b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
B4	VPA[6]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
A3	VPA[5]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
B3	VPA[4]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
A2	VPA[3]	101b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
B2	VPA[2]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
B1	VPA[1]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
C1	VPA[0]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]

[1] Only for TFBGA package.

In the same way:

- SWAP_B[2:0] is used to map incoming video port to the internal port VP[19:16].
- SWAP_C[2:0] is used to map incoming video port to the internal port VP[15:12].
- SWAP_D[2:0] is used to map incoming video port to the internal port VP[11:8].
- SWAP_E[2:0] is used to map incoming video port to the internal port VP[7:4].
- SWAP_F[2:0] is used to map incoming video port to the internal port VP[3:0].

The device expects to receive big endian incoming data. However, in cases where the input digital stream to the chip is little endian, the use of the mirror bit of the same register can help to re-order the input bits as described in Table 6.

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Table 6. TDA19988 input/output capability

Bit setting	Internal port	To be mapped to
MIRR_A = 1 SWAP_A[2:0] = 1	VP[23]	VPC[0]
	VP[22]	VPC[1]
	VP[21]	VPC[2]
	VP[20]	VPC[3]
MIRR_B = 1 SWAP_B[2:0] = 0	VP[19]	VPC[4]
	VP[18]	VPC[5]
	VP[17]	VPC[6]
	VP[16]	VPC[7]
MIRR_C = 1 SWAP_C[2:0] = 3	VP[15]	VPB[0]
	VP[14]	VPB[1]
	VP[13]	VPB[2]
	VP[12]	VPB[3]
MIRR_D = 1 SWAP_D[2:0] = 2	VP[11]	VPB[4]
	VP[10]	VPB[5]
	VP[9]	VPB[6]
	VP[8]	VPB[7]
MIRR_E = 1 SWAP_E[2:0] = 5	VP[7]	VPA[0]
	VP[6]	VPA[1]
	VP[5]	VPA[2]
	VP[4]	VPA[3]
MIRR_F = 1 SWAP_F[2:0] = 4	VP[3]	VPA[4]
	VP[2]	VPA[5]
	VP[1]	VPA[6]
	VP[0]	VPA[7]

Remark: Unused input port can be set in 3-state or grounded by using appropriate configuration.

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7.2.3 Input format mappings

Table 7 gives more information concerning input format supported.

Table 7. Inputs of video input formatter

Color space	Format	Channels	Sync type	Rising edge	Falling edge	Double edge	Transmission input format	Max. pixel clock (MHz)	Max. input format	Comments	Reference
RGB	4 : 4 : 4	3 × 8-bit	external	X			-	165	-		Section 7.2.3.1
					X		-	165	-		
			embedded	X			-	165	-		
					X		-	165	-		
YCbCr	4 : 4 : 4	3 × 8-bit	external	X			-	165	-		Section 7.2.3.2
					X		-	165	-		
			embedded	X			-	165	-		
					X		-	165	-		
YCbCr	4 : 2 : 2	up to 1 × 12-bit ITU656-like	external	X			ITU656-like	54.054	480p/576p		Section 7.2.3.3
								148.5	720p/1080i		
					X		ITU656-like	54.054	480p/576p		
								148.5	720p/1080i		
						X	ITU656-like	74.25	720p/1080i	double edge	Section 7.2.3.4
			embedded	X			ITU656-like	54.054	480p/576p		Section 7.2.3.5
								148.5	720p/1080i		
					X		ITU656-like	54.054	480p/576p		
								148.5	720p/1080i		
						X	ITU656-like	74.25	720p/1080i	double edge	Section 7.2.3.6
		up to 2 × 12-bit semi-planar	external	X			SMPTE293M	148.5	1080p		Section 7.2.3.7
					X		SMPTE293M	148.5	1080p		
			embedded	X			SMPTE293M	148.5	1080p		Section 7.2.3.8
					X		SMPTE293M	148.5	1080p		

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For all formats, active video windows can be selected using either external DE signal or internal timing generator engine.

7.2.3.1 RGB 4 : 4 : 4 external synchronization (rising edge)

Table 8. RGB (3 × 8-bit) external synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**
VPA[0]	B[0]	VPB[0]	G[0]	VPC[0]	R[0]	HSYNC/HREF	used
VPA[1]	B[1]	VPB[1]	G[1]	VPC[1]	R[1]	VSYNC/VREF	used
VPA[2]	B[2]	VPB[2]	G[2]	VPC[2]	R[2]	DE/FREF	used
VPA[3]	B[3]	VPB[3]	G[3]	VPC[3]	R[3]		
VPA[4]	B[4]	VPB[4]	G[4]	VPC[4]	R[4]		
VPA[5]	B[5]	VPB[5]	G[5]	VPC[5]	R[5]		
VPA[6]	B[6]	VPB[6]	G[6]	VPC[6]	R[6]		
VPA[7]	B[7]	VPB[7]	G[7]	VPC[7]	R[7]		

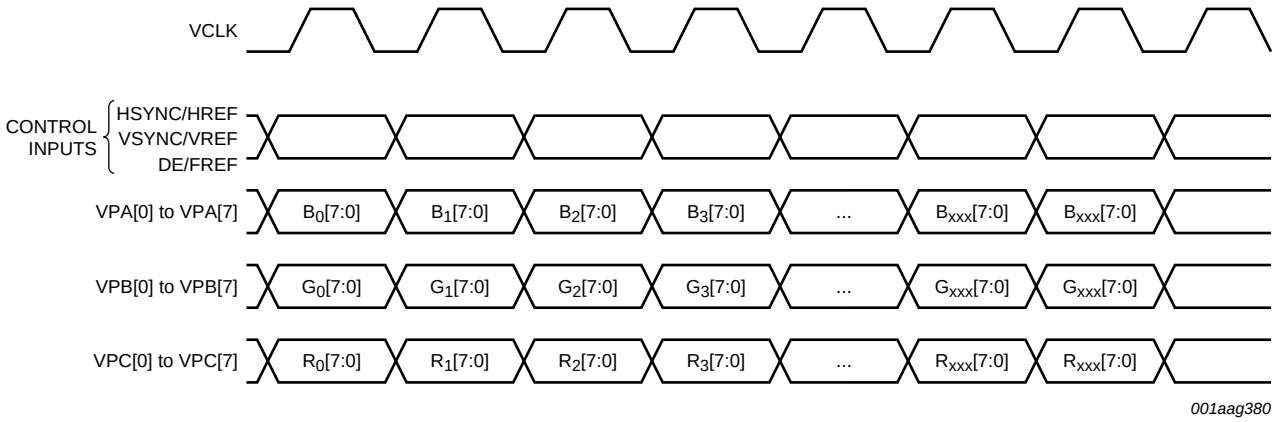

Fig 6. Pixel encoding RGB 4 : 4 : 4 external synchronization input (rising edge)

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7.2.3.2 YCbCr 4 : 4 : 4 external synchronization (rising edge)

Table 9. YCbCr 4 : 4 : 4 (3 × 8-bit) external synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**
VPA[0]	Cb[0]	VPB[0]	Y[0]	VPC[0]	Cr[0]	HSYNC/HREF	used
VPA[1]	Cb[1]	VPB[1]	Y[1]	VPC[1]	Cr[1]	VSYNC/VREF	used
VPA[2]	Cb[2]	VPB[2]	Y[2]	VPC[2]	Cr[2]	DE/FREF	used
VPA[3]	Cb[3]	VPB[3]	Y[3]	VPC[3]	Cr[3]		
VPA[4]	Cb[4]	VPB[4]	Y[4]	VPC[4]	Cr[4]		
VPA[5]	Cb[5]	VPB[5]	Y[5]	VPC[5]	Cr[5]		
VPA[6]	Cb[6]	VPB[6]	Y[6]	VPC[6]	Cr[6]		
VPA[7]	Cb[7]	VPB[7]	Y[7]	VPC[7]	Cr[7]		

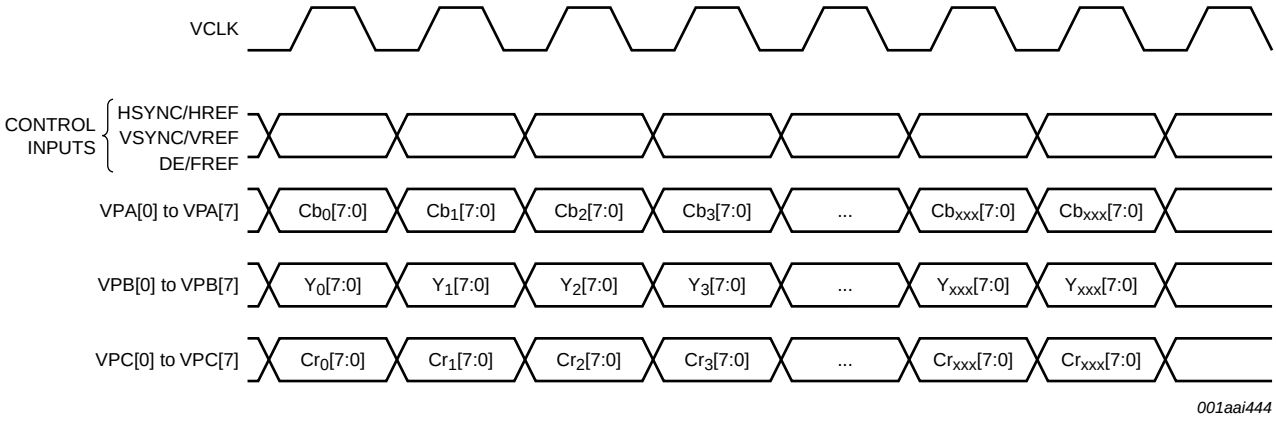

Fig 7. Pixel encoding YCbCr 4 : 4 : 4 external synchronization input (rising edge)

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7.2.3.3 YCbCr 4 : 2 : 2 ITU656-like external synchronization (rising edge)

Table 10. YCbCr 4 : 2 : 2 ITU656-like external synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

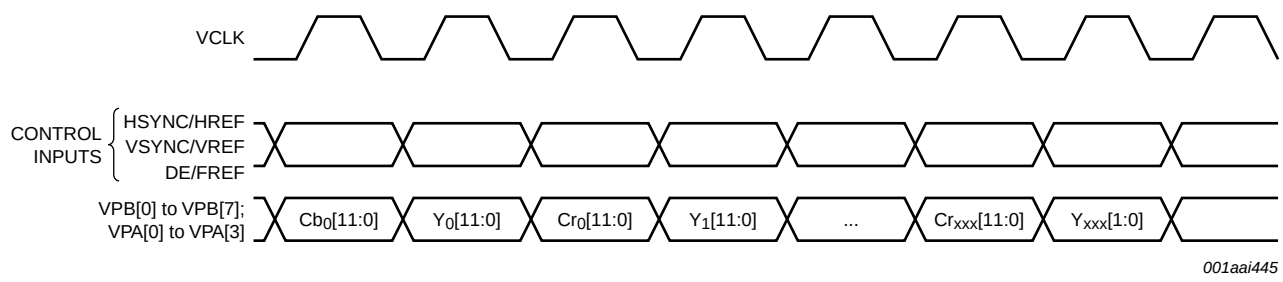

Fig 8. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like external synchronization input (rising edge)

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7.2.3.4 YCbCr 4 : 2 : 2 ITU656-like external synchronization (double edge)

Table 11. YCbCr 4 : 2 : 2 ITU656-like external synchronization input (double edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

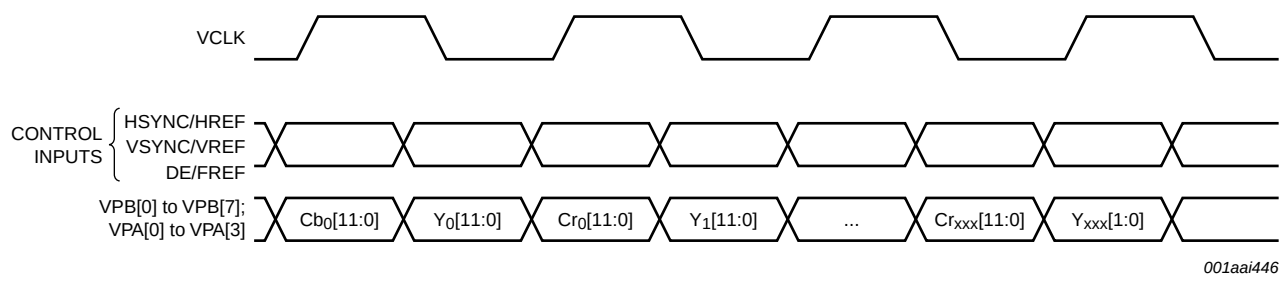

Fig 9. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like external synchronization input (double edge)

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7.2.3.5 YCbCr 4 : 2 : 2 ITU656-like embedded synchronization (rising edge)

Table 12. YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (rising edge) mappings

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	not used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

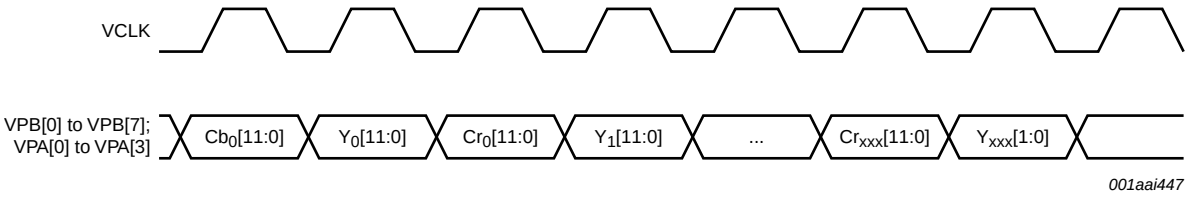

Fig 10. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (rising edge)

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7.2.3.6 YCbCr 4 : 2 : 2 ITU656-like embedded synchronization (double edge)

Table 13. YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (double edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	not used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

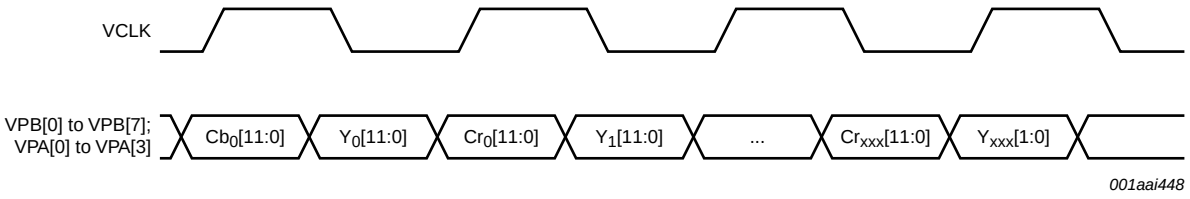

Fig 11. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (double edge)

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7.2.3.7 YCbCr 4 : 2 : 2 semi-planar external synchronization (rising edge)

Table 14. YCbCr 4 : 2 : 2 semi-planar external synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	Cb[4]	Cr[4]	HSYNC/HREF	used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	Cb[5]	Cr[5]	VSYNC/VREF	used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	Cb[6]	Cr[6]	DE/FREF	used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	Cb[7]	Cr[7]		
VPA[4]	Cb[0]	Cr[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	Cb[8]	Cr[8]		
VPA[5]	Cb[1]	Cr[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	Cb[9]	Cr[9]		
VPA[6]	Cb[2]	Cr[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	Cb[10]	Cr[10]		
VPA[7]	Cb[3]	Cr[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	Cb[11]	Cr[11]		

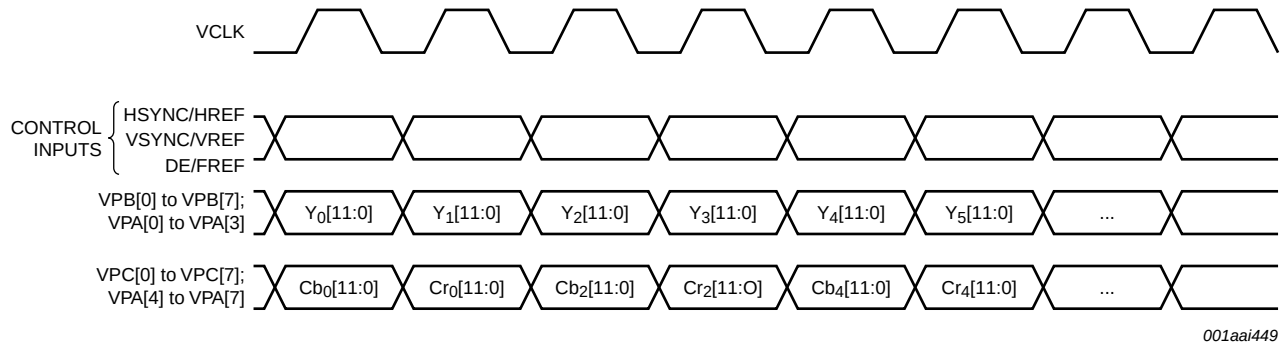

Fig 12. Pixel encoding YCbCr 4 : 2 : 2 semi-planar external input synchronization (rising edge)

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7.2.3.8 YCbCr 4 : 2 : 2 semi-planar embedded synchronization (rising edge)

Table 15. YCbCr 4 : 2 : 2 semi-planar embedded synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	Cb[4]	Cr[4]	HSYNC/HREF	not used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	Cb[5]	Cr[5]	VSYNC/VREF	not used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	Cb[6]	Cr[6]	DE/FREF	not used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	Cb[7]	Cr[7]		
VPA[4]	Cb[0]	Cr[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	Cb[8]	Cr[8]		
VPA[5]	Cb[1]	Cr[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	Cb[9]	Cr[9]		
VPA[6]	Cb[2]	Cr[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	Cb[10]	Cr[10]		
VPA[7]	Cb[3]	Cr[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	Cb[11]	Cr[11]		

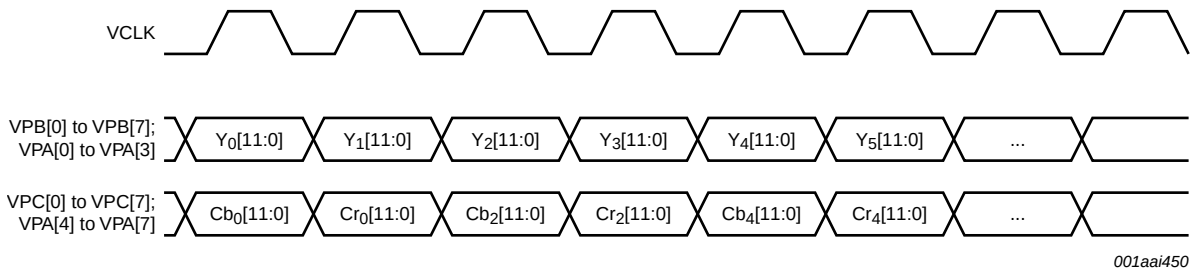

Fig 13. Pixel encoding YCbCr 4 : 2 : 2 semi-planar embedded synchronization input (rising edge)

7.2.4 Synchronization

TDA19988 can be synchronized with extraction of the sync information from embedded sync (SAV/EAV) codes inside the video stream or with external HSYNC/VSYNC inputs.

7.2.4.1 Timing extraction generator

Synchronization signals can be extracted from Start Active Video (SAV) and End Active Video (EAV) in case of embedded synchronization in the data stream.

Synchronization signals can be embedded or external.

7.2.4.2 Data enable generator

TDA19988 contains a Data Enable (DE) generator; this can generate an internal DE signal for a system which does not provide one.

7.3 Input and output video format

Thanks to the flexible video input formatter, TDA19988 can accept a large range of input formats. This flexibility allows TDA19988 to be compatible with the maximum possible number of audio/video processors. Moreover, these input formats may be changed in many ways (color space converter, upsampler, downsampler) before it is transmitted across the HDMI link. Table 16 gives the possible inputs and outputs.

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Table 16. Use of color space converter, upsampler and downsampler

Input			Output		
Color space	**Format**	**Channels**	**Color space**	**Format**	**Channels**
RGB	4 : 4 : 4	3 × 8-bit	RGB	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 2 : 2	2 × 12-bit
YCbCr	4 : 4 : 4	3 × 8-bit	RGB	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 2 : 2	2 × 12-bit
YCbCr	4 : 2 : 2	up to 2 × 12-bit semi-planar	RGB	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 2 : 2	2 × 12-bit
YCbCr	4 : 2 : 2	up to 1 × 12-bit ITU656	RGB	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 2 : 2	2 × 12-bit

7.4 Upsampler

The incoming YCbCr 4 : 2 : 2 (2 × 12-bit) data stream format may be upsampled into YCbCr 4 : 4 : 4 (3 × 8-bit) data stream by repeating or linearly interpolating the chrominance pixels.

7.5 Color space converter

The color space converter is used to convert input video data from one type to another color space (e.g. RGB to YCbCr and YCbCr to RGB). This block can be bypassed and each coefficient is programmable via the I^2C-bus register.

$$\begin{bmatrix} Y\backslash G \\ Cr\backslash R \\ Cb\backslash B \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left(\begin{bmatrix} Y \\ R/Cr \\ B/Cb \end{bmatrix} + \begin{bmatrix} Oin_{G/Y} \\ Oin_{R/Cr} \\ Oin_{B/Cb} \end{bmatrix} \right) + \begin{bmatrix} Oout_{Y\backslash G} \\ Oout_{Cr\backslash R} \\ Oout_{Cb\backslash B} \end{bmatrix} \quad (1)$$

7.6 Gamut-related metadata

Gamut-related metadata is an enhanced colorimetry beyond the default standard with higher definition colorimetries. Profile P0 is supported, which means that only one packet per video field is sent.

Examples:

- xvYCC601 (IEC 61966-2-4 – SD) (using YCbCr)
- xvYCC709 (IEC 61966-2-4 – HD) (using YCbCr)
- AdobeYCC601 (IEC 61966-2-5) (using YCbCr)
- AdobeRGB (IEC 61966-2-5) (using RGB)

Remark: Gamut-related metadata is an HDMI 1.4a feature.

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7.7 Downsampler

This block works only with YCbCr input format; the filters downsample the Cb and Cr signals by a factor of 2. A delay is added on the Y channel, which corresponds to the pipeline delay of the filters, to put the Y channel in phase with the Cb-Cr channel.

7.8 Audio input format

TDA19988 is compatible with the following audio features described in the *"HDMI specification 1.4a"*:

- S/PDIF
- I²S-bus up to four stereo channels (depending on package)

TDA19988 can carry audio in I²S-bus format (one stereo to four stereo channels) or in S/PDIF format through audio pins named AP1, AP2, AP3 and AP4 (depending on package). S/PDIF or I²S-bus format can be selected via the I²C-bus. Only one audio format can be used at a time: either S/PDIF or I²S-bus. Table 17 shows the audio port allocation and Section 7.8.3 gives more details.

Table 17. Audio port configuration

Audio port	Input configuration	
	S/PDIF	I²S-bus
AP0	-	WS (word select)
AP1	S/PDIF input	I²S-bus channel 0
AP2	S/PDIF input	I²S-bus channel 1
AP3[1]		I²S-bus channel 2
AP4[1]		I²S-bus channel 3
ACLK	-	SCK (I²S-bus clock)

[1] Depending on package.

All audio ports are LV-CMOS 1.8 V compatible and LV-CMOS 3.3 V tolerant. It is possible to deactivate unused ports via I²C-bus with ENA_AP register on page 00h for both audio and clock inputs.

7.8.1 S/PDIF

In this format TDA19988 supports 2-channel uncompressed PCM data (IEC 60958) layout 0, or compressed bit stream (Dolby Digital, DTS, AC3 etc.) layout 1.

Only one S/PDIF input can be used at the same time. The selection is done by register.

TDA19988 is able to recover the original clock from the S/PDIF signal (no need of external clock). In addition, it can also use an external clock to decode the S/PDIF signal.

7.8.2 I²S-bus

There are 2 × I²S-bus or 4 × I²S-bus (depending on package) stereo input, which enables 4 or 8 (depending on package) PCM channels to be carried. The I²S-bus input interface receives an I²S-bus signal including serial data, word select and serial clock.

Typical waveforms for the I²S-bus signals at $64f_s$ are given by Figure 14.

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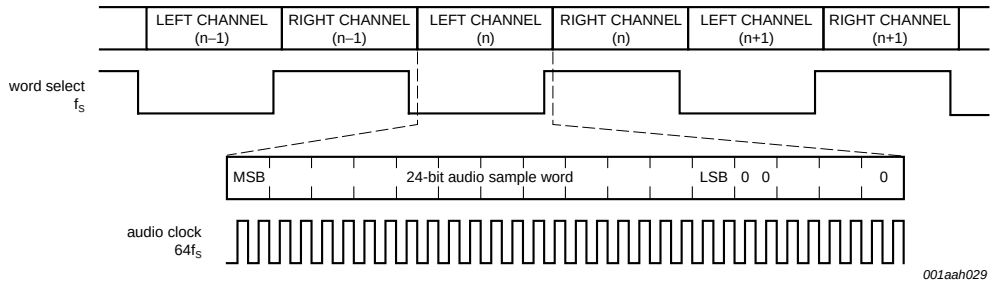
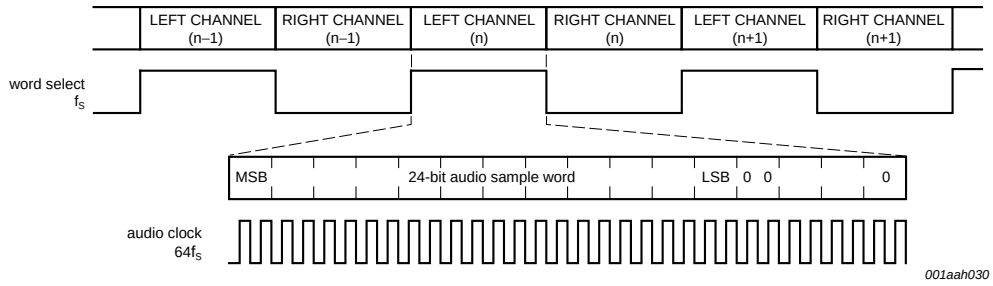
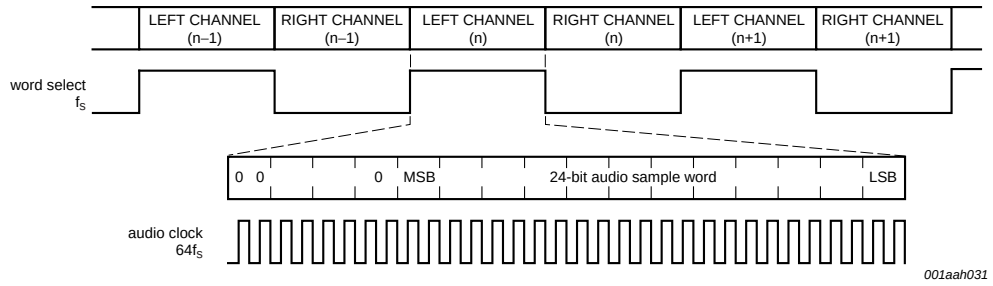


a. Philips format.



b. Left justified format.



c. Right justified format.

Fig 14. I^2S-bus formats

The I^2S-bus input interface can receive up to 24-bit wide audio samples via the serial data input with a clock frequency of at least 32 times the input sample frequency f_S.

Audio samples with a precision better than 24-bit are truncated to 24-bit. If the input clock has a frequency of $32f_S$, only 16-bit audio-samples can be received. In this case, the 8 LSBs will be set to 0. If the input clock has a frequency of $64f_S$ and is left justified or Philips, the audio word is truncated to 24-bit format and other bits padded with zeros. If the input clock has a frequency of $64f_S$ and is right justified, audio sample size has to be specified via software drivers.

The serial data signal carries the serial baseband audio data, sample by sample left/right interleaved.

The word select signal indicates whether left or right channel information is transferred over the serial data line.

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7.8.3 Audio port internal assignment

The aim of the internal audio input assignment is to internally map any of the incoming data from the audio port AP1, AP2 to S/PDIF internal ports by setting the appropriate I²C-bus register.

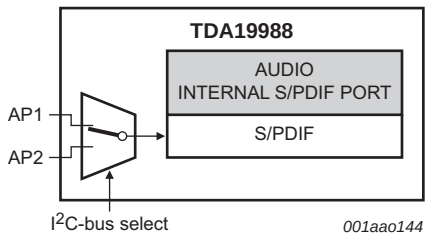

Fig 15. Audio input swap to S/PDIF

7.9 Power management

TDA19988 HDMI and CEC cores can be independently powered down by the I²C-bus register. In Standby mode all activities are reduced by switching off all PLLs, HDMI and CEC cores and disconnecting the biasing structure of the output stage. TDA19988 has a very low power consumption, which is suitable for portable applications.

Table 18 gives the typical power consumption of the device in different configurations.

Table 18. TDA19988 typical power consumption in different configurations

Typical power	Configuration	Comment
18 μW	Standby mode:	default configuration: after power-up; PLLs HDMI and CEC cores are OFF; can be switched ON via I²C-bus register
	• I²C-bus ON	
	• HDMI interruption (HPD, RxSense only)	
0.9 mW	Sleep mode without CEC:	no sink connected; CEC is OFF
	• HDMI interruption (HPD, RxSense only)	
1.3 mW	Sleep mode with CEC:	no sink connected; CEC is ON
	• HDMI interruption (HPD, RxSense only)	
	• CEC interruption	
60 mW	Operation mode:	sink connected; 30 % activity on video input ports
	• Video format 720p/1080i	
	• Video input RGB 24-bit	
95 mW	Full speed mode:	30 % activity on video input ports
	• Video format 1080p	
	• Video input RGB 24-bit	

In both Standby and Sleep modes, all video and audio pins are equivalent to high-impedance.

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7.10 Interrupt controller

Pin INT is used to alert the system microcontroller that a critical event concerning the HDMI or CEC has occurred. The software provided with the device read a status register (I^2C-bus) to determine which block between HDMI and CEC has caused the interruption before processing it. Some of theses interrupts are maskable. The interrupt types are described in Table 19.

Table 19. Interruptions

Interrupt domain	Interrupt name	Definition	Maskable feature
HDCP	r0	r0 = R'0 check done	maskable
	pj	pj = P'j check fails	
	sha-1	V = V' check success	
	bstatus	bstatus available	
	bcaps	bcaps available	
	t0	error in HDCP state machine	
HPD	hpd	transition on HPD input	maskable
RxSense	rx_sense	transition on RxSense	maskable
Interrupt	sw_intsoftware	test purpose (output an interrupt signal)	maskable
EDID	edid_block_rd	EDID block read finished	maskable
CEC	cec_int	CEC message received	not maskable

7.10.1 Hot plug/unplug detect

The Hot Plug Detect (HPD) pin is 5 V input tolerant. The HPD signal, when asserted, tells the transmitter that the receiver is connected. When changing from LOW-to-HIGH, TDA19988 has to read the EDID of the receiver in order to select video format that the receiver can handle.

7.10.2 Receiver sensitivity

TDA19988 has the capability to sense the receiver connectivity and working behavior. This feature (RxSense) detects the presence of the 50 Ω pull-up resistor R_T on the TMDS clock channel of the downstream side.

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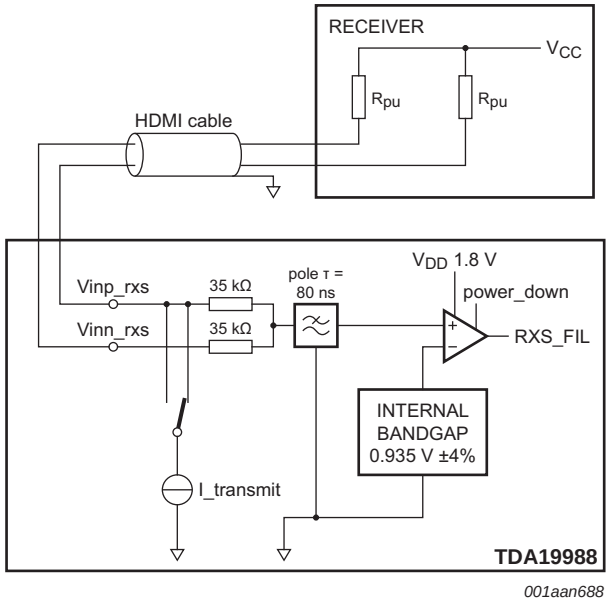

Fig 16. Receiver sensitivity detection

As long as the receiver is connected to the transmitter and powered-up, bit RXS_FIL is set to logic 1.

As soon as the cable is unplugged or receiver side powered off (assuming in this case that V_{CC} is switched off), the RxSense generates an interrupt inside TDA19988, changing the value of bit RXS_FIL to logic 0 (See Table 20). This allows the application to stop sending unnecessary video content.

This feature is very useful when the receiver recovers from an off-state and does not generate a HPD transition HIGH-to-LOW-to-HIGH. In this particular case, RxSense will generate an interrupt so that the chip restarts sending video.

Table 20. Receiver detection according to averaged terminal voltage

Average voltage (Vinp_rxs + Vinn_rxs) / 2	bit RXS_FIL: receiver powered on	bit RXS_FIL: receiver powered off
$V \geq 1.2$ V	1	0
0.7 V < V < 1.2 V	undefined	0
$V \leq 0.7$ V	0	0

Remark: According to the HDMI specification, only the HPD interrupt allows the application to read the EDID. The RxSense interrupt is not mandatory to initialize the EDID reading procedure.

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7.11 HDCP processing (TDA19988AHN and TDA19988AET only)

7.11.1 High-bandwidth digital content protection

TDA19988AHN and TDA19988AET contain an HDCP function, which encrypts the transmitted stream content (both video and audio). This function can be enabled and disabled via the I^2C-bus.

The keys are stored internally in OTP non-volatile memory for maximum security.

7.11.1.1 Repeater function

TDA19988AHN and TDA19988AET can be used in a repeater device according to the *HDCP specification, Rev 1.4*. TDA19988AHN and TDA19988AET are able to store the KSV list of a maximum of 127 devices in a register memory.

7.11.1.2 SHA-1

To deal with repeater, a SHA-1 calculation is performed by the transmitter and by the downstream repeater. For security purposes and in order to relieve the microcontroller, the SHA-1 has been implemented within TDA19988.

This calculation is worked out after the transmitter has loaded the KSV list (see *HDCP specification, Rev 1.4*). If SHA-1 calculated by transmitter equals the SHA-1 calculated by repeater, then an interrupt is sent.

7.12 CEC

TDA19988 with its embedded CEC block provides a complete solution to enable Consumer Electronic Control (CEC) in product (DSC, DVC, PMP, UM PC). This eliminates the need of any additional device to handle this feature thus improving BOM (Bill Of Materials). CEC capability allows AV products (CEC enable) to communicate together over the home appliance network which could be controlled using only one remote control.

The CEC block manages low level transactions (compliant to CEC timing specification) over the one bidirectional line. It translates CEC protocol in I^2C-bus for the host processor and vice versa. It manages CEC message reception and transmission compliant to CEC protocol and provides the message to the system microcontroller (host processor).

For power consumption optimization purpose CEC could be enabled or disabled through I^2C-bus register. The following sections describe CEC:

- Features
- Clocking scheme

7.12.1 Features

- Receive and transmit CEC messages to host processor
- Supports multiple CEC logical addresses
- Supports CEC messages up to 16 bytes long
- Programmable retry count
- Comprehensive arbitration and collision handling

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7.12.2 Clock

CEC clock must be running in Sleep mode (with CEC) to wake up TDA19988 using CEC specific message as described in *"HDMI specification 1.4a"*.

CEC module can be clocked using:

- External clock:
  - 12 MHz crystal ± 1 %.
- Internal clock:
  - FRO (Free Running Oscillator). FRO frequency varies and in the range from 12.64 MHz to 12.9 MHz. See Figure 17.

CEC operates normally (i.e. matches the timing requested CEC specification) if and only if its clock frequency is set to 12 MHz.

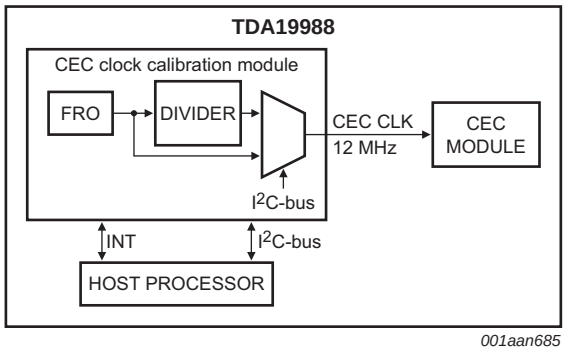

Fig 17. Modules involved in CEC clock calibration process

Calibration procedure is completely handled by the software delivered together with the device, it has the following steps:

- Host processor set TDA19988 in calibration mode
- Host processor generates a negative pulse of 10 ms ± 1 % on INT pin
- Host processor deselects the calibration mode when it is completed, the chip is ready to operate

CEC clock calibration must be performed at each power-up and each time TDA19988 moves from Standby or Sleep (without CEC) state to normal operating mode.

Non successful calibration will lead to CEC signal not matching timings specification; as a consequence, CEC will not be functional.

7.12.3 CEC interrupt

Pin INT is used by TDA19988 to warn the host processor that HDMI or CEC events (CEC message is available to read) have occurred.

Software interrupt status register reads determine which block between HDMI or CEC has raised the interruption before processing it.

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7.13 HDMI core

7.13.1 Pixel repetition

To transmit video formats with pixel rates below 25 megasamples per second or to increase the number of audio sample packets in each frame, TDA19988 allows pixel repetition to increase the transmitted pixel clock. Pixel repetition factor can be adjusted from 1 to 10.

7.13.2 DDC-bus channel

The DDC-bus pins DSDA and DSCL are 5 V tolerant and can work at standard mode (100 kHz). The DDC-bus is used as a master interface when reading the EDID.

When the device is power-off, DSDA and DSCL ports:

- become in high-impedance
- can withstand 5 V from the sink

7.14 E-EDID

7.14.1 E-EDID reading

As a master interface for the EDID process, the DDC-bus is compliant with the I^2C-bus specification and has the possibility of repeat/start condition to enable quick access to the EDID content, as well as the possibility of reading a large EDID (with the use of segment pointer).

TDA19988 has a whole I^2C-bus (page 09h) dedicated to the EDID where one block (128 bytes) can be stored. The block can be read by the system microcontroller to determine the supported video and audio format of the downstream site.

Remark: When the block is read by TDA19988, it generates an interrupt to warn the main processor that the chip is ready to transmit the content. Once the content is read out by the main processor, it can allow other blocks to be read if required.

7.14.2 HDMI and DVI receiver discrimination

This information is located in the E-EDID receiver part, in the ‘vendor-specific data block’ within the first CEA EDID timing extension.

If the 24-bit IEEE Registration Identifier contains the value 00 0C03h, then the receiver will support HDMI, otherwise the device will be treated as a DVI device.

However, even through TDA19988 have directly access to that information, it is the task of the host processor to ask to switch from DVI to HDMI mode.

8. I^2C-bus interface and register definitions

8.1 I^2C-bus protocol

The I^2C-bus pins CSDA and CSCL are 1.8 V and 3.3 V tolerant. Both Fast mode (400 kHz) and Standard mode (100 kHz) are supported.

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The registers of TDA19988 can be accessed via the I²C-bus. All registers are R/W except for those which are confidential.

HDMI and CEC cores I²C-bus addresses are given in Table 21 and Table 22.

Table 21. HDMI core I²C-bus address

HDMI core address							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	1	0	0	X[1]	X[1]	0/1

[1] X can be selected for HVQFN package. X is set to 0 for TFBGA package

Table 22. CEC core I²C-bus address

CEC core address							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
0	1	1	0	1	X[1]	X[1]	0/1

[1] X can be selected for HVQFN package. X is set to 0 for TFBGA package

For read access, the master writes the address of TDA19988 HDMI or CEC core, and the subaddress to access the specific register and then the data.

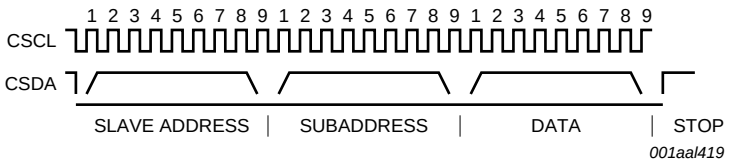

Fig 18. I²C-bus access

8.2 Memory page management

The I²C-bus memory is split into several pages for HDMI core only, and the selection between pages is made with common register CURPAGE_ADR. It is only necessary to write in this register once to change the current page. So multiple read or write operations in the same page need a write register CURPAGE_ADR once at the beginning.

The following memory pages are available for TDA19988:

- Page 00h: general control
- Page 02h: PLL settings
- Page 09h: EDID control page
- Page 10h: information frames and packets
- Page 11h: audio settings and content info packets
- Page 12h: HDCP (TDA19988AHN and TDA19988AET only) and OTP
- Page 13h: gamut-related metadata packets

The CEC core does not need memory page mechanism due to its reduced number of registers.

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8.3 ID version

The ID version readable via I²C-bus is defined by the concatenation of VERSION_MSB and VERSION registers. The ID version value is 212h.

8.4 Clock stretching

Clock stretching pauses a transaction by holding the CSCL line LOW. The transaction cannot continue until the line is released HIGH again.

For example: on the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the CSCL line LOW after reception and acknowledgment of a byte to force the master into a wait state until the slave is ready for the next byte transfer; see Table 31.

Clock stretching must be supported by I²C-bus master especially when CEC feature of TDA19988 is used. If CEC feature of TDA19988 is not used, I²C-bus master does not need to support clock stretching.

9. Input format

In Table 23 the port VPA has been mapped to C_b (YCbCr space)/B (RGB space), VPB has been mapped to Y (YCbCr space)/G (RGB space) and VPC has been mapped to Cr (YCbCr space)/R (RGB space).

Table 23. Input format

L: recommend tied to LOW voltage, e.g. ground

Input pins	Signal	RGB	YCbCr						
		4 : 4 : 4	4 : 4 : 4	4 : 2 : 2 (semi-planar)		4 : 2 : 2 (ITU 656-like)			
Video port A									
VPA[0]	Cb[0]/B[0]	B[0]	Cb[0]	Y_0[0]	Y_1[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]
VPA[1]	Cb[1]/B[1]	B[1]	Cb[1]	Y_0[1]	Y_1[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]
VPA[2]	Cb[2]/B[2]	B[2]	Cb[2]	Y_0[2]	Y_1[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]
VPA[3]	Cb[3]/B[3]	B[3]	Cb[3]	Y_0[3]	Y_1[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]
VPA[4]	Cb[4]/B[4]	B[4]	Cb[4]	Cb[0]	Cr[0]	L	L	L	L
VPA[5]	Cb[5]/B[5]	B[5]	Cb[5]	Cb[1]	Cr[1]	L	L	L	L
VPA[6]	Cb[6]/B[6]	B[6]	Cb[6]	Cb[2]	Cr[2]	L	L	L	L
VPA[7]	Cb[7]/B[7]	B[7]	Cb[7]	Cb[3]	Cr[3]	L	L	L	L
Video port B									
VPB[0]	Y[0]/G[0]	G[0]	Y[0]	Y_0[4]	Y_1[4]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]
VPB[1]	Y[1]/G[1]	G[1]	Y[1]	Y_0[5]	Y_1[5]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]
VPB[2]	Y[2]/G[2]	G[2]	Y[2]	Y_0[6]	Y_1[6]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]
VPB[3]	Y[3]/G[3]	G[3]	Y[3]	Y_0[7]	Y_1[7]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]
VPB[4]	Y[4]/G[4]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
VPB[5]	Y[5]/G[5]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
VPB[6]	Y[6]/G[6]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
VPB[7]	Y[7]/G[7]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]

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Table 23. Input format *...continued*

L: recommend tied to LOW voltage, e.g. ground

Input pins	Signal	RGB	YCbCr						
		4 : 4 : 4	4 : 4 : 4	4 : 2 : 2 (semi-planar)		4 : 2 : 2 (ITU 656-like)			
Video port C									
VPC[0]	Cr[0]/R[0]	R[0]	Cr[0]	Cb[4]	Cr[4]	L	L	L	L
VPC[1]	Cr[1]/R[1]	R[1]	Cr[1]	Cb[5]	Cr[5]	L	L	L	L
VPC[2]	Cr[2]/R[2]	R[2]	Cr[2]	Cb[6]	Cr[6]	L	L	L	L
VPC[3]	Cr[3]/R[3]	R[3]	Cr[3]	Cb[7]	Cr[7]	L	L	L	L
VPC[4]	Cr[4]/R[4]	R[4]	Cr[4]	Cb[8]	Cr[8]	L	L	L	L
VPC[5]	Cr[5]/R[5]	R[5]	Cr[5]	Cb[9]	Cr[9]	L	L	L	L
VPC[6]	Cr[6]/R[6]	R[6]	Cr[6]	Cb[10]	Cr[10]	L	L	L	L
VPC[7]	Cr[7]/R[7]	R[7]	Cr[7]	Cb[11]	Cr[11]	L	L	L	L

9.1 Timing parameters for video supported

TDA19988 supports all EIA/CEA-861B standards and ATSC video formats.

Table 24. Timing parameters for EIA/CEA-861B

EIA/CEA-861B Video code	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition
59.94 Hz systems							
1 (VGA)	640 × 480p	59.9401	800	525	31.469	25.175	1
2, 3	720 × 480p	59.9401	858	525	31.469	27.000	1
4	1280 × 720p	59.9401	1650	750	44.955	74.175	1
5	1920 × 1080i	59.9401	2200	1125	33.716	74.175	1
6, 7 (NTSC)	1440 × 480i	59.9401	1716	525	15.734	27.000	2
16	1920 × 1080p	60.000	2200	1125	67.432	148.350	1
60 Hz systems							
1 (VGA)	640 × 480p	60.000	800	525	31.500	25.200	1
2, 3	720 × 480p	60.000	858	525	31.500	27.027	1
4	1280 × 720p	60.000	1650	750	45.000	74.250	1
5	1920 × 1080i	60.000	2200	1125	33.750	74.250	1
6, 7 (NTSC)	1440 × 480i	60.000	1716	525	15.750	27.027	2
16	1920 × 1080p	60.000	2200	1125	67.500	148.50	1
50 Hz systems							
17, 18	720 × 576p	50.000	864	625	31.250	27.000	1
19	1280 × 720p	50.000	1980	750	37.500	74.250	1
20	1920 × 1080i	50.000	2640	1125	28.125	74.250	1
21, 22 (PAL)	1440 × 576i	50.000	1728	625	15.625	27.000	2
31	1920 × 1080p	50.000	2640	1125	56.250	148.50	1
Various systems							
32	1920 × 1080p	23.976	2750	1125	26.973	74.175824	1
32	1920 × 1080p	24	2750	1125	27	74.25	1

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Table 24. Timing parameters for EIA/CEA-861B *…continued*

EIA/CEA-861B Video code	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition
33	1920 × 1080p	25	2640	1125	28.125	74.25	1
34	1920 × 1080p	29.97	2200	1125	33.716	74.175824	1
34	1920 × 1080p	30	2200	1125	33.75	74.25	1

TDA19988 support other video formats, so software implementation can be considered on request.

9.2 Timing parameters for PC standards supported

TDA19988 can support all major PC Standards up to 165 MHz.

Table 25. Timing parameters for PC standards below 165 MHz

Standard	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition
0.31M3 VGA	640 × 480p	59.940	800	525	31.469	25.175	-
	640 × 480p	72.809	832	520	37.861	31.500	-
	640 × 480p	75.000	840	500	37.500	31.500	-
	640 × 480p	85.008	832	509	43.269	36.000	-
0.48M3 SVGA	800 × 600p	60.317	1056	628	37.879	40.000	-
	800 × 600p	72.188	1040	666	48.077	50.000	-
	800 × 600p	75.000	1056	625	46.875	49.500	-
	800 × 600p	85.061	1048	631	53.674	56.250	-
0.79M3 XGA	1024 × 768p	60.004	1344	806	48.363	65.000	-
	1024 × 768p	70.069	1328	806	56.476	75.000	-
	1024 × 768p	75.029	1312	800	60.023	78.750	-
1.31M4 SXGA	1280 × 1024p	60.020	1688	1066	63.981	108.000	-
VDMTREV	1600 × 1200p	60.000	2160	1250	75.000	162.000	-

For other PC video formats in the range from VGA to 1600 × 1200 at 60 Hz implementation can be considered on request.

9.3 Primary 3D video formats

Table 26. 3D video formats timing supported

Resolution	3D transmission type
1280 × 720p at 59.94 Hz and 60 Hz	(Frame Packing, Side-by-Side (Half)), Top-and-Bottom
1280 × 720p at 50 Hz	(Frame Packing, Side-by-Side (Half)), Top-and-Bottom
1280 × 720p at 23.98 Hz and 24 Hz	Frame Packing
1280 × 720p at 29.97 Hz and 30 Hz	Frame Packing
1920 × 1080i at 59.94 Hz and 60 Hz	Side-by-Side (Half)
1920 × 1080i at 50 Hz	Side-by-Side (Half)
1920 × 1080p at 23.98 Hz and 24 Hz	Side-by-Side (Half), Top-and-Bottom

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Table 26. 3D video formats timing supported *…continued*

Resolution	3D transmission type
1920 × 1080p at 29.97 Hz and 30 Hz	Top-and-Bottom
1920 × 1080p at 59.94 Hz and 60 Hz	Top-and-Bottom
1920 × 1080p at 50 Hz	Top-and-Bottom

TDA19988 support other 3D video formats, so software implementation can be considered on request.

10. Limiting values

Table 27. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDA(TMDS)(1V8)}$	TMDS analog supply voltage (1.8 V)			–0.5	+2.5	V
$V_{DDA(PLL)(1V8)}$	PLL analog supply voltage (1.8 V)			–0.5	+2.5	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)			–0.5	+2.5	V
$V_{DDD(IO)(1V8)}$	I/O digital supply voltage (1.8 V)			–0.5	+2.5	V
V_{DDDC}	core digital supply voltage			–0.5	+2.5	V
ΔV_{DD}	supply voltage difference			–2	+2	V
V_{IO}	input/output voltage	3.3 V tolerant I/O		–0.3	+3.6	V
		5 V tolerant I/O		–0.3	+5.5	V
V_{ESD}	electrostatic discharge voltage	EIA/JESD22-A114 (HBM)	[1]	–2.5	+2.5	kV
		EIA/JESD22-C101-C (FCDM)	[2]	–1	+1	kV

[1] On TMDS outputs.

[2] It withstands class III of JEDEC classification.

11. Thermal characteristics

Table 28. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC 4L board	-	56.9	-	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		-	15.1	-	K/W
T_{stg}	storage temperature		-	-	+150	°C
T_{amb}	ambient temperature		–20	-	+85	°C
T_j	junction temperature		-	-	+125	°C

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12. Static characteristics

Table 29. Supplies

T_{amb} = −20 °C to +85 °C; without HDCP; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDDC}	core digital supply voltage		[1]	1.7	1.8	1.9	V
$V_{DDA(TMDS)(1V8)}$	TMDS analog supply voltage (1.8 V)			1.7	1.8	1.9	V
$V_{DDA(PLL)(1V8)}$	PLL analog supply voltage (1.8 V)			1.7	1.8	1.9	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)			1.7	1.8	1.9	V
$V_{DDD(IO)(1V8)}$	I/O digital supply voltage (1.8 V)			1.7	1.8	1.9	V
$I_{DDA(sum)(1V8)}$	sum analog supply current (1.8 V)	720p60	[2]	-	13	16	mA
		1080p60	[2]	-	23	27	mA
$I_{DDA(PLL)(1V8)}$	PLL analog supply current (1.8 V)		[2]	-	6	8	mA
$I_{DDD(IO)(1V8)}$	input/output digital supply current (1.8 V)		[2]	-	0.06	0.1	mA
$I_{DDDC(1V8)}$	core digital supply current (1.8 V)	720p60	[2]	-	26	29	mA
		1080p60	[2]	-	40	42	mA
P_{cons}	power consumption	720p60	[3]	-	60	75	mW
		1080p60	[3]	-	95	115	mW
		1080p60	[4]	-	-	146	mW
		Sleep mode with CEC		-	1.3	-	mW
		Sleep mode without CEC		-	0.9	-	mW
		Standby mode		-	18	-	μW
P_{tot}	total power dissipation		[2]	-	172	-	mW
			[2]	-	207	-	mW

[1] See Table 7.

[2] Full RGB input 24-bit 30 % activity on video ports, HDMI RGB output, HDCP (TDA19988AHN and TDA19988AET only) enable.

[3] Full RGB input 24-bit 30 % activity on video ports, HDMI RGB output, HDCP (TDA19988AHN and TDA19988AET only) disable.

[4] Full YCbCr input 24-bit 30 % activity on video ports, HDMI RGB output, HDCP (TDA19988AHN and TDA19988AET only) enable.

Table 30. Digital inputs and outputs

T_{amb} = −20 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Not 5 V tolerant CMOS 1.8 V and CMOS 3.3 V tolerant digital input pins HSYNC, VSYNC, APn, ACLK, VPA[n], VPB[n], VPC[n], VCLK, DE						
V_{IL}	LOW-level input voltage	-	-	-	0.75	V
V_{IH}	HIGH-level input voltage	-	1.4	-	-	V
I_{IL}	LOW-level input current		−2	-	+2	μA
I_{IH}	HIGH-level input current		−2	-	+2	μA
C_i	input capacitance		-	4.5	-	pF
5 V tolerant input pin HPD						
V_{IL}	LOW-level input voltage	-	-	-	0.8	V
V_{IH}	HIGH-level input voltage	-	2	-	-	V
C_i	input capacitance		-	4.5	-	pF

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Table 30. Digital inputs and outputs *...continued*

T_{amb} = −20 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMOS 1.8 V and CMOS 3.3 V tolerant digital input/output pin INT						
V_{IL}	LOW-level input voltage	-	-	-	0.85	V
V_{IH}	HIGH-level input voltage	-	1.4	-	-	V
V_{OL}	LOW-level output voltage	C_L = 10 pF; I_{OL} = 2 mA	-	-	0.4	V
5 V tolerant master bus: DDC-bus pins DSDA, DSCL[1]						
V_{OL}	LOW-level output voltage		-	-	0.4	V
V_{IL}	LOW-level input voltage		-	-	1.5	V
V_{IH}	HIGH-level input voltage		3.0	-	-	V
1.8 V to 3.3 V tolerant slave bus: I²C-bus input/output pins CSCL, CSDA[1]						
V_{OL}	LOW-level output voltage		-	-	0.4	V
V_{IL}	LOW-level input voltage		-	-	0.85	V
V_{IH}	HIGH-level input voltage		1.4	-	-	V
CEC input/output[2] pin						
V_{OL}	LOW-level output voltage		-	-	0.4	V
V_{OH}	HIGH-level output voltage		2.5	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
TMDS output pins: TX0−, TX0+, TX1−, TX1+, TX2−, TX2+, TXC− and TXC+						
$V_{O(dif)}$	differential output voltage	R_{EXT_SWING} = 10 kΩ ± 1 %	420	500	580	mV

[1] See Section 7.1 and refer to the *I²C-bus specification version 2.1* (document order number 9398 393 40011).

[2] For information, input hysteresis is normally supplied by the microprocessor input circuit: in this circumstance, external hysteresis circuitry is not needed.

13. Dynamic characteristics

Table 31. Timing characteristics

T_{amb} = −20 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock input: pin VCLK							
$f_{clk(max)}$	maximum clock frequency	-		165	-	-	MHz
$t_{su(D)}$	data input set-up time	see Figure 19 and 20		1.5	-	-	ns
$t_{h(D)}$	data input hold time	see Figure 19 and 20		0.7	-	-	ns
δ_{clk}	clock duty cycle		[1]	30	50	70	%
f_{clk}	clock frequency	CEC		-	12	-	MHz
Clock input: pin ACLK							
$t_{su(D)}$	data input set-up time			3	-	-	ns
$t_{h(D)}$	data input hold time			0.7	-	-	ns
DDC-bus: pins DSDA, DSCL (5 V tolerant) master bus[2]							
f_{SCL}	SCL frequency	Standard mode		-	-	100	kHz
C_i	capacitance for each I/O pin			-	7	-	pF
I²C-bus: pins CSCL, CSDA (5 V tolerant) slave bus[2]							

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Table 31. Timing characteristics *...continued*

T_{amb} = −20 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL frequency	Standard mode	-	-	100	kHz
		Fast mode	-	-	400	kHz
$t_{stretch}$	stretch time	CEC	-	80	-	µs
CEC input/output[3]						
t_r	rise time	10 % to 90 %	-	-	50	µs
t_f	fall time	10 % to 90 %	-	-	2	µs
TMDS output pins: TXC− and TXC+						
$f_{clk(max)}$	maximum clock frequency	on the TMDS link	165	-	-	MHz
TMDS output pins: TX0−, TX0+, TX1−, TX1+, TX2− and TX2+						
$f_{clk(max)}$	maximum clock frequency		1.65	-	-	GHz

[1] $\delta_{clk} = t_{clk(H)} / (t_{clk(H)} + t_{clk(L)})$.

[2] See Section 7.1 and refer to the *I^2C-bus specification version 2.1* (document order number 9398 393 40011).

[3] For details about CEC electrical specification, see *HDMI specification 1.4a.*

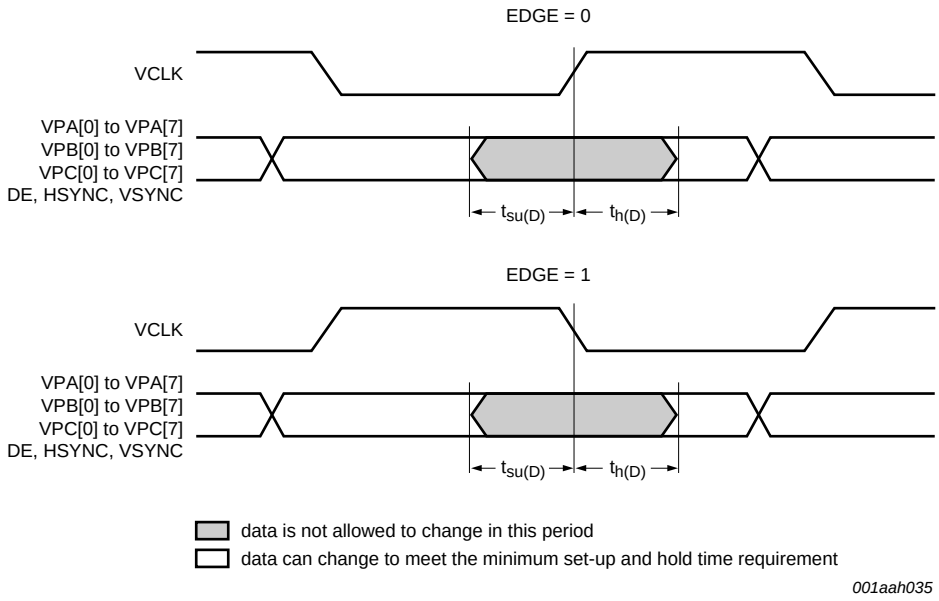

Fig 19. Set-up and hold time definition diagram for single-edge clock mode

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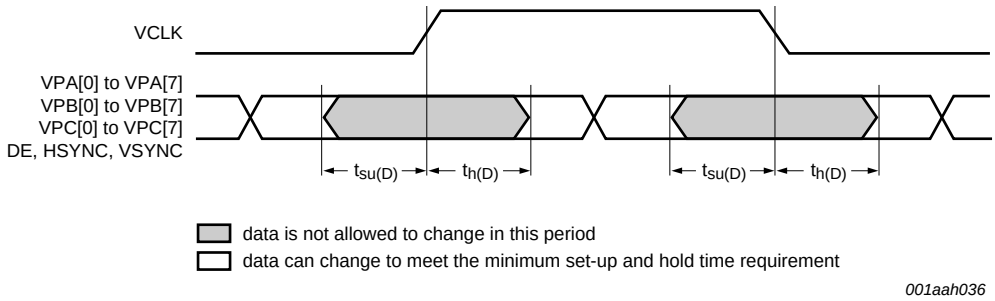

Fig 20. Set-up and hold time definition diagram for double-edge clock mode

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14. Application information

14.1 Transmitter connection with external world

Figure 21 and Figure 22 refer to a simple receiver application. However, TDA19988 can be part of a repeater application as described in *"HDMI specification 1.4a"*.

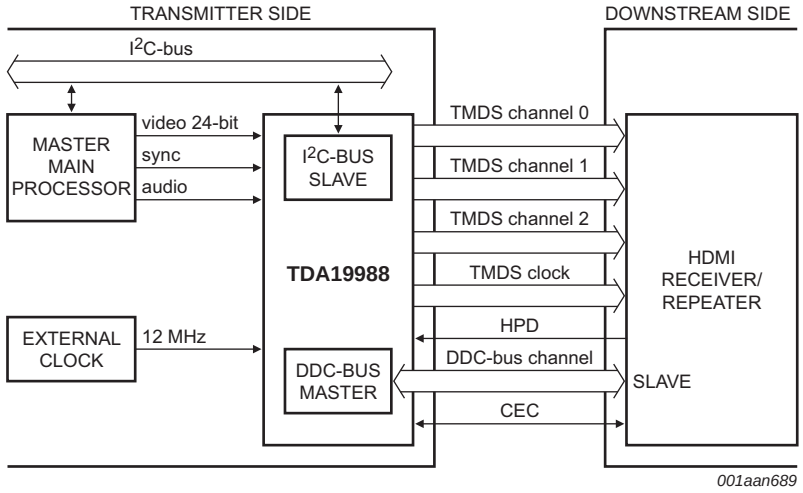

Fig 21. Connecting TDA19988 transmitter using external clock source

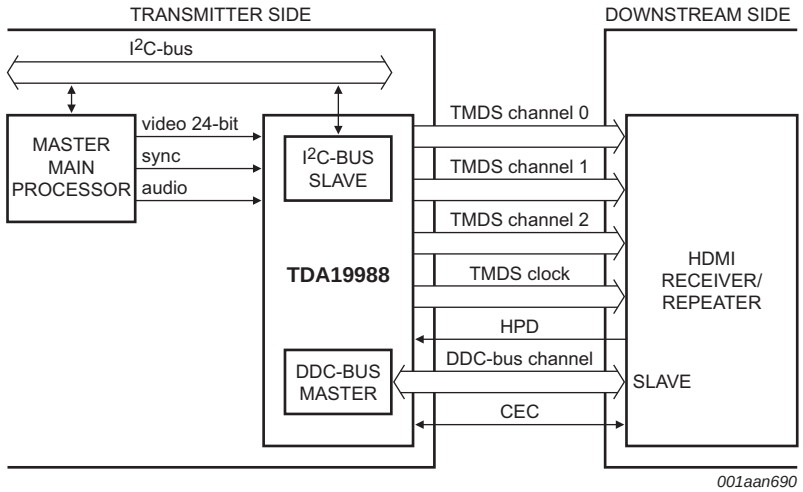

Fig 22. Connecting TDA19988 transmitter using internal FRO for CEC

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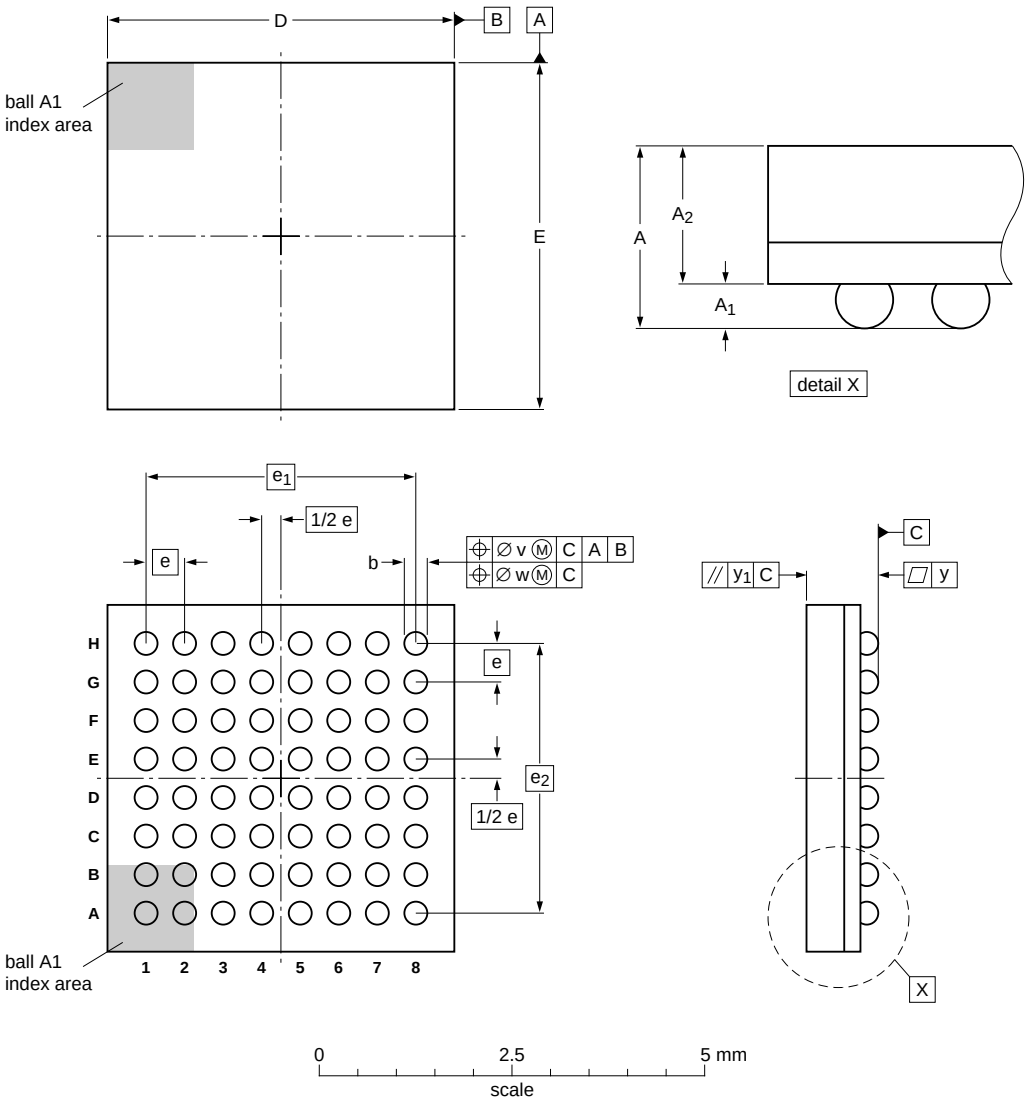
15. Package outline

TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls **SOT962-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.10	0.30	0.80	0.35	4.6	4.6	0.5	3.5	3.5	0.15	0.05	0.08	0.1
	nom	0.95	0.25	0.70	0.30	4.5	4.5							
	min	0.85	0.20	0.65	0.25	4.4	4.4							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT962-3	- - -	- - -	- - -			~~08-05-26~~ 08-06-18

Fig 23. Package outline SOT962-3 (TFBGA64)

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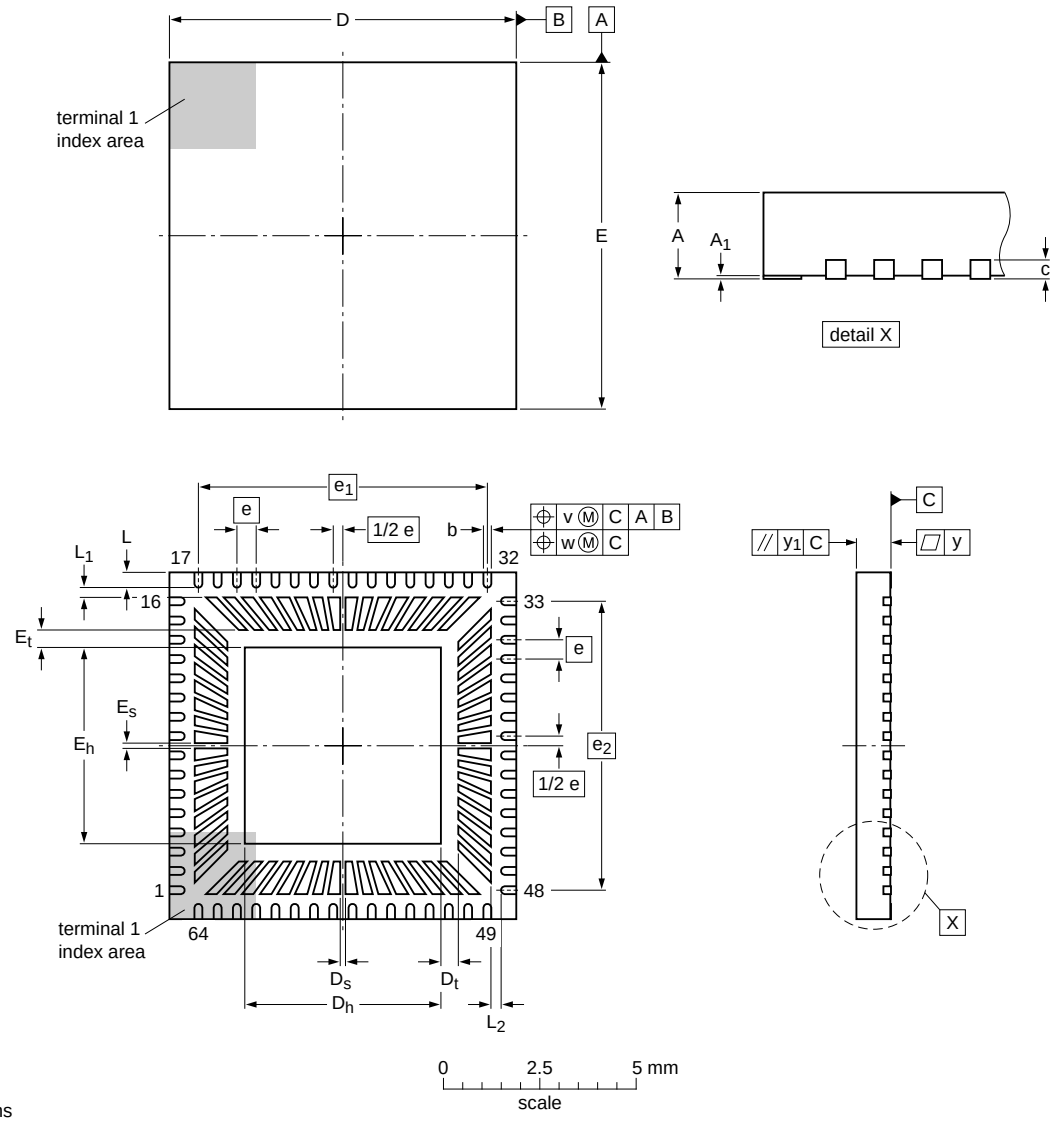
HVQFN64: plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm **SOT804-4**



Dimensions

Unit		A	A_1	b	c	$D^{(1)}$	D_h	D_s	D_t	$E^{(1)}$	E_h	E_s	E_t	e	e_1	e_2	L	L_1	L_2	v	w	y	y_1
	max	1.00	0.05	0.30		9.1	5.25	0.19	0.50	9.1	5.25	0.19	0.50				0.5						
mm	nom	0.85	0.02	0.21	0.2	9.0	5.10	0.14	0.45	9.0	5.10	0.14	0.45	0.5	7.5	7.5	0.4	0.25	0.25	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		8.9	4.95	0.09	0.40	8.9	4.95	0.09	0.40				0.3						

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot804-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT804-4	- - -	- - -	- - -			~~10-05-26~~ 10-05-27

Fig 24. Package outline SOT804-4 (HVQFN64)

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16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 32 and 33

Table 32. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 33. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.

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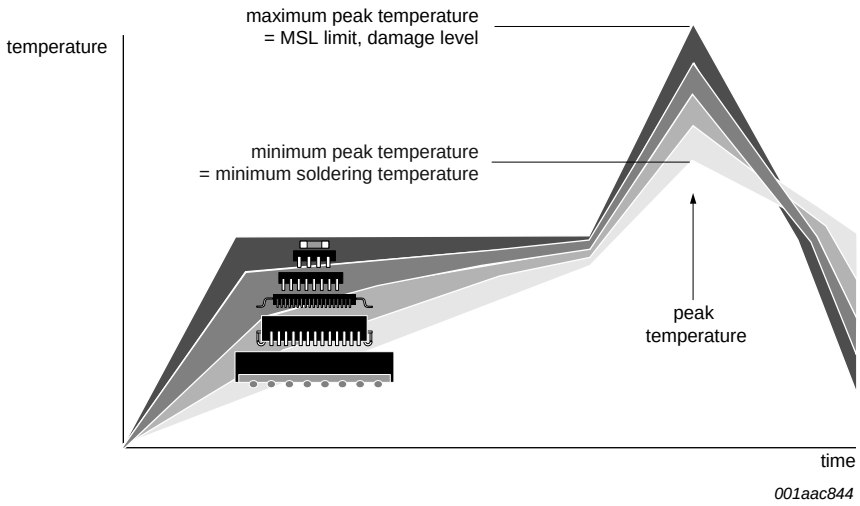

MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 34. Abbreviations

Acronym	Description
AC3	Active Coding-3
ACP	Audio Content Protection
ACR	Audio Clock Recovery
ATSC	Advanced Television Systems Committee
AV	Audio Video
AVR	Audio Video Recorder
BOM	Bill Of Materials
CEA	Consumer Electronics Association
CEC	Consumer Electronics Control
CTS/N	Clock Time Stamp integer divider
DDC	Display Data Channel
DDR	Double Data Rate
DE	Data Enable
DSC	Digital Still Camera
DTS	Digital Transmission System
DVC	Digital Video Camera
DVD	Digital Versatile Disc
DVI	Digital Visual Interface
EAV	End Active Video

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Table 34. Abbreviations *...continued*

Acronym	Description
EDID	Extended Display Identification Data
E-EDID	Enhanced Extended Display Identification Data
EIA	Electronic Industries Alliance
FCDM	Field Charged Device Model
FIFO	First In, First Out
FREF	Field REFerence
FRO	Free Running Oscillator
HBM	Human Body Model
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detection
HREF	Horizontal REFerence
HSYNC	Horizontal SYNChronization
KSV	Key Selection Vector
LSB	Least Significant Bit
LV-CMOS	Low Voltage Complementary Metal-Oxide Semiconductor
MID	Mobile Internet Device
MSB	Most Significant Bit
OTP	One Time Programming
PC	Personal Computer
PCM	Pulse Code Modulation
PLL	Phase-Locked Loop
PMP	Portable Multimedia Player
POR	Power-On Reset
RGB	R = red, G = green, B = blue
SAV	Start Active Video
SDR	Single Data Rate
SHA-1	Secure Hash Algorithm
SMPTE	Society of Motion Picture and Television Engineers
S/PDIF	Sony/Philips Digital Interface
STB	Set-Top Box
TMDS	Transition Minimized Differential Signalling
Tx	Transmitter
UM PC	Ultra-Mobile Personal Computer
UXGA60	Ultra Extended Graphics Array
VHREF	Vertical Horizontal REFerence
VREF	Vertical REFerence
VSYNC	Vertical SYNChronization
YCbCr	Y = luminance, Cb = Chroma component blue, Cr = Chroma component red
WS	Word Select

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18. Revision history

Table 35. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA19988 v.3	20110721	Product data sheet	-	TDA19988 v.2
Modifications:	• Section 1: updated • Section 2: updated • Section 3: updated • Section 7.11: updated • Figure 1: updated • Table 27: updated • Table 30: updated • Table 31: updated			
TDA19988 v.2	20110601	Product data sheet	-	TDA19988 v.1
TDA19988 v.1	20110304	Objective data sheet	-	-

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19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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