Precision Monolithic Quad SPST CMOS Analog Switches

DESCRIPTION

The DG411HS series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power (0.35 µW) with high speed (t_{ON}: 68 ns), the DG411HS family is ideally suited for portable and battery powered industrial and military applications.

To achieve high-voltage ratings and superior switching performance, the DG411HS series was built on Vishay Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages up to the supply levels when off.

The DG411HS and DG412HS respond to opposite control logic as shown in the Truth Table. The DG413HS has two normally open and two normally closed switches.

FEATURES

- 44 V supply max. rating
- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 25 Ω
- Fast switching - t_{ON}: 68 ns
- Ultra low power - P_D: 0.35 µW
- TTL, CMOS compatible
- Single supply capability

Pb-free Available

RoHS* COMPLIANT

BENEFITS

- Widest dynamic range
- Low signal rrrors and distortion
- Break-before-make switching action
- Simple interfacing

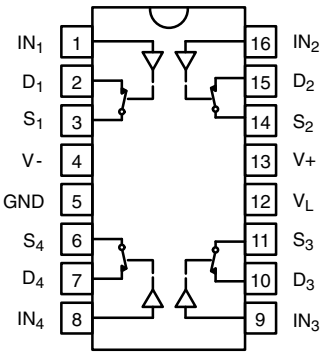
APPLICATIONS

- Precision automatic test equipment
- Precision data acquisition
- Communication systems
- Battery powered systems
- Computer peripherals

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

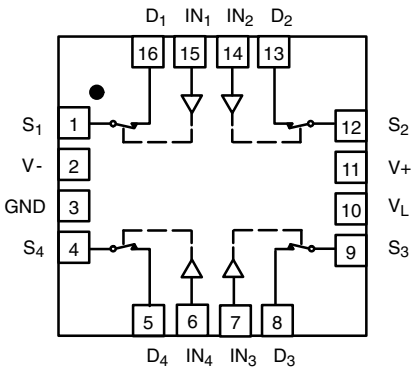
DG411HS

Dual-In-Line and SOIC



Top View

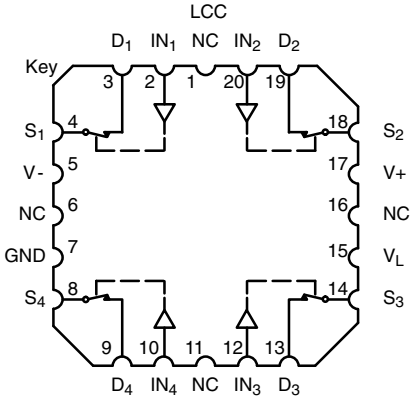
DG411HS
QFN16



Top View

DG411HS

LCC



Top View

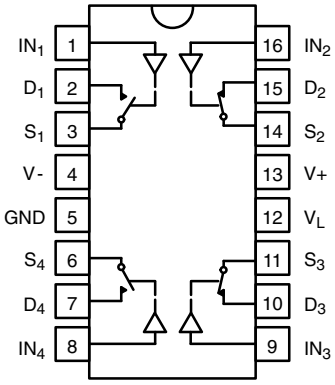
TRUTH TABLE		
Logic	**DG411HS**	**DG412HS**
0	ON	OFF
1	OFF	ON

* Pb containing terminations are not RoHS compliant, exemptions may apply

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

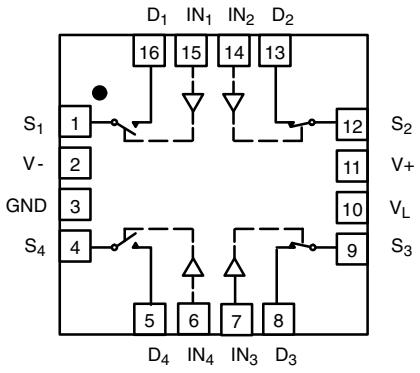
DG413HS

Dual-In-Line and SOIC



Top View

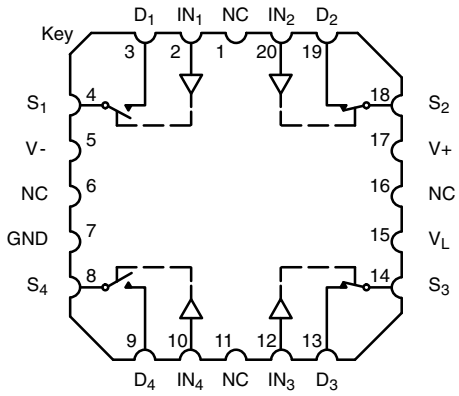
DG413HS
QFN16



Top View

DG413HS

LCC



Top View

TRUTH TABLE		
Logic	**SW_1, SW_4**	**SW_2, SW_3**
0	OFF	ON
1	ON	OFF

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
DG411HS, DG412HS		
- 40 °C to 85 °C	16-Pin Plastic DIP	DG411HSDJ DG411HSDJ-E3
		DG412HSDJ DG412HSDJ-E3
	16-Pin Narrow SOIC	DG411HSDY DG411HSDY-E3 DG411HSDY-T1 DG411HSDY-T1-E3
		DG412HSDY DG412HSDY-E3 DG412HSDY-T1 DG412HSDY-T1-E3
	16-Pin QFN 4 x 4 mm	DG411HSDN-T1-E4
		DG412HSDN-T1-E4
DG413HS		
- 40 °C to 85 °C	16-Pin Plastic DIP	DG413HSDJ DG413HSDJ-E3
	16-Pin Narrow SOIC	DG413HSDY DG413HSDY-E3 DG413HSDY-T1 DG413HSDY-T1-E3
	16-Pin QFN 4 x 4 mm	DG413HSDN-T1-E4

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
V+ to V-		44	V
GND to V-		25	
V_L		(GND - 0.3) to (V+) + 0.3	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Continuous Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed 1 ms, 10 % duty cycle)		100	
Storage Temperature	(AK, AZ Suffix)	- 65 to 150	°C
	(DJ, DY, DN Suffix)	- 65 to 125	
Power Dissipation (Package)[b]	16-Pin Plastic DIP[c]	470	mW
	16-Pin Narrow SOIC[d]	600	
	16-Pin CerDIP[e]	900	
	LCC-20[e]	900	
	16-Pin (4 x 4 mm) QFN[f]	1880	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 25 °C.
d. Derate 7.6 mW/°C above 75 °C.
e. Derate 12 mW/°C above 75 °C.
f. Derate 23.5 mW/°C above 70 °C.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V- = - 15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 13.5 V, V- = - 13.5 V I_S = - 10 mA, V_D = ± 8.5 V	Room Full	25		35 45		35 45	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V- = - 16.5 V V_D = ± 15.5 mA, V_S = ± 15.5 V	Room Full	± 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	nA
	$I_{D(off)}$		Room Full	± 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V- = - 16.5 V V_D = V_S = ± 15.5 V	Room Full	± 0.1	- 0.4 - 40	0.4 40	- 0.4 - 10	0.4 10	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V	Full	0.005	- 0.5	0.5	- 0.5	0.5	µA
Input Current, V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V	Full	0.005	- 0.5	0.5	- 0.5	0.5	
Input Capacitance[e]	C_{IN}	f = 1 MHz	Room	5					pF
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ± 10 V, see figure 2	Room Full	68		105 127		105 116	ns
Turn-Off Time	t_{OFF}		Room Full	42		80 94		80 90	
Break-Before-Make Time Delay	t_D	DG413HS only, V_S = 10 V R_L = 300 Ω, C_L = 35 pF	Room	20					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	22					pC

SPECIFICATIONS[a]									
		Test Conditions Unless Specified V+ = 15 V, V- = - 15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]			A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		
Parameter	Symbol		Temp.[b]	Typ.[c]	Min.[d]	Max.[d]	Min.[d]	Max.[d]	Unit
Dynamic Characteristics (Cont'd)									
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	- 91					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	- 88					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	12					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	12					
Channel On Capacitance[e]	$C_{D(on)}$		Room	30					
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V- = - 16.5 V V_{IN} = 0 or 5 V	Room Full	0.0001		1 5		1 5	µA
Negative Supply Current	I-		Room Full	- 0.0001	- 1 - 5		- 1 - 5		
Logic Supply Current	I_L		Room Full	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Full	- 0.0001	- 1 - 5		- 1 - 5		

SPECIFICATIONS[a] (for Unipolar Supplies)									
		Test Conditions Unless Specified V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]			A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		
Parameter	Symbol		Temp.[b]	Typ.[c]	Min.[d]	Max.[d]	Min.[d]	Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full			12		12	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 10.8 V, I_S = - 10 mA V_D = 3 V, 8 V	Room Full	49		80 100		80 100	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 8 V, see figure 2	Room Hot	95		140 180		140 160	ns
Turn-Off Time	t_{OFF}		Room Hot	36		70 79		70 74	
Break-Before-Make Time Delay	t_D	DG413HS only, V_S = 8 V R_L = 300 Ω, C_L = 35 pF	Room	60					
Charge Injection	Q	V_g = 6 V, R_g = 0 Ω, C_L = 1 nF	Room	60					pC
Power Supplies									
Positive Supply Current	I+	V+ = 13.2 V, V_{IN} = 0 or 5 V	Room Hot	0.0001		1 5		1 5	µA
Negative Supply Current	I-		Room Hot	- 0.0001	- 1 - 5		- 1 - 5		
Logic Supply Current	I_L		Room Hot	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Hot	- 0.0001	- 1 - 5		- 1 - 5		

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, Full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

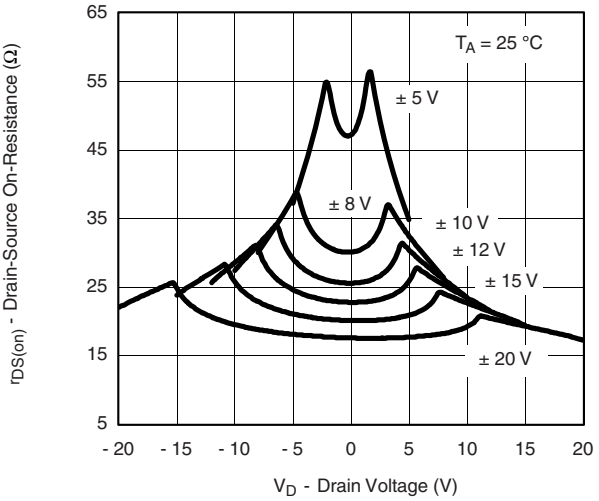
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

e. Guaranteed by design, not subject to production test.

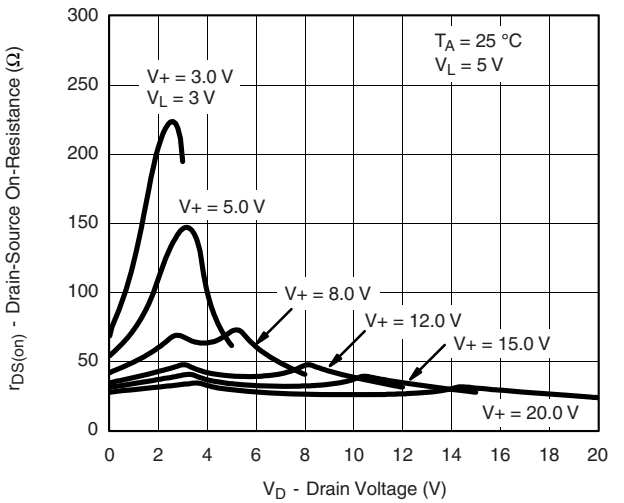
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

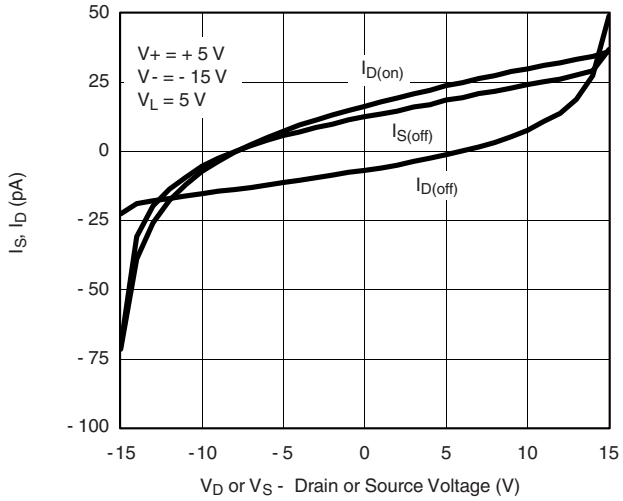
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



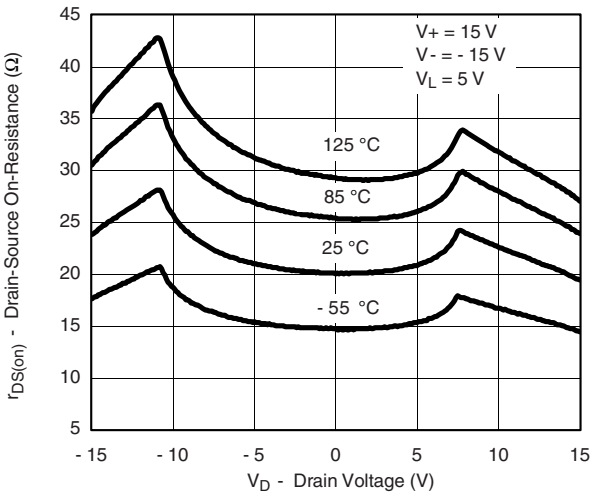
On-Resistance vs. V_D and Dual Supply Voltage



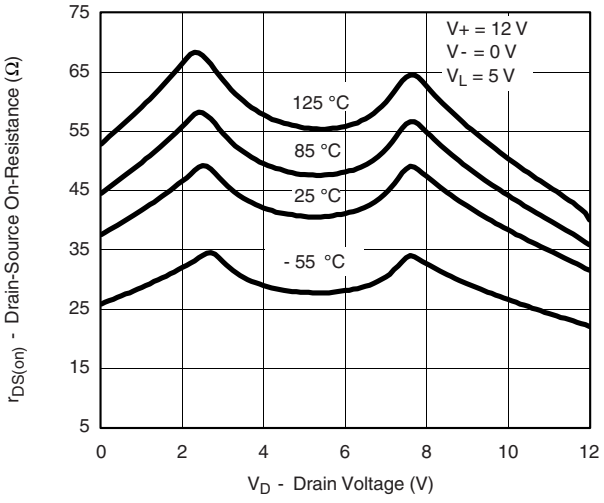
On-Resistance vs. V_D and Unipolar Supply Voltage



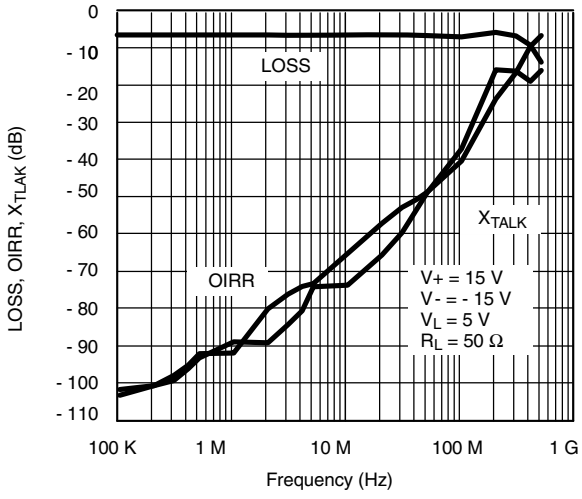
Leakage Current vs. Analog Voltage



On-Resistance vs. V_D and Temperature

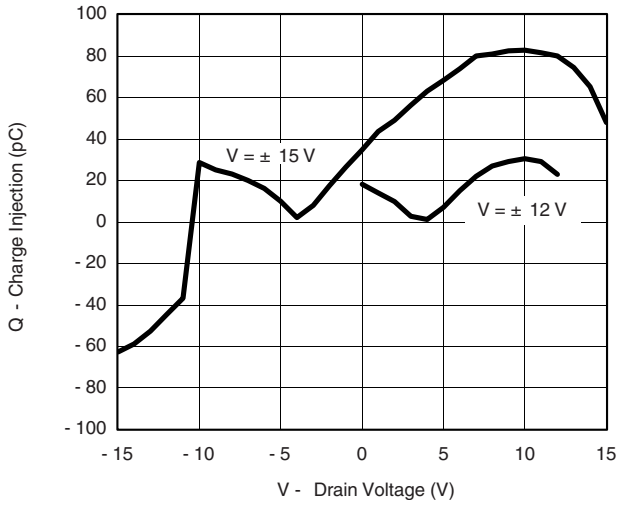


On-Resistance vs. V_D and Temperature

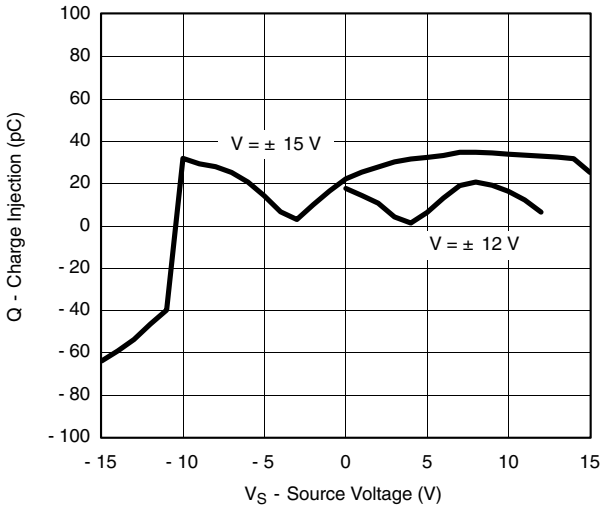


Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

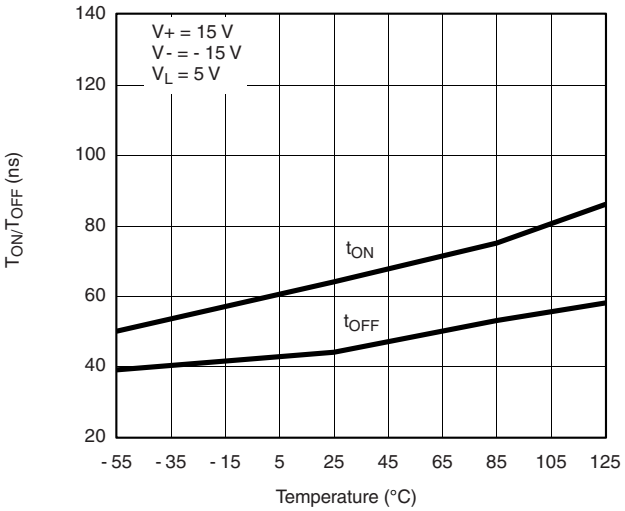
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



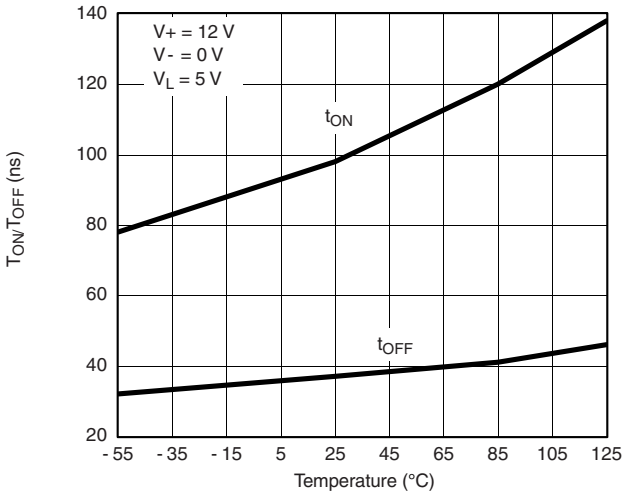
Charge Injection vs. Analog Voltage



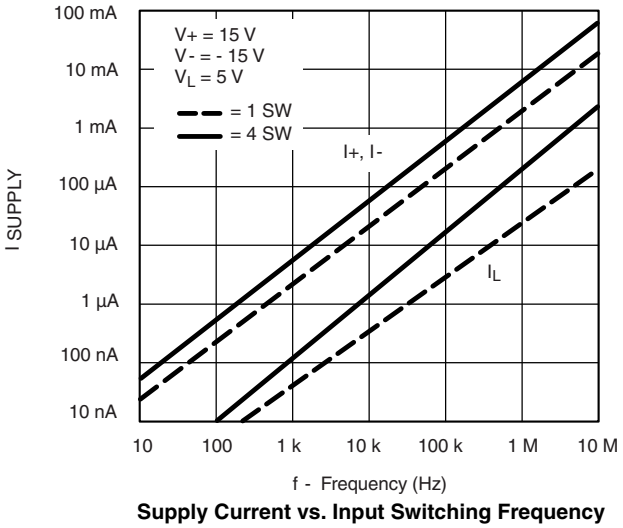
Charge Injection vs. Analog Voltage



Switching Time vs. Temperature



Switching Time vs. Temperature



Supply Current vs. Input Switching Frequency

SCHEMATIC DIAGRAM (Typical Channel)

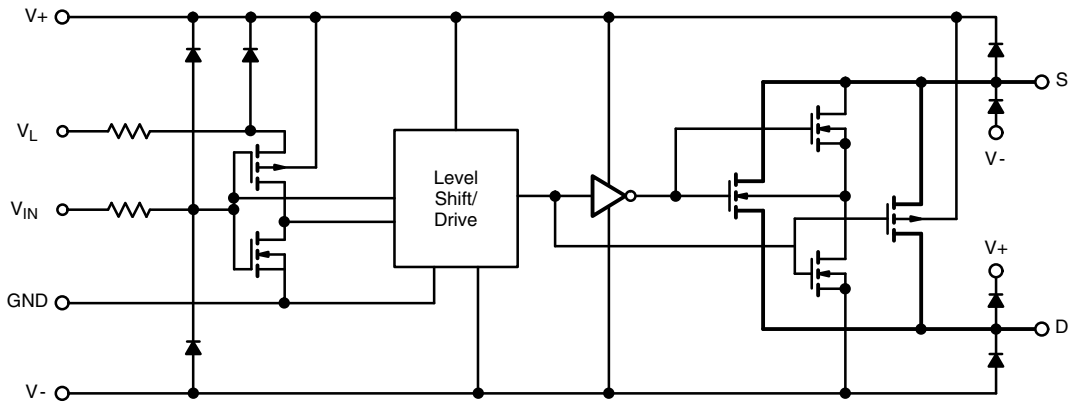
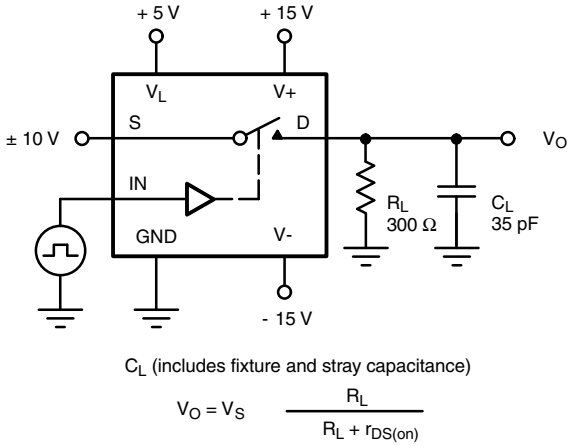


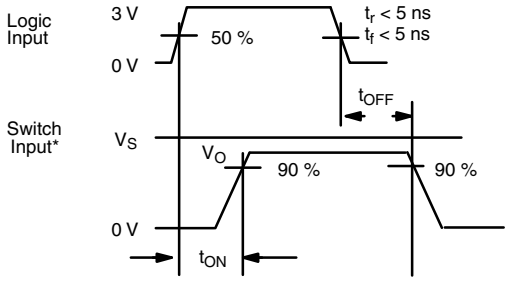
Figure 1.

TEST CIRCUITS



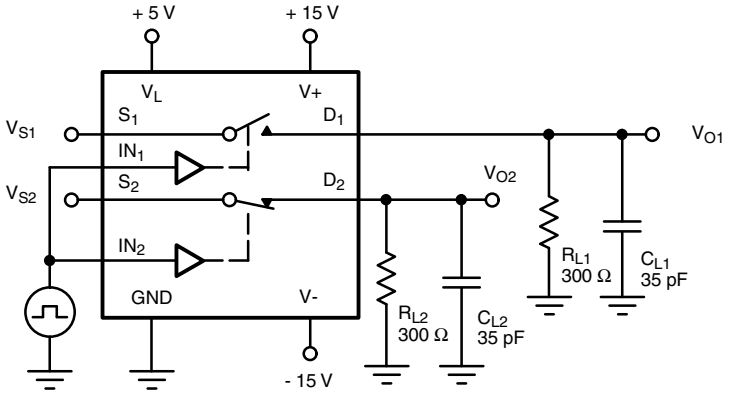
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time



C_L (includes fixture and stray capacitance)

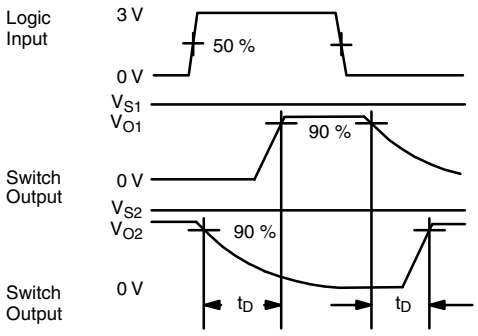


Figure 3. Break-Before-Make (DG413HS)

TEST CIRCUITS

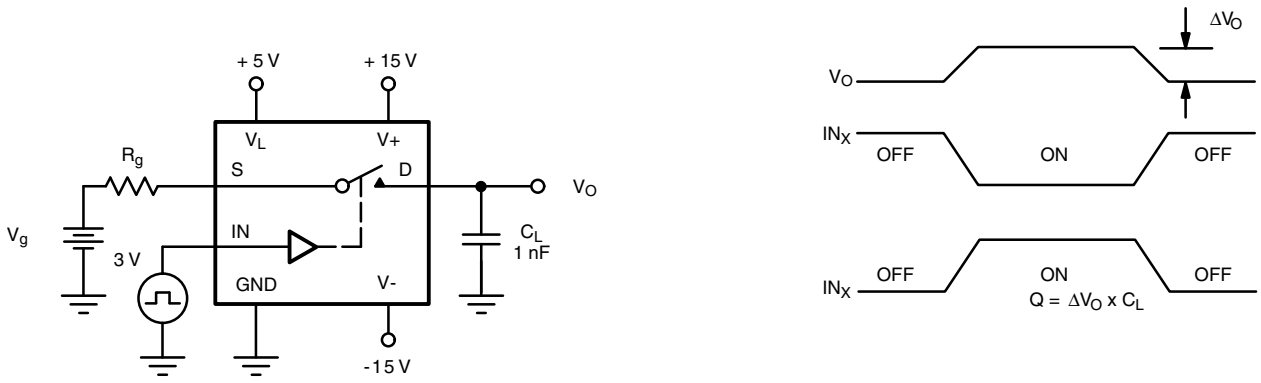


Figure 4. Charge Injection

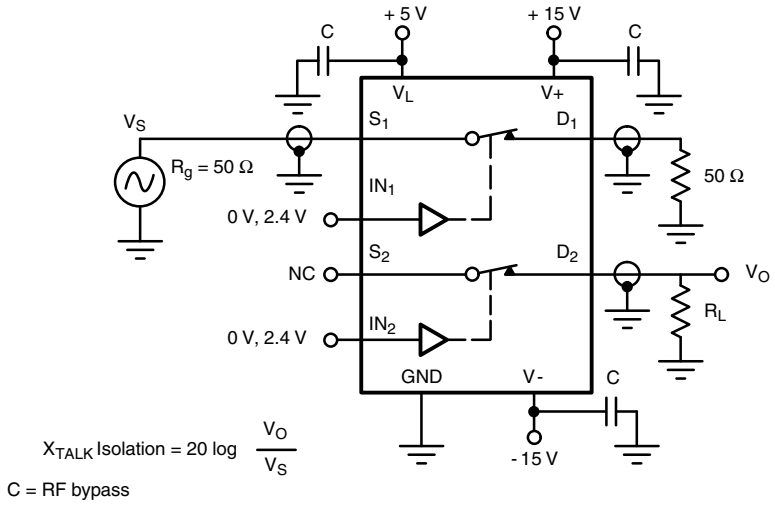


Figure 5. Crosstalk

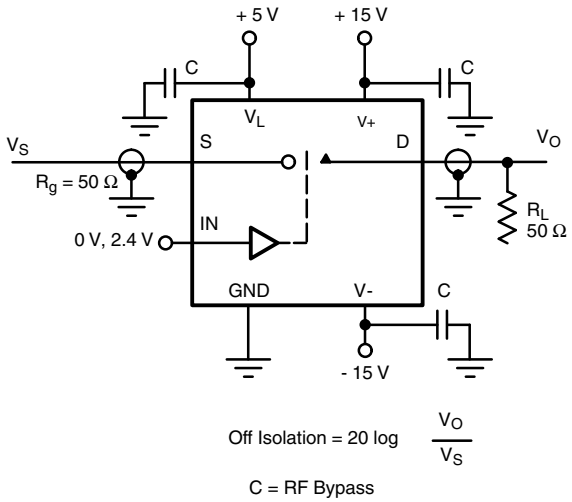


Figure 6. Off-Isolation

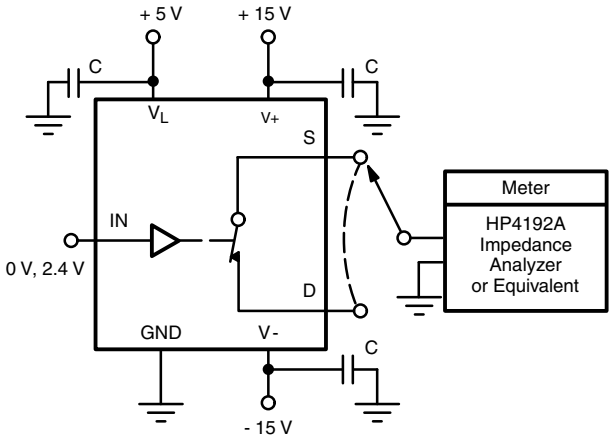


Figure 7. Source/Drain Capacitances

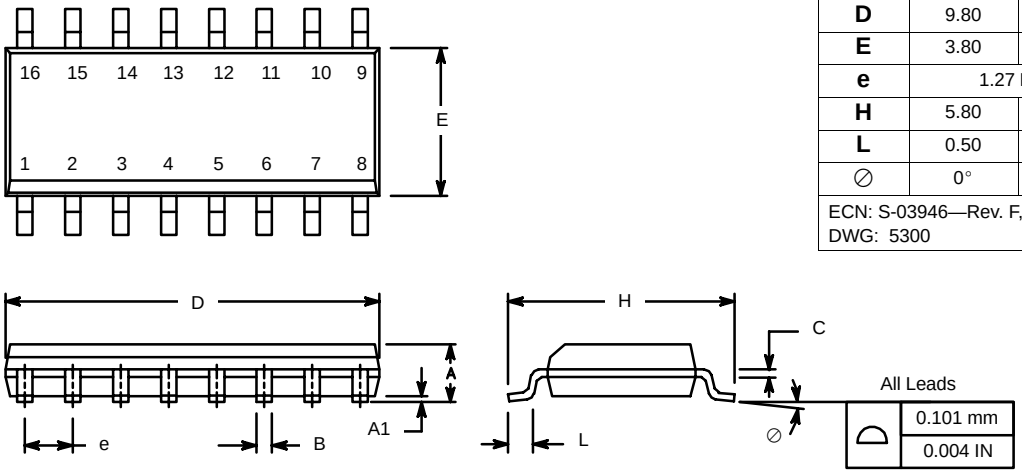
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72053.

SOIC (NARROW): 16-LEAD

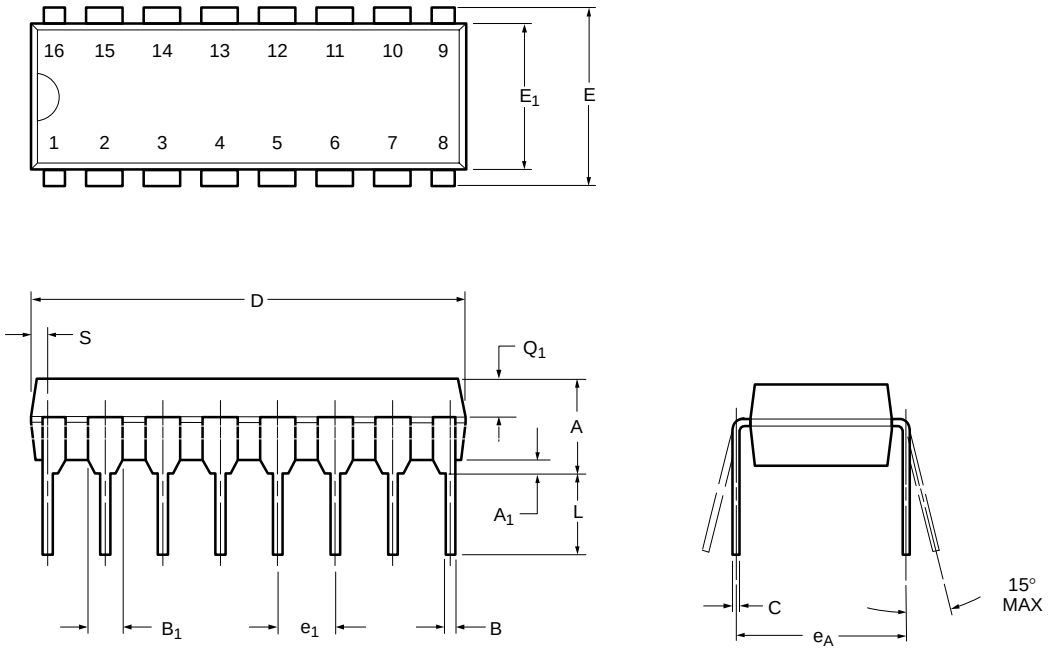
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

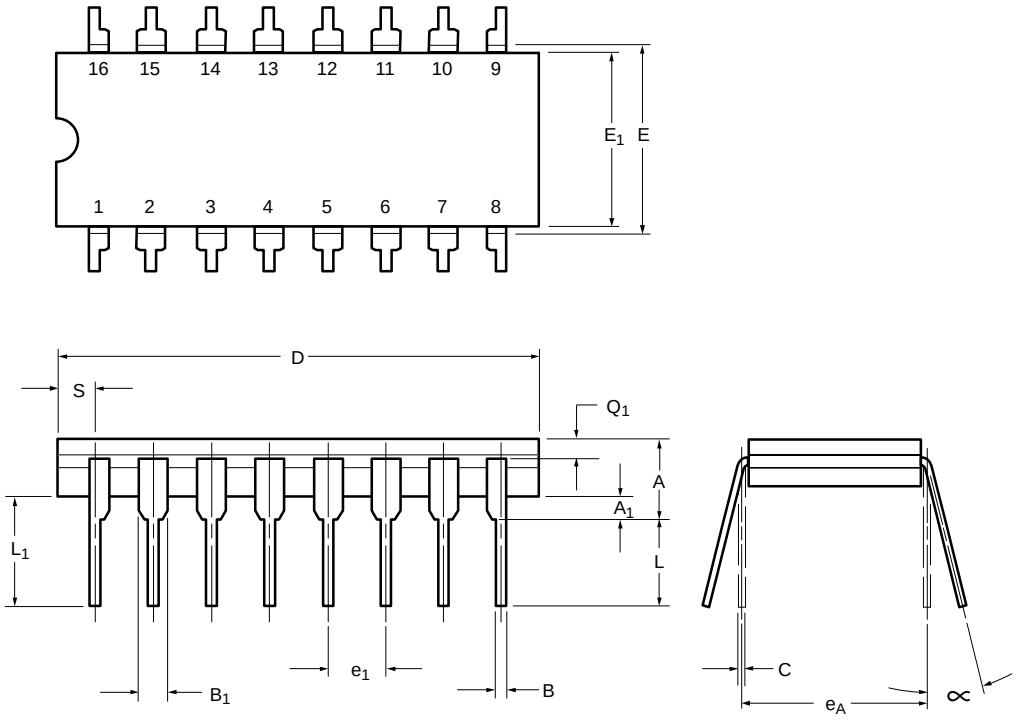


PDIP: 16-LEAD



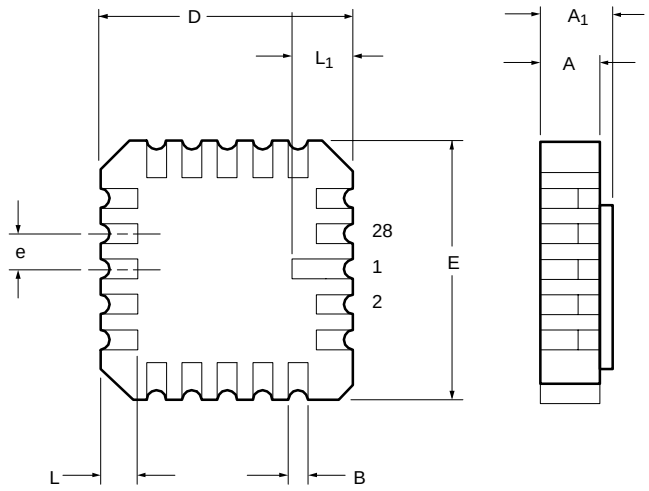
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

CERDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B_1	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E_1	6.60	7.62	0.260	0.300
e_1	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L_1	3.81	5.08	0.150	0.200
Q_1	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∝	0°	15°	0°	15°
ECN: S-03946—Rev. G, 09-Jul-01 DWG: 5403				

20-LEAD LCC

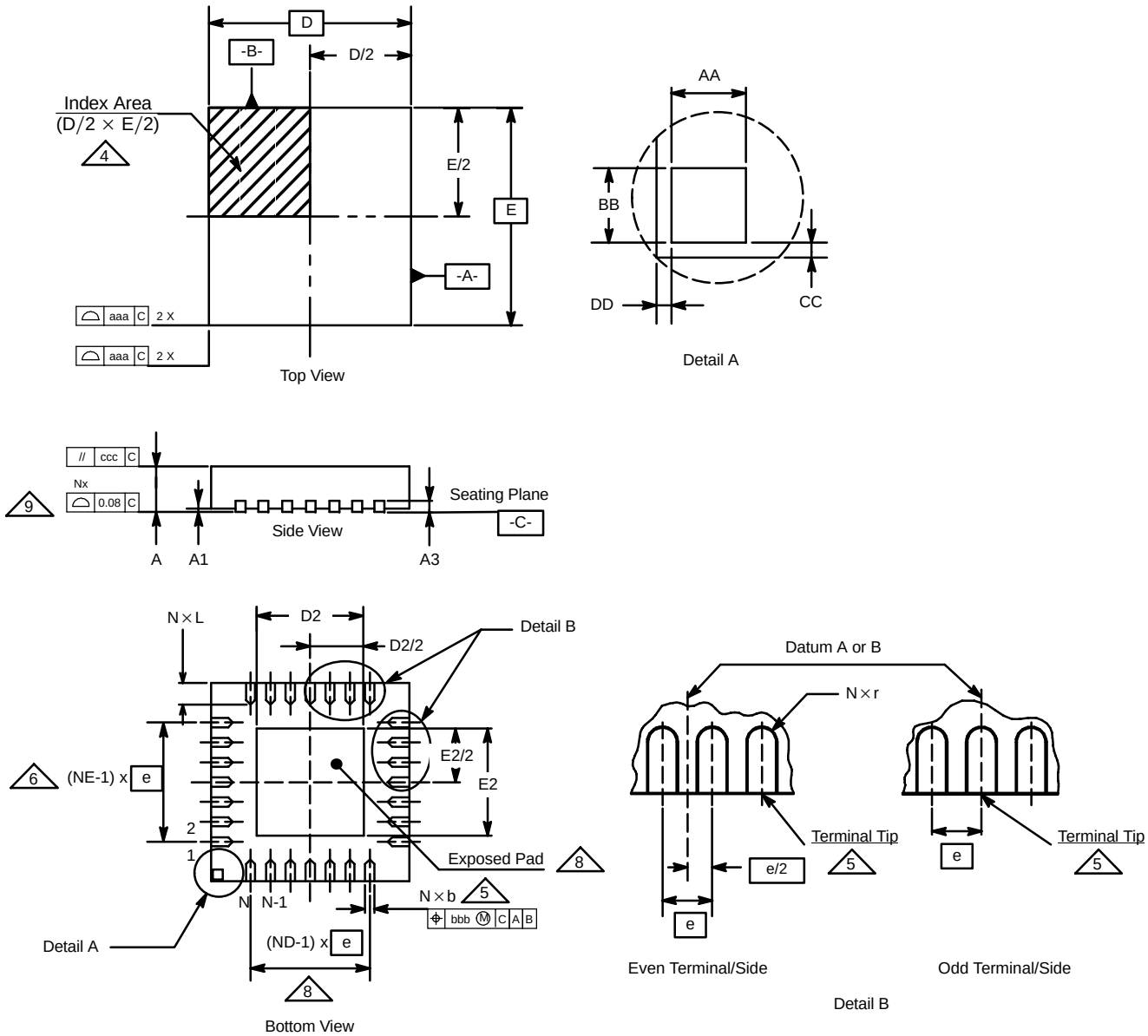


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A_1	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
E	8.69	9.09	0.442	0.358
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L_1	1.96	2.36	0.077	0.093

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5321

QFN-16 (4 × 4 mm)

JEDEC Part Number: MO-220



QFN-16 (4 × 4 mm)
JEDEC Part Number: MO-220

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.0315	0.0354	0.0394	
A1	0	0.02	0.05	0	0.0008	0.0020	
A3	-	0.20 Ref	-	-	0.0079	-	
AA	-	0.345	-	-	0.0136	-	
aaa	-	0.25	-	-	0.0098	-	
BB	-	0.345	-	-	0.0136	-	
b	0.23	0.30	0.38	0.0091	0.0118	0.0150	5
bbb	-	0.10	-	-	0.0039	-	
CC	-	0.18	-	-	0.0071	-	
ccc	-	0.10	-	-	0.0039	-	
D		4.00 BSC			0.1575 BSC		
D2	2.00	2.15	2.25	0.0787	0.0846	0.0886	
DD	-	0.18	-	-	0.0071	-	
E		4.00 BSC			0.1575 BSC		
E2	2.00	2.15	2.25	0.0787	0.0846	0.0886	
e		0.65 BSC			0.0256 BSC		
L	0.45	0.55	0.65	0.0177	0.0217	0.0256	
N		16			16		3, 7
ND	-	4	-	-	4	-	6
NE	-	4	-	-	4	-	6
r	b(min)/2	-	-	b(min)/2	-	-	

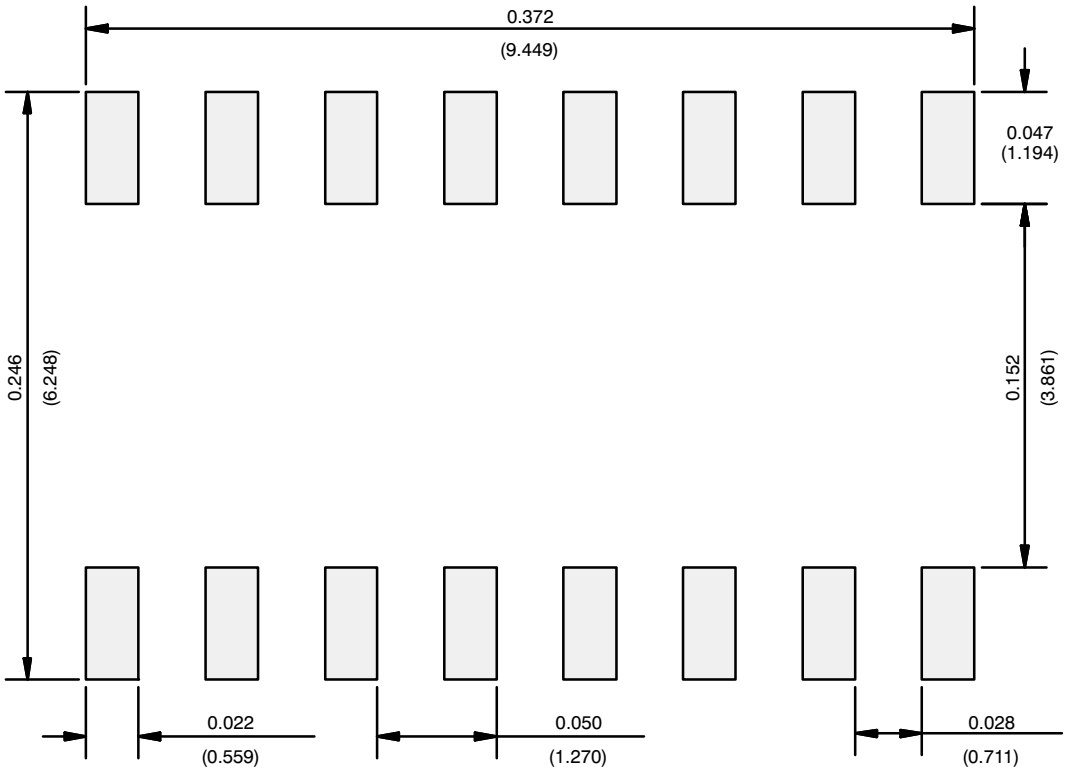
* Use millimeters as the primary measurement.

ECN: S-21437—Rev. A, 19-Aug-02
DWG: 5890

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a molded or marked feature. The X and Y dimension will vary according to lead counts.
5. Dimension b applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.
6. ND and NE refer to the number of terminals on the D and E side respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Variation HHD is shown for illustration only.
9. Coplanarity applies to the exposed heat sink slug as well as the terminals.

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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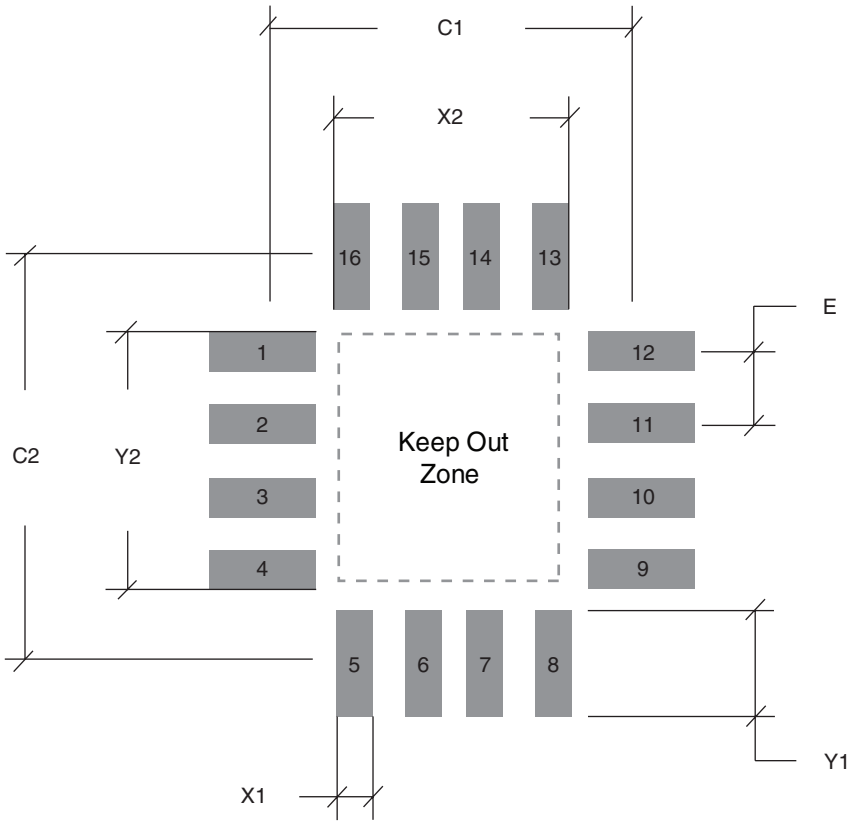
RECOMMENDED MINIMUM PADS FOR QFN-16 (4 x 4 MM BODY)



	Inches	Millimeters
C1	0.142	3.60
C2	0.142	3.60
E	0.026	0.65
X1	0.014	0.35
X2	0.089	2.25
Y1	0.037	0.95
Y2	0.089	2.25

Note:
QFN-16 (4 x 4) has an exposed center pad that must not come into contact with any metalized structure on the PCB. This area is considered a Keep Out Zone.

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