RE46C190

CMOS Low Voltage Photoelectric Smoke Detector ASIC with Interconnect and Timer Mode

Features

- Two AA Battery Operation
- Internal Power On Reset
- Low Quiescent Current Consumption
- Available in 16L N SOIC
- Local Alarm Memory
- Interconnect up to 40 Detectors
- 9 Minute Timer for Sensitivity Control
- Temporal or Continuous Horn Pattern
- Internal Low Battery and Chamber Test
- All Internal Oscillator
- Internal Infrared Emitter Diode (IRED) driver
- Adjustable IRED Drive current
- Adjustable Hush Sensitivity
- 2% Low Battery Set Point

Description

The RE46C190 is a low power, low voltage CMOS photoelectric type smoke detector IC. With minimal external components, this circuit will provide all the required features for a photoelectric-type smoke detector.

The design incorporates a gain-selectable photo amplifier for use with an infrared emitter/detector pair.

An internal oscillator strobes power to the smoke detection circuitry every 10 seconds, to keep the standby current to a minimum. If smoke is sensed, the detection rate is increased to verify an Alarm condition. A high gain mode is available for push button chamber testing.

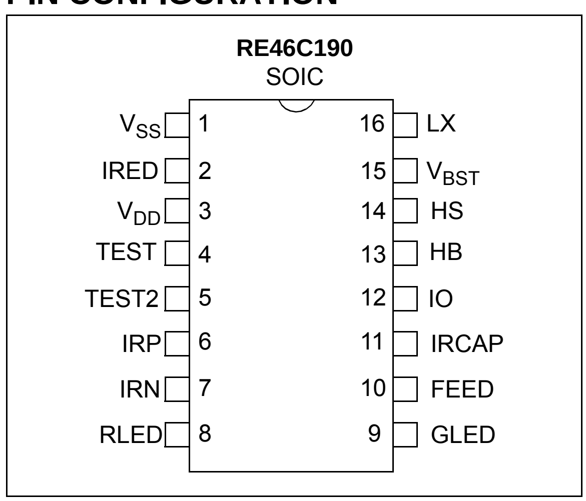
A check for a low battery condition is performed every 86 seconds, and chamber integrity is tested once every 43 seconds, when in Standby. The temporal horn pattern supports the NFPA 72 emergency evacuation signal.

An interconnect pin allows multiple detectors to be connected such that, when one unit alarms, all units will sound.

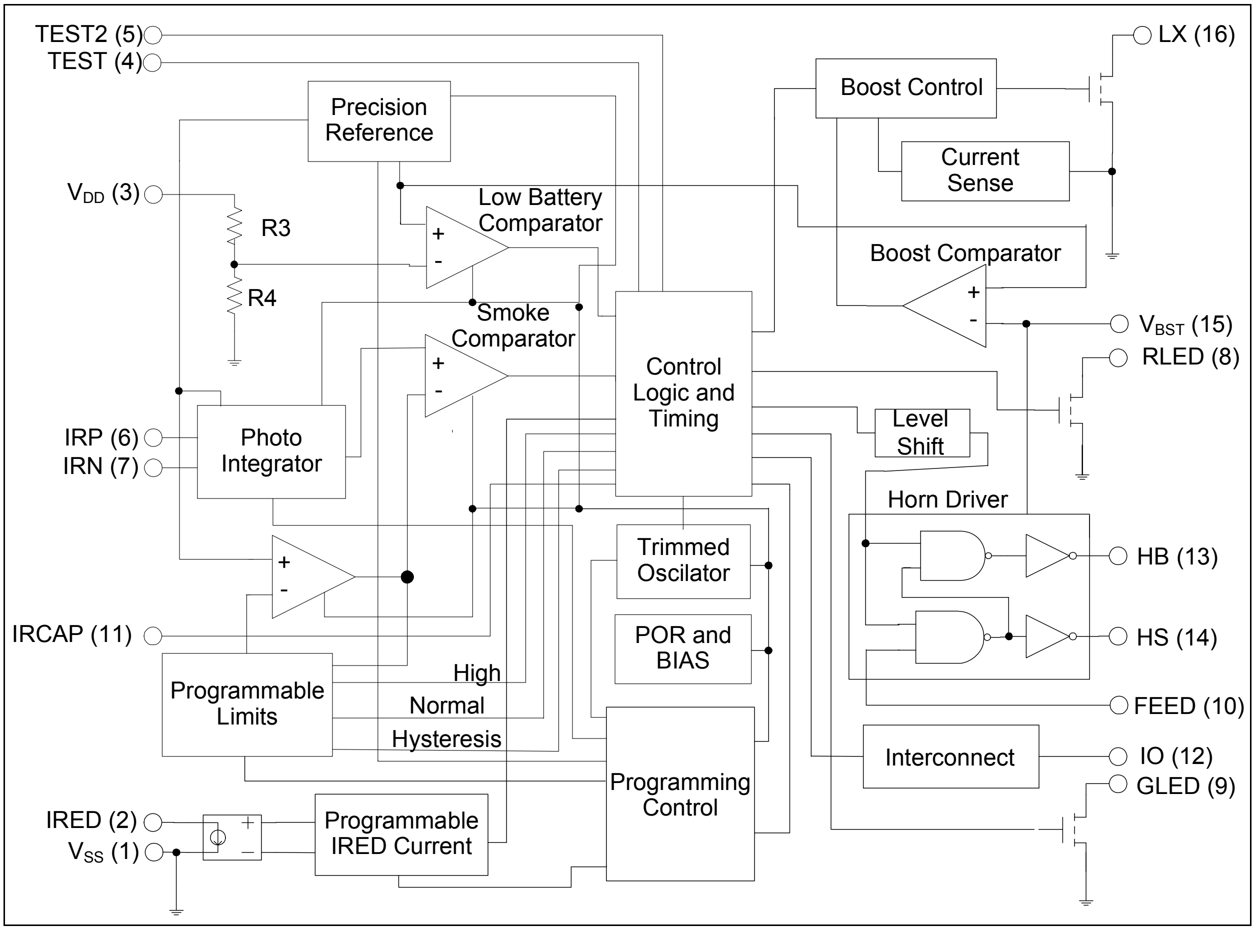
An internal 9 minute timer can be used for a Reduced Sensitivity mode.

Utilizing low power CMOS technology, the RE46C190 was designed for use in smoke detectors that comply with Underwriters Laboratory Specification UL217 and UL268.

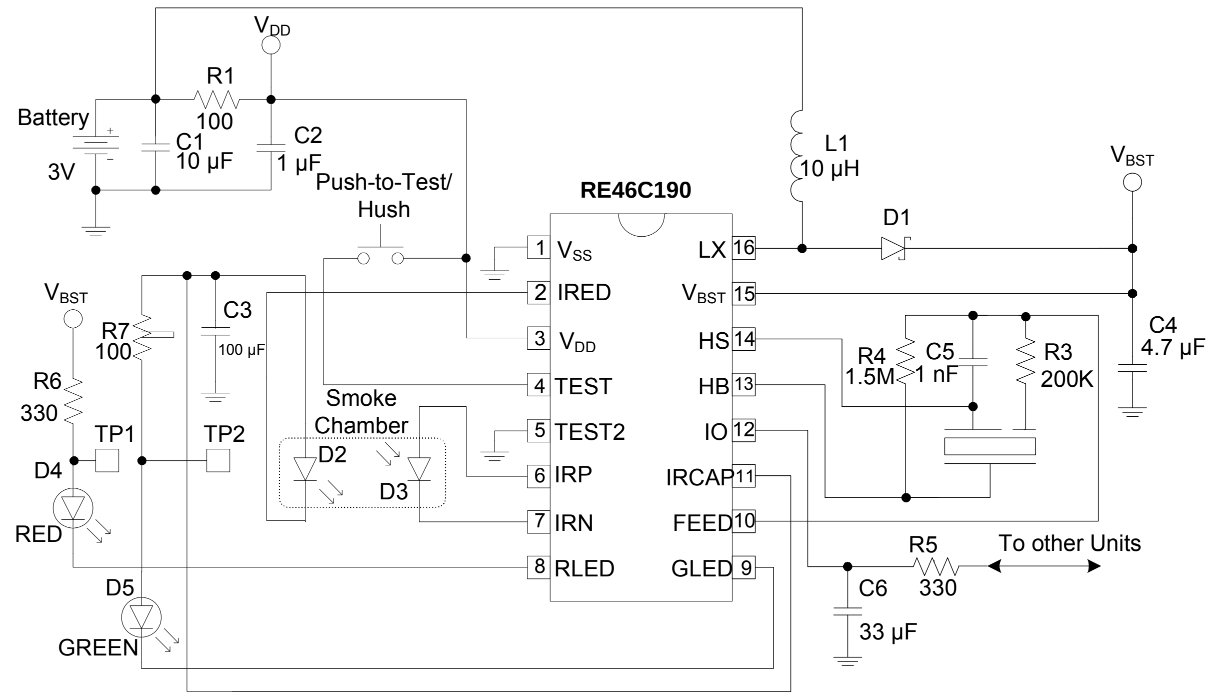
PIN CONFIGURATION



TYPICAL BLOCK DIAGRAM



TYPICAL BATTERY APPLICATION



Note 1: C2 should be located as close as possible to the device power pins, and C1 should be located as close as possible to V_{SS}.

2: R3, R4 and C5 are typical values and may be adjusted to maximize sound pressure.

3: DC-DC converter in High Boost mode (nominal V_{BST} = 9.6V) can draw current pulses of greater than 1A, and is therefore very sensitive to series resistance. Critical components of this resistance are the inductor DC resistance, the internal resistance of the battery and the resistance in the connections from the inductor to the battery, from the inductor to the LX pin and from the V_{SS} pin to the battery. In order to function properly under full load at V_{DD}= 2V, the total of the inductor and interconnect resistances should not exceed 0.3 Ω. The internal battery resistance should be no more than 0.5 Ω, and a low ESR capacitor of 10 µF or more should be connected in parallel with the battery, to average the current draw over the boost converter cycle.

4: Schottky diode D1 must have a maximum peak current rating of at least 1.5A. For best results it should have forward voltage specification of less than 0.5V at 1A, and low reverse leakage.

5: Inductor L1 must have a maximum peak current rating of at least 1.5A.

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ....V_{DD}=5.5V; V_{BST} =13V
Input Voltage Range Except FEED, TEST..... V_{IN} = -.3V to V_{DD} +.3V
FEED Input Voltage Range..................... V_{INFD} =-10 to +22V
TEST Input Voltage Range .... V_{INTEST} =-.3V to V_{BST}+.3V
Input Current except FEED.................................. I_{IN} = 10 mA
Continuous Operating Current (HS, HB, V_{BST})...... I_O= 40 mA
Continuous Operating Current (IRED) ....I_{OIR}= 300 mA
Operating Temperature ....T_A = -10 to +60°C
Storage Temperature ....T_{STG} = -55 to +125°C
ESD Human Body Model .... V_{HBM} = 750V
ESD Machine Model ....V_{MM} = 75V

† **Notice:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10 to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted)(**Note 1**, **Note 2**, **Note 3**)

Parameter	Symbol	Test Pin	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	3	2	—	5.0	V	Operating
Supply Current	I_{DD1}	3	—	1	2	µA	Standby, Inputs low, No loads, Boost Off, No smoke check
Standby Boost Current	I_{BST1}	15	—	100	—	nA	Standby, Inputs low, No loads, Boost Off, No smoke check
IRCAP Supply Current	I_{IRCAP}	11	—	500	—	µA	During smoke check
Boost Voltage	V_{BST1}	15	3.0	3.6	4.2	V	IRCAP charging for Smoke Check, GLED operation I_{OUT} = 40 mA
	V_{BST2}	15	8.5	9.6	10.7	V	No local alarm, RLED Operation, I_{OUT} = 40 mA, IO as an input
Input Leakage	I_{INOP}	6	-200	—	200	pA	IRP = V_{DD} or V_{SS}
		7	-200	—	200	pA	IRN = V_{DD} or V_{SS}
	I_{IHF}	10	—	20	50	µA	FEED = 22V; V_{BST} = 9V
	I_{ILF}	10	-50	-15	—	µA	FEED = -10V; V_{BST} = 10.7V
Input Voltage Low	V_{IL1}	10	—	—	2.7	V	FEED, V_{BST} = 9V
	V_{IL2}	12	—	—	800	mV	No local alarm, IO as an input

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guardbanded limits.

4: Not production tested.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10 to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted)(**Note 1**, **Note 2**, **Note 3**)

Parameter	Symbol	Test Pin	Min	Typ	Max	Units	Conditions
Input Voltage High	V_{IH1}	10	6.2	—	—	V	FEED; V_{BST} = 9V
	V_{IH2}	12	2.0	—	—	V	No local alarm, IO as an input
IO Hysteresis	V_{HYST1}	12	—	150	—	mV	
Input Pull Down Current	I_{PD1}	4, 5	0.25	—	10	µA	$V_{IN} = V_{DD}$
	I_{PDIO1}	12	20	—	80	µA	$V_{IN} = V_{DD}$
	I_{PDIO2}	12	—	—	140	µA	V_{IN} = 15V
Output Voltage Low	V_{OL1}	13, 14	—	—	1	V	I_{OL} = 16 mA, V_{BST} = 9V
	V_{OL2}	8	—	—	300	mV	I_{OL} = 10 mA, V_{BST} = 9V
	V_{OL3}	9	—	—	300	mV	I_{OL} = 10 mA, V_{BST} = 3.6V
Output High Voltage	V_{OH1}	13, 14	8.5	—	—	V	I_{OL} = 16 mA, V_{BST} = 9V
Output Current	I_{IOH1}	12	-4	-5	—	mA	Alarm, V_{IO} = 3V or V_{IO} = 0V, V_{BST} = 9V
	I_{IODMP}	12	5	30	—	mA	At Conclusion of Local Alarm or Test, V_{IO}=1V
	I_{IRED50}	2	45	50	55	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (50 mA option selected; T_A = 27°C)
	$I_{IRED100}$	2	90	100	110	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (100 mA option selected; T_A = 27°C)
	$I_{IRED150}$	2	135	150	165	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (150 mA option selected; T_A = 27°C)
	$I_{IRED2050}$	2	180	200	220	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (200 mA option selected; T_A = 27°C)
IRED Current Temperature Coefficient	TC_{IRED}		—	0.5	—	%/°C	V_{BST} = 5V, IRCAP = 5V; **Note 4**

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guardbanded limits.

4: Not production tested.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10 to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted)(**Note 1**, **Note 2**, **Note 3**)

Parameter	Symbol	Test Pin	Min	Typ	Max	Units	Conditions
Low Battery Alarm Voltage	V_{LB1}	3	2.05	2.1	2.15	V	Falling Edge; 2.1V nominal selected
	V_{LB2}	3	2.15	2.2	2.25	V	Falling Edge; 2.2V nominal selected
	V_{LB3}	3	2.25	2.3	2.35	V	Falling Edge; 2.3V nominal selected
	V_{LB4}	3	2.35	2.4	2.45	V	Falling Edge; 2.4V nominal selected
	V_{LB5}	3	2.45	2.5	2.55	V	Falling Edge; 2.5V nominal selected
	V_{LB6}	3	2.55	2.6	2.65	V	Falling Edge; 2.6V nominal selected
	V_{LB7}	3	2.65	2.7	2.75	V	Falling Edge; 2.7V nominal selected
	V_{LB8}	3	2.75	2.8	2.85	V	Falling Edge; 2.8V nominal selected
Low Battery Hysteresis	V_{LBHYST}	3	—	100	—	mV	
IRCAP Turn On Voltage	V_{TIR1}	11	3.6	4.0	4.4	V	Falling edge; V_{BST} = 5V; I_{OUT} = 20 mA
IRCAP Turn Off Voltage	V_{TIR2}	11	4.0	4.4	4.8	V	Rising edge; V_{BST} = 5V; I_{OUT} = 20 mA

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guardbanded limits.

4: Not production tested.

AC ELECTRICAL CHARACTERISTICS

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted) (**Note 1** to **Note 4**).							
Parameter	**Symbol**	**Test Pin**	**Min**	**Typ**	**Max**	**Units**	**Condition**
Time Base							
Internal Clock Period	T_{PCLK}		9.80	10.4	11.0	ms	PROGSET, IO = high
RLED Indicator							
On Time	T_{ON1}	8	9.80	10.4	11.0	ms	Operating
Standby Period	T_{PLED1}	8	320	344	368	s	Standby, no alarm
Local Alarm Period	T_{PLED2A}	8	470	500	530	ms	Local alarm condition with temporal horn pattern
	T_{PLED2B}	8	625	667	710	ms	Local alarm condition with continuous horn pattern
Hush Timer Period	T_{PLED4}	8	10	10.7	11.4	s	Timer mode, no local alarm
External Alarm Period	T_{PLED0}	8		LED IS NOT ON		s	Remote alarm only
GLED Indicator							
Latched Alarm Period	T_{PLED3}	9	40	43	46	s	Latched Alarm Condition, LED enabled
Latched Alarm Pulse Train (3x) Off Time	T_{OFLED}	9	1.25	1.33	1.41	s	Latched Alarm Condition, LED enabled
Latched Alarm LED Enabled Duration	T_{LALED}	9	22.4	23.9	25.3	Hours	Latched Alarm Condition, LED enabled
Smoke Check							
Smoke Test Period with Temporal Horn Pattern	T_{PER0A}	2	10	10.7	11.4	s	Standby, no alarm
	T_{PER1A}	2	1.88	2.0	2.12	s	Standby, after one valid smoke sample
	T_{PER2A}	2	0.94	1.0	1.06	s	Standby, after two consecutive valid smoke samples
	T_{PER3A}	2	0.94	1.0	1.06	s	Local Alarm (three consecutive valid smoke samples)
	T_{PER4A}	2	235	250	265	ms	Push button test, >1 chamber detections
			313	333	353	ms	Push button test, no chamber detections
	T_{PER5A}	2	7.5	8.0	8.5	s	In remote alarm

Note 1: See timing diagram for Horn Pattern (Figure 5-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested, and are based on characterization data.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted) (**Note 1** to **Note 4**).

Parameter	Symbol	Test Pin	Min	Typ	Max	Units	Condition
Smoke Test Period with Continuous Horn Pattern	T_{PER0B}	2	10	10.7	11.4	s	Standby, no alarm
	T_{PER1B}	2	2.5	2.7	2.9	s	Standby, after one valid smoke sample
	T_{PER2B}	2	1.25	1.33	1.41	s	Standby, after two consecutive valid smoke samples
	T_{PER3B}	2	1.25	1.33	1.41	s	Local Alarm (three consecutive valid smoke samples)
	T_{PER4B}	2	313	333	353	ms	Push button test
	T_{PER5B}	2	10	10.7	11.4	s	In remote alarm
Chamber Test Period	T_{PCT1}	2	40	43	46	s	Standby, no alarm
Long Term Drift Sample Period	T_{LTD}	2	400	430	460	s	Standby, no alarm LTD enabled
Low Battery							
Low Battery Sample Period	T_{PLB1}	3	320	344	368	s	RLED on
	T_{PLB2}	3	80	86	92	s	RLED on
Horn Operation							
Low Battery Horn Period	T_{HPER1}	13	40	43	46	s	Low battery, no alarm
Chamber Fail Horn Period	T_{HPER2}	13	40	43	46	s	Chamber failure
Low Battery Horn On Time	T_{HON1}	13	9.8	10.4	11.0	ms	Low battery, no alarm
Chamber Fail Horn On Time	T_{HON2}	13	9.8	10.4	11.0	ms	Chamber failure
Chamber Fail Off Time	T_{HOF1}	13	305	325	345	ms	Failed chamber, no alarm, 3x chirp option
Alarm On Time with Temporal Horn Pattern	T_{HON2A}	13	470	500	530	ms	Local or remote alarm (**Note 1**)
Alarm Off Time with Temporal Horn Pattern	T_{HOF2A}	13	470	500	530	ms	Local or remote alarm (**Note 1**)
	T_{HOF3A}	13	1.4	1.5	1.6	s	Local or remote alarm (**Note 1**)
Alarm On Time with Continuous Horn Pattern	T_{HON2B}	13	235	250	265	ms	Local or remote alarm (**Note 1**)
Alarm Off Time with Continuous Horn Pattern	T_{HOF2B}	13	78	83	88	ms	Local or remote alarm (**Note 1**)

Note 1: See timing diagram for Horn Pattern (Figure 5-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested, and are based on characterization data.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 3V, V_{BST} = 4.2V, Typical Application (unless otherwise noted) (Note 1 to Note 4).

Parameter	Symbol	Test Pin	Min	Typ	Max	Units	Condition
Push-to-Test Alarm Memory On Time	T_{HON4}	13	9.8	10.4	11.0	ms	Alarm memory active, push-to-test
Push-to-Test Alarm Memory Horn Period	T_{HPER4}	13	235	250	265	ms	Alarm memory active, push-to-test
Interconnect Signal Operation (IO)							
IO Active Delay	T_{IODLY1}	12	—	0	—	s	From start of local alarm to IO active
Remote Alarm Delay with Temporal Horn Pattern	$T_{IODLY2A}$	12	0.780	1.00	1.25	s	No local alarm, from IO active to alarm
Remote Alarm Delay with Continuous Horn Pattern	$T_{IODLY2B}$	12	380	572	785	ms	No local alarm, from IO active to alarm
IO Charge Dump Duration	T_{IODMP}	12	1.23	1.31	1.39	s	At conclusion of local alarm or test
IO Filter	T_{IOFILT}	12	—	—	313	ms	Standby, no alarm
Hush Timer Operation							
Hush Timer Period	T_{TPER}		8.0	8.6	9.1	Min	No alarm
EOL							
End-of-Life Age Sample	T_{EOL}		314	334	354	Hours	EOL Enabled; Standby
Detection							
IRED On Time	T_{IRON}	2	—	100	—	µs	Prog Bits 3,4 = 1,1
		2	—	200	—	µs	Prog Bits 3,4 = 0,1
		2	—	300	—	µs	Prog Bits 3,4 = 1,0
		2	—	400	—	µs	Prog Bits 3,4 = 0,0

Note 1: See timing diagram for Horn Pattern (Figure 5-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested, and are based on characterization data.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: All limits specified for V_{DD} = 3V, V_{BST} = 4.2V and V_{SS} = 0V, Except where noted in the Electrical Characteristics.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-10	—	+60	°C	
Storage Temperature Range	T_{STG}	-55	—	+125	°C	
Thermal Package Resistances						
Thermal Resistance, 16L-SOIC (150 mil.)	θ_{JA}	—	86.1	—	°C/W	

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

RE46C190 SOIC	**Symbol**	**Function**
1	V_{SS}	Connect to the negative supply voltage.
2	IRED	Provides a regulated and programmable pulsed current for the infrared emitter diode.
3	V_{DD}	Connect to the positive supply or battery voltage.
4	TEST	This input is used to invoke Test modes and the Timer mode. This input has an internal pull-down.
5	TEST2	Test input for test and programming modes. This input has an internal pull-down.
6	IRP	Connect to the anode of the photo diode.
7	IRN	Connect to the cathode of the photo diode.
8	RLED	Open drain NMOS output, used to drive a visible LED. This pin provides load current for the low battery test, and is a visual indicator for Alarm and Hush modes.
9	GLED	Open drain NMOS output used to drive a visible LED to provide visual indication of an Alarm Memory condition.
10	FEED	Usually connected to the feedback electrode through a current limiting resistor. If not used, this pin must be connected to V_{DD} or V_{SS}.
11	IRCAP	Used to charge and monitor the IRED capacitor.
12	IO	This bidirectional pin provides the capability to interconnect many detectors in a single system. This pin has an internal pull-down device and a charge dump device.
13	HB	This pin is connected to the metal electrode of a piezoelectric transducer.
14	HS	This pin is a complementary output to HB, connected to the ceramic electrode of the piezoelectric transducer.
15	V_{BST}	Boosted voltage produced by DC-DC converter.
16	LX	Open drain NMOS output, used to drive the boost converter inductor. The inductor should be connected from this pin to the positive supply through a low resistance path.

NOTES:

3.0 DEVICE DESCRIPTION

3.1 Standby Internal Timing

The internal oscillator is trimmed to ±6% tolerance. Once every 10 seconds, the boost converter is powered up, the IRcap is charged from V_{BST} and then the detection circuitry is active for 10 ms. Prior to completion of the 10 mS period, the IRED pulse is active for a user-programmable duration of 100-400 µs. During this IRED pulse, the photo diode current is integrated and then digitized. The result is compared to a limit value stored in EEPROM during calibration to determine the photo chamber status. If a smoke condition is present, the period to the next detection decreases, and additional checks are made.

3.2 Smoke Detection Circuitry

The digitized photo amplifier integrator output is compared to the stored limit value at the conclusion of the IRED pulse period. The IRED drive is all internal, and both the period and current are user programmable. Three consecutive smoke detections will cause the device to go into Alarm and activate the horn and interconnect circuits. In Alarm, the horn is driven at the high boost voltage level, which is regulated based on an internal voltage reference, and therefore results in consistent audibility over battery life. RLED will turn on for 10 ms at a 2 Hz rate. In Local Alarm, the integration limit is internally decreased to provide alarm hysteresis. The integrator has three separate gain settings:

- Normal and Hysteresis
- Reduced Sensitivity (HUSH)
- High Gain for Chamber Test and Push-to-Test

There are four separate sets of integration limits (all user programmable):

- Normal Detection
- Hysteresis
- HUSH
- Chamber Test and Push-to-Test modes

In addition, there are user selectable integrator gain settings to optimize detection levels (see Table 4-1).

3.3 Supervisory Tests

Once every 86 seconds, the status of the battery voltage is checked by enabling the boost converter for 10 ms and comparing a fraction of the V_{DD} voltage to an internal reference. In each period of 344 seconds, the battery voltage is checked four times. Three checks are unloaded and one check is performed with the RLED enabled, which provides a battery load. The High Boost mode is active only for the loaded low battery test. In addition, once every 43 seconds the chamber is activated and a High Gain mode and chamber test limits are internally selected. A check of the chamber is made by amplifying background reflections. The Low Boost mode is used for the chamber test.

If either the low battery test or the chamber test fails, the horn will pulse on for 10 ms every 43 seconds, and will continue to pulse until the failing condition passes. If two consecutive chamber tests fail, the horn will pulse on three times for 10 ms, separated by 330 ms every 43 seconds. Each of the two supervisory test audible indicators is separated by approximately 20 seconds.

As an option, a Low Battery Silence mode can be invoked. If a low battery condition exists, and the TEST input is driven high, the RLED will turn on. If the TEST input is held for more than 0.5 second, the unit will enter the Push-to-test operation described in **Section 3.4 "Push-to-Test Operation (PTT)"**. After the TEST input is driven low, the unit enters in Low Battery Hush mode, and the 10 ms horn pulse is silenced for 8 hours. The activation of the test button will also initiate the 9 minute Reduced Sensitivity mode described in **Section 3.6 "Reduced Sensitivity Mode"**. At the end of the 8 hours, the audible indication will resume if the low battery condition still exists.

3.4 Push-to-Test Operation (PTT)

If the TEST input pin is activated (V_{IH}), the smoke detection rate increases to once every 250 ms after one internal clock cycle. In Push-to-Test, the photo amplifier High Gain mode is selected, and background reflections are used to simulate a smoke condition. After the required three consecutive detections, the device will go into a Local Alarm condition. When the TEST input is driven low (V_{IL}), the photo amplifier Normal Gain is selected, after one clock cycle. The detection rate continues at once every 250 ms until three consecutive No Smoke conditions are detected. At this point, the device returns to standby timing. In addition, after the TEST input goes low, the device enters the HUSH mode (see **Section 3.6 "Reduced Sensitivity Mode"**).

3.5 Interconnect Operation

The bidirectional IO pin allows the interconnection of multiple detectors. In a Local Alarm condition, this pin is driven high (High Boost) immediately through a constant current source. Shorting this output to ground will not cause excessive current. The IO is ignored as input during a Local Alarm.

The IO pin also has an NMOS discharge device that is active for 1.3 seconds after the conclusion of any type of Local Alarm. This device helps to quickly discharge any capacitance associated with the interconnect line.

If a remote, active high signal is detected, the device goes into Remote Alarm and the horn will be active. RLED will be off, indicating a Remote Alarm condition. Internal protection circuitry allows the signaling unit to have a higher supply voltage than the signaled unit, without excessive current draw.

The interconnect input has a 336 ms nominal digital filter. This allows the interconnection to other types of alarms (carbon monoxide, for example) that may have a pulsed interconnect signal.

3.6 Reduced Sensitivity Mode

A Reduced Sensitivity or Hush mode is initiated by activating the TEST input (V_{IH}). If the TEST input is activated during a Local Alarm, the unit is immediately reset out of the alarm condition, and the horn is silenced. When the TEST input is deactivated (V_{IL}), the device enters into a 9-minute nominal Hush mode. During this period, the HUSH integration limit is selected. The hush gain is user programmable. In Reduced Sensitivity mode, the RLED flashes for 10 ms every 10 seconds to indicate that the mode is active. As an option, the Hush mode will be cancelled if any of the following conditions exist:

- Reduced sensitivity threshold is exceeded (high smoke level)
- An interconnect alarm occurs
- TEST input is activated again

3.7 Local Alarm Memory

An Alarm Memory feature allows easy identification of any unit that had previously been in a Local Alarm condition. If a detector has entered a Local Alarm, when it exits that Local Alarm, the Alarm Memory latch is set. Initially the GLED can be used to visually identify any unit that had previously been in a Local Alarm condition. The GLED flashes three times spaced 1.3 seconds apart. This pattern will repeat every 43 seconds. The duration of the flash is 10 ms. In order to preserve battery power, this visual indication will stop after a period of 24 hours. The user will still be able to identify a unit with an active alarm memory by pressing the Push-to-Test button. When this button is active, the horn will chirp for 10 ms every 250 ms.

If the Alarm Memory condition is set, then any time the Push-to-Test button is pressed and released, the Alarm Memory latch is reset.

The initial 24 hour visual indication is not displayed if a low battery condition exists.

3.8 End of Life Indicator

As an option, after every 14 days of continuous operation, the device will read a stored age count from the EEPROM and increment this count. After 10 years of powered operation, an audible warning will occur indicating that the unit should be replaced. This indicator will be similar to the chamber test failure warning in that the horn will pulse on three times for 10 ms separated by 330 ms every 43 seconds. This indicator will be separated from the low battery indicator by approximately 20 seconds.

3.9 Photo Chamber Long Term Drift Adjustment

As an option, the design includes a Long Term Drift Adjustment for the photo chamber. If this option is selected, during calibration a normal no-smoke baseline integration measurement is made and stored in EEPROM. During normal operation, a new baseline is calculated by making 64 integration measurements over a period of 8 hours. These measurements are averaged and compared to the original baseline stored during calibration to calculate the long term drift. All four limits stored during calibration are adjusted by this drift factor. Drift sampling is suspended during Hush, Local Smoke and Remote Smoke conditions.

4.0 USER PROGRAMMING MODES

TABLE 4-1: PARAMETRIC PROGRAMMING

Parametric Programming		Range		Resolution	
IRED Period		100-400 µs		100 µs	
IRED Current Sink		50-200 mA		50 mA	
Low Battery Detection Voltage		2.1 – 2.8V		100 mV	
Photo Detection Limits		Typical Maximum Input Current (nA)			
		100 µs	200 µs	300 µs	400 µs
Normal/Hysteresis	GF = 1	58	29	19.4	14.5
	GF = 2	29	14.5	9.6	7.2
	GF = 3	14.5	7.2	4.8	3.6
	GF = 4	7.2	3.6	2.4	1.8
Hush	GF = 1	116	58	38.8	29
	GF = 2	58	29	19.4	14.5
	GF = 3	29	14.5	9.6	7.2
	GF = 4	14.5	7.2	4.8	3.6
Chamber Test	GF = 1	29	14.5	9.6	7.2
	GF = 2	14.5	7.2	4.8	3.6
	GF = 3	7.2	3.6	2.4	1.8
	GF = 4	3.6	1.8	1.2	0.9

Note 1: GF is the user selectable Photo Integration Gain Factor. Once selected, it applies to all modes of operation. For example, if GF = 1 and integration time is selected to be 100 µs, the ranges will be as follows: Normal/Hysteresis = 58 nA, Hush = 116 nA, Chamber Test = 29 nA.

2: Nominal measurement resolution in each case will be 1/31 of the maximum input range.

3: The same current resolution and ranges applies to the limits.

TABLE 4-2: FEATURES PROGRAMMING

Features	Options
Tone Select	Continuous or NFPA Tone
10 Year End-of-life Indicator	Enable/Disable
Photo Chamber Long Term Drift Adjustment	Enable/Disable
Low Battery Hush	Enable/Disable
Hush Options	Option 1: Hush mode is not cancelled for any reason. If the test button is pushed during Hush, the unit reverts to Normal Sensitivity to test the unit, but when it comes out of test, resumes in Hush where it left off.
	Option 2: The Hush mode is cancelled if the Reduced Sensitivity threshold is exceeded (high smoke level), and if an external (interconnect alarm) is signaled. If the test button is pushed during Hush, after the test is executed, the Hush mode is terminated.

4.1 Calibration and Programming Procedures

Eleven separate programming and test modes are available for user customization. To enter these modes, after power-up, TEST2 must be driven to V_{DD} and held at that level. The TEST input is then clocked to step through the modes. FEED and IO are reconfigured to become test mode inputs, while RLED, GLED and HB become test mode outputs. The test mode functions for each pin are outlined in Table 4-3.

When TEST2 is held at V_{DD}, TEST becomes a tri-state input with nominal input levels at V_{SS}, V_{DD} and V_{BST}. A TEST clock occurs whenever the TEST input switches from V_{SS} to V_{BST}. The TEST Data column represents the state of TEST when used as a data input, which would be either V_{SS} or V_{DD}. The TEST pin can therefore be used as both a clock, to change modes, and a data input, once a mode is set. Other pin functions are described in **Section 4.2 "User Selections"**.

TABLE 4-3: TEST MODE FUNCTIONS

Mode	Description	TEST Clock	TEST Data	TEST2	FEED	IO	RLED	GLED	HB
	V_{IH}	V_{BST}	V_{DD}	V_{DD}	V_{BST}	V_{DD}	—	—	—
	V_{IL}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	—	—	—
T0	Photo Gain Factor (2 bits)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Integ Time (2 bits)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	IRED Current (2 bits)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Low Battery Trip (3 bits)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	LTD Enable (1 bit)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Hush Option (1 bit)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	LB Hush Enable (1 bit)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	EOL Enable (1 bit)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Tone Select (1 bit)	0	ProgData	V_{DD}	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
T1	Norm Lim Set (5 bits)(4)	1	not used	V_{DD}	CalCLK	LatchLim(3)	Gamp	IntegOut	SmkComp(1)
T2	Hyst Lim Set (5 bits)(4)	2	not used	V_{DD}	CalCLK	LatchLim(3)	Gamp	IntegOut	SmkComp(1)
T3	Hush Lim Set (5 bits)(4)	3	not used	V_{DD}	CalCLK	LatchLim(3)	Gamp	IntegOut	SmkComp(1)
T4	Ch Test Lim Set (5 bits)(4)	4	not used	V_{DD}	CalCLK	LatchLim(3)	Gamp	IntegOut	SmkComp(1)
T5	LTD Baseline (5 bits)	5	not used	V_{DD}	MeasEn	ProgEn 25 bits	Gamp	IntegOut	SmkComp(1)
T6	Serial Read/Write	6	ProgData	V_{DD}	ProgCLK	ProgEn	RLED	GLED	Serial Out
T7	Norm Lim Check	7	not used	V_{DD}	MeasEn	not used	Gamp	IntegOut	SCMP(2)
T8	Hyst Lim Check	8	not used	V_{DD}	MeasEn	not used	Gamp	IntegOut	SCMP(2)
T9	Hush Lim Check	9	not used	V_{DD}	MeasEn	not used	Gamp	IntegOut	SCMP(2)
T10	Ch Test Lim Check	10	not used	V_{DD}	MeasEn	not used	Gamp	IntegOut	SCMP(2)
T11	Horn Test	11	not used	V_{DD}	FEED	HornEn	RLED	GLED	HB

Note 1: SmkComp (HB) – digital comparator output (high if Gamp < IntegOut; low if Gamp > IntegOut)

2: SCMP (HB) – digital output representing comparison of measurement value and associated limit. Signal is valid only after MeasEn has been asserted and measurement has been made. (SCMP high if measured value > limit; low if measured value < limit).

3: LatchLim (IO) – digital input used to latch present state of limits (Gamp level) for later storage. T1-T4 limits are latched, but not stored until ProgEn is asserted in T5 mode.

4: Operating the circuit in this manner with nearly continuous IRED current for an extended period of time may result in undesired or excessive heating of the part. The duration of this step should be minimized.

4.2 User Selections

Prior to smoke calibration, the user must program the functional options and parametric selections. This requires that 14 bits, representing selected values, be clocked in serially using TEST as a data input and FEED as a clock input, and then be stored in the internal EEPROM.

The detailed steps are as follows:

1. Power up with bias conditions as shown in Figure 4-1. At power-up TEST = TEST2 = FEED = IO = V_{SS}.

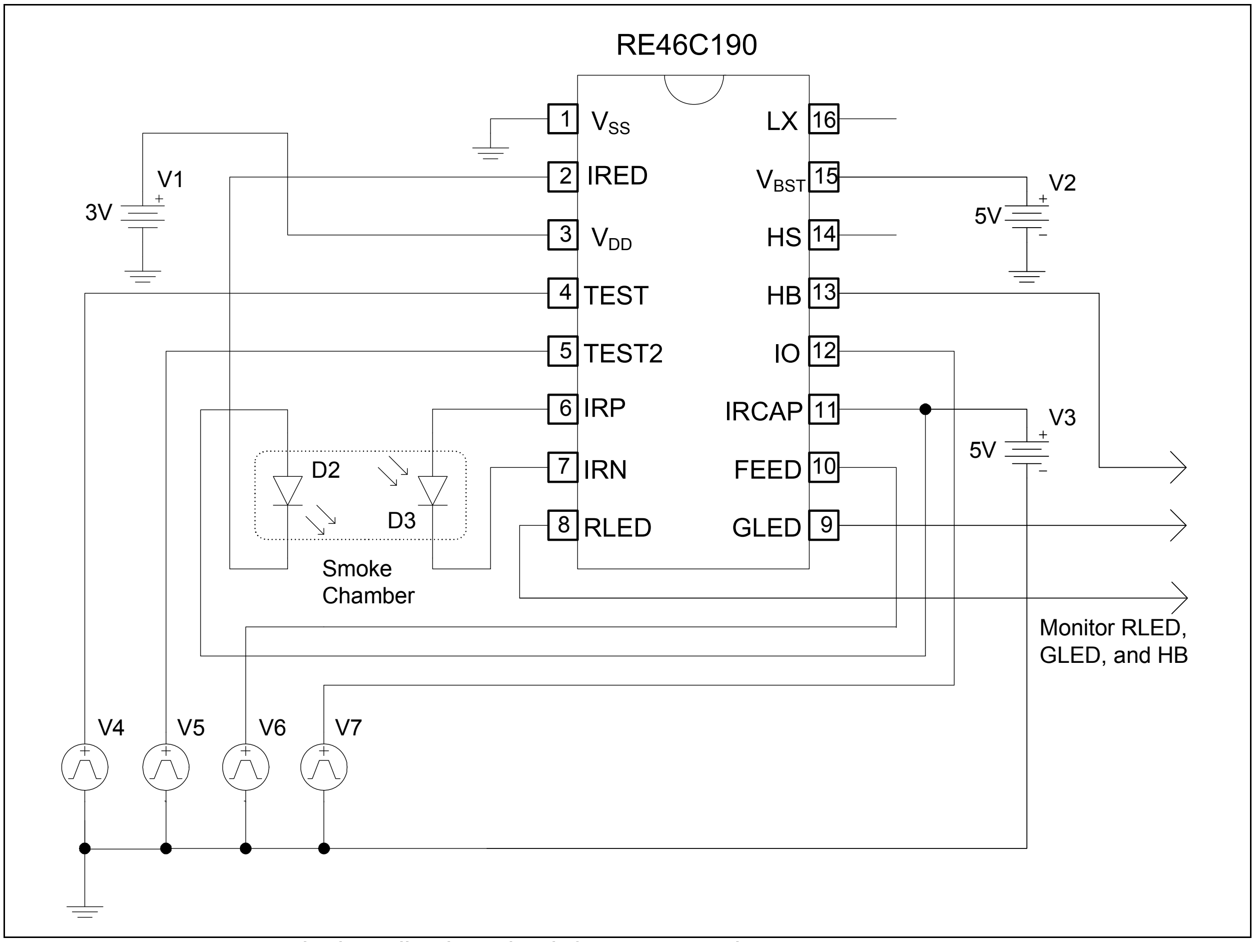


FIGURE 4-1: *Nominal Application Circuit for Programming.*

2. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} through Step 5 below.
3. Using TEST as data and FEED as clock, shift in values as selected from Register 4-1.

Note: For test mode T0 only 14 bits (bits 25-38) will be loaded. For test mode T6 all 39 bits (bits 0-38), will be loaded.

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER

W-x	W-x	W-x	W-x	W-x	W-x	W-x
TS	EOL	LBH	HUSH	LTD	LB0	LB1
bit 38						bit 32

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
LB2	IRC1	IRC0	IT1	IT0	PAGF1	PAGF0	NL4
bit 31							bit 24

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
NL3	NL2	NL1	NL0	HYL4	HYL3	HYL2	HYL1
bit 23							bit 16

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
HYL0	HUL4	HUL3	HUL2	HUL1	HUL0	CTL4	CTL3
bit 15							bit 8

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
CTL2	CTL1	CTL0	LTD4	LTD3	LTD2	LTD1	LTD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 38 **TS:** Tone Select bit
1 = Temporal Horn Pattern
0 = Continuous Horn Pattern

bit 37 **EOL:** End of Life Enable bit
1 = Enable
0 = Disable

bit 36 **LBH:** Low Battery Hush Enable bit
1 = Enable
0 = Disable

bit 35 **HUSH:** Hush Option bit
1 = Cancelled for high smoke level, interconnect alarm, or second push of TEST button (as described above)
0 = Never Cancel

bit 34 **LTD:** Long Term Drift Enable bit
1 = Enable
0 = Disable

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER (CONTINUED)

bit 33-31	**LB<0:2>:** Low Battery Trip Point bits 000 = 2.1V 001 = 2.5V 010 = 2.3V 011 = 2.7V 100 = 2.2V 101 = 2.6V 110 = 2.4V 111 = 2.8V
bit 30-29	**IRC<1:0>:** IRED Current bits 00 = 50 mA 01 = 100 mA 10 = 150 mA 11 = 200 mA
bit 28-27	**IT<1:0>:** Integration Time bits 00 = 400 µs 01 = 300 µs 10 = 200 µs 11 = 100 µs
bit 26-25	**PAGF<1:0>:** Photo Amplifier Gain Factor bits 00 = 1 01 = 2 10 = 3 11 = 4
bit 24-20	**NL<4:0>:** Normal Limits bits (**Section 3.2**) 00000 = 0 00001 = 1 • • • 11110 = 30 11111 = 31
bit 19-15	**HYL<4:0>:** Hysteresis Limits bits (**Section 3.2**) 00000 = 0 00001 = 1 • • • 11110 = 30 11111 = 31
bit 14-10	**HUL<4:0>:** Hush Limits bits (**Section 3.6**) 00000 = 0 00001 = 1 • • • 11110 = 30 11111 = 31

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER (CONTINUED)

bit 9-5 **CTL<4:0>:** Chamber Test Limits bits (**Section 3.3**)

`00000` = 0
`00001` = 1
•
•
•
`11110` = 30
`11111` = 31

bit 4-0 **LTD<4:0>:** Long Term Drift Sample bits (**Section 3.9**)

`00000` = 0
`00001` = 1
•
•
•
`11110` = 30
`11111` = 31

The minimum pulse width for FEED is 10 µs, while the minimum pulse width for TEST is 100 µs. For example, for the following options, the sequence would be:

data -	0	0	0	1	1	0	0	0	1	0	0	0	0	1
bit -	25	26	27	28	29	30	31	32	33	34	35	36	37	38

Photo Amp Gain Factor = 1
Integration Time = 200 µs
IRED Current = 100 mA
Low Battery Trip = 2.2V
Long Term Drift, Low Battery Hush and EOL are all disabled
Hush Option = Never Cancel
Tone Select = Temporal

4. After shifting in data, pull IO input to V_{DD}, then V_{SS} (minimum pulse width of 10 ms) to store shift register contents into the memory.
5. If any changes are required, power down the part and return to Step 1. All bit values must be reentered.

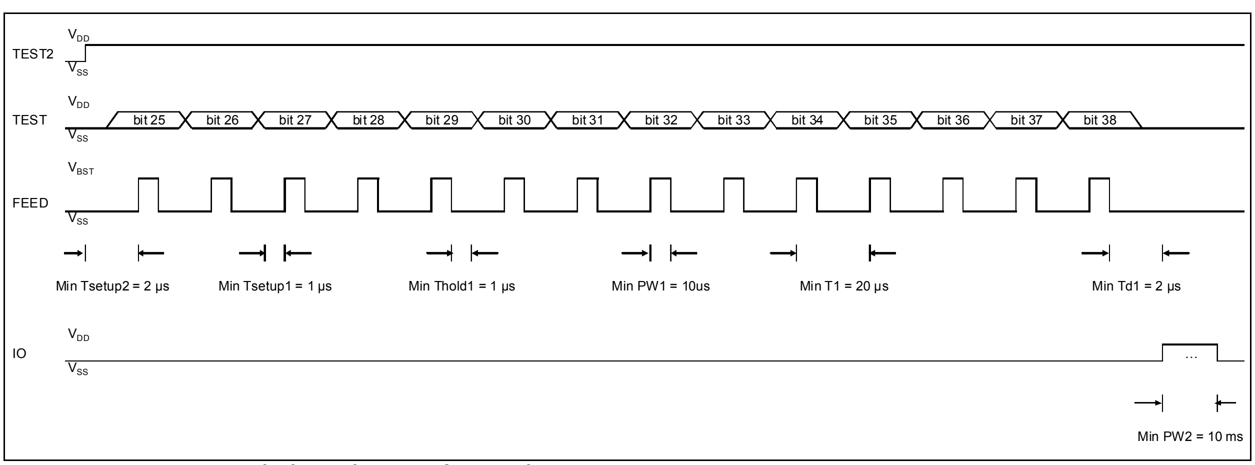


FIGURE 4-2: Timing Diagram for Mode T0.

As an alternative to Figure 4-1, Figure 4-3 can be used to program while in the application circuit. Note that in addition to the five programming supplies, connections to V_{SS} are needed at TP1 and TP2.

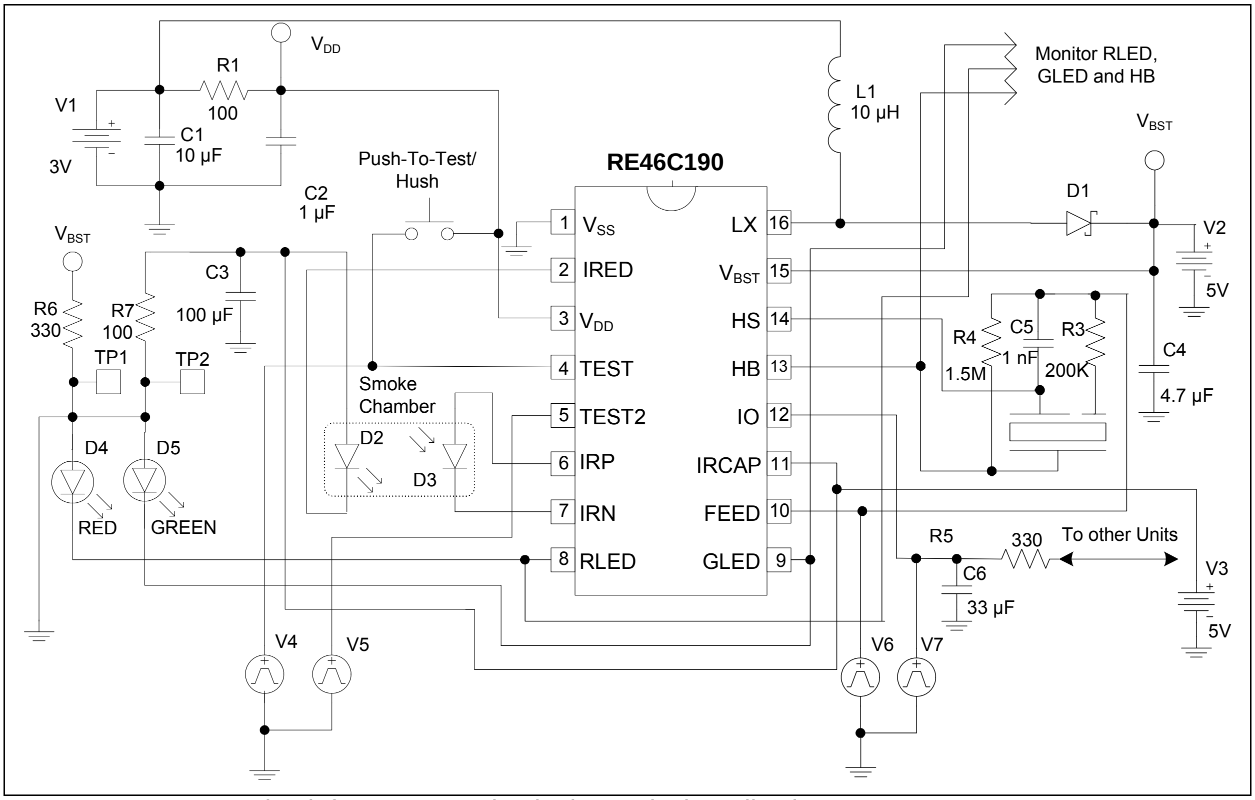


FIGURE 4-3: Circuit for Programming in the Typical Application.

4.3 Smoke Calibration

A separate calibration mode is entered for each measurement mode (Normal, Hysteresis, Hush and Chamber Test) so that independent limits can be set for each. In all calibration modes, the integrator output can be accessed at the GLED output.

The Gamp output voltage, which represents the smoke detection level, can be accessed at the RLED output. The SmkComp output voltage is the result of the comparison of Gamp with the integrator output, and can be accessed at HB. The FEED input can be clocked to step up the smoke detection level at RLED. Once the desired smoke threshold is reached, the TEST input is pulsed low to high to store the result.

The procedure is described in the following steps:

1. Power up with the bias conditions shown in Figure 4-1.
2. Drive TEST2 input from V_{SS} to V_{DD} to enter the Programming mode. TEST2 should remain at V_{DD} through Step 8 described below.
3. Apply a clock pulse to the TEST input to enter in T1 mode. This initiates the calibration mode for Normal Limits setting. The Integrator output saw tooth should appear at GLED and the smoke detection level at RLED. Clock FEED to increase the smoke detection level as needed. Once the desired smoke threshold is reached, the IO input is pulsed low to high to enter the result. See typical waveforms in Figure 4-4. Operating the circuit in this manner, with nearly continuous IRED current for an extended period of time, may result in undesired or excessive heating of the part. The duration of this step should be minimized.
4. Apply a second clock pulse to the TEST input to enter in T2 mode. This initiates the calibration mode for Hysteresis Limits. Clock FEED as in Step 3 and apply pulse to IO, once desired level is reached.Operating the circuit in this manner, with nearly continuous IRED current for an extended period of time, may result in undesired or excessive heating of the part. The duration of this step should be minimized.
5. Apply a clock pulse to the TEST input again to enter in T3 mode and initiate calibration for Hush Limits. Clock FEED as in the steps above and apply a pulse to IO, once the desired level is reached. Operating the circuit in this manner, with nearly continuous IRED current for an extended period of time, may result in undesired or excessive heating of the part. The duration of this step should be minimized.
6. Apply a clock pulse to the TEST input a fourth time to enter in T4 mode, and initiate the calibration for Chamber Test Limits. Clock FEED and apply pulse to IO, once desired level is reached. Operating the circuit in this manner, with nearly continuous IRED current for an extended period of time, may result in undesired or excessive heating of the part. The duration of this step should be minimized.
7. If the Long Term Drift Adjustment is enabled, after all limits have been set, the long term drift (LTD) baseline measurement must be made. To do this, a measurement must be made under no-smoke conditions. To enable the baseline measurement, pull TEST from V_{SS} to V_{BST} again and return to V_{SS}. Once the chamber is clear, pulse FEED low to high to make the baseline measurement.
8. After limits have been set and baseline LTD measurement has been made, pulse IO to store all results in memory. Before this step, no limits are stored in memory.

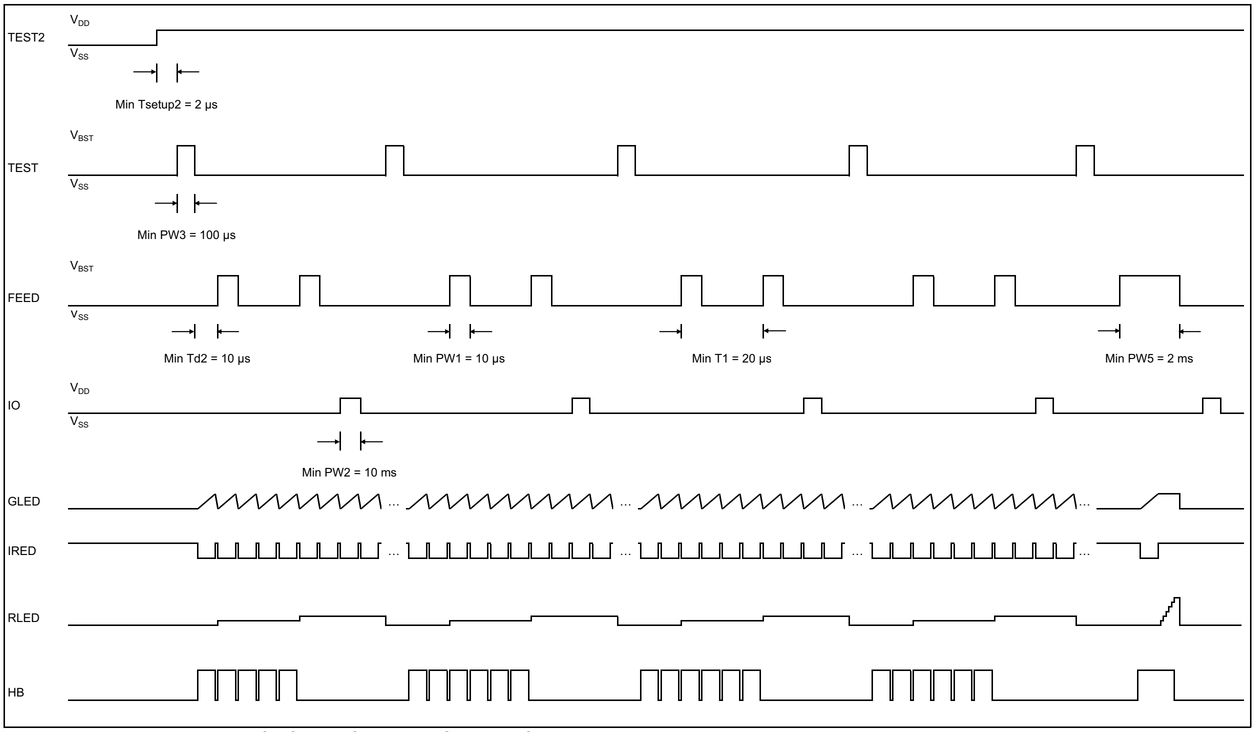


FIGURE 4-4: *Timing Diagram for Modes T1 to T5.*

4.4 Serial Read/Write

As an alternative to the steps in **Section 4.3 "Smoke Calibration"**, if the system has been well characterized, the limits and baseline can be entered directly from a serial read/write calibration mode.

To enter this mode, follow these steps:

1. Set up the application as shown in Figure 4-1.
2. Drive TEST2 input from V_{SS} to V_{DD} to enter in Programming mode. TEST2 should remain at V_{DD} until all data has been entered.
3. Clock the TEST input to mode T6 (High = V_{BST}, Low = V_{SS}, 6 clocks). This enables the serial read/write mode.
4. TEST now acts as a data input (High = V_{DD}, Low = V_{SS}). FEED acts as the clock input (High = V_{BST}, Low = V_{SS}). Clock in the limits, LTD baseline, functional and parametric options. The data sequence should be as follows:

5 bit	LTD sample (LSB first)
5 bit	Chamber Test Limits (LSB first)
5 bit	Hush Limits (LSB first)
5 bit	Hysteresis Limits (LSB first),
5 bit	Normal Limits (LSB first)

Then, the data sequence follows the pattern described in Register 4-1:

2 bit	Photo Amp Gain Factor
2 bit	Integration Time
2 bit	IRED current
3 bit	Low Battery Trip Point
1 bit	Long Term Drift Enable
1 bit	Hush Option
1 bit	Low Battery Hush Enable
1 bit	EOL enable
1 bit	Tone Select

A serial data output is available at HB.

5. After all 39 bits have been entered, pulse IO to store into the EEPROM memory.

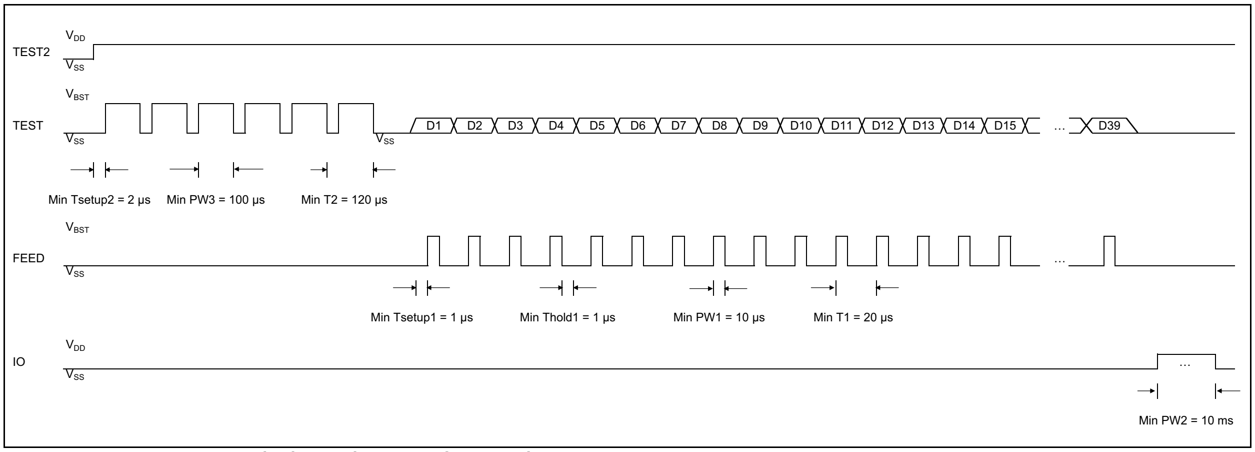


FIGURE 4-5: *Timing Diagram for Mode T6.*

4.5 Limits Verification

After all limits and LTD baseline have been entered and stored into the memory, additional test modes are available to verify if the limits are functioning as expected. Table 4-4 describes several verification tests.

TABLE 4-4: LIMITS VERIFICATION DESCRIPTION

Limit	Test Description
Normal Limits	Clock TEST to Mode T7 (7 clocks). With appropriate smoke level in chamber, pull FEED to V_{DD} and hold for at least 1 ms. The HB output will indicate the detection status (High = smoke detected).
Hysteresis Limits	Clock TEST to Mode T8 (8 clocks). Pulse FEED and monitor HB as in Normal Limits case.
Hush Limits	Clock TEST to Mode T9 (9 clocks). Pulse FEED and monitor HB.
Chamber Test Limits	Clock TEST to Mode T10 (10 clocks). Pulse FEED and monitor HB.

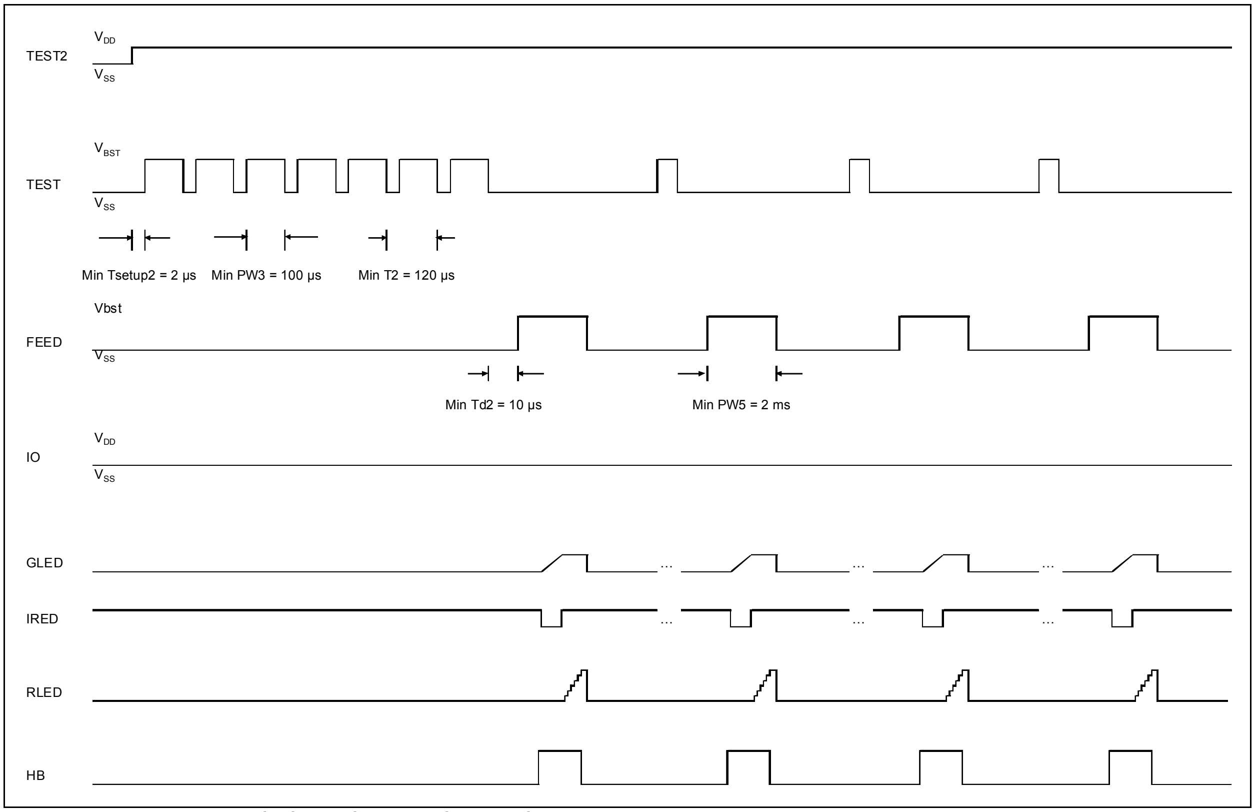


FIGURE 4-6: Timing Diagram for Modes T7-T10.

4.6 Horn Test

The last test mode allows the horn to be enabled indefinitely for audibility testing. To enter this mode, clock TEST to Mode T11 (11 clocks). The IO pin is configured as horn enable.

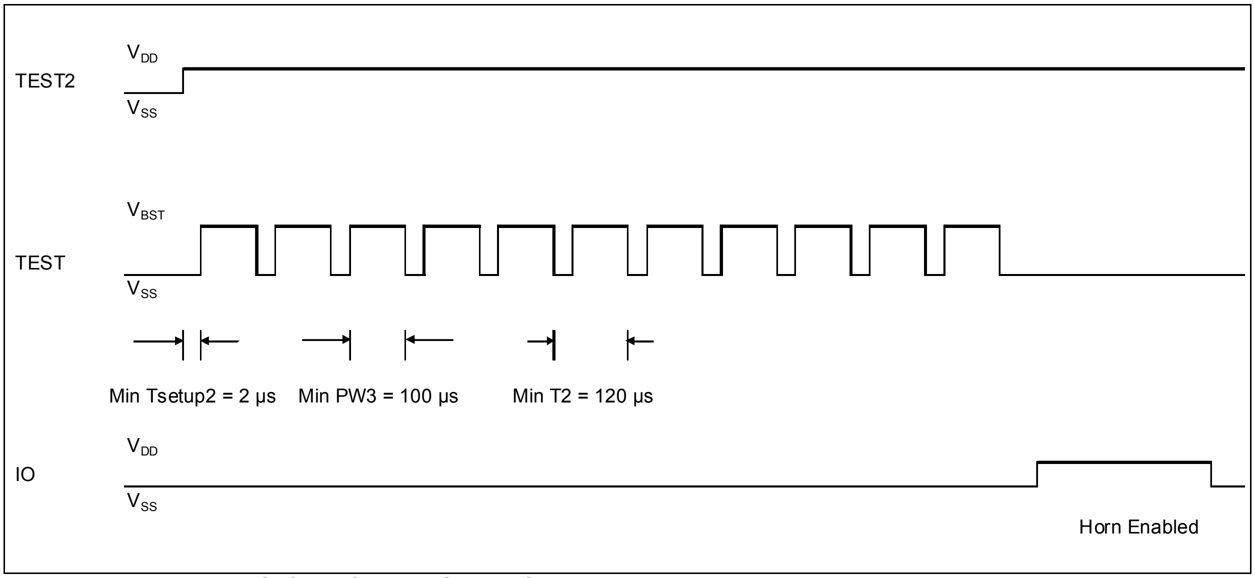


FIGURE 4-7: *Timing Diagram for Mode T11.*

5.0 APPLICATION NOTES

5.1 Standby Current Calculation and Battery Life

The supply current shown in the **DC Electrical Characteristics** table is only one component of the average standby current and, in most cases, can be a small fraction of the total, because power consumption generally occurs in relatively infrequent bursts and depends on many external factors. These include the values selected for IRED current and integration time, the V_{BST} and IR capacitor sizes and leakages, the V_{BAT} level, and the magnitude of any external resistances that will adversely affect the boost converter efficiency.

A calculation of the standby current for the battery life is shown in Table 5-1, based on the following parameters:

V_{BAT}	=	3
V_{BST1}	=	3.6
V_{BST2}	=	9
Boost capacitor size	=	4.70E-06
Boost Efficiency	=	8.50E-01
IRED on time	=	2.000E-04
IRED Current	=	1.000E-01

TABLE 5-1: STANDBY CURRENT CALCULATION

I_{DD} Component	Voltage (V)	Current (A)	Duration (s)	Energy (J)	Period (s)	Average Power (W)	I_{BAT} Contribution (A)	I_{BAT} (µA)
Fixed I_{DD}	3	1.00E-06	—	—	—	3.00E-06	1.00E-06	1.0
Photo Detection Current								
Chamber test (excluding IR drive)	3.6	1.00E-03	1.00E-02	3.60E-05	43	9.85E-07	3.28E-07	0.3
IR drive during Chamber Test	3.6	0.10	2.00E-04	7.20E-05	43	1.97E-06	6.57E-07	0.7
Smoke Detection (excluding IR drive)	3.6	1.00E-03	1.00E-02	3.60E-05	10.75	3.94E-06	1.31E-06	1.3
IR drive during Smoke Detection	3.6	0.10	2.00E-04	7.20E-05	10.75	7.88E-06	2.63E-06	2.6
Low Battery Check Current								
Loaded Test								
Load	9	2.00E-02	1.00E-02	1.80E-03	344	6.16E-06	2.05E-06	2.1
Boost	V_{BST1} to V_{BST2}	—	—	6.85E-05	344	2.34E-07	7.81E-08	0.1
Unloaded Test								
Load	3.6	1.00E-04	1.00E-02	3.60E-06	43	9.85E-08	3.28E-08	0.0
						Total	8.09E-06	8.1

The following paragraphs explain the components in Table 5-1, and the calculations in the example.

5.1.1 FIXED I_{DD}

The I_{DD} is the Supply Current shown in the **DC Electrical Characteristics** table.

5.1.2 PHOTO DETECTION CURRENT

Photo Detection Current is the current draw due to the smoke testing every 10.75 seconds, and the chamber test every 43 seconds. The current for both the IR diode and the internal measurement circuitry comes primarily from V_{BST}, so the average current must be scaled for both on-time and boost voltage.

The contribution to I_{BAT} is determined by first calculating the energy consumed by each component, given its duration. An average power is then calculated based on the period of the event and the boost converter efficiency (assumed to be 85% in this case). An I_{BAT} contribution is then calculated based on this average power and the given V_{BAT}. For example, the IR drive contribution during chamber test is detailed in Equation 5-1:

EQUATION 5-1:

$$\frac{3.6V \times 0.1A \times 200\mu s}{43s \times 0.85 \times 3V} = 0.657\mu A$$

5.1.3 LOW BATTERY CHECK CURRENT

The Low Battery Check Current is the current required for the low battery test. It includes both the loaded (RLED on) and unloaded (RLED Off) tests. The boost component of the loaded test represents the cost of charging the boost capacitor to the higher voltage level. This has a fixed cost for every loaded check, because the capacitor is gradually discharged during subsequent operations, and the energy is generally not recovered. The other calculations are similar to those shown in Equation 5-1. The unloaded test has a minimal contribution because it involves only some internal reference and comparator circuitry.

5.1.4 BATTERY LIFE

When estimating the battery life, several additional factors must be considered. These include battery resistance, battery self discharge rate, capacitor leakages and the effect of the operating temperature on all of these characteristics. Some number of false alarms and user tests should also be included in any calculation.

For ten year applications, a 3V spiral wound lithium manganese dioxide battery with a laser seal is recommended. These can be found with capacities of 1400 to 1600 mAh.

5.1.5 FUNCTIONAL TIMING DIAGRAMS

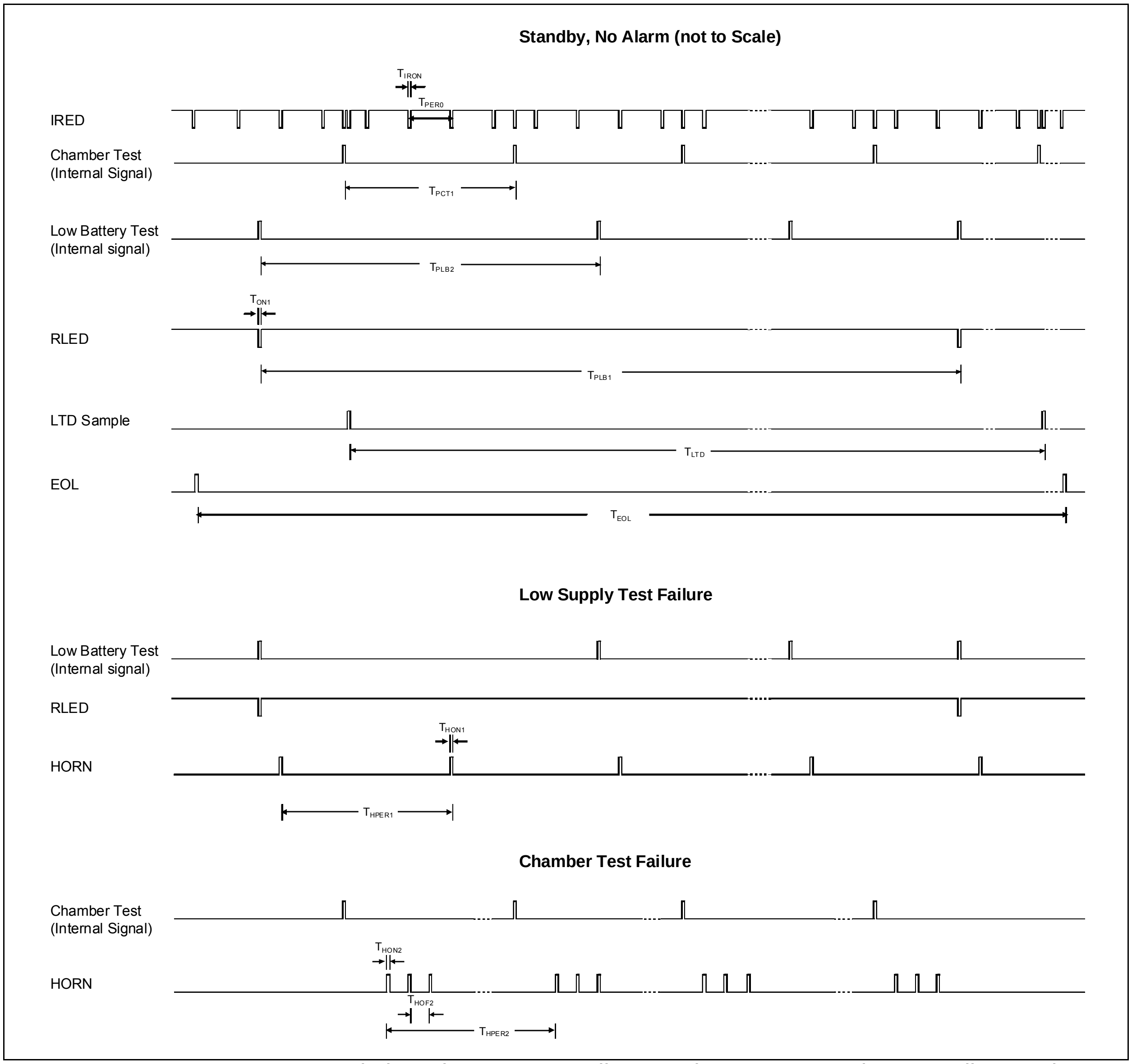


FIGURE 5-1: *RE46C190 Timing Diagram – Standby, No Alarm, Low Supply Test Failure and Chamber Test Failure.*

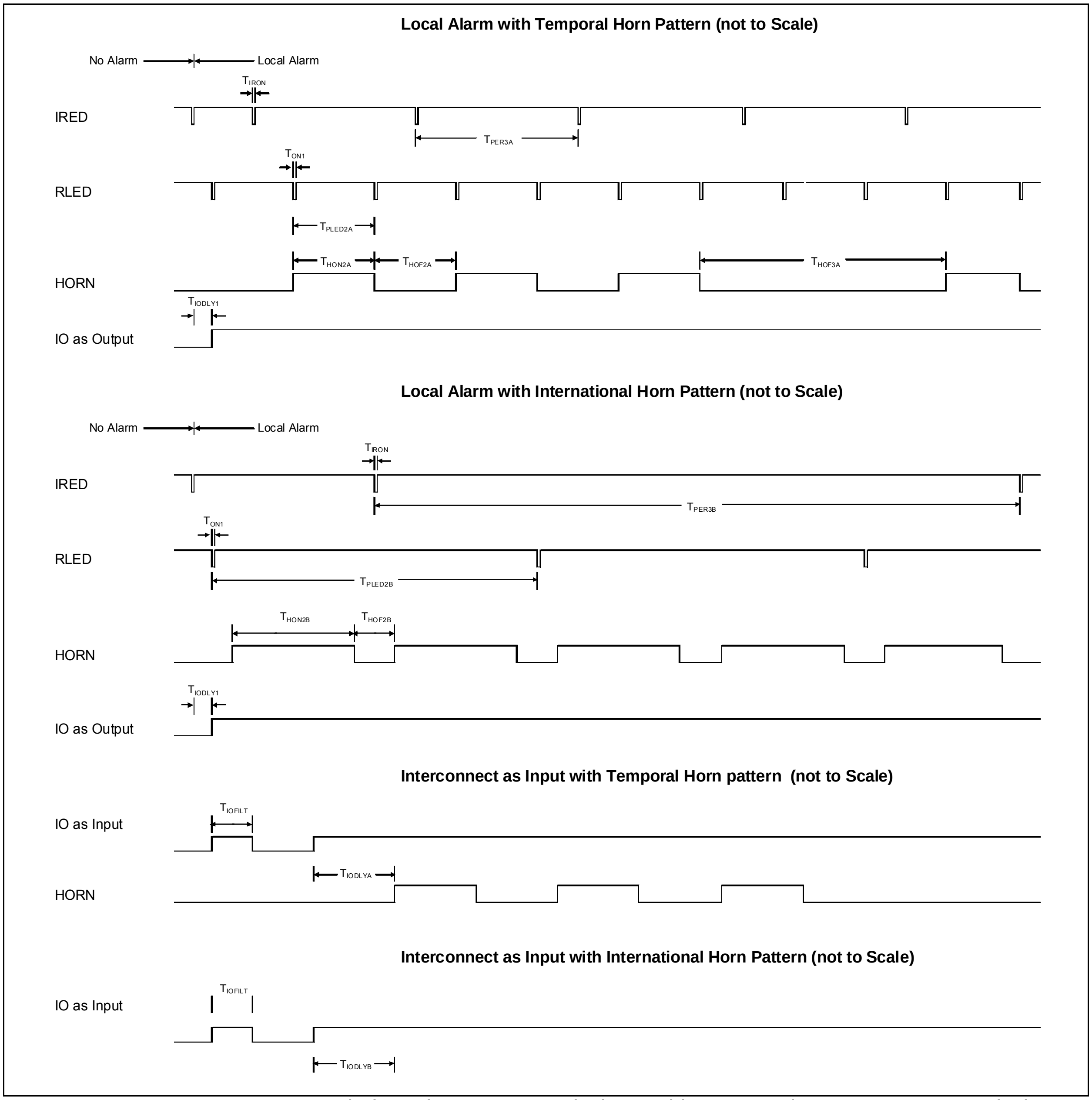


FIGURE 5-2: *RE46C190 Timing Diagram – Local Alarm with Temporal Horn Pattern, Local Alarm with International Horn Pattern, Interconnect as Input with Temporal Horn Pattern and Interconnect as Input with International Horn Pattern.*

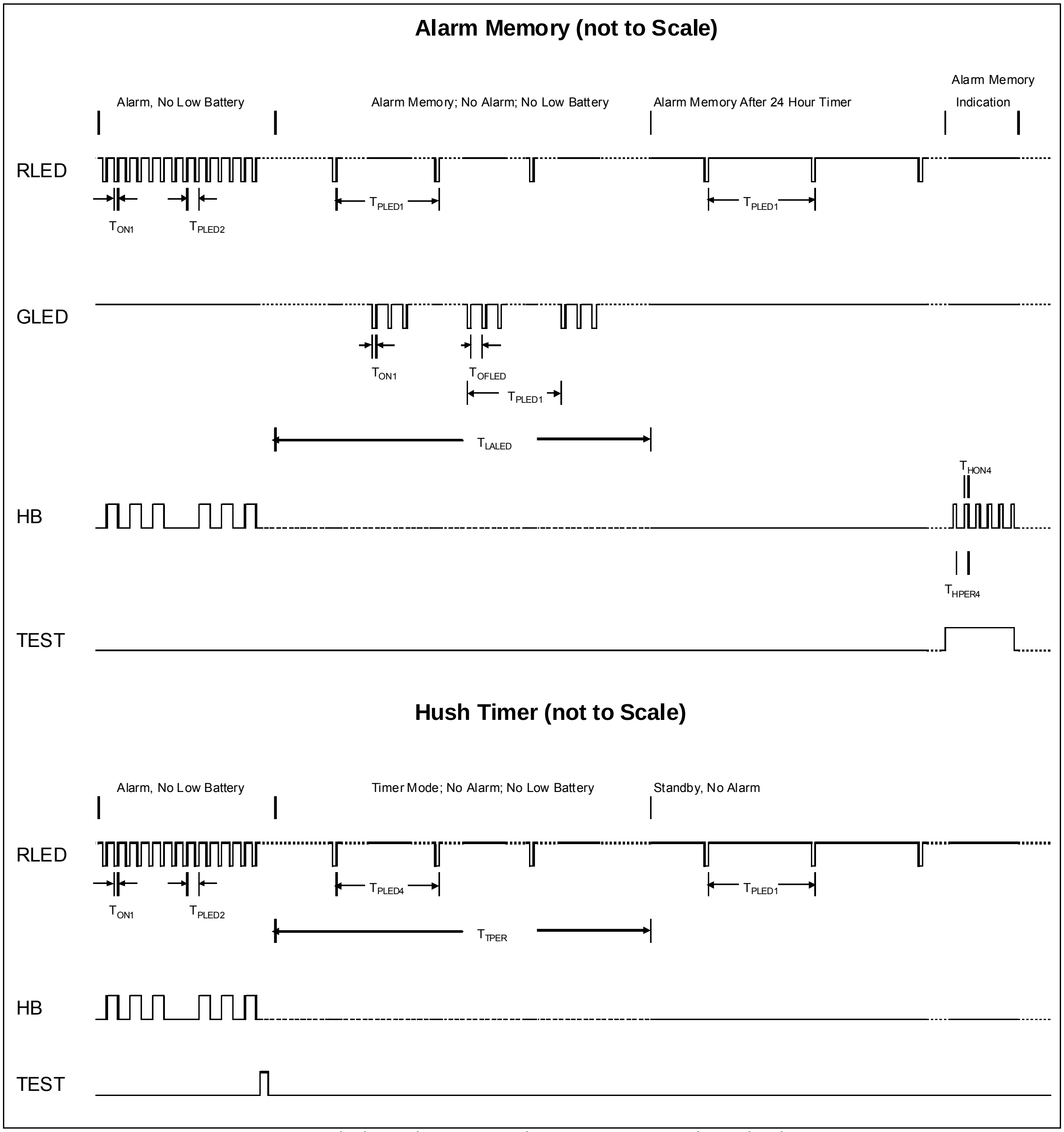


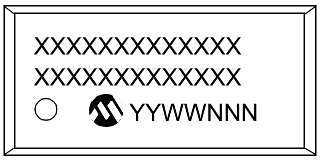
FIGURE 5-3: *RE46C190 Timing Diagram – Alarm Memory and Hush Timer.*

NOTES:

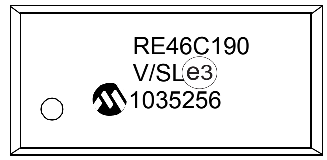
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead SOIC (.150”)



Example

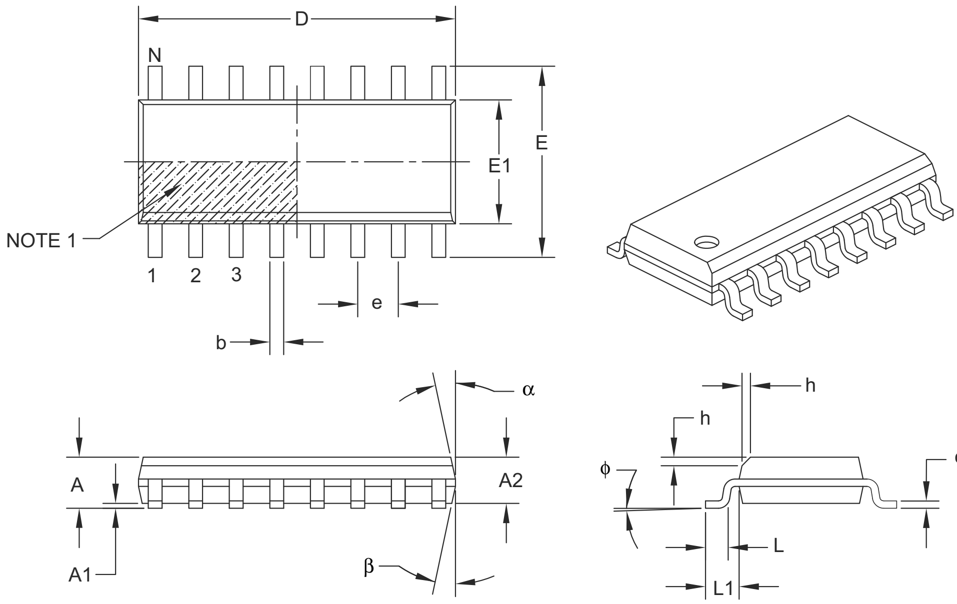


Legend:		
	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		9.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

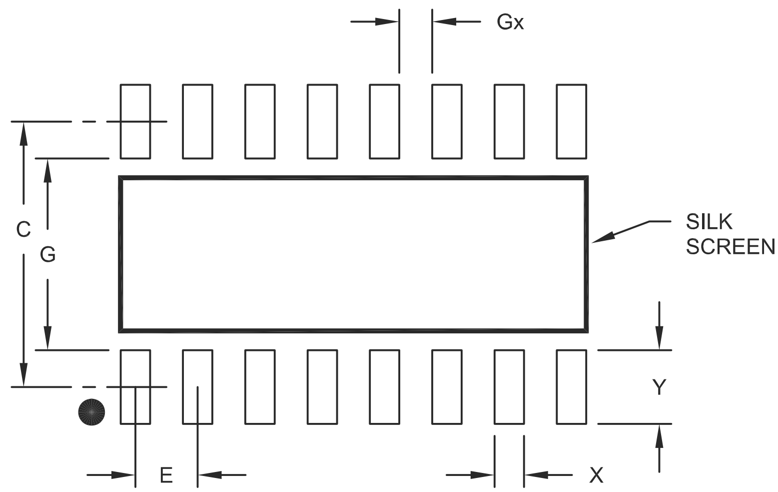
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-108B

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2108A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (December 2010)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	T	X
Device	Package	Number of Pins	Tape and Reel	Lead Free

Device	RE46C190:	CMOS Photoelectric Smoke Detector ASIC
	RE46C190T:	CMOS Photoelectric Smoke Detector ASIC (Tape and Reel)
Package	S =	Small Plastic Outline - Narrow, 3.90 mm Body, 16-Lead (SOIC)

Examples:

a) RE46C190S16F: 16LD SOIC Package, Lead Free

b) RE46C190S16TF: 16LD SOIC Package, Tape and Reel, Lead Free

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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ISBN: 978-1-60932-782-8

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