# S6J3310 Series
# S6J3320 Series
# S6J3330 Series
# S6J3340 Series

## 32-bit Microcontroller Traveo™ Family

The Traveo family expands the company's automotive applications, scalability and high performance into one line-up and at the same time adds new features to fulfill the latest requirements of the automotive industry. Based on the powerful Arm® Cortex®- R5F core in single operations, it offers state-of-the-art real time performance, safety and security features. The family supports the latest in-car networks and offers high performance graphics engines optimized for a minimum memory footprint and embeds dedicated features to increase data security in the car.
S6J3310/20/30/40 is a microcontroller series for instrument clusters with small thin-film transistor (TFT) displays.

## Features

- System
  - 32-bit Arm Cortex-R5F CPU core at up to 240 MHz
  - General purpose I/O port: up to 148
  - 12-bit A/D converter: up to 48 channels
  - External interrupt: up to 24 channels
  - Base timer: up to 32 channels
  - 32-bit reload timer: up to 6 channels
  - 32-bit free-run timer: 8 channels
  - Input capture unit: 12 channels
  - Output compare unit: 12 channels
  - Stepper motor controller (SMC): 6 Units
  - Built-in CR oscillator
  - Real-time clock
  - DMA controller: 16 channels
  - JTAG debug interface
- Graphics and Display (optional)
  - 2D graphic engine
  - RGB888
  - LCD : up to 4 COM x 32 SEG
- Communication
  - CAN-FD: up to 6 channels
  - Multi-function serial interface: up to 12 channels, selectable protocol: UART, CSIO, LIN and $I^2C$
  - Ethernet AVB MAC (optional)
  - MediaLB (optional)
  - Automotive Remote Handler for APIX® (optional)
- Memory
  - HyperBus™ Memory interface
  - DDR High Speed SPI
  - External BUS interface
- Multimedia (optional)
  - I2S input/output: 2 channels
  - PCM to PWM output unit
  - Sound mixer: 1 unit x 10 inputs
  - Stereo audio DAC
- Security and Safety
  - Secure Hardware Extension – SHE
  - Safety features, such as MPU, TPU, ECC and others
  - CRC generator: 1 channel
  - Watchdog timer with window function
  - Low voltage detector
  - Clock supervisor for all source clocks

## Applications

- Instrument cluster

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# 1. Overview

## 1.1 Overview

S6J3310/20/30/40 is a microcontroller series which is to be applied to automotive systems representative of a graphical cluster control unit on a dashboard.

## 1.2 Document Definition

The related documents of S6J3310/20/30/40 are the followings.

**Table 1-1: Document Definition**

| Document Type | Definition | Primary User | Document Code |
|---|---|---|---|
| S6J3310/20/30/40 Datasheet | This document.<br><br>The function and its characteristics are specified quantitatively. | Investigator and hardware engineer | 002-10635 |
| S6J3300 Hardware Manual | S6J3300 Series 32-bit Microcontroller Traveo™ Family Hardware Manual<br><br>The function and its operation of S6J3300 series are described. | Software engineer | 002-10185 |
| Traveo™ Platform Hardware Manual | 32-Bit Microcontroller Traveo™ Family S6J33xx, S6J34xx, S6J35xx Series Hardware Manual Platform Part<br><br>The function and its operation of CPU core platform are described. | Software engineer | 002-07884 |
| Application Note | The reference software, sample application, the reference board design and so on are explained. | Software and hardware engineer | 002-03898<br>002-04455<br>002-04446<br>002-09716<br>002-04452<br>002-04096<br>002-12061<br>002-02495 |

***Notes:***

- *Refer all documents for the system development.*
- *"Primary user" is a most likely engineer for whom the document is the most useful.*
- *The description of the datasheet and the S6J3300 Hardware Manual should precede the duplicated description of Traveo™ Platform Hardware Manual.*
- *Traveo™ Platform Hardware Manual is expected to be used as dictionary of platform specification.*

# 2. Function List

## 2.1 Function List

The table shows the functions which are implemented in S6J3310/20/30/40 series.

**Table 2-1: Function List**

| Function | S6J3310 | S6J3320 | S6J3330 | S6J3340 | Remarks |
|---|---|---|---|---|---|
| CPU core | Arm Cortex R5F | | | | |
| FPU | Available | | | | |
| PPU | Available | | | | |
| MPU | Available | | | | |
| TPU | Available | | | | |
| Endian | Little endian | | | | |
| Core clock frequency | 240 MHz | | | | |
| HPM bus frequency | 200 MHz | | | | |
| LLPM bus frequency | 240 MHz | | | | |
| Resource clock frequency | 80 MHz (Max) | | | | |
| Embedded CR oscillation | Slow clock:100 kHz,<br>Fast clock: 4 MHz<br>(Center frequency) | | | | See 9.1.4.1 |
| PLL | PLL0, 1, 2, 3 | | | | |
| SSCG PLL | SSCG0, 1, 2, 3 | | | | |
| Clock supervisor | Available | | | | |
| DMA | 16 ch | | | | |
| Boot-ROM | 16 Kbyte | | | | |
| JTAG | Available | | | | |
| Data cache | 16 Kbyte | | | | |
| Instruction cache | 16 Kbyte | | | | |
| Program FLASH | Option | | | | See 2.2.1 |
| Work FLASH | 112 Kbyte | | | | |
| TCRAM | 128 Kbyte | | | | |
| System SRAM | 384 Kbyte | | | | |
| Backup RAM | 32 Kbyte | | | | |
| Security (SHE) | Option | | | | |
| Low latency interrupt | Available | | | | |
| Power domain | 5 domains | | | | |
| External power supply | 5 V (VCC5, VCC53),<br>3 V (VCC3, VCC53),<br>1.2 V (VCC12) | | | | |
| Embedded LDO power supply for 5.0 V | Available | | | | |
| Low voltage detection of external power supply | Available | | | | |
| Low voltage detection of internal LDO output | Available | | | | |
| Hardware watchdog timer | Available | | | | |
| Software watchdog timer | Available | | | | |
| Package | Option | | | | See 2.2.1 |
| AUTOSAR | AUTOSAR 4.0.3 | | | | |
| General Purpose I/O | Option | | | | See 2.2.3 |
| Up/down counter | 2 ch | | | | |
| I/O timer | (FRT 5 ch x ICU 6 ch x OCU 6 ch) + (FRT 3 ch x ICU 6 ch x OCU 6 ch) | | | | |
| 32bit Reload timer | 6 ch | | | | |
| Real time clock | Available | | | | Automatic calibration |
| Sound generator | 5 ch | | | | |
| Sound waveform generator | 1 unit x 5 outputs | | No | | See 2.2.1 |
| Sound mixer | 1 unit x 10 inputs | | No | | See 2.2.1 |

| Function | S6J3310 | S6J3320 | S6J3330 | S6J3340 | Remarks |
|---|---|---|---|---|---|
| Stereo audio DAC | 1 unit (L and R) | | No | | See 2.2.1 |
| PCM-PWM | 1 unit (L and R) | | No | | See 2.2.1 |
| Base timer | 16 units (32 ch) | | | | |
| Stepping motor controller (SMC) | For 6 gauges | | | | |
| 12bit-A/D converter | 2 unit - 48 input ports (Max) | | | | See 2.2.3 |
| CRC | 4 units | | | | |
| Programmable CRC | 1 unit | | | | |
| Source clock timer | 4 ch | | | | |
| NMI | Available | | | | |
| External interrupt | 24 ch | | | | |
| Internal interrupt | 512 vectors | | | | |
| I2S | 2 ch | | 1 ch | | One only supports an output as a function of the sound system. |
| DDR HSSPI | 1 ch | | | | A type of Quad SPI |
| Hyper BUS | 1 ch | | | | See the AC specification on 9.1.4.17. |
| Multi-function serial interface | 12 ch | | | | |
| CAN-FD | 6 ch | | | | |
| CAN-FD RAM (ECC supported) | 16 KB/ch<br>It equivalents to 128 message buffer per channel of MCAN module | | | | |
| Ethernet AVB | 1 unit | | | No | See 2.2.1 |
| Media-LB (MOST50) | 1 unit | | | No | See 2.2.1 |
| LCD controller | 4 COM x 32 SEG (Max) | | | | See 2.2.3 |
| Indicator PWM | 1 ch | | | | |
| MPU for AHB | 1 unit | | | | |
| MPU for AXI | 1 unit | | | | |
| Graphic engine clock | 80 MHz (Max) | | | | |
| Graphic AXI clock | 80 MHz (Max) | | | | |
| Display clock | 25 MHz | | | | |
| Display clock source | Graphic display controller clock or external clock | | | | |
| Target resolution | WQVGA 480 x 272 | | | | |
| Target frame rate | 60 fps | | | | |
| Number of display outputs | 1 output | | | | |
| TTL output (RGB888) | Option | | | | See 2.2.1 |
| 2D Graphic engine | 1 unit | | | | |
| 2D Driver API | CYPRESS proprietary | | | | |
| External BUS | 1 ch | | | | |
| APIX® for ARH (Automotive Remote Handler) | 1 unit (2 ch) | No | | | See 2.2.1 |

***Notes:***

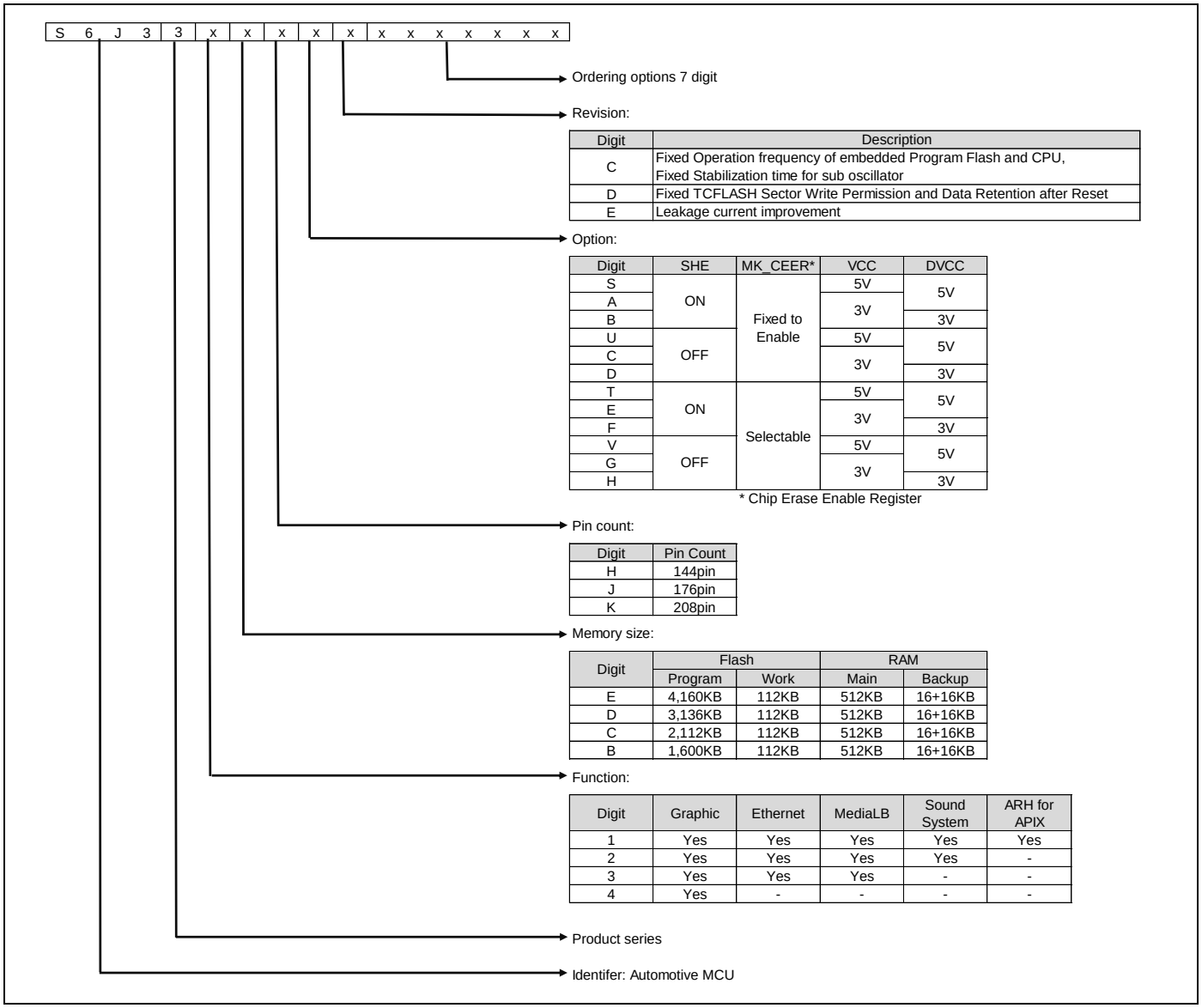
- *The options are described in 2.2.*

## 2.2 Optional Function

### *2.2.1 Basic Option*

The figure shows the optional function and the part number relations of the series.

**Figure 2-1: Option and Part Number for S6J3310/20/30/40 Series**




| Digit | Description |
|---|---|
| C | Fixed Operation frequency of embedded Program Flash and CPU, Fixed Stabilization time for sub oscillator |
| D | Fixed TCFLASH Sector Write Permission and Data Retention after Reset |
| E | Leakage current improvement |

| Digit | SHE | MK_CEER* | VCC | DVCC |
|---|---|---|---|---|
| S | ON | Fixed to Enable | 5V | 5V |
| A | | | 3V | |
| B | | | | 3V |
| U | OFF | | 5V | 5V |
| C | | | 3V | |
| D | | | | 3V |
| T | ON | Selectable | 5V | 5V |
| E | | | 3V | |
| F | | | | 3V |
| V | OFF | | 5V | 5V |
| G | | | 3V | |
| H | | | | 3V |

* Chip Erase Enable Register

| Digit | Pin Count |
|---|---|
| H | 144pin |
| J | 176pin |
| K | 208pin |

| Digit | Flash | | RAM | |
|---|---|---|---|---|
| | Program | Work | Main | Backup |
| E | 4,160KB | 112KB | 512KB | 16+16KB |
| D | 3,136KB | 112KB | 512KB | 16+16KB |
| C | 2,112KB | 112KB | 512KB | 16+16KB |
| B | 1,600KB | 112KB | 512KB | 16+16KB |

| Digit | Graphic | Ethernet | MediaLB | Sound System | ARH for APIX |
|---|---|---|---|---|---|
| 1 | Yes | Yes | Yes | Yes | Yes |
| 2 | Yes | Yes | Yes | Yes | - |
| 3 | Yes | Yes | Yes | - | - |
| 4 | Yes | - | - | - | - |

***Notes:***

- *This table only shows the relations between the optional function and the part numbers. That is, all products are not necessarily available for orders. See 11, and confirm actual availabilities of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*

### 2.2.2 ID

ID is specified for each function digit and revision which is defined at Figure 2-1.

| Function Digit | Revision | Chip ID | JTAG ID |
|---|---|---|---|
| S,U,T,V | C | 0x10122100 | 0x1000B5CF |
| | D, E | 0x10122200 | |
| A,C,E,G | C | 0x10128100 | |
| | D, E | 0x10128200 | |
| B,D,F,H | C | 0x10120100 | |
| | D, E | 0x10120200 | |

### 2.2.3 Restriction

Some functions have restrictions which depend on package pin counts.

**Table 2-2: Pin Restriction**

| Function | TEQFP176 | TEQFP144 |
|---|---|---|
| Analog input port (12bit-ADC) | - | AN4~7, AN10~11,<br>AN14~15,<br>AN25~26, AN28~30, |
| SEG port of LCD controller | - | SEG0~3<br>SEG5~8 |
| General Purpose I/O | P4_00 ~ P4_31 | P4_00 ~ P4_31<br>P3_00 ~ P3_31 |
| CAN | RX0_2, TX0_2<br>RX1_0, TX1_0<br>RX1_1, TX1_1<br>RX2_0, TX2_0<br>RX2_1, TX2_1<br>RX3_2, TX3_2 | RX0_1, TX0_1<br>RX0_2, TX0_2<br>RX1_0, TX1_0<br>RX1_1, TX1_1<br>RX2_0, TX2_0<br>RX2_1, TX2_1<br>RX3_1, TX3_1<br>RX3_2, TX3_2<br>RX5_1, TX5_1<br>RX6_1, TX6_1 |
| BaseTimer | - | PPG4/5/6/7/8/9_TOUT0_1<br>PPG4/5/6/7/8/9_TOUT2_1<br>PPG10/11/12/13/15_TOUT0_1<br>PPG10/11/12/13/14/15_TOUT2_1<br>PPG0/1/2/3/4/5_TIN1_1<br>PPG6/7/8/9/10/11_TIN1_1<br>PPG12/13/14/15_TIN1_1 |
| ExtBus | - | MDQM1<br>MAD15~21<br>MDATA8~15 |

| Function | TEQFP176 | TEQFP144 |
|---|---|---|
| External Interrupt | EINT1_4, EINT1_5<br>EINT2_1, EINT2_2<br>EINT3_2, EINT4_2<br>EINT5_4, EINT5_5<br>EINT6_4, EINT7_1<br>EINT7_4, EINT8_4<br>EINT8_5, EINT9_1<br>EINT10_1, EINT10_4<br>EINT10_5, EINT13_2<br>EINT13_3, EINT14_2<br>EINT14_3, EINT15_3<br>EINT16_1, EINT16_3<br>EINT16_4, EINT19_4<br>EINT20_3, EINT21_3<br>EINT22_1, EINT22_3<br>EINT23_3, EINT23_4 | EINT0_4, EINT1_1<br>EINT1_4, EINT1_5<br>EINT2_1, EINT2_2<br>EINT2_4, EINT3_1<br>EINT3_2, EINT3_4<br>EINT4_2, EINT4_4<br>EINT5_4, EINT5_5<br>EINT6_1, EINT6_4<br>EINT7_1, EINT7_4<br>EINT8_1, EINT8_4<br>EINT8_5, EINT9_1<br>EINT9_2, EINT10_1<br>EINT10_2, EINT10_4<br>EINT10_5, EINT11_2<br>EINT11_5, EINT12_1<br>EINT12_2, EINT12_5<br>EINT13_2, EINT13_3<br>EINT13_5, EINT14_1<br>EINT14_2, EINT14_3<br>EINT14_5, EINT15_2<br>EINT15_3, EINT16_1<br>EINT16_2, EINT16_3<br>EINT16_4, EINT16_5<br>EINT17_1, EINT17_3<br>EINT17_5, EINT18_1<br>EINT18_3, EINT18_5<br>EINT19_1, EINT19_3<br>EINT19_4, EINT20_1<br>EINT20_2, EINT20_3<br>EINT21_1, EINT21_3<br>EINT22_1, EINT22_3<br>EINT23_3, EINT23_4 |

***Notes:***

- *See multiplexed functions on pin assignment sheet.*
- *The optional restriction will be added without notification.*

# 3. Product Description

## 3.1 Overview

This chapter explains the product features of S6J3310/20/30/40 series. The description of this chapter should precede the duplicated description on *Traveo™ Platform Hardware Manual*.

## 3.2 Product Description

The table shows features.

**Table 3-1: Product Features**

| Feature | Description |
|---|---|
| Technology | 40-nm CMOS technology with embedded FLASH<br>Fully automotive qualified according to ISO/TS 16949 and AEC-Q100<br>Developed according to ISO26262, safety target ASIL-B |
| Functional Safety | The product series has some functional safety features suited for ASIL-B application. |
| Peripherals | See function list. |
| Power Domain (PD) | See the *Traveo™ Platform Hardware Manual* and chapter STATE TRANSITION in detail.<br>The product series supports the power off control of PD1, PD2 (including PD3 and 5), PD4_0, PD4_1 and PD6.<br>The power domain resets of PD3 and PD5 included in PD2 are not supported in the product series, and "0" is always read from the reset factor flags of them.<br>This series doesn't support partial wakeup for PD6. |
| Debug and Trace | See the *Traveo™ Platform Hardware Manual* in detail.<br>- Standard 5-pin JTAG interface<br>- 4 kB Embedded Trace Buffer<br>4-bit trace support for TEQFP package. |
| System Control | See the *Traveo™ Platform Hardware Manual* in detail.<br>Main and sub oscillator is available.<br>- A wide range of 3.6 - 16MHz is available for main oscillator<br>- 32KHz is available for sub oscillator<br>Sub clock is enable/disable by register settings |
| Clock | See the *Traveo™ Platform Hardware Manual* in detail.<br>CLK_CLKO (Clock Output Function) is supported.<br>Main Oscillation Stabilization Wait Time (at 4 MHz):8.19ms (Initial value) |
| Embedded CR oscillation | See the *Traveo™ Platform Hardware Manual* in detail.<br>Stabilization time is as followings.<br>− 0.35 ms to 0.8 ms for 4 MHz (Fast clock)<br>− 0.43 ms to 1.28 ms for 100 kHz (Slow clock) |
| Clock Supervisor | See the *Traveo™ Platform Hardware Manual* in detail.<br>This product series doesn’t support clock supervisor output port. (Related register and internal circuit is implemented.) |
| Reset | RSTX pin + MD pin simultaneous assert INITX (Same as INITX pin input)<br>- Occurrence factor: Simultaneously inputting “L” level to RSTX pin and inputting “L” level to MD pin<br>- Release factor: Inputting “H” level to RSTX pin<br>See the *Traveo™ Platform Hardware Manual* in detail.<br>Following resets are not mounted on this device.<br>- SRSTX (and nSRST pin)<br>The product series does not support EX5VRST and writing EX5VRSTCNT bits in SYSC0_SPECFGR has no effect. |

| Feature | Description |
|---|---|
| Hardware watchdog | See the *Traveo™ Platform Hardware Manual* in detail.<br>Hardware watchdog function stops during PSS mode. In the related register of HWDG_CFG, the bit<br>ALLOWSTOPCLK is always read as 1 (HWDG_CFG.ALLOWSTOPCLK = 1).<br>The product series doesn't support Watchdog Counter Monitor Output port. (Related register and internal circuit is implemented.) |
| Standby mode | See the *Traveo™ Platform Hardware Manual* in detail.<br>Standby mode with 5 V (or 3 V) single external power supply is available.<br>Turning off the 1.2 V external power supply in standby mode is available.<br>The long term pulse of the indicator PWM can be outputted during RTC Standby mode. |
| PLL / SSCG PLL | See the *Traveo™ Platform Hardware Manual* in detail.<br>Use case assumption is following.<br>PLL<br>– Sound system clock<br>– Sound frequency master clock<br>– Peripherals<br>– Display clock<br>– Trace clock<br><br>SSCG<br>– CPU core<br>– GDC core<br>– Hyper BUS<br>– DDR-HSSPI<br>Product supports down spread and center spread modes with the conditions defined in 9.1.4.3 Internal Clock Timing (S6J3310). |
| External Interrupts | See the *Traveo™ Platform Hardware Manual* in detail. |
| NMI | See the *Traveo™ Platform Hardware Manual* in detail.<br>1 NMI pin. |
| Memory Protection | MPU16 AHB: See the *Traveo™ Platform Hardware Manual* in detail.<br>MPU for AXI: ch.0<br>MPU for AHB: ch.1<br>Additional MPU for Graphic sub system, MediaLB and Ethernet AVB. They are described on the chapter of MPU for AHB and MPU for AXI<br><br>To configure Lock or Unlock for both MPUXn_UNLOCK and MPUHn_UNLOCK,<br>− Lock: 0x112ABB56<br>− Unlock: 0xACCABB56 |
| Peripheral Protection | See the *Traveo™ Platform Hardware Manual* in detail.<br>Protected peripherals are described in the base address map. |
| Internal Memories System SRAM | 384 KByte<br>1 wait cycle is necessary for RAM read at over 120MHz. |
| Internal Memories TCRAM | 128 KByte |
| Internal Memories Backup RAM | 32 KByte<br>Backup RAM can only be operated in RUN mode (normal operation mode). In other mode the memory content should be retained, but it cannot be operated. SLEEP control for Backup RAM is not supported and cannot be used. |

| Feature | Description |
|---|---|
| Embedded Program/Work Flash Memory | Embedded Program Flash can be accessed with 0-wait-cycle if CPU frequency is 80MHz or less.<br>0-wait-cycle: 80MHz or less.<br>1-wait-cycle: 160MHz or less.<br>2-wait-cycle: more than 160MHz.<br><br>Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less.<br>6-wait-cycle: 80MHz or less.<br>12-wait-cycle: 160MHz or less.<br><br>The wait-cycle setting see the *Traveo™ Platform Hardware Manual* in details.<br>The CLK_FCLK maximum frequency should be referred in 9.1.4.3.<br><br>Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended.<br>Serial Flash programing and Parallel Flash programing are supported.<br>Margin mode is not supported. |
| Internal Power Domain | PD1: Always ON<br>PD2: Cortex R5F platform/ GDC/ additional peripherals<br>PD4: Backup RAM in Always On domain<br>PD6: Peripherals in Always On domain<br>* The chapter of the block diagram explains in detail. |
| Power Supply | 5 V, and 3 V, 1.2 V external power supply is required.<br>Built in LDO provides internal power supply for Always On region (PD1).<br>1.2 V external power supply control pin is supported.<br>3 V external power supply could be controlled by GPIO.<br>There are constraints of power on/off sequence. |
| Low Voltage Detection | LVD for external voltage is supported.<br>LVD for internal voltage is supported.<br>See 9.1.4.11 and 9.1.4.12. |
| Low voltage detection for RAM retention (RVD) | RVD for RAM retention is effective during the standby mode only. That is, it is only for the Backup RAM of 32KB that the function is available. |
| Resource inter-connect | The output signal of some resources can be inputted to the other resource. |
| I/O Ports | 5 V general purpose I/O<br>3 V general purpose I/O<br>Multi input level and multi output drivability<br>Pull-up, pull-down function is available.<br>Resource input and output is multiplexed.<br>+B input is allowed many pins of 3.3 V, 5 V and 3.3 V/5 V I/O domain. |
| A/D Converter | 12 bit resolution, 2 unit (Unit0 is possible to select channels 4-31. Unit1 is possible to select channels 32-63.)<br>48 channels of analog input for TEQFP208<br>48 channels of analog input for TEQFP176<br>35 channel of analog input for TEQFP144<br>24 channels of them are shared with the SMC for TEQFP208/176/144<br>External trigger and timer trigger are available.<br>The description of the A/D converter function should be referred in the *S6J3300 Hardware Manual*. Though the chapter of I/O port in *Traveo™ Platform Hardware Manual* describes another A/D converter function, do not refer it.<br>A/D Channel Control Register (ADC12Bn_CHCTRL0) [bit5:0] ANIN[5:0]: Analog Input Selection bits.<br>This register setting is possible of channel 0-31 (the register value is 00_0000 to 01_1111).<br>AN39 to AN63 are not support for S6J33xxxAx, S6J33xxxCx, S6J33xxxEx, and S6J33xxxGx option. |
| CRC | See the *Traveo™ Platform Hardware Manual* in detail. |

| Feature | Description |
|---|---|
| Programmable CRC | DMA support |
| Sound Generator | Produces sound/melody with varying frequency and amplitude for convenient duration<br>Square wave sound output<br>Automatic linear amplitude increment or decrement<br>Interrupt request generated when specified sound length has ended |
| Sound Waveform generator | Sine waveform, saw-tooth waveform and Square waveform are generated with easy configuration of the parameters which specified sound sources.<br>Fade-in and Fade-out control for reverberation. |
| Sound Mixer | The input channels of 0 - 4 are reserved for waveform generator.<br>Mixing different sampling frequency sounds.<br>Mixing Internal sounds and External I2S input sounds.<br>Saturating addition function for keeping sound quality.<br>Cut a specific frequency data by digital filter.<br>LPF is support by FIR filter.<br>Fade-in and Fade-out control. |
| PCM-PWM | Conversion of PCM audio streaming to Pulse Width Modulated signals.<br>Supports 2 output channels for stereo and mono data<br>Up to 16-bit output sample resolution<br>Support for half and full H-bridges |
| Audio DAC | The sound source of the fixed 48 kHz sampling frequency can be outputted.<br>1 unit, L/R channels support.<br>BTL connection is available. |
| I2S | 2 ch.<br>– I2S0 only supports the output of sound sources.<br>– I2S1 supports both the input and the output. |
| Base Timer | See the *Traveo™ Platform Hardware Manual* in detail.<br><br>A unit consists of a pair of 16-bit base timers. 16 units, that is, 32 channels of base timers are available. |
| Reload Timer | See the *Traveo™ Platform Hardware Manual* in detail. |
| I/O Timer | See the *Traveo™ Platform Hardware Manual* in detail. |
| Up/Down Counter | See the *Traveo™ Platform Hardware Manual* in detail. |
| Multi-Functional Serial (MFS) | See the *Traveo™ Platform Hardware Manual* in detail.<br><br>Only 2 ports of MFS have the dedicated I/O for $I^2C$.<br>See $I^2C$ timing in 9.1.4.6 Multi-Function Serial in detail.<br>The $I^2C$ is not designed to be hot swappable.<br>CTS/RTS is not mounted (hardware flow control is not supported for this series.) |
| CAN-FD | Flexible data rate is supported.<br>16 KB/ch of message RAM is available.<br>The clock output from CAN pre-scaler is supplied to every CAN. ECC error generation function of the message RAM is not supported for this device. Therefore CAN FD ECC Error Insertion Control Register (FDFECR) is not writeable. |
| Real Time Clock (RTC) with auto-calibration | See the *Traveo™ Platform Hardware Manual* in detail. |
| DDR High Speed SPI | ch.0: HSSPI as a MCU peripheral |
| Hyper BUS I/F | ch.0: Hyper Bus as a MCU peripheral<br>The following register is not supported and cannot be used.<br>– Controller Status Register (HYPERBUSIn_CSR)<br>– Interrupt Enable Register (HYPERBUSIn_IEN)<br>– Interrupt Status Register (HYPERBUSIn_ISR)<br>– Write Protection Register (HYPERBUSIn_WPR)<br>– Test Register (HYPERBUSIn_TEST)<br>GPO signal can only be used for "Internal Control example by GPO" in this product, that is, it can select using HyperBus of PF or using HyperBus of Graphic Sub System. |

| Feature | Description |
|---|---|
| Stepper Motor Control (SMC) | Each channel has 6 motor drivers with high output capability |
| External Interrupt Capture Unit (EICU) | See the *Traveo™ Platform Hardware Manual* in detail. |
| Ethernet AVB | 10/100 Mbps<br>MII-Interface<br>Supports Audio-Video Bridging (AVB) |
| MediaLB | MOST50 (1024FS)<br>3 wires<br>Maximum 15 ch is available. |
| LCD Controller | TEQFP208: 4 com x 32 seg<br>TEQFP176: 4 com x 32 seg<br>TEQFP144: 4 com x 24 seg<br>LCDC pins are initialized with Reset. (Stop LCDC alternating current output)<br>Duty and Static of segment output is supported. (SEG23/ST0, SEG24/ST1, SEG25/ST2, SEG26/ST3, SEG27/ST4, SEG28/ST5, SEG29/ST6, SEG30/ST7, SEG31/ST8) |
| SHE | See the *Traveo™ Platform Hardware Manual* in detail. |
| Source Clock Timer | See the *Traveo™ Platform Hardware Manual* in detail. |
| Graphics Subsystem | 80 MHz maximum clock frequency<br>Variable setting about GDC clock. (Asynchronous with CPU clock)<br>480 x 272 pixels maximum frame resolution<br>Video modes up to 25 MHz pixel clock<br>RGB888,<br>Order replacement of RGB pins. |
| External BUS | TEQFP208: 22 bit address and 16 bit data<br>TEQFP176: 22 bit address and 16 bit data<br>TEQFP144: 15 bit address and 8 bit data |
| ARH | 2 ch<br>This device does not have PHY macro and its function. |
| Power Supply Control (PSC) | PSC (PSC_1) output is used for external 1.2 V power supply module control and automatically switched with the following condition.<br>"High": Request to supply VCC12<br>- "Power ON Reset" is released<br>- CPU wakes up from PSS shutdown mode<br>"Low": Request to stop supplying VCC12<br>- CPU transfers from RUN mode to PSS shutdown mode.<br><br>For timing chart of output signals include PSC in detail, see the "*S6J3300 Hardware Manual*" and chapter "State Transition" |

### *3.2.1 Ethernet*

The following functions are not supported.

| Functions | Remarks |
|---|---|
| External FIFO Interface | |
| Additional Low Latency TX FIFO Interface for DMA configurations | |
| MAC Transmit Block<br>- half-duplex<br>- collision<br>- back_pressure | |
| MAC Filtering Block<br>- external address match<br>- Wakeup On Lan | |
| Energy Efficient Ethernet support | |
| LPI Operation in Cadence IP | |
| PHY Interface<br>- GMII<br>- SGMII<br>- TBI | |
| 10/100/1000 Operation<br>- 1000 M | |
| SGMII Operation | |
| Jumbo Frames | |
| Physical Control Sub-Layer | |

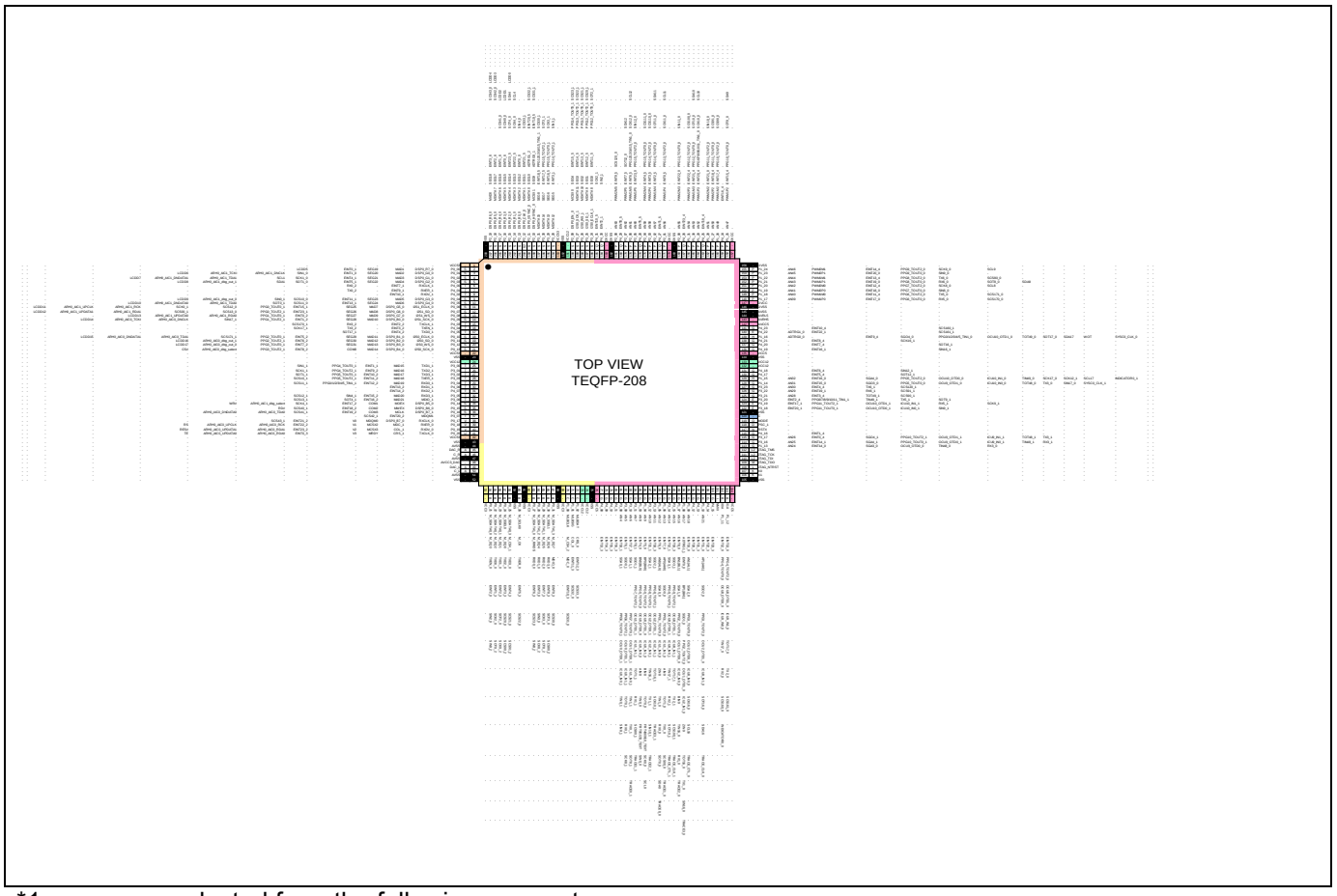
# 4. Package and Pin Assignment

## 4.1 Pin Assignment

Alphabets with pin numbers are signs specify I/O circuit type.

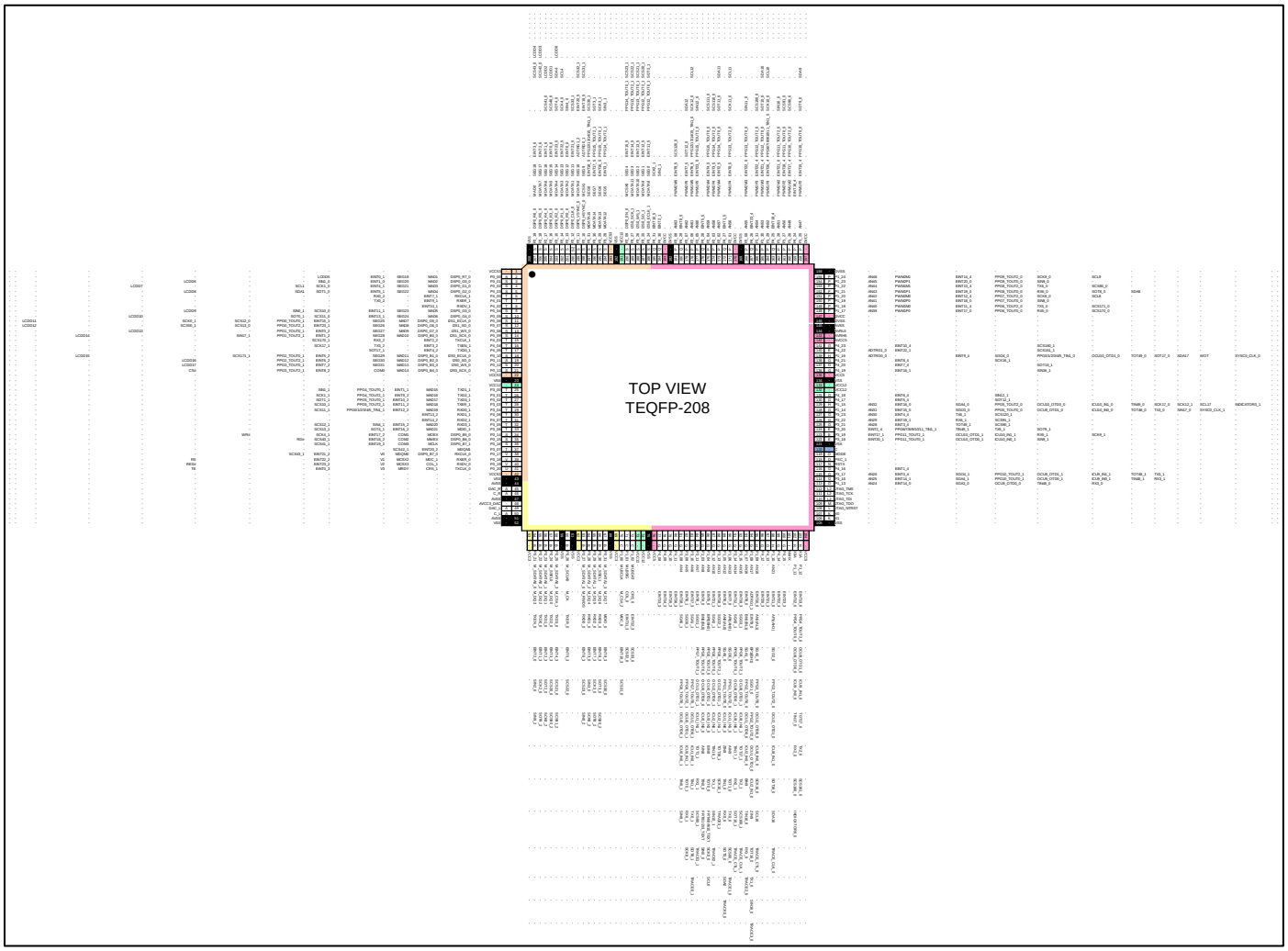
### *4.1.1 TEQFP-208 Pin Assignment*

**Figure 4-1: TEQFP-208 (S6J331xKyz *1)**



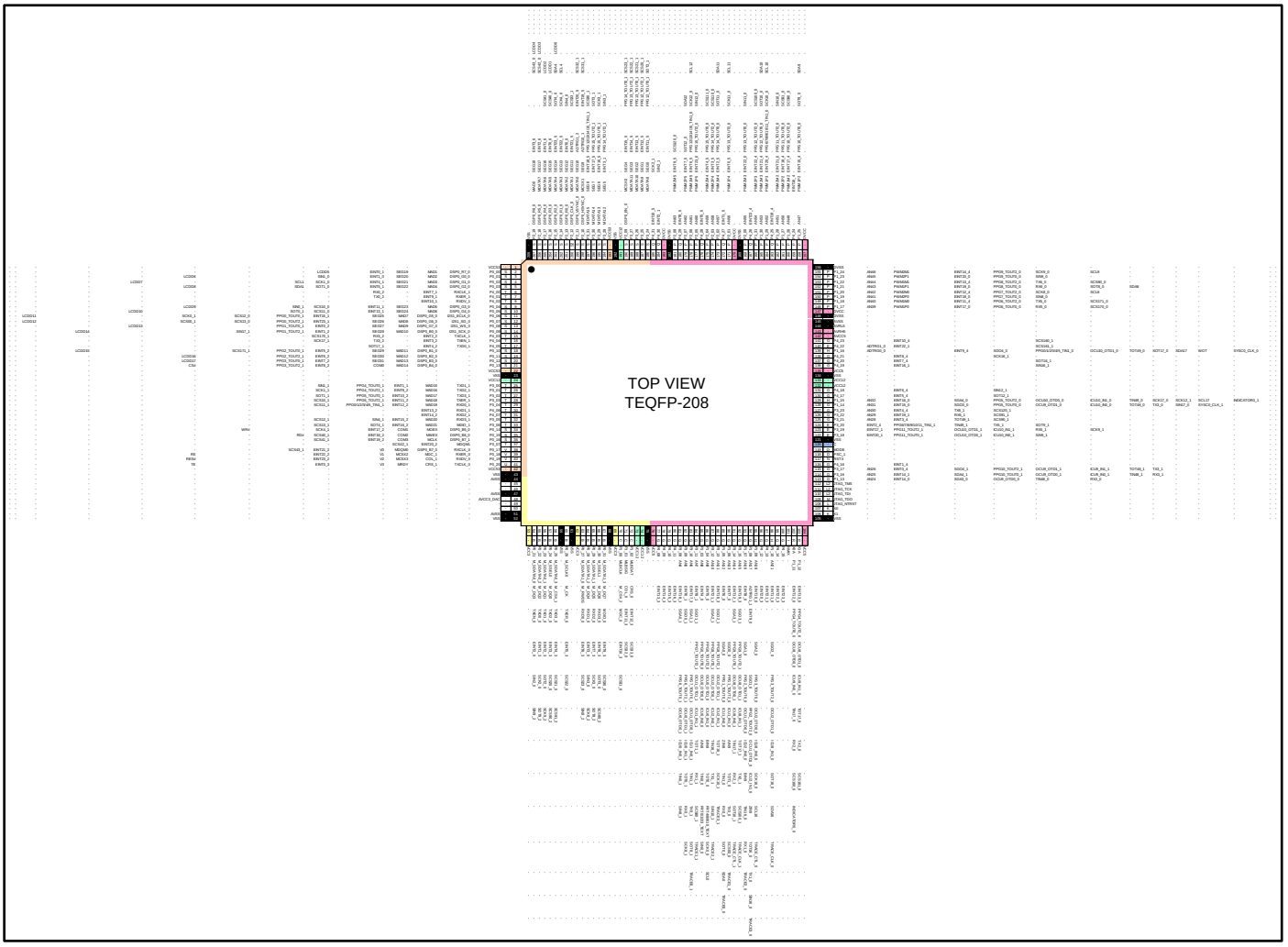

*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

**Figure 4-2: TEQFP-208 (S6J332xKyz *1)**



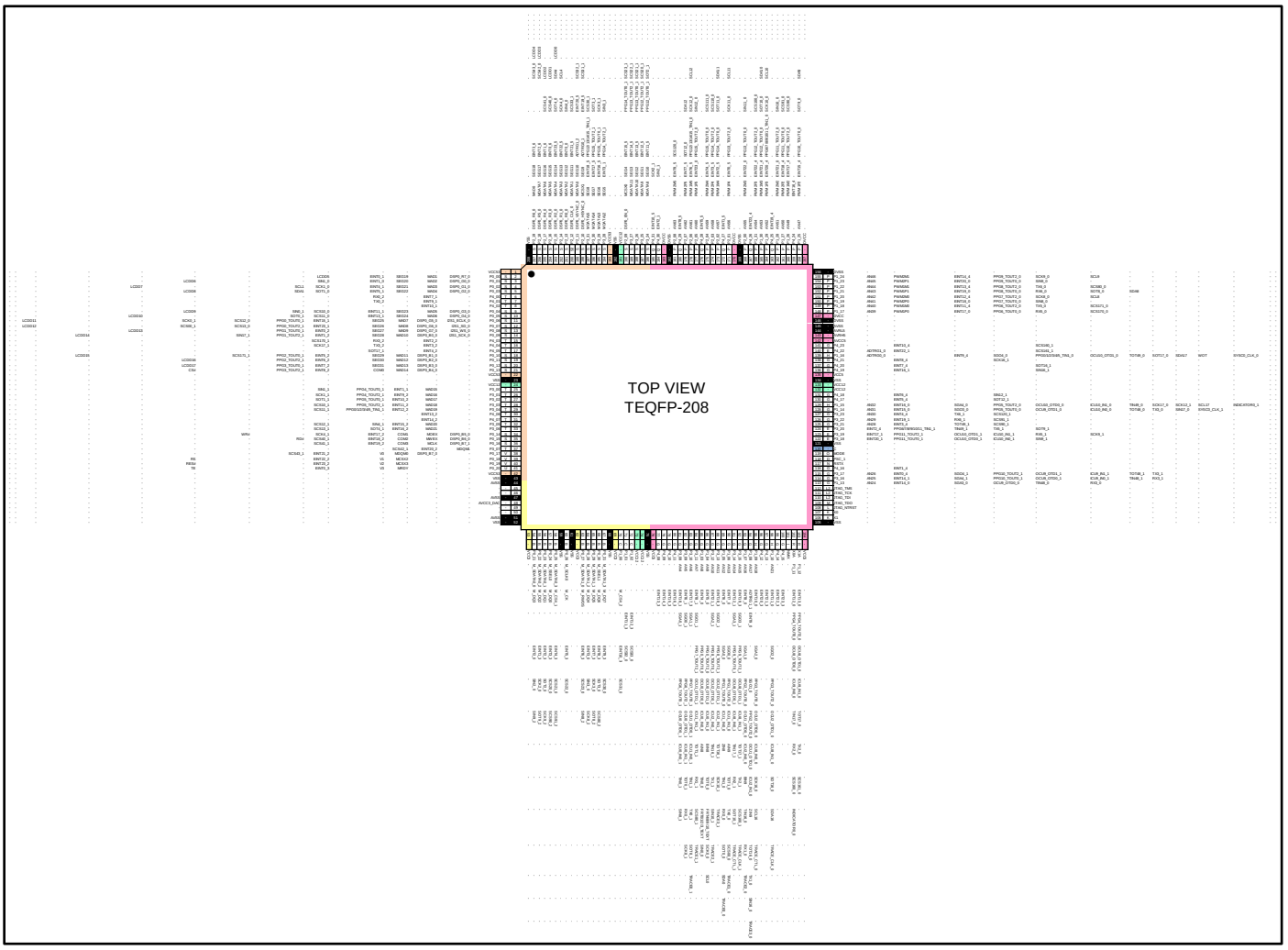

*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

**Figure 4-3: TEQFP-208 (S6J333xKyz *1)**




*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

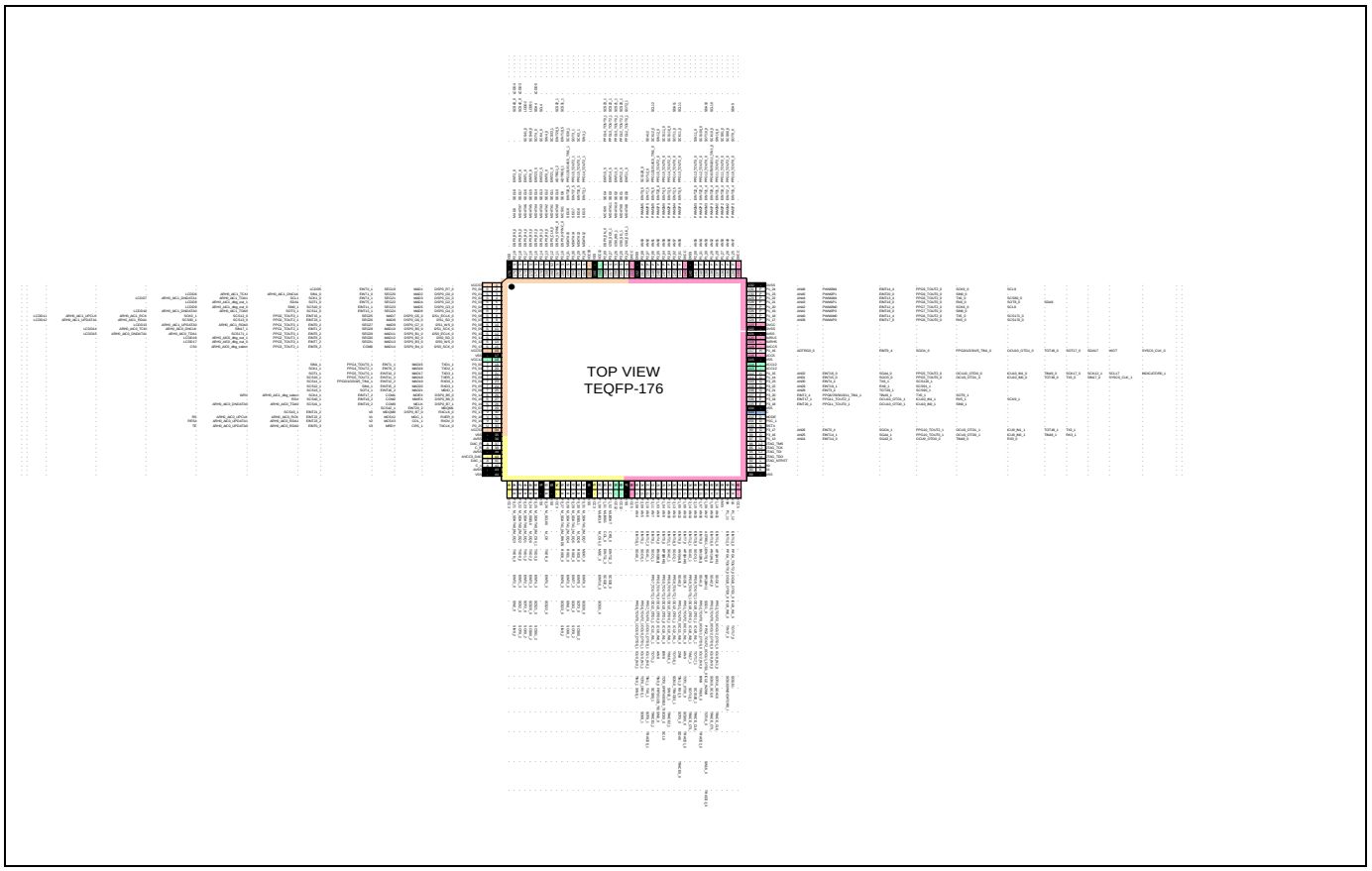
**Figure 4-4: TEQFP-208 (S6J334xKyz *1)**




*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

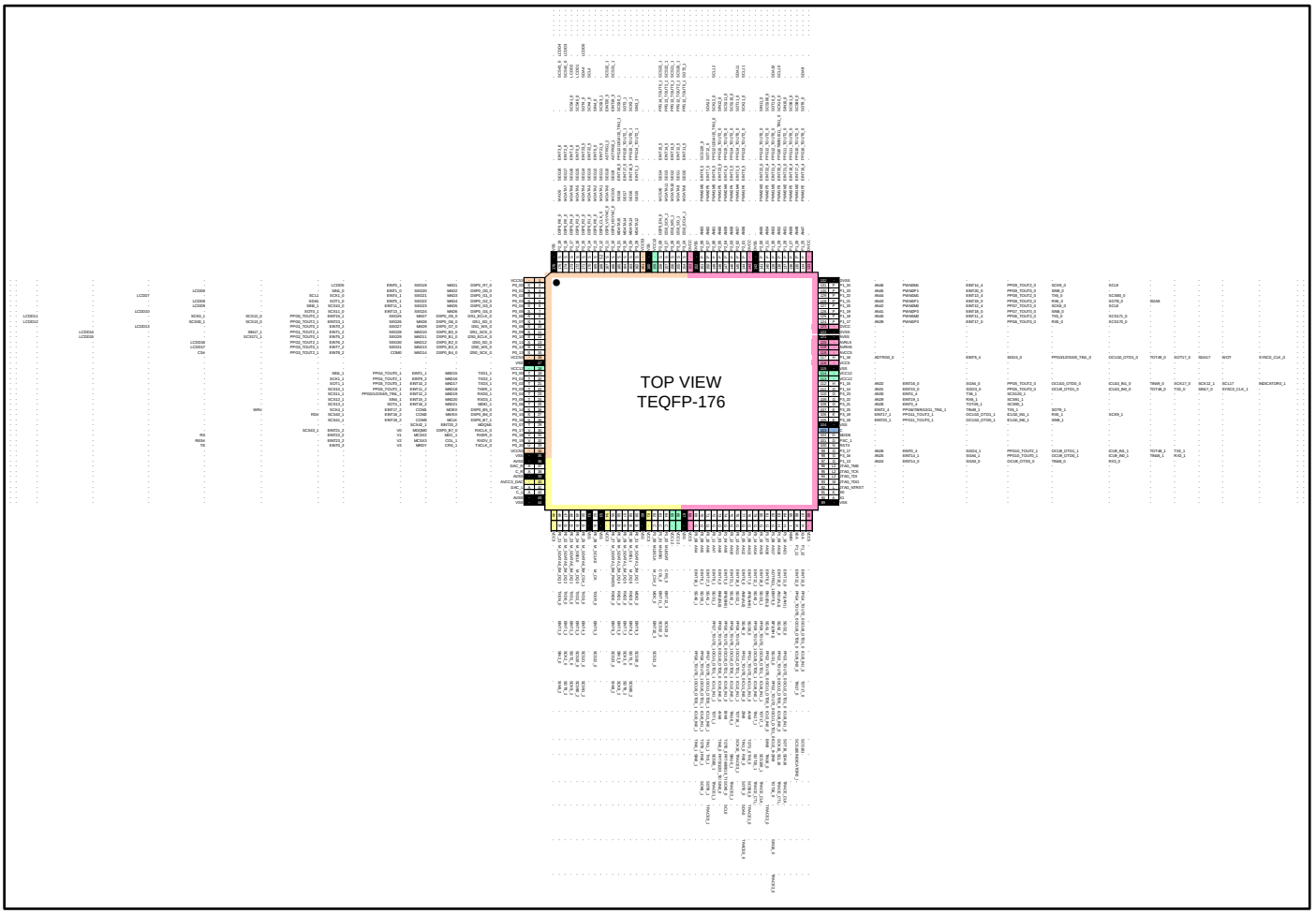
### 4.1.2 TEQFP-176 Pin Assignment

**Figure 4-5: TEQFP-176 (S6J331xJyz *1)**



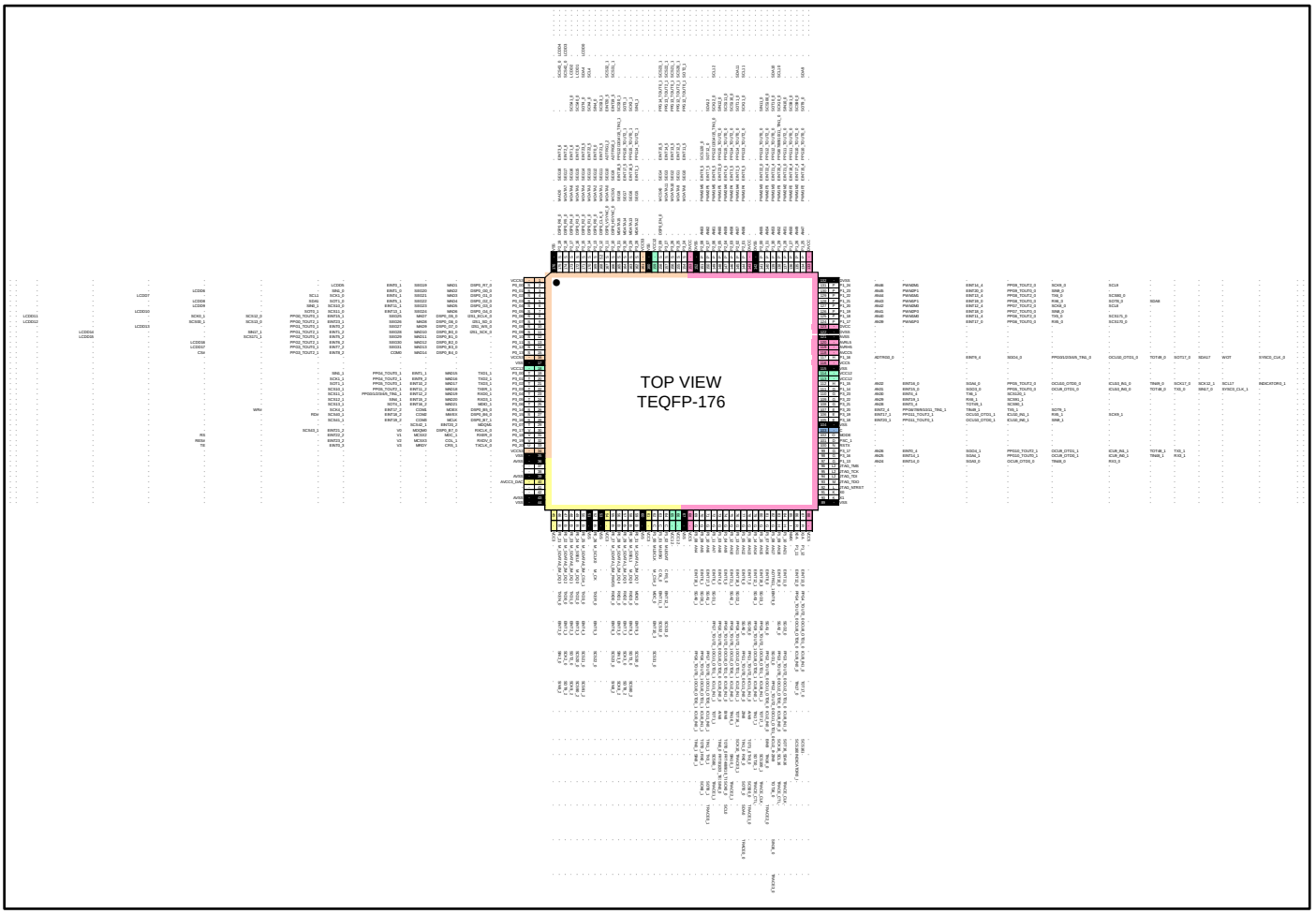

*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

**Figure 4-6: TEQFP-176 (S6J332xJyz *1)**



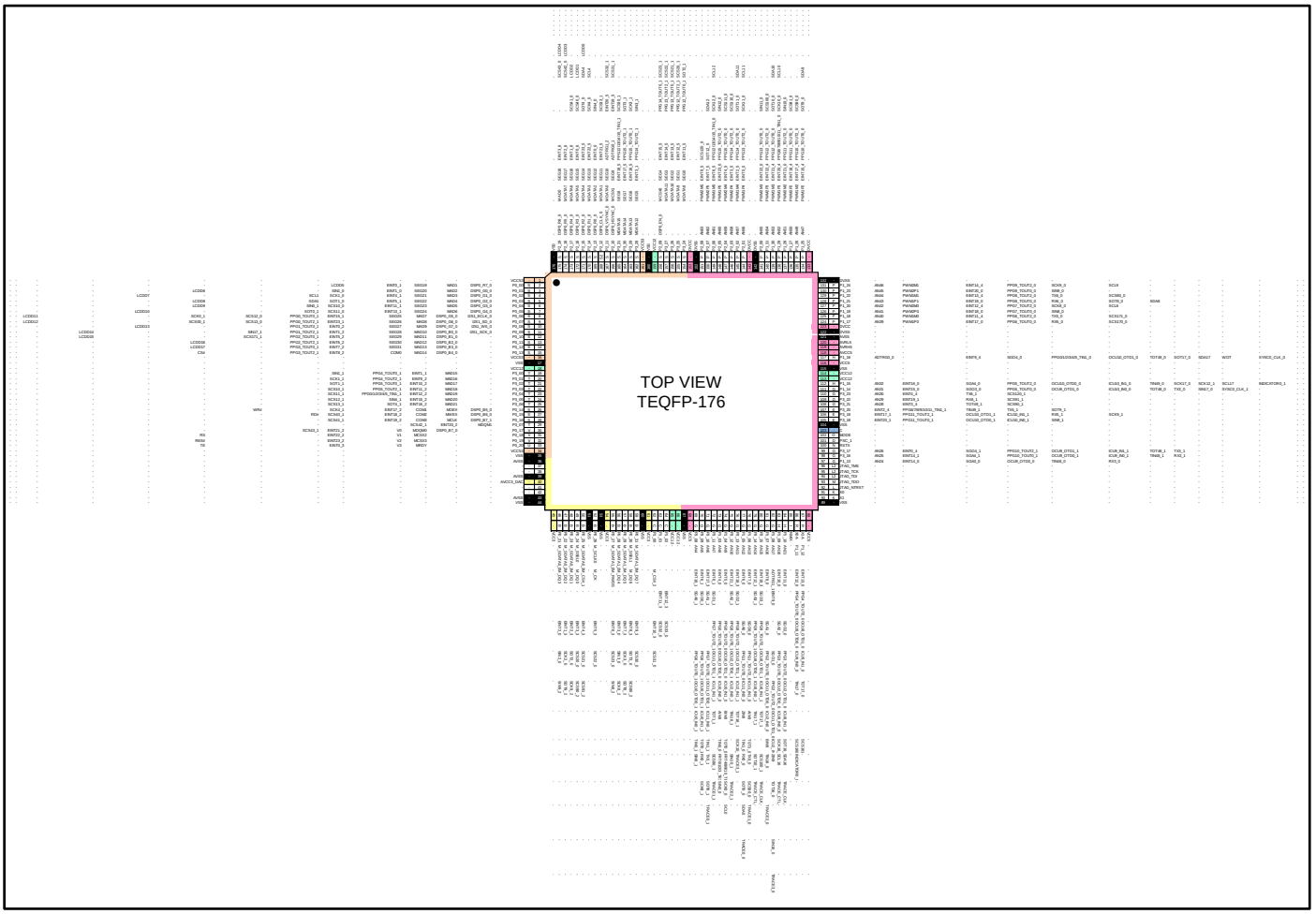

*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

**Figure 4-7: TEQFP-176 (S6J333xJyz *1)**




*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

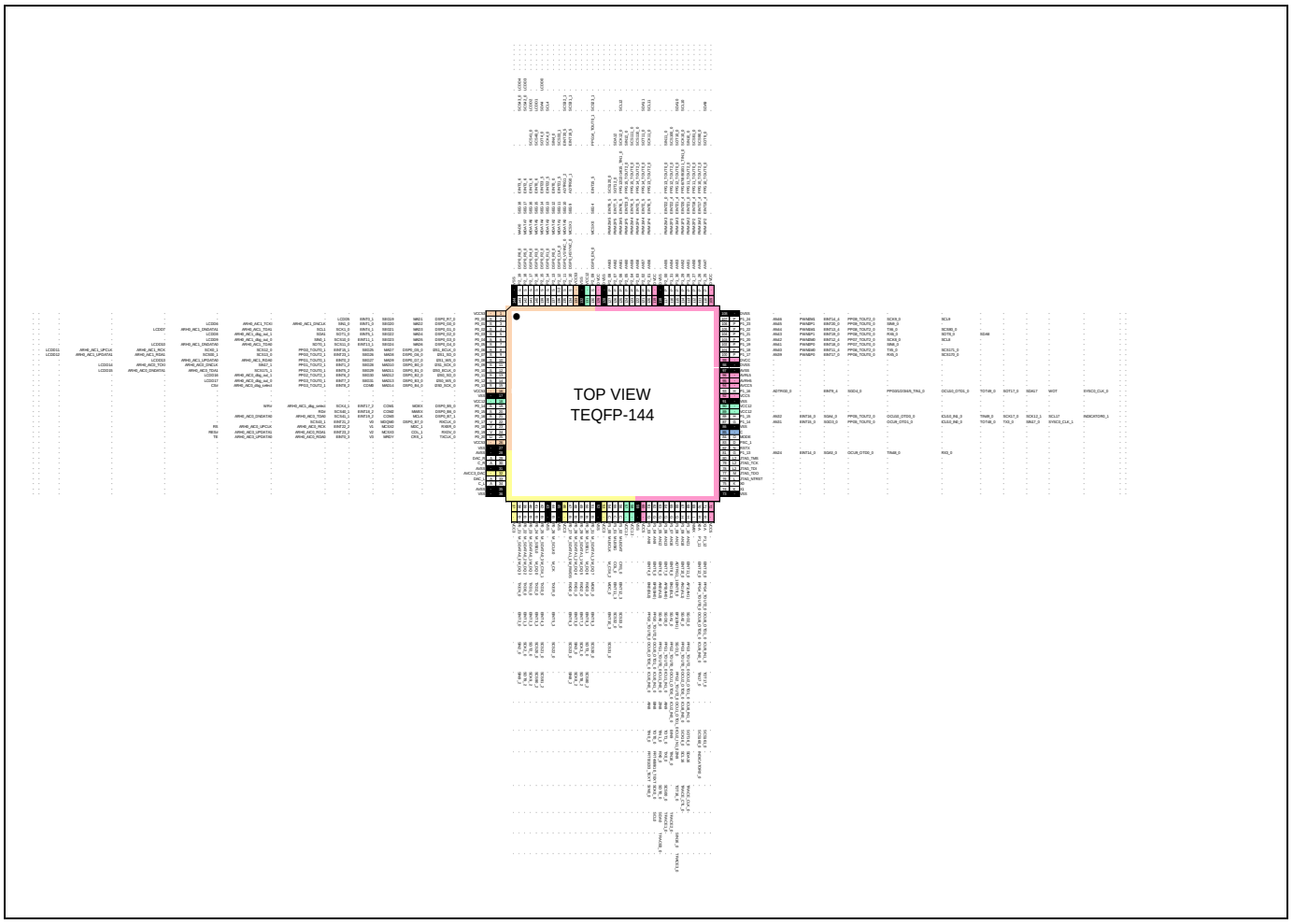
**Figure 4-8: TEQFP-176 (S6J334xJyz *1)**




*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

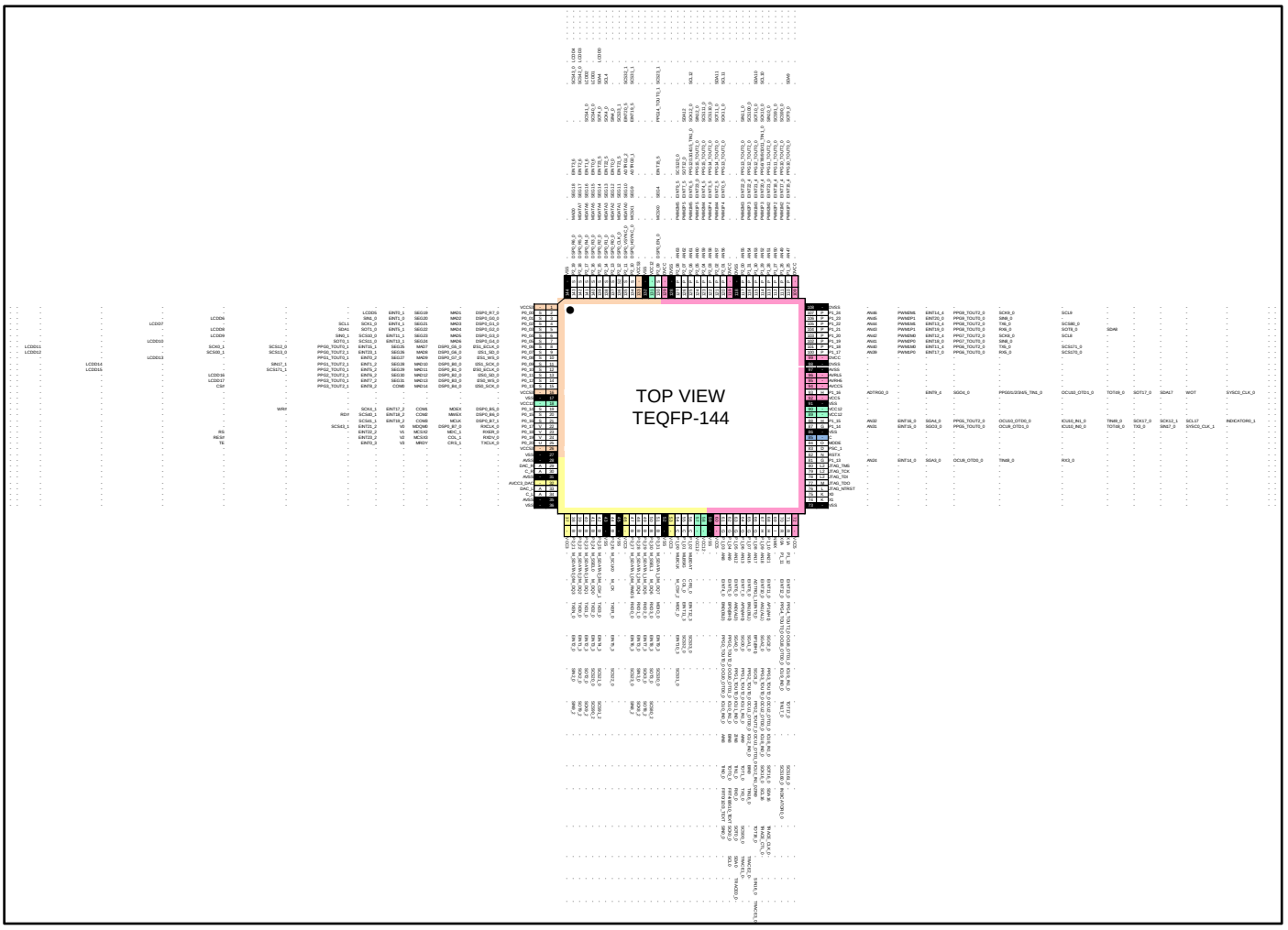
### 4.1.3 TEQFP-144 Pin Assignment

**Figure 4-9: TEQFP-144 (S6J331xHyz *1)**



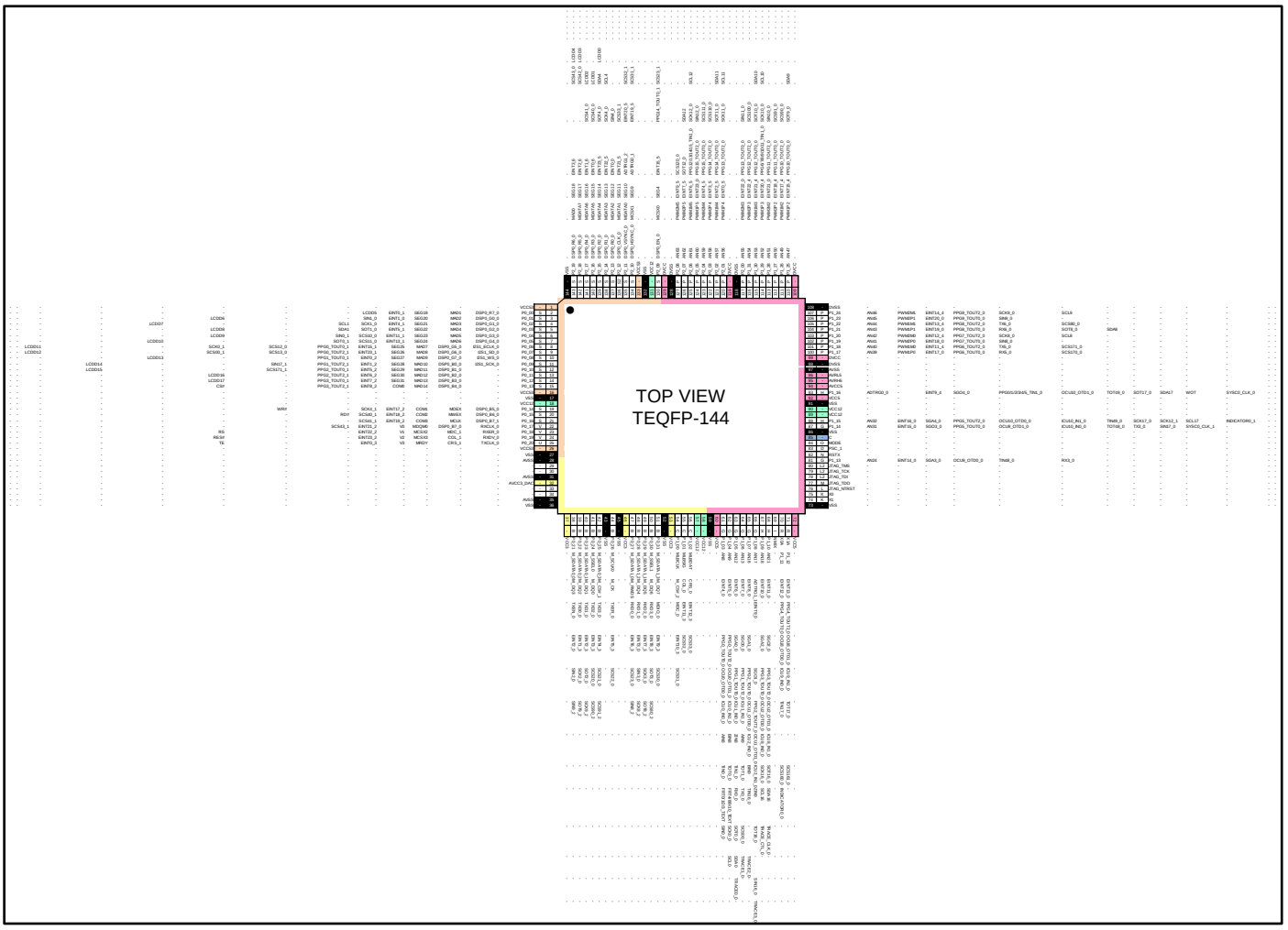

*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

**Figure 4-10: TEQFP-144 (S6J332xHyz *1)**



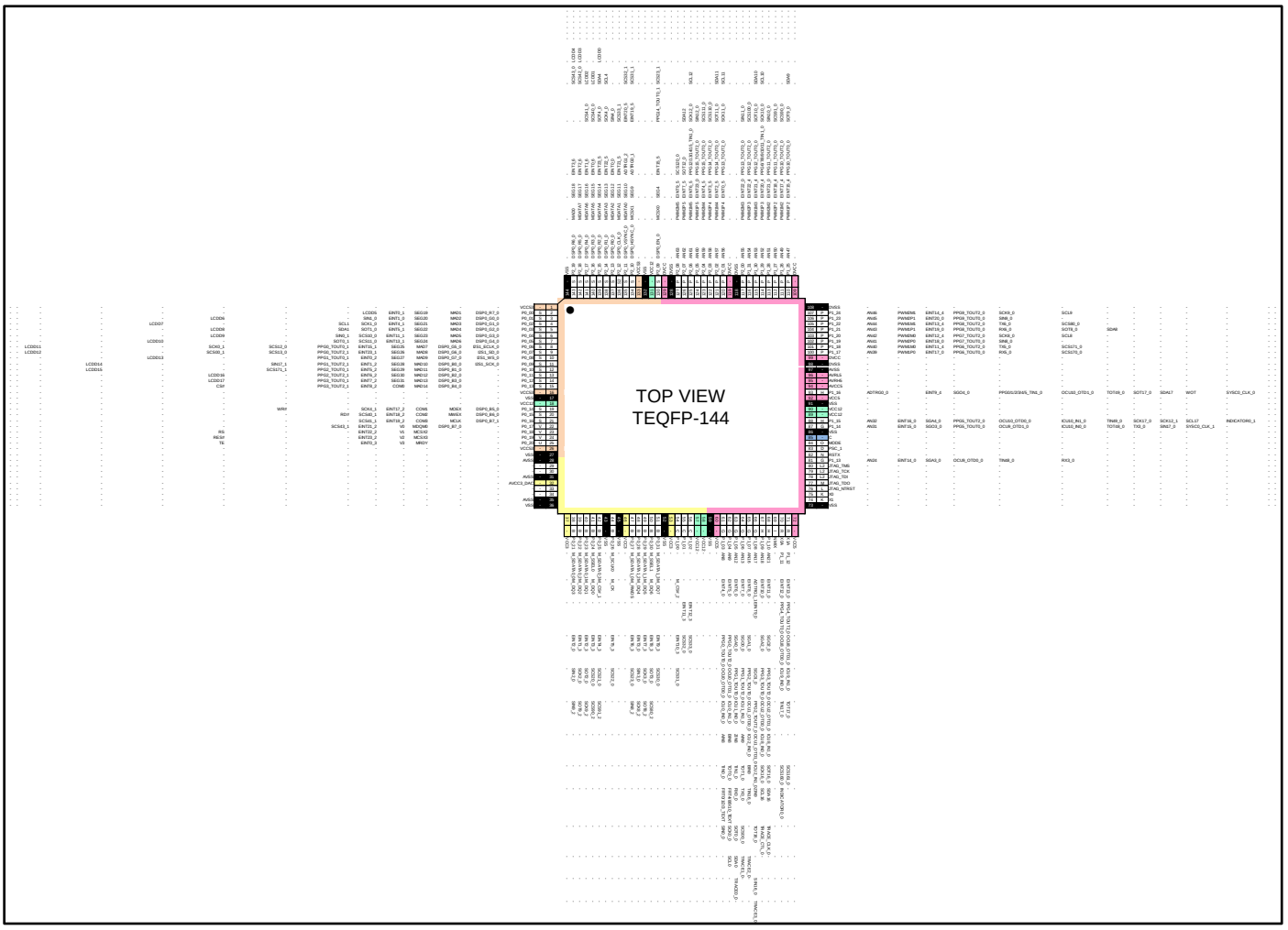

*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

**Figure 4-11: TEQFP-144 (S6J333xHyz *1)**




*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

**Figure 4-12: TEQFP-144 (S6J334xHyz *1)**



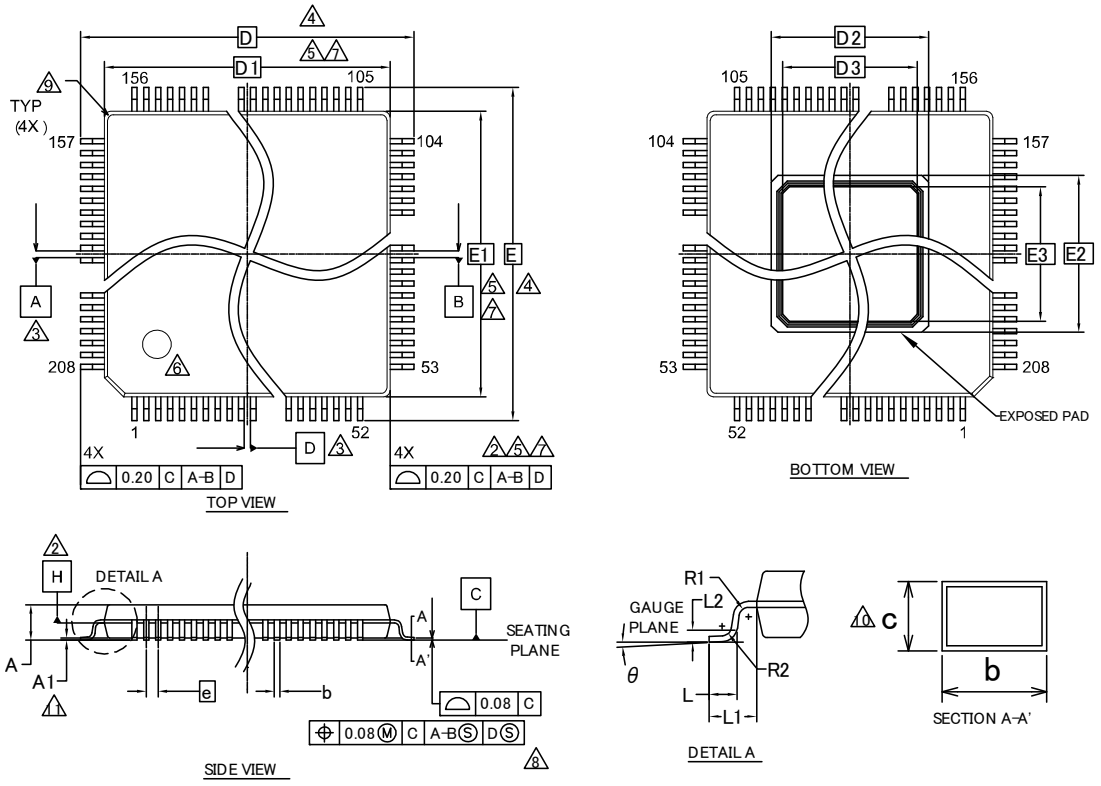

*1: x, y, z are selected from the following parameters:
x: E, D, C, B (Memory Size)
y: S, A, B, U, C, D, T, E, F, V, G, H (Option)
z: C, D, E (Revision)

## 4.2 Package Dimensions

### *4.2.1 TEQFP208*

**Figure 4-13: TEQFP208**

| Package Type | Package Code |
|---|---|
| TEQFP 208 pin | LEW208 |




| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| D | | 30.00 BSC | |
| D1 | | 28.00 BSC | |
| D2 | | 7.05 REF | |
| D3 | | 6.05 REF | |
| E | | 30.00 BSC | |
| E1 | | 28.00 BSC | |
| E2 | | 7.05 REF | |
| E3 | | 6.05 REF | |
| R1 | 0.08 | — | — |
| R2 | 0.08 | — | 0.20 |
| θ | 0° | 4° | 8° |
| c | 0.09 | — | 0.20 |
| b | 0.17 | 0.22 | 0.27 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 REF | |
| L2 | | 0.25 | |
| e | | 0.50 BSC | |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

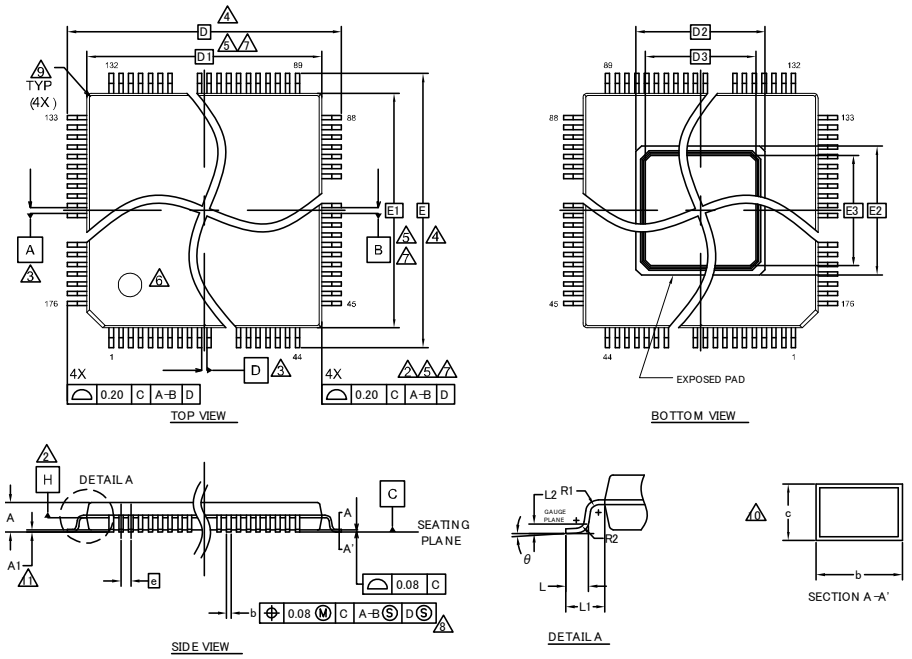
002-12477 **

PACKAGE OUTLINE, 208 LEAD TEQFP
28.0X28.0X1.7 MM LEW208 REV**

### 4.2.2 TEQFP176

**Figure 4-14: TEQFP176**

| Package Type | Package Code |
|---|---|
| TEQFP 176 pin | LEV176 |




| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | —— | —— | 1.70 |
| A1 | 0.05 | —— | 0.15 |
| D | | 26.00 BSC | |
| D1 | | 24.00 BSC | |
| D2 | | 6.65 REF | |
| D3 | | 5.45 REF | |
| E | | 26.00 BSC | |
| E1 | | 24.00 BSC | |
| E2 | | 6.65 REF | |
| E3 | | 5.45 REF | |
| R1 | 0.08 | —— | 0.20 |
| R2 | 0.08 | —— | —— |
| θ | 0° | 2° | 8° |
| c | 0.09 | —— | 0.20 |
| b | 0.17 | 0.22 | 0.27 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 REF | |
| L2 | | 0.25 | |
| e | | 0.50 BSC | |

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

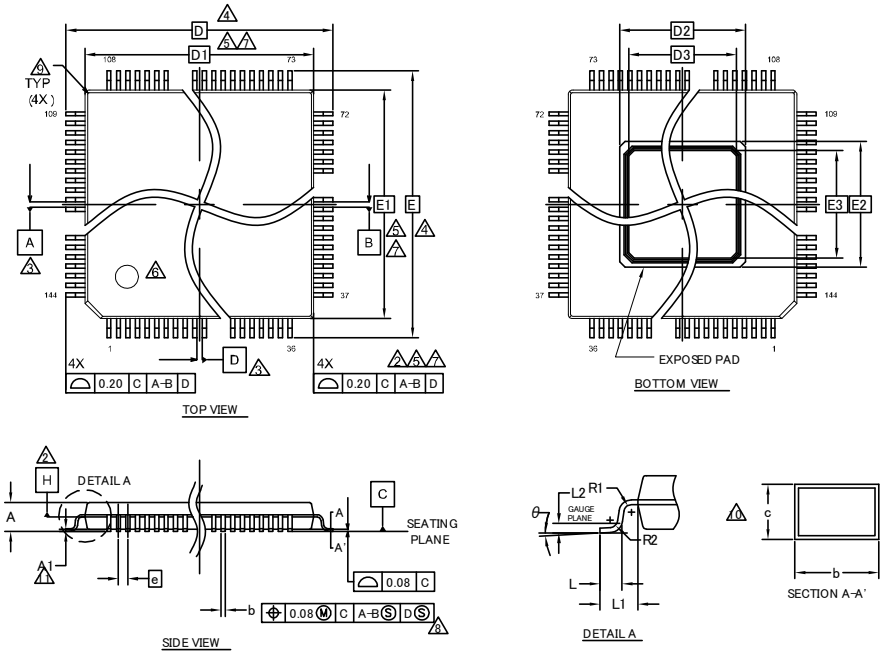
002-13653 **

PACKAGE OUTLINE, 176 LEAD TEQFP
24.0X24.0X1.7 MM LEV176 REV**

### 4.2.3 TEQFP144

**Figure 4-15: TEQFP144 (0.5 mm Pitch)**

| Package Type | Package Code |
|---|---|
| TEQFP 144 pin | LEX144 |




| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| D | | 22.00 BSC | |
| D1 | | 20.00 BSC | |
| D2 | | 5.80 REF | |
| D3 | | 4.60 REF | |
| E | | 22.00 BSC | |
| E1 | | 20.00 BSC | |
| E2 | | 5.80 REF | |
| E3 | | 4.60 REF | |
| R1 | 0.08 | — | — |
| R2 | 0.08 | — | 0.20 |
| θ | 0° | 4° | 8° |
| c | 0.09 | — | 0.20 |
| b | 0.17 | 0.22 | 0.27 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 REF | |
| L2 | | 0.25 | |
| e | | 0.50 BSC | |

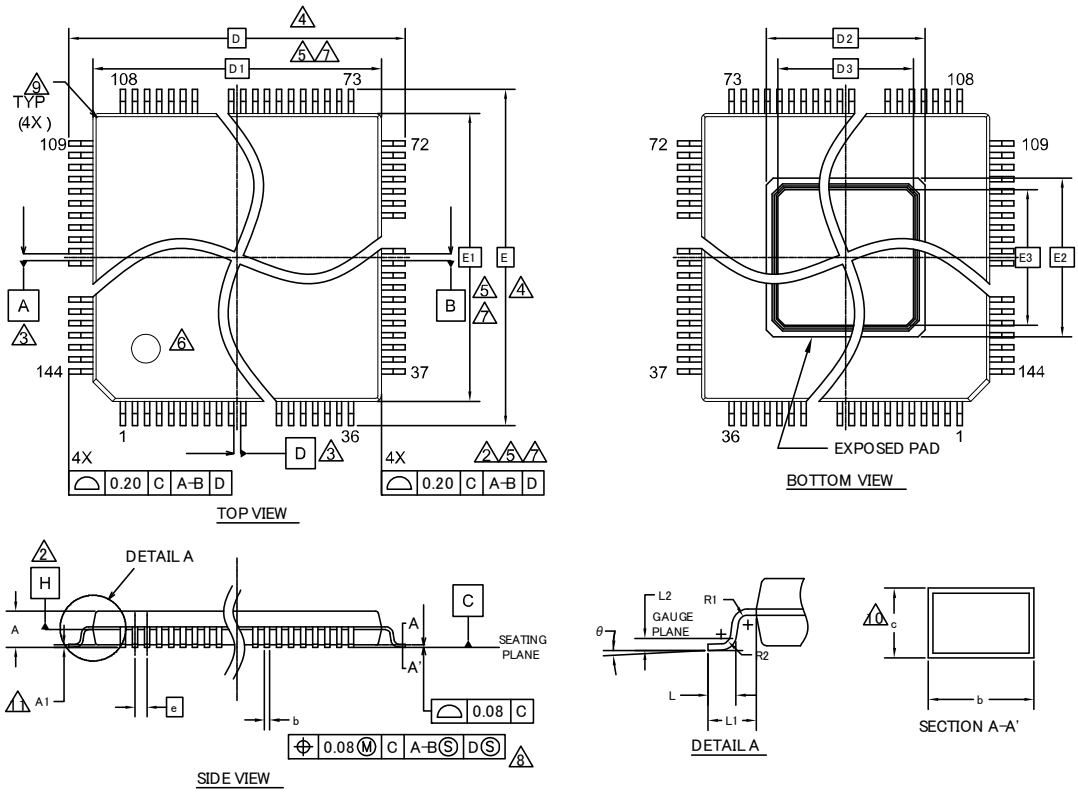
NOTES
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13553 **

PACKAGE OUTLINE, 144 LEAD TEQFP
20.0X20.0X1.7 MM LEX144 REV**

**Figure 4-16: TEQFP144 (0.4 mm Pitch)**

| Package Type | Package Code |
|---|---|
| TEQFP 144 pin | LEK144 |




| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| D | 18.00 BSC | | |
| D1 | 16.00 BSC | | |
| D2 | 5.80 REF | | |
| D3 | 4.60 REF | | |
| E | 18.00 BSC | | |
| E1 | 16.00 BSC | | |
| E2 | 5.80 REF | | |
| E3 | 4.60 REF | | |
| R1 | 0.08 | — | — |
| R2 | 0.08 | — | 0.20 |
| θ | 0° | 4° | 8° |
| c | 0.09 | — | 0.20 |
| b | 0.13 | 0.18 | 0.23 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| L2 | 0.25 | | |
| e | 0.40 BSC | | |

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

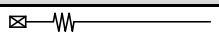
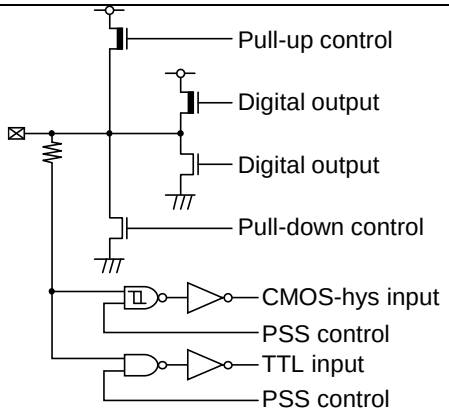
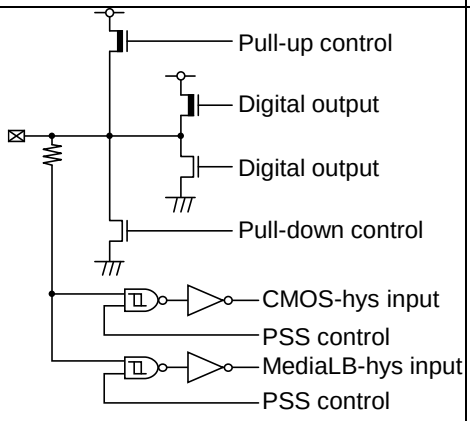
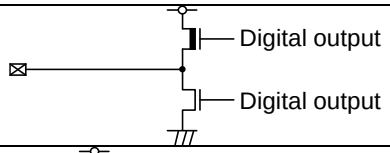
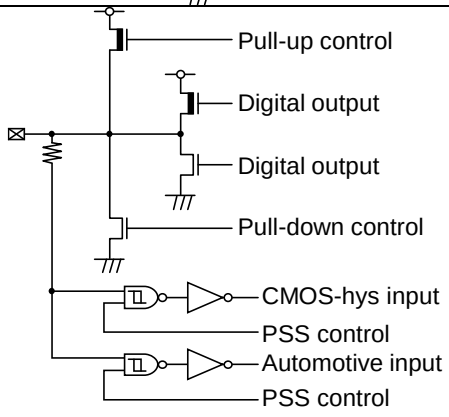
002-11502 **

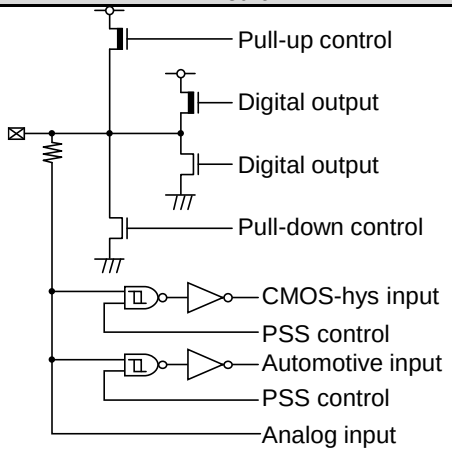
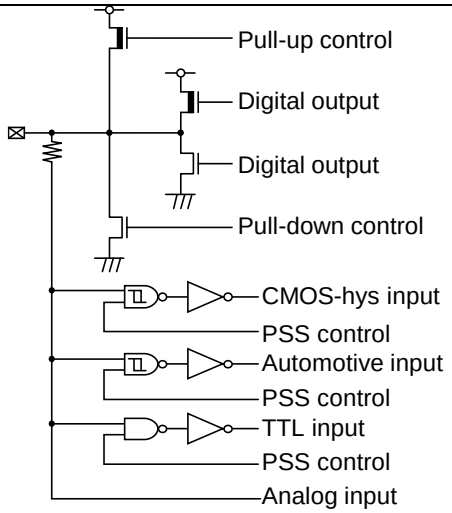
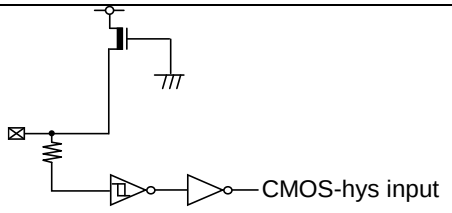
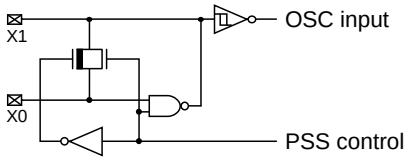
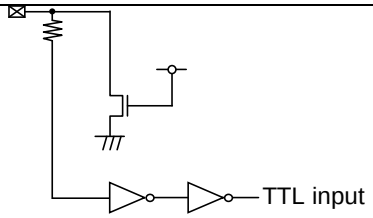
PACKAGE OUTLINE, 144 LEAD TEQFP
16.0X16.0X1.7 MM LEK144 REV**

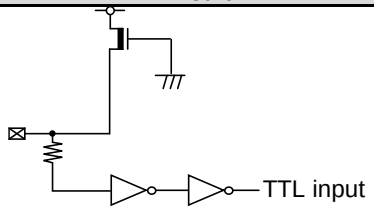
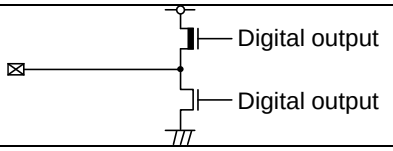
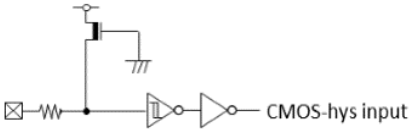
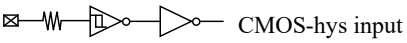
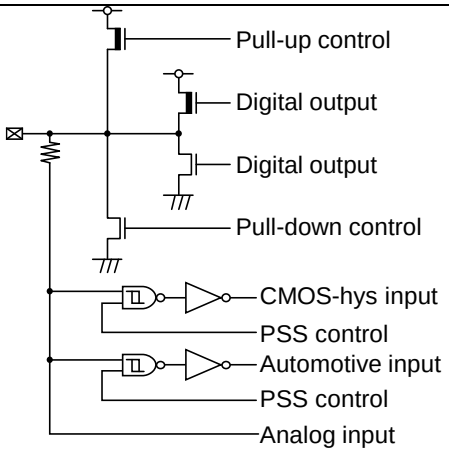
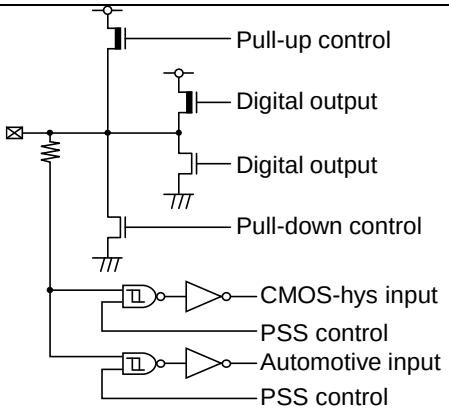
# 5. IO Circuit Type

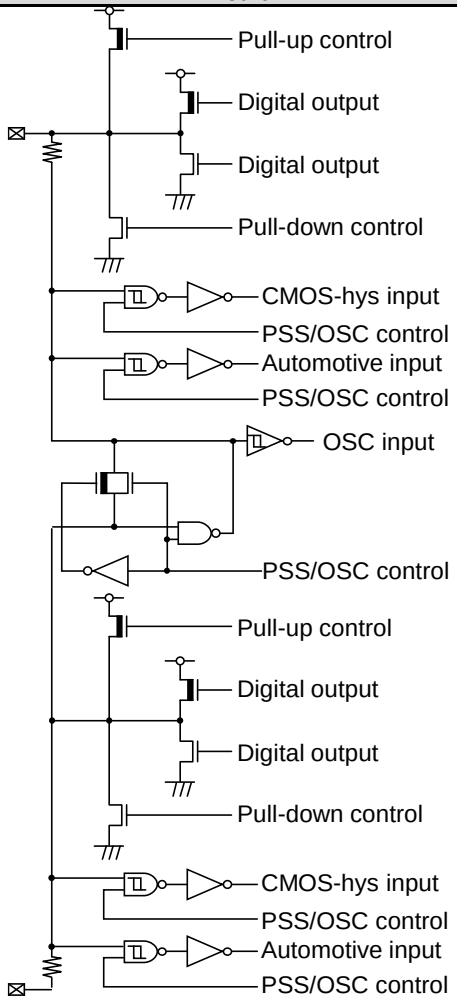
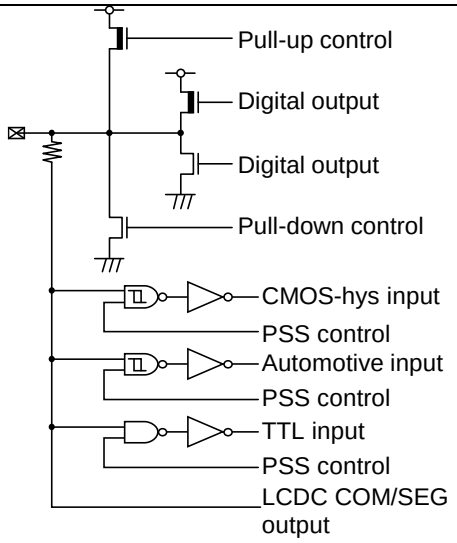
## 5.1 I/O Circuit Type

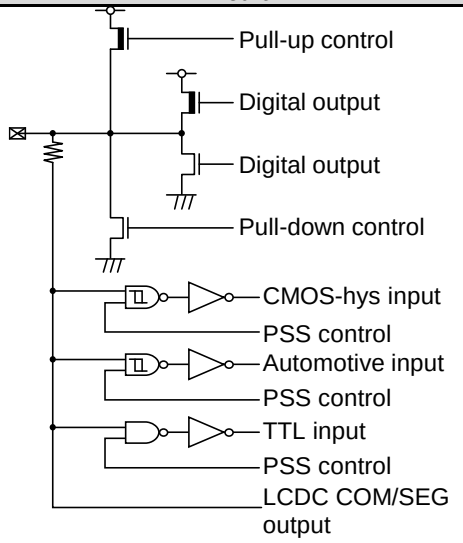
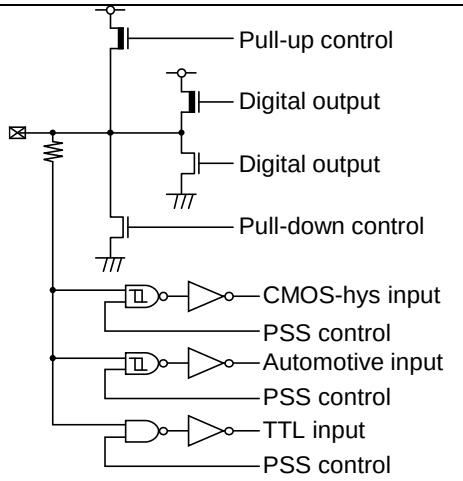
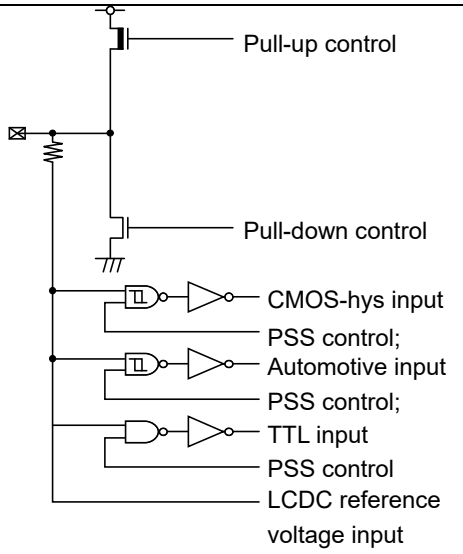
This section explains I/O circuit types.

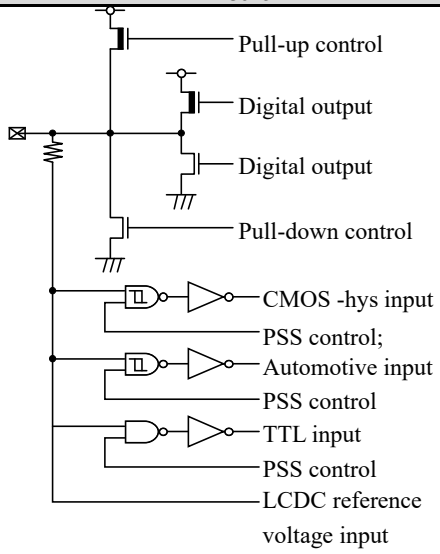
| Type | Circuit | Remarks |
|---|---|---|
| A |  | – Analog output (3 V)<br>– Audio DAC output |
| B |  | – General-purpose I/O port<br>– Output 2 mA, 5 mA, 6 mA or 15 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– TTL input |
| C |  | – General-purpose I/O port<br>– Output 2 mA, 5 mA, 6 mA or 15 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– MediaLB level hysteresis input |
| D |  | – External 1.2 V regulator control<br>– Output 2 mA |
| E |  | – General-purpose I/O port<br>– Output 1 mA, 2 mA or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input |

| Type | Circuit | Remarks |
|---|---|---|
| G |  | – General-purpose I/O port with analog input<br>– Output 1 mA, 2 mA or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input |
| H |  | – General-purpose I/O port with analog input<br>– Output 1 mA, 2 mA, 3 mA ($I^2C$) or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input<br>– TTL input |
| I |  | – 50 kΩ with pull-up<br>– CMOS hysteresis input |
| K |  | – Main oscillation I/O |
| L |  | – JTAG_NTRST<br>– 50 kΩ with pull-down<br>– TTL input |

| Type | Circuit | Remarks |
|---|---|---|
| L2 |  | – JTAG_TDI/TMS/TCK<br>– 50 kΩ with pull-up<br>– TTL input |
| M |  | – JTAG_TDO<br>– Output 5 mA |
| N |  | – RSTX input<br>– 50 kΩ with pull-up<br>– CMOS hysteresis input |
| O |  | – CMOS hysteresis input |
| P |  | – General-purpose I/O port with analog input<br>– Output 1 mA, 2 mA, 5 mA or 30 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input |
| Q |  | – General-purpose I/O port<br>– Output 1 mA, 2 mA, 5 mA or 30 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input |

| Type | Circuit | Remarks |
|---|---|---|
| R |  | – Sub oscillation I/O shared General-purpose I/O port<br>– Output 1 mA, 2 mA or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input |
| S |  | – General-purpose I/O port with LCDC COM/SEG output<br>– Output 1 mA, 2 mA or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input<br>– TTL input |

| Type | Circuit | Remarks |
|---|---|---|
| S2 |  | – General-purpose I/O port with LCDC COM/SEG output<br>– Output 1 mA, 2 mA, 5 mA or 15 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input<br>– TTL input |
| T |  | – General-purpose I/O port<br>– Output 1 mA, 2 mA or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input<br>– TTL input |
| U |  | – General-purpose input port with LCDC reference voltage input<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input<br>– TTL input |

| Type | Circuit | Remarks |
|---|---|---|
| V |  | – General-purpose I/O port with LCDC reference voltage input<br>– Output 1 mA, 2 mA or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input<br>– TTL input |

## 5.2 Note

Alphabet which shows I/O circuit type is described with corresponding pin number in pin assignment figure.

# 6. Port Description

## 6.1 Port Description List

The table shows the port function of description which is supported. The port function which is not described in the table is not supported for the product.

**Table 6-1 S6J3310 Series**

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| VCC12 | 1.2 V external power supply pin | 18, 57, 58, 89, 90, 131 | 18, 65, 66, 113, 114, 159 | 24, 73, 74, 132, 133, 191 | |
| VCC5 | 5 V external power supply pin | 60, 72, 92 | 68, 88, 116 | 76, 104, 135, | |
| VCC3 | 3 V external power supply pin | 37, 46, 53 | 45, 54, 61 | 53, 62, 69 | |
| VCC53 | 3 V/5 V external power supply pin | 1, 16, 26, 133 | 1, 16, 34, 161 | 1, 22, 42, 193 | |
| VSS | GND | 17, 27, 36, 43, 45, 52, 59, 73, 86, 91, 132, 144 | 17, 35, 44, 51, 53, 60, 67, 89, 104, 115, 160, 176 | 23, 43, 52, 59, 61, 68, 75, 105, 121, 134, 192, 208 | |
| AVCC3_DAC | Audio DAC power supply pin | 32 | 40 | 48 | |
| AVCC5 | A/D converter analog power supply pin | 94 | 118 | 142 | |
| AVRH5 | A/D converter upper limit reference voltage pin | 95 | 119 | 143 | |
| AVRL5 | A/D converter lower limit reference voltage pin | 96 | 120 | 144 | |
| AVSS | A/D converter GND | 28, 31, 35, 97 | 36, 39, 43, 121 | 44, 47, 51, 145 | |
| DVCC | SMC large current port power supply pin | 99 109 119 129 | 123 133 143 153 | 147 157 170 183 | |
| DVSS | SMC large current port GND | 98 108 118 128 | 122 132 142 152 | 146 156 169 182 | |
| X1 | Main clock oscillator output pin | 74 | 90 | 106 | |
| X0 | Main clock oscillator input pin | 75 | 91 | 107 | |
| X1A | Sub-clock oscillator output | 71 | 87 | 103 | |
| X0A | Sub-clock oscillator input | 70 | 86 | 102 | |
| NMIX | Non-maskable interrupt input pin | 69 | 85 | 101 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| RSTX | External reset input pin | 82 | 100 | 117 | |
| PSC_1 | External Power Supply Control pin | 83 | 101 | 118 | |
| MODE | Mode Pin | 84 | 102 | 119 | |
| C | External capacity connection output pin | 85 | 103 | 120 | |
| JTAG_NTRST | JTAG test reset input pin | 76 | 92 | 108 | |
| JTAG_TDO | JTAG test data output pin | 77 | 93 | 109 | |
| JTAG_TDI | JTAG test data input pin | 78 | 94 | 110 | |
| JTAG_TCK | JTAG test clock input pin | 79 | 95 | 111 | |
| JTAG_TMS | JTAG test mode state input pin | 80 | 96 | 112 | |
| TRACE0_0 | Trace data 0 output pin (0) | 63 | 77 | 89 | |
| TRACE1_0 | Trace data 1 output pin (0) | 64 | 78 | 90 | |
| TRACE2_0 | Trace data 2 output pin (0) | 65 | 81 | 93 | |
| TRACE3_0 | Trace data 3 output pin (0) | 66 | 82 | 94 | |
| TRACE_CLK_0 | Trace clock (0) | 68 | 84 | 98 | |
| TRACE_CTL_0 | Trace control (0) | 67 | 83 | 95 | |
| TRACE0_1 | Trace data 0 output pin (1) | - | 71 | 83 | |
| TRACE1_1 | Trace data 1 output pin (1) | - | 72 | 84 | |
| TRACE2_1 | Trace data 2 output pin (1) | - | 75 | 87 | |
| TRACE3_1 | Trace data 3 output pin (1) | - | 76 | 88 | |
| TRACE_CLK_1 | Trace clock (1) | - | 80 | 92 | |
| TRACE_CTL_1 | Trace control (1) | - | 79 | 91 | |
| ADTRG0_0 | A/D converter external trigger input pin (0) | 93 | 117 | 139 | |
| ADTRG1_0 | A/D converter external trigger input pin (0) | - | - | 140 | |
| ADTRG0_1 | A/D converter external trigger input pin (1) | 134 | 166 | 198 | |
| ADTRG1_1 | A/D converter external trigger input pin (1) | 66 | 82 | 94 | |
| ADTRG1_2 | A/D converter external trigger input pin (2) | 135 | 167 | 199 | |
| AN4 | ADC Unit0 ch.4 input pin | - | 69 | 81 | |
| AN5 | ADC Unit0 ch.5 input pin | - | 70 | 82 | |
| AN6 | ADC Unit0 ch.6 input pin | - | 71 | 83 | |
| AN7 | ADC Unit0 ch.7 input pin | - | 72 | 84 | |
| AN8 | ADC Unit0 ch.8 input pin | 61 | 73 | 85 | |
| AN9 | ADC Unit0 ch.9 input pin | 62 | 74 | 86 | |
| AN10 | ADC Unit0 ch.10 input pin | - | 75 | 87 | |
| AN11 | ADC Unit0 ch.11 input pin | - | 76 | 88 | |
| AN12 | ADC Unit0 ch.12 input pin | 63 | 77 | 89 | |
| AN13 | ADC Unit0 ch.13 input pin | 64 | 78 | 90 | |
| AN14 | ADC Unit0 ch.14 input pin | - | 79 | 91 | |
| AN15 | ADC Unit0 ch.15 input pin | - | 80 | 92 | |
| AN16 | ADC Unit0 ch.16 input pin | 65 | 81 | 93 | |
| AN17 | ADC Unit0 ch.17 input pin | 66 | 82 | 94 | |
| AN18 | ADC Unit0 ch.18 input pin | 67 | 83 | 95 | |
| AN21 | ADC Unit0 ch.21 input pin | 68 | 84 | 98 | |
| AN24 | ADC Unit0 ch.24 input pin | 81 | 97 | 113 | |
| AN25 | ADC Unit0 ch.25 input pin | - | 98 | 114 | |
| AN26 | ADC Unit0 ch.26 input pin | - | 99 | 115 | |
| AN28 | ADC Unit0 ch.28 input pin | - | 108 | 125 | |
| AN29 | ADC Unit0 ch.29 input pin | - | 109 | 126 | |
| AN30 | ADC Unit0 ch.30 input pin | - | 110 | 127 | |
| AN31 | ADC Unit0 ch.31 input pin | 87 | 111 | 128 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| AN32 | ADC Unit1 ch.32 input pin | 88 | 112 | 129 | |
| AN39 | ADC Unit1 ch.39 input pin | 100 | 124 | 148 | |
| AN40 | ADC Unit1 ch.40 input pin | 101 | 125 | 149 | |
| AN41 | ADC Unit1 ch.41 input pin | 102 | 126 | 150 | |
| AN42 | ADC Unit1 ch.42 input pin | 103 | 127 | 151 | |
| AN43 | ADC Unit1 ch.43 input pin | 104 | 128 | 152 | |
| AN44 | ADC Unit1 ch.44 input pin | 105 | 129 | 153 | |
| AN45 | ADC Unit1 ch.45 input pin | 106 | 130 | 154 | |
| AN46 | ADC Unit1 ch.46 input pin | 107 | 131 | 155 | |
| AN47 | ADC Unit1 ch.47 input pin | 110 | 134 | 158 | |
| AN49 | ADC Unit1 ch.49 input pin | 111 | 135 | 160 | |
| AN50 | ADC Unit1 ch.50 input pin | 112 | 136 | 161 | |
| AN51 | ADC Unit1 ch.51 input pin | 113 | 137 | 162 | |
| AN52 | ADC Unit1 ch.52 input pin | 114 | 138 | 164 | |
| AN53 | ADC Unit1 ch.53 input pin | 115 | 139 | 165 | |
| AN54 | ADC Unit1 ch.54 input pin | 116 | 140 | 166 | |
| AN55 | ADC Unit1 ch.55 input pin | 117 | 141 | 168 | |
| AN56 | ADC Unit1 ch.56 input pin | 120 | 144 | 171 | |
| AN57 | ADC Unit1 ch.57 input pin | 121 | 145 | 173 | |
| AN58 | ADC Unit1 ch.58 input pin | 122 | 146 | 174 | |
| AN59 | ADC Unit1 ch.59 input pin | 123 | 147 | 175 | |
| AN60 | ADC Unit1 ch.60 input pin | 124 | 148 | 177 | |
| AN61 | ADC Unit1 ch.61 input pin | 125 | 149 | 178 | |
| AN62 | ADC Unit1 ch.62 input pin | 126 | 150 | 179 | |
| AN63 | ADC Unit1 ch.63 input pin | 127 | 151 | 181 | |
| TX0_0 | CAN transmission data 0 output pin (0) | 64 | 78 | 90 | |
| TX1_0 | CAN transmission data 1 output pin (0) | - | - | 94 | |
| TX2_0 | CAN transmission data 2 output pin (0) | - | - | 103 | |
| TX3_0 | CAN transmission data 3 output pin (0) | 87 | 111 | 128 | |
| TX5_0 | CAN transmission data 5 output pin (0) | 101 | 125 | 149 | |
| TX6_0 | CAN transmission data 6 output pin (0) | 105 | 129 | 153 | |
| TX0_1 | CAN transmission data 0 output pin (1) | - | 71 | 83 | |
| TX1_1 | CAN transmission data 1 output pin (1) | - | - | 87 | |
| TX2_1 | CAN transmission data 2 output pin (1) | - | - | 92 | |
| TX3_1 | CAN transmission data 3 output pin (1) | - | 99 | 115 | |
| TX5_1 | CAN transmission data 5 output pin (1) | - | 107 | 124 | |
| TX6_1 | CAN transmission data 6 output pin (1) | - | 110 | 127 | |
| TX0_2 | CAN transmission data 0 output pin (2) | - | - | 7 | |
| TX3_2 | CAN transmission data 3 output pin (2) | - | - | 16 | |
| RX0_0 | CAN reception data 0 input pin (0) | 63 | 77 | 89 | |
| RX1_0 | CAN reception data 1 input pin (0) | - | - | 93 | |
| RX2_0 | CAN reception data 2 input pin (0) | - | - | 102 | |
| RX3_0 | CAN reception data 3 input pin (0) | 81 | 97 | 113 | |
| RX5_0 | CAN reception data 5 input pin (0) | 100 | 124 | 148 | |
| RX6_0 | CAN reception data 6 input pin (0) | 104 | 128 | 152 | |
| RX0_1 | CAN reception data 0 input pin (1) | - | 70 | 82 | |
| RX1_1 | CAN reception data 1 input pin (1) | - | - | 84 | |
| RX2_1 | CAN reception data 2 input pin (1) | - | - | 91 | |
| RX3_1 | CAN reception data 3 input pin (1) | - | 98 | 114 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| RX5_1 | CAN reception data 5 input pin (1) | - | 106 | 123 | |
| RX6_1 | CAN reception data 6 input pin (1) | - | 109 | 126 | |
| RX0_2 | CAN reception data 0 input pin (2) | - | - | 6 | |
| RX3_2 | CAN reception data 3 input pin (2) | - | - | 15 | |
| EINT0_0 | External interrupt input pin (0) | 137 | 169 | 201 | |
| EINT1_0 | External interrupt input pin (0) | 3 | 3 | 3 | |
| EINT2_0 | External interrupt input pin (0) | 38 | 46 | 54 | |
| EINT3_0 | External interrupt input pin (0) | 48 | 56 | 64 | |
| EINT4_0 | External interrupt input pin (0) | 61 | 73 | 85 | |
| EINT5_0 | External interrupt input pin (0) | 62 | 74 | 86 | |
| EINT6_0 | External interrupt input pin (0) | 63 | 77 | 89 | |
| EINT7_0 | External interrupt input pin (0) | 64 | 78 | 90 | |
| EINT8_0 | External interrupt input pin (0) | 65 | 81 | 93 | |
| EINT9_0 | External interrupt input pin (0) | 66 | 82 | 94 | |
| EINT10_0 | External interrupt input pin (0) | 67 | 83 | 95 | |
| EINT11_0 | External interrupt input pin (0) | 68 | 84 | 98 | |
| EINT12_0 | External interrupt input pin (0) | 70 | 86 | 102 | |
| EINT13_0 | External interrupt input pin (0) | 71 | 87 | 103 | |
| EINT14_0 | External interrupt input pin (0) | 81 | 97 | 113 | |
| EINT15_0 | External interrupt input pin (0) | 87 | 111 | 128 | |
| EINT16_0 | External interrupt input pin (0) | 88 | 112 | 129 | |
| EINT17_0 | External interrupt input pin (0) | 100 | 124 | 148 | |
| EINT18_0 | External interrupt input pin (0) | 102 | 126 | 150 | |
| EINT19_0 | External interrupt input pin (0) | 104 | 128 | 152 | |
| EINT20_0 | External interrupt input pin (0) | 106 | 130 | 154 | |
| EINT21_0 | External interrupt input pin (0) | 113 | 137 | 162 | |
| EINT22_0 | External interrupt input pin (0) | 117 | 141 | 168 | |
| EINT23_0 | External interrupt input pin (0) | 124 | 148 | 177 | |
| EINT0_1 | External interrupt input pin (1) | 2 | 2 | 2 | |
| EINT1_1 | External interrupt input pin (1) | - | 19 | 25 | |
| EINT2_1 | External interrupt input pin (1) | - | - | 184 | |
| EINT3_1 | External interrupt input pin (1) | - | 162 | 194 | |
| EINT4_1 | External interrupt input pin (1) | 4 | 4 | 4 | |
| EINT5_1 | External interrupt input pin (1) | 5 | 5 | 5 | |
| EINT6_1 | External interrupt input pin (1) | - | 70 | 82 | |
| EINT7_1 | External interrupt input pin (1) | - | - | 6 | |
| EINT8_1 | External interrupt input pin (1) | - | 72 | 84 | |
| EINT9_1 | External interrupt input pin (1) | - | - | 7 | |
| EINT10_1 | External interrupt input pin (1) | - | - | 8 | |
| EINT11_1 | External interrupt input pin (1) | 6 | 6 | 9 | |
| EINT12_1 | External interrupt input pin (1) | - | 79 | 91 | |
| EINT13_1 | External interrupt input pin (1) | 7 | 7 | 10 | |
| EINT14_1 | External interrupt input pin (1) | - | 98 | 114 | |
| EINT15_1 | External interrupt input pin (1) | 8 | 8 | 11 | |
| EINT16_1 | External interrupt input pin (1) | - | - | 136 | |
| EINT17_1 | External interrupt input pin (1) | - | 106 | 123 | |
| EINT18_1 | External interrupt input pin (1) | - | 69 | 81 | |
| EINT19_1 | External interrupt input pin (1) | - | 109 | 126 | |
| EINT20_1 | External interrupt input pin (1) | - | 105 | 122 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| EINT21_1 | External interrupt input pin (1) | - | 75 | 87 | |
| EINT22_1 | External interrupt input pin (1) | - | - | 140 | |
| EINT23_1 | External interrupt input pin (1) | 9 | 9 | 12 | |
| EINT0_2 | External interrupt input pin (2) | 10 | 10 | 13 | |
| EINT1_2 | External interrupt input pin (2) | 11 | 11 | 14 | |
| EINT2_2 | External interrupt input pin (2) | - | - | 15 | |
| EINT3_2 | External interrupt input pin (2) | - | - | 16 | |
| EINT4_2 | External interrupt input pin (2) | - | - | 17 | |
| EINT5_2 | External interrupt input pin (2) | 12 | 12 | 18 | |
| EINT6_2 | External interrupt input pin (2) | 13 | 13 | 19 | |
| EINT7_2 | External interrupt input pin (2) | 14 | 14 | 20 | |
| EINT8_2 | External interrupt input pin (2) | 15 | 15 | 21 | |
| EINT9_2 | External interrupt input pin (2) | - | 20 | 26 | |
| EINT10_2 | External interrupt input pin (2) | - | 21 | 27 | |
| EINT11_2 | External interrupt input pin (2) | - | 22 | 28 | |
| EINT12_2 | External interrupt input pin (2) | - | 23 | 29 | |
| EINT13_2 | External interrupt input pin (2) | - | - | 30 | |
| EINT14_2 | External interrupt input pin (2) | - | - | 31 | |
| EINT15_2 | External interrupt input pin (2) | - | 24 | 32 | |
| EINT16_2 | External interrupt input pin (2) | - | 25 | 33 | |
| EINT17_2 | External interrupt input pin (2) | 19 | 26 | 34 | |
| EINT18_2 | External interrupt input pin (2) | 20 | 27 | 35 | |
| EINT19_2 | External interrupt input pin (2) | 21 | 28 | 36 | |
| EINT20_2 | External interrupt input pin (2) | - | 29 | 37 | |
| EINT21_2 | External interrupt input pin (2) | 22 | 30 | 38 | |
| EINT22_2 | External interrupt input pin (2) | 23 | 31 | 39 | |
| EINT23_2 | External interrupt input pin (2) | 24 | 32 | 40 | |
| EINT0_3 | External interrupt input pin (3) | 25 | 33 | 41 | |
| EINT1_3 | External interrupt input pin (3) | 39 | 47 | 55 | |
| EINT2_3 | External interrupt input pin (3) | 40 | 48 | 56 | |
| EINT3_3 | External interrupt input pin (3) | 41 | 49 | 57 | |
| EINT4_3 | External interrupt input pin (3) | 42 | 50 | 58 | |
| EINT5_3 | External interrupt input pin (3) | 44 | 52 | 60 | |
| EINT6_3 | External interrupt input pin (3) | 47 | 55 | 63 | |
| EINT7_3 | External interrupt input pin (3) | 49 | 57 | 65 | |
| EINT8_3 | External interrupt input pin (3) | 50 | 58 | 66 | |
| EINT9_3 | External interrupt input pin (3) | 51 | 59 | 67 | |
| EINT10_3 | External interrupt input pin (3) | 54 | 62 | 70 | |
| EINT11_3 | External interrupt input pin (3) | 55 | 63 | 71 | |
| EINT12_3 | External interrupt input pin (3) | 56 | 64 | 72 | |
| EINT13_3 | External interrupt input pin (3) | - | - | 77 | |
| EINT14_3 | External interrupt input pin (3) | - | - | 78 | |
| EINT15_3 | External interrupt input pin (3) | - | - | 79 | |
| EINT16_3 | External interrupt input pin (3) | - | - | 80 | |
| EINT17_3 | External interrupt input pin (3) | - | 71 | 83 | |
| EINT18_3 | External interrupt input pin (3) | - | 76 | 88 | |
| EINT19_3 | External interrupt input pin (3) | - | 80 | 92 | |
| EINT20_3 | External interrupt input pin (3) | - | - | 96 | |
| EINT21_3 | External interrupt input pin (3) | - | - | 97 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| EINT22_3 | External interrupt input pin (3) | - | - | 99 | |
| EINT23_3 | External interrupt input pin (3) | - | - | 100 | |
| EINT0_4 | External interrupt input pin (4) | - | 99 | 115 | |
| EINT1_4 | External interrupt input pin (4) | - | - | 116 | |
| EINT2_4 | External interrupt input pin (4) | - | 107 | 124 | |
| EINT3_4 | External interrupt input pin (4) | - | 108 | 125 | |
| EINT4_4 | External interrupt input pin (4) | - | 110 | 127 | |
| EINT5_4 | External interrupt input pin (4) | - | - | 130 | |
| EINT6_4 | External interrupt input pin (4) | - | - | 131 | |
| EINT7_4 | External interrupt input pin (4) | - | - | 137 | |
| EINT8_4 | External interrupt input pin (4) | - | - | 138 | |
| EINT9_4 | External interrupt input pin (4) | 93 | 117 | 139 | |
| EINT10_4 | External interrupt input pin (4) | - | - | 141 | |
| EINT11_4 | External interrupt input pin (4) | 101 | 125 | 149 | |
| EINT12_4 | External interrupt input pin (4) | 103 | 127 | 151 | |
| EINT13_4 | External interrupt input pin (4) | 105 | 129 | 153 | |
| EINT14_4 | External interrupt input pin (4) | 107 | 131 | 155 | |
| EINT15_4 | External interrupt input pin (4) | 110 | 134 | 158 | |
| EINT16_4 | External interrupt input pin (4) | - | - | 159 | |
| EINT17_4 | External interrupt input pin (4) | 111 | 135 | 160 | |
| EINT18_4 | External interrupt input pin (4) | 112 | 136 | 161 | |
| EINT19_4 | External interrupt input pin (4) | - | - | 163 | |
| EINT20_4 | External interrupt input pin (4) | 114 | 138 | 164 | |
| EINT21_4 | External interrupt input pin (4) | 115 | 139 | 165 | |
| EINT22_4 | External interrupt input pin (4) | 116 | 140 | 166 | |
| EINT23_4 | External interrupt input pin (4) | - | - | 167 | |
| EINT0_5 | External interrupt input pin (5) | 120 | 144 | 171 | |
| EINT1_5 | External interrupt input pin (5) | - | - | 172 | |
| EINT2_5 | External interrupt input pin (5) | 121 | 145 | 173 | |
| EINT3_5 | External interrupt input pin (5) | 122 | 146 | 174 | |
| EINT4_5 | External interrupt input pin (5) | 123 | 147 | 175 | |
| EINT5_5 | External interrupt input pin (5) | - | - | 176 | |
| EINT6_5 | External interrupt input pin (5) | 125 | 149 | 178 | |
| EINT7_5 | External interrupt input pin (5) | 126 | 150 | 179 | |
| EINT8_5 | External interrupt input pin (5) | - | - | 180 | |
| EINT9_5 | External interrupt input pin (5) | 127 | 151 | 181 | |
| EINT10_5 | External interrupt input pin (5) | - | - | 185 | |
| EINT11_5 | External interrupt input pin (5) | - | 154 | 186 | |
| EINT12_5 | External interrupt input pin (5) | - | 155 | 187 | |
| EINT13_5 | External interrupt input pin (5) | - | 156 | 188 | |
| EINT14_5 | External interrupt input pin (5) | - | 157 | 189 | |
| EINT15_5 | External interrupt input pin (5) | 130 | 158 | 190 | |
| EINT16_5 | External interrupt input pin (5) | - | 163 | 195 | |
| EINT17_5 | External interrupt input pin (5) | - | 164 | 196 | |
| EINT18_5 | External interrupt input pin (5) | - | 165 | 197 | |
| EINT19_5 | External interrupt input pin (5) | 134 | 166 | 198 | |
| EINT20_5 | External interrupt input pin (5) | 135 | 167 | 199 | |
| EINT21_5 | External interrupt input pin (5) | 136 | 168 | 200 | |
| EINT22_5 | External interrupt input pin (5) | 138 | 170 | 202 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| EINT23_5 | External interrupt input pin (5) | 139 | 171 | 203 | |
| EINT0_6 | External interrupt input pin (6) | 140 | 172 | 204 | |
| EINT1_6 | External interrupt input pin (6) | 141 | 173 | 205 | |
| EINT2_6 | External interrupt input pin (6) | 142 | 174 | 206 | |
| EINT3_6 | External interrupt input pin (6) | 143 | 175 | 207 | |
| SCS00_0 | Multi-function serial ch.0 chip select 0 I/O pin (0) | 64 | 78 | 90 | |
| SCS10_0 | Multi-function serial ch.1 chip select 0 I/O pin (0) | 6 | 6 | 9 | |
| SCS11_0 | Multi-function serial ch.1 chip select 1 output pin (0) | 7 | 7 | 10 | |
| SCS12_0 | Multi-function serial ch.1 chip select 2 output pin (0) | 8 | 8 | 11 | |
| SCS13_0 | Multi-function serial ch.1 chip select 3 output pin (0) | 9 | 9 | 12 | |
| SCS20_0 | Multi-function serial ch.2 chip select 0 I/O pin (0) | 41 | 49 | 57 | |
| SCS21_0 | Multi-function serial ch.2 chip select 1 output pin (0) | 42 | 50 | 58 | |
| SCS22_0 | Multi-function serial ch.2 chip select 2 output pin (0) | 44 | 52 | 60 | |
| SCS23_0 | Multi-function serial ch.2 chip select 3 output pin (0) | 47 | 55 | 63 | |
| SCS30_0 | Multi-function serial ch.3 chip select 0 I/O pin (0) | 51 | 59 | 67 | |
| SCS31_0 | Multi-function serial ch.3 chip select 1 output pin (0) | 54 | 62 | 70 | |
| SCS32_0 | Multi-function serial ch.3 chip select 2 output pin (0) | 55 | 63 | 71 | |
| SCS33_0 | Multi-function serial ch.3 chip select 3 output pin (0) | 56 | 64 | 72 | |
| SCS40_0 | Multi-function serial ch.4 chip select 0 I/O pin (0) | 140 | 172 | 204 | |
| SCS41_0 | Multi-function serial ch.4 chip select 1 output pin (0) | 141 | 173 | 205 | |
| SCS42_0 | Multi-function serial ch.4 chip select 2 output pin (0) | 142 | 174 | 206 | |
| SCS43_0 | Multi-function serial ch.4 chip select 3 output pin (0) | 143 | 175 | 207 | |
| SCS80_0 | Multi-function serial ch.8 chip select 0 I/O pin (0) | 105 | 129 | 153 | |
| SCS90_0 | Multi-function serial ch.9 chip select 0 I/O pin (0) | 111 | 135 | 160 | |
| SCS91_0 | Multi-function serial ch.9 chip select 1 output pin (0) | 112 | 136 | 161 | |
| SCS100_0 | Multi-function serial ch.10 chip select 0 I/O pin (0) | 116 | 140 | 166 | |
| SCS110_0 | Multi-function serial ch.11 chip select 0 I/O pin (0) | 122 | 146 | 174 | |
| SCS111_0 | Multi-function serial ch.11 chip select 1 output pin (0) | 123 | 147 | 175 | |
| SCS120_0 | Multi-function serial ch.12 chip select 0 I/O pin (0) | 127 | 151 | 181 | |
| SCS160_0 | Multi-function serial ch.16 chip select 0 I/O pin (0) | 70 | 86 | 102 | |
| SCS161_0 | Multi-function serial ch.16 chip select 1 output pin (0) | 71 | 87 | 103 | |
| SCS170_0 | Multi-function serial ch.17 chip select 0 I/O pin (0) | 100 | 124 | 148 | |
| SCS171_0 | Multi-function serial ch.17 chip select 1 output pin (0) | 101 | 125 | 149 | |
| SCS00_1 | Multi-function serial ch.0 chip select 0 I/O pin (1) | 9 | 9 | 12 | |
| SCS10_1 | Multi-function serial ch.1 chip select 0 I/O pin (1) | - | 22 | 28 | |
| SCS11_1 | Multi-function serial ch.1 chip select 1 output pin (1) | - | 23 | 29 | |
| SCS12_1 | Multi-function serial ch.1 chip select 2 output pin (1) | - | 24 | 32 | |
| SCS13_1 | Multi-function serial ch.1 chip select 3 output pin (1) | - | 25 | 33 | |
| SCS20_1 | Multi-function serial ch.2 chip select 0 I/O pin (1) | - | 155 | 187 | |
| SCS21_1 | Multi-function serial ch.2 chip select 1 output pin (1) | - | 156 | 188 | |
| SCS22_1 | Multi-function serial ch.2 chip select 2 output pin (1) | - | 157 | 189 | |
| SCS23_1 | Multi-function serial ch.2 chip select 3 output pin (1) | 130 | 158 | 190 | |
| SCS30_1 | Multi-function serial ch.3 chip select 0 I/O pin (1) | - | 165 | 197 | |
| SCS31_1 | Multi-function serial ch.3 chip select 1 output pin (1) | 134 | 166 | 198 | |
| SCS32_1 | Multi-function serial ch.3 chip select 2 output pin (1) | 135 | 167 | 199 | |
| SCS33_1 | Multi-function serial ch.3 chip select 3 output pin (1) | 136 | 168 | 200 | |
| SCS40_1 | Multi-function serial ch.4 chip select 0 I/O pin (1) | 20 | 27 | 35 | |
| SCS41_1 | Multi-function serial ch.4 chip select 1 output pin (1) | 21 | 28 | 36 | |
| SCS42_1 | Multi-function serial ch.4 chip select 2 output pin (1) | - | 29 | 37 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| SCS43_1 | Multi-function serial ch.4 chip select 3 output pin (1) | 22 | 30 | 38 | |
| SCS80_1 | Multi-function serial ch.8 chip select 0 I/O pin (1) | - | 72 | 84 | |
| SCS90_1 | Multi-function serial ch.9 chip select 0 I/O pin (1) | - | 108 | 125 | |
| SCS91_1 | Multi-function serial ch.9 chip select 1 output pin (1) | - | 109 | 126 | |
| SCS100_1 | Multi-function serial ch.10 chip select 0 I/O pin (1) | - | 80 | 92 | |
| SCS120_1 | Multi-function serial ch.12 chip select 0 I/O pin (1) | - | 110 | 127 | |
| SCS160_1 | Multi-function serial ch.16 chip select 0 I/O pin (1) | - | - | 141 | |
| SCS161_1 | Multi-function serial ch.16 chip select 1 output pin (1) | - | - | 140 | |
| SCS170_1 | Multi-function serial ch.17 chip select 0 I/O pin (1) | - | - | 15 | |
| SCS171_1 | Multi-function serial ch.17 chip select 1 output pin (1) | 12 | 12 | 18 | |
| SCS80_2 | Multi-function serial ch.8 chip select 0 I/O pin (2) | 50 | 58 | 66 | |
| SCS90_2 | Multi-function serial ch.9 chip select 0 I/O pin (2) | 41 | 49 | 57 | |
| SCS91_2 | Multi-function serial ch.9 chip select 1 output pin (2) | 42 | 50 | 58 | |
| SCK0_0 | Multi-function serial ch.0 clock I/O pin (0) | 62 | 74 | 86 | |
| SCK1_0 | Multi-function serial ch.1 clock I/O pin (0) | 4 | 4 | 4 | |
| SCK2_0 | Multi-function serial ch.2 clock I/O pin (0) | 39 | 47 | 55 | |
| SCK3_0 | Multi-function serial ch.3 clock I/O pin (0) | 49 | 57 | 65 | |
| SCK4_0 | Multi-function serial ch.4 clock I/O pin (0) | 138 | 170 | 202 | |
| SCK8_0 | Multi-function serial ch.8 clock I/O pin (0) | 103 | 127 | 151 | |
| SCK9_0 | Multi-function serial ch.9 clock I/O pin (0) | 107 | 131 | 155 | |
| SCK10_0 | Multi-function serial ch.10 clock I/O pin (0) | 114 | 138 | 164 | |
| SCK11_0 | Multi-function serial ch.11 clock I/O pin (0) | 120 | 144 | 171 | |
| SCK12_0 | Multi-function serial ch.12 clock I/O pin (0) | 125 | 149 | 178 | |
| SCK16_0 | Multi-function serial ch.16 clock I/O pin (0) | 67 | 83 | 95 | |
| SCK17_0 | Multi-function serial ch.17 clock I/O pin (0) | 88 | 112 | 129 | |
| SCK0_1 | Multi-function serial ch.0 clock I/O pin (1) | 8 | 8 | 11 | |
| SCK1_1 | Multi-function serial ch.1 clock I/O pin (1) | - | 20 | 26 | |
| SCK2_1 | Multi-function serial ch.2 clock I/O pin (1) | - | - | 185 | |
| SCK3_1 | Multi-function serial ch.3 clock I/O pin (1) | - | 163 | 195 | |
| SCK4_1 | Multi-function serial ch.4 clock I/O pin (1) | 19 | 26 | 34 | |
| SCK8_1 | Multi-function serial ch.8 clock I/O pin (1) | - | 70 | 82 | |
| SCK9_1 | Multi-function serial ch.9 clock I/O pin (1) | - | 106 | 123 | |
| SCK10_1 | Multi-function serial ch.10 clock I/O pin (1) | - | 76 | 88 | |
| SCK12_1 | Multi-function serial ch.12 clock I/O pin (1) | 88 | 112 | 129 | |
| SCK16_1 | Multi-function serial ch.16 clock I/O pin (1) | - | - | 138 | |
| SCK17_1 | Multi-function serial ch.17 clock I/O pin (1) | - | - | 16 | |
| SCK8_2 | Multi-function serial ch.8 clock I/O pin (2) | 48 | 56 | 64 | |
| SCK9_2 | Multi-function serial ch.9 clock I/O pin (2) | 40 | 48 | 56 | |
| SIN0_0 | Multi-function serial ch.0 serial data input pin (0) | 61 | 73 | 85 | |
| SIN1_0 | Multi-function serial ch.1 serial data input pin (0) | 3 | 3 | 3 | |
| SIN2_0 | Multi-function serial ch.2 serial data input pin (0) | 38 | 46 | 54 | |
| SIN3_0 | Multi-function serial ch.3 serial data input pin (0) | 48 | 56 | 64 | |
| SIN4_0 | Multi-function serial ch.4 serial data input pin (0) | 137 | 169 | 201 | |
| SIN8_0 | Multi-function serial ch.8 serial data input pin (0) | 102 | 126 | 150 | |
| SIN9_0 | Multi-function serial ch.9 serial data input pin (0) | 106 | 130 | 154 | |
| SIN10_0 | Multi-function serial ch.10 serial data input pin (0) | 113 | 137 | 162 | |
| SIN11_0 | Multi-function serial ch.11 serial data input pin (0) | 117 | 141 | 168 | |
| SIN12_0 | Multi-function serial ch.12 serial data input pin (0) | 124 | 148 | 177 | |
| SIN16_0 | Multi-function serial ch.16 serial data input pin (0) | 66 | 82 | 94 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| SIN17_0 | Multi-function serial ch.17 serial data input pin (0) | 87 | 111 | 128 | |
| SIN0_1 | Multi-function serial ch.0 serial data input pin (1) | 6 | 6 | 9 | |
| SIN1_1 | Multi-function serial ch.1 serial data input pin (1) | - | 19 | 25 | |
| SIN2_1 | Multi-function serial ch.2 serial data input pin (1) | - | - | 184 | |
| SIN3_1 | Multi-function serial ch.3 serial data input pin (1) | - | 162 | 194 | |
| SIN4_1 | Multi-function serial ch.4 serial data input pin (1) | - | 24 | 32 | |
| SIN8_1 | Multi-function serial ch.8 serial data input pin (1) | - | 69 | 81 | |
| SIN9_1 | Multi-function serial ch.9 serial data input pin (1) | - | 105 | 122 | |
| SIN10_1 | Multi-function serial ch.10 serial data input pin (1) | - | 75 | 87 | |
| SIN12_1 | Multi-function serial ch.12 serial data input pin (1) | - | - | 131 | |
| SIN16_1 | Multi-function serial ch.16 serial data input pin (1) | - | - | 136 | |
| SIN17_1 | Multi-function serial ch.17 serial data input pin (1) | 11 | 11 | 14 | |
| SIN8_2 | Multi-function serial ch.8 serial data input pin (2) | 47 | 55 | 63 | |
| SIN9_2 | Multi-function serial ch.9 serial data input pin (2) | 38 | 46 | 54 | |
| SOT0_0 | Multi-function serial ch.0 serial data output pin (0) | 63 | 77 | 89 | |
| SOT1_0 | Multi-function serial ch.1 serial data output pin (0) | 5 | 5 | 5 | |
| SOT2_0 | Multi-function serial ch.2 serial data output pin (0) | 40 | 48 | 56 | |
| SOT3_0 | Multi-function serial ch.3 serial data output pin (0) | 50 | 58 | 66 | |
| SOT4_0 | Multi-function serial ch.4 serial data output pin (0) | 139 | 171 | 203 | |
| SOT8_0 | Multi-function serial ch.8 serial data output pin (0) | 104 | 128 | 152 | |
| SOT9_0 | Multi-function serial ch.9 serial data output pin (0) | 110 | 134 | 158 | |
| SOT10_0 | Multi-function serial ch.10 serial data output pin (0) | 115 | 139 | 165 | |
| SOT11_0 | Multi-function serial ch.11 serial data output pin (0) | 121 | 145 | 173 | |
| SOT12_0 | Multi-function serial ch.12 serial data output pin (0) | 126 | 150 | 179 | |
| SOT16_0 | Multi-function serial ch.16 serial data output pin (0) | 68 | 84 | 98 | |
| SOT17_0 | Multi-function serial ch.17 serial data output pin (0) | 93 | 117 | 139 | |
| SOT0_1 | Multi-function serial ch.0 serial data output pin (1) | 7 | 7 | 10 | |
| SOT1_1 | Multi-function serial ch.1 serial data output pin (1) | - | 21 | 27 | |
| SOT2_1 | Multi-function serial ch.2 serial data output pin (1) | - | 154 | 186 | |
| SOT3_1 | Multi-function serial ch.3 serial data output pin (1) | - | 164 | 196 | |
| SOT4_1 | Multi-function serial ch.4 serial data output pin (1) | - | 25 | 33 | |
| SOT8_1 | Multi-function serial ch.8 serial data output pin (1) | - | 71 | 83 | |
| SOT9_1 | Multi-function serial ch.9 serial data output pin (1) | - | 107 | 124 | |
| SOT10_1 | Multi-function serial ch.10 serial data output pin (1) | - | 79 | 91 | |
| SOT12_1 | Multi-function serial ch.12 serial data output pin (1) | - | - | 130 | |
| SOT16_1 | Multi-function serial ch.16 serial data output pin (1) | - | - | 137 | |
| SOT17_1 | Multi-function serial ch.17 serial data output pin (1) | - | - | 17 | |
| SOT8_2 | Multi-function serial ch.8 serial data output pin (2) | 49 | 57 | 65 | |
| SOT9_2 | Multi-function serial ch.9 serial data output pin (2) | 39 | 47 | 55 | |
| SCL0 | $I^2C$ ch.0 clock I/O pin | 62 | 74 | 86 | |
| SCL1 | $I^2C$ ch.1 clock I/O pin | 4 | 4 | 4 | |
| SCL4 | $I^2C$ ch.4 clock I/O pin | 138 | 170 | 202 | |
| SCL8 | $I^2C$ ch.8 clock I/O pin | 103 | 127 | 151 | |
| SCL9 | $I^2C$ ch.9 clock I/O pin | 107 | 131 | 155 | |
| SCL10 | $I^2C$ ch.10 clock I/O pin | 114 | 138 | 164 | |
| SCL11 | $I^2C$ ch.11 clock I/O pin | 120 | 144 | 171 | |
| SCL12 | $I^2C$ ch.12 clock I/O pin | 125 | 149 | 178 | |
| SCL16 | $I^2C$ ch.16 clock I/O pin | 67 | 83 | 95 | |
| SCL17 | $I^2C$ ch.17 clock I/O pin | 88 | 112 | 129 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| SDA0 | I²C ch.0 serial data I/O pin | 63 | 77 | 89 | |
| SDA1 | I²C ch.1 serial data I/O pin | 5 | 5 | 5 | |
| SDA4 | I²C ch.4 serial data I/O pin | 139 | 171 | 203 | |
| SDA8 | I²C ch.8 serial data I/O pin | 104 | 128 | 152 | |
| SDA9 | I²C ch.9 serial data I/O pin | 110 | 134 | 158 | |
| SDA10 | I²C ch.10 serial data I/O pin | 115 | 139 | 165 | |
| SDA11 | I²C ch.11 serial data I/O pin | 121 | 145 | 173 | |
| SDA12 | I²C ch.12 serial data I/O pin | 126 | 150 | 179 | |
| SDA16 | I²C ch.16 serial data I/O pin | 68 | 84 | 98 | |
| SDA17 | I²C ch.17 serial data I/O pin | 93 | 117 | 139 | |
| PPG0_TOUT0_0 | Base timer 0 output pin (0) | 61 | 73 | 85 | |
| PPG0_TOUT2_0 | Base timer 1 output pin (0) | 62 | 74 | 86 | |
| PPG1_TOUT0_0 | Base timer 2 output pin (0) | 63 | 77 | 89 | |
| PPG1_TOUT2_0 | Base timer 3 output pin (0) | 64 | 78 | 90 | |
| PPG2_TOUT0_0 | Base timer 4 output pin (0) | 65 | 81 | 93 | |
| PPG2_TOUT2_0 | Base timer 5 output pin (0) | 66 | 82 | 94 | |
| PPG3_TOUT0_0 | Base timer 6 output pin (0) | 67 | 83 | 95 | |
| PPG3_TOUT2_0 | Base timer 7 output pin (0) | 68 | 84 | 98 | |
| PPG4_TOUT0_0 | Base timer 8 output pin (0) | 70 | 86 | 102 | |
| PPG4_TOUT2_0 | Base timer 9 output pin (0) | 71 | 87 | 103 | |
| PPG5_TOUT0_0 | Base timer 10 output pin (0) | 87 | 111 | 128 | |
| PPG5_TOUT2_0 | Base timer 11 output pin (0) | 88 | 112 | 129 | |
| PPG6_TOUT0_0 | Base timer 12 output pin (0) | 100 | 124 | 148 | |
| PPG6_TOUT2_0 | Base timer 13 output pin (0) | 101 | 125 | 149 | |
| PPG7_TOUT0_0 | Base timer 14 output pin (0) | 102 | 126 | 150 | |
| PPG7_TOUT2_0 | Base timer 15 output pin (0) | 103 | 127 | 151 | |
| PPG8_TOUT0_0 | Base timer 16 output pin (0) | 104 | 128 | 152 | |
| PPG8_TOUT2_0 | Base timer 17 output pin (0) | 105 | 129 | 153 | |
| PPG9_TOUT0_0 | Base timer 18 output pin (0) | 106 | 130 | 154 | |
| PPG9_TOUT2_0 | Base timer 19 output pin (0) | 107 | 131 | 155 | |
| PPG10_TOUT0_0 | Base timer 20 output pin (0) | 110 | 134 | 158 | |
| PPG10_TOUT2_0 | Base timer 21 output pin (0) | 111 | 135 | 160 | |
| PPG11_TOUT0_0 | Base timer 22 output pin (0) | 112 | 136 | 161 | |
| PPG11_TOUT2_0 | Base timer 23 output pin (0) | 113 | 137 | 162 | |
| PPG12_TOUT0_0 | Base timer 24 output pin (0) | 115 | 139 | 165 | |
| PPG12_TOUT2_0 | Base timer 25 output pin (0) | 116 | 140 | 166 | |
| PPG13_TOUT0_0 | Base timer 26 output pin (0) | 117 | 141 | 168 | |
| PPG13_TOUT2_0 | Base timer 27 output pin (0) | 120 | 144 | 171 | |
| PPG14_TOUT0_0 | Base timer 28 output pin (0) | 121 | 145 | 173 | |
| PPG14_TOUT2_0 | Base timer 29 output pin (0) | 122 | 146 | 174 | |
| PPG15_TOUT0_0 | Base timer 30 output pin (0) | 123 | 147 | 175 | |
| PPG15_TOUT2_0 | Base timer 31 output pin (0) | 124 | 148 | 177 | |
| PPG0_TOUT0_1 | Base timer 0 output pin (1) | 8 | 8 | 11 | |
| PPG0_TOUT2_1 | Base timer 1 output pin (1) | 9 | 9 | 12 | |
| PPG1_TOUT0_1 | Base timer 2 output pin (1) | 10 | 10 | 13 | |
| PPG1_TOUT2_1 | Base timer 3 output pin (1) | 11 | 11 | 14 | |
| PPG2_TOUT0_1 | Base timer 4 output pin (1) | 12 | 12 | 18 | |
| PPG2_TOUT2_1 | Base timer 5 output pin (1) | 13 | 13 | 19 | |
| PPG3_TOUT0_1 | Base timer 6 output pin (1) | 14 | 14 | 20 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| PPG3_TOUT2_1 | Base timer 7 output pin (1) | 15 | 15 | 21 | |
| PPG4_TOUT0_1 | Base timer 8 output pin (1) | - | 19 | 25 | |
| PPG4_TOUT2_1 | Base timer 9 output pin (1) | - | 20 | 26 | |
| PPG5_TOUT0_1 | Base timer 10 output pin (1) | - | 21 | 27 | |
| PPG5_TOUT2_1 | Base timer 11 output pin (1) | - | 22 | 28 | |
| PPG6_TOUT0_1 | Base timer 12 output pin (1) | - | 69 | 81 | |
| PPG6_TOUT2_1 | Base timer 13 output pin (1) | - | 70 | 82 | |
| PPG7_TOUT0_1 | Base timer 14 output pin (1) | - | 71 | 83 | |
| PPG7_TOUT2_1 | Base timer 15 output pin (1) | - | 72 | 84 | |
| PPG8_TOUT0_1 | Base timer 16 output pin (1) | - | 75 | 87 | |
| PPG8_TOUT2_1 | Base timer 17 output pin (1) | - | 76 | 88 | |
| PPG9_TOUT0_1 | Base timer 18 output pin (1) | - | 79 | 91 | |
| PPG9_TOUT2_1 | Base timer 19 output pin (1) | - | 80 | 92 | |
| PPG10_TOUT0_1 | Base timer 20 output pin (1) | - | 98 | 114 | |
| PPG10_TOUT2_1 | Base timer 21 output pin (1) | - | 99 | 115 | |
| PPG11_TOUT0_1 | Base timer 22 output pin (1) | - | 105 | 122 | |
| PPG11_TOUT2_1 | Base timer 23 output pin (1) | - | 106 | 123 | |
| PPG12_TOUT0_1 | Base timer 24 output pin (1) | - | 154 | 186 | |
| PPG12_TOUT2_1 | Base timer 25 output pin (1) | - | 155 | 187 | |
| PPG13_TOUT0_1 | Base timer 26 output pin (1) | - | 156 | 188 | |
| PPG13_TOUT2_1 | Base timer 27 output pin (1) | - | 157 | 189 | |
| PPG14_TOUT0_1 | Base timer 28 output pin (1) | 130 | 158 | 190 | |
| PPG14_TOUT2_1 | Base timer 29 output pin (1) | - | 162 | 194 | |
| PPG15_TOUT0_1 | Base timer 30 output pin (1) | - | 163 | 195 | |
| PPG15_TOUT2_1 | Base timer 31 output pin (1) | - | 164 | 196 | |
| PPG0/1/2/3/4/5_TIN1_0 | Base timer 0/2/4/6/8/10 input pin (0) | 93 | 117 | 139 | |
| PPG6/7/8/9/10/11_TIN1_0 | Base timer 12/14/16/18/20/22 input pin (0) | 114 | 138 | 164 | |
| PPG12/13/14/15_TIN1_0 | Base timer 24/26/28/30 input pin (0) | 125 | 149 | 178 | |
| PPG0/1/2/3/4/5_TIN1_1 | Base timer 0/2/4/6/8/10 input pin (1) | - | 23 | 29 | |
| PPG6/7/8/9/10/11_TIN1_1 | Base timer 12/14/16/18/20/22 input pin (1) | - | 107 | 124 | |
| PPG12/13/14/15_TIN1_1 | Base timer 24/26/28/30 input pin (1) | - | 165 | 197 | |
| WOT | RTC overflow output pin | 93 | 117 | 139 | |
| PWM1M0 | SMC ch.0 output pin | 101 | 125 | 149 | |
| PWM1M1 | SMC ch.1 output pin | 105 | 129 | 153 | |
| PWM1M2 | SMC ch.2 output pin | 111 | 135 | 160 | |
| PWM1M3 | SMC ch.3 output pin | 115 | 139 | 165 | |
| PWM1M4 | SMC ch.4 output pin | 121 | 145 | 173 | |
| PWM1M5 | SMC ch.5 output pin | 125 | 149 | 178 | |
| PWM1P0 | SMC ch.0 output pin | 100 | 124 | 148 | |
| PWM1P1 | SMC ch.1 output pin | 104 | 128 | 152 | |
| PWM1P2 | SMC ch.2 output pin | 110 | 134 | 158 | |
| PWM1P3 | SMC ch.3 output pin | 114 | 138 | 164 | |
| PWM1P4 | SMC ch.4 output pin | 120 | 144 | 171 | |
| PWM1P5 | SMC ch.5 output pin | 124 | 148 | 177 | |
| PWM2M0 | SMC ch.0 output pin | 103 | 127 | 151 | |
| PWM2M1 | SMC ch.1 output pin | 107 | 131 | 155 | |
| PWM2M2 | SMC ch.2 output pin | 113 | 137 | 162 | |
| PWM2M3 | SMC ch.3 output pin | 117 | 141 | 168 | |
| PWM2M4 | SMC ch.4 output pin | 123 | 147 | 175 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| PWM2M5 | SMC ch.5 output pin | 127 | 151 | 181 | |
| PWM2P0 | SMC ch.0 output pin | 102 | 126 | 150 | |
| PWM2P1 | SMC ch.1 output pin | 106 | 130 | 154 | |
| PWM2P2 | SMC ch.2 output pin | 112 | 136 | 161 | |
| PWM2P3 | SMC ch.3 output pin | 116 | 140 | 166 | |
| PWM2P4 | SMC ch.4 output pin | 122 | 146 | 174 | |
| PWM2P5 | SMC ch.5 output pin | 126 | 150 | 179 | |
| OCU0_OTD0_0 | Output compare 0 ch.0 output pin (0) | 61 | 73 | 85 | |
| OCU0_OTD1_0 | Output compare 0 ch.1 output pin (0) | 62 | 74 | 86 | |
| OCU1_OTD0_0 | Output compare 1 ch.0 output pin (0) | 65 | 81 | 93 | |
| OCU1_OTD1_0 | Output compare 1 ch.1 output pin (0) | 66 | 82 | 94 | |
| OCU2_OTD0_0 | Output compare 2 ch.0 output pin (0) | 67 | 83 | 95 | |
| OCU2_OTD1_0 | Output compare 2 ch.1 output pin (0) | 68 | 84 | 98 | |
| OCU8_OTD0_0 | Output compare 8 ch.0 output pin (0) | 70 | 86 | 102 | |
| OCU8_OTD1_0 | Output compare 8 ch.1 output pin (0) | 71 | 87 | 103 | |
| OCU9_OTD0_0 | Output compare 9 ch.0 output pin (0) | 81 | 97 | 113 | |
| OCU9_OTD1_0 | Output compare 9 ch.1 output pin (0) | 87 | 111 | 128 | |
| OCU10_OTD0_0 | Output compare 10 ch.0 output pin (0) | 88 | 112 | 129 | |
| OCU10_OTD1_0 | Output compare 10 ch.1 output pin (0) | 93 | 117 | 139 | |
| OCU0_OTD0_1 | Output compare 0 ch.0 output pin (1) | - | 69 | 81 | |
| OCU0_OTD1_1 | Output compare 0 ch.1 output pin (1) | - | 70 | 82 | |
| OCU1_OTD0_1 | Output compare 1 ch.0 output pin (1) | - | 71 | 83 | |
| OCU1_OTD1_1 | Output compare 1 ch.1 output pin (1) | - | 72 | 84 | |
| OCU2_OTD0_1 | Output compare 2 ch.0 output pin (1) | - | 75 | 87 | |
| OCU2_OTD1_1 | Output compare 2 ch.1 output pin (1) | - | 76 | 88 | |
| OCU8_OTD0_1 | Output compare 8 ch.0 output pin (1) | - | 79 | 91 | |
| OCU8_OTD1_1 | Output compare 8 ch.1 output pin (1) | - | 80 | 92 | |
| OCU9_OTD0_1 | Output compare 9 ch.0 output pin (1) | - | 98 | 114 | |
| OCU9_OTD1_1 | Output compare 9 ch.1 output pin (1) | - | 99 | 115 | |
| OCU10_OTD0_1 | Output compare 10 ch.0 output pin (1) | - | 105 | 122 | |
| OCU10_OTD1_1 | Output compare 10 ch.1 output pin (1) | - | 106 | 123 | |
| ICU0_IN0_0 | Input Capture 0 ch.0 input pin (0) | 61 | 73 | 85 | |
| ICU0_IN1_0 | Input Capture 0 ch.1 input pin (0) | 62 | 74 | 86 | |
| ICU1_IN0_0 | Input Capture 1 ch.0 input pin (0) | 63 | 77 | 89 | |
| ICU1_IN1_0 | Input Capture 1 ch.1 input pin (0) | 64 | 78 | 90 | |
| ICU2_IN0_0 | Input Capture 2 ch.0 input pin (0) | 65 | 81 | 93 | |
| ICU2_IN1_0 | Input Capture 2 ch.1 input pin (0) | 66 | 82 | 94 | |
| ICU8_IN0_0 | Input Capture 8 ch.0 input pin (0) | 67 | 83 | 95 | |
| ICU8_IN1_0 | Input Capture 8 ch.1 input pin (0) | 68 | 84 | 98 | |
| ICU9_IN0_0 | Input Capture 9 ch.0 input pin (0) | 70 | 86 | 102 | |
| ICU9_IN1_0 | Input Capture 9 ch.1 input pin (0) | 71 | 87 | 103 | |
| ICU10_IN0_0 | Input Capture 10 ch.0 input pin (0) | 87 | 111 | 128 | |
| ICU10_IN1_0 | Input Capture 10 ch.1 input pin (0) | 88 | 112 | 129 | |
| ICU0_IN0_1 | Input Capture 0 ch.0 input pin (1) | - | 69 | 81 | |
| ICU0_IN1_1 | Input Capture 0 ch.1 input pin (1) | - | 70 | 82 | |
| ICU1_IN0_1 | Input Capture 1 ch.0 input pin (1) | - | 71 | 83 | |
| ICU1_IN1_1 | Input Capture 1 ch.1 input pin (1) | - | 72 | 84 | |
| ICU2_IN0_1 | Input Capture 2 ch.0 input pin (1) | - | 75 | 87 | |
| ICU2_IN1_1 | Input Capture 2 ch.1 input pin (1) | - | 76 | 88 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| ICU8_IN0_1 | Input Capture 8 ch.0 input pin (1) | - | 79 | 91 | |
| ICU8_IN1_1 | Input Capture 8 ch.1 input pin (1) | - | 80 | 92 | |
| ICU9_IN0_1 | Input Capture 9 ch.0 input pin (1) | - | 98 | 114 | |
| ICU9_IN1_1 | Input Capture 9 ch.1 input pin (1) | - | 99 | 115 | |
| ICU10_IN0_1 | Input Capture 10 ch.0 input pin (1) | - | 105 | 122 | |
| ICU10_IN1_1 | Input Capture 10 ch.1 input pin (1) | - | 106 | 123 | |
| SGA0_0 | Sound generator ch.0 SGA output pin (0) | 63 | 77 | 89 | |
| SGA1_0 | Sound generator ch.1 SGA output pin (0) | 65 | 81 | 93 | |
| SGA2_0 | Sound generator ch.2 SGA output pin (0) | 67 | 83 | 95 | |
| SGA3_0 | Sound generator ch.3 SGA output pin (0) | 81 | 97 | 113 | |
| SGA4_0 | Sound generator ch.4 SGA output pin (0) | 88 | 112 | 129 | |
| SGA0_1 | Sound generator ch.0 SGA output pin (1) | - | 69 | 81 | |
| SGA1_1 | Sound generator ch.1 SGA output pin (1) | - | 71 | 83 | |
| SGA2_1 | Sound generator ch.2 SGA output pin (1) | - | 75 | 87 | |
| SGA3_1 | Sound generator ch.3 SGA output pin (1) | - | 79 | 91 | |
| SGA4_1 | Sound generator ch.4 SGA output pin (1) | - | 98 | 114 | |
| SGO0_0 | Sound generator ch.0 SGO output pin (0) | 64 | 78 | 90 | |
| SGO1_0 | Sound generator ch.1 SGO output pin (0) | 66 | 82 | 94 | |
| SGO2_0 | Sound generator ch.2 SGO output pin (0) | 68 | 84 | 98 | |
| SGO3_0 | Sound generator ch.3 SGO output pin (0) | 87 | 111 | 128 | |
| SGO4_0 | Sound generator ch.4 SGO output pin (0) | 93 | 117 | 139 | |
| SGO0_1 | Sound generator ch.0 SGO output pin (1) | - | 70 | 82 | |
| SGO1_1 | Sound generator ch.1 SGO output pin (1) | - | 72 | 84 | |
| SGO2_1 | Sound generator ch.2 SGO output pin (1) | - | 76 | 88 | |
| SGO3_1 | Sound generator ch.3 SGO output pin (1) | - | 80 | 92 | |
| SGO4_1 | Sound generator ch.4 SGO output pin (1) | - | 99 | 115 | |
| AN0 (AL0) | PCM PWM ch.0 output pin | 63 | 77 | 89 | |
| AN1 (AL1) | PCM PWM ch.1 output pin | 67 | 83 | 95 | |
| AP0 (AH0) | PCM PWM ch.0 output pin | 64 | 78 | 90 | |
| AP1 (AH1) | PCM PWM ch.1 output pin | 68 | 84 | 98 | |
| BN0 (BL0) | PCM PWM ch.0 output pin | 61 | 73 | 85 | |
| BN1 (BL1) | PCM PWM ch.1 output pin | 65 | 81 | 93 | |
| BP0 (BH0) | PCM PWM ch.0 output pin | 62 | 74 | 86 | |
| BP1 (BH1) | PCM PWM ch.1 output pin | 66 | 82 | 94 | |
| I2S0_ECLK_0 | I2S external clock ch.0 input pin (0) | 12 | 12 | 18 | |
| I2S0_ECLK_1 | I2S external clock ch.0 input pin (1) | - | 154 | 186 | |
| I2S1_ECLK_0 | I2S external clock ch.1 input pin (0) | 8 | 8 | 11 | |
| I2S0_SCK_0 | I2S continuous serial clock ch.0 I/O pin (0) | 15 | 15 | 21 | |
| I2S0_SCK_1 | I2S continuous serial clock ch.0 I/O pin (1) | - | 157 | 189 | |
| I2S1_SCK_0 | I2S continuous serial clock ch.1 I/O pin (0) | 11 | 11 | 14 | |
| I2S0_SD_0 | I2S serial data ch.0 I/O pin (0) | 13 | 13 | 19 | |
| I2S0_SD_1 | I2S serial data ch.0 I/O pin (1) | - | 155 | 187 | |
| I2S1_SD_0 | I2S serial data ch.1 I/O pin (0) | 9 | 9 | 12 | |
| I2S0_WS_0 | I2S word select ch.0 I/O pin (0) | 14 | 14 | 20 | |
| I2S0_WS_1 | I2S word select ch.0 I/O pin (1) | - | 156 | 188 | |
| I2S1_WS_0 | I2S word select ch.1 I/O pin (0) | 10 | 10 | 13 | |
| C_L | Audio DAC external capacity connection output pin (L) | 34 | 42 | 50 | |
| C_R | Audio DAC external capacity connection output pin (R) | 30 | 38 | 46 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| DAC_L | Audio DAC output pin (L) | 33 | 41 | 49 | |
| DAC_R | Audio DAC output pin (R) | 29 | 37 | 45 | |
| FRT0/1/2/3_TEXT | Free-run timer ch.0/1/2/3 clock input pin | 61 | 73 | 85 | |
| FRT4/8/9/10_TEXT | Free-run timer ch.4/8/9/10 clock input pin | 62 | 74 | 86 | |
| TIN0_0 | Reload timer ch.0 event input pin (0) | 61 | 73 | 85 | |
| TIN1_0 | Reload timer ch.1 event input pin (0) | 63 | 77 | 89 | |
| TIN16_0 | Reload timer ch.16 event input pin (0) | 65 | 81 | 93 | |
| TIN17_0 | Reload timer ch.17 event input pin (0) | 70 | 86 | 102 | |
| TIN48_0 | Reload timer ch.48 event input pin (0) | 81 | 97 | 113 | |
| TIN49_0 | Reload timer ch.49 event input pin (0) | 88 | 112 | 129 | |
| TIN0_1 | Reload timer ch.0 event input pin (0) | - | 69 | 81 | |
| TIN1_1 | Reload timer ch.1 event input pin (1) | - | 71 | 83 | |
| TIN16_1 | Reload timer ch.16 event input pin (1) | - | 75 | 87 | |
| TIN17_1 | Reload timer ch.17 event input pin (1) | - | 79 | 91 | |
| TIN48_1 | Reload timer ch.48 event input pin (1) | - | 98 | 114 | |
| TIN49_1 | Reload timer ch.49 event input pin (1) | - | 107 | 124 | |
| TOT0_0 | Reload timer ch.0 output pin (0) | 62 | 74 | 86 | |
| TOT1_0 | Reload timer ch.1 output pin (0) | 64 | 78 | 90 | |
| TOT16_0 | Reload timer ch.16 output pin (0) | 66 | 82 | 94 | |
| TOT17_0 | Reload timer ch.17 output pin (0) | 71 | 87 | 103 | |
| TOT48_0 | Reload timer ch.48 output pin (0) | 87 | 111 | 128 | |
| TOT49_0 | Reload timer ch.49 output pin (0) | 93 | 117 | 139 | |
| TOT0_1 | Reload timer ch.0 output pin (1) | - | 70 | 82 | |
| TOT1_1 | Reload timer ch.1 output pin (1) | - | 72 | 84 | |
| TOT16_1 | Reload timer ch.16 output pin (1) | - | 76 | 88 | |
| TOT17_1 | Reload timer ch.17 output pin (1) | - | 80 | 92 | |
| TOT48_1 | Reload timer ch.48 output pin (1) | - | 99 | 115 | |
| TOT49_1 | Reload timer ch.49 output pin (1) | - | 108 | 125 | |
| AIN8 | Up/Down counter AIN input pin ch.8 | 61 | 73 | 85 | |
| AIN9 | Up/Down counter AIN input pin ch.9 | 64 | 78 | 90 | |
| BIN8 | Up/Down counter BIN input pin ch.8 | 62 | 74 | 86 | |
| BIN9 | Up/Down counter BIN input pin ch.9 | 65 | 81 | 93 | |
| ZIN8 | Up/Down counter ZIN input pin ch.8 | 63 | 77 | 89 | |
| ZIN9 | Up/Down counter ZIN input pin ch.9 | 66 | 82 | 94 | |
| RXD0_0 | Ethernet pin (0) | 47 | 55 | 63 | |
| RXD1_0 | Ethernet pin (0) | 48 | 56 | 64 | |
| RXD2_0 | Ethernet pin (0) | 49 | 57 | 65 | |
| RXD3_0 | Ethernet pin (0) | 50 | 58 | 66 | |
| TXD0_0 | Ethernet pin (0) | 39 | 47 | 55 | |
| TXD1_0 | Ethernet pin (0) | 40 | 48 | 56 | |
| TXD2_0 | Ethernet pin (0) | 41 | 49 | 57 | |
| TXD3_0 | Ethernet pin (0) | 42 | 50 | 58 | |
| COL_0 | Ethernet pin (0) | 55 | 63 | 71 | |
| CRS_0 | Ethernet pin (0) | 56 | 64 | 72 | |
| RXER_0 | Ethernet pin (0) | 23 | 31 | 39 | |
| RXDV_0 | Ethernet pin (0) | 24 | 32 | 40 | |
| RXCLK_0 | Ethernet pin (0) | 22 | 30 | 38 | |
| TXER_0 | Ethernet pin (0) | 44 | 52 | 60 | |
| TXEN_0 | Ethernet pin (0) | 38 | 46 | 54 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| TXCLK_0 | Ethernet pin (0) | 25 | 33 | 41 | |
| MDC_0 | Ethernet pin (0) | 54 | 62 | 70 | |
| MDIO_0 | Ethernet pin (0) | 51 | 59 | 67 | |
| RXD0_1 | Ethernet pin (1) | - | 23 | 29 | |
| RXD1_1 | Ethernet pin (1) | - | - | 30 | |
| RXD2_1 | Ethernet pin (1) | - | - | 31 | |
| RXD3_1 | Ethernet pin (1) | - | 24 | 32 | |
| TXD0_1 | Ethernet pin (1) | - | - | 17 | |
| TXD1_1 | Ethernet pin (1) | - | 19 | 25 | |
| TXD2_1 | Ethernet pin (1) | - | 20 | 26 | |
| TXD3_1 | Ethernet pin (1) | - | 21 | 27 | |
| COL_1 | Ethernet pin (1) | 24 | 32 | 40 | |
| CRS_1 | Ethernet pin (1) | 25 | 33 | 41 | |
| RXER_1 | Ethernet pin (1) | - | - | 7 | |
| RXDV_1 | Ethernet pin (1) | - | - | 8 | |
| RXCLK_1 | Ethernet pin (1) | - | - | 6 | |
| TXER_1 | Ethernet pin (1) | - | 22 | 28 | |
| TXEN_1 | Ethernet pin (1) | - | - | 16 | |
| TXCLK_1 | Ethernet pin (1) | - | - | 15 | |
| MDC_1 | Ethernet pin (1) | 23 | 31 | 39 | |
| MDIO_1 | Ethernet pin (1) | - | 25 | 33 | |
| MLBCLK | MediaLB pin | 54 | 62 | 70 | |
| MLBDAT | MediaLB pin | 56 | 64 | 72 | |
| MLBSIG | MediaLB pin | 55 | 63 | 71 | |
| M_SCLK0 | MCU HS-SPI clock output pin | 44 | 52 | 60 | |
| M_SDATA0_0 | MCU HS-SPI0 data 0 I/O pin | 38 | 46 | 54 | |
| M_SDATA0_1 | MCU HS-SPI0 data 1 I/O pin | 40 | 48 | 56 | |
| M_SDATA0_2 | MCU HS-SPI0 data 2 I/O pin | 39 | 47 | 55 | |
| M_SDATA0_3 | MCU HS-SPI0 data 3 I/O pin | 42 | 50 | 58 | |
| M_SDATA1_0 | MCU HS-SPI1 data 0 I/O pin | 47 | 55 | 63 | |
| M_SDATA1_1 | MCU HS-SPI1 data 1 I/O pin | 49 | 57 | 65 | |
| M_SDATA1_2 | MCU HS-SPI1 data 2 I/O pin | 48 | 56 | 64 | |
| M_SDATA1_3 | MCU HS-SPI1 data 3 I/O pin | 51 | 59 | 67 | |
| M_SSEL0 | MCU HS-SPI0 select output pin | 41 | 49 | 57 | |
| M_SSEL1 | MCU HS-SPI1 select output pin | 50 | 58 | 66 | |
| M_CK | MCU Hyper Bus clock output pin | 44 | 52 | 60 | |
| M_CS#_1 | MCU Hyper Bus select 1 output pin | 42 | 50 | 58 | |
| M_CS#_2 | MCU Hyper Bus select 2 output pin | 54 | 62 | 70 | |
| M_DQ0 | MCU Hyper Bus Data 0 pin | 41 | 49 | 57 | |
| M_DQ1 | MCU Hyper Bus Data 1 pin | 40 | 48 | 56 | |
| M_DQ2 | MCU Hyper Bus Data 2 pin | 39 | 47 | 55 | |
| M_DQ3 | MCU Hyper Bus Data 3 pin | 38 | 46 | 54 | |
| M_DQ4 | MCU Hyper Bus Data 4 pin | 48 | 56 | 64 | |
| M_DQ5 | MCU Hyper Bus Data 5 pin | 49 | 57 | 65 | |
| M_DQ6 | MCU Hyper Bus Data 6 pin | 50 | 58 | 66 | |
| M_DQ7 | MCU Hyper Bus Data 7 pin | 51 | 59 | 67 | |
| M_RWDS | MCU Hyper Bus RWDS | 47 | 55 | 63 | |
| COM0 | LCDC Segment (Duty) Common Output Pin | 15 | 15 | 21 | |
| COM1 | LCDC Segment (Duty) Common Output Pin | 19 | 26 | 34 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| COM2 | LCDC Segment (Duty) Common Output Pin | 20 | 27 | 35 | |
| COM3 | LCDC Segment (Duty) Common Output Pin | 21 | 28 | 36 | |
| SEG0 | LCDC Segment (Duty) Output Pin | - | 154 | 186 | |
| SEG1 | LCDC Segment (Duty) Output Pin | - | 155 | 187 | |
| SEG2 | LCDC Segment (Duty) Output Pin | - | 156 | 188 | |
| SEG3 | LCDC Segment (Duty) Output Pin | - | 157 | 189 | |
| SEG4 | LCDC Segment (Duty) Output Pin | 130 | 158 | 190 | |
| SEG5 | LCDC Segment (Duty) Output Pin | - | 162 | 194 | |
| SEG6 | LCDC Segment (Duty) Output Pin | - | 163 | 195 | |
| SEG7 | LCDC Segment (Duty) Output Pin | - | 164 | 196 | |
| SEG8 | LCDC Segment (Duty) Output Pin | - | 165 | 197 | |
| SEG9 | LCDC Segment (Duty) Output Pin | 134 | 166 | 198 | |
| SEG10 | LCDC Segment (Duty) Output Pin | 135 | 167 | 199 | |
| SEG11 | LCDC Segment (Duty) Output Pin | 136 | 168 | 200 | |
| SEG12 | LCDC Segment (Duty) Output Pin | 137 | 169 | 201 | |
| SEG13 | LCDC Segment (Duty) Output Pin | 138 | 170 | 202 | |
| SEG14 | LCDC Segment (Duty) Output Pin | 139 | 171 | 203 | |
| SEG15 | LCDC Segment (Duty) Output Pin | 140 | 172 | 204 | |
| SEG16 | LCDC Segment (Duty) Output Pin | 141 | 173 | 205 | |
| SEG17 | LCDC Segment (Duty) Output Pin | 142 | 174 | 206 | |
| SEG18 | LCDC Segment (Duty) Output Pin | 143 | 175 | 207 | |
| SEG19 | LCDC Segment (Duty) Output Pin | 2 | 2 | 2 | |
| SEG20 | LCDC Segment (Duty) Output Pin | 3 | 3 | 3 | |
| SEG21 | LCDC Segment (Duty) Output Pin | 4 | 4 | 4 | |
| SEG22 | LCDC Segment (Duty) Output Pin | 5 | 5 | 5 | |
| SEG23 | LCDC Segment (Duty/Static) Output Pin | 6 | 6 | 9 | |
| SEG24 | LCDC Segment (Duty/Static) Output Pin | 7 | 7 | 10 | |
| SEG25 | LCDC Segment (Duty/Static) Output Pin | 8 | 8 | 11 | |
| SEG26 | LCDC Segment (Duty/Static) Output Pin | 9 | 9 | 12 | |
| SEG27 | LCDC Segment (Duty/Static) Output Pin | 10 | 10 | 13 | |
| SEG28 | LCDC Segment (Duty/Static) Output Pin | 11 | 11 | 14 | |
| SEG29 | LCDC Segment (Duty/Static) Output Pin | 12 | 12 | 18 | |
| SEG30 | LCDC Segment (Duty/Static) Output Pin | 13 | 13 | 19 | |
| SEG31 | LCDC Segment (Duty/Static) Output Pin | 14 | 14 | 20 | |
| V0 | LCDC Reference Voltage V0 Input Pin | 22 | 30 | 38 | |
| V1 | LCDC Reference Voltage V1 Input Pin | 23 | 31 | 39 | |
| V2 | LCDC Reference Voltage V2 Input Pin | 24 | 32 | 40 | |
| V3 | LCDC Reference Voltage V3 Input Pin | 25 | 33 | 41 | |
| DSP0_CLK_0 | Display 0 Clock output pin | 136 | 168 | 200 | |
| DSP0_EN_0 | Display 0 Data Enable output pin | 130 | 158 | 190 | |
| DSP0_VSYNC_0 | Display 0 Vertical Synchronization output pin | 135 | 167 | 199 | |
| DSP0_HSYNC_0 | Display 0 Horizontal Synchronization output pin | 134 | 166 | 198 | |
| DSP0_R0_0 | Display 0 RGB color output pin (0) | 137 | 169 | 201 | |
| DSP0_R1_0 | Display 0 RGB color output pin (0) | 138 | 170 | 202 | |
| DSP0_R2_0 | Display 0 RGB color output pin (0) | 139 | 171 | 203 | |
| DSP0_R3_0 | Display 0 RGB color output pin (0) | 140 | 172 | 204 | |
| DSP0_R4_0 | Display 0 RGB color output pin (0) | 141 | 173 | 205 | |
| DSP0_R5_0 | Display 0 RGB color output pin (0) | 142 | 174 | 206 | |
| DSP0_R6_0 | Display 0 RGB color output pin (0) | 143 | 175 | 207 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| DSP0_R7_0 | Display 0 RGB color output pin (0) | 2 | 2 | 2 | |
| DSP0_G0_0 | Display 0 RGB color output pin (0) | 3 | 3 | 3 | |
| DSP0_G1_0 | Display 0 RGB color output pin (0) | 4 | 4 | 4 | |
| DSP0_G2_0 | Display 0 RGB color output pin (0) | 5 | 5 | 5 | |
| DSP0_G3_0 | Display 0 RGB color output pin (0) | 6 | 6 | 9 | |
| DSP0_G4_0 | Display 0 RGB color output pin (0) | 7 | 7 | 10 | |
| DSP0_G5_0 | Display 0 RGB color output pin (0) | 8 | 8 | 11 | |
| DSP0_G6_0 | Display 0 RGB color output pin (0) | 9 | 9 | 12 | |
| DSP0_G7_0 | Display 0 RGB color output pin (0) | 10 | 10 | 13 | |
| DSP0_B0_0 | Display 0 RGB color output pin (0) | 11 | 11 | 14 | |
| DSP0_B1_0 | Display 0 RGB color output pin (0) | 12 | 12 | 18 | |
| DSP0_B2_0 | Display 0 RGB color output pin (0) | 13 | 13 | 19 | |
| DSP0_B3_0 | Display 0 RGB color output pin (0) | 14 | 14 | 20 | |
| DSP0_B4_0 | Display 0 RGB color output pin (0) | 15 | 15 | 21 | |
| DSP0_B5_0 | Display 0 RGB color output pin (0) | 19 | 26 | 34 | |
| DSP0_B6_0 | Display 0 RGB color output pin (0) | 20 | 27 | 35 | |
| DSP0_B7_0 | Display 0 RGB color output pin (0) | 22 | 30 | 38 | |
| DSP0_B7_1 | Display 0 RGB color output pin (1) | 21 | 28 | 36 | |
| LCDD0 | LCD Bus IF Data I/O pin | 139 | 171 | 203 | |
| LCDD1 | LCD Bus IF Data I/O pin | 140 | 172 | 204 | |
| LCDD2 | LCD Bus IF Data I/O pin | 141 | 173 | 205 | |
| LCDD3 | LCD Bus IF Data I/O pin | 142 | 174 | 206 | |
| LCDD4 | LCD Bus IF Data I/O pin | 143 | 175 | 207 | |
| LCDD5 | LCD Bus IF Data I/O pin | 2 | 2 | 2 | |
| LCDD6 | LCD Bus IF Data I/O pin | 3 | 3 | 3 | |
| LCDD7 | LCD Bus IF Data I/O pin | 4 | 4 | 4 | |
| LCDD8 | LCD Bus IF Data I/O pin | 5 | 5 | 5 | |
| LCDD9 | LCD Bus IF Data I/O pin | 6 | 6 | 9 | |
| LCDD10 | LCD Bus IF Data I/O pin | 7 | 7 | 10 | |
| LCDD11 | LCD Bus IF Data I/O pin | 8 | 8 | 11 | |
| LCDD12 | LCD Bus IF Data I/O pin | 9 | 9 | 12 | |
| LCDD13 | LCD Bus IF Data I/O pin | 10 | 10 | 13 | |
| LCDD14 | LCD Bus IF Data I/O pin | 11 | 11 | 14 | |
| LCDD15 | LCD Bus IF Data I/O pin | 12 | 12 | 18 | |
| LCDD16 | LCD Bus IF Data I/O pin | 13 | 13 | 19 | |
| LCDD17 | LCD Bus IF Data I/O pin | 14 | 14 | 20 | |
| CS# | LCD Bus IF Chip Select output pin | 15 | 15 | 21 | |
| WR# | LCD Bus IF Write enable output pin | 19 | 26 | 34 | |
| RD# | LCD Bus IF Read enable output pin | 20 | 27 | 35 | |
| RS | LCD Bus IF Register Select output pin | 23 | 31 | 39 | |
| TE | LCD Bus IF Tearing Effect input pin | 25 | 33 | 41 | |
| RES# | LCD Bus IF Reset Control output pin | 24 | 32 | 40 | |
| ARH0_AIC0_DNCLK | APIX output pin | 11 | 11 | 14 | |
| ARH0_AIC0_DNDATA0 | APIX output pin | 21 | 28 | 36 | |
| ARH0_AIC0_DNDATA1 | APIX output pin | 12 | 12 | 18 | |
| ARH0_AIC0_RCK | APIX input pin | 23 | 31 | 39 | |
| ARH0_AIC0_RDA0 | APIX input pin | 25 | 33 | 41 | |
| ARH0_AIC0_RDA1 | APIX input pin | 24 | 32 | 40 | |
| ARH0_AIC0_TCKI | APIX input pin | 11 | 11 | 14 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| ARH0_AIC0_TDA0 | APIX output pin | 21 | 28 | 36 | |
| ARH0_AIC0_TDA1 | APIX output pin | 12 | 12 | 18 | |
| ARH0_AIC0_UPCLK | APIX input pin | 23 | 31 | 39 | |
| ARH0_AIC0_UPDATA0 | APIX input pin | 25 | 33 | 41 | |
| ARH0_AIC0_UPDATA1 | APIX input pin | 24 | 32 | 40 | |
| ARH0_AIC0_dbg_out_0 | APIX output pin | 14 | 14 | 20 | |
| ARH0_AIC0_dbg_out_1 | APIX output pin | 13 | 13 | 19 | |
| ARH0_AIC0_dbg_select | APIX input pin | 15 | 15 | 21 | |
| ARH0_AIC1_DNCLK | APIX output pin | 3 | 3 | 3 | |
| ARH0_AIC1_DNDATA0 | APIX output pin | 7 | 7 | 10 | |
| ARH0_AIC1_DNDATA1 | APIX output pin | 4 | 4 | 4 | |
| ARH0_AIC1_RCK | APIX input pin | 8 | 8 | 11 | |
| ARH0_AIC1_RDA0 | APIX input pin | 10 | 10 | 13 | |
| ARH0_AIC1_RDA1 | APIX input pin | 9 | 9 | 12 | |
| ARH0_AIC1_TCKI | APIX input pin | 3 | 3 | 3 | |
| ARH0_AIC1_TDA0 | APIX output pin | 7 | 7 | 10 | |
| ARH0_AIC1_TDA1 | APIX output pin | 4 | 4 | 4 | |
| ARH0_AIC1_UPCLK | APIX input pin | 8 | 8 | 11 | |
| ARH0_AIC1_UPDATA0 | APIX input pin | 10 | 10 | 13 | |
| ARH0_AIC1_UPDATA1 | APIX input pin | 9 | 9 | 12 | |
| ARH0_AIC1_dbg_out_0 | APIX output pin | 6 | 6 | 9 | |
| ARH0_AIC1_dbg_out_1 | APIX output pin | 5 | 5 | 5 | |
| ARH0_AIC1_dbg_select | APIX input pin | 19 | 26 | 34 | |
| INDICATOR0_0 | Indicator PWM output pin 0 (It can also obtained from INDICATOR0_1) | 70 | 86 | 102 | |
| INDICATOR0_1 | Indicator PWM output pin 1 (It can also obtained from INDICATOR0_0) | 88 | 112 | 129 | |
| SYSC0_CLK_0 | System clock output pin (0) | 93 | 117 | 139 | |
| SYSC0_CLK_1 | System clock output pin (1) | 87 | 111 | 128 | |
| MAD0 | External Bus pin | 143 | 175 | 207 | |
| MAD1 | External Bus pin | 2 | 2 | 2 | |
| MAD2 | External Bus pin | 3 | 3 | 3 | |
| MAD3 | External Bus pin | 4 | 4 | 4 | |
| MAD4 | External Bus pin | 5 | 5 | 5 | |
| MAD5 | External Bus pin | 6 | 6 | 9 | |
| MAD6 | External Bus pin | 7 | 7 | 10 | |
| MAD7 | External Bus pin | 8 | 8 | 11 | |
| MAD8 | External Bus pin | 9 | 9 | 12 | |
| MAD9 | External Bus pin | 10 | 10 | 13 | |
| MAD10 | External Bus pin | 11 | 11 | 14 | |
| MAD11 | External Bus pin | 12 | 12 | 18 | |
| MAD12 | External Bus pin | 13 | 13 | 19 | |
| MAD13 | External Bus pin | 14 | 14 | 20 | |
| MAD14 | External Bus pin | 15 | 15 | 21 | |
| MAD15 | External Bus pin | - | 19 | 25 | |
| MAD16 | External Bus pin | - | 20 | 26 | |
| MAD17 | External Bus pin | - | 21 | 27 | |
| MAD18 | External Bus pin | - | 22 | 28 | |
| MAD19 | External Bus pin | - | 23 | 29 | |
| MAD20 | External Bus pin | - | 24 | 32 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| MAD21 | External Bus pin | - | 25 | 33 | |
| MDATA0 | External Bus pin | 135 | 167 | 199 | |
| MDATA1 | External Bus pin | 136 | 168 | 200 | |
| MDATA2 | External Bus pin | 137 | 169 | 201 | |
| MDATA3 | External Bus pin | 138 | 170 | 202 | |
| MDATA4 | External Bus pin | 139 | 171 | 203 | |
| MDATA5 | External Bus pin | 140 | 172 | 204 | |
| MDATA6 | External Bus pin | 141 | 173 | 205 | |
| MDATA7 | External Bus pin | 142 | 174 | 206 | |
| MDATA8 | External Bus pin | - | 154 | 186 | |
| MDATA9 | External Bus pin | - | 155 | 187 | |
| MDATA10 | External Bus pin | - | 156 | 188 | |
| MDATA11 | External Bus pin | - | 157 | 189 | |
| MDATA12 | External Bus pin | - | 162 | 194 | |
| MDATA13 | External Bus pin | - | 163 | 195 | |
| MDATA14 | External Bus pin | - | 164 | 196 | |
| MDATA15 | External Bus pin | - | 165 | 197 | |
| MCLK | External Bus pin | 21 | 28 | 36 | |
| MOEX | External Bus pin | 19 | 26 | 34 | |
| MWEX | External Bus pin | 20 | 27 | 35 | |
| MDQM0 | External Bus pin | 22 | 30 | 38 | |
| MDQM1 | External Bus pin | - | 29 | 37 | |
| MCSX0 | External Bus pin | 130 | 158 | 190 | |
| MCSX1 | External Bus pin | 134 | 166 | 198 | |
| MCSX2 | External Bus pin | 23 | 31 | 39 | |
| MCSX3 | External Bus pin | 24 | 32 | 40 | |
| MRDY | External Bus pin | 25 | 33 | 41 | |
| P0_00 | General-Purpose I/O port | 2 | 2 | 2 | |
| P0_01 | General-Purpose I/O port | 3 | 3 | 3 | |
| P0_02 | General-Purpose I/O port | 4 | 4 | 4 | |
| P0_03 | General-Purpose I/O port | 5 | 5 | 5 | |
| P0_04 | General-Purpose I/O port | 6 | 6 | 9 | |
| P0_05 | General-Purpose I/O port | 7 | 7 | 10 | |
| P0_06 | General-Purpose I/O port | 8 | 8 | 11 | |
| P0_07 | General-Purpose I/O port | 9 | 9 | 12 | |
| P0_08 | General-Purpose I/O port | 10 | 10 | 13 | |
| P0_09 | General-Purpose I/O port | 11 | 11 | 14 | |
| P0_10 | General-Purpose I/O port | 12 | 12 | 18 | |
| P0_11 | General-Purpose I/O port | 13 | 13 | 19 | |
| P0_12 | General-Purpose I/O port | 14 | 14 | 20 | |
| P0_13 | General-Purpose I/O port | 15 | 15 | 21 | |
| P0_14 | General-Purpose I/O port | 19 | 26 | 34 | |
| P0_15 | General-Purpose I/O port | 20 | 27 | 35 | |
| P0_16 | General-Purpose I/O port | 21 | 28 | 36 | |
| P0_17 | General-Purpose I/O port | 22 | 30 | 38 | |
| P0_18 | General-Purpose I/O port | 23 | 31 | 39 | |
| P0_19 | General-Purpose I/O port | 24 | 32 | 40 | |
| P0_20 | General-Purpose input port | 25 | 33 | 41 | |
| P0_21 | General-Purpose I/O port | 38 | 46 | 54 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| P0_22 | General-Purpose I/O port | 39 | 47 | 55 | |
| P0_23 | General-Purpose I/O port | 40 | 48 | 56 | |
| P0_24 | General-Purpose I/O port | 41 | 49 | 57 | |
| P0_25 | General-Purpose I/O port | 42 | 50 | 58 | |
| P0_26 | General-Purpose I/O port | 44 | 52 | 60 | |
| P0_27 | General-Purpose I/O port | 47 | 55 | 63 | |
| P0_28 | General-Purpose I/O port | 48 | 56 | 64 | |
| P0_29 | General-Purpose I/O port | 49 | 57 | 65 | |
| P0_30 | General-Purpose I/O port | 50 | 58 | 66 | |
| P0_31 | General-Purpose I/O port | 51 | 59 | 67 | |
| P1_00 | General-Purpose I/O port | 54 | 62 | 70 | |
| P1_01 | General-Purpose I/O port | 55 | 63 | 71 | |
| P1_02 | General-Purpose I/O port | 56 | 64 | 72 | |
| P1_03 | General-Purpose I/O port | 61 | 73 | 85 | |
| P1_04 | General-Purpose I/O port | 62 | 74 | 86 | |
| P1_05 | General-Purpose I/O port | 63 | 77 | 89 | |
| P1_06 | General-Purpose I/O port | 64 | 78 | 90 | |
| P1_07 | General-Purpose I/O port | 65 | 81 | 93 | |
| P1_08 | General-Purpose I/O port | 66 | 82 | 94 | |
| P1_09 | General-Purpose I/O port | 67 | 83 | 95 | |
| P1_10 | General-Purpose I/O port | 68 | 84 | 98 | |
| P1_11 | General-Purpose I/O port | 70 | 86 | 102 | |
| P1_12 | General-Purpose I/O port | 71 | 87 | 103 | |
| P1_13 | General-Purpose I/O port | 81 | 97 | 113 | |
| P1_14 | General-Purpose I/O port | 87 | 111 | 128 | |
| P1_15 | General-Purpose I/O port | 88 | 112 | 129 | |
| P1_16 | General-Purpose I/O port | 93 | 117 | 139 | |
| P1_17 | General-Purpose I/O port | 100 | 124 | 148 | |
| P1_18 | General-Purpose I/O port | 101 | 125 | 149 | |
| P1_19 | General-Purpose I/O port | 102 | 126 | 150 | |
| P1_20 | General-Purpose I/O port | 103 | 127 | 151 | |
| P1_21 | General-Purpose I/O port | 104 | 128 | 152 | |
| P1_22 | General-Purpose I/O port | 105 | 129 | 153 | |
| P1_23 | General-Purpose I/O port | 106 | 130 | 154 | |
| P1_24 | General-Purpose I/O port | 107 | 131 | 155 | |
| P1_25 | General-Purpose I/O port | 110 | 134 | 158 | |
| P1_26 | General-Purpose I/O port | 111 | 135 | 160 | |
| P1_27 | General-Purpose I/O port | 112 | 136 | 161 | |
| P1_28 | General-Purpose I/O port | 113 | 137 | 162 | |
| P1_29 | General-Purpose I/O port | 114 | 138 | 164 | |
| P1_30 | General-Purpose I/O port | 115 | 139 | 165 | |
| P1_31 | General-Purpose I/O port | 116 | 140 | 166 | |
| P2_00 | General-Purpose I/O port | 117 | 141 | 168 | |
| P2_01 | General-Purpose I/O port | 120 | 144 | 171 | |
| P2_02 | General-Purpose I/O port | 121 | 145 | 173 | |
| P2_03 | General-Purpose I/O port | 122 | 146 | 174 | |
| P2_04 | General-Purpose I/O port | 123 | 147 | 175 | |
| P2_05 | General-Purpose I/O port | 124 | 148 | 177 | |
| P2_06 | General-Purpose I/O port | 125 | 149 | 178 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| P2_07 | General-Purpose I/O port | 126 | 150 | 179 | |
| P2_08 | General-Purpose I/O port | 127 | 151 | 181 | |
| P2_09 | General-Purpose I/O port | 130 | 158 | 190 | |
| P2_10 | General-Purpose I/O port | 134 | 166 | 198 | |
| P2_11 | General-Purpose I/O port | 135 | 167 | 199 | |
| P2_12 | General-Purpose I/O port | 136 | 168 | 200 | |
| P2_13 | General-Purpose I/O port | 137 | 169 | 201 | |
| P2_14 | General-Purpose I/O port | 138 | 170 | 202 | |
| P2_15 | General-Purpose I/O port | 139 | 171 | 203 | |
| P2_16 | General-Purpose I/O port | 140 | 172 | 204 | |
| P2_17 | General-Purpose I/O port | 141 | 173 | 205 | |
| P2_18 | General-Purpose I/O port | 142 | 174 | 206 | |
| P2_19 | General-Purpose I/O port | 143 | 175 | 207 | |
| P3_00 | General-Purpose I/O port | - | 19 | 25 | |
| P3_01 | General-Purpose I/O port | - | 20 | 26 | |
| P3_02 | General-Purpose I/O port | - | 21 | 27 | |
| P3_03 | General-Purpose I/O port | - | 22 | 28 | |
| P3_04 | General-Purpose I/O port | - | 23 | 29 | |
| P3_05 | General-Purpose I/O port | - | 24 | 32 | |
| P3_06 | General-Purpose I/O port | - | 25 | 33 | |
| P3_07 | General-Purpose I/O port | - | 29 | 37 | |
| P3_08 | General-Purpose I/O port | - | 69 | 81 | |
| P3_09 | General-Purpose I/O port | - | 70 | 82 | |
| P3_10 | General-Purpose I/O port | - | 71 | 83 | |
| P3_11 | General-Purpose I/O port | - | 72 | 84 | |
| P3_12 | General-Purpose I/O port | - | 75 | 87 | |
| P3_13 | General-Purpose I/O port | - | 76 | 88 | |
| P3_14 | General-Purpose I/O port | - | 79 | 91 | |
| P3_15 | General-Purpose I/O port | - | 80 | 92 | |
| P3_16 | General-Purpose I/O port | - | 98 | 114 | |
| P3_17 | General-Purpose I/O port | - | 99 | 115 | |
| P3_18 | General-Purpose I/O port | - | 105 | 122 | |
| P3_19 | General-Purpose I/O port | - | 106 | 123 | |
| P3_20 | General-Purpose I/O port | - | 107 | 124 | |
| P3_21 | General-Purpose I/O port | - | 108 | 125 | |
| P3_22 | General-Purpose I/O port | - | 109 | 126 | |
| P3_23 | General-Purpose I/O port | - | 110 | 127 | |
| P3_24 | General-Purpose I/O port | - | 154 | 186 | |
| P3_25 | General-Purpose I/O port | - | 155 | 187 | |
| P3_26 | General-Purpose I/O port | - | 156 | 188 | |
| P3_27 | General-Purpose I/O port | - | 157 | 189 | |
| P3_28 | General-Purpose I/O port | - | 162 | 194 | |
| P3_29 | General-Purpose I/O port | - | 163 | 195 | |
| P3_30 | General-Purpose I/O port | - | 164 | 196 | |
| P3_31 | General-Purpose I/O port | - | 165 | 197 | |
| P4_00 | General-Purpose I/O port | - | - | 6 | |
| P4_01 | General-Purpose I/O port | - | - | 7 | |
| P4_02 | General-Purpose I/O port | - | - | 8 | |
| P4_03 | General-Purpose I/O port | - | - | 15 | |

| Port Name | Description | Package Pin Number | | | Remark |
|---|---|---|---|---|---|
| | | TEQFP 144 | TEQFP 176 | TEQFP 208 | |
| P4_04 | General-Purpose I/O port | - | - | 16 | |
| P4_05 | General-Purpose I/O port | - | - | 17 | |
| P4_06 | General-Purpose I/O port | - | - | 30 | |
| P4_07 | General-Purpose I/O port | - | - | 31 | |
| P4_08 | General-Purpose I/O port | - | - | 77 | |
| P4_09 | General-Purpose I/O port | - | - | 78 | |
| P4_10 | General-Purpose I/O port | - | - | 79 | |
| P4_11 | General-Purpose I/O port | - | - | 80 | |
| P4_12 | General-Purpose I/O port | - | - | 96 | |
| P4_13 | General-Purpose I/O port | - | - | 97 | |
| P4_14 | General-Purpose I/O port | - | - | 99 | |
| P4_15 | General-Purpose I/O port | - | - | 100 | |
| P4_16 | General-Purpose I/O port | - | - | 116 | |
| P4_17 | General-Purpose I/O port | - | - | 130 | |
| P4_18 | General-Purpose I/O port | - | - | 131 | |
| P4_19 | General-Purpose I/O port | - | - | 136 | |
| P4_20 | General-Purpose I/O port | - | - | 137 | |
| P4_21 | General-Purpose I/O port | - | - | 138 | |
| P4_22 | General-Purpose I/O port | - | - | 140 | |
| P4_23 | General-Purpose I/O port | - | - | 141 | |
| P4_24 | General-Purpose I/O port | - | - | 159 | |
| P4_25 | General-Purpose I/O port | - | - | 163 | |
| P4_26 | General-Purpose I/O port | - | - | 167 | |
| P4_27 | General-Purpose I/O port | - | - | 172 | |
| P4_28 | General-Purpose I/O port | - | - | 176 | |
| P4_29 | General-Purpose I/O port | - | - | 180 | |
| P4_30 | General-Purpose I/O port | - | - | 184 | |
| P4_31 | General-Purpose I/O port | - | - | 185 | |

## 6.2 Remark

***Notes:***

- *The port description list shows the port function of description which is mounted and supported on the product. The function which is not described in this table is not supported and assured.*
- *See the function list of the product as well.*

# 7. Port Configuration

## 7.1 Resource Input Configuration Module

The resource input configuration module (RIC) is a function to select input from an external or output from another internal resource as resource input. A resource which supports either a port input relocation or a resource inputs from the other resource has its RIC_RESIN register to configure resource input configuration. The Resource which are available through only one port does not have the multiplexer implemented i.e. No RIC_RESIN register.

### *7.1.1 RIC (S6J3310)*

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN000 (0x0000) | SIN16 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_08 | P4_19 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN001 (0x0002) | SCK16 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_09 | P4_21 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN002 (0x0004) | SCL16 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN003 (0x0006) | SDA16 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN004 (0x0008) | MFS16_TRIGGER | RESSEL (0-7) | TOT48 | TOT49 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN005 (0x000A) | SCS16 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_11 | P4_23 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN007 (0x000E) | SIN17 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_14 | P0_09 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN008 (0x0010) | SCK17 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_15 | P4_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN009 (0x0012) | SCL17 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN010 (0x0014) | SDA17 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN011 (0x0016) | MFS17_TRIGGER | RESSEL (0-7) | TOT48 | TOT49 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN012 (0x0018) | SCS17 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_17 | P4_03 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN021 (0x002A) | SIN0 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_03 | P0_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN022 (0x002C) | SCK0 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_04 | P0_06 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN023 (0x002E) | SCL0 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN024 (0x0030) | SDA0 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN025 (0x0032) | MFS0_TRIGGER | RESSEL (0-7) | TOT0 | TOT1 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN026 (0x0034) | SCS0 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_06 | P0_07 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN028 (0x0038) | SIN1 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_01 | P3_00 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN029 (0x003A) | SCK1 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_02 | P3_01 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN030 (0x003C) | SCL1 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN031 (0x003E) | SDA1 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN032 (0x0040) | MFS1_TRIGGER | RESSEL (0-7) | TOT0 | TOT1 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN033 (0x0042) | SCS1 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_04 | P3_03 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN035 (0x0046) | SIN2 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_21 | P4_30 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN036 (0x0048) | SCK2 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_22 | P4_31 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN039 (0x004E) | MFS2_TRIGGER | RESSEL (0-7) | TOT0 | TOT1 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN040 (0x0050) | SCS2 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_24 | P3_25 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN042 (0x0054) | SIN3 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_28 | P3_28 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN043 (0x0056) | SCK3 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_29 | P3_29 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN046 (0x005C) | MFS3_TRIGGER | RESSEL (0-7) | TOT0 | TOT1 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN047 (0x005E) | SCS3 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_31 | P3_31 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN049 (0x0062) | SIN4 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_13 | P3_05 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN050 (0x0064) | SCK4 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_14 | P0_14 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN051 (0x0066) | SCL4 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN052 (0x0068) | SDA4 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN053 (0x006A) | MFS4_TRIGGER | RESSEL (0-7) | TOT0 | TOT1 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN054 (0x006C) | SCS4 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_16 | P0_15 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN077 (0x009A) | SIN8 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_19 | P3_08 | P0_27 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN078 (0x009C) | SCK8 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_20 | P3_09 | P0_28 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN079 (0x009E) | SCL8 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN080 (0x00A0) | SDA8 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN081 (0x00A2) | MFS8_TRIGGER | RESSEL (0-7) | TOT16 | TOT17 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN082 (0x00A4) | SCS8 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_22 | P3_11 | P0_30 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN084 (0x00A8) | SIN9 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_23 | P3_18 | P0_21 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN085 (0x00AA) | SCK9 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_24 | P3_19 | P0_23 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN086 (0x00AC) | SCL9 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN087 (0x00AE) | SDA9 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN088 (0x00B0) | MFS9_TRIGGER | RESSEL (0-7) | TOT16 | TOT17 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN089 (0x00B2) | SCS9 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_26 | P3_21 | P0_24 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN091 (0x00B6) | SIN10 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_28 | P3_12 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN092 (0x00B8) | SCK10 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_29 | P3_13 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN093 (0x00BA) | SCL10 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN094 (0x00BC) | SDA10 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN095 (0x00BE) | MFS10_TRIGGER | RESSEL (0-7) | TOT16 | TOT17 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN096 (0x00C0) | SCS10 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_31 | P3_15 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN100 (0x00C8) | SCL11 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN101 (0x00CA) | SDA11 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN102 (0x00CC) | MFS11_TRIGGER | RESSEL (0-7) | TOT16 | TOT17 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN105 (0x00D2) | SIN12 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_05 | P4_18 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN106 (0x00D4) | SCK12 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_06 | P1_15 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN107 (0x00D6) | SCL12 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN108 (0x00D8) | SDA12 | RESSEL (0-7) | 80 ns noise filter disable | 80 ns noise filter enable | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN109 (0x00DA) | MFS12_TRIGGER | RESSEL (0-7) | TOT16 | TOT17 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN110 (0x00DC) | SCS12 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_08 | P3_23 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN133 (0x010A) | RX5 | RESSEL (0-7) | PORT_PIN | MCAN5_PIN_AND_TX | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_17 | P3_19 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN134 (0x010C) | RX6 | RESSEL (0-7) | PORT_PIN | MCAN6_PIN_AND_TX | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_21 | P3_22 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN136 (0x0110) | RX0 | RESSEL (0-7) | PORT_PIN | MCAN0_PIN_AND_TX | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_05 | P3_09 | P4_00 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN137 (0x0112) | RX1 | RESSEL (0-7) | PORT_PIN | MCAN1_PIN_AND_TX | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_07 | P3_11 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN138 (0x0114) | RX2 | RESSEL (0-7) | PORT_PIN | MCAN2_PIN_AND_TX | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_11 | P3_14 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN139 (0x0116) | RX3 | RESSEL (0-7) | PORT_PIN | MCAN3_PIN_AND_TX | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_13 | P3_16 | P4_03 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN141 (0x011A) | TIN48 | RESSEL (0-7) | PORT_PIN | TOT49 | RLT49_UFSET | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_13 | P3_16 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN142 (0x011C) | TIN49 | RESSEL (0-7) | PORT_PIN | TOT48 | RLT48_UFSET | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_15 | P3_20 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN144 (0x0120) | TIN0 | RESSEL (0-7) | PORT_PIN | TOT1 | RLT1_UFSET | - | PPG0_TOUT0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_03 | P3_08 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN145 (0x0122) | TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | - | PPG1_TOUT0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_05 | P3_10 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN160 (0x0140) | TIN16 | RESSEL (0-7) | PORT_PIN | TOT17 | RLT17_UFSET | - | PPG6_TOUT0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_07 | P3_12 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN161 (0x0142) | TIN17 | RESSEL (0-7) | PORT_PIN | TOT16 | RLT16_UFSET | - | PPG7_TOUT0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_11 | P3_14 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN192 (0x0180) | EINT0 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_13 | P0_00 | P0_08 | P0_20 | P3_17 | P2_01 | P2_16 | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN193 (0x0182) | EINT1 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_01 | P3_00 | P0_09 | P0_22 | P4_16 | P4_27 | P2_17 | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN194 (0x0184) | EINT2 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_21 | P4_30 | P4_03 | P0_23 | P3_20 | P2_02 | P2_18 | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN195 (0x0186) | EINT3 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_28 | P3_28 | P4_04 | P0_24 | P3_21 | P2_03 | P2_19 | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN196 (0x0188) | EINT4 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_03 | P0_02 | P4_05 | P0_25 | P3_23 | P2_04 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN197 (0x018A) | EINT5 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_04 | P0_03 | P0_10 | P0_26 | P4_17 | P4_28 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN198 (0x018C) | EINT6 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_05 | P3_09 | P0_11 | P0_27 | P4_18 | P2_06 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN199 (0x018E) | EINT7 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_06 | P4_00 | P0_12 | P0_29 | P4_20 | P2_07 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN200 (0x0190) | EINT8 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_07 | P3_11 | P0_13 | P0_30 | P4_21 | P4_29 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN201 (0x0192) | EINT9 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_08 | P4_01 | P3_01 | P0_31 | P1_16 | P2_08 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN202 (0x0194) | EINT10 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_09 | P4_02 | P3_02 | P1_00 | P4_23 | P4_31 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN203 (0x0196) | EINT11 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_10 | P0_04 | P3_03 | P1_01 | P1_18 | P3_24 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN204 (0x0198) | EINT12 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_11 | P3_14 | P3_04 | P1_02 | P1_20 | P3_25 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN205 (0x019A) | EINT13 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_12 | P0_05 | P4_06 | P4_08 | P1_22 | P3_26 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN206 (0x019C) | EINT14 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_13 | P3_16 | P4_07 | P4_09 | P1_24 | P3_27 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN207 (0x019E) | EINT15 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_14 | P0_06 | P3_05 | P4_10 | P1_25 | P2_09 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN208 (0x01A0) | EINT16 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_15 | P4_19 | P3_06 | P4_11 | P4_24 | P3_29 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN209 (0x01A2) | EINT17 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_17 | P3_19 | P0_14 | P3_10 | P1_26 | P3_30 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN210 (0x01A4) | EINT18 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_19 | P3_08 | P0_15 | P3_13 | P1_27 | P3_31 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN211 (0x01A6) | EINT19 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_21 | P3_22 | P0_16 | P3_15 | P4_25 | P2_10 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN212 (0x01A8) | EINT20 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_23 | P3_18 | P3_07 | P4_12 | P1_29 | P2_11 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN213 (0x01AA) | EINT21 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_28 | P3_12 | P0_17 | P4_13 | P1_30 | P2_12 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN214 (0x01AC) | EINT22 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_00 | P4_22 | P0_18 | P4_14 | P1_31 | P2_14 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN215 (0x01AE) | EINT23 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_05 | P0_07 | P0_19 | P4_15 | P4_26 | P2_15 | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN216 (0x01B0) | TEXT0 | RESSEL (0-7) | PORT_PIN | TOT0 | TOT1 | PPG0_TOUT2 | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN217 (0x01B2) | TEXT1 | RESSEL (0-7) | PORT_PIN | TOT0 | TOT1 | PPG1_TOUT2 | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN218 (0x01B4) | TEXT2 | RESSEL (0-7) | PORT_PIN | TOT0 | TOT1 | PPG2_TOUT2 | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN219 (0x01B6) | TEXT3 | RESSEL (0-7) | PORT_PIN | TOT0 | TOT1 | PPG3_TOUT2 | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN220 (0x01B8) | TEXT4 | RESSEL (0-7) | PORT_PIN | TOT0 | TOT1 | PPG4_TOUT2 | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN224 (0x01C0) | TEXT8 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | PPG6_TOUT2 | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN225 (0x01C2) | TEXT9 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | PPG7_TOUT2 | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN226 (0x01C4) | TEXT10 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | PPG8_TOUT2 | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| IN232 (0x01D0) | OCU0_CK0 | RESSEL (0-7) | FRT0 | FRT1 | FRT2 | FRT3 | FRT4 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_CK1 | RESSEL (0-7) | FRT0 | FRT1 | FRT2 | FRT3 | FRT4 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_DOWNB0 | RESSEL (0-7) | FRT0_DOWNB | FRT1_DOWNB | FRT2_DOWNB | FRT3_DOWNB | FRT4_DOWNB | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_DOWNB1 | RESSEL (0-7) | FRT0_DOWNB | FRT1_DOWNB | FRT2_DOWNB | FRT3_DOWNB | FRT4_DOWNB | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_FCMD0 | RESSEL (0-7) | FRT0_FCMD | FRT1_FCMD | FRT2_FCMD | FRT3_FCMD | FRT4_FCMD | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| IN232 (0x01D0) | OCU0_FCMD1 | RESSEL (0-7) | FRT0_FCMD | FRT1_FCMD | FRT2_FCMD | FRT3_FCMD | FRT4_FCMD | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_MTSF0 | RESSEL (0-7) | FRT0_MTSF | FRT1_MTSF | FRT2_MTSF | FRT3_MTSF | FRT4_MTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_MTSF1 | RESSEL (0-7) | FRT0_MTSF | FRT1_MTSF | FRT2_MTSF | FRT3_MTSF | FRT4_MTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_T0[31:0] | RESSEL (0-7) | FRT0_T[31:0] | FRT1_T[31:0] | FRT2_T[31:0] | FRT3_T[31:0] | FRT4_T[31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_T1[31:0] | RESSEL (0-7) | FRT0_T[31:0] | FRT1_T[31:0] | FRT2_T[31:0] | FRT3_T[31:0] | FRT4_T[31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| IN232 (0x01D0) | OCU0_ZTSF0 | RESSEL (0-7) | FRT0_ZTSF | FRT1_ZTSF | FRT2_ZTSF | FRT3_ZTSF | FRT4_ZTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU0_ZTSF1 | RESSEL (0-7) | FRT0_ZTSF | FRT1_ZTSF | FRT2_ZTSF | FRT3_ZTSF | FRT4_ZTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN233 (0x01D2) | OCU0_MOD0 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN234 (0x01D4) | OCU0_MOD1 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN235 (0x01D6) | OCU1_CK0 | RESSEL (0-7) | FRT0 | FRT1 | FRT2 | FRT3 | FRT4 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN235 (0x01D6) | OCU1_CK1 | RESSEL (0-7) | FRT0 | FRT1 | FRT2 | FRT3 | FRT4 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU1_DOWNB0 | RESSEL (0-7) | FRT0_DOWNB | FRT1_DOWNB | FRT2_DOWNB | FRT3_DOWNB | FRT4_DOWNB | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU1_DOWNB1 | RESSEL (0-7) | FRT0_DOWNB | FRT1_DOWNB | FRT2_DOWNB | FRT3_DOWNB | FRT4_DOWNB | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU1_FCMD0 | RESSEL (0-7) | FRT0_FCMD | FRT1_FCMD | FRT2_FCMD | FRT3_FCMD | FRT4_FCMD | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU1_FCMD1 | RESSEL (0-7) | FRT0_FCMD | FRT1_FCMD | FRT2_FCMD | FRT3_FCMD | FRT4_FCMD | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN235 (0x01D6) | OCU1_MTSF0 | RESSEL (0-7) | FRT0_MTSF | FRT1_MTSF | FRT2_MTSF | FRT3_MTSF | FRT4_MTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU1_MTSF1 | RESSEL (0-7) | FRT0_MTSF | FRT1_MTSF | FRT2_MTSF | FRT3_MTSF | FRT4_MTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU1_T0[31:0] | RESSEL (0-7) | FRT0_T[31:0] | FRT1_T[31:0] | FRT2_T[31:0] | FRT3_T[31:0] | FRT4_T[31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU1_T1[31:0] | RESSEL (0-7) | FRT0_T[31:0] | FRT1_T[31:0] | FRT2_T[31:0] | FRT3_T[31:0] | FRT4_T[31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN235 (0x01D6) | OCU1_ZTSF0 | RESSEL (0-7) | FRT0_ZTSF | FRT1_ZTSF | FRT2_ZTSF | FRT3_ZTSF | FRT4_ZTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU1_ZTSF1 | RESSEL (0-7) | FRT0_ZTSF | FRT1_ZTSF | FRT2_ZTSF | FRT3_ZTSF | FRT4_ZTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN236 (0x01D8) | OCU1_MOD0 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN237 (0x01DA) | OCU1_MOD1 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN238 (0x01DC) | OCU2_CK0 | RESSEL (0-7) | FRT0 | FRT1 | FRT2 | FRT3 | FRT4 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_CK1 | RESSEL (0-7) | FRT0 | FRT1 | FRT2 | FRT3 | FRT4 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_DOWNB0 | RESSEL (0-7) | FRT0_DOWNB | FRT1_DOWNB | FRT2_DOWNB | FRT3_DOWNB | FRT4_DOWNB | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN238 (0x01DC) | OCU2_DOWNB1 | RESSEL (0-7) | FRT0_DOWNB | FRT1_DOWNB | FRT2_DOWNB | FRT3_DOWNB | FRT4_DOWNB | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_FCMD0 | RESSEL (0-7) | FRT0_FCMD | FRT1_FCMD | FRT2_FCMD | FRT3_FCMD | FRT4_FCMD | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_FCMD1 | RESSEL (0-7) | FRT0_FCMD | FRT1_FCMD | FRT2_FCMD | FRT3_FCMD | FRT4_FCMD | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_MTSF0 | RESSEL (0-7) | FRT0_MTSF | FRT1_MTSF | FRT2_MTSF | FRT3_MTSF | FRT4_MTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_MTSF1 | RESSEL (0-7) | FRT0_MTSF | FRT1_MTSF | FRT2_MTSF | FRT3_MTSF | FRT4_MTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN238 (0x01DC) | OCU2_T0[31:0] | RESSEL (0-7) | FRT0_T [31:0] | FRT1_T [31:0] | FRT2_T [31:0] | FRT3_T [31:0] | FRT4_T [31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_T1[31:0] | RESSEL (0-7) | FRT0_T [31:0] | FRT1_T [31:0] | FRT2_T [31:0] | FRT3_T [31:0] | FRT4_T [31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_ZTSF0 | RESSEL (0-7) | FRT0_ZTSF | FRT1_ZTSF | FRT2_ZTSF | FRT3_ZTSF | FRT4_ZTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU2_ZTSF1 | RESSEL (0-7) | FRT0_ZTSF | FRT1_ZTSF | FRT2_ZTSF | FRT3_ZTSF | FRT4_ZTSF | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN239 (0x01DE) | OCU2_MOD0 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN240 (0x01E0) | OCU2_MOD1 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN256 (0x0200) | OCU8_CK0 | RESSEL (0-7) | FRT8 | FRT9 | FRT10 | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_CK1 | RESSEL (0-7) | FRT8 | FRT9 | FRT10 | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_DOWNB0 | RESSEL (0-7) | FRT8_DOWNB | FRT9_DOWNB | FRT10_DOWNB | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_DOWNB1 | RESSEL (0-7) | FRT8_DOWNB | FRT9_DOWNB | FRT10_DOWNB | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_FCMD0 | RESSEL (0-7) | FRT8_FCMD | FRT9_FCMD | FRT10_FCMD | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN256 (0x0200) | OCU8_FCMD1 | RESSEL (0-7) | FRT8_FCMD | FRT9_FCMD | FRT10_FCMD | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_MTSF0 | RESSEL (0-7) | FRT8_MTSF | FRT9_MTSF | FRT10_MTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_MTSF1 | RESSEL (0-7) | FRT8_MTSF | FRT9_MTSF | FRT10_MTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_T0[31:0] | RESSEL (0-7) | FRT8_T[31:0] | FRT9_T[31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_T1[31:0] | RESSEL (0-7) | FRT8_T[31:0] | FRT9_T[31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN256 (0x0200) | OCU8_ZTSF0 | RESSEL (0-7) | FRT8_ZTSF | FRT9_ZTSF | FRT10_ZTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU8_ZTSF1 | RESSEL (0-7) | FRT8_ZTSF | FRT9_ZTSF | FRT10_ZTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN257 (0x0202) | OCU8_MOD0 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN258 (0x0204) | OCU8_MOD1 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN259 (0x0206) | OCU9_CK0 | RESSEL (0-7) | FRT8 | FRT9 | FRT10 | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_CK1 | RESSEL (0-7) | FRT8 | FRT9 | FRT10 | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN259 (0x0206) | OCU9_DOWNB0 | RESSEL (0-7) | FRT8_DOWNB | FRT9_DOWNB | FRT10_DOWNB | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_DOWNB1 | RESSEL (0-7) | FRT8_DOWNB | FRT9_DOWNB | FRT10_DOWNB | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_FCMD0 | RESSEL (0-7) | FRT8_FCMD | FRT9_FCMD | FRT10_FCMD | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_FCMD1 | RESSEL (0-7) | FRT8_FCMD | FRT9_FCMD | FRT10_FCMD | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_MTSF0 | RESSEL (0-7) | FRT8_MTSF | FRT9_MTSF | FRT10_MTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN259 (0x0206) | OCU9_MTSF1 | RESSEL (0-7) | FRT8_MTSF | FRT9_MTSF | FRT10_MTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_T0[31:0] | RESSEL (0-7) | FRT8_T[31:0] | FRT9_T[31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_T1[31:0] | RESSEL (0-7) | FRT8_T[31:0] | FRT9_T[31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_ZTSF0 | RESSEL (0-7) | FRT8_ZTSF | FRT9_ZTSF | FRT10_ZTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU9_ZTSF1 | RESSEL (0-7) | FRT8_ZTSF | FRT9_ZTSF | FRT10_ZTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN260 (0x0208) | OCU9_MOD0 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN261 (0x020A) | OCU9_MOD1 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN262 (0x020C) | OCU10_CK0 | RESSEL (0-7) | FRT8 | FRT9 | FRT10 | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_CK1 | RESSEL (0-7) | FRT8 | FRT9 | FRT10 | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_DOWNB0 | RESSEL (0-7) | FRT8_DOWNB | FRT9_DOWNB | FRT10_DOWNB | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_DOWNB1 | RESSEL (0-7) | FRT8_DOWNB | FRT9_DOWNB | FRT10_DOWNB | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_FCMD0 | RESSEL (0-7) | FRT8_FCMD | FRT9_FCMD | FRT10_FCMD | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN262 (0x020C) | OCU10_FCMD1 | RESSEL (0-7) | FRT8_FCMD | FRT9_FCMD | FRT10_FCMD | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_MTSF0 | RESSEL (0-7) | FRT8_MTSF | FRT9_MTSF | FRT10_MTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_MTSF1 | RESSEL (0-7) | FRT8_MTSF | FRT9_MTSF | FRT10_MTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_T0[31:0] | RESSEL (0-7) | FRT8_T[31:0] | FRT9_T[31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_T1[31:0] | RESSEL (0-7) | FRT8_T[31:0] | FRT9_T[31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN262 (0x020C) | OCU10_ZTSF0 | RESSEL (0-7) | FRT8_ZTSF | FRT9_ZTSF | FRT10_ZTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | OCU10_ZTSF1 | RESSEL (0-7) | FRT8_ZTSF | FRT9_ZTSF | FRT10_ZTSF | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN263 (0x020E) | OCU10_MOD0 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN264 (0x0210) | OCU10_MOD1 | RESSEL (0-7) | set 1 | set 0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN280 (0x0230) | ICU0_IN0 | RESSEL (0-7) | PORT_PIN | MFS0_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_03 | P3_08 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN281 (0x0232) | ICU0_IN1 | RESSEL (0-7) | PORT_PIN | MFS1_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_04 | P3_09 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN282 (0x0234) | ICU0_T0[31:0] | RESSEL (0-7) | FRT0_T [31:0] | FRT1_T [31:0] | FRT2_T [31:0] | FRT3_T [31:0] | FRT4_T [31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | ICU0_T1[31:0] | RESSEL (0-7) | FRT0_T [31:0] | FRT1_T [31:0] | FRT2_T [31:0] | FRT3_T [31:0] | FRT4_T [31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN283 (0x0236) | ICU1_IN0 | RESSEL (0-7) | PORT_PIN | MFS2_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_05 | P3_10 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN284 (0x0238) | ICU1_IN1 | RESSEL (0-7) | PORT_PIN | MFS3_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_06 | P3_11 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN285 (0x023A) | ICU1_T0[31:0] | RESSEL (0-7) | FRT0_T [31:0] | FRT1_T [31:0] | FRT2_T [31:0] | FRT3_T [31:0] | FRT4_T [31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | ICU1_T1[31:0] | RESSEL (0-7) | FRT0_T [31:0] | FRT1_T [31:0] | FRT2_T [31:0] | FRT3_T [31:0] | FRT4_T [31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN286 (0x023C) | ICU2_IN0 | RESSEL (0-7) | PORT_PIN | MFS4_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_07 | P3_12 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN287 (0x023E) | ICU2_IN1 | RESSEL (0-7) | PORT_PIN | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_08 | P3_13 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN288 (0x0240) | ICU2_T0[31:0] | RESSEL (0-7) | FRT0_T [31:0] | FRT1_T [31:0] | FRT2_T [31:0] | FRT3_T [31:0] | FRT4_T [31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | ICU2_T1[31:0] | RESSEL (0-7) | FRT0_T [31:0] | FRT1_T [31:0] | FRT2_T [31:0] | FRT3_T [31:0] | FRT4_T [31:0] | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN304 (0x0260) | ICU8_IN0 | RESSEL (0-7) | PORT_PIN | MFS8_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_09 | P3_14 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN305 (0x0262) | ICU8_IN1 | RESSEL (0-7) | PORT_PIN | MFS9_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_10 | P3_15 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN306 (0x0264) | ICU8_T0[31:0] | RESSEL (0-7) | FRT8_T [31:0] | FRT9_T [31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | ICU8_T1[31:0] | RESSEL (0-7) | FRT8_T [31:0] | FRT9_T [31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN307 (0x0266) | ICU9_IN0 | RESSEL (0-7) | PORT_PIN | MFS10_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_11 | P3_16 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN308 (0x0268) | ICU9_IN1 | RESSEL (0-7) | PORT_PIN | MFS11_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_12 | P3_17 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN309 (0x026A) | ICU9_T0[31:0] | RESSEL (0-7) | FRT8_T [31:0] | FRT9_T [31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | ICU9_T1[31:0] | RESSEL (0-7) | FRT8_T [31:0] | FRT9_T [31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN310 (0x026C) | ICU10_IN0 | RESSEL (0-7) | PORT_PIN | MFS12_LSYN | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_14 | P3_18 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN311 (0x026E) | ICU10_IN1 | RESSEL (0-7) | PORT_PIN | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_15 | P3_19 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN312 (0x0270) | ICU10_T0 [31:0] | RESSEL (0-7) | FRT8_T [31:0] | FRT9_T [31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| | ICU10_T1 [31:0] | RESSEL (0-7) | FRT8_T [31:0] | FRT9_T [31:0] | FRT10_T[31:0] | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN352 (0x02C0) | AIN8 | RESSEL (0-7) | PORT_PIN | TOT0 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN353 (0x02C2) | BIN8 | RESSEL (0-7) | PORT_PIN | TOT1 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN354 (0x02C4) | ZIN8 | RESSEL (0-7) | PORT_PIN | TOT16 | PPG6_TOUT0 | PPG6_TOUT2 | PPG7_TOUT0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN355 (0x02C6) | AIN9 | RESSEL (0-7) | PORT_PIN | TOT16 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN356 (0x02C8) | BIN9 | RESSEL (0-7) | PORT_PIN | TOT17 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN357 (0x02CA) | ZIN9 | RESSEL (0-7) | PORT_PIN | TOT0 | PPG6_TOUT0 | PPG6_TOUT2 | PPG7_TOUT0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN376 (0x02F0) | PPG0_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT0 | RLT0_UFSET | FRT0_MTSF | OCU0_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_16 | P3_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN377 (0x02F2) | PPG0_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN378 (0x02F4) | PPG0_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN379 (0x02F6) | PPG1_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT0 | RLT0_UFSET | FRT0_MTSF | OCU0_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_16 | P3_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN380 (0x02F8) | PPG1_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN381 (0x02FA) | PPG1_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN382 (0x02FC) | PPG2_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT0 | RLT0_UFSET | FRT0_MTSF | OCU0_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_16 | P3_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN383 (0x02FE) | PPG2_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN384 (0x0300) | PPG2_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN385 (0x0302) | PPG3_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT1 | RLT1_UFSET | FRT0_MTSF | OCU0_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_16 | P3_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN386 (0x0304) | PPG3_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN387 (0x0306) | PPG3_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN388 (0x0308) | PPG4_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT1 | RLT1_UFSET | FRT0_MTSF | OCU0_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_16 | P3_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN389 (0x030A) | PPG4_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN390 (0x030C) | PPG4_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN391 (0x030E) | PPG5_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT1 | RLT1_UFSET | FRT0_MTSF | OCU0_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_16 | P3_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN392 (0x0310) | PPG5_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN393 (0x0312) | PPG5_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN394 (0x0314) | PPG6_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT16 | RLT16_UFSET | FRT8_MTSF | OCU8_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_29 | P3_20 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN395 (0x0316) | PPG6_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN396 (0x0318) | PPG6_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN397 (0x031A) | PPG7_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT16 | RLT16_UFSET | FRT8_MTSF | OCU8_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_29 | P3_20 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN398 (0x031C) | PPG7_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN399 (0x031E) | PPG7_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN400 (0x0320) | PPG8_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT16 | RLT16_UFSET | FRT8_MTSF | OCU8_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_29 | P3_20 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN401 (0x0322) | PPG8_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN402 (0x0324) | PPG8_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN403 (0x0326) | PPG9_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT17 | RLT17_UFSET | FRT8_MTSF | OCU8_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_29 | P3_20 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN404 (0x0328) | PPG9_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN405 (0x032A) | PPG9_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN406 (0x032C) | PPG10_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT17 | RLT17_UFSET | FRT8_MTSF | OCU8_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_29 | P3_20 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN407 (0x032E) | PPG10_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN408 (0x0330) | PPG10_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN409 (0x0332) | PPG11_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | TOT17 | RLT17_UFSET | FRT8_MTSF | OCU8_OTD0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_29 | P3_20 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN410 (0x0334) | PPG11_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN411 (0x0336) | PPG11_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN430 (0x035C) | PPG12_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_06 | P3_31 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN431 (0x035E) | PPG12_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN432 (0x0360) | PPG12_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN433 (0x0362) | PPG13_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_06 | P3_31 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN434 (0x0364) | PPG13_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN435 (0x0366) | PPG13_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN436 (0x0368) | PPG14_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_06 | P3_31 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN437 (0x036A) | PPG14_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN438 (0x036C) | PPG14_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN439 (0x036E) | PPG15_TIN1 | RESSEL (0-7) | PORT_PIN | TOT0 | RLT0_UFSET | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P2_06 | P3_31 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN440 (0x0370) | PPG15_TIN2 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN441 (0x0372) | PPG15_TIN3 | RESSEL (0-7) | set 0 | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN490 (0x03D4) | ADC12B0_HWTRG0 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU1_OTD0 | PPG0_TOUT0 | PPG1_TOUT2 | PPG3_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN491 (0x03D6) | ADC12B0_HWTRG1 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU2_OTD0 | PPG0_TOUT2 | PPG2_TOUT0 | PPG4_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN492 (0x03D8) | ADC12B0_HWTRG2 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU8_OTD0 | PPG1_TOUT0 | PPG2_TOUT2 | PPG4_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN493 (0x03DA) | ADC12B0_HWTRG3 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU9_OTD0 | PPG1_TOUT2 | PPG3_TOUT0 | PPG5_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN494 (0x03DC) | ADC12B0_HWTRG4 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU10_OTD0 | PPG2_TOUT0 | PPG3_TOUT2 | PPG5_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN495 (0x03DE) | ADC12B0_HWTRG5 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU0_OTD0 | PPG2_TOUT2 | PPG4_TOUT0 | PPG6_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN496 (0x03E0) | ADC12B0_HWTRG6 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU2_OTD0 | PPG3_TOUT0 | PPG4_TOUT2 | PPG6_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN497 (0x03E2) | ADC12B0_HWTRG7 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU8_OTD0 | PPG3_TOUT2 | PPG5_TOUT0 | PPG7_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN498 (0x03E4) | ADC12B0_HWTRG8 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU9_OTD0 | PPG4_TOUT0 | PPG5_TOUT2 | PPG7_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN499 (0x03E6) | ADC12B0_HWTRG9 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU10_OTD0 | PPG4_TOUT2 | PPG6_TOUT0 | PPG8_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN500 (0x03E8) | ADC12B0_HWTRG10 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU0_OTD0 | PPG5_TOUT0 | PPG6_TOUT2 | PPG8_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN501 (0x03EA) | ADC12B0_HWTRG11 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU1_OTD0 | PPG5_TOUT2 | PPG7_TOUT0 | PPG9_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN502 (0x03EC) | ADC12B0_HWTRG12 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU8_OTD0 | PPG6_TOUT0 | PPG7_TOUT2 | PPG9_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN503 (0x03EE) | ADC12B0_HWTRG13 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU9_OTD0 | PPG6_TOUT2 | PPG8_TOUT0 | PPG10_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN504 (0x03F0) | ADC12B0_HWTRG14 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU10_OTD0 | PPG7_TOUT0 | PPG8_TOUT2 | PPG10_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN505 (0x03F2) | ADC12B0_HWTRG15 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU0_OTD0 | PPG7_TOUT2 | PPG9_TOUT0 | PPG11_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN506 (0x03F4) | ADC12B0_HWTRG16 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU1_OTD0 | PPG8_TOUT0 | PPG9_TOUT2 | PPG11_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN507 (0x03F6) | ADC12B0_HWTRG17 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU2_OTD0 | PPG8_TOUT2 | PPG10_TOUT0 | PPG12_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN508 (0x03F8) | ADC12B0_HWTRG18 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU9_OTD0 | PPG9_TOUT0 | PPG10_TOUT2 | PPG12_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN509 (0x03FA) | ADC12B0_HWTRG19 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU10_OTD0 | PPG9_TOUT2 | PPG11_TOUT0 | PPG13_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN510 (0x03FC) | ADC12B0_HWTRG20 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU0_OTD0 | PPG10_TOUT0 | PPG11_TOUT2 | PPG13_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN511 (0x03FE) | ADC12B0_HWTRG21 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU1_OTD0 | PPG10_TOUT2 | PPG12_TOUT0 | PPG14_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN512 (0x0400) | ADC12B0_HWTRG22 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU2_OTD0 | PPG11_TOUT0 | PPG12_TOUT2 | PPG14_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN513 (0x0402) | ADC12B0_HWTRG23 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU8_OTD0 | PPG11_TOUT2 | PPG13_TOUT0 | PPG15_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN514 (0x0404) | ADC12B0_HWTRG24 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU10_OTD0 | PPG12_TOUT0 | PPG13_TOUT2 | PPG15_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN515 (0x0406) | ADC12B0_HWTRG25 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU0_OTD0 | PPG12_TOUT2 | PPG14_TOUT0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN516 (0x0408) | ADC12B0_HWTRG26 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU1_OTD0 | PPG13_TOUT0 | PPG14_TOUT2 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN517 (0x040A) | ADC12B0_HWTRG27 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU2_OTD0 | PPG13_TOUT2 | PPG15_TOUT0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN518 (0x040C) | ADC12B0_HWTRG28 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU8_OTD0 | PPG14_TOUT0 | PPG15_TOUT2 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN519 (0x040E) | ADC12B0_HWTRG29 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU9_OTD0 | PPG14_TOUT2 | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN520 (0x0410) | ADC12B0_HWTRG30 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU1_OTD0 | PPG15_TOUT0 | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN521 (0x0412) | ADC12B0_HWTRG31 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU2_OTD0 | PPG15_TOUT2 | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN522 (0x0414) | ADC12B0_HWTRG32 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU8_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN523 (0x0416) | ADC12B0_HWTRG33 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN524 (0x0418) | ADC12B0_HWTRG34 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN525 (0x041A) | ADC12B0_HWTRG35 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN526 (0x041C) | ADC12B0_HWTRG36 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU2_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN527 (0x041E) | ADC12B0_HWTRG37 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU8_OTD0 | - | - | |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN528 (0x0420) | ADC12B0_HWTRG38 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN529 (0x0422) | ADC12B0_HWTRG39 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN530 (0x0424) | ADC12B0_HWTRG40 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN531 (0x0426) | ADC12B0_HWTRG41 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU1_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN532 (0x0428) | ADC12B0_HWTRG42 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU8_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN533 (0x042A) | ADC12B0_HWTRG43 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN534 (0x042C) | ADC12B0_HWTRG44 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN535 (0x042E) | ADC12B0_HWTRG45 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN536 (0x0430) | ADC12B0_HWTRG46 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU1_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN537 (0x0432) | ADC12B0_HWTRG47 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU2_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN538 (0x0434) | ADC12B0_HWTRG48 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN539 (0x0436) | ADC12B0_HWTRG49 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN540 (0x0438) | ADC12B0_HWTRG50 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN541 (0x043A) | ADC12B0_HWTRG51 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU1_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN542 (0x043C) | ADC12B0_HWTRG52 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU2_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN543 (0x043E) | ADC12B0_HWTRG53 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU8_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN544 (0x0440) | ADC12B0_HWTRG54 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN545 (0x0442) | ADC12B0_HWTRG55 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN546 (0x0444) | ADC12B0_HWTRG56 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU1_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN547 (0x0446) | ADC12B0_HWTRG57 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU2_OTD0 | - | - | PPG0_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN548 (0x0448) | ADC12B0_HWTRG58 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU8_OTD0 | - | - | PPG0_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN549 (0x044A) | ADC12B0_HWTRG59 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU9_OTD0 | - | - | PPG1_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN550 (0x044C) | ADC12B0_HWTRG60 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU1_OTD0 | - | - | PPG1_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN551 (0x044E) | ADC12B0_HWTRG61 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU2_OTD0 | - | PPG0_TOUT0 | PPG2_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN552 (0x0450) | ADC12B0_HWTRG62 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU8_OTD0 | - | PPG0_TOUT2 | PPG2_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN553 (0x0452) | ADC12B0_HWTRG63 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU9_OTD0 | - | PPG1_TOUT0 | PPG3_OUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN554 (0x0454) | ADC12B1_HWTRG0 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU1_OTD0 | PPG0_TOUT0 | PPG1_TOUT2 | PPG3_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN555 (0x0456) | ADC12B1_HWTRG1 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU2_OTD0 | PPG0_TOUT2 | PPG2_TOUT0 | PPG4_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN556 (0x0458) | ADC12B1_HWTRG2 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU8_OTD0 | PPG1_TOUT0 | PPG2_TOUT2 | PPG4_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN557 (0x045A) | ADC12B1_HWTRG3 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU9_OTD0 | PPG1_TOUT2 | PPG3_TOUT0 | PPG5_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN558 (0x045C) | ADC12B1_HWTRG4 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU10_OTD0 | PPG2_TOUT0 | PPG3_TOUT2 | PPG5_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN559 (0x045E) | ADC12B1_HWTRG5 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU0_OTD0 | PPG2_TOUT2 | PPG4_TOUT0 | PPG6_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN560 (0x0460) | ADC12B1_HWTRG6 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU2_OTD0 | PPG3_TOUT0 | PPG4_TOUT2 | PPG6_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN561 (0x0462) | ADC12B1_HWTRG7 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU8_OTD0 | PPG3_TOUT2 | PPG5_TOUT0 | PPG7_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN562 (0x0464) | ADC12B1_HWTRG8 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU9_OTD0 | PPG4_TOUT0 | PPG5_TOUT2 | PPG7_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN563 (0x0466) | ADC12B1_HWTRG9 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU10_OTD0 | PPG4_TOUT2 | PPG6_TOUT0 | PPG8_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN564 (0x0468) | ADC12B1_HWTRG10 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU0_OTD0 | PPG5_TOUT0 | PPG6_TOUT2 | PPG8_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN565 (0x046A) | ADC12B1_HWTRG11 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU1_OTD0 | PPG5_TOUT2 | PPG7_TOUT0 | PPG9_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN566 (0x046C) | ADC12B1_HWTRG12 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU8_OTD0 | PPG6_TOUT0 | PPG7_TOUT2 | PPG9_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN567 (0x046E) | ADC12B1_HWTRG13 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU9_OTD0 | PPG6_TOUT2 | PPG8_TOUT0 | PPG10_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN568 (0x0470) | ADC12B1_HWTRG14 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU10_OTD0 | PPG7_TOUT0 | PPG8_TOUT2 | PPG10_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN569 (0x0472) | ADC12B1_HWTRG15 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU0_OTD0 | PPG7_TOUT2 | PPG9_TOUT0 | PPG11_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN570 (0x0474) | ADC12B1_HWTRG16 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU1_OTD0 | PPG8_TOUT0 | PPG9_TOUT2 | PPG11_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN571 (0x0476) | ADC12B1_HWTRG17 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU2_OTD0 | PPG8_TOUT2 | PPG10_TOUT0 | PPG12_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN572 (0x0478) | ADC12B1_HWTRG18 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU9_OTD0 | PPG9_TOUT0 | PPG10_TOUT2 | PPG12_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN573 (0x047A) | ADC12B1_HWTRG19 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU10_OTD0 | PPG9_TOUT2 | PPG11_TOUT0 | PPG13_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN574 (0x047C) | ADC12B1_HWTRG20 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU0_OTD0 | PPG10_TOUT0 | PPG11_TOUT2 | PPG13_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN575 (0x047E) | ADC12B1_HWTRG21 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU1_OTD0 | PPG10_TOUT2 | PPG12_TOUT0 | PPG14_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN576 (0x0480) | ADC12B1_HWTRG22 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU2_OTD0 | PPG11_TOUT0 | PPG12_TOUT2 | PPG14_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN577 (0x0482) | ADC12B1_HWTRG23 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU8_OTD0 | PPG11_TOUT2 | PPG13_TOUT0 | PPG15_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN578 (0x0484) | ADC12B1_HWTRG24 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU10_OTD0 | PPG12_TOUT0 | PPG13_TOUT2 | PPG15_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN579 (0x0486) | ADC12B1_HWTRG25 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU0_OTD0 | PPG12_TOUT2 | PPG14_TOUT0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN580 (0x0488) | ADC12B1_HWTRG26 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU1_OTD0 | PPG13_TOUT0 | PPG14_TOUT2 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN581 (0x048A) | ADC12B1_HWTRG27 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU2_OTD0 | PPG13_TOUT2 | PPG15_TOUT0 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN582 (0x048C) | ADC12B1_HWTRG28 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU8_OTD0 | PPG14_TOUT0 | PPG15_TOUT2 | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN583 (0x048E) | ADC12B1_HWTRG29 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU9_OTD0 | PPG14_TOUT2 | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN584 (0x0490) | ADC12B1_HWTRG30 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU1_OTD0 | PPG15_TOUT0 | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN585 (0x0492) | ADC12B1_HWTRG31 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU2_OTD0 | PPG15_TOUT2 | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN586 (0x0494) | ADC12B1_HWTRG32 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU8_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN587 (0x0496) | ADC12B1_HWTRG33 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN588 (0x0498) | ADC12B1_HWTRG34 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN589 (0x049A) | ADC12B1_HWTRG35 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN590 (0x049C) | ADC12B1_HWTRG36 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU2_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN591 (0x049E) | ADC12B1_HWTRG37 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU8_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN592 (0x04A0) | ADC12B1_HWTRG38 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN593 (0x04A2) | ADC12B1_HWTRG39 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN594 (0x04A4) | ADC12B1_HWTRG40 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN595 (0x04A6) | ADC12B1_HWTRG41 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU1_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN596 (0x04A8) | ADC12B1_HWTRG42 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU8_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN597 (0x04AA) | ADC12B1_HWTRG43 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN598 (0x04AC) | ADC12B1_HWTRG44 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN599 (0x04AE) | ADC12B1_HWTRG45 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU0_OTD0 | - | - | -- |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN600 (0x04B0) | ADC12B1_HWTRG46 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU1_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN601 (0x04B2) | ADC12B1_HWTRG47 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU2_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN602 (0x04B4) | ADC12B1_HWTRG48 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN603 (0x04B6) | ADC12B1_HWTRG49 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN604 (0x04B8) | ADC12B1_HWTRG50 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN605 (0x04BA) | ADC12B1_HWTRG51 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU1_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN606 (0x04BC) | ADC12B1_HWTRG52 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT16_UFSET | OCU9_OTD0 | OCU2_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN607 (0x04BE) | ADC12B1_HWTRG53 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT17_UFSET | OCU10_OTD0 | OCU8_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN608 (0x04C0) | ADC12B1_HWTRG54 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT0_UFSET | OCU0_OTD0 | OCU10_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN609 (0x04C2) | ADC12B1_HWTRG55 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT1_UFSET | OCU1_OTD0 | OCU0_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN610 (0x04C4) | ADC12B1_HWTRG56 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU1_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN611 (0x04C6) | ADC12B1_HWTRG57 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU2_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN612 (0x04C8) | ADC12B1_HWTRG58 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT1_UFSET | OCU9_OTD0 | OCU8_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN613 (0x04CA) | ADC12B1_HWTRG59 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT16_UFSET | OCU10_OTD0 | OCU9_OTD0 | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN614 (0x04CC) | ADC12B1_HWTRG60 | RESSEL (0-7) | PORT_PIN | RLT0_UFSET | RLT1_UFSET | OCU0_OTD0 | OCU1_OTD0 | - | - | PPG1_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN615 (0x04CE) | ADC12B1_HWTRG61 | RESSEL (0-7) | PORT_PIN | RLT1_UFSET | RLT16_UFSET | OCU1_OTD0 | OCU2_OTD0 | - | PPG0_TOUT0 | PPG2_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN616 (0x04D0) | ADC12B1_HWTRG62 | RESSEL (0-7) | PORT_PIN | RLT16_UFSET | RLT17_UFSET | OCU2_OTD0 | OCU8_OTD0 | - | PPG0_TOUT2 | PPG2_TOUT2 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN617 (0x04D2) | ADC12B1_HWTRG63 | RESSEL (0-7) | PORT_PIN | RLT17_UFSET | RLT0_UFSET | OCU8_OTD0 | OCU9_OTD0 | - | PPG1_TOUT0 | PPG3_TOUT0 |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN626 (0x04E4) | DDRHSSPI_MSTART | RESSEL (0-7) | - | TOT0 | TOT16 | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN629 (0x04EA) | MDIO | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_31 | P3_06 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN630 (0x04EC) | CRS | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_02 | P0_20 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN631 (0x04EE) | RXD0 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_27 | P3_04 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN632 (0x04F0) | RXD1 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_28 | P4_06 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN633 (0x04F2) | RXD2 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_29 | P4_07 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN634 (0x04F4) | RXD3 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_30 | P3_05 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN635 (0x04F6) | COL | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_01 | P0_19 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN636 (0x04F8) | RXDV | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_19 | P4_02 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN637 (0x04FA) | RXER | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_18 | P4_01 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN638 (0x04FC) | RXCLK | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_17 | P4_00 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN639 (0x04FE) | TXCLK | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_20 | P4_03 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN643 (0x0506) | I2S0_WS | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_12 | P3_26 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN644 (0x0508) | I2S0_SD | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_11 | P3_25 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN645 (0x050A) | I2S0_SCK | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_13 | P3_27 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

| Register (Offset) | Resource | RESSEL [3:0] /PORT SEL[3:0] | Source for Resource Input | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| RIC_RESIN646 (0x050C) | I2S0_ECLK | RESSEL (0-7) | PORT_PIN | SYSC1_CLK_CD4 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P0_10 | P3_24 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN650 (0x0514) | I2S1_ECLK | RESSEL (0-7) | PORT_PIN | SYSC1_CLK_CD4 | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | - | - | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN685 (0x055A) | ADTRG0 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P1_16 | P2_10 | - | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |
| RIC_RESIN686 (0x055C) | ADTRG1 | RESSEL (0-7) | - | - | - | - | - | - | - | - |
| | | RESSEL (8-15) | - | - | - | - | - | - | - | - |
| | | PORTSEL (0-7) | P4_22 | P1_08 | P2_11 | - | - | - | - | - |
| | | PORTSEL (8-15) | - | - | - | - | - | - | - | - |

***Notes:***

- *When both GPIO_PORTEN.GPORTEN and PPC_PCFGR.PIE are configured as 0, the input signal is disconnected and external interrupt cannot be detected. During disconnecting, I/O internally outputs "low" to internal logic, and if ELVR is configured as low-level-detection, falling-edge-detection, or both-edge-detection it will be detected as external interrupt with EIRR = 1.*
- *"Set 0" (Set 1) means that "0" ("1") is inputted.*
- *OCUx_MODn is described as MODn pin in Traveo™ Platform Hardware Manual.*

## 7.2 Port Output Function Configuration

The port output function configuration (POF) is a function to select a function to output to a port.

A resource which supports a port output relocation has its PPC_PCFGR.POF to configure resource output.

### *7.2.1 Standard Configuration (S6J3310)*

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR000 (0x0000) | P0_00 | GPIO_PODR0:POD00 | - | LCDD5 | - | - | DSP0_R7_0 | - | MAD1 |
| PPC_PCFGR001 (0x0002) | P0_01 | GPIO_PODR0:POD01 | - | LCDD6 | ARH0_AIC1_DNCLK | - | DSP0_G0_0 | - | MAD2 |
| PPC_PCFGR002 (0x0004) | P0_02 | GPIO_PODR0:POD02 | SCK1_0 | LCDD7 | ARH0_AIC1_TDA1 | ARH0_AIC1_DNDATA1 | DSP0_G1_0 | SCL1 | MAD3 |
| PPC_PCFGR003 (0x0006) | P0_03 | GPIO_PODR0:POD03 | SOT1_0 | LCDD8 | ARH0_AIC1_dbg_out_1 | - | DSP0_G2_0 | SDA1 | MAD4 |
| PPC_PCFGR004 (0x0008) | P0_04 | GPIO_PODR0:POD04 | SCS10_0 | LCDD9 | ARH0_AIC1_dbg_out_0 | - | DSP0_G3_0 | - | MAD5 |
| PPC_PCFGR005 (0x000A) | P0_05 | GPIO_PODR0:POD05 | SCS11_0 | LCDD10 | ARH0_AIC1_TDA0 | ARH0_AIC1_DNDATA0 | DSP0_G4_0 | SOT0_1 | MAD6 |
| PPC_PCFGR006 (0x000C) | P0_06 | GPIO_PODR0:POD06 | SCS12_0 | LCDD11 | SCK0_1 | - | DSP0_G5_0 | PPG0_TOUT0_1 | MAD7 |
| PPC_PCFGR007 (0x000E) | P0_07 | GPIO_PODR0:POD07 | SCS13_0 | LCDD12 | SCS00_1 | I2S1_SD_0 | DSP0_G6_0 | PPG0_TOUT2_1 | MAD8 |
| PPC_PCFGR008 (0x0010) | P0_08 | GPIO_PODR0:POD08 | - | LCDD13 | - | I2S1_WS_0 | DSP0_G7_0 | PPG1_TOUT0_1 | MAD9 |
| PPC_PCFGR009 (0x0012) | P0_09 | GPIO_PODR0:POD09 | - | LCDD14 | ARH0_AIC0_DNCLK | I2S1_SCK_0 | DSP0_B0_0 | PPG1_TOUT2_1 | MAD10 |
| PPC_PCFGR010 (0x0014) | P0_10 | GPIO_PODR0:POD10 | SCS171_1 | LCDD15 | ARH0_AIC0_TDA1 | ARH0_AIC0_DNDATA1 | DSP0_B1_0 | PPG2_TOUT0_1 | MAD11 |
| PPC_PCFGR011 (0x0016) | P0_11 | GPIO_PODR0:POD11 | - | LCDD16 | ARH0_AIC0_dbg_out_1 | I2S0_SD_0 | DSP0_B2_0 | PPG2_TOUT2_1 | MAD12 |
| PPC_PCFGR012 (0x0018) | P0_12 | GPIO_PODR0:POD12 | - | LCDD17 | ARH0_AIC0_dbg_out_0 | I2S0_WS_0 | DSP0_B3_0 | PPG3_TOUT0_1 | MAD13 |
| PPC_PCFGR013 (0x001A) | P0_13 | GPIO_PODR0:POD13 | - | CS# | - | I2S0_SCK_0 | DSP0_B4_0 | PPG3_TOUT2_1 | MAD14 |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR014 (0x001C) | P0_14 | GPIO_PODR0:POD14 | - | WR# | - | - | DSP0_B5_0 | SCK4_1 | MOEX |
| PPC_PCFGR015 (0x001E) | P0_15 | GPIO_PODR0:POD15 | - | RD# | - | - | DSP0_B6_0 | SCS40_1 | MWEX |
| PPC_PCFGR016 (0x0020) | P0_16 | GPIO_PODR0:POD16 | DSP0_B7_1 | - | ARH0_AIC0_TDA0 | ARH0_AIC0_DNDATA0 | - | SCS41_1 | MCLK |
| PPC_PCFGR017 (0x0022) | P0_17 | GPIO_PODR0:POD17 | - | - | - | - | DSP0_B7_0 | SCS43_1 | MDQM0 |
| PPC_PCFGR018 (0x0024) | P0_18 | GPIO_PODR0:POD18 | - | RS | - | MDC_1 | - | - | MCSX2 |
| PPC_PCFGR019 (0x0026) | P0_19 | GPIO_PODR0:POD19 | - | RES# | - | - | - | - | MCSX3 |
| PPC_PCFGR020 (0x0028) | P0_20 | GPIO_PODR0:POD20 | - | - | - | - | - | - | - |
| PPC_PCFGR021 (0x002A) | P0_21 | GPIO_PODR0:POD21 | - | M_SDATA0_0 | TXEN_0 | M_DQ3 | - | - | - |
| PPC_PCFGR022 (0x002C) | P0_22 | GPIO_PODR0:POD22 | SCK2_0 | M_SDATA0_2 | TXD0_0 | M_DQ2 | SOT9_2 | - | - |
| PPC_PCFGR023 (0x002E) | P0_23 | GPIO_PODR0:POD23 | SOT2_0 | M_SDATA0_1 | TXD1_0 | M_DQ1 | SCK9_2 | - | - |
| PPC_PCFGR024 (0x0030) | P0_24 | GPIO_PODR0:POD24 | SCS20_0 | M_SSEL0 | TXD2_0 | M_DQ0 | SCS90_2 | - | - |
| PPC_PCFGR025 (0x0032) | P0_25 | GPIO_PODR0:POD25 | SCS21_0 | M_SDATA0_3 | TXD3_0 | M_CS#_1 | SCS91_2 | - | - |
| PPC_PCFGR026 (0x0034) | P0_26 | GPIO_PODR0:POD26 | SCS22_0 | M_SCLK0 | TXER_0 | M_CK | - | - | - |
| PPC_PCFGR027 (0x0036) | P0_27 | GPIO_PODR0:POD27 | SCS23_0 | M_SDATA1_0 | - | M_RWDS | - | - | - |
| PPC_PCFGR028 (0x0038) | P0_28 | GPIO_PODR0:POD28 | - | M_SDATA1_2 | - | M_DQ4 | SCK8_2 | - | - |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR029 (0x003A) | P0_29 | GPIO_PODR0:POD29 | SCK3_0 | M_SDATA1_1 | - | M_DQ5 | SOT8_2 | - | - |
| PPC_PCFGR030 (0x003C) | P0_30 | GPIO_PODR0:POD30 | SOT3_0 | M_SSEL1 | - | M_DQ6 | SCS80_2 | - | - |
| PPC_PCFGR031 (0x003E) | P0_31 | GPIO_PODR0:POD31 | SCS30_0 | M_SDATA1_3 | MDIO_0 | M_DQ7 | - | - | - |
| PPC_PCFGR100 (0x0040) | P1_00 | GPIO_PODR1:POD00 | SCS31_0 | - | MDC_0 | M_CS#_2 | - | - | - |
| PPC_PCFGR101 (0x0042) | P1_01 | GPIO_PODR1:POD01 | SCS32_0 | - | - | - | - | - | MLBSIG |
| PPC_PCFGR102 (0x0044) | P1_02 | GPIO_PODR1:POD02 | SCS33_0 | - | - | - | - | - | MLBDAT |
| PPC_PCFGR103 (0x0046) | P1_03 | GPIO_PODR1:POD03 | - | - | - | OCU0_OTD0_0 | - | PPG0_TOUT0_0 | BN0(BL0) |
| PPC_PCFGR104 (0x0048) | P1_04 | GPIO_PODR1:POD04 | SCK0_0 | - | SCL0 | OCU0_OTD1_0 | TOT0_0 | PPG0_TOUT2_0 | BP0(BH0) |
| PPC_PCFGR105 (0x004A) | P1_05 | GPIO_PODR1:POD05 | SOT0_0 | SGA0_0 | SDA0 | TRACE0_0 | - | PPG1_TOUT0_0 | AN0(AL0) |
| PPC_PCFGR106 (0x004C) | P1_06 | GPIO_PODR1:POD06 | SCS00_0 | SGO0_0 | TX0_0 | TRACE1_0 | TOT1_0 | PPG1_TOUT2_0 | AP0(AH0) |
| PPC_PCFGR107 (0x004E) | P1_07 | GPIO_PODR1:POD07 | - | SGA1_0 | TRACE2_0 | OCU1_OTD0_0 | - | PPG2_TOUT0_0 | BN1(BL1) |
| PPC_PCFGR108 (0x0050) | P1_08 | GPIO_PODR1:POD08 | TRACE3_0 | SGO1_0 | TX1_0 | OCU1_OTD1_0 | TOT16_0 | PPG2_TOUT2_0 | BP1(BH1) |
| PPC_PCFGR109 (0x0052) | P1_09 | GPIO_PODR1:POD09 | SCK16_0 | SGA2_0 | SCL16 | OCU2_OTD0_0 | TRACE_CTL_0 | PPG3_TOUT0_0 | AN1(AL1) |
| PPC_PCFGR110 (0x0054) | P1_10 | GPIO_PODR1:POD10 | SOT16_0 | SGO2_0 | SDA16 | OCU2_OTD1_0 | TRACE_CLK_0 | PPG3_TOUT2_0 | AP1(AH1) |
| PPC_PCFGR111 (0x0056) | P1_11 | GPIO_PODR1:POD11 | SCS160_0 | INDICATOR0_0 | - | OCU8_OTD0_0 | - | PPG4_TOUT0_0 | - |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR112 (0x0058) | P1_12 | GPIO_PODR1:POD12 | SCS161_0 | - | - | OCU8_OTD1_0 | TOT17_0 | PPG4_TOUT2_0 | TX2_0 |
| PPC_PCFGR113 (0x005A) | P1_13 | GPIO_PODR1:POD13 | - | SGA3_0 | - | OCU9_OTD0_0 | - | - | - |
| PPC_PCFGR114 (0x005C) | P1_14 | GPIO_PODR1:POD14 | SYSC0_CLK_1 | SGO3_0 | - | OCU9_OTD1_0 | TOT48_0 | PPG5_TOUT0_0 | TX3_0 |
| PPC_PCFGR115 (0x005E) | P1_15 | GPIO_PODR1:POD15 | SCK17_0 | SGA4_0 | SCL17 | OCU10_OTD0_0 | SCK12_1 | PPG5_TOUT2_0 | INDICATOR0_1 |
| PPC_PCFGR116 (0x0060) | P1_16 | GPIO_PODR1:POD16 | SOT17_0 | SGO4_0 | SDA17 | OCU10_OTD1_0 | TOT49_0 | SYSC0_CLK_0 | WOT |
| PPC_PCFGR117 (0x0062) | P1_17 | GPIO_PODR1:POD17 | SCS170_0 | - | - | - | PWM1P0 | PPG6_TOUT0_0 | - |
| PPC_PCFGR118 (0x0064) | P1_18 | GPIO_PODR1:POD18 | SCS171_0 | - | - | - | PWM1M0 | PPG6_TOUT2_0 | TX5_0 |
| PPC_PCFGR119 (0x0066) | P1_19 | GPIO_PODR1:POD19 | - | - | - | - | PWM2P0 | PPG7_TOUT0_0 | - |
| PPC_PCFGR120 (0x0068) | P1_20 | GPIO_PODR1:POD20 | SCK8_0 | - | SCL8 | - | PWM2M0 | PPG7_TOUT2_0 | - |
| PPC_PCFGR121 (0x006A) | P1_21 | GPIO_PODR1:POD21 | SOT8_0 | - | SDA8 | - | PWM1P1 | PPG8_TOUT0_0 | - |
| PPC_PCFGR122 (0x006C) | P1_22 | GPIO_PODR1:POD22 | SCS80_0 | - | - | - | PWM1M1 | PPG8_TOUT2_0 | TX6_0 |
| PPC_PCFGR123 (0x006E) | P1_23 | GPIO_PODR1:POD23 | - | - | - | - | PWM2P1 | PPG9_TOUT0_0 | - |
| PPC_PCFGR124 (0x0070) | P1_24 | GPIO_PODR1:POD24 | SCK9_0 | - | SCL9 | - | PWM2M1 | PPG9_TOUT2_0 | - |
| PPC_PCFGR125 (0x0072) | P1_25 | GPIO_PODR1:POD25 | SOT9_0 | - | SDA9 | - | PWM1P2 | PPG10_TOUT0_0 | - |
| PPC_PCFGR126 (0x0074) | P1_26 | GPIO_PODR1:POD26 | SCS90_0 | - | - | - | PWM1M2 | PPG10_TOUT2_0 | - |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR127 (0x0076) | P1_27 | GPIO_PODR1:POD27 | SCS91_0 | - | - | - | PWM2P2 | PPG11_TOUT0_0 | - |
| PPC_PCFGR128 (0x0078) | P1_28 | GPIO_PODR1:POD28 | - | - | - | - | PWM2M2 | PPG11_TOUT2_0 | - |
| PPC_PCFGR129 (0x007A) | P1_29 | GPIO_PODR1:POD29 | SCK10_0 | - | SCL10 | - | PWM1P3 | - | - |
| PPC_PCFGR130 (0x007C) | P1_30 | GPIO_PODR1:POD30 | SOT10_0 | - | SDA10 | - | PWM1M3 | PPG12_TOUT0_0 | - |
| PPC_PCFGR131 (0x007E) | P1_31 | GPIO_PODR1:POD31 | SCS100_0 | - | - | - | PWM2P3 | PPG12_TOUT2_0 | - |
| PPC_PCFGR200 (0x0080) | P2_00 | GPIO_PODR2:POD00 | - | - | - | - | PWM2M3 | PPG13_TOUT0_0 | - |
| PPC_PCFGR201 (0x0082) | P2_01 | GPIO_PODR2:POD01 | SCK11_0 | - | SCL11 | - | PWM1P4 | PPG13_TOUT2_0 | - |
| PPC_PCFGR202 (0x0084) | P2_02 | GPIO_PODR2:POD02 | SOT11_0 | - | SDA11 | - | PWM1M4 | PPG14_TOUT0_0 | - |
| PPC_PCFGR203 (0x0086) | P2_03 | GPIO_PODR2:POD03 | SCS110_0 | - | - | - | PWM2P4 | PPG14_TOUT2_0 | - |
| PPC_PCFGR204 (0x0088) | P2_04 | GPIO_PODR2:POD04 | SCS111_0 | - | - | - | PWM2M4 | PPG15_TOUT0_0 | - |
| PPC_PCFGR205 (0x008A) | P2_05 | GPIO_PODR2:POD05 | - | - | - | - | PWM1P5 | PPG15_TOUT2_0 | - |
| PPC_PCFGR206 (0x008C) | P2_06 | GPIO_PODR2:POD06 | SCK12_0 | - | SCL12 | - | PWM1M5 | - | - |
| PPC_PCFGR207 (0x008E) | P2_07 | GPIO_PODR2:POD07 | SOT12_0 | - | SDA12 | - | PWM2P5 | - | - |
| PPC_PCFGR208 (0x0090) | P2_08 | GPIO_PODR2:POD08 | SCS120_0 | - | - | - | PWM2M5 | - | - |
| PPC_PCFGR209 (0x0092) | P2_09 | GPIO_PODR2:POD09 | SCS23_1 | - | - | - | DSP0_EN_0 | PPG14_TOUT0_1 | MCSX0 |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR210 (0x0094) | P2_10 | GPIO_PODR2:POD10 | SCS31_1 | - | - | - | DSP0_HSYNC_0 | - | MCSX1 |
| PPC_PCFGR211 (0x0096) | P2_11 | GPIO_PODR2:POD11 | SCS32_1 | - | - | - | DSP0_VSYNC_0 | - | MDATA0 |
| PPC_PCFGR212 (0x0098) | P2_12 | GPIO_PODR2:POD12 | SCS33_1 | - | - | - | DSP0_CLK_0 | - | MDATA1 |
| PPC_PCFGR213 (0x009A) | P2_13 | GPIO_PODR2:POD13 | - | - | - | - | DSP0_R0_0 | - | MDATA2 |
| PPC_PCFGR214 (0x009C) | P2_14 | GPIO_PODR2:POD14 | SCK4_0 | - | SCL4 | - | DSP0_R1_0 | - | MDATA3 |
| PPC_PCFGR215 (0x009E) | P2_15 | GPIO_PODR2:POD15 | SOT4_0 | LCDD0 | SDA4 | - | DSP0_R2_0 | - | MDATA4 |
| PPC_PCFGR216 (0x00A0) | P2_16 | GPIO_PODR2:POD16 | SCS40_0 | LCDD1 | - | - | DSP0_R3_0 | - | MDATA5 |
| PPC_PCFGR217 (0x00A2) | P2_17 | GPIO_PODR2:POD17 | SCS41_0 | LCDD2 | - | - | DSP0_R4_0 | - | MDATA6 |
| PPC_PCFGR218 (0x00A4) | P2_18 | GPIO_PODR2:POD18 | SCS42_0 | LCDD3 | - | - | DSP0_R5_0 | - | MDATA7 |
| PPC_PCFGR219 (0x00A6) | P2_19 | GPIO_PODR2:POD19 | SCS43_0 | LCDD4 | - | - | DSP0_R6_0 | - | MAD0 |
| PPC_PCFGR300 (0x00C0) | P3_00 | GPIO_PODR3:POD00 | - | TXD1_1 | - | - | - | PPG4_TOUT0_1 | MAD15 |
| PPC_PCFGR301 (0x00C2) | P3_01 | GPIO_PODR3:POD01 | SCK1_1 | TXD2_1 | - | - | - | PPG4_TOUT2_1 | MAD16 |
| PPC_PCFGR302 (0x00C4) | P3_02 | GPIO_PODR3:POD02 | SOT1_1 | TXD3_1 | - | - | - | PPG5_TOUT0_1 | MAD17 |
| PPC_PCFGR303 (0x00C6) | P3_03 | GPIO_PODR3:POD03 | SCS10_1 | TXER_1 | - | - | - | PPG5_TOUT2_1 | MAD18 |
| PPC_PCFGR304 (0x00C8) | P3_04 | GPIO_PODR3:POD04 | SCS11_1 | - | - | - | - | - | MAD19 |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR305 (0x00CA) | P3_05 | GPIO_PODR3:POD05 | SCS12_1 | - | - | - | - | - | MAD20 |
| PPC_PCFGR306 (0x00CC) | P3_06 | GPIO_PODR3:POD06 | SCS13_1 | MDIO_1 | - | - | - | SOT4_1 | MAD21 |
| PPC_PCFGR307 (0x00CE) | P3_07 | GPIO_PODR3:POD07 | - | - | - | - | - | SCS42_1 | MDQM1 |
| PPC_PCFGR308 (0x00D0) | P3_08 | GPIO_PODR3:POD08 | - | SGA0_1 | PPG6_TOUT0_1 | OCU0_OTD0_1 | - | - | - |
| PPC_PCFGR309 (0x00D2) | P3_09 | GPIO_PODR3:POD09 | SCK8_1 | SGO0_1 | PPG6_TOUT2_1 | OCU0_OTD1_1 | TOT0_1 | - | - |
| PPC_PCFGR310 (0x00D4) | P3_10 | GPIO_PODR3:POD10 | SOT8_1 | SGA1_1 | PPG7_TOUT0_1 | OCU1_OTD0_1 | TRACE0_1 | - | TX0_1 |
| PPC_PCFGR311 (0x00D6) | P3_11 | GPIO_PODR3:POD11 | SCS80_1 | SGO1_1 | PPG7_TOUT2_1 | OCU1_OTD1_1 | TOT1_1 | TRACE1_1 | - |
| PPC_PCFGR312 (0x00D8) | P3_12 | GPIO_PODR3:POD12 | - | SGA2_1 | PPG8_TOUT0_1 | OCU2_OTD0_1 | - | TRACE2_1 | TX1_1 |
| PPC_PCFGR313 (0x00DA) | P3_13 | GPIO_PODR3:POD13 | SCK10_1 | SGO2_1 | PPG8_TOUT2_1 | OCU2_OTD1_1 | TOT16_1 | TRACE3_1 | - |
| PPC_PCFGR314 (0x00DC) | P3_14 | GPIO_PODR3:POD14 | SOT10_1 | SGA3_1 | PPG9_TOUT0_1 | OCU8_OTD0_1 | - | TRACE_CTL_1 | - |
| PPC_PCFGR315 (0x00DE) | P3_15 | GPIO_PODR3:POD15 | SCS100_1 | SGO3_1 | PPG9_TOUT2_1 | OCU8_OTD1_1 | TOT17_1 | TRACE_CLK_1 | TX2_1 |
| PPC_PCFGR316 (0x00E0) | P3_16 | GPIO_PODR3:POD16 | - | SGA4_1 | PPG10_TOUT0_1 | OCU9_OTD0_1 | - | - | - |
| PPC_PCFGR317 (0x00E2) | P3_17 | GPIO_PODR3:POD17 | - | SGO4_1 | PPG10_TOUT2_1 | OCU9_OTD1_1 | TOT48_1 | - | TX3_1 |
| PPC_PCFGR318 (0x00E4) | P3_18 | GPIO_PODR3:POD18 | - | - | PPG11_TOUT0_1 | OCU10_OTD0_1 | - | - | - |
| PPC_PCFGR319 (0x00E6) | P3_19 | GPIO_PODR3:POD19 | SCK9_1 | - | PPG11_TOUT2_1 | OCU10_OTD1_1 | - | - | - |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR320 (0x00E8) | P3_20 | GPIO_PODR3:POD20 | SOT9_1 | - | - | - | - | - | TX5_1 |
| PPC_PCFGR321 (0x00EA) | P3_21 | GPIO_PODR3:POD21 | SCS90_1 | - | - | - | TOT49_1 | - | - |
| PPC_PCFGR322 (0x00EC) | P3_22 | GPIO_PODR3:POD22 | SCS91_1 | - | - | - | - | - | - |
| PPC_PCFGR323 (0x00EE) | P3_23 | GPIO_PODR3:POD23 | - | - | - | - | SCS120_1 | - | TX6_1 |
| PPC_PCFGR324 (0x00F0) | P3_24 | GPIO_PODR3:POD24 | SOT2_1 | - | - | - | - | PPG12_TOUT0_1 | MDATA8 |
| PPC_PCFGR325 (0x00F2) | P3_25 | GPIO_PODR3:POD25 | SCS20_1 | - | - | - | I2S0_SD_1 | PPG12_TOUT2_1 | MDATA9 |
| PPC_PCFGR326 (0x00F4) | P3_26 | GPIO_PODR3:POD26 | SCS21_1 | - | - | - | I2S0_WS_1 | PPG13_TOUT0_1 | MDATA10 |
| PPC_PCFGR327 (0x00F6) | P3_27 | GPIO_PODR3:POD27 | SCS22_1 | - | - | - | I2S0_SCK_1 | PPG13_TOUT2_1 | MDATA11 |
| PPC_PCFGR328 (0x00F8) | P3_28 | GPIO_PODR3:POD28 | - | - | - | - | - | PPG14_TOUT2_1 | MDATA12 |
| PPC_PCFGR329 (0x00FA) | P3_29 | GPIO_PODR3:POD29 | SCK3_1 | - | - | - | - | PPG15_TOUT0_1 | MDATA13 |
| PPC_PCFGR330 (0x00FC) | P3_30 | GPIO_PODR3:POD30 | SOT3_1 | - | - | - | - | PPG15_TOUT2_1 | MDATA14 |
| PPC_PCFGR331 (0x00FE) | P3_31 | GPIO_PODR3:POD31 | SCS30_1 | - | - | - | - | - | MDATA15 |
| PPC_PCFGR400 (0x0100) | P4_00 | GPIO_PODR4:POD00 | - | - | - | - | - | - | - |
| PPC_PCFGR401 (0x0102) | P4_01 | GPIO_PODR4:POD01 | - | - | - | - | TX0_2 | - | - |
| PPC_PCFGR402 (0x0104) | P4_02 | GPIO_PODR4:POD02 | - | - | - | - | - | - | - |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR403 (0x0106) | P4_03 | GPIO_PODR4:POD03 | - | - | SCS170_1 | - | - | - | - |
| PPC_PCFGR404 (0x0108) | P4_04 | GPIO_PODR4:POD04 | - | TXEN_1 | SCK17_1 | - | TX3_2 | - | - |
| PPC_PCFGR405 (0x010A) | P4_05 | GPIO_PODR4:POD05 | - | TXD0_1 | SOT17_1 | - | - | - | - |
| PPC_PCFGR406 (0x010C) | P4_06 | GPIO_PODR4:POD06 | - | - | - | - | - | - | - |
| PPC_PCFGR407 (0x010E) | P4_07 | GPIO_PODR4:POD07 | - | - | - | - | - | - | - |
| PPC_PCFGR408 (0x0110) | P4_08 | GPIO_PODR4:POD08 | - | - | - | - | - | - | - |
| PPC_PCFGR409 (0x0112) | P4_09 | GPIO_PODR4:POD09 | - | - | - | - | - | - | - |
| PPC_PCFGR410 (0x0114) | P4_10 | GPIO_PODR4:POD10 | - | - | - | - | - | - | - |
| PPC_PCFGR411 (0x0116) | P4_11 | GPIO_PODR4:POD11 | - | - | - | - | - | - | - |
| PPC_PCFGR412 (0x0118) | P4_12 | GPIO_PODR4:POD12 | - | - | - | - | - | - | - |
| PPC_PCFGR413 (0x011A) | P4_13 | GPIO_PODR4:POD13 | - | - | - | - | - | - | - |
| PPC_PCFGR414 (0x011C) | P4_14 | GPIO_PODR4:POD14 | - | - | - | - | - | - | - |
| PPC_PCFGR415 (0x011E) | P4_15 | GPIO_PODR4:POD15 | - | - | - | - | - | - | - |
| PPC_PCFGR416 (0x0120) | P4_16 | GPIO_PODR4:POD16 | - | - | - | - | - | - | - |
| PPC_PCFGR417 (0x0122) | P4_17 | GPIO_PODR4:POD17 | - | - | - | - | SOT12_1 | - | - |

| Register (Offset) | Port | Resource Functional Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | POF = 0 | POF = 1 | POF = 2 | POF = 3 | POF = 4 | POF = 5 | POF = 6 | POF = 7 |
| PPC_PCFGR418 (0x0124) | P4_18 | GPIO_PODR4:POD18 | - | - | - | - | - | - | - |
| PPC_PCFGR419 (0x0126) | P4_19 | GPIO_PODR4:POD19 | - | - | - | - | - | - | - |
| PPC_PCFGR420 (0x0128) | P4_20 | GPIO_PODR4:POD20 | - | - | - | - | SOT16_1 | - | - |
| PPC_PCFGR421 (0x012A) | P4_21 | GPIO_PODR4:POD21 | - | - | - | - | SCK16_1 | - | - |
| PPC_PCFGR422 (0x012C) | P4_22 | GPIO_PODR4:POD22 | - | - | - | - | SCS161_1 | - | - |
| PPC_PCFGR423 (0x012E) | P4_23 | GPIO_PODR4:POD23 | - | - | - | - | SCS160_1 | - | - |
| PPC_PCFGR424 (0x0130) | P4_24 | GPIO_PODR4:POD24 | - | - | - | - | - | - | - |
| PPC_PCFGR425 (0x0132) | P4_25 | GPIO_PODR4:POD25 | - | - | - | - | - | - | - |
| PPC_PCFGR426 (0x0134) | P4_26 | GPIO_PODR4:POD26 | - | - | - | - | - | - | - |
| PPC_PCFGR427 (0x0136) | P4_27 | GPIO_PODR4:POD27 | - | - | - | - | - | - | - |
| PPC_PCFGR428 (0x0138) | P4_28 | GPIO_PODR4:POD28 | - | - | - | - | - | - | - |
| PPC_PCFGR429 (0x013A) | P4_29 | GPIO_PODR4:POD29 | - | - | - | - | - | - | - |
| PPC_PCFGR430 (0x013C) | P4_30 | GPIO_PODR4:POD30 | - | - | - | - | - | - | - |
| PPC_PCFGR431 (0x013E) | P4_31 | GPIO_PODR4:POD31 | SCK2_1 | - | - | - | - | - | - |

***Notes:***

- *The hyphen indicates that setting is prohibited. If setting the port will be operated as input independent on the register value of the GPIO_DDR.*
- The register for P0_20 for POF exists though the port only supports input not supports output. The configuration of POF = 0 for the port does not affect anything.

# 8. Precautions and Handling Devices

## 8.1 Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

### *8.1.1 Precautions for Product Design*

This section describes precautions when designing electronic equipment using semiconductor devices.

#### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, and so on.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

### *8.1.2 Precautions for Package Mounting*

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

#### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

#### Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

#### Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

#### Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70 % relative humidity, and at temperatures between 5 ˚C and 30 ˚C. When you open Dry Package that recommends humidity 40 % to 70 % relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

#### Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 ˚C/24 h

#### Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40 % and 70 %.
Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

### *8.1.3 Precautions for Use Environment*

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

## 8.2 Handling Devices

### For Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than VCC or lower than VSS; or the voltage applied between a VCC pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Also be careful that analog power supplies (AVCC5,AVRH5) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times.
The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (VCC) and analog supply voltages (AVCC5,AVRH5), or turn on the digital supply voltage (VCC) and then the analog supply voltages (AVCC5,AVRH5).

### About Handling Unused Pins

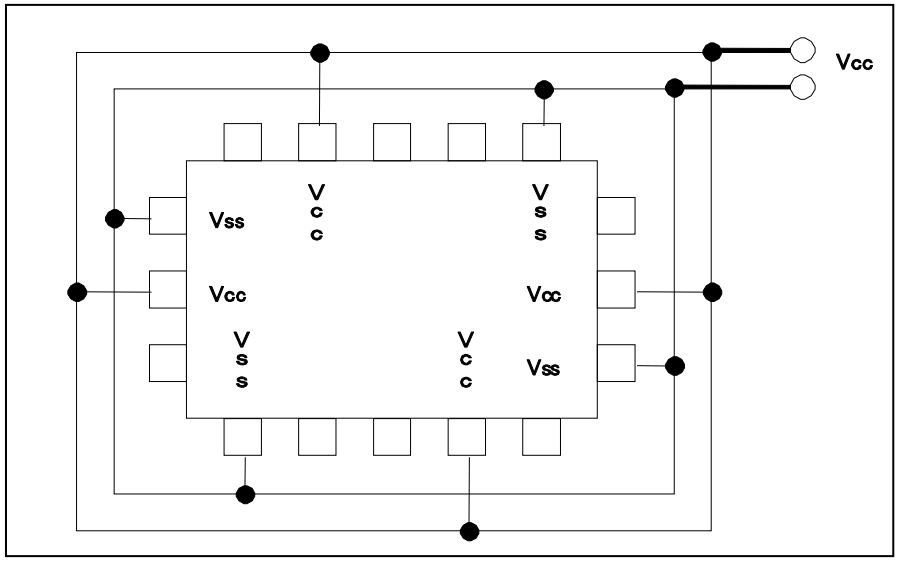
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures for unused pins, such as pulling up or pulling down the voltage with resistors of 2 kilo ohms or higher.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

### About Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins that should be at the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the VCC and VSS pins to the power source and ground externally. Also handle all the VSS power supply pins in this way as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

**Figure 8-1 Pin Assignment**




In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

We recommend connecting a ceramic capacitor as a bypass capacitor between VCC and VSS, near this device.

### About the Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

### About the Mode Pin (MODE)

Use mode pin MODE by directly connecting it to a VCC or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC or VSS pin on the printed circuit board, and connect them with low impedance.

### About the Power-on Time

To prevent the internal built-in voltage step-down circuit from malfunctioning, secure a voltage rising time of 50 µs (between 0.2 V and 2.7 V) or longer at the power-on time.

### Point to Note during PLL Clock Operation

While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

### Power Supply Pin Processing of an A/D Converter

Even when no A/D converter is used, establish a connection such that AVCC5 = AVRH5 = VCC5 and AVSS/AVRL5 = VSS.

### Points to Note About Using External Clocks

External clocks are not supported.

External direct clock input cannot be used.

### Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter

Be sure to turn on the digital power supply (VCC) before the application of the power supplies (AVCC, AVRH, and AVRL) and analog inputs (AN0 to AN63) of an A/D converter.
At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC). Perform these power-on and power-off operations without AVRH exceeding AVCC. Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed AVCC. (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

### Method to Switch Off VCC12 during Power-Off Sequence

During power-off sequence, it is necessary to switch off VCC12 by driving PSC1 pin low by entering PSS mode (power domain 2 off). If VCC12 needs to be switched off by other means, RSTX needs to be asserted before switching off VCC12 to inactivate the operation of VCC12 supplied domain below the operation assurance range.

### About C Pin Processing

This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest data sheet.

### Precautions on Designing a Mounting Substrate

Measures against heat generation from the package must be taken for the mounting substrate to observe the absolute maximum rating (operating temperature). Design a mounting substrate with 4 or more layers. Connect the back of the package stage and the substrate pad with solder paste. Arrange thermal via holes on the substrate pad.

### Notes on Writing to a Register Containing a Status Flag

In writing to a register containing a status flag (particularly an interrupt request flag, etc.) to control a function, it is important to take care not to accidentally clear the status flag.
Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value.
Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions have only 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

Note: Bit instructions take this point into account for registers that support bit-band units, so it does not need to be a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

# 9. Electric Characteristics

## 9.1 Electrical Characteristics

This chapter contains target values and information.
Target values and information are subjects to change without notice.

### *9.1.1 Absolute Maximum Rating*

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1, *2 | $V_{CC}5$ | $V_{SS}$-0.3 | $V_{SS}$+6.0 | V | |
| | $V_{CC}53$ | $V_{SS}$-0.3 | $V_{SS}$+6.0 | V | $V_{CC}53 \leq V_{CC}5$ |
| | $V_{CC}3$ | $V_{SS}$-0.3 | $V_{SS}$+4.0 | V | $V_{CC}3 \leq V_{CC}5$ |
| | $DV_{CC}$ | $V_{SS}$-0.3 | $V_{SS}$+6.0 | V | |
| | $V_{CC}12$ | $V_{SS}$-0.3 | $V_{SS}$+1.8 | V | $V_{CC}12 \leq AV_{CC}5$ |
| Analog supply voltage*1, *2 | $AV_{CC}5$ | $V_{SS}$-0.3 | $V_{SS}$+6.0 | V | $AV_{CC}5 \leq V_{CC}5$ |
| | AVcc3_DAC | $V_{SS}$-0.3 | $V_{SS}$+4.0 | V | for DAC |
| Analog reference voltage*1 | AVRH | $V_{SS}$-0.3 | $V_{SS}$+6.0 | V | AVRH ≤ $AV_{CC}5$ |
| Input voltage*1 | $V_{I1}$ | $V_{SS}$-0.3 | $V_{CC}5$+0.3 | V | 5 V pins not shared SMC |
| | $V_{I2}$ | $V_{SS}$-0.3 | $DV_{CC}$+0.3 | V | 5 V pins shared SMC |
| | $V_{I3}$ | $V_{SS}$-0.3 | $V_{CC}3$+0.3 | V | 3 V pins |
| | $V_{IE}$ | $V_{SS}$-0.3 | $V_{CC}53$+0.3 | V | 5 V/3 V pins |
| Analog pin input voltage*1 | $V_{IA}$ | $V_{SS}$-0.3 | $V_{CC}5$+0.3 | V | |
| Output voltage*1 | $V_{O1}$ | $V_{SS}$-0.3 | $V_{CC}5$+0.3 | V | 5 V pins not shared SMC |
| | $V_{O2}$ | $V_{SS}$-0.3 | $DV_{CC}$+0.3 | V | 5 V pins shared SMC |
| | $V_{O3}$ | $V_{SS}$-0.3 | $V_{CC}3$+0.3 | V | 3 V pins |
| | $V_{O4}$ | $V_{SS}$-0.3 | $V_{CC}53$+0.3 | V | 5 V/3 V pins |
| Maximum clamp current | $\|I_{CLAMP}\|$ | - | 4 | mA | *13, *A |
| Total maximum clamp current | $\Sigma\|I_{CLAMP}\|$ | - | 20 | mA | *13, *A |
| Total maximum clamp current | $\Sigma\|I_{CLAMP}\|$ | - | 90 | mA | *B |
| Total maximum clamp current | $\Sigma\|I_{CLAMP}\|$ | - | 65 | mA | *C |
| "L"-level maximum output current*3 | $I_{OL1}$ | - | 3.5 | mA | When setting is 1 mA*6, *7, *8 |
| | $I_{OL2}$ | - | 7 | mA | When setting is 2 mA*6, *7, *8, *9 |
| | $I_{OL3}$ | - | 10 | mA | When setting is 5 mA*9 |
| | $I_{OL4}$ | - | 16 | mA | When setting is 10 mA*9 |
| | $I_{OL6}$ | - | 40 | mA | When setting is 30 mA*7 |
| | $I_{OL7}$ | - | 8 | mA | When setting is 3 mA *10 |
| | $I_{OL8}$ | - | 11 | mA | When setting is 6 mA *11 |
| | $I_{OL9}$ | - | 21 | mA | When setting is 15 mA *12 |
| "L"-level average output current*4 | $I_{OLAV1}$ | - | 1 | mA | When setting is 1 mA*6, *7, *8 |
| | $I_{OLAV2}$ | - | 2 | mA | When setting is 2 mA*6, *7, *8, *9 |
| | $I_{OLAV3}$ | - | 5 | mA | When setting is 5 mA*9 |
| | $I_{OLAV4}$ | - | 10 | mA | When setting is 10 mA*9 |
| | $I_{OLAV6}$ | - | 30 | mA | When setting is 30 mA*7 |
| | $I_{OLAV7}$ | - | 3 | mA | When setting is 3 mA *10 |
| | $I_{OLAV8}$ | - | 6 | mA | When setting is 6 mA *11 |
| | $I_{OLAV9}$ | - | 15 | mA | When setting is 15 mA *12 |
| "L"-level total output current*5 | $\Sigma I_{OL1}$ | - | 50 | mA | *6, *10 |
| | $\Sigma I_{OL2}$ | - | 250 | mA | *7 |

| Parameter | Symbol | Rating | | Unit | Remarks | |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| "L"-level total output current*5 | $\Sigma I_{OL3}$ | - | 50 | mA | *8 | |
| | $\Sigma I_{OL4}$ | - | 50 | mA | *9, *11 | |
| "H"-level maximum output current*3 | $I_{OH1}$ | - | -3.5 | mA | When setting is 1 mA*6, *7, *8 | |
| | $I_{OH2}$ | - | -7 | mA | When setting is 2 mA*6, *7, *8, *9 | |
| | $I_{OH3}$ | - | -10 | mA | When setting is 5 mA*9 | |
| | $I_{OH4}$ | - | -16 | mA | When setting is 10 mA*9 | |
| | $I_{OH6}$ | - | -40 | mA | When setting is 30 mA*7 | |
| | $I_{OH8}$ | - | -11 | mA | When setting is 6 mA *11 | |
| | $I_{OH9}$ | - | -21 | mA | When setting is 15 mA *12 | |
| "H"-level average output current*4 | $I_{OHAV1}$ | - | -1 | mA | When setting is 1 mA*6, *7, *8 | |
| | $I_{OHAV2}$ | - | -2 | mA | When setting is 2 mA*6, *7, *8, *9 | |
| | $I_{OHAV3}$ | - | -5 | mA | When setting is 5 mA*9 | |
| | $I_{OHAV4}$ | - | -10 | mA | When setting is 10 mA*9 | |
| | $I_{OHAV6}$ | - | -30 | mA | When setting is 30 mA*7 | |
| | $I_{OHAV8}$ | - | -6 | mA | When setting is 6 mA *11 | |
| | $I_{OHAV9}$ | - | -15 | mA | When setting is 15 mA *12 | |
| "H"-level total output current*5 | $\Sigma I_{OH1}$ | - | -50 | mA | *6, *10 | |
| | $\Sigma I_{OH2}$ | - | -250 | mA | *7 | |
| | $\Sigma I_{OH3}$ | - | -50 | mA | *8 | |
| | $\Sigma I_{OH4}$ | - | -50 | mA | *9 *11 | |
| Power consumption | $P_D$ | - | 2000 | mW | -40 °C ≤ $T_A$ ≤ 105 °C | |
| | | - | 1100 | mW | -40 °C ≤ $T_A$ ≤ 125 °C | |
| Operating temperature | $T_A$ | -40 | +105 | °C | $P_D$ ≤ 2000 mW | |
| | | -40 | +125 | °C | $P_D$ ≤ 1100 mW | |
| System Thermal Resistance | Theta j-a1 | - | 17 | °C/W | TEQFP 208 | The minimum value depends on the system specification of heat radiation. The described value is estimated under the condition which is specified at "9.1.2 Recommended Operating ". |
| | Theta j-a2 | - | 19 | °C/W | TEQFP 176 | |
| | Theta j-a3 | - | 20 | °C/W | TEQFP 144 (0.5 mm Pitch) | |
| | Theta j-a4 | - | 22 | °C/W | TEQFP 144 (0.4 mm Pitch) | |
| Package Thermal Resistance | Psi j-t1 | - | 0.6 | °C/W | TEQFP208 | |
| | Psi j-t2 | - | 1.0 | °C/W | TEQFP176 | |
| | Psi j-t3 | - | 2.0 | °C/W | TEQFP144 (0.5 mm Pitch) | |
| | Psi j-t4 | - | 2.0 | °C/W | TEQFP144 (0.4 mm Pitch) | |
| Storage temperature | Tstg | -55 | +150 | °C | | |

*1 These parameters are based on the condition that $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0.0 V.

*2 Take care that $DV_{CC}$, $AV_{CC}5$ do not exceed $V_{CC}5$ at, for example, the power-on time.

*3 The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4 The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5 The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6 Output of 5 V pins.

*7 Output of SMC pins.

*8 Output of 5 V/3 V pins.

*9 Output of 3 V pins.

*10 Output of $I^2C$.

*11 Output of Media LB pins

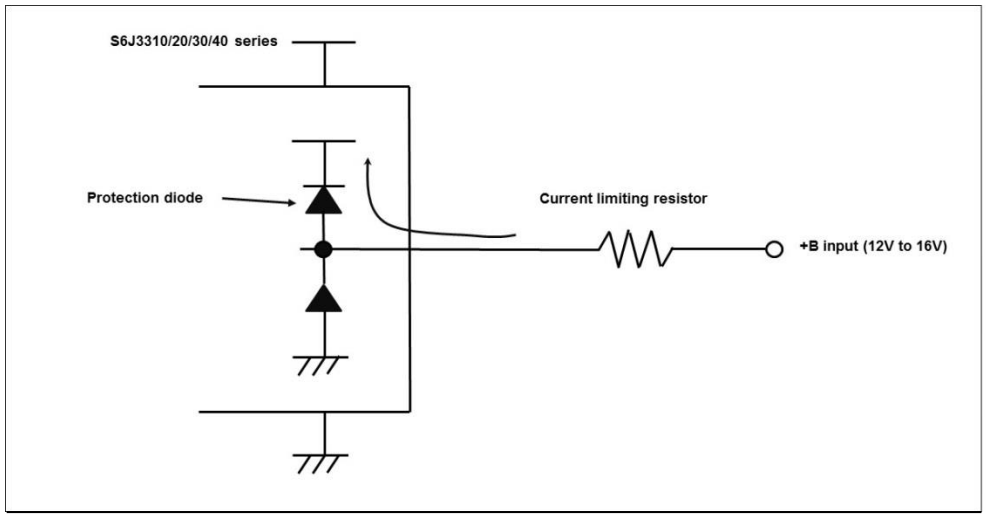
*12 Output of DSP0_CLK pins

*13 VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating.

*A Relevant pins: All general-purpose ports and analog input pins

- Corresponding pins: all general-purpose ports
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

Example of a recommended circuit




***WARNING:***

– *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

*B Relevant pins: All general-purpose ports and analog input pins

- Corresponding pins: all general-purpose ports
- Use within recommended operating conditions.
- Use at DC voltage (current).
  MCU is operational, IO is driving LOW level (i.e. NMOS transistor active), there are negative biased pulses (-B signal) applied to active IO according to following specification (must not be exceeded).

Pulse condition specification:

U_pulse = max -40 V
T_pulse = max 1 ms
#_pulse = max 5000

Current and Power Dissipation

U_peak = -40 V
R_serial = 22 k
=> I_pin = 1.8 mA

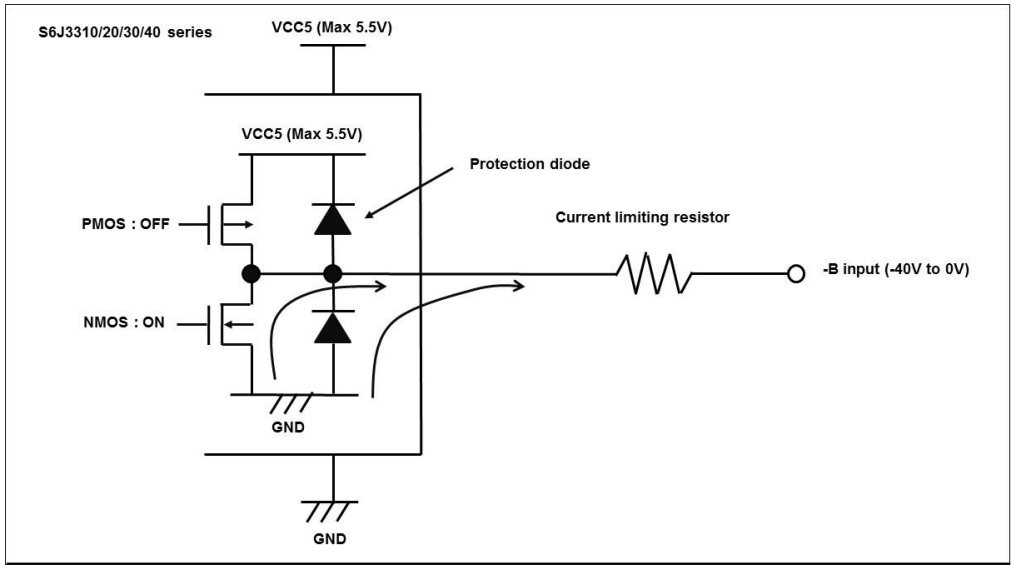
U_out = -0.1 V (current drawn mainly over NMOS transistor)

=> I_total = 50 pins x 1.8 mA = 90 mA
=> P_total = 50 pins x (1.8 mA x 0.1 V) = 9 mW

I_total and P_total are within allowed limits of extended specification.

- The - B signal should always be applied by connecting a limiting resistor between the - B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the - B signal is input.
- Do not leave - B input pins open.

Example of a recommended circuit




***WARNING:***

– *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

*C Relevant pins: All general-purpose ports and analog input pins

- Corresponding pins: all general-purpose ports
- Use within non operation conditions. The device is not supplied (VCC5: off, VCC12: off, VCC53: off).
- Use at DC voltage (current).
  MCU is non-operational, PCB is in reverse polarity condition (supply of the MCU is off), negative biased voltage level (-B signal) is applied to inactive IO according to following specification (must not be exceeded).

Reverse polarity condition specification:

U_reverse = max -28 V
T_reverse = max 4 h

Current and Power Dissipation

U_reverse = -28 V
R_serial = 22 k
=> I_pin = 1.3 mA

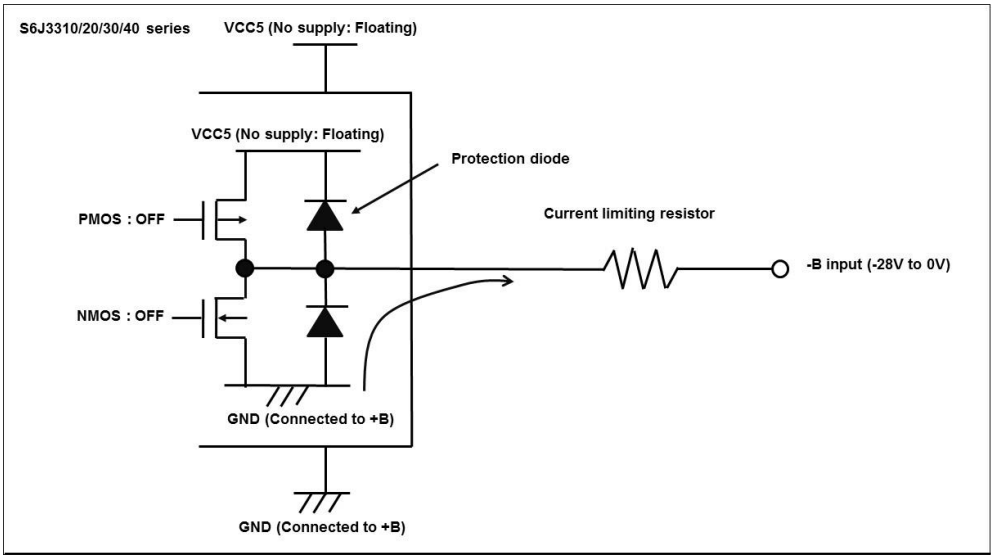
U_out = -0.7 V (current drawn mainly over clamping diodes)

=> I_total = 50 pins x 1.3 mA = 65 mA
=> P_total = 50 pins x (1.3 mA x 0.7 V) = 46 mW

I_total and P_total are within allowed limits of extended specification.

- The - B signal should always be applied by connecting a limiting resistor between the - B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the - B signal is input.
- Do not leave - B input pins open.

Example of a recommended circuit




***WARNING:***

− *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

### 9.1.2 Recommended Operating Condition

| Parameter | Symbol | Pin Name | Rating | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Supply voltage Recommended operation assurance range*4 | $V_{CC}5$ | VCC5 | 4.5 | 5.5 | V | *1 |
| | | | 3 | 3.6 | | *2 *3 |
| | $V_{CC}53$ | VCC53 | 4.5 | 5.5 | V | *1 |
| | | | 3 | 3.6 | V | |
| | $DV_{CC}$ | DVCC | 4.5 | 5.5 | V | *1 *3 |
| | | | 3.0 | 3.6 | | *2 |
| | $AV_{CC}5$ | AVCC5 | 4.5 | 5.5 | V | *1 |
| | | | 3 | 3.6 | | *2 *3 |
| | $V_{CC}3$ | VCC3 | 3 | 3.6 | V | |
| | $V_{CC}12$ | VCC12 | 1.09 | 1.21 | V | |
| | $AV_{CC}3$_DAC | AVCC3_DAC | 3 | 3.6 | V | |
| Supply voltage Operation assurance range | $V_{CC}5$ | VCC5 | 3.5 | 5.5 | V | *1 |
| | | | 2.7 | 3.6 | | *2 *3 |
| | $V_{CC}53$ | VCC53 | 2.7 | 5.5 | V | *1 |
| | | | 2.7 | 3.6 | | |
| | $DV_{CC}$ | DVCC | 3.5 | 5.5 | V | *1 *3 |
| | | | 2.7 | 3.6 | | *2 |
| | $AV_{CC}5$ | AVCC5 | 3.5 | 5.5 | V | *1 |
| | | | 2.7 | 3.6 | | *2 *3 |
| | $V_{CC}3$ | VCC3 | 2.7 | 3.6 | V | |
| | $V_{CC}12$ | VCC12 | 1.09 | 1.21 | V | *5 |
| | $AV_{CC}3$_DAC | AVCC3_DAC | 2.7 | 3.6 | V | |
| Smoothing capacitor* | $C_S$ | C | 4.7 | | µF | Tolerance of up to ±40 % |
| Operating temperature | $T_A$ | - | -40 | 105 | °C | $P_D \leq 2000$ mW |
| | $T_A$ | - | -40 | 125 | °C | $P_D \leq 1100$ mW |

*1:For S6J33xxxSx or S6J33xxxUx or S6J33xxxTx or S6J33xxxVx option.

*2:For S6J33xxxBx or S6J33xxxDx or S6J33xxxFx or S6J33xxxHx option.

*3:For S6J33xxxAx or S6J33xxxCx or S6J33xxxEx or S6J33xxxGx option.

*4:Corresponding functions for Low voltage monitoring of supply voltage are described in CHAPTER 13 Low Voltage Detection of *S6J3300 Series Hardware Manual*.

The detection/release threshold values of following LVD channels are potentially below supply range defined in 9.1.2 Recommended operating condition (refer to "9.1.4.11 Low Voltage Detection (External Voltage)" and “9.1.4.12 Low Voltage Detection (Internal Voltage)" for detection/release threshold values for these LVD channels):

LVDL0

LVDL1

LVDL2

LVDH0

LVDH1

LVDH2

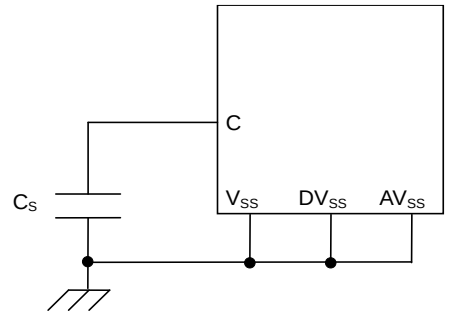
When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative. The initial detection voltage of the external low voltage detection is 2.6 V ± 3.5 %[*2] [*3] (LVDH1/LVDH2) or 0.8 V ± 3.5 % (LVDL2). This LVD setting and internal LVD (LVDL0/LVDL1) cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

- Please use these LVD channels with your own risk
- Please monitor the external power supplies on the PCB if needed

*5:When the voltage of Vcc12 is in the out of range against supply voltage operation assurance, the operation of circuit which Vcc12 used as the power source becomes unstable status. In that case, the value of each registers including RESCAUSEUR Register cannot be guaranteed, so these flags should don't care by software processing

*: For the connections of smoothing capacitor $C_S$, see the following diagram.

**C Pin Connection Diagram**




***Notes:***

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the electrical characteristics of the device are warranted when the device is operated within these ranges.*
  *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact sales representatives beforehand.*
- *Required power supply sequence is the following:*
  *{VCC5 -> AVCC5} -> [DVCC or VCC53 or VCC3 or AVCC3_DAC or VCC12]*
  *Note that power supplies inside "[ ]" can be turned on in arbitrary order and "{ }" can be turned on in shown sequence or simultaneously.*

***Notes:***

- *$T_A$: Ambient temperature (JEDEC)*
- *$T_C$: Case temperature (JEDEC), the maximum measured temperature of package case top.*
- *Both rating of $T_A$ and $T_C$ should simultaneously be satisfied as maximum operation temperature.*
- *The following condition should be satisfied in order to facilitate heat dissipation.*
    1. *Four or more layers PCB should be used.*
    2. *The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)*
    3. *One layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90 % or more. The layer can be used for system ground.*
    4. *35 % or more of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.*
    5. *The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.*

Example thermal via holes on PCB

- *The above figure is a schematic diagram showing PCB in section.*
- *Thermal via holes should closely be placed and aligned with lands.*
- *It is recommended to connect the land pattern to the VSS-ground level (GND plan of inner layer bellow the MCU) as thermal heat sink.*

### 9.1.3 DC Characteristics

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level Input voltage | $V_{IH1}$ | P0_00 to P0_20, P2_09 to P2_19, P3_00 to P3_07, P3_24 to P3_31, P4_00 to P4_07 | CMOS hysteresis input level is selected | 0.7×$V_{CC}53$ | - | $V_{CC}53$+0.3 | V | |
| | $V_{IH2}$ | | Automotive input level is selected | 0.8×$V_{CC}53$ | - | $V_{CC}53$+0.3 | V | |
| | $V_{IH3}$ | | TTL input level is selected | 2.0 | - | $V_{CC}53$+0.3 | V | |
| | $V_{IH4}$ | P1_03 to P1_16, P3_08 to P3_23, P4_08 to P4_23 | CMOS hysteresis input level is selected | 0.7×$V_{CC}5$ | - | $V_{CC}5$+0.3 | V | |
| | $V_{IH5}$ | | Automotive input level is selected | 0.8×$V_{CC}5$ | - | $V_{CC}5$+0.3 | V | |
| | $V_{IH6}$ | P1_09, P1_10, P1_15, P1_16 | TTL input level is selected | 2.0 | - | $V_{CC}5$+0.3 | V | |
| | $V_{IH7}$ | P1_17 to P1_31, P2_00 to P2_08, P4_24 to P4_31 | CMOS hysteresis input level is selected | 0.7×$DV_{CC}$ | - | $DV_{CC}$+0.3 | V | |
| | $V_{IH8}$ | | Automotive input level is selected | 0.8×$DV_{CC}$ | - | $DV_{CC}$+0.3 | V | |
| | $V_{IH9}$ | RSTX NMIX | - | 0.7×$V_{CC}5$ | - | $V_{CC}5$+0.3 | V | |
| | $V_{IH10}$ | MD | - | 0.7×$V_{CC}5$ | - | $V_{CC}5$+0.3 | V | |
| | $V_{IH11}$ | JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS | - | 2.7 | - | $V_{CC}5$+0.3 | V | |
| | $V_{IH12}$ | P0_21 to P0_31, P1_00 to P1_02 | CMOS hysteresis input level is selected | 0.7×$V_{CC}3$ | - | $V_{CC}3$+0.3 | V | |
| | $V_{IH13}$ | P0_21 to P0_31 | TTL input level is selected | 2.0 | - | $V_{CC}3$+0.3 | V | |
| | $V_{IH14}$ | P1_00 to P1_02 | - | 1.7 | - | $V_{CC}3$+0.3 | V | MediaLB |

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$ = 5.0 V ± 10%, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ =0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "L" level Input voltage | $V_{IL1}$ | P0_00 to P0_20, P2_09 to P2_19, P3_00 to P3_07, P3_24 to P3_31, P4_00 to P4_07 | CMOS hysteresis input level is selected | Vss-0.3 | - | 0.3×$V_{CC}$53 | V | |
| | $V_{IL2}$ | | Automotive input level is selected | Vss-0.3 | - | 0.5×$V_{CC}$53 | V | |
| | $V_{IL3}$ | | TTL input level is selected | Vss-0.3 | - | 0.8 | V | |
| | $V_{IL4}$ | P1_03 to P1_16, P3_08 to P3_23, P4_08 to P4_23 | CMOS hysteresis input level is selected | Vss-0.3 | - | 0.3×$V_{CC}$5 | V | |
| | $V_{IL5}$ | | Automotive input level is selected | Vss-0.3 | - | 0.5×$V_{CC}$5 | V | |
| | $V_{IL6}$ | P1_09, P1_10, P1_15, P1_16 | TTL input level is selected | Vss-0.3 | - | 0.8 | V | |
| | $V_{IL7}$ | P1_17 to P1_31, P2_00 to P2_08, P4_24 to P4_31 | CMOS hysteresis input level is selected | Vss-0.3 | - | 0.3×$DV_{CC}$ | V | |
| | $V_{IL8}$ | | Automotive input level is selected | Vss-0.3 | - | 0.5×$DV_{CC}$ | V | |
| | $V_{IL9}$ | RSTX NMIX | - | Vss-0.3 | - | 0.3×$V_{CC}$5 | V | |
| | $V_{IL10}$ | MD | - | Vss-0.3 | - | 0.3×$V_{CC}$5 | V | |
| | $V_{IL11}$ | JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS | - | Vss-0.3 | - | 0.8 | V | |
| | $V_{IL12}$ | P0_21 to P0_31, P1_00 to P1_02 | CMOS hysteresis input level is selected | Vss-0.3 | - | 0.3×$V_{CC}$3 | V | |
| | $V_{IL13}$ | P0_21 to P0_31 | TTL input level is selected | Vss-0.3 | - | 0.8 | V | |
| | $V_{IL14}$ | P1_00 to P1_02 | - | Vss-0.3 | - | 0.7 | V | MediaLB |

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Hysteresis voltage | $V_{HYS1}$ | P0_00 to P0_20, P2_09 to P2_19, P3_00 to P3_07, P3_24 to P3_31, P4_00 to P4_07 | CMOS hysteresis input level is selected | - | $0.05 \times V_{CC}53$ | - | V | |
| | $V_{HYS2}$ | | Automotive input level is selected | - | $0.03 \times V_{CC}53$ | - | V | |
| | $V_{HYS3}$ | | TTL input level is selected | - | 0.035 | - | V | |
| | $V_{HYS4}$ | P1_03 to P1_16, P3_08 to P3_23, P4_08 to P4_23 | CMOS hysteresis input level is selected | - | $0.05 \times V_{CC}5$ | - | V | |
| | $V_{HYS5}$ | | Automotive input level is selected | - | $0.03 \times V_{CC}5$ | - | V | |
| | $V_{HYS6}$ | P1_09, P1_10, P1_15, P1_16 | TTL input level is selected | - | 0.035 | - | V | |
| | $V_{HYS7}$ | P1_17 to P1_31, P2_00 to P2_08, P4_24 to P4_31 | CMOS hysteresis input level is selected | - | $0.05 \times D V_{CC}$ | - | V | |
| | $V_{HYS8}$ | | Automotive input level is selected | - | $0.03 \times D V_{CC}$ | - | V | |
| | $V_{HYS9}$ | RSTX NMIX | - | - | $0.05 \times V_{CC}5$ | - | V | |
| | $V_{HYS10}$ | MD | - | - | $0.05 \times V_{CC}5$ | - | V | |
| | $V_{HYS11}$ | JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS | - | - | 0.035 | - | V | |
| | $V_{HYS12}$ | P0_21 to P0_31, P1_00 to P1_02 | CMOS hysteresis input level is selected | - | $0.05 \times V_{CC}3$ | - | V | |
| | $V_{HYS13}$ | P0_21 to P0_31 | TTL input level is selected | - | 0.035 | - | V | |
| | $V_{HYS14}$ | P1_00 to P1_02 | - | - | 0.080 | - | V | MediaLB |

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ =0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level output voltage | $V_{OH1}$ | P0_00 to P0_19, P2_09 to P2_11, P2_13 to P2_19, P3_00 to P3_07, P3_24 to P3_31, P4_00 to P4_07 | $V_{CC}53$ = 4.5 V $I_{OH}$ = -1.0 mA<br>$V_{CC}53$ = 3.0 V $I_{OH}$=-0.5 mA | $V_{CC}53$ - 0.5 | - | $V_{CC}53$ | V | ODR[1:0]= 2b00 |
| | $V_{OH2}$ | | $V_{CC}53$ = 4.5 V $I_{OH}$ = -2.0 mA<br>$V_{CC}53$ = 3.0 V $I_{OH}$ = -1.0 mA | $V_{CC}53$ - 0.5 | - | $V_{CC}53$ | V | ODR[1:0]= 2b01 |
| | $V_{OH3}$ | | $V_{CC}53$ = 4.5 V $I_{OH}$ = -5.0 mA<br>$V_{CC}53$ = 3.0 V $I_{OH}$ = -2.0 mA | $V_{CC}53$ - 0.5 | - | $V_{CC}53$ | V | ODR[1:0]= 2b10 |
| | $V_{OH4}$ | P1_03 to P1_16, P3_08 to P3_23, P4_08 to P4_23 | $V_{CC}5$ = 4.5 V $I_{OH}$ = -1.0 mA | $V_{CC}5$ - 0.5 | - | $V_{CC}5$ | V | |
| | $V_{OH5}$ | | $V_{CC}5$ = 4.5 V $I_{OH}$ = -2.0 mA | $V_{CC}5$ - 0.5 | - | $V_{CC}5$ | V | |
| | $V_{OH6}$ | | $V_{CC}5$ = 4.5 V $I_{OH}$ = -5.0 mA | $V_{CC}5$ - 0.5 | - | $V_{CC}5$ | V | |
| | $V_{OH7}$ | PSC_1 | $V_{CC}5$ = 4.5 V $I_{OH}$ = -2.0 mA | $V_{CC}5$ - 0.5 | - | $V_{CC}5$ | V | |
| | $V_{OH8}$ | JTAG_TDO | $V_{CC}5$ = 4.5 V $I_{OH}$ = -5.0 mA | $V_{CC}5$ - 0.5 | - | $V_{CC}5$ | V | |
| | $V_{OH10}$ | P1_17 to P1_31, P2_00 to P2_08, P4_24 to P4_31 | $DV_{CC}$ = 4.5 V $I_{OH}$ = -1.0 mA | $DV_{CC}$ - 0.5 | - | $DV_{CC}$ | V | |
| | $V_{OH11}$ | | $DV_{CC}$ = 4.5 V $I_{OH}$ = -2.0 mA | $DV_{CC}$ - 0.5 | - | $DV_{CC}$ | V | |
| | $V_{OH12}$ | | $DV_{CC}$ = 4.5 V $I_{OH}$ = -5.0 mA | $DV_{CC}$ - 0.5 | - | $DV_{CC}$ | V | |
| | $V_{OH13}$ | | $DV_{CC}$ = 4.5 V $I_{OH}$ = -30.0 mA | $DV_{CC}$ - 0.5 | - | $DV_{CC}$ | V | SMC |
| | $V_{OH14}$ | | $DV_{CC}$ = 4.5 V $I_{OH}$ = -40.0 mA | $DV_{CC}$ - 0.5 | - | $DV_{CC}$ | V | SMC Tj = -40 °C |
| | $V_{OH15}$ | P0_21 to P0_31, P1_00 to P1_02 | $V_{CC}3$ = 3.0 V $I_{OH}$ = -2.0 mA | $V_{CC}3$ - 0.5 | - | $V_{CC}3$ | V | |
| | $V_{OH16}$ | | $V_{CC}3$ = 3.0 V $I_{OH}$ = -5.0 mA | $V_{CC}3$ - 0.5 | - | $V_{CC}3$ | V | |
| | $V_{OH17}$ | | $V_{CC}3$ = 3.0 V $I_{OH}$ = -6.0 mA | $V_{CC}3$ - 0.5 | - | $V_{CC}3$ | V | |
| | $V_{OH18}$ | | $V_{CC}3$ = 3.0 V $I_{OH}$ = -15.0 mA | $V_{CC}3$ - 0. 5 | - | $V_{CC}3$ | V | |

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10%, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level output voltage | $V_{OH19}$ | P2_12 | $V_{CC}53$ = 4.5 V<br>$I_{OH}$ = -1.0 mA | $V_{CC}53$ - 0.5 | - | $V_{CC}53$ | V | ODR[1:0] = 2b00 |
| | $V_{OH20}$ | | $V_{CC}53$ = 3.0 V<br>$I_{OH}$ = -0.5 mA | | | | | |
| | $V_{OH21}$ | | $V_{CC}53$ = 4.5 V<br>$I_{OH}$ = -2.0 mA | $V_{CC}53$ - 0.5 | - | $V_{CC}53$ | V | ODR[1:0] = 2b01 |
| | $V_{OH22}$ | | $V_{CC}53$ = 3.0 V<br>$I_{OH}$ = -1.0 mA | | | | | |
| | $V_{OH23}$ | | $V_{CC}53$ = 4.5 V<br>$I_{OH}$ = -5.0 mA | $V_{CC}53$ - 0.5 | - | $V_{CC}53$ | V | ODR[1:0] = 2b10 |
| | $V_{OH24}$ | | $V_{CC}53$ = 3.0 V<br>$I_{OH}$ = -2.0 mA | | | | | |
| | $V_{OH26}$ | | $V_{CC}53$ = 3.0 V<br>$I_{OH}$ = -15.0 mA | $V_{CC}53$ - 0.5 | - | Vcc53 | V | ODR[1:0] = 2b11 |

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "L" level output voltage | $V_{OL1}$ | P0_00 to P0_19, P2_09 to P2_11, P2_13 to P2_19, P3_00 to P3_07, P3_24 to P3_31, P4_00 to P4_07 | $V_{CC}53$ = 4.5 V<br>$I_{OL}$ = 1.0 mA<br>$V_{CC}53$ = 3.0 V<br>$I_{OL}$ = 0.5 mA | 0 | - | 0.4 | V | ODR[1:0] = 2b00 |
| | $V_{OL2}$ | | $V_{CC}53$ = 4.5 V<br>$I_{OL}$ = 2.0 mA<br>$V_{CC}53$ = 3.0 V<br>$I_{OL}$ = 1.0 mA | 0 | - | 0.4 | V | ODR[1:0] = 2b01 |
| | $V_{OL3}$ | | $V_{CC}53$ = 4.5 V<br>$I_{OL}$ = 5.0 mA<br>$V_{CC}53$ = 3.0 V<br>$I_{OL}$ = 2.0 mA | 0 | - | 0.4 | V | ODR[1:0] = 2b10 |
| | $V_{OL4}$ | P1_03 to P1_16, P3_08 to P3_23, P4_08 to P4_23 | $V_{CC}5$ = 4.5 V<br>$I_{OL}$ = 1.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL5}$ | | $V_{CC}5$ = 4.5 V<br>$I_{OL}$ = 2.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL6}$ | | $V_{CC}5$ = 4.5 V<br>$I_{OL}$ = 5.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL7}$ | PSC_1 | $V_{CC}5$ = 4.5 V<br>$I_{OL}$ = 2.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL8}$ | JTAG_TDO | $V_{CC}5$ = 4.5 V<br>$I_{OL}$ = 5.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL9}$ | P1_09, P1_10, P1_15, P1_16 | $V_{CC}5$ = 4.5 V<br>$I_{OL}$ = 3.0 mA | 0 | - | 0.4 | V | $I^2C$ |
| | $V_{OL10}$ | P1_17 to P1_31, P2_00 to P2_08, P4_24 to P4_31 | $DV_{CC}$ = 4.5 V<br>$I_{OL}$ = 1.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL11}$ | | $DV_{CC}$ = 4.5 V<br>$I_{OL}$ = 2.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL12}$ | | $DV_{CC}$ = 4.5 V<br>$I_{OL}$ = 5.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL13}$ | | $DV_{CC}$ = 4.5 V<br>$I_{OL}$ = 30.0 mA | 0 | - | 0.55 | V | SMC |
| | $V_{OL14}$ | | $DV_{CC}$ = 4.5 V<br>$I_{OL}$ = 40.0 mA | 0 | - | 0.55 | V | SMC<br>Tj = -40 °C |
| | $V_{OL15}$ | P0_21 to P0_31, P1_00 to P1_02 | $V_{CC}3$ = 3.0 V<br>$I_{OL}$ = 2.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL16}$ | | $V_{CC}3$ = 3.0 V<br>$I_{OL}$ = 5.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL17}$ | | $V_{CC}3$ = 3.0 V<br>$I_{OL}$ = 6.0 mA | 0 | - | 0.4 | V | |
| | $V_{OL18}$ | | $V_{CC}3$ = 3.0 V<br>$I_{OL}$ = 15.0 mA | 0 | - | 0.4 | V | |

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "L" level output voltage | $V_{OL19}$ | P2_12 | $V_{CC}53$ = 4.5 V $I_{OL}$ = 1.0 mA | 0 | - | 0.4 | V | ODR[1:0] = 2b00 |
| | $V_{OL20}$ | | $V_{CC}53$ = 3.0 V $I_{OL}$ = 0.5 mA | | | | | |
| | $V_{OL21}$ | | $V_{CC}53$ = 4.5 V $I_{OL}$ = 2.0 mA | 0 | - | 0.4 | V | ODR[1:0] = 2b01 |
| | $V_{OL22}$ | | $V_{CC}53$ = 3.0 V $I_{OL}$ = 1.0 mA | | | | | |
| | $V_{OL23}$ | | $V_{CC}53$ = 4.5 V $I_{OL}$ = 5.0 mA | 0 | - | 0.4 | V | ODR[1:0] = 2b10 |
| | $V_{OL24}$ | | $V_{CC}53$ = 3.0 V $I_{OL}$ = 2.0 mA | | | | | |
| | $V_{OL26}$ | | $V_{CC}53$ = 3.0 V $I_{OL}$ = 15.0 mA | 0 | - | 0.4 | V | ODR[1:0] = 2b11 |

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leakage current | $I_{IL}$ | P0_00 to P0_20, P1_03 to P1_31, P2_00 to P2_19, P3_00 to P3_31, P4_00 to P4_31 | $V_{CC}5$ = $V_{CC}53$ = $DV_{CC}$ = $AV_{CC}$ = 5.5 V $V_{SS}$ < VI < $V_{CC}$ | -5 | - | +5 | µA | 5 V pins 5 V/3 V pins |
| | | P0_21 to P0_31, P1_00 to P1_02 | $V_{CC}3$ = 3.6 V $V_{SS}$ < VI < $V_{CC}3$ | -10 | - | +10 | µA | 3 V pins |
| Pull-up resistor | $R_{UP1}$ | RSTX, NMIX | - | 25 | 50 | 100 | kΩ | |
| | $R_{UP2}$ | P0_00 to P0_20, P1_03 to P1_31, P2_00 to P2_19, P3_00 to P3_31, P4_00 to P4_31 | Pull-up resistor selected | 25 | 50 | 100 | kΩ | 5 V pins 5 V/3 V pins |
| | $R_{UP3}$ | P0_21 to P0_31, P1_00 to P1_02 | Pull-up resistor selected | 17 | 50 | 66 | kΩ | 3 V pins |
| | $R_{UP4}$ | JTAG_TDI, JTAG_TMS, JTAG_TCK | - | 25 | 50 | 100 | kΩ | |
| Pull-down resistor | $R_{down1}$ | P0_00 to P0_20, P1_03 to P1_31, P2_00 to P2_19, P3_00 to P3_31, P4_00 to P4_31 | Pull-down resistor selected | 25 | 50 | 100 | kΩ | 5 V pins 5 V/3 V pins |
| | $R_{down2}$ | P0_21 to P0_31, P1_00 to P1_02 | Pull-down resistor selected | 17 | 50 | 66 | kΩ | 3 V pins |
| | $R_{down3}$ | JTAG_NTRST | - | 25 | 50 | 100 | kΩ | |
| Input capacitance | $C_{IN1}$ | P0_00 to P0_31, P1_00 to P1_16, P2_09 to P2_19, P3_00 to P3_31, P4_00 to P4_23 | - | - | 5 | 15 | pF | |
| | $C_{IN2}$ | P1_17 to P1_31, P2_00 to P2_08, P4_24 to P4_31 | - | - | 15 | 45 | pF | When using SMC |

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CC12}$ | VCC12 | Normal operation | - | 315 | 775 | mA | $T_A$ = -40 ~ 105 °C<br>CPU:240MHz, HPM:120 MHz<br>(CPU:200 MHz, HPM:200 MHz)<br>GDC: 200 MHz |
| | | | | - | - | 395 | mA | Example use case *1<br>$T_A$ = -40 ~ 105 °C<br>CPU:60 MHz, HPM:60 MHz<br>GDC: 60 MHz |
| | | | Flash write/erase | - | 320 | 780 | mA | $T_A$ = -40 ~ 105 °C<br>CPU:240 MHz, HPM:120 MHz<br>(CPU:200 MHz, HPM:200 MHz)<br>GDC: 200 MHz |
| | $I_{CCH12}$ | | Timer/ Stop Mode | - | - | 420 | mA | |
| | $I_{CC5}$ | VCC5 | Normal operation | - | 25 | 45 | mA | |
| | | | Flash write/erase | - | - | 60 | mA | |

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CCT5}$ | VCC5 | Timer mode | - | 370 | 810 | µA | $T_A$ = 25 °C. 4 MHz crystal for main oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON |
| | | | | - | 360 | 780 | µA | $T_A$ = 25 °C. 4 MHz crystal for main oscillator. PD1 = ON, PD4_0 = ON or PD4_1 = ON |
| | | | | - | 350 | 750 | µA | $T_A$ = 25 °C. 4 MHz crystal for main oscillator. PD1 = ON |
| | | | | - | 450 | 890 | µA | $T_A$ = 25 °C. 8 MHz crystal for main oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON |
| | | | | - | 440 | 860 | µA | $T_A$ = 25 °C. 8 MHz crystal for main oscillator. PD1 = ON, PD4_0 = ON or PD4_1 = ON |
| | | | | - | 430 | 830 | µA | $T_A$ = 25 °C. 8 MHz crystal for main oscillator. PD1 = ON |
| | | | | - | 110 | 430 | µA | $T_A$ = 25 °C. 32 kHz crystal for sub oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON |
| | | | | - | 100 | 400 | µA | $T_A$ = 25 °C. 32 kHz crystal for sub oscillator. PD1 = ON, PD4_0 = ON or PD4_1 = ON |
| | | | | - | 90 | 370 | µA | $T_A$ = 25 °C. 32 kHz crystal for sub oscillator. PD1 = ON |
| | $I_{CCH5}$ | | Stop mode | - | 100 | 400 | µA | $T_A$ = 25 °C. PD1 = ON, PD4_0 = ON, PD4_1 = ON |
| | | | | - | 90 | 370 | µA | $T_A$ = 25 °C. PD1 = ON, PD4_0 = ON or PD4_1 = ON |
| | | | | - | 80 | 340 | µA | $T_A$ = 25 °C. PD1 = ON |

*1: Example use case at following condition
CPU:60MHz, HPM:60MHz, GDC: 60MHz
Peripherals:
- DMAC active (WorkFlash => SystemRAM)
- All timers active
- 6 SMCs, 1 CAN, 2LIN, 1SPI, PWMs, ADCs
Display controller:
- 2 (= all) layers active (60 MHz, noise RGBA, 32 bpp, 2048 x 5 pixels)
- Any other resources inactive
- IOs no toggle

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current * | $I_{CCT5}$ | VCC5 | Timer mode | - | 345 | 630 | µA | $T_A$ = 25 °C. 4 MHz crystal for main oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON |
| | | | | - | 340 | 625 | µA | $T_A$ = 25 °C. 4 MHz crystal for main oscillator. PD1 = ON, PD4_0 = ON or PD4_1 = ON |
| | | | | - | 335 | 620 | µA | $T_A$ = 25 °C. 4 MHz crystal for main oscillator. PD1 = ON |
| | | | | - | 420 | 705 | µA | $T_A$ = 25 °C. 8 MHz crystal for main oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON |
| | | | | - | 415 | 700 | µA | $T_A$ = 25 °C. 8 MHz crystal for main oscillator. PD1 = ON, PD4_0 = ON or PD4_1 = ON |
| | | | | - | 410 | 695 | µA | $T_A$ = 25 °C. 8 MHz crystal for main oscillator. PD1 = ON |
| | | | | - | 80 | 135 | µA | $T_A$ = 25 °C. 32 kHz crystal for sub oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON |
| | | | | - | 75 | 130 | µA | $T_A$ = 25 °C. 32 kHz crystal for sub oscillator. PD1 = ON, PD4_0 = ON or PD4_1 = ON |
| | | | | - | 70 | 125 | µA | $T_A$ = 25 °C. 32 kHz crystal for sub oscillator. PD1 = ON |
| | $I_{CCH5}$ | | Stop mode | - | 75 | 130 | µA | $T_A$ = 25 °C. PD1 = ON, PD4_0 = ON, PD4_1 = ON |
| | | | | - | 70 | 125 | µA | $T_A$ = 25 °C. PD1 = ON, PD4_0 = ON or PD4_1 = ON |
| | | | | - | 65 | 120 | µA | $T_A$ = 25 °C. PD1 = ON |

* Electric Characteristics for S6J33xxxxE.

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| High current output drive capacity Phase-to-phase deviation1 | Delta-$V_{OH13}$ | PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn (n = 0 to 5) | $DV_{CC}$ = 4.5 V $I_{OH}$ = -30.0 mA Maximum deviation of $V_{OH13}$ | - | - | 90 | mV | * |
| High current output drive capacity Phase-to-phase deviation2 | Delta-$V_{OL13}$ | | $DV_{CC}$ = 4.5 V $I_{OL}$ = 30.0 mA Maximum deviation of $V_{OL13}$ | - | - | 90 | mV | * |
| LCD divider resistor | $R_{LCD}$ | V0 to V1, V1 to V2, V2 to V3 | - | 6.25 | 12.5 | 25 | kΩ | |
| COM0 to COM3 output impedance | $R_{VCOM}$ | COMm (m = 0 to 3) | - | - | - | 4.5 | kΩ | |
| SEG00 to SEG31 output impedance | $R_{VSEG}$ | SEGn (n = 00 to 31) | - | - | - | 17 | kΩ | |
| LCDC leak current | $I_{LCDC}$ | V0 to V3, COMm (m = 0 to 3), SEGn (n = 00 to 31) | $T_A$ = 25 °C | -0.5 | - | +0.5 | µA | |

*: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of $V_{OH13}$ / $V_{OL13}$ for each pin is defined. Same for other channels.

### 9.1.4 AC Characteristics

#### 9.1.4.1 Source Clock Timing

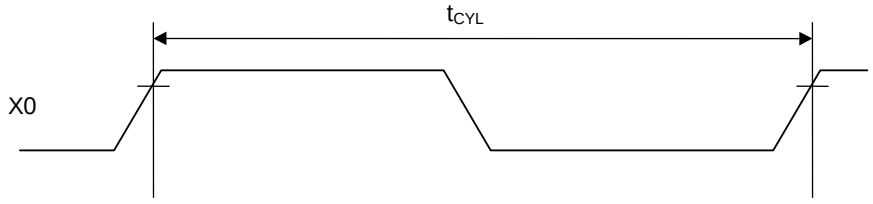
($T_A$: Recommended operating conditions, Vcc5 = 5.0 V ±10 %, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Source oscillation clock frequency | $F_C$ | X0, X1 | - | 3.6 | - | 16.0 | MHz | |
| Source oscillation clock cycle time | $t_{CYL}$ | X0, X1 | - | 62.5 | - | 277.8 | ns | |
| CAN PLL jitter (when locked) | $t_{PJ}$ | - | - | -10 | - | 10 | ns | |
| Internal Slow CR oscillation frequency | $F_{CRS}$ | - | - | 50 | 100 | 150 | kHz | |
| Internal Fast CR oscillation frequency | $F_{CRF}$ | - | - | 2.40 | 4.00 | 5.61- | MHz | Before trim |
| | | | | 3.20 | 4.00 | 4.81 | MHz | After trim |

***Notes:***

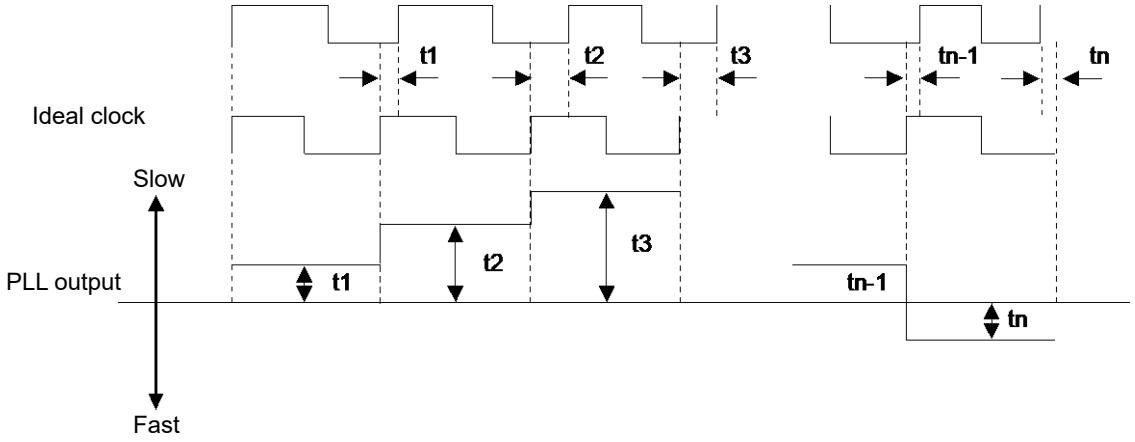
- *The maximum/minimum values have been standardized with the main clock and PLL clock in use.*
- *Jitter of source oscillator must be smaller than 300 ppm.*
- *Enough evaluation and adjustment are recommended using oscillator on your system board.*

- X0 and X1 clock timing




CAN PLL jitter

A time difference from the ideal clock is guaranteed for each cycle period within 20,000 cycles.

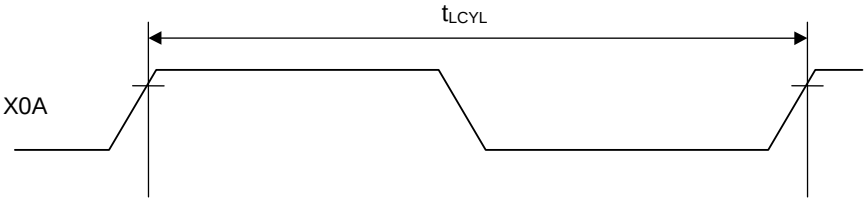


### 9.1.4.2 *Sub Clock Timing*

($T_A$: Recommended operating conditions, Vcc5 = 5.0 V ±10 %, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Source oscillation clock frequency | $F_{CL}$ | X0A, X1A | - | - | 32.768 | - | kHz | |
| Source oscillation clock cycle time | $t_{LCYL}$ | X0A, X1A | - | - | 30.52 | - | µs | |

- X0A and X1A clock timing



*9.1.4.3 Internal Clock Timing (S6J3310)*

- This chapter shows the TARGET characteristics for internal clock timing at the current stage.
- In the column symbol, same clock names as described in CHAPTER 5: CLOCK SYSTEM of *Traveo™ Platform Hardware Manual* are used.
- Corresponding functions for these clocks are described in CHAPTER 5: CLOCK CONFIGURATION of *S6J3300 Series Hardware Manual*.

($T_A$: Recommended operating conditions, $V_{CC}5$ = 5.0 V ±10 %, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Max *1 | Max *2 | Max *3 | | |
| Internal clock frequency | $F_{SSCG0}$ | 480 | 400 | 360 | MHz | SSCG0 output clock *4 |
| | $F_{SSCG1}$ | 400 | 400 | 400 | MHz | SSCG1 output clock *4 |
| | $F_{SSCG2}$ | 320 | 320 | 320 | MHz | SSCG2 output clock *4 |
| | $F_{SSCG3}$ | 400 | 400 | 400 | MHz | SSCG3 output clock *4 |
| | $F_{PLL0}$ | 480 | 400 | 360 | MHz | PLL0 output clock *4 |
| | $F_{PLL1}$ | 400 | 400 | 400 | MHz | PLL1 output clock *4 |
| | $F_{PLL2}$ | 400 | 400 | 400 | MHz | PLL2 output clock *4 |
| | $F_{PLL3}$ | 480 | 480 | 480 | MHz | PLL3 output clock *4 |
| | $F_{CLK_CPU0}$ | 240 | 200 | 180 | MHz | |
| | $F_{CLK_SHE}$ | 240 | 200 | 180 | MHz | |
| | $F_{CLK_FCLK}$ | 80 | 66.7 | 90 | MHz | |
| | $F_{CLK_ATB}$ | 120 | 100 | 90 | MHz | |
| | $F_{CLK_DBG}$ | 120 | 100 | 90 | MHz | |
| | $F_{CLK_HPM}$ | 120 | 200 | 180 | MHz | |
| | $F_{CLK_HPM2}$ | 60 | 100 | 90 | MHz | |
| | $F_{CLK_DMA}$ | 120 | 200 | 180 | MHz | |
| | $F_{CLK_MEMC}$ | 120 | 200 | 180 | MHz | |
| | $F_{CLK_EXTBUS}$ | 40 | 40 | 30 | MHz | |
| | $F_{CLK_SYSC1}$ | 40 | 40 | 60 | MHz | |
| | $F_{CLK_HAPP0A0}$ | 40 | 40 | 30 | MHz | Unused |
| | $F_{CLK_HAPP0A1}$ | 40 | 40 | 30 | MHz | Unused |
| | $F_{CLK_HAPP1B0}$ | 80 | 50 | 60 | MHz | |
| | $F_{CLK_HAPP1B1}$ | 40 | 50 | 30 | MHz | Unused |
| | $F_{CLK_LLPBM}$ | 240 | 200 | 180 | MHz | |
| | $F_{CLK_LLPBM2}$ | 120 | 100 | 90 | MHz | |
| | $F_{CLK_LCP}$ | 80 | 50 | 60 | MHz | |
| | $F_{CLK_LCP0}$ | 40 | 40 | 30 | MHz | |
| | $F_{CLK_LCP0A}$ | 80 | 66.7 | 60 | MHz | |
| | $F_{CLK_LCP1}$ | 40 | 40 | 30 | MHz | Unused |
| | $F_{CLK_LCP1A}$ | 80 | 66.7 | 60 | MHz | |
| | $F_{CLK_LAPP0}$ | 40 | 40 | 30 | MHz | Unused |
| | $F_{CLK_LAPP0A}$ | 40 | 40 | 30 | MHz | Unused |
| | $F_{CLK_LAPP1}$ | 40 | 40 | 30 | MHz | Unused |
| | $F_{CLK_LAPP1A}$ | 40 | 40 | 30 | MHz | Unused |
| | $F_{CLK_TRC}$ | 100 | 100 | 100 | MHz | |
| | $F_{CLK_CD1}$ | 200 | 200 | 200 | MHz | |
| | $F_{CLK_CD1A0}$ | 100 | 100 | 100 | MHz | Unused |
| | $F_{CLK_CD1A1}$ | 100 | 100 | 100 | MHz | Unused |
| | $F_{CLK_CD1B0}$ | 100 | 100 | 100 | MHz | Unused |
| | $F_{CLK_CD1B1}$ | 100 | 100 | 100 | MHz | Unused |
| | $F_{CLK_CD2}$ | 200 | 200 | 200 | MHz | Unused |
| | $F_{CLK_CD2A0}$ | 200 | 200 | 200 | MHz | |
| | $F_{CLK_CD2A1}$ | 200 | 200 | 200 | MHz | Unused |
| | $F_{CLK_CD2B0}$ | 200 | 200 | 200 | MHz | Unused |
| | $F_{CLK_CD2B1}$ | 200 | 200 | 200 | MHz | Unused |
| | $F_{CLK_CD3}$ | 80 | 80 | 80 | MHz | Unused |
| | $F_{CLK_CD3A0}$ | 80 | 80 | 80 | MHz | |
| | $F_{CLK_CD3A1}$ | 80 | 80 | 80 | MHz | Unused |

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Max *1 | Max *2 | Max *3 | | |
| Internal clock frequency | $F_{CLK_CD3B0}$ | 80 | 80 | 80 | MHz | Unused |
| | $F_{CLK_CD3B1}$ | 80 | 80 | 80 | MHz | Unused |
| | $F_{CLK_CD4}$ | 200 | 200 | 200 | MHz | |
| | $F_{CLK_CD4A0}$ | 200 | 200 | 200 | MHz | Unused |
| | $F_{CLK_CD4A1}$ | 200 | 200 | 200 | MHz | Unused |
| | $F_{CLK_CD4B0}$ | 200 | 200 | 200 | MHz | Unused |
| | $F_{CLK_CD4B1}$ | 200 | 200 | 200 | MHz | Unused |
| | $F_{CLK_CD5}$ | 240 | 240 | 240 | MHz | |
| | $F_{CLK_CD5A0}$ | 120 | 120 | 120 | MHz | |
| | $F_{CLK_CD5A1}$ | 120 | 120 | 120 | MHz | Unused |
| | $F_{CLK_CD5B0}$ | 60 | 60 | 60 | MHz | |
| | $F_{CLK_CD5B1}$ | 60 | 60 | 60 | MHz | Unused |
| | $F_{CLK_HSSPI}$ | 200 | 200 | 200 | MHz | |
| | $F_{CLK_SYSC0H}$ | 80 | 66.7 | 60 | MHz | |
| | $F_{CLK_COMH}$ | 80 | 66.7 | 60 | MHz | |
| | $F_{CLK_RAM0H}$ | 80 | 66.7 | 60 | MHz | |
| | $F_{CLK_RAM1H}$ | 80 | 66.7 | 60 | MHz | |
| | $F_{CLK_SYSC0P}$ | 80 | 66.7 | 60 | MHz | |
| | $F_{CLK_COMP}$ | 80 | 66.7 | 60 | MHz | |

*1: Target maximum clock frequencies when CPU clock = 240MHz

*2: Target maximum clock frequencies when CPU clock = 200MHz

*3: Target maximum clock frequencies when CPU clock = 180MHz

*4: The PLLx/SSCGx cannot set under 200MHz.

- Note that Ta = 125 condition is not supported in this product type.

When using SSCG_PLL output for these internal clock, the MAX value of frequency has the following restrictions.

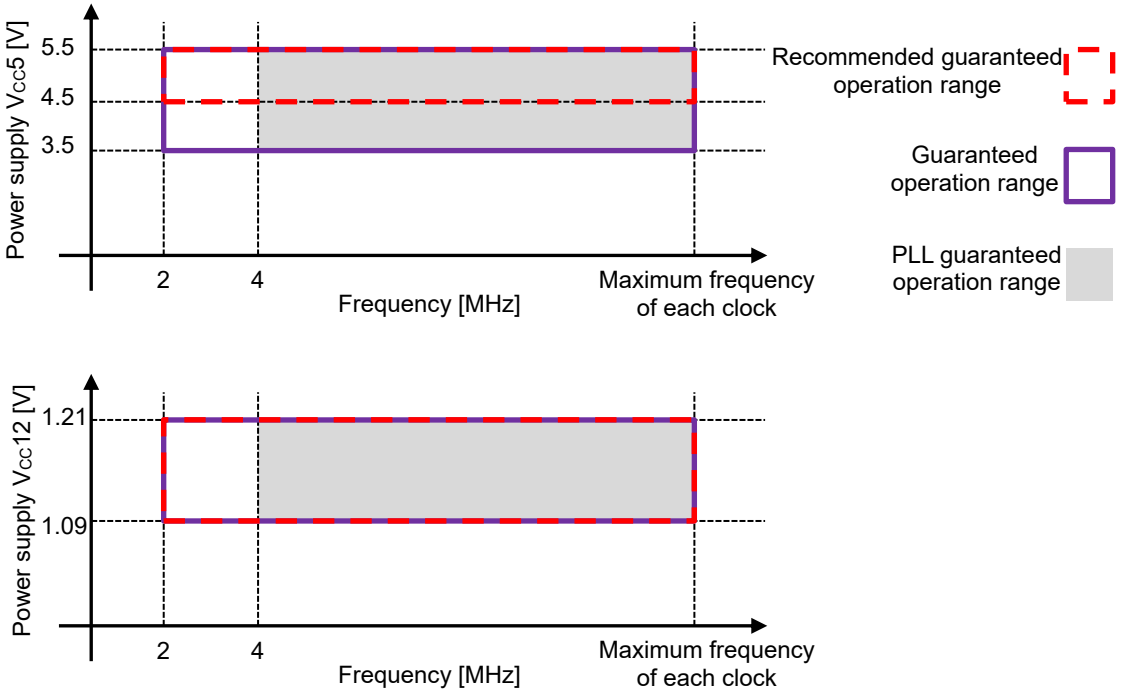
- On the presumption that the modulation mode of SSCG_PLL is used with down spread,

the MAX value of the frequency is standardized.

- This means that MAX value of frequency is the maximum value when SSCG_PLL was modulated.
- "Unused" means a clock source which doesn't have any supply destinations. Configure it as disable with performing at the lower clock frequency than the described maximum.

- Operation assurance range

Relationship between the internal clock frequency and supply voltage

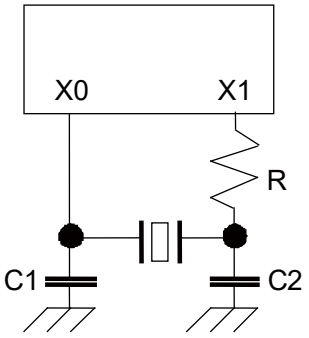



Note: CPU will be reset, when the power supply voltage is equal to or less than LVD setting voltage.

- Relationship between the oscillation clock frequency and internal clock frequency

| | | Internal Operation Clock Frequency | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Main Clock | PLL Clock | | | | | | |
| | | | Multiplied by 1 | Multiplied by 2 | | Multiplied by 15 | Multiplied by 30 | Multiplied by 40 | Multiplied by 60 |
| Oscillation clock frequency [MHz] | 4 | 2 | 4 | 8 | … | 60 | 120 | 160 | 240 |
| | 8 | 4 | 8 | 16 | … | 120 | 240 | | |
| | 16 | 8 | 16 | 32 | … | 240 | | | |

- Oscillation circuit example

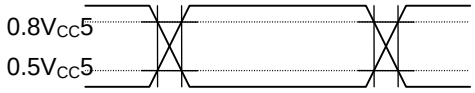



Note:
For the configuration of an oscillation circuit, request the oscillator manufacturer to perform a circuit matching evaluation before starting design.

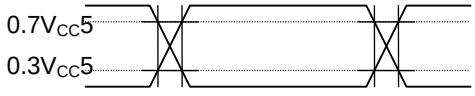
AC characteristics are specified by the following measurement reference voltage values.

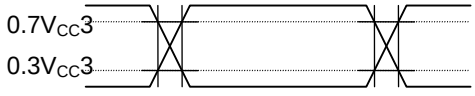
- Input signal waveform

Hysteresis input pin (Automotive)

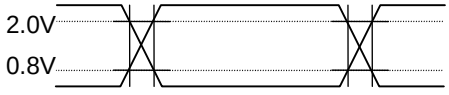



Hysteresis input pin (CMOS Schmitt)



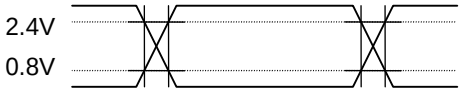




Hysteresis input pin (TTL)




- Output signal waveform

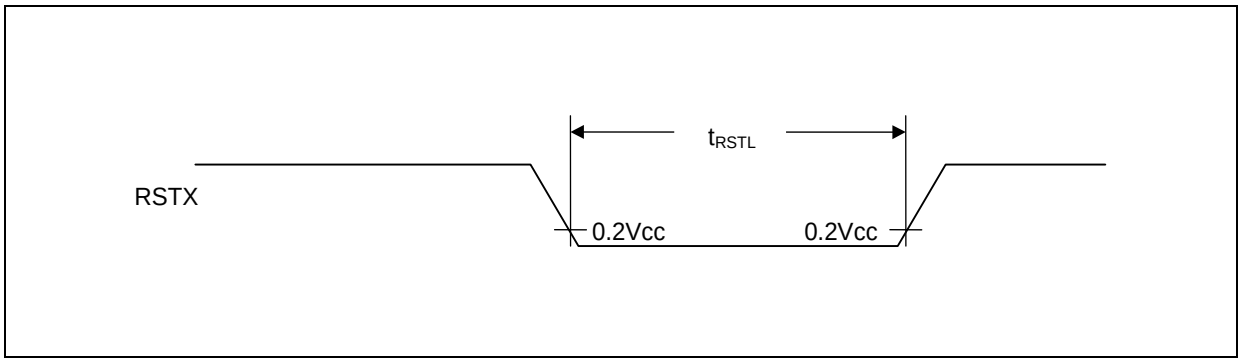
Output pin



### 9.1.4.4 *Reset Input*

($T_A$: Recommended operating conditions, Vcc5 = 5.0 V ±10 %, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | RSTX | - | 10 | - | µs | |
| Width for reset input removal | | | | 1 | - | µs | |



### 9.1.4.5 Power-on Conditions

($T_A$: Recommended operating conditions, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Level detection voltage | - | VCC5 | - | 2.2 | 2.4 | 2.6 | V | |
| Level detection hysteresis width | - | VCC5 | - | - | 100 | - | mV | |
| Level detection time | - | - | - | - | - | 40 | µs | *1 |
| Power off time | $t_{OFF}$ | VCC5 | - | 100 | - | - | µs | *2 |
| Power ramp rate | dV/dt | VCC5 | VCC5: 1.5 V to 2.6 V | - | - | 1 | V/µs | *3 |
| Maximum ramp rate guaranteed to not generate power-on reset | \|dV/dt\| | VCC5 | VCC5: Between 2.4 V and 4.5 V | - | - | 50 | mV/µs | *4 |

*1: This specification is at 1 V/µs of power ramp rate.

*2: VCC5 must be held below 1.5 V for a minimum period of $t_{OFF}$.

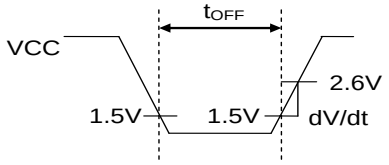
*3: Power ramp rate must be 1 V/us or less from 1.5 V to 2.6 V.
Power-on can detect by satisfying power ramp rate when power off time is satisfied.

*4: This specification is specified the power supply fluctuation after power on detection. When VCC5 voltage is between 2.4 V and 4.5 V, the power supply fluctuation is below 50 mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5 V and 5.5 V.

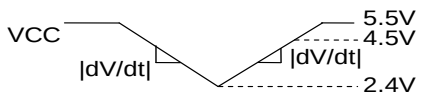
***Notes:***

When using S6J3310/20/30/40, *2 and *3 must be satisfied. When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power up and any brownout event.

- **Power off time, Power ramp rate**




- **Maximum ramp rate guaranteed to not generate power-on reset**



*9.1.4.6 Multi-Function Serial*

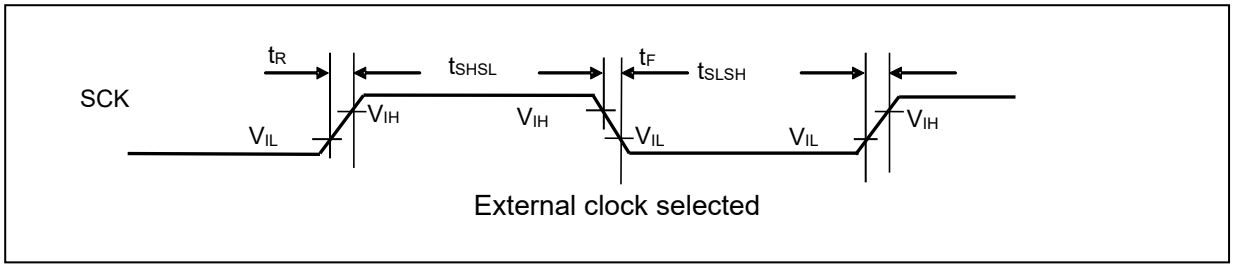
UART (asynchronous serial interface) timing (SMR:MD2-0 = 0b000, 0b001)

**(1) External Clock Selected (BGR:EXT = 1)**

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ±0.3 V, Vcc5 = DVcc = 5.0 V ± 10 % /3.3 V ± 0.3 V, Vcc53 = 5.0 V ±10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}12$ = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK4, SCK8 to SCK12 | - | $t_{CLK_LCPnA}$*1 +10 | - | ns | |
| | | SCK16 to SCK17 | | $t_{CLK_COMP}$ +10 | - | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK4, SCK8 to SCK12 | | $t_{CLK_LCPnA}$*1 +10 | - | ns | |
| | | SCK16 to SCK17 | | $t_{CLK_COMP}$ +10 | - | ns | |
| SCK falling time | $t_F$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 | | - | 5 | ns | |
| SCK rising time | $t_R$ | | | - | 5 | ns | |

*1: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12



External clock selected

CSIO timing (SMR:MD2-0 = 0b010)

### (1) Normal Synchronous Transfer (SCR:SPI = 0) and Mark Level "H" of Serial Clock Output (SMR:SCINV = 0)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 % /3.3 V ± 0.3 V, Vcc53 = 5.0 V ±10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}12$ = 1.15 V ± 0.06 V)

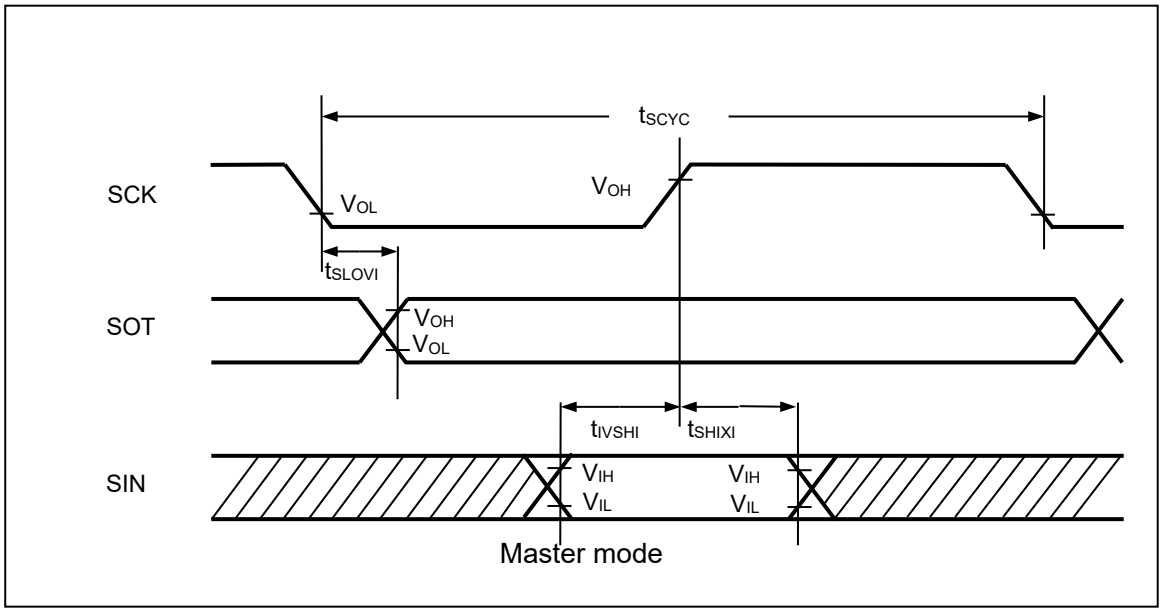
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12 | Master Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $8t_{CLK_LCPnA}$*1 | - | ns | - |
| | | SCK16 to SCK17 | | $8t_{CLK_COMP}$ | - | ns | |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0, SOT1, SOT2_1, SOT3_1, SOT4, SOT8 to SOT12, SOT16 to SOT17 | | -30 | +30 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0, SIN1, SIN2_1, SIN3_1, SIN4, SIN8 to SIN12, SIN16 to SIN17 | | 40 | - | ns | |
| SCK ↑→ Valid SIN hold time | $t_{SHIXI}$ | | | 0 | - | ns | |
| Serial clock cycle time | $t_{SCYC}$ | SCK2_0, SCK3_0 | Master Mode (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $2t_{CLK_LCPnA}$*1 | - | ns | - |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK2_0, SCK3_0, SOT2_0, SOT3_0 | | -7.5 | +7.5 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCK2_0, SCK3_0, SIN2_0, SIN3_0 | | 10 | - | ns | |
| SCK ↑→ Valid SIN hold time | $t_{SHIXI}$ | | | 0 | - | ns | |

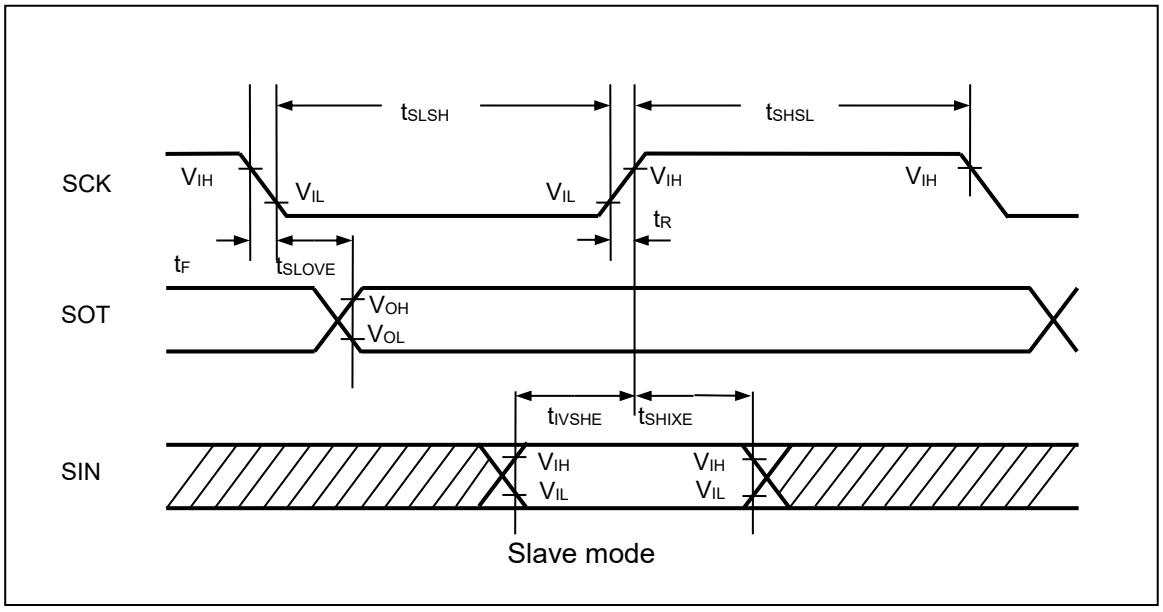
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK4, SCK8 to SCK12 | Slave Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $4t_{CLK_LCPnA}$*1 | - | ns | - |
| | | SCK16 to SCK17 | | $4t_{CLK_COMP}$ | - | ns | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK4, SCK8 to SCK12 | | $4t_{CLK_LCPnA}$*1 | - | ns | |
| | | SCK16 to SCK17 | | $4t_{CLK_COMP}$ | - | ns | |
| SCK ↓→ SOT delay time | $t_{SLOVE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | - | 40 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17 | | 10 | - | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | | | 10 | - | ns | |
| SCK falling time | $t_F$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 | | - | 5 | ns | |
| SCK rising time | $t_R$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 | | - | 5 | ns | |

*1: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

***Notes:***

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the Traveo™ Platform Hardware Manual.*




SCK
SOT
SIN
tSLSH
tSHSL
VIH
VIL
VIL
VIH
VIH
tR
tF
tSLOVE
VOH
VOL
tIVSHE
tSHIXE
VIH
VIL
VIH
VIL
Slave mode

### (2) Normal Synchronous Transfer (SCR:SPI = 0) and Mark Level "L" of Serial Clock Output (SMR:SCINV = 1)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10% /3.3 V ± 0.3 V, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}12$ = 1.15 V ± 0.06 V)

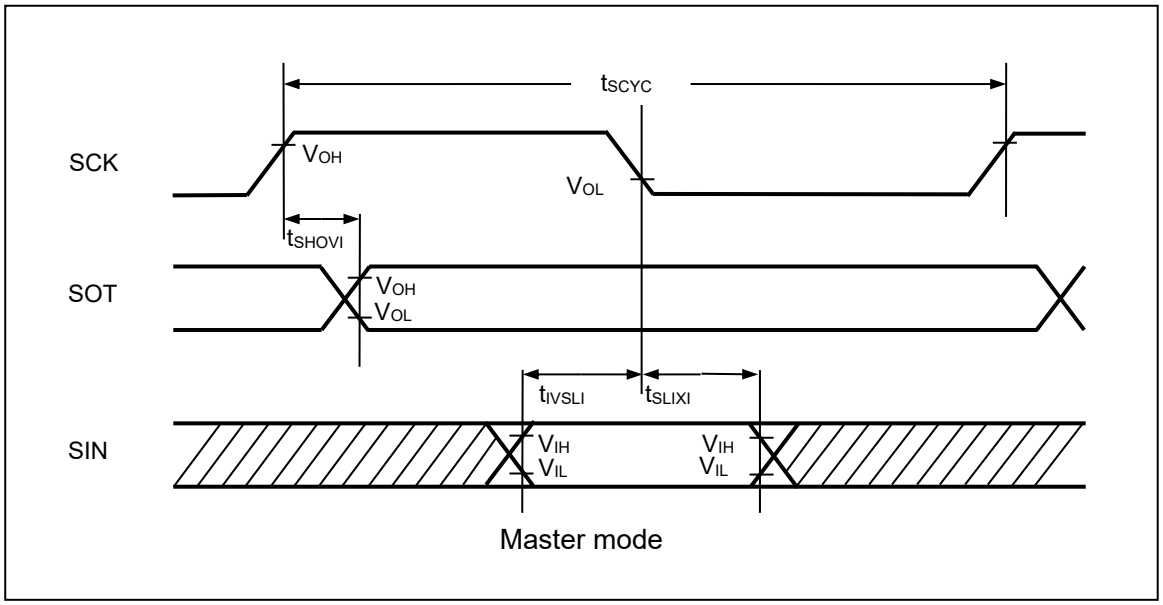
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12 | Master Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $8t_{CLK_LCPnA}$*1 | - | ns | |
| | | SCK16 to SCK17 | | $8t_{CLK_COMP}$ | - | ns | |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0, SOT1, SOT2_1, SOT3_1, SOT4, SOT8 to SOT12, SOT16 to SOT17 | | -30 | +30 | ns | |
| Valid SIN → SCK ↓ setup time | $t_{IVSLI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0, SIN1, SIN2_1, SIN3_1, SIN4, SIN8 to SIN12, SIN16 to SIN17 | | 40 | - | ns | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | | | 0 | - | ns | |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK2_0, SCK3_0 | Master Mode (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $2t_{CLK_LCPnA}$*1 | - | ns | |
| SCK ↓ → SOT delay time | $t_{SHOVI}$ | SCK2_0, SCK3_0, SOT2_0, SOT3_0 | | -7.5 | +7.5 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSLI}$ | SCK2_0, SCK3_0, SIN2_0, SIN3_0 | | 10 | - | ns | |
| SCK ↑→ Valid SIN hold time | $t_{SLIXI}$ | | | 0 | - | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK4, SCK8 to SCK12 | Slave Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $4t_{CLK_LCPnA}$*1 | - | ns | |
| | | SCK16 to SCK17 | | $4t_{CLK_COMP}$ | - | ns | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK4, SCK8 to SCK12 | | $4t_{CLK_LCPnA}$*1 | - | ns | |
| | | SCK16 to SCK17 | | $4t_{CLK_COMP}$ | - | ns | |
| SCK ↑ → SOT delay time | $t_{SHOVE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | - | 40 | ns | |
| Valid SIN → SCK ↓ setup time | $t_{IVSLE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17 | | 10 | - | ns | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXE}$ | | | 10 | - | ns | |
| SCK falling time | $t_F$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 | | - | 5 | ns | |
| SCK rising time | $t_R$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 | | - | 5 | ns | |

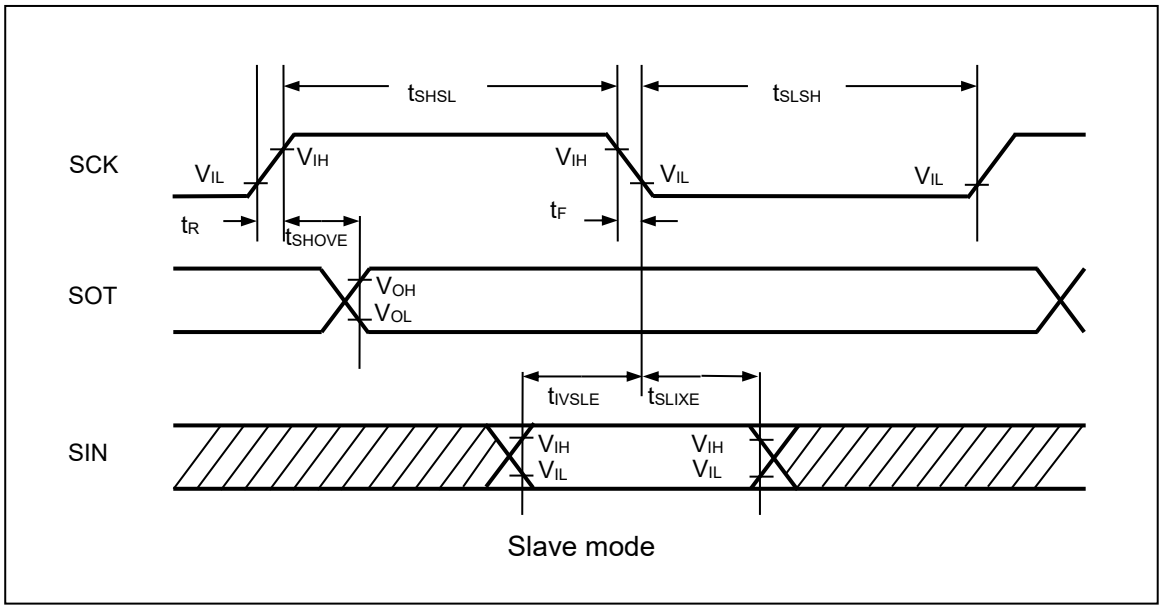
*1: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

***Notes:***

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the Traveo™ Platform Hardware Manual.*




Master mode




Slave mode

### (3) SPI Supported (SCR:SPI = 1), and Mark Level "H" of Serial Clock Output (SMR:SCINV = 0)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 % /3.3 V ± 0.3 V, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}12$ = 1.15 V ± 0.06 V)

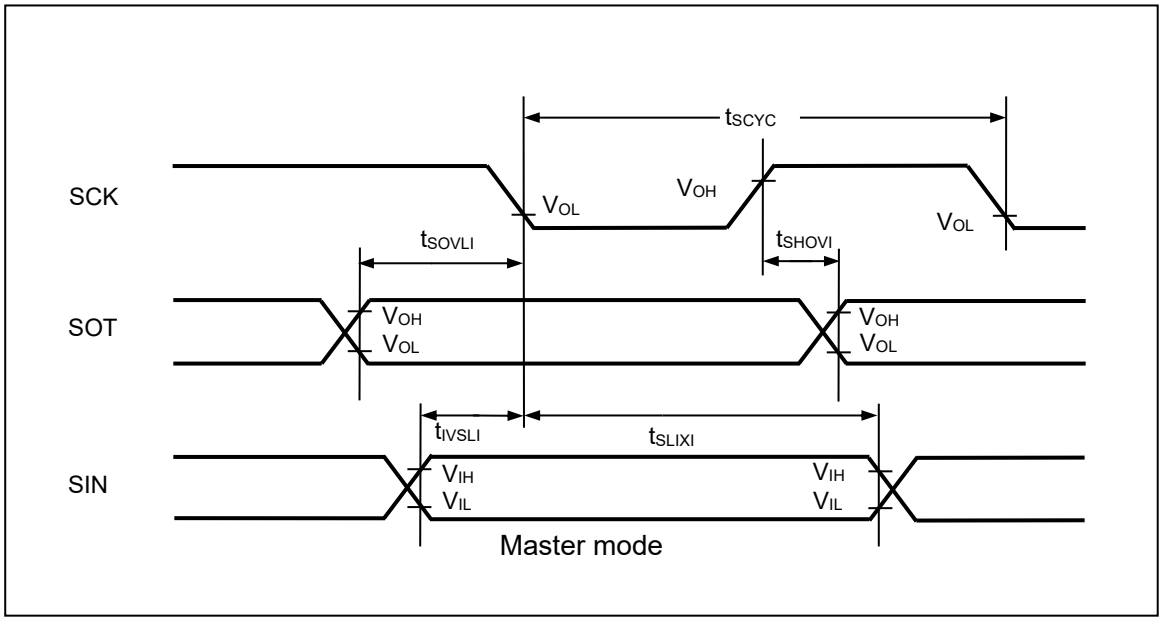
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12 | Master Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $8t_{CLK_LCPnA}$*1 | - | ns | - |
| | | SCK16 to SCK17 | | $8t_{CLK_COMP}$ | - | ns | |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0, SOT1, SOT2_1, SOT3_1, SOT4, SOT8 to SOT12, SOT16 to SOT17 | | -30 | +30 | ns | |
| Valid SIN → SCK ↓ setup time | $t_{IVSLI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0, SIN1, SIN2_1, SIN3_1, SIN4, SIN8 to SIN12, SIN16 to SIN17 | | 40 | - | ns | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | | | 0 | - | ns | |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0, SOT1, SOT2_1, SOT3_1, SOT4, SOT8 to SOT12, SOT16 to SOT17 | | $4t_{CLK_LCPnA}$*1 - 30 | - | ns | |
| | | SCK16 to SCK17 SOT16 to SOT17 | | $4t_{CLK_COMP}$*1 - 30 | - | ns | - |
| Serial clock cycle time | $t_{SCYC}$ | SCK2_0, SCK3_0 | Master Mode (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $2t_{CLK_LCPnA}$*1 | - | ns | - |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK2_0, SCK3_0, SOT2_0, SOT3_0 | | -7.5 | +7.5 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCK2_0, SCK3_0, SIN2_0, SIN3_0 | | 10 | - | ns | |
| SCK ↑→ Valid SIN hold time | $t_{SHIXI}$ | | | 0 | - | ns | |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK2_0, SCK3_0, SOT2_0, SOT3_0 | | $t_{CLK_LCPnA}$*1 - 7.5 | - | ns | |

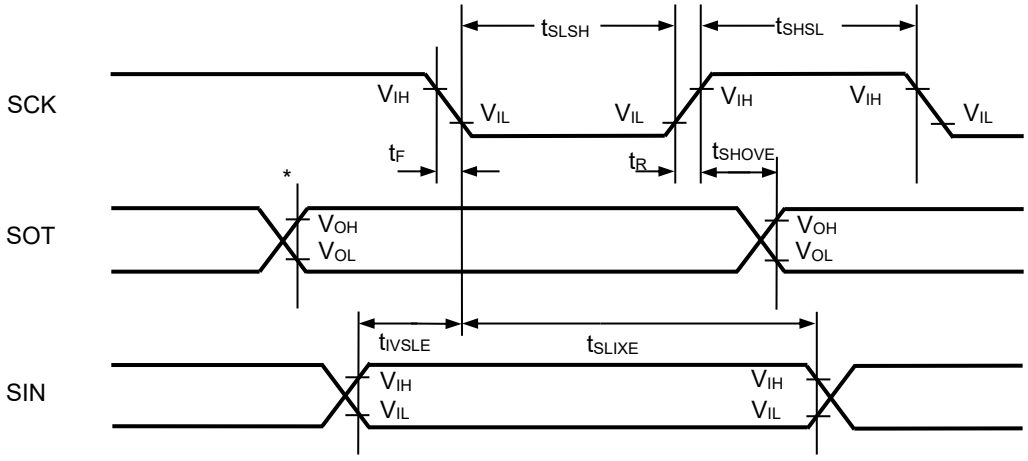
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK4, SCK8 to SCK12 | Slave Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $4t_{CLK_LCPnA}$*1 | - | ns | |
| | | SCK16 to SCK17 | | $4t_{CLK_COMP}$ | - | ns | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK4, SCK8 to SCK12 | | $4t_{CLK_LCPnA}$*1 | - | ns | |
| | | SCK16 to SCK17 | | $4t_{CLK_COMP}$ | - | ns | |
| SCK ↑ → SOT delay time | $t_{SHOVE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | - | 40 | ns | |
| Valid SIN → SCK ↓ setup time | $t_{IVSLE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17 | | 10 | - | ns | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXE}$ | | | 10 | - | ns | |
| SCK falling time | $t_F$ | SCK0 to SCK4, SCK8 to SCK12 SCK16 to SCK17 | | - | 5 | ns | |
| SCK rising time | $t_R$ | SCK0 to SCK4, SCK8 to SCK12 SCK16 to SCK17 | | - | 5 | ns | |

*1: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

***Notes:***

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the Traveo™ Platform Hardware Manual.*






* Changes when writing to the TDR register

Slave mode

### (4) SPI Supported (SCR:SPI = 1), and Mark Level "L" of Serial Clock Output (SMR:SCINV = 1)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 % /3.3 V ± 0.3 V, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}12$ = 1.15 V ± 0.06 V)

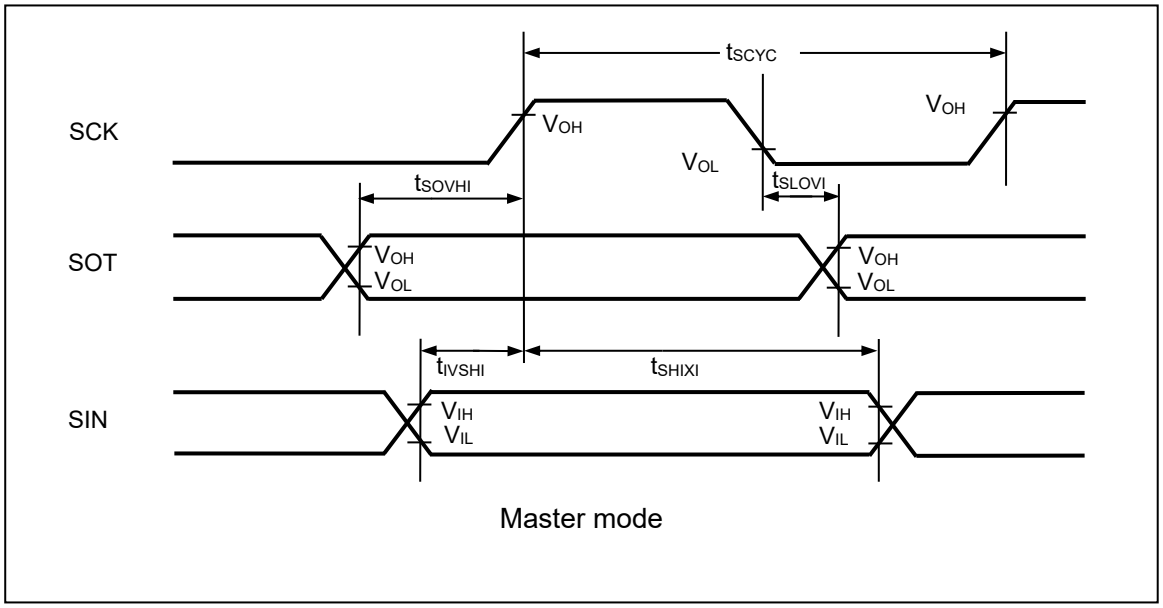
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12 | Master Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $8t_{CLK_LCPnA}$*1 | - | ns | - |
| | | SCK16 to SCK17 | | $8t_{CLK_COMP}$ | - | ns | |
| SCK ↓ -> SOT delay time | $t_{SLOVI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0, SOT1, SOT2_1, SOT3_1, SOT4, SOT8 to SOT12, SOT16 to SOT17 | | -30 | +30 | ns | |
| Valid SIN -> SCK ↑ setup time | $t_{IVSHI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0, SIN1, SIN2_1, SIN3_1, SIN4, SIN8 to SIN12, SIN16 to SIN17 | | 40 | - | ns | |
| SCK ↑ -> Valid SIN hold time | $t_{SHIXI}$ | | | 0 | - | ns | |
| SOT -> SCK ↑ delay time | $t_{SOVHI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0, SOT1, SOT2_1, SOT3_1, SOT4, SOT8 to SOT12, SOT16 to SOT17 | | $4t_{CLK_LCPnA}$*1 - 30 | - | ns | |
| | | SCK16 to SCK17 SOT16 to SOT17 | | $4t_{CLK_COMP}$ - 30 | - | ns | |
| Serial clock cycle time | $t_{SCYC}$ | SCK2_0, SCK3_0 | Master Mode (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $2t_{CLK_LCPnA}$*1 | - | ns | - |
| SCK ↓ -> SOT delay time | $t_{SLOVI}$ | SCK2_0, SCK3_0, SOT2_0, SOT3_0 | | -7.5 | +7.5 | ns | |
| Valid SIN -> SCK ↑ setup time | $t_{IVSHI}$ | SCK2_0, SCK3_0, SIN2_0, SIN3_0 | | 10 | - | ns | |
| SCK ↑ -> Valid SIN hold time | $t_{SHIXI}$ | | | 0 | - | ns | |
| SOT -> SCK ↑ delay time | $t_{SOVHI}$ | SCK2_0, SCK3_0, SOT2_0, SOT3_0 | | $t_{CLK_LCPnA}$*1 - 7.5 | - | ns | |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK4, SCK8 to SCK12 | Slave Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $4t_{CLK_LCPnA}$*1 | - | ns | - |
| | | SCK16 to SCK17 | | $4t_{CLK_COMP}$ | - | ns | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK4, SCK8 to SCK12 | | $4t_{CLK_LCPnA}$*1 | - | ns | |
| | | SCK16 to SCK17 | | $4t_{CLK_COMP}$ | - | ns | |
| SCK ↓ -> SOT delay time | $t_{SLOVE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | - | 40 | ns | |
| Valid SIN -> SCK ↑ setup time | $t_{IVSHE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17 | | 10 | - | ns | |
| SCK ↑ -> Valid SIN hold time | $t_{SHIXE}$ | | | 10 | - | ns | |
| SCK falling time | $t_F$ | SCK0 to SCK4, SCK8 to SCK12 SCK16 to SCK17 | | - | 5 | ns | |
| SCK rising time | $t_R$ | SCK0 to SCK4, SCK8 to SCK12 SCK16 to SCK17 | | - | 5 | ns | |

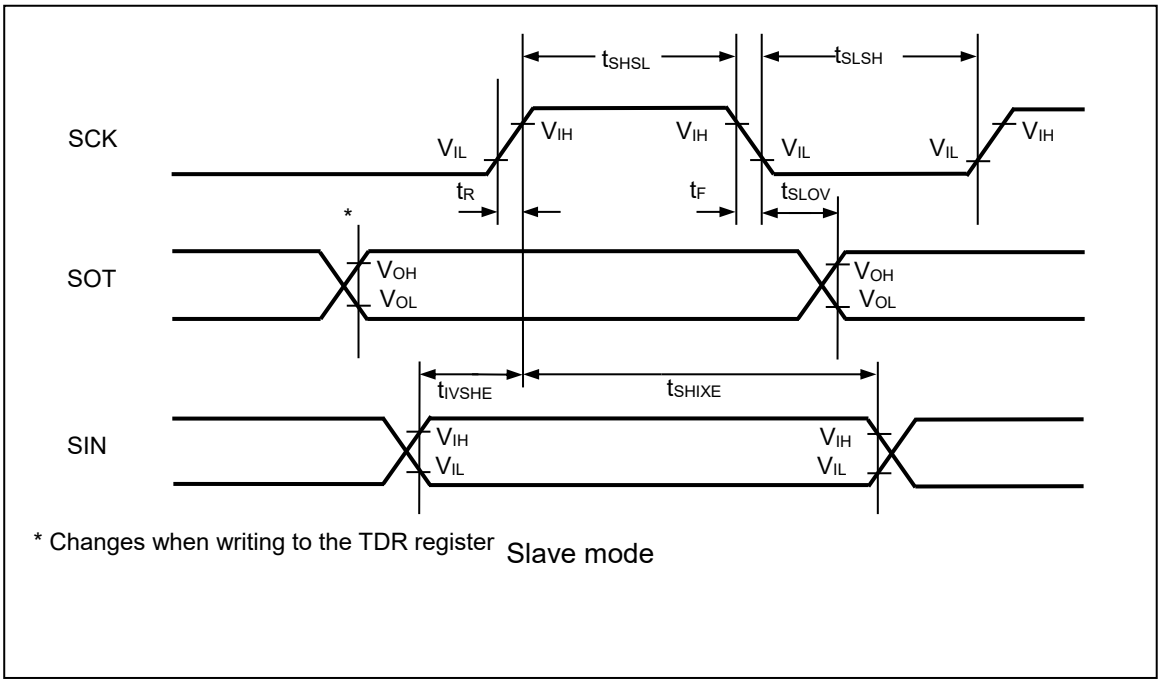
*1: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

***Notes:***

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the Traveo™ Platform Hardware Manual.*




Master mode




* Changes when writing to the TDR register

Slave mode

### (5) Serial Chip Select Used (SCSCR:CSEN = 1)

■Mark level "H" of serial clock output (SMR, SCSFR:SCINV = 0)

■Inactive level "H" of serial chip select (SCSCR, SCSFR:CSLVL = 1)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10% /3.3 V ± 0.3 V, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}$12 = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS ↑ → SCK ↓ setup time | $t_{CSSI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x, SCS16x to SCS17x | Master Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $t_{CSSU}$*1-15 | - | ns | |
| SCK ↑ → SCS ↑ hold time | $t_{CSHI}$ | | | $t_{CSHD}$*2+0 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x | | $t_{CSDS}$*3-15 +5$t_{CLK_LCPnA}$*4 | - | ns | |
| | | SCS16x to SCS17x | | $t_{CSDS}$*3-15 +5$t_{CLK_COMP}$ | - | ns | |
| SCS ↑ → SCK ↓ setup time | $t_{CSSI}$ | SCK2_0, SCK3_0, SCS2x_0, SCS3x_0 | Master Mode (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $t_{CSSU}$*1-10 | - | ns | |
| SCK ↑ → SCS ↑ hold time | $t_{CSHI}$ | | | $t_{CSHD}$*2+0 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS2x_0, SCS3x_0 | | $t_{CSDS}$*3-10 +5$t_{CLK_LCPnA}$*4 | - | ns | |
| SCS ↓ → SCK ↓ setup time | $t_{CSSE}$ | SCK0 to SCK4, SCK8 to SCK12 SCS0x to SCS4x, SCS8x to SCS12x | Slave Mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | 4$t_{CLK_LCPnA}$*4 +15 | - | ns | |
| | | SCK16 to SCK17, SCS16x to SCS17x | | 4$t_{CLK_COMP}$ +15 | - | ns | |
| SCK ↑ → SCS ↑ hold time | $t_{CSHE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17, SCS0x to SCS4x, SCS8x to SCS12x, SCS16x to SCS17x | | 0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS0x to SCS4x, SCS8x to SCS12x | | 4$t_{CLK_LCPnA}$*4 +15 | - | ns | |
| | | SCS16x to SCS17x | | 4$t_{CLK_COMP}$ +15 | - | ns | |
| SCS ↓ → SOT delay time | $t_{DSE}$ | SCS0x to SCS4x, SCS8x to SCS12x, SCS16x to SCS17x, SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | - | 40 | ns | |
| SCS ↑ → SOT delay time | $t_{DEE}$ | | | 0 | - | ns | |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCK ↓ → SCS ↓ clock switching time | $t_{SCC}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x | Master mode round operation (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $4t_{CLK_LCPnA}$*4 +0 | $4t_{CLK_LCPnA}$*4 +15 | ns | |
| | | SCK16 to SCK17 SCS16x to SCS17x | | $4t_{CLK_COMP}$ +0 | $4t_{CLK_COMP}$ +15 | ns | |
| | | SCK2_0, SCK3_0, SCS2x_0, SCS3x_0 | Master mode round operation (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $4t_{CLK_LCPnA}$*4 +0 | $4t_{CLK_LCPnA}$*4 +10 | ns | |

*1: $t_{CSSU}$ = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: $t_{CSHD}$ = SCSTR:CSHD[7:0] x serial chip select timing operating clock

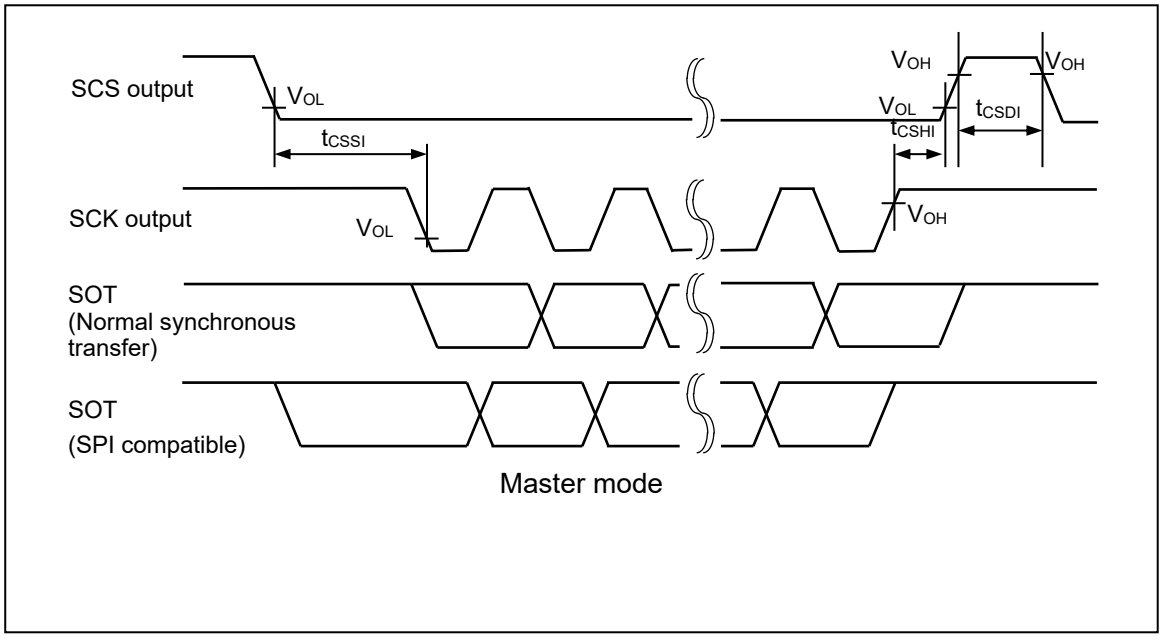
*3: $t_{CSDS}$ = SCSTR:CSDS[15:0] x serial chip select timing operating clock

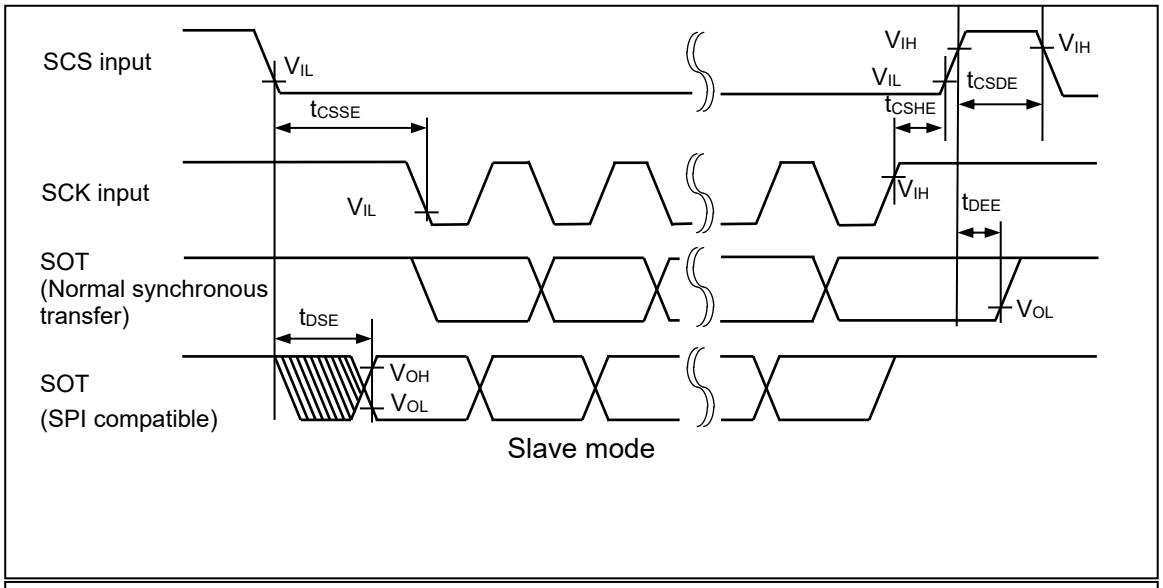
For details on *1, *2, and *3 above, see the Traveo™ Platform Hardware Manual.

*4 $t_{CLK_LCPnA}$ n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

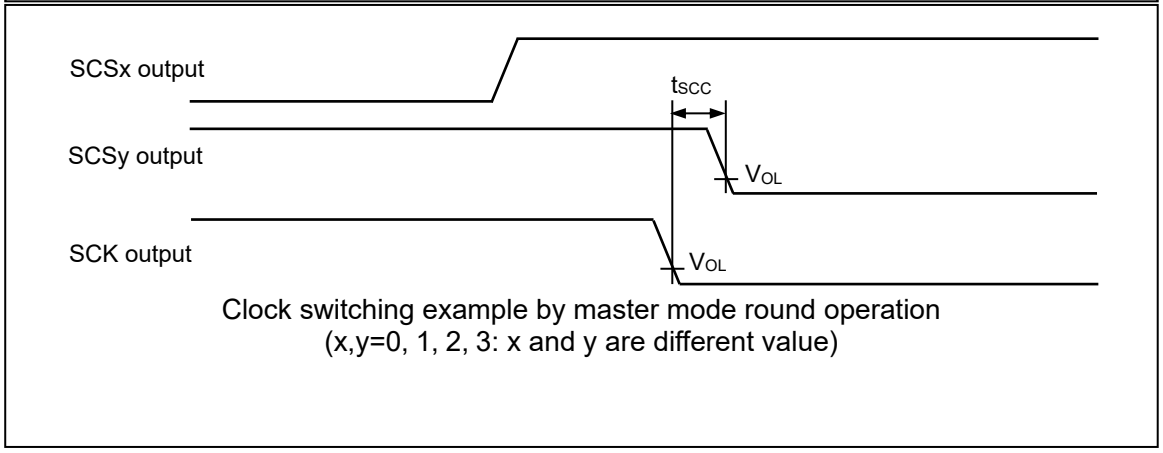
***Notes:***

- *This is the AC characteristic in CLK synchronized mode.*
- *CL is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the Traveo™ Platform Hardware Manual.*






Slave mode




Clock switching example by master mode round operation
(x,y=0, 1, 2, 3: x and y are different value)

### (6) Serial Chip Select Used (SCSCR:CSEN = 1)

■Serial clock output signal detect level "L" (SMR, SCSFR:SCINV = 1)

■Serial chip select inactive level "H" (SCSCR, SCSFR:CSLVL = 1)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 % /3.3 V ± 0.3 V, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}12$ = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS ↓→ SCK ↑ setup time | $t_{CSSI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x, SCS16x to SCS17x | Master mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $t_{CSSU}$*1-15 | - | ns | |
| SCK ↓→ SCS ↑ hold time | $t_{CSHI}$ | | | $t_{CSHD}$*2+0 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x | | $t_{CSDS}$*3-15 +5$t_{CLK_LCPnA}$*4 | - | ns | |
| | | SCS16x to SCS17x | | $t_{CSDS}$*3-15 +5$t_{CLK_COMP}$ | - | ns | |
| SCS ↓→ SCK ↑ setup time | $t_{CSSI}$ | SCK2_0, SCK3_0, SCS2x_0, SCS3x_0 | Master Mode (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $t_{CSSU}$*1-10 | - | ns | |
| SCK ↓→ SCS ↑ hold time | $t_{CSHI}$ | | | $t_{CSHD}$*2+0 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS2x_0, SCS3x_0 | | $t_{CSDS}$*3-10 +5$t_{CLK_LCPnA}$*4 | - | ns | |
| SCS ↓ → SCK ↑ setup time | $t_{CSSE}$ | SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x | Slave mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | 4$t_{CLK_LCPnA}$*4 +15 | - | ns | |
| | | SCK16 to SCK17, SCS16x to SCS17x | | 4$t_{CLK_COMP}$ +15 | - | ns | |
| SCK ↓ → SCS ↑ hold time | $t_{CSHE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17, SCS0x to SCS4x, SCS8x to SCS12x, SCS16x to SCS17x | | 0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS0x to SCS4x, SCS8x to SCS12x | | 4$t_{CLK_LCPnA}$*4 +15 | - | ns | |
| | | SCS16x to SCS17x | | 4$t_{CLK_COMP}$ +15 | - | ns | |
| SCS ↓ → SOT delay time | $t_{DSE}$ | SCS0x to SCS4x, SCS8x to SCS12x, SCS16x to SCS17x, SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | - | 40 | ns | |
| SCS ↑ → SOT delay time | $t_{DEE}$ | | | 0 | - | ns | |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCK ↑ → SCS ↓ clock switching time | $t_{SCC}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x | Master mode round operation (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $4t_{CLK_LCPnA}$*4 +0 | $4t_{CLK_LCPnA}$*4 +15 | ns | |
| | | SCK16 to SCK17 SCS16x to SCS17x | | $4t_{CLK_COMP}$ +0 | $4t_{CLK_COMP}$ +15 | ns | |
| | | SCK2_0, SCK3_0, SCS2x_0, SCS3x_0 | Master mode round operation (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $4t_{CLK_LCPnA}$*4 +0 | $4t_{CLK_LCPnA}$*4 +10 | ns | |

*1: $t_{CSSU}$ = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: $t_{CSHD}$ = SCSTR:CSHD[7:0] x serial chip select timing operating clock

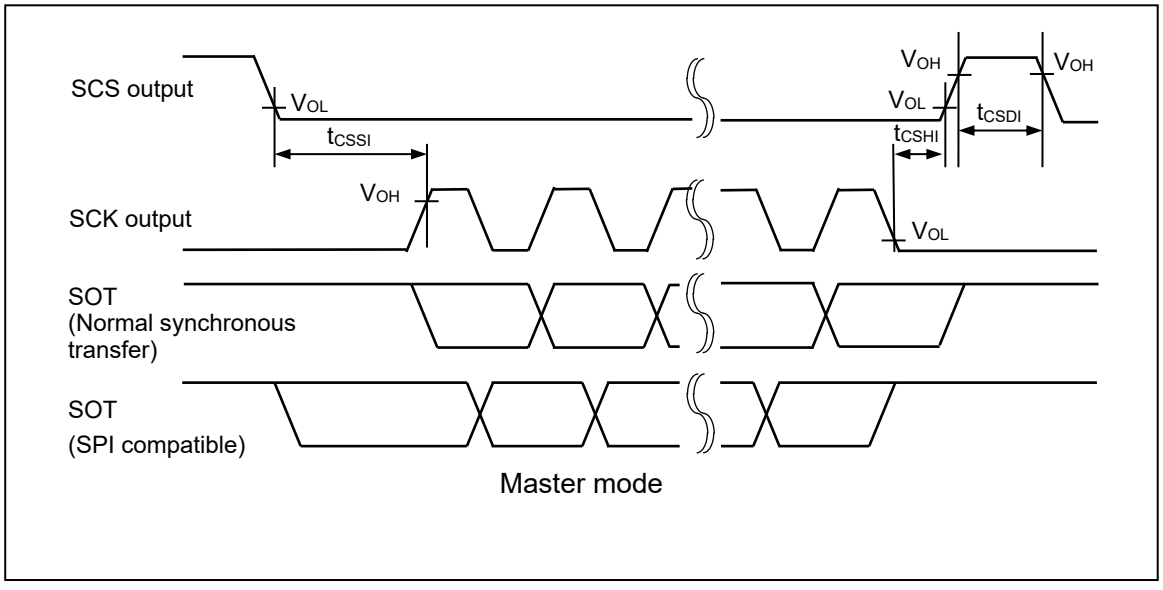
*3: $t_{CSDS}$ = SCSTR:CSDS[15:0] x serial chip select timing operating clock

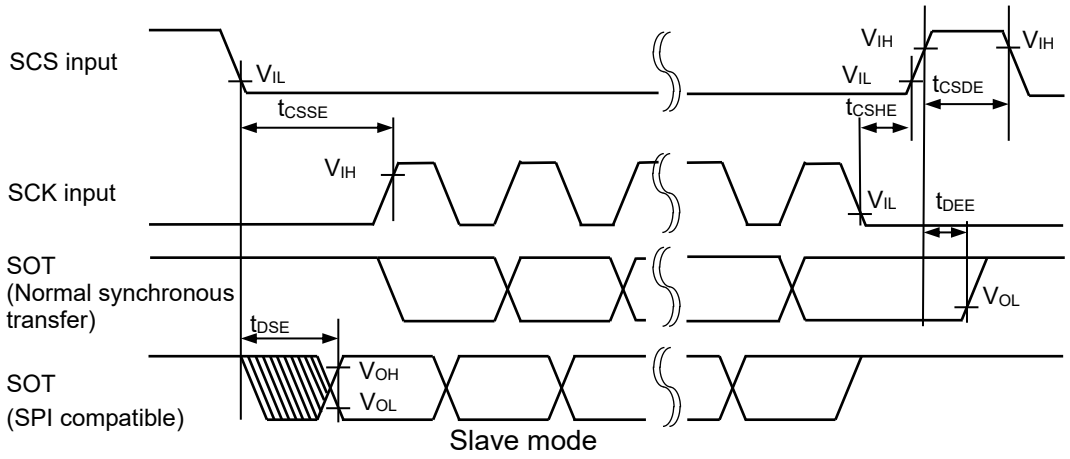
For details on *1, *2, and *3 above, see the Traveo™ Platform Hardware Manual.

*4 $t_{CLK_LCPnA}$ n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

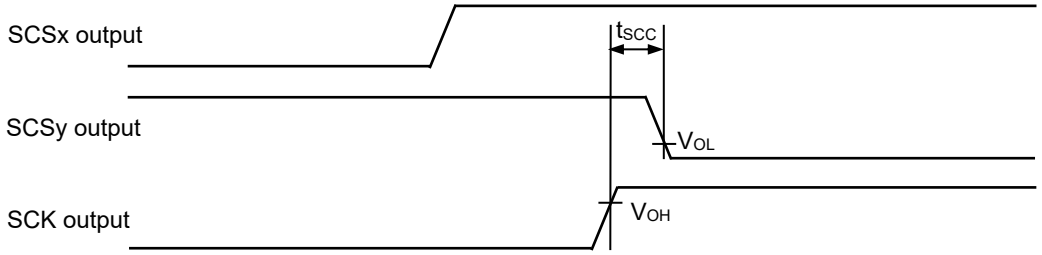
***Notes:***

- *This is the AC characteristic in CLK synchronized mode.*
- *CL is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the Traveo™ Platform Hardware Manual.*






Slave mode




Clock switching example by master mode round operation
(x,y=0, 1, 2, 3: x and y are different value)

### (7) Serial Chip Select Used (SCSCR:CSEN = 1)

■Serial clock output signal detect level "H" (SMR, SCSFR:SCINV = 0)

■Serial Chip select inactive level "L" (SCSCR, SCSFR:CSLVL = 0

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 % /3.3 V ± 0.3 V, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}$12 = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS ↑ → SCK ↓ setup time | $t_{CSSI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x, SCS16x to SCS17x | Master mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $t_{CSSU}$*1-15 | - | ns | |
| SCK ↑ → SCS ↓ hold time | $t_{CSHI}$ | | | $t_{CSHD}$*2+0 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x | | $t_{CSDS}$*3-15 +5 $t_{CLK_LCPnA}$*4 | - | ns | |
| | | SCS16x to SCS17x | | $t_{CSDS}$*3-15 +5$t_{CLK_COMP}$ | - | ns | |
| SCS ↑ → SCK ↓ setup time | $t_{CSSI}$ | SCK2_0, SCK3_0, SCS2x_0, SCS3x_0 | Master Mode (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $t_{CSSU}$*1-10 | - | ns | |
| SCK ↑ → SCS ↓ hold time | $t_{CSHI}$ | | | $t_{CSHD}$*2+0 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS2x_0, SCS3x_0 | | $t_{CSDS}$*3-10 +5$t_{CLK_LCPnA}$*4 | - | ns | |
| SCS ↑ → SCK ↓ setup time | $t_{CSSE}$ | SCK0 to SCK4, SCK8 to SCK12 SCS0x to SCS4x, SCS8x to SCS12x | Slave mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | 4$t_{CLK_LCPnA}$*4 +15 | - | ns | |
| | | SCK16 to SCK17, SCS16x to SCS17x | | 4$t_{CLK_COMP}$ +15 | - | ns | |
| SCK ↑ → SCS ↓ hold time | $t_{CSHE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17, SCS0x to SCS4x, SCS8x to SCS12x, SCS16x to SCS17x | | 0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS0x to SCS4x, SCS8x to SCS12x | | 4$t_{CLK_LCPnA}$*4 +15 | - | ns | |
| | | SCS16x to SCS17x | | 4$t_{CLK_COMP}$ +15 | - | ns | |
| SCS ↑ → SOT delay time | $t_{DSE}$ | SCS0x to SCS4x, SCS8x to SCS12x, SCS16x to SCS17x, SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | - | 40 | ns | |
| SCS ↓ → SOT delay time | $t_{DEE}$ | | | 0 | - | ns | |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCK ↓ → SCS ↑ clock switching time | $t_{SCC}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12 SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x | Master mode round operation (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $4t_{CLK_LCPnA}$ *4 +0 | $4t_{CLK_LCPnA}$ *4 +15 | ns | |
| | | SCK16 to SCK17 SCS16x to SCS17x | | $4t_{CLK_COMP}$ +0 | $4t_{CLK_COMP}$ +15 | ns | |
| | | SCK2_0, SCK3_0, SCS2x_0, SCS3x_0 | Master mode round operation (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $4t_{CLK_LCPnA}$ *4 +0 | $4t_{CLK_LCPnA}$ *4 +10 | ns | |

*1: $t_{CSSU}$ = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: $t_{CSHD}$ = SCSTR:CSHD[7:0] x serial chip select timing operating clock

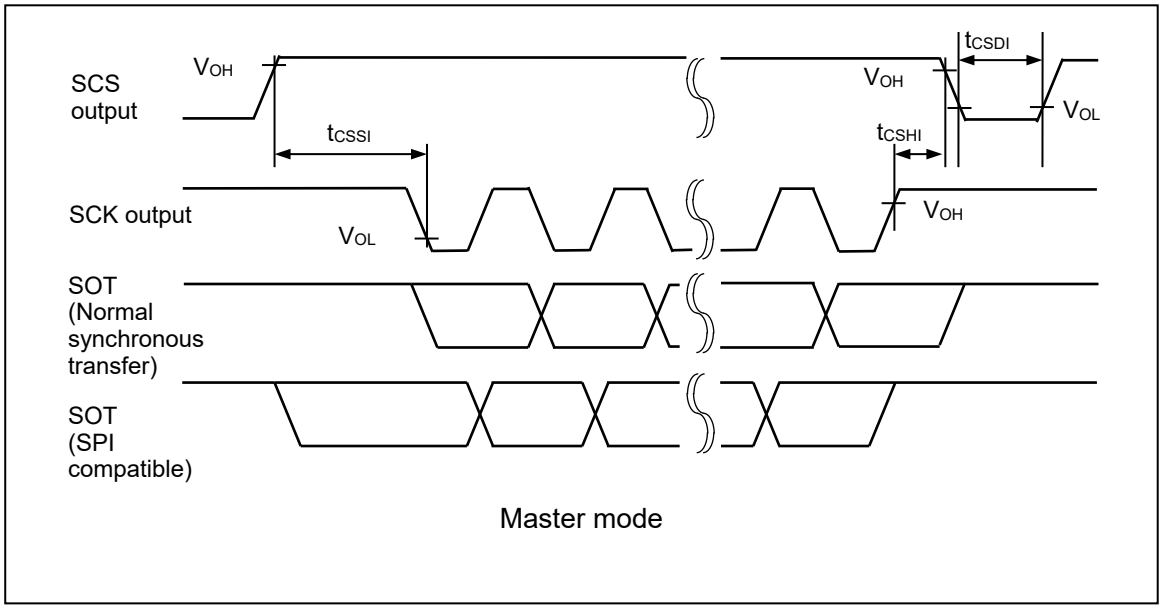
*3: $t_{CSDS}$ = SCSTR:CSDS[15:0] x serial chip select timing operating clock

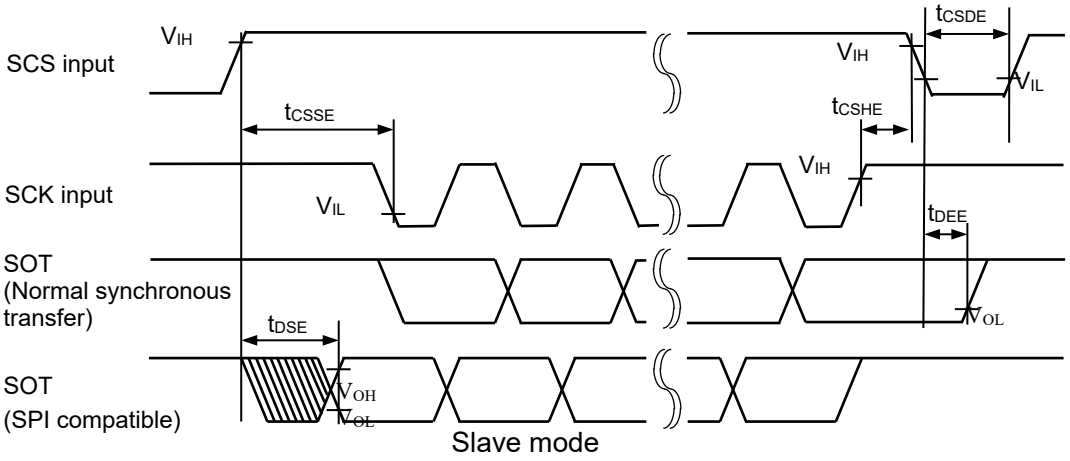
For details on *1, *2, and *3 above, see the Traveo™ Platform Hardware Manual.

*4 $t_{CLK_LCPnA}$ n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

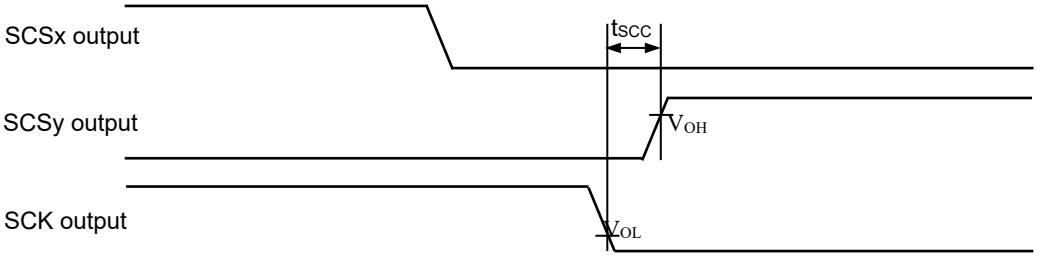
***Notes:***

- *This is the AC characteristic in CLK synchronized mode.*
- *CL is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the Traveo™ Platform Hardware Manual.*






Slave mode




Clock switching example by master mode round operation
(x,y=0, 1, 2, 3: x and y are different value)

### (8) Serial Chip Select Used (SCSCR:CSEN = 1)

■Serial clock output signal detect level "L" (SMR, SCSFR:SCINV = 1)

■Serial Chip select inactive level "L" (SCSCR, SCSFR:CSLVL = 0)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 % /3.3 V ± 0.3 V, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}$12 = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS ↑ → SCK ↑ setup time | $t_{CSSI}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCK16 to SCK17 SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x, SCS16x to SCS17x | Master mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $t_{CSSU}$*1-15 | - | ns | |
| SCK ↓ → SCS ↓ hold time | $t_{CSHI}$ | | | $t_{CSHD}$*2+0 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x | | $t_{CSDS}$*3-15 +5$t_{CLK_LCPnA}$*4 | - | ns | |
| | | SCS16x to SCS17x | | $t_{CSDS}$*3-15 +5$t_{CLK_COMP}$ | - | ns | |
| SCS ↑ → SCK ↑ setup time | $t_{CSSI}$ | SCK2_0, SCK3_0, SCS2x_0, SCS3x_0 | Master Mode (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $t_{CSSU}$*1-10 | - | ns | |
| SCK ↓ → SCS ↓ hold time | $t_{CSHI}$ | | | $t_{CSHD}$*2+0 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS2x_0, SCS3x_0 | | $t_{CSDS}$*3-10 +5$t_{CLK_LCPnA}$*4 | - | ns | |
| SCS ↑ → SCK ↑ setup time | $t_{CSSE}$ | SCK0 to SCK4, SCK8 to SCK12 SCS0x to SCS4x, SCS8x to SCS12x | Slave mode (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | 4$t_{CLK_LCPnA}$*4+ 15 | - | ns | |
| | | SCK16 to SCK17, SCS16x to SCS17x | | 4$t_{CLK_COMP}$+ 15 | - | ns | |
| SCK ↓ → SCS ↓ hold time | $t_{CSHE}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17, SCS0x to SCS4x, SCS8x to SCS12x, SCS16x to SCS17x | | 0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS0x to SCS4x, SCS8x to SCS12x | | 4$t_{CLK_LCPnA}$*4+ 15 | - | ns | |
| | | SCS16x to SCS17x | | 4$t_{CLK_COMP}$+1 5 | - | ns | |
| SCS ↑ → SOT delay time | $t_{DSE}$ | SCS0x to SCS4x, SCS8x to SCS12x, SCS16x to SCS17x, SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | - | 40 | ns | |
| SCS ↓ → SOT delay time | $t_{DEE}$ | | | 0 | - | ns | |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCK ↑ → SCS ↑ clock switching time | $t_{SCC}$ | SCK0, SCK1, SCK2_1, SCK3_1, SCK4, SCK8 to SCK12, SCS0x, SCS1x, SCS2x_1, SCS3x_1, SCS4, SCS8x to SCS12x | Master mode round operation (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | $4t_{CLK_LCPnA}$*4+ 0 | $4t_{CLK_LCPnA}$* 4 +15 | ns | |
| | | SCK16 to SCK17, SCS16x to SCS17x | | $4t_{CLK_COMP}$+0 | $4t_{CLK_COMP}$ +15 | ns | |
| | | SCK2_0, SCK3_0, SCS2x_0, SCS3x_0 | Master mode round operation (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA) | $4t_{CLK_LCPnA}$*4 +0 | $4t_{CLK_LCPnA}$* 4 +10 | ns | |

*1: $t_{CSSU}$ = SCSTR:CSSU[7:0] x serial chip select timing operating clock

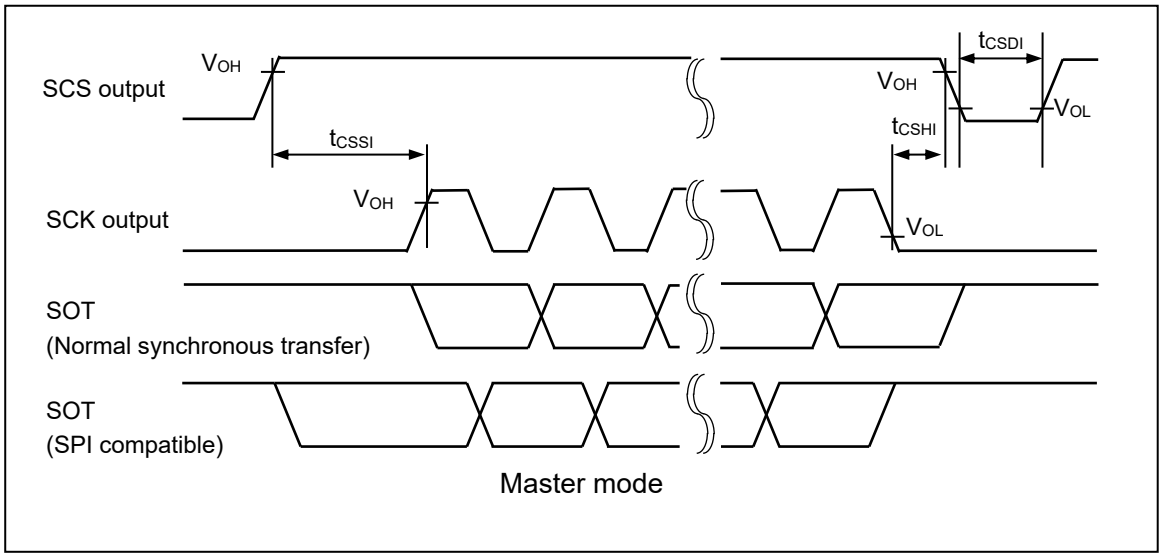
*2: $t_{CSHD}$ = SCSTR:CSHD[7:0] x serial chip select timing operating clock

*3: $t_{CSDS}$ = SCSTR:CSDS[15:0] x serial chip select timing operating clock
For details on *1, *2, and *3 above, see the Traveo™ Platform Hardware Manual.

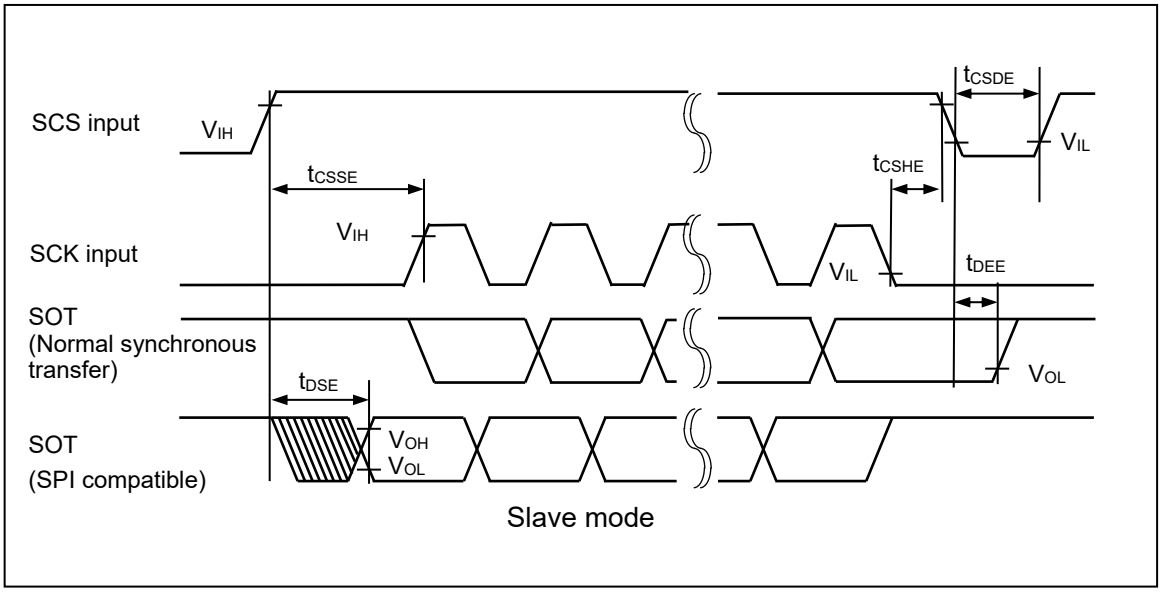
*4 $t_{CLK_LCPnA}$ n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

***Notes:***

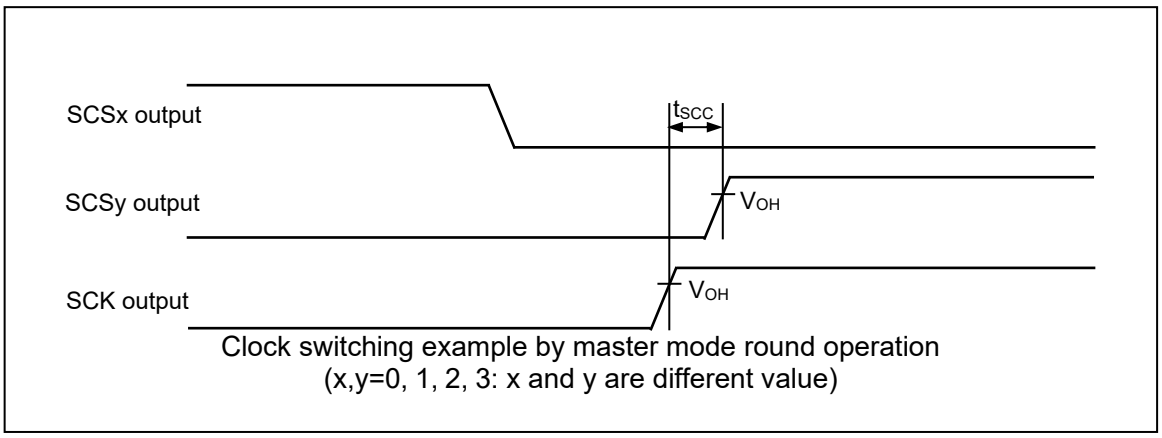
- *This is the AC characteristic in CLK synchronized mode.*
- *CL is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the Traveo™ Platform Hardware Manual.*




Master mode




Slave mode




Clock switching example by master mode round operation
(x,y=0, 1, 2, 3: x and y are different value)

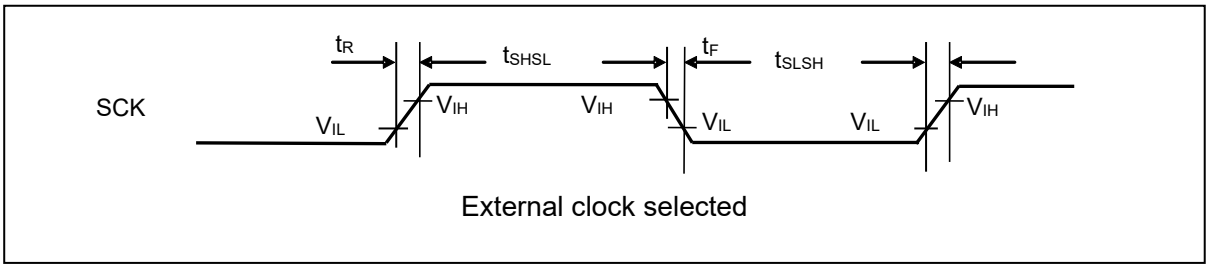
LIN interface (v2.1) (LIN communication control interface (v2.1)) timing (SMR:MD2-0 = 0b011)

### (1) External Clock Selected (BGR:EXT = 1)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 % /3.3 V ± 0.3 V, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}$12 = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK4, SCK8 to SCK12 | - | $t_{CLK_LCPnA}$*1+10 | - | ns | |
| | | SCK16 to SCK17 | | $t_{CLK_COMP}$ +10 | - | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK4, SCK8 to SCK12 | | $t_{CLK_LCPnA}$*1+10 | - | ns | |
| | | SCK16 to SCK17 | | $t_{CLK_COMP}$ +10 | - | ns | |
| SCK falling time | $t_F$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 | | - | 5 | ns | |
| SCK rising time | $t_R$ | | | - | 5 | ns | |

*1: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12




External clock selected

$I^2C$ timing (SMR:MD2-0 = 0b100)

($T_A$: Recommended operating conditions, Vcc5 = Vcc53 = 5.0 V ± 10 %, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Standard Mode | | Fast Mode | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | | |
| SCL clock frequency | $f_{SCL}$ | SCL0, SCL1, SCL4, SCL8 to SCL12, SCL16 to SCL17 | $C_L$ = 50 pF, R = (Vp/$I_{OL}$)*1 | 0 | 100 | 0 | 400 | kHz | |
| Repeat "start" condition hold time SDA↓ → SCL↓ | $t_{HDSTA}$ | SDA0, SDA1, SDA4 SDA8 to SDA12, SDA16 to SDA17, SCL0, SCL1, SCL4, SCL8 to SCL12, SCL16 to SCL17 | | 4.0 | - | 0.6 | - | µs | |
| Period of "L" for SCL clock | $t_{LOW}$ | SCL0, SCL1, SCL4, SCL8 to SCL12, SCL16 to SCL17 | | 4.7 | - | 1.3 | - | µs | |
| Period of "H" for SCL clock | $t_{HIGH}$ | | | 4.0 | - | 0.6 | - | µs | |
| Repeat "start" condition setup time SCL↑ → SDA↓ | $t_{SUSTA}$ | SDA0, SDA1, SDA4 SDA8 to SDA12, SDA16 to SDA17, SCL0, SCL1, SCL4, SCL8 to SCL12, SCL16 to SCL17 | | 4.7 | - | 0.6 | - | µs | |
| Data hold time SCL↓ → SDA↓↑ | $t_{HDDAT}$ | | | 0 | 3.45*2 | 0 | 0.9*3 | µs | |
| Data setup time SDA↓↑ → SCL↑ | $t_{SUDAT}$ | | | 250 | - | 100 | - | ns | |
| "Stop" condition setup time SCL↑ → SDA↑ | $t_{SUSTO}$ | | | 4.0 | - | 0.6 | - | µs | |
| Bus-free time between "stop" condition and "start" condition | $t_{BUF}$ | - | | 4.7 | - | 1.3 | - | µs | |
| Noise filter | $t_{SP}$ | - | | $t_{NFT}$*4 | - | $t_{NFT}$*4 | - | ns | |

Notes: Only ch.16 and ch.17 are standard mode/high-speed mode correspondence. In ch.0, ch.1, ch.4, and ch.8 to ch.12, only a standard mode is correspondence.

*1: R and $C_L$ represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.
Vp shows that the power-supply voltage of the pull-up resistor and $I_{OL}$ shows the $V_{OL}$ guarantee current.

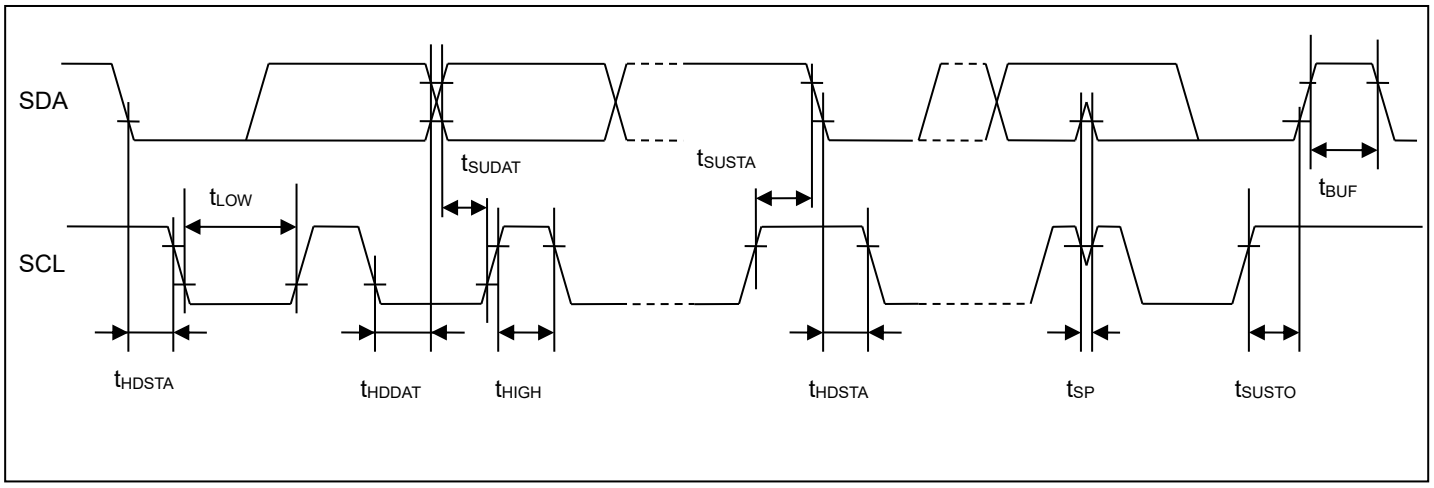
*2: The maximum $t_{HDDAT}$ only has to be met if the device does not extend the "L" width ($t_{LOW}$) of the SCL signal.

*3: A fast mode $I^2C$ bus device can be used on a standard mode $I^2C$ bus system as long as the device satisfies the requirement of "$t_{SUDAT}$ ≥ 250 ns".

*4: $t_{NFT}$ = (NFCR:NFT[4:0]+1) x 2 x $t_{CLK_LCP0A}$ (ch.0, ch.1, ch4)

$t_{NFT}$ = (NFCR:NFT[4:0]+1) x 2 x $t_{CLK_LCP1A}$ (ch.8 to ch.12)

$t_{NFT}$ = (NFCR:NFT[4:0]+1) x 2 x $t_{CLK_COMP}$ (ch.16 to ch.17)


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

### 9.1.4.7 Timer Input

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 %, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}12$ = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TWH}$, $t_{TWL}$ | PPG0_TIN1 to PPG31_TIN1 | - | $4t_{CLK_LCPnA}$*1 | - | ns | $4t_{CLK_LCPnA}$*1 ≥100 ns |
| | | | | 100 | | | $4t_{CLK_LCPnA}$*1 <100 ns |
| | | ICU0_IN0 to ICU2_IN0, ICU8_IN0 to ICU10_IN0, ICU0_IN1 to ICU2_IN1, ICU8_IN1 to ICU10_IN1 | - | $4t_{CLK_LCPnA}$*2 | - | ns | $4t_{CLK_LCPnA}$*2 ≥100 ns |
| | | | | 100 | | | $4t_{CLK_LCPnA}$*2 <100 ns |
| | | FRT0_TEXT to FRT4_TEXT, FRT8_TEXT to FRT10_TEXT | - | $4t_{CLK_LCPnA}$*3 | - | ns | $4t_{CLK_LCPnA}$*3 ≥100 ns |
| | | | | 100 | | | $4t_{CLK_LCPnA}$*3 <100 ns |
| | | TIN0 to TIN1, TIN16 to TIN17 | - | $4t_{CLK_LCPnA}$*4 | - | ns | $4t_{CLK_LCPnA}$*4 ≥100 ns |
| | | | | 100 | | | $4t_{CLK_LCPnA}$*4 <100 ns |
| | | TIN48 to TIN49 | - | $4t_{CLK_COMP}$ | - | ns | $4t_{CLK_COMP}$ ≥100 ns |
| | | | | 100 | | | $4t_{CLK_COMP}$ <100 ns |

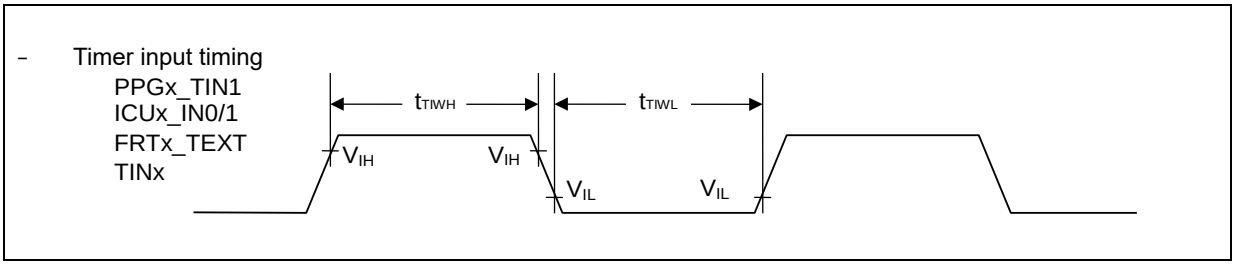
*1: n = 0: unit.0 to unit.5, unit.12 to unit.31, n = 1:unit.6 to unit.11

*2: n = 0:unit.0 to unit.2, n = 1:unit.8 to unit.10

*3: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.10

*4: n = 0:ch.0 to ch.1, n = 1:ch.16 to ch.17

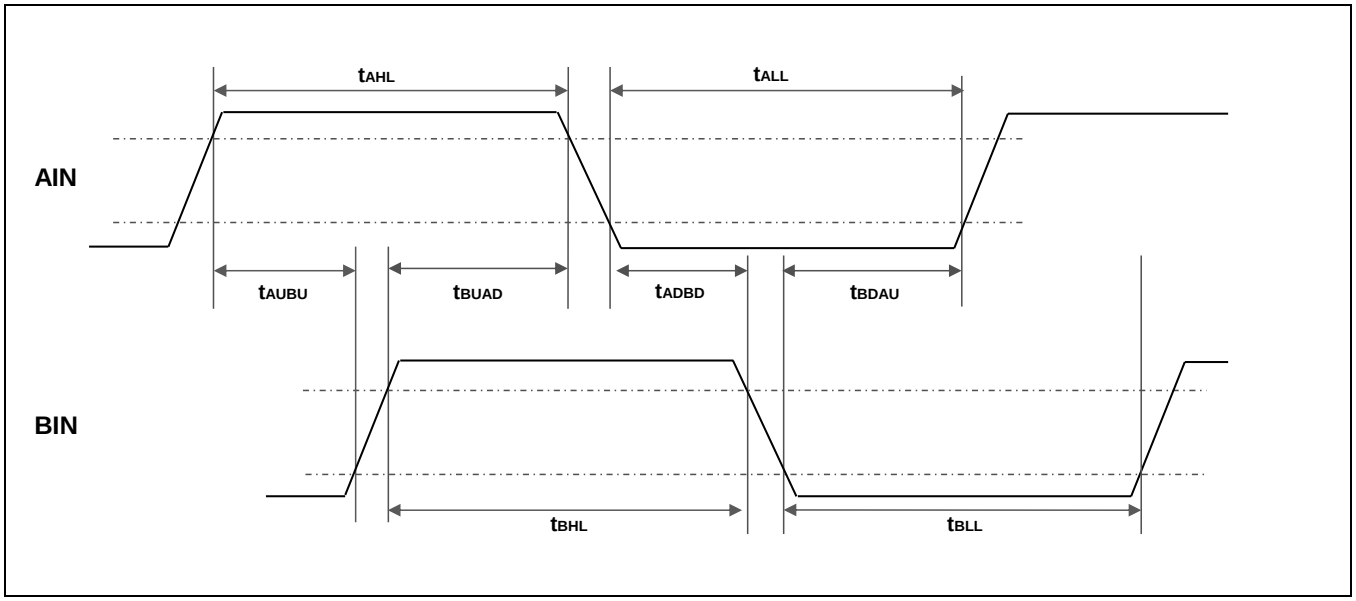
- Timer input timing

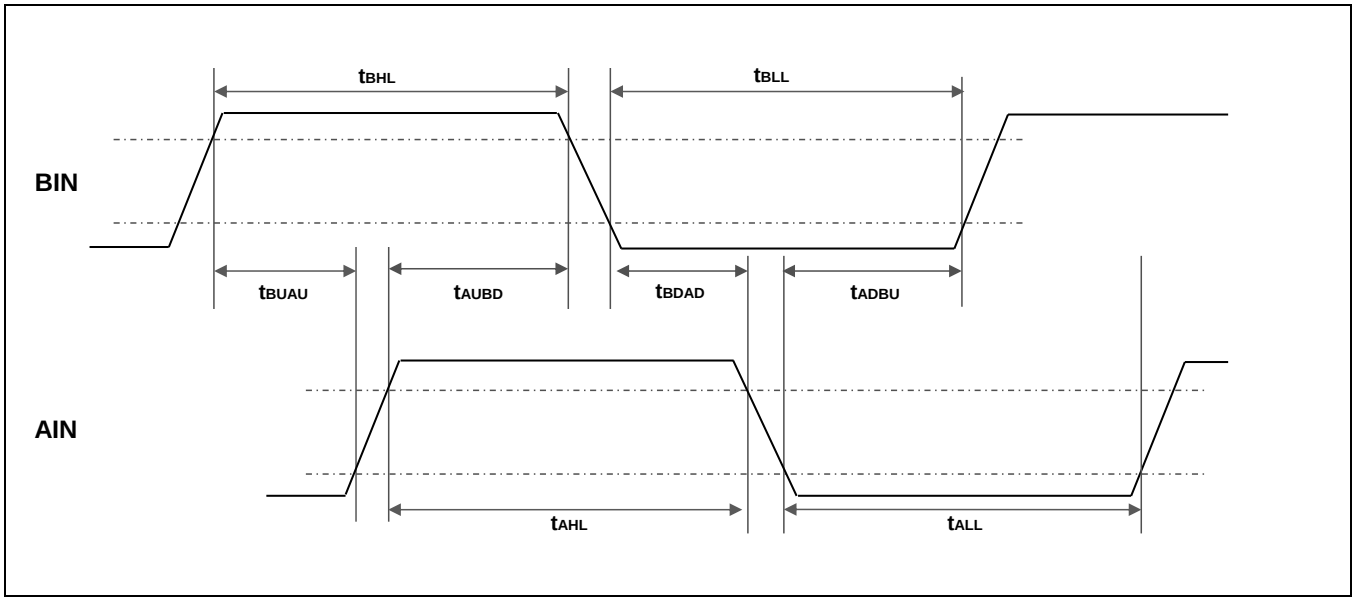


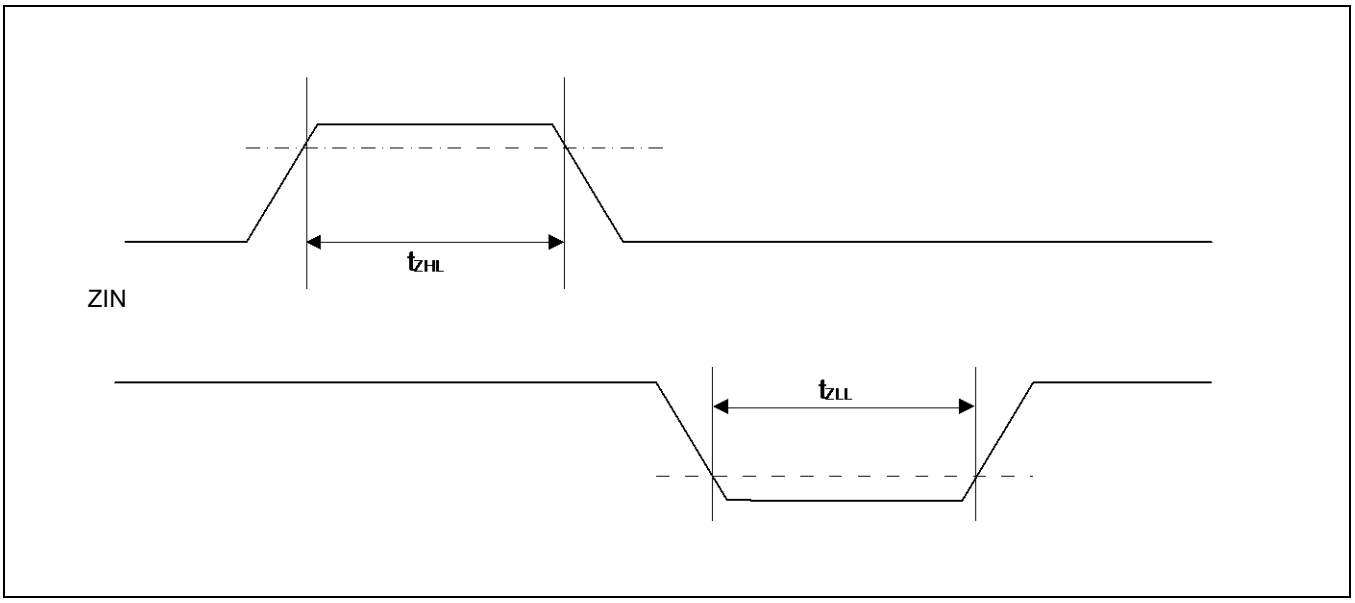
### 9.1.4.8 QPRC timing

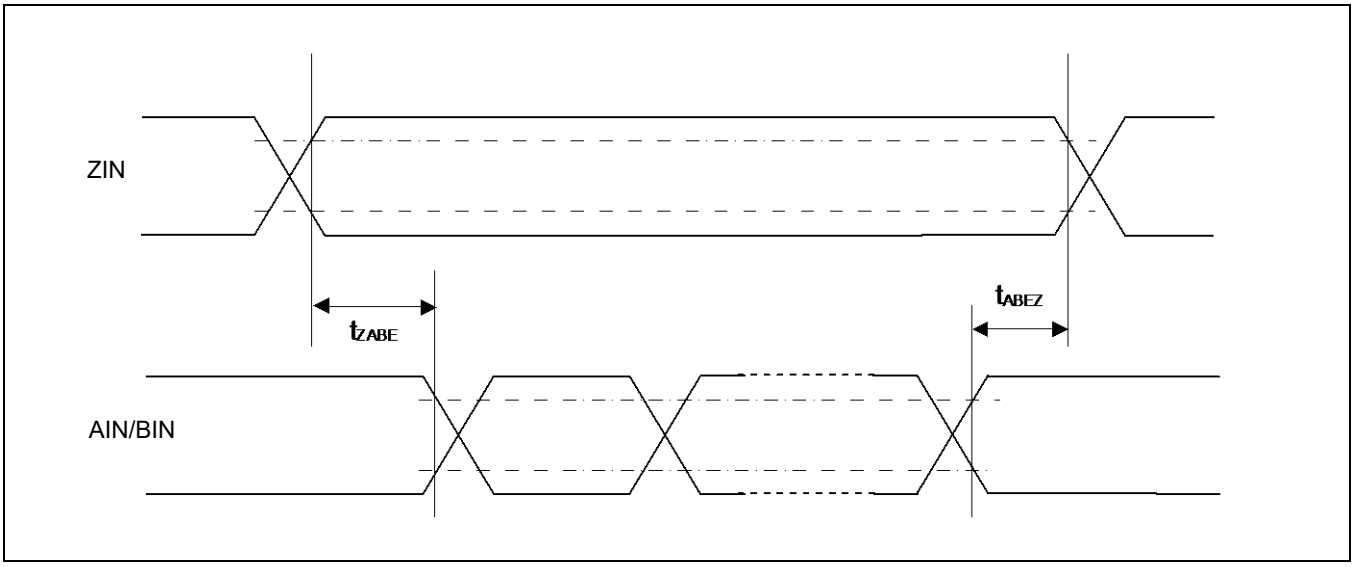
($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 %, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}$12 = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| AIN pin "H" width | $t_{AHL}$ | AIN8 to AIN9 | - | $4t_{CLK_LCP1A}$ | - | ns | $4t_{CLK_LCP1A} \geq 100$ ns |
| AIN pin "L" width | $t_{ALL}$ | AIN8 to AIN9 | - | | | | |
| BIN pin "H" width | $t_{BHL}$ | BIN8 to BIN9 | - | | | | |
| BIN pin "L" width | $t_{BLL}$ | BIN8 to BIN9 | - | | | | |
| Time from AIN pin "H" level to BIN rise | $t_{AUBU}$ | AIN8 to AIN9, BIN8 to BIN9 | PC_Mode2 or PC_Mode3 | | | | |
| Time from BIN pin "H" level to AIN fall | $t_{BUAD}$ | AIN8 to AIN9, BIN8 to BIN9 | PC_Mode2 or PC_Mode3 | | | | |
| Time from AIN pin "L" level to BIN fall | $t_{ADBD}$ | AIN8 to AIN9, BIN8 to BIN9 | PC_Mode2 or PC_Mode3 | | | | |
| Time from BIN pin "L" level to AIN rise | $t_{BDAU}$ | AIN8 to AIN9, BIN8 to BIN9 | PC_Mode2 or PC_Mode3 | | | | |
| Time from BIN pin "H" level to AIN rise | $t_{BUAU}$ | AIN8 to AIN9, BIN8 to BIN9 | PC_Mode2 or PC_Mode3 | | | | |
| Time from AIN pin "H" level to BIN fall | $t_{AUBD}$ | AIN8 to AIN9, BIN8 to BIN9 | PC_Mode2 or PC_Mode3 | | | | |
| Time from BIN pin "L" level to AIN fall | $t_{BDAD}$ | AIN8 to AIN9, BIN8 to BIN9 | PC_Mode2 or PC_Mode3 | | | | |
| Time from AIN pin "L" level to BIN rise | $t_{ADBU}$ | AIN8 to AIN9, BIN8 to BIN9 | PC_Mode2 or PC_Mode3 | | | | |
| ZIN pin "H" width | $t_{ZHL}$ | ZIN8 to ZIN9 | QCR:CGSC = "0" | | | | |
| ZIN pin "L" width | $t_{ZLL}$ | ZIN8 to ZIN9 | QCR:CGSC = "0" | | | | |
| Time from determined ZIN level to AIN/BIN rise and fall | $t_{ZABE}$ | AIN8 to AIN9, BIN8 to BIN9, ZIN8 to ZIN9 | QCR:CGSC = "1" | | | | |
| Time from AIN/BIN rise and fall time to determined ZIN level | $t_{ABEZ}$ | AIN8 to AIN9, BIN8 to BIN9, ZIN8 to ZIN9 | QCR:CGSC = "1" | | | | |


AIN
BIN
tAHL
tALL
tAUBU
tBUAD
tADBD
tBDAU
tBHL
tBLL


BIN
AIN
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tAHL
tALL


ZIN
tZHL
tZLL

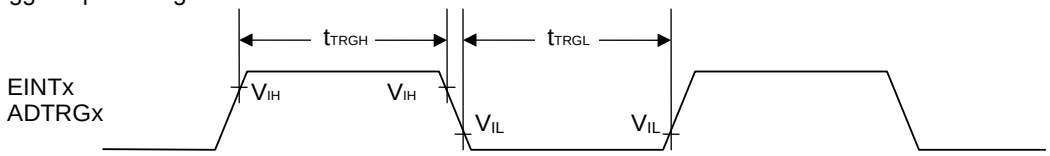

ZIN
tZABE
tABEZ
AIN/BIN

### 9.1.4.9 *Trigger Input*

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, Vcc5 = DVcc = 5.0 V ± 10 %, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = 0.0 V, $V_{CC}$12 = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$, $t_{TRGL}$ | EINT0 to EINT23 | - | 100 | - | ns | |
| | | ADTRG0 to ADTRG1 | - | $5t_{CLK_LCP1A}$ | - | ns | $5t_{CLK_LCP1A}$ ≥100 ns |
| | | | | 100 | | | $5t_{CLK_LCP1A}$ <100 ns |
| | | EINT0 to EINT23 | - | 1 | - | µs | Stop mode |

- Trigger input timing

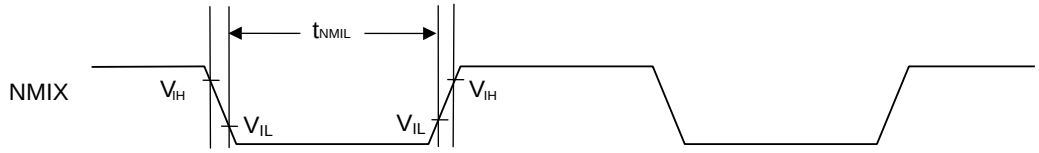


*9.1.4.10 NMI Input*

($T_A$: Recommended operating conditions, Vcc5 = 5.0 V ± 10 %, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{NMIL}$ | NMIX | - | 300 | - | ns | |

- NMIX input timing



*9.1.4.11 Low Voltage Detection (External Voltage)*

Low-voltage detection (external low-voltage detection)

($T_A$: Recommended operating conditions, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply voltage range | $V_{DP5}$ | VCC5 | - | 3.5 *3 | - | 5.5 *3 | V | |
| | | | | 2.7 *4 | - | 3.6 *4 | | |
| | $V_{DP3}$ | VCC3 | - | 2.7 | - | 3.6 | V | |
| Detection voltage (before trimming) | $V_{DLBT}$ | VCC5 | *1 | 3.6 *3 | 4.0 *3 | 4.4 *3 | V | When power-supply voltage falls and detection level is set initially |
| | | | *1 *5 | 2.3 *4 | 2.6 *4 | 2.9 *4 | | |
| | | VCC3 | *1 *5 | 2.3 | 2. 6 | 2.9 | V | |
| Detection voltage (after trimming) | $V_{DLAT}$ | VCC5 | *1 | 3.86 *3 | 4.0 *3 | 4.14 *3 | V | When power-supply voltage falls and detection level is set initially Typ ±3.5 % |
| | | | *1 *5 | 2.51 *4 | 2.6 *4 | 2.69 *4 | | |
| | | VCC3 | *1 *5 | 2.51 | 2.6 | 2.69 | V | |
| Hysteresis width | $V_{HYS}$ | VCC5 | - | - | 100 | - | mV | When power-supply voltage rises |
| Low-voltage detection time | Td | - | - | - | - | 40 | µs | |
| Power supply voltage regulation | - | VCC5 | - | -2 | - | 2 | V/ms | *2 |

*1: If the fluctuation of the power supply is faster than the low-voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage (VDL)

*3: For S6J33xxxSx or S6J33xxxUx or S6J33xxxTx or S6J33xxxVx option.

*4: For S6J33xxxAx or S6J33xxxBx or S6J33xxxCx or S6J33xxxDx or S6J33xxxEx or S6J33xxxFx or S6J33xxxGx or S6J33xxxHx option.

*5: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (2.7 V).

***Notes:***

- *The detection/release threshold values of following LVD channels are potentially below supply range defined in 9.1.2 Recommended Operating Condition.*
  *LVDH1 (VCC5)*
  *LVDH2 (VCC3)*
- *Please use these LVD channels with your own risk.*
- *Please monitor the external power supplies on the PCB if needed.*
- *For S6J33xxxSC or S6J33xxxUC or S6J33xxxTC or S6J33xxxVC options:*
  *Depending on the threshold setting, LVDH1 can always detect VCC5 low voltage before the supply drops below the level defined in 9.1.2 Recommended Operating Condition. Please refer to S6J3300 series Hardware Manual for available list of LVDH1 threshold settings.*

Low-voltage detection (1.15 V power supply low-voltage detection)

($T_A$: Recommended operating conditions, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply voltage range | $V_{RDP12}$ | VCC12 | - | 1.09 | - | 1.21 | V | |
| Detection voltage (before trimming)* | $V_{RDLBT}$ | VCC12 | *1 *2 | 0.7125 | 0.8125 | 0.9125 | V | When power-supply voltage falls |
| Detection voltage (after trimming) | $V_{RDLAT}$ | VCC12 | *1 *2 | 0.7841 | 0.8125 | 0.8410 | V | When power-supply voltage falls Typ ±3.5 % |
| Hysteresis width | $V_{RHYS}$ | - | - | - | 75 | - | mV | When power-supply voltage rises |
| Low-voltage detection time | TRd | - | - | - | - | 30 | µs | |

*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be canceled after the supply voltage has passed the detection voltage range.

*2: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (1.09 V).

***Notes:***

- *The detection/release threshold values of LVDL2 channel is potentially below supply range defined in 9.1.2 Recommended Operating Condition.*
- *Please use this LVDL2 channel with your own risk.*
- *Please monitor the external power supplies on the PCB if needed.*

### 9.1.4.12 Low Voltage Detection (Internal Voltage)

Low-voltage detection (internal low-voltage detection for LVDL0)

($T_A$: Recommended operating conditions, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply voltage range | $V_{RDP5}$ | - | - | 1.05 | - | 1.21 | V | |
| Detection voltage | $V_{RDL}$ | - | *1 *2 | 0.75 | 0.85 | 0.95 | V | When power-supply voltage falls |
| Hysteresis width | $V_{RHYS}$ | - | - | - | 75 | - | mV | When power-supply voltage rises |
| Low-voltage detection time | TRd | - | - | - | - | 30 | µs | *3 |

*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be canceled after the supply voltage has passed the detection voltage range.

*2: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (1.05 V).

*3: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.

***Notes:***

− *The detection/release threshold values of LVDL0 channel is potentially below supply range defined in 9.1.2 Recommended Operating Condition.*

Low-voltage detection (internal low-voltage detection for LVDL1)

($T_A$: Recommended operating conditions, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply voltage range | $V_{RDP5}$ | - | - | 1.05 | - | 1.21 | V | |
| Detection voltage (before trimming) | $V_{RDLBT}$ | - | *1 *2 | 0.775 | 0.875 | 0.975 | V | When power-supply voltage falls |
| Detection voltage (after trimming) | $V_{RDLAT}$ | - | *1 *2 | 0.844 | 0.875 | 0.906 | V | When power-supply voltage falls Typ ±3.5 % |
| Hysteresis width | $V_{RHYS}$ | - | - | - | 75 | - | mV | When power-supply voltage rises |
| Low-voltage detection time | TRd | - | - | - | - | 30 | µs | *3 |

*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be canceled after the supply voltage has passed the detection voltage range.

*2: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (1.05 V).

*3: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.

***Notes:***

− *The detection/release threshold values of LVDL1 channel is potentially below supply range defined in 9.1.2 Recommended Operating Condition.*

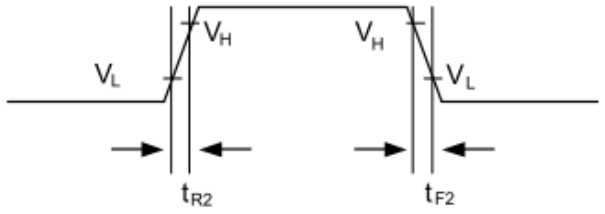
*9.1.4.13 High Current Output Slew Rate*

($T_A$: Recommended operating conditions,

$V_{CC}5$,$V_{CC}53$,$DV_{CC}$ = 5.0 V ± 10 %, $V_{CC}3$ = 3.3 V ± 0.3 V, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Output rise / fall time | $t_{R2}$,$t_{F2}$ | P1_17 to P1_31, P2_00 to P2_08 | - | 15 | - | 100 | ns | Load capacitance 85 pF |

• Slew rate output timing




$V_H$=$V_{OL8}$+0.9 x ($V_{OH8}$-$V_{OL8}$)
$V_L$=$V_{OL8}$+0.1 x ($V_{OH8}$-$V_{OL8}$)

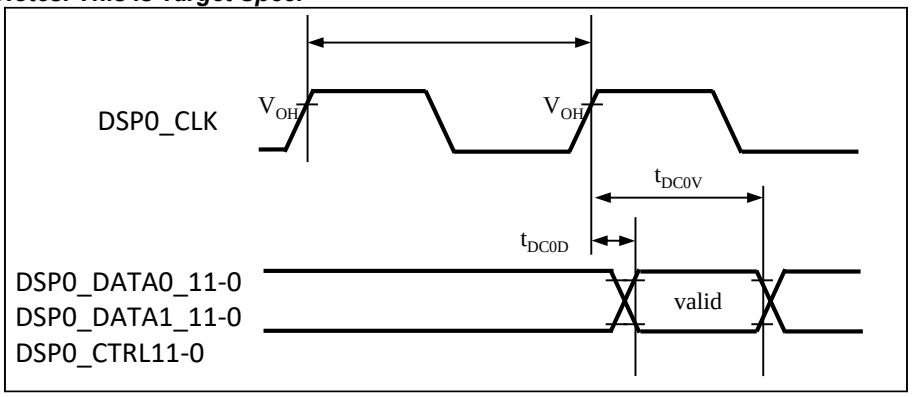
*9.1.4.14 Display Controller*

### (1) Display Controller0 Timing (TTL Mode)

($T_A$: Recommended operating conditions, Vcc53 = 5.0 V ± 10 %, 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Clock Cycle | $t_{DC0CYC}$ | DSP0_CLK | (CL = 20 pF, $I_{OL}$ = -15 mA, $I_{OH}$ = 15 mA), | 25 | - | ns | |
| Output delay from DSP0_CLK↑ | $\|t_{DC0D}\|$ | DSP0_R7-0<br>DSP0_G7-0<br>DSP0_B7-0<br>DSP0_EN<br>DSP0_HSYNC<br>DSP0_VSYNC | (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA) | - | 3.2 | ns | |
| Output data valid time | $t_{DC0V}$ | DSP0_R7-0<br>DSP0_G7-0<br>DSP0_B7-0<br>DSP0_EN<br>DSP0_HSYNC<br>DSP0_VSYNC | | 21.8 | - | ns | $t_{DC0CYC}$ - 3.3 ns+0.1 ns |

***Notes: This is Target Spec.***



*9.1.4.15 External Bus Interface Timing*

Clock Output Timing

($T_A$: Recommended operating conditions, Vcc53 = 5.0 V ± 10 %, $V_{SS}$ = 0.0 V)

(External load capacitance 16 pF)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | MCLK | 2 mA is selected in ODR bit in PPC_PCFGR register. | 62.5 | - | ns | |
| Clock high width *1 | $t_{CHCL}$ | MCLK | | $d_Ht_{cyc}$ - 7 | $d_Ht_{cyc}$ + 7 | ns | |
| Clock low width *2 | $t_{CLCH}$ | MCLK | | $d_Lt_{cyc}$ - 7 | $d_Lt_{cyc}$ + 7 | ns | |

*1: If division-ratio is even value, dH is equivalent to 0.5.

Otherwise, dH is calculated as the following.

dH = The number rounding "division-ratio x 0.5" down to the nearest integer / division-ratio

division-ratio is multiplication value among SYSDIV bit, HPMDIV bit and EXTBUSDIV bit setting.

ex). Setting SYSDIV to 1-division, HPMDIV to 7-division, EXTBUSDIV to 1-division, dH is calculated as 0.429.

*2: If division-ratio is even value, dL is equivalent to 0.5.

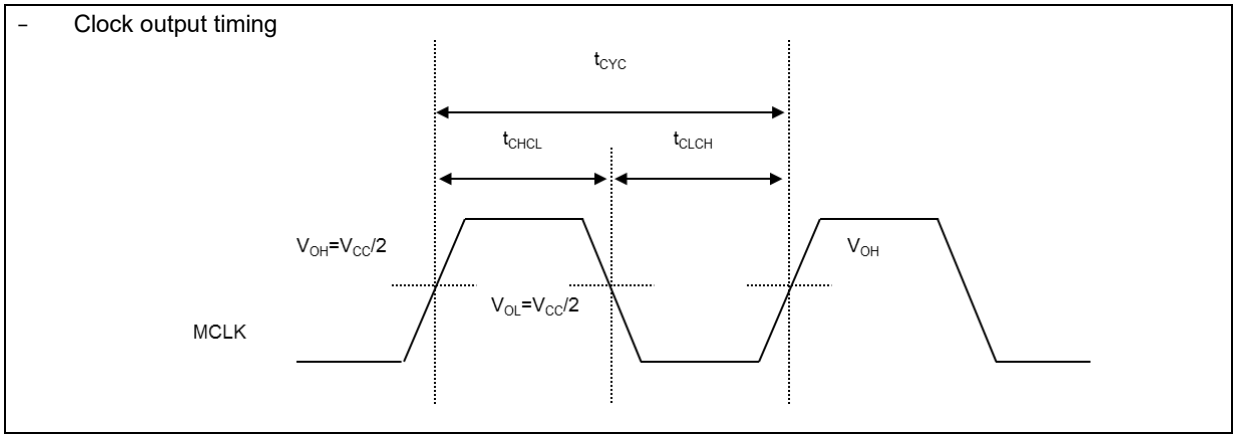
Otherwise, dL is calculated as the following.

dL = The number rounding "division-ratio x 0.5" up to the nearest integer / division-ratio

division-ratio is multiplication value among SYSDIV bit, HPMDIV bit and EXTBUSDIV bit setting.

ex). Setting SYSDIV to 1-division, HPMDIV to 7-division, EXTBUSDIV to 1-division, dL is calculated as 0.571.

- Clock output timing



Common Timing between Read and Write

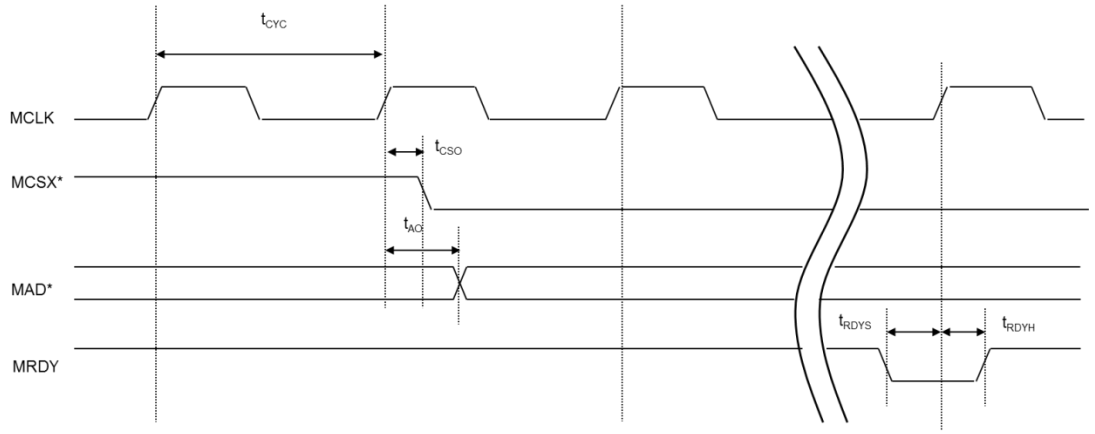
($T_A$: Recommended operating conditions, Vcc53 = 5.0 V ± 10 %, $V_{SS}$ = 0.0 V)

(External load capacitance 16 pF)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Cycle time (without MRDY) | $t_{CYC}$ | MCLK | 2 mA is selected in ODR bit in PPC_PCFGR register. | 62.5 | - | ns | |
| Cycle time (with MRDY) | $t_{CYC}$ | MCLK | | 62.5 | - | ns | If using MRDY, set MCLK to 20 MHz or less. |
| CS delay time | $t_{CSO}$ | MCLK, MCSX0 to MCSX3 | | 0.5 | 18 | ns | |
| Address delay time | $t_{AO}$ | MCLK, MAD00 to MAD23 | | 0.5 | 18 | ns | |
| RDY setup time | $t_{RDYS}$ | MCLK, MRDY | "CMOS Schmitt input" and "Disable noise filter" are selected in PPC_PCFGR register. | 21 | - | ns | |
| RDY hold time | $t_{RDYH}$ | MCLK, MRDY | | 0 | - | ns | |

***Notes: This is Target Spec.***

- External bus I/F common timing



Read Timing

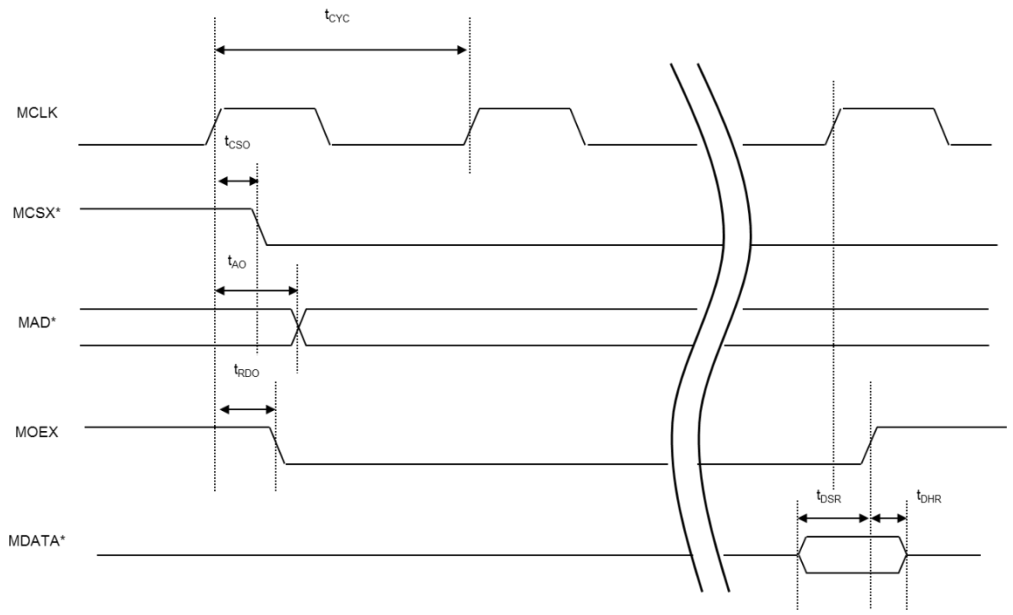
($T_A$: Recommended operating conditions, Vcc53 = 5.0 V ± 10 %, $V_{SS}$ = 0.0 V)

(External load capacitance 16 pF)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Data setup time | $t_{DSR}$ | MOEX, MDATA00 to MDATA15 | "CMOS Schmitt input" and "Disable noise filter" are selected in PPC_PCFGR register. | $21+t_{cyc}$ | - | ns | |
| Data hold time | $t_{DHR}$ | MOEX, MDATA00 to MDATA15 | | 0 | - | ns | |
| MOEX delay time | $t_{RDO}$ | MCLK, MOEX | 2 mA is selected in ODR bit in PPC_PCFGR register. | 0.5 | 18 | ns | |

***Notes: This is Target Spec.***

- External bus I/F read timing



Write Timing

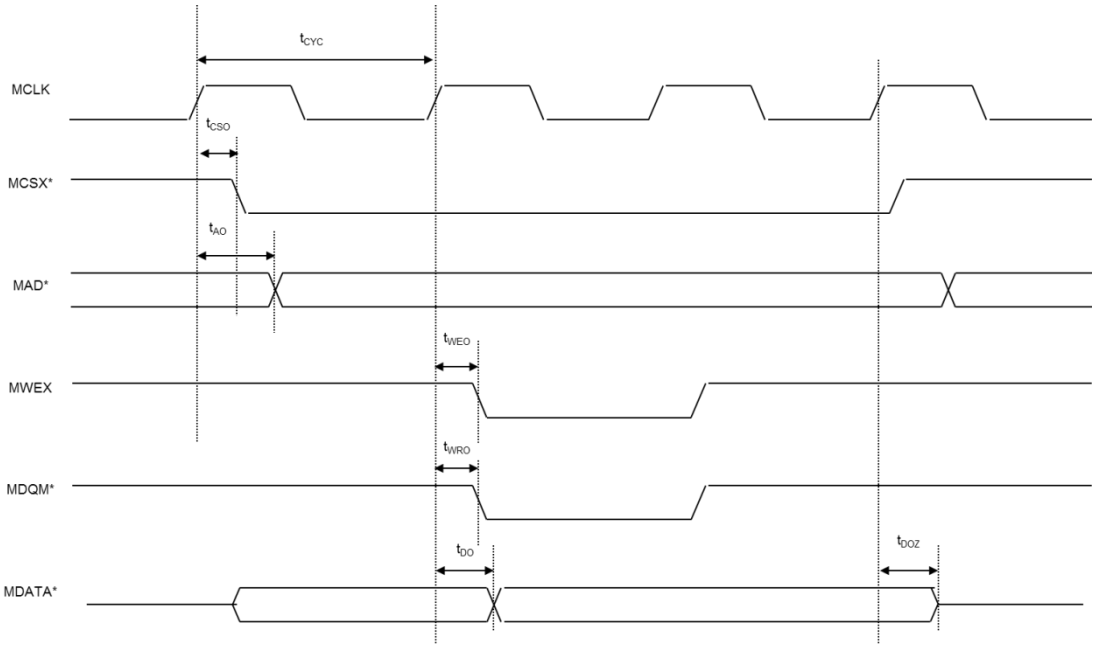
($T_A$: Recommended operating conditions, Vcc53 = 5.0 V ± 10 %, $V_{SS}$ = 0.0 V)

(External load capacitance 16 pF)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MWEX delay time | $t_{WEO}$ | MCLK, MWEX | 2 mA is selected in ODR bit in PPC_PCFGR register. | 0.5 | 18 | ns | |
| Byte mask delay time | $t_{WRO}$ | MCLK, MDQM0 to MDQM1 | | 0.5 | 18 | ns | |
| Data delay time | $t_{DO}$ | MCLK, MDATA00 to MDATA15 | | 0.5 | 18 | ns | |
| Data delay time (Hi-Z output) | $t_{DOZ}$ | MCLK, MDATA00 to MDATA15 | | - | 18 | ns | |

***Notes: This is Target Spec.***

- External bus I/F write timing



*9.1.4.16 DDR-HSSPI*

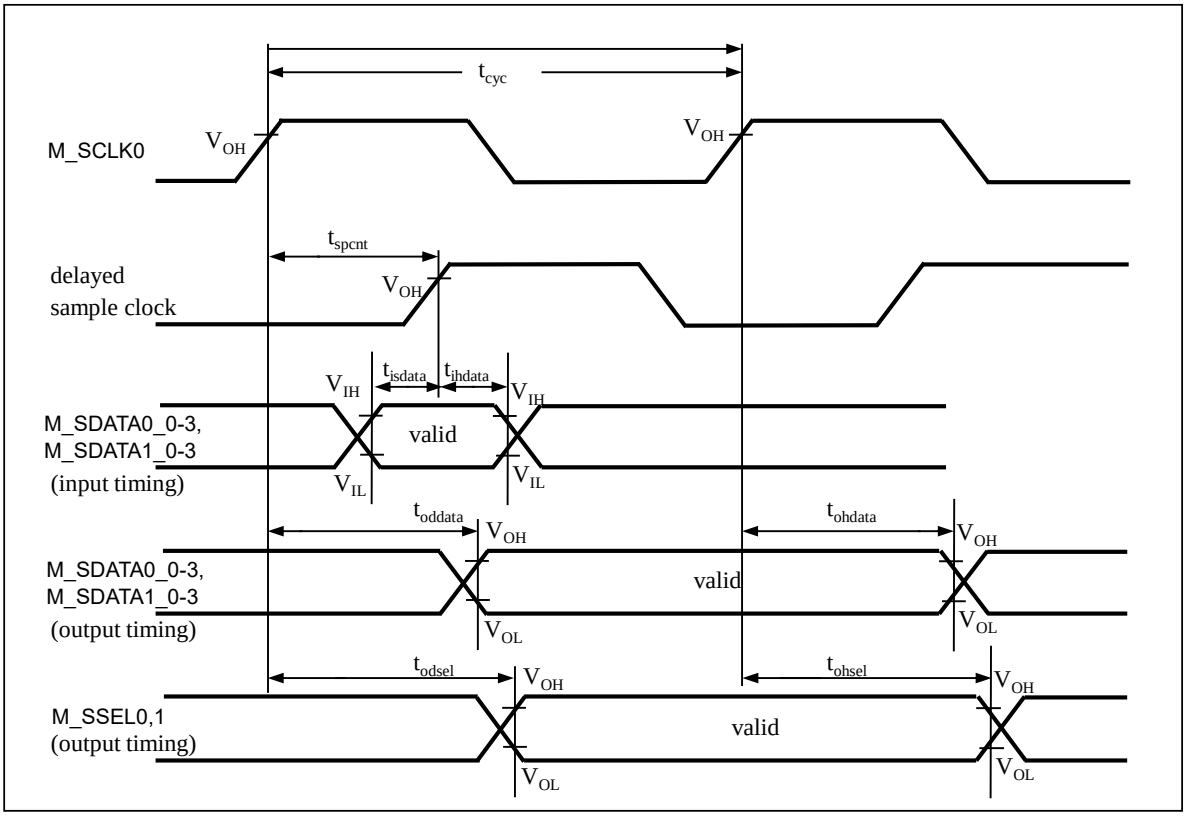
**(1) DDR-HSSPI Interface Timing (SDR Mode)**

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| HSSPI clock cycle | $t_{cyc}$ | M_SCLK0 | (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA), | 10 | - | ns | |
| | | | | 20 | - | | when Quad Page Program |
| M_SCLK↑ -> delayed sample clock↑ | $t_{spcnt}$ | - | | 0 | 31.5 | ns | |
| M_SDATA -> M_SLCK↑ Input setup time | $t_{isdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | *1 | - | ns | |
| M_SLCK↑ -> M_SDATA Input hold time | $t_{ihdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | *1 | - | ns | |
| M_SCLK↑ -> M_SDATA Output delay time | $t_{oddata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | - | $t_{cyc}$/2 + 2 | ns | |
| M_SCLK↑ -> M_SDATA Output hold time | $t_{ohdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | $t_{cyc}$/2 - 3 | - | ns | |
| M_SCLK↑ -> M_SSEL Output delay time | $t_{odsel}$ | M_SSEL0, 1 | | -12.00+(SS2CD+0.5)* $t_{cyc}$ | - | ns | |
| M_SCLK↑ -> M_SSEL Output hold time | $t_{ohsel}$ | M_SSEL0, 1 | | $t_{cyc}$ - 2 | - | ns | |

***Notes: This is Target Spec.***

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured (DLP function).*



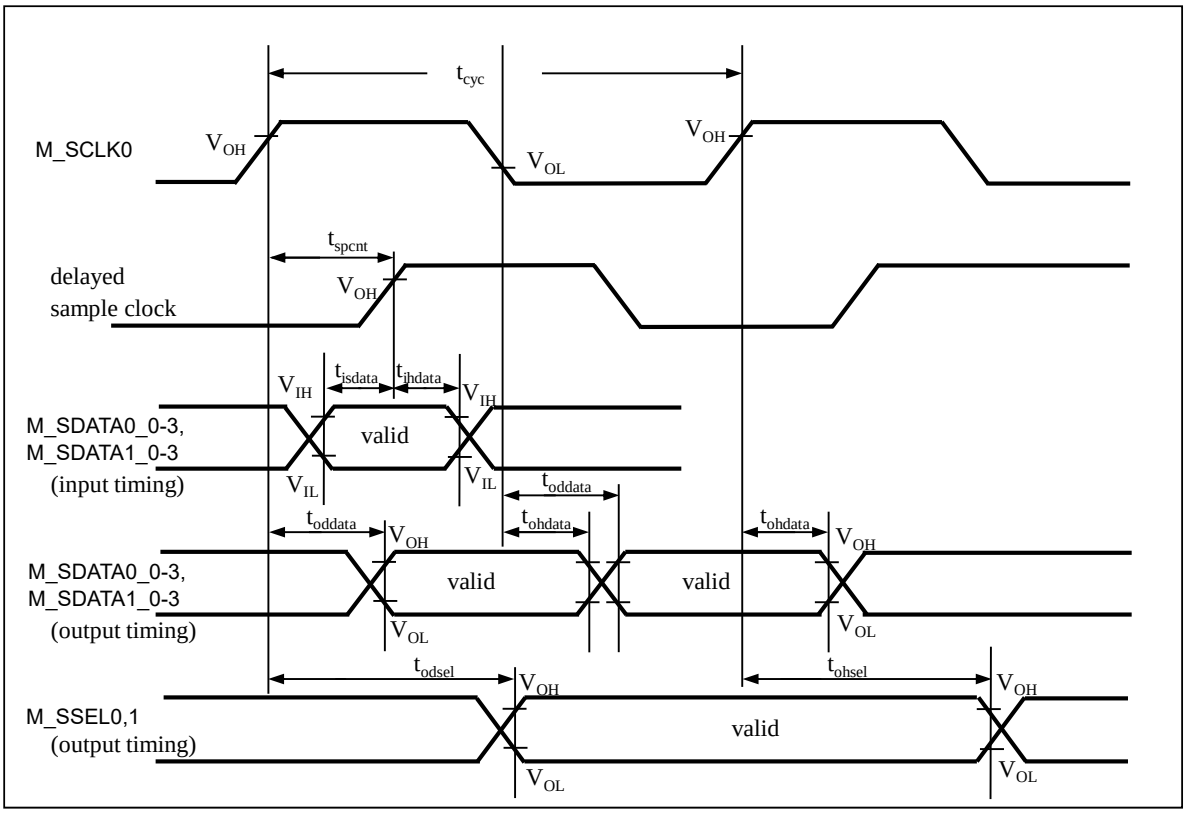

### (2) DDR-HSSPI Interface Timing (DDR Mode)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| HSSPI clock cycle | $t_{cyc}$ | M_SCLK0 | (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA), | 12.5 | - | ns | |
| M_SCLK↑ -> delayed sample clock↑ | $t_{spcnt}$ | | | 0 | 31.5 | ns | |
| M_SDATA -> M_SLCK↑ Input setup time | $t_{isdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | *1 | - | ns | |
| M_SLCK↑ -> M_SDATA Input hold time | $t_{ihdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | *1 | - | ns | |
| M_SCLK↑ -> M_SDATA Output delay time | $t_{oddata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | - | tcyc/4 + 1.5 | ns | |
| M_SCLK↑ -> M_SDATA Output hold time | $t_{ohdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | Tcyc/4 - 1.0 | - | ns | |
| M_SCLK↑ -> M_SSEL Output delay time | $t_{odsel}$ | M_SSEL0, 1 | | - 15.75+(SS2CD+0.5)*tcyc | - | ns | |
| M_SCLK↑ -> M_SSEL Output hold time | $t_{ohsel}$ | M_SSEL0, 1 | | 0.75*tcyc - 2.0 | - | ns | |

***Notes: This is Target Spec.***

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured (DLP function)*



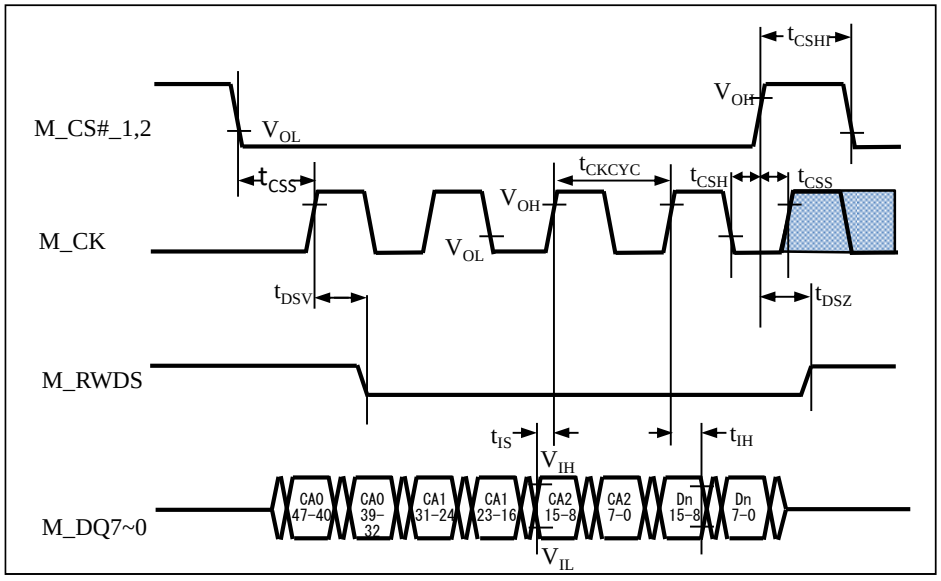
*9.1.4.17 Hyper BUS*

### (1) Hyper Bus Write Timing (HyperFlash)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Hyper Bus clock cycle | $t_{CKCYC}$ | M_CK | (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA), | 10.0 | - | ns | |
| CS↑↓ -> CK↑ Chip Select setup time | $t_{CSS}$ | M_CS#_1,2 | | $t_{CKCYC}$ -2.0 | - | ns | |
| DQ -> CK↑↓ Input setup time | $t_{IS}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↑↓ -> DQ Input hold time | $t_{IH}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↓ -> CS↑ Chip select hold time | $t_{CSH}$ | M_CS#_1,2 | | $t_{CKCYC}$/2 | - | ns | |

***Notes: This is Target Spec***

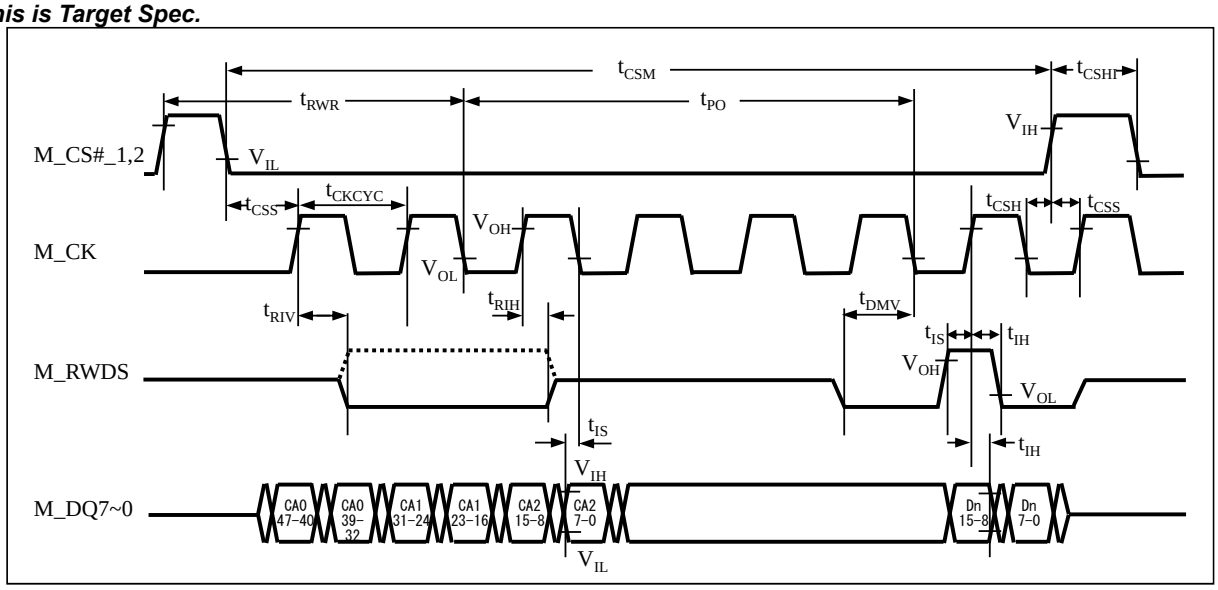


### (2) Hyper Bus Write Timing (HyperRAM)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Hyper Bus clock cycle | $t_{CKCYC}$ | M_CK | (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA), | 10.0 | - | ns | |
| CS↑↓ -> CK↑ Chip Select setup time | $t_{CSS}$ | M_CS#_1,2 | | $t_{CKCYC}$ - 2.0 | - | ns | |
| DQ -> CK↑↓ Input setup time | $t_{IS}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↑↓ -> DQ Input hold time | $t_{IH}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↓ -> CS↑ Chip select hold time | $t_{CSH}$ | M_CS#_1,2 | | $t_{CKCYC}$/2 | - | ns | |
| RWDS↓-> CK↓ Data Mask Valid | $t_{DMV}$ | M_RWDS | | 1 | - | ns | |
| CK↑ -> RWDS↑↓ Refresh Indicator Valid | $t_{RIV}$ | M_RWDS | | - | 6 | ns | |
| CK↑ -> RWDS (Hi-z) Refresh Indicator Hold | $t_{RIH}$ | M_RWDS | | 0 | - | ns | |

***Notes: This is Target Spec.***

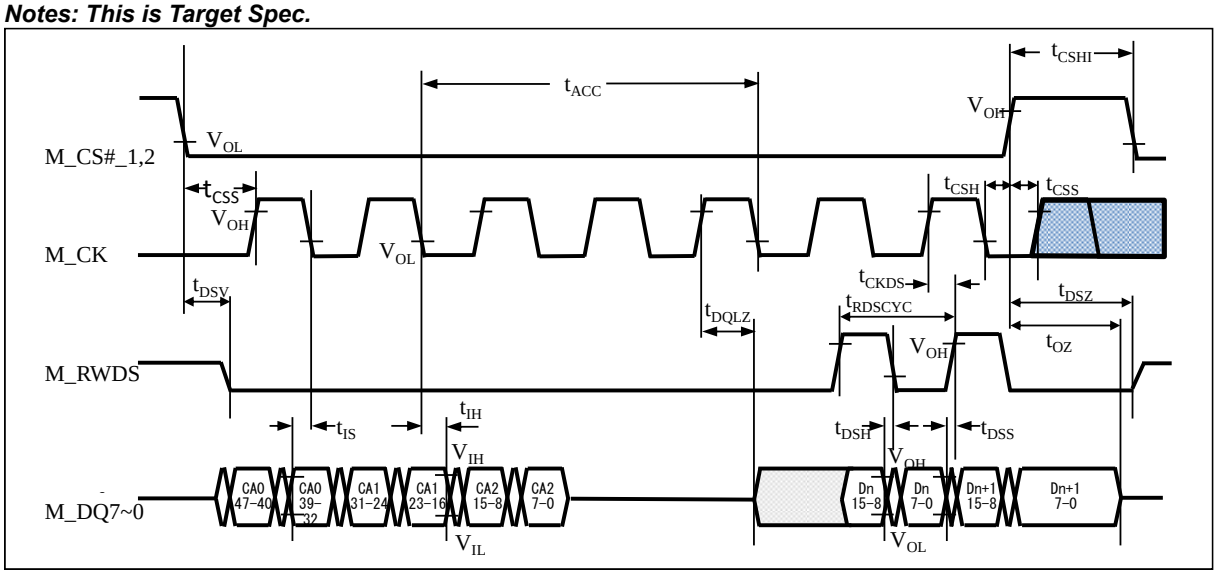


### (3) Hyper Bus Read Timing (HyperFlash)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 3.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Hyper Bus clock cycle | $t_{RDSCYC}$ | M_CK | (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA), | 10.0 | - | ns | |
| CS↑↓ -> CK↑ Chip Select setup time | $t_{CSS}$ | M_CS#_1,2 | | $t_{RDSCYC}$ -2.0 | - | ns | |
| DQ -> CK↑↓ Setup time | $t_{IS}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↑↓ -> DQ Hold time | $t_{IH}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↓ -> CS↑ Chip select hold time | $t_{CSH}$ | M_CS#_1,2 | | $t_{RDSCYC}$ / 2 | - | ns | |
| RDS↑↓> DQ Setup time | $t_{DSS}$ | M_DQ7-0 | | -0.8 | - | ns | |
| RDS↑↓> DQ Hold time | $t_{DSH}$ | M_DQ7-0 | | -0.8 | - | ns | |

***Notes: This is Target Spec.***

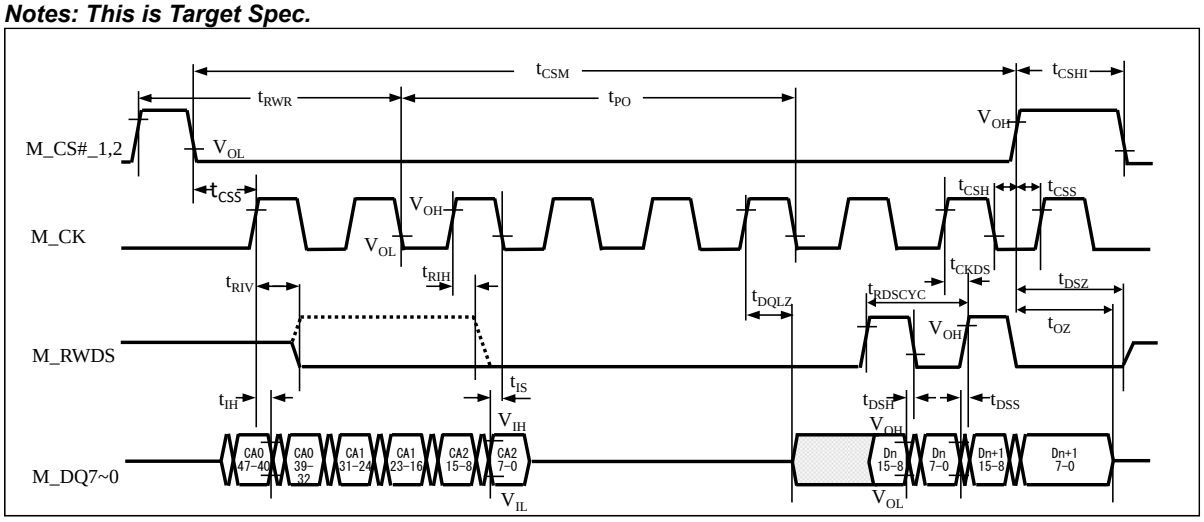


### (4) Hyper Bus Read Timing (HyperRAM)

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Hyper Bus clock cycle | $t_{RDSCYC}$ | M_CK | (CL = 20 pF, $I_{OL}$ = -10 mA, $I_{OH}$ = 10 mA), | 10.0 | - | ns | |
| CS↑↓ -> CK↑ Chip Select setup time | $t_{CSS}$ | M_CS#_1,2 | | $t_{RDSCYC}$ -2.0 | - | ns | |
| DQ -> CK↑↓ Setup time | $t_{IS}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↑↓ -> DQ Hold time | $t_{IH}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↓ -> CS↑ Chip select hold time | $t_{CSH}$ | M_CS#_1,2 | | $t_{RDSCYC}$ /2 | - | ns | |
| RWDS↑↓> DQ (valid) Setup time | $t_{DSS}$ | M_DQ7-0 | | -0.8 | - | ns | |
| RWDS↑↓> DQ (invalid) Hold time | $t_{DSH}$ | M_DQ7-0 | | -0.8 | - | ns | |
| CK↑ -> RWDS↑↓ Refresh Indicator Valid | $t_{RIV}$ | M_RWDS | | - | 6 | ns | |
| CK↑ -> RWDS (Hi-z) Refresh Indicator Hold | $t_{RIH}$ | M_RWDS | | 0 | - | ns | |

***Notes: This is Target Spec.***



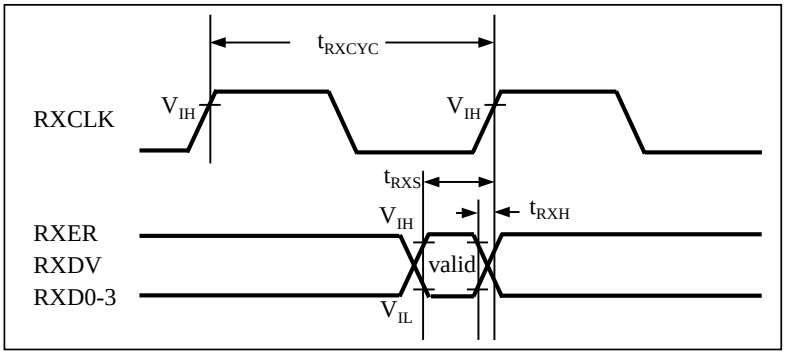
*9.1.4.18 Ethernet AVB*

### (1) Ethernet Receive Timing

($T_A$: Recommended operating conditions, Vcc53 = Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RXCLK cycle | $t_{RXCYC}$ | RXCLK | - | 40.0 | - | ns | - |
| RX setup time | $t_{RXS}$ | RXER<br>RXDV<br>RXD0-3 | | 10.0 | - | ns | $t_{RXCYC}$ -30 ns |
| RX hold time | $t_{RXH}$ | RXER<br>RXDV<br>RXD0-3 | | 0 | - | ns | - |

***Notes: This is Target Spec.***

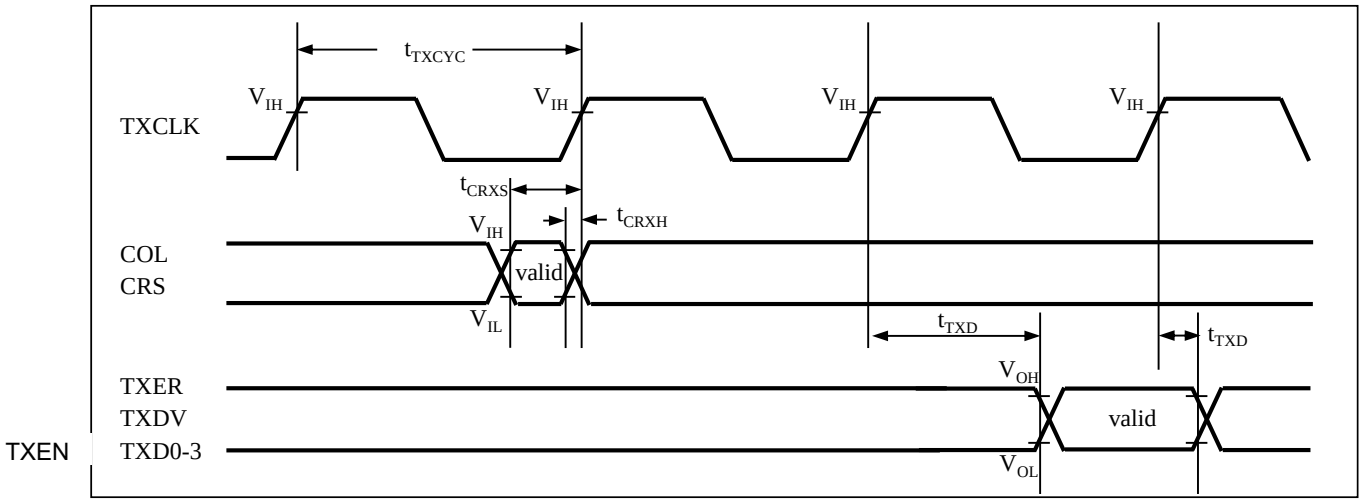


### (2) Ethernet Transmit Timing

($T_A$: Recommended operating conditions, Vcc53 = Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| TXCLK cycle | $t_{TXCYC}$ | TXCLK | (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA), | 40.0 | - | ns | - |
| COL/CRS input setup time | $t_{CRXS}$ | COL CRS | | 12.0 | - | ns | - |
| COL/CRS input hold time | $t_{CRXH}$ | COL CRS | | 0.5 | - | ns | - |
| Tx delay time | $t_{TXD}$ | TXER TXEN TXD0-3 | | 0.5 | 25 | ns | - |

***Notes: This is Target Spec.***

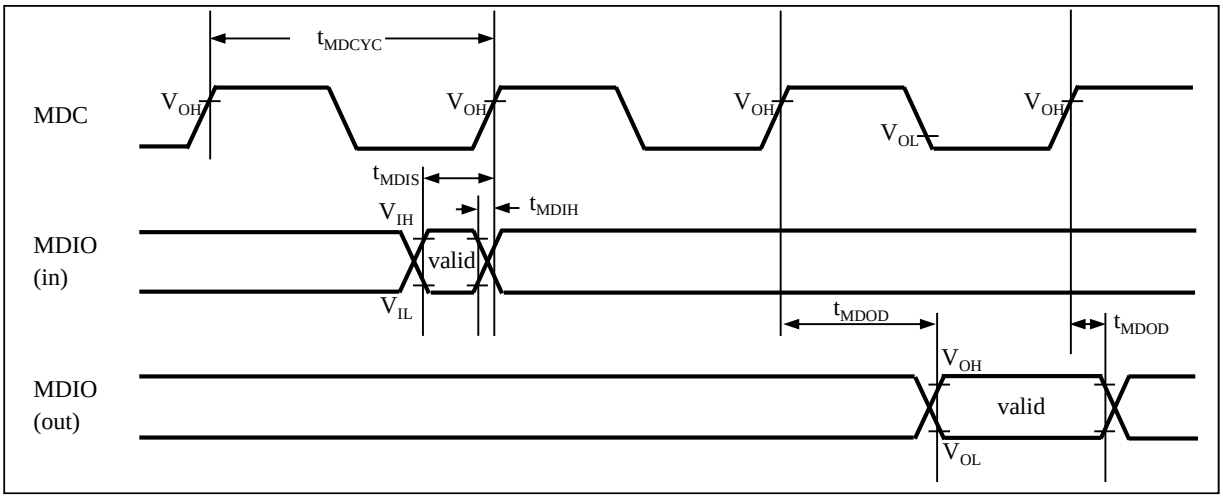


### (3) MDIO Timing

($T_A$: Recommended operating conditions, Vcc53 = Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MDC cycle | $t_{MDCYC}$ | MDC | (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA), | 400.0 | - | ns | - |
| MDIO input setup time | $t_{MDIS}$ | MDIO | | 100.0 | - | ns | |
| MDIO input hold time | $t_{MDIH}$ | MDIO | | 0.0 | - | ns | |
| MDIO output delay time | $t_{MDOD}$ | MDIO | | 10.0 | 190.0 | ns | |

***Notes: This is Target Spec.***



*9.1.4.19 MediaLB*

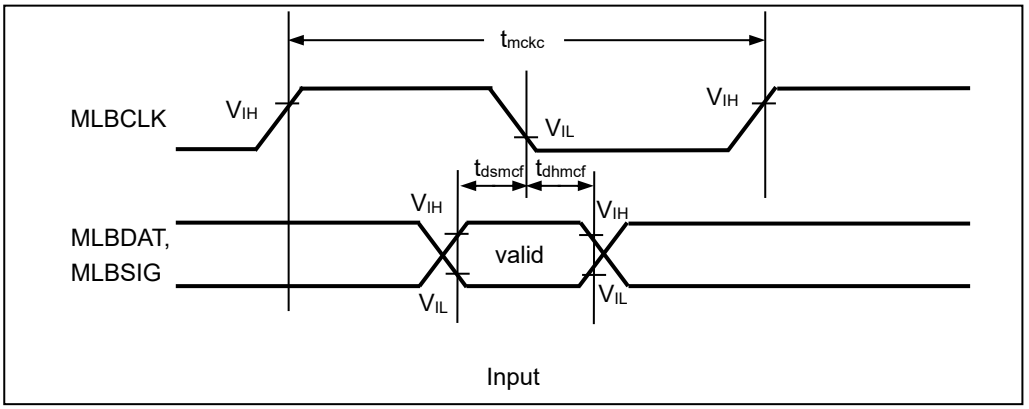
### (1) MediaLB Input Timing

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MLBCLK cycle | $t_{mckc}$ | MLBCLK | - | 40.0 | - | ns | - |
| MLBSIG, MLBDAT Input setup | $t_{dsmcf}$ | MLBSIG MLBDAT | | 1.0 | - | ns | |
| MLBSIG, MLBDAT Input hold | $t_{dhmcf}$ | MLBSIG MLBDAT | | 4.0 | - | ns | |

***Notes: This is Target Spec.***

− *CLK_HAPP1B0 (internal) frequency > MLBCLK (external) frequency*



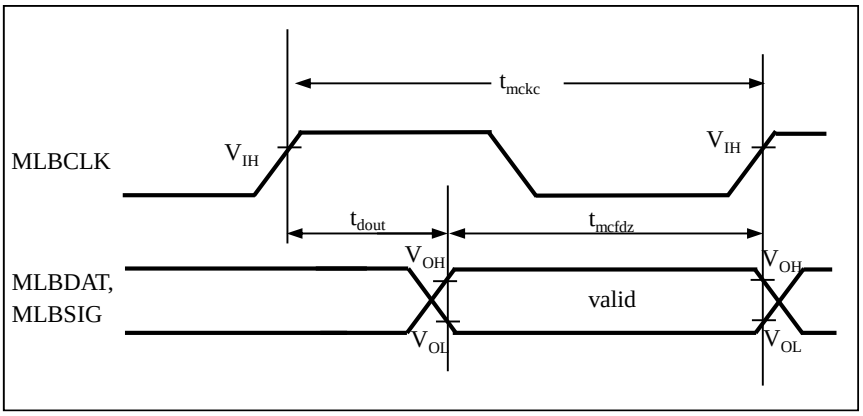

### (2) MediaLB Output Timing

($T_A$: Recommended operating conditions, Vcc3 = 3.3 V ± 0.3 V, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MLBCLK cycle | $t_{mckc}$ | MLBCLK | (CL = 20 pF, $I_{OL}$ = -6 mA, $I_{OH}$ = 6 mA), | 40.0 | - | ns | - |
| MLBSIG, MLBDAT output stop | $t_{mcfdz}$ | MLBSIG MLBDAT | | 26.5 | - | ns | $t_{mckc}$ - $t_{dout}$ |
| MLBSIG, MLBDAT output delay | $t_{dout}$ | MLBSIG MLBDAT | | 0 | 13.5 | ns | - |

***Notes: This is Target Spec.***

− *CLK_HAPP1B0 (internal) frequency > MLBCLK (external) frequency*



*9.1.4.20 Port Noise Filter*

($T_A$: Recommended operating conditions, $V_{CC}5$,$V_{CC}53$,$DV_{CC}5$ = 5.0 V ± 10 %, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

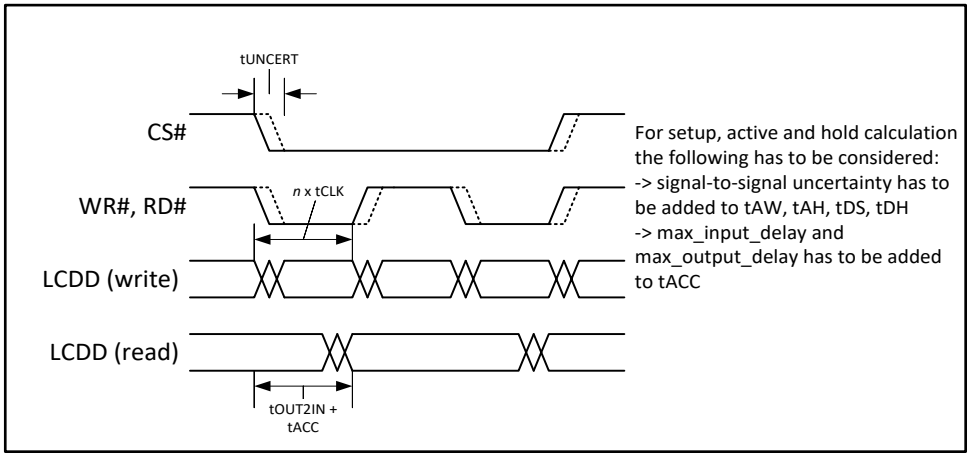
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Width for input removal | - | ALL GPIO | - | - | 17 | ns | - |

* Input pulse width less than at least 17 nm is removed when Port noise filter is enabled.

### 9.1.4.21 LCD Bus I/F

($T_A$: Recommended operating conditions, Vcc53 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V, VCC12 = 1.15 V ± 0.06 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Clock cycle time | tCLK | WR#, RD# | (CL = 20 pF, $I_{OL}$ = -5 mA, $I_{OH}$ = 5 mA), | 12.5 | - | ns | – |
| Signal-to-Signal uncertainty | tUNCERT | CS# | | - | 5.0 | ns | – |
| Output to input duration | tOUT2IN | LCDD0-17 | | - | 25.0 | ns | – |




***Note:***

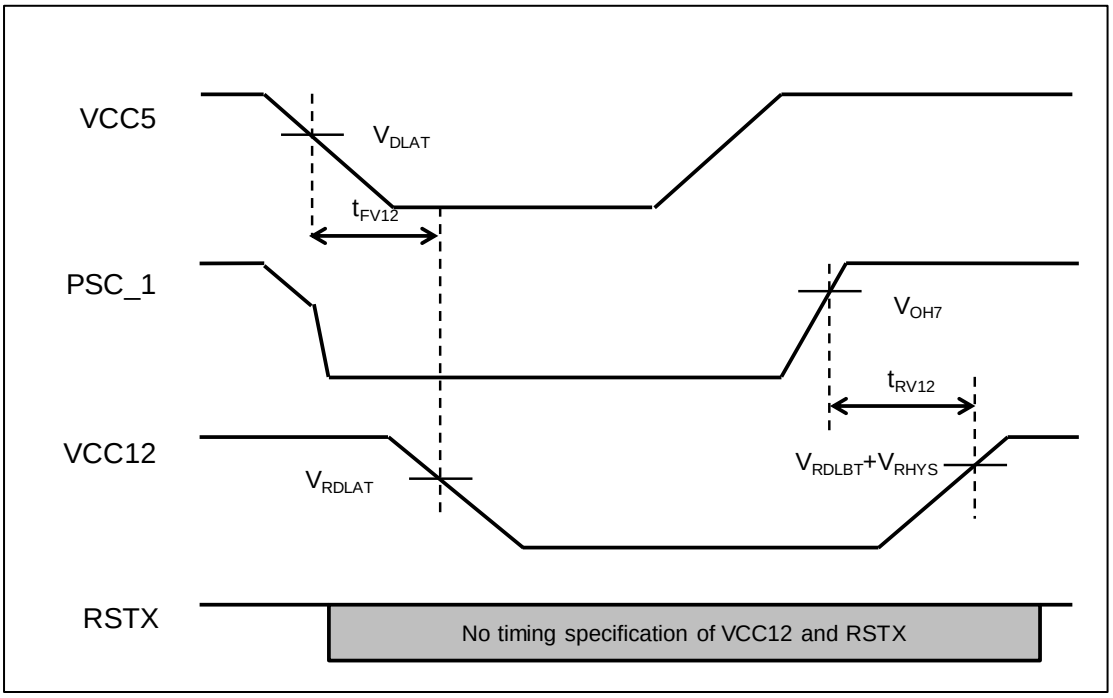
- *In order to calculate interface timing, refer to the LCD controller specification of the external display for the required AC characteristics and S6J3300 Series Hardware Manual.*

*9.1.4.22 Power and Reset Sequence*

VCC5 and VCC12 sequence

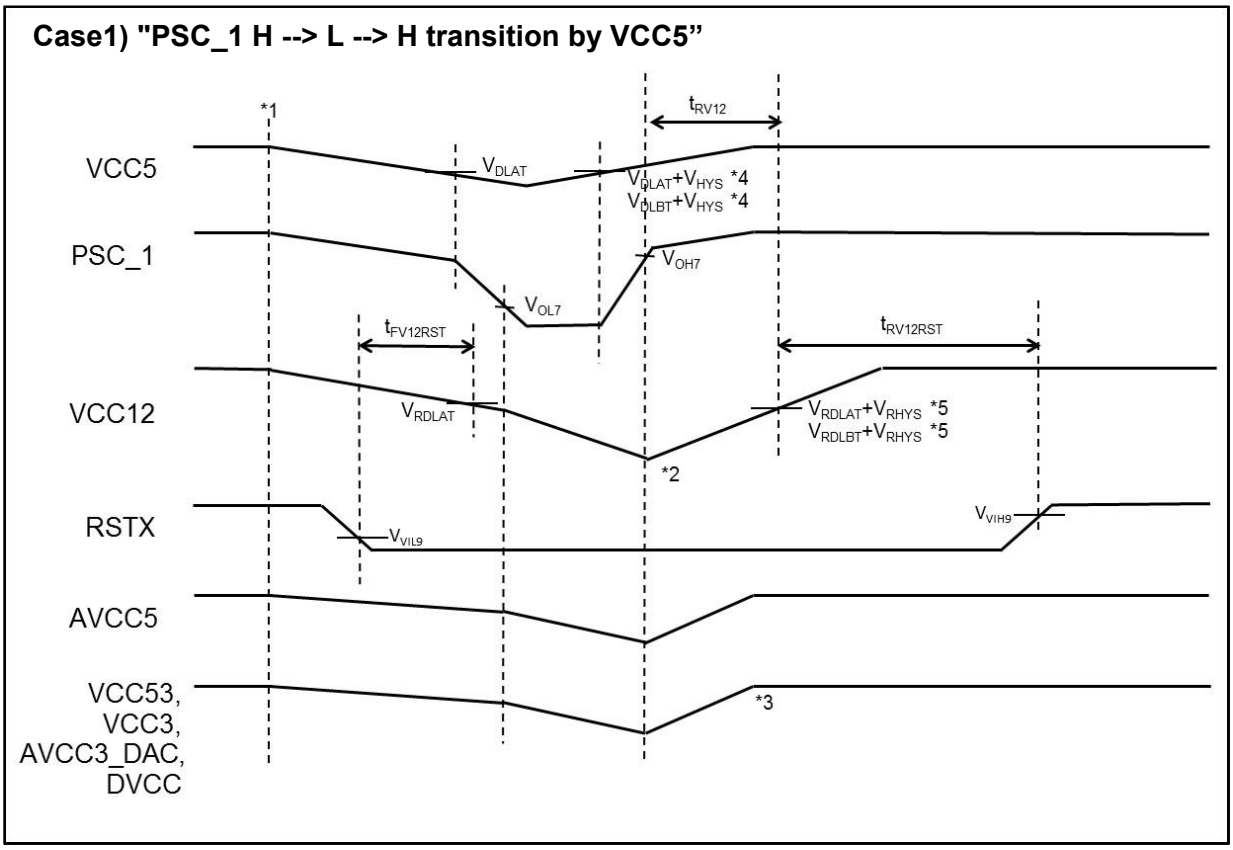
($T_A$: Recommended operating conditions, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Wait time from LVDH1 level detection to falling VCC12 | $t_{FV12}$ | VCC12 | - | 0.6 | - | ms | - |
| VCC12 stabilization time during power-on | $t_{RV12}$ | VCC12 | - | - | 14.2 | ms | - |




***Note:***

- *VDLAT, VRDLAT, VRDLBT and VRHYS are referred to "9.1.4.11 Low Voltage Detection (External Voltage)". VOH7 is referred to "9.1.3 DC Characteristics".*
- *LVDH1 reset need to be "always enable". For details, see the Traveo™ Platform Hardware Manual.*
- *The above sequence needs not to be applied in the following cases the application enters PSS mode: "VCC12 is controlled by PSC_1 at entry and exit from PSS mode" (Normal Sequence).*




***Note:***

- *RSTX controlled by VCC5.*
- *VCC12 and AVCC5 controlled by PSC_1.*
- *VCC53, VCC3, AVCC3_DAC and DVCC controlled by PSC_1. Can be controlled by VCC5 GPIO also.*
- *VDLAT, VDLBT and VHYS are referred to "9.1.4.11 Low Voltage Detection (External Voltage)".*
  *VRDLAT, VRDLBT and VRHYS are referred to “9.1.4.12 Low Voltage Detection (Internal Voltage)".*
  *VOH7, VIL9 and VIH9 are referred to "9.1.3 DC Characteristics".*
  *$t_{RV12}$, $t_{FV12RST}$ and $t_{RV12RST}$ are referred to “9.1.4.22 Power and Reset Sequence”.*

**1: Battery Disconnect: All supplies fall together.*

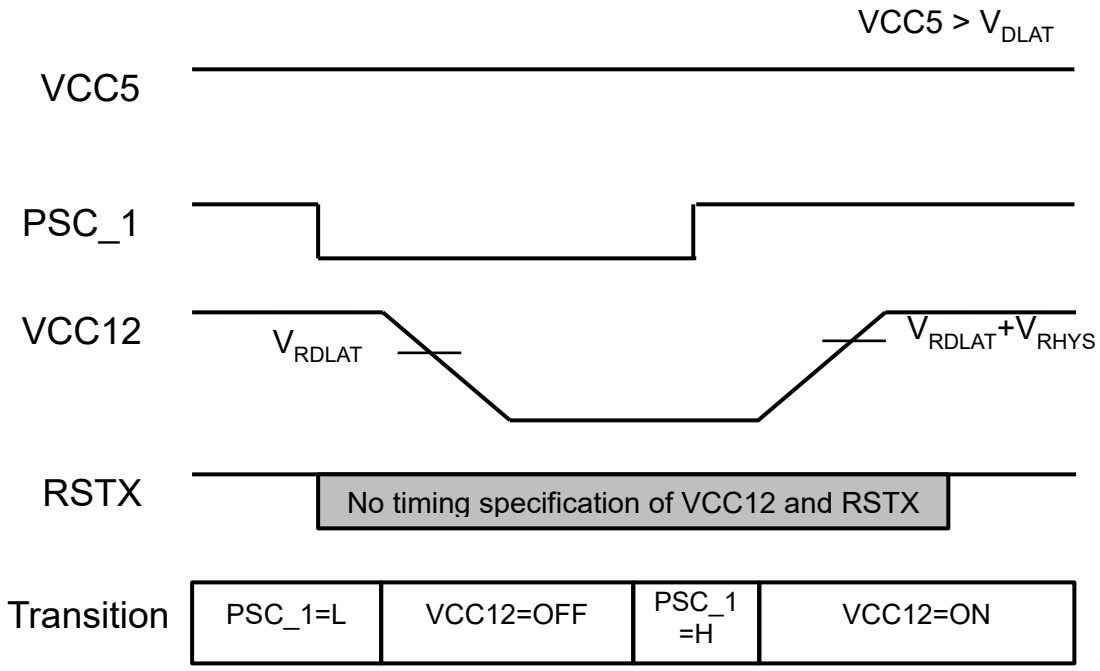
**2: VCC12 can be fully depleted or not full depleted.*

**3: DVCC, VCC53 and VCC3 can start before or after VCC12.*

**4:VCC5 is higher than level detection voltage: VDLAT+VHYS*
*VCC5 is lower than level detection voltage: VDLBT+VHYS*
*VDLAT, VDLBT and VHYS are referred to "9.1.4.11 Low Voltage Detection (External Voltage)".*

**5:VCC5 is higher than level detection voltage: VRDLAT+VRHYS*
*VCC5 is lower than level detection voltage: VRDLBT+VRHYS*
*VRDLAT, VRDLBT and VRHYS are referred to "9.1.4.11 Low Voltage Detection (External Voltage)".*

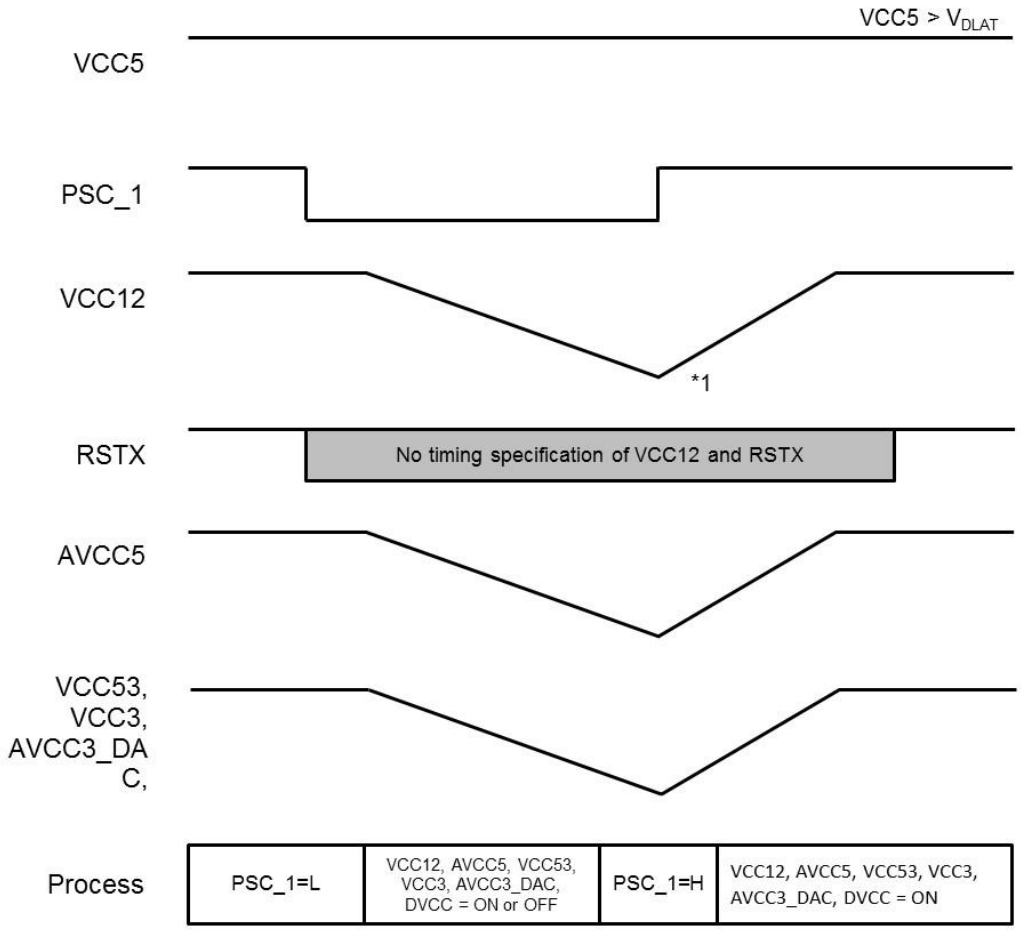
**Case2-1) "PSC_1 H --> L --> H transition by User Program”**




***Note:***

- *VCC12 controlled by PSC_1.*
- *VCC12 can be fully deplete*

**Case2-2) "PSC_1 H --> L --> H transition by User Program"**




***Note:***

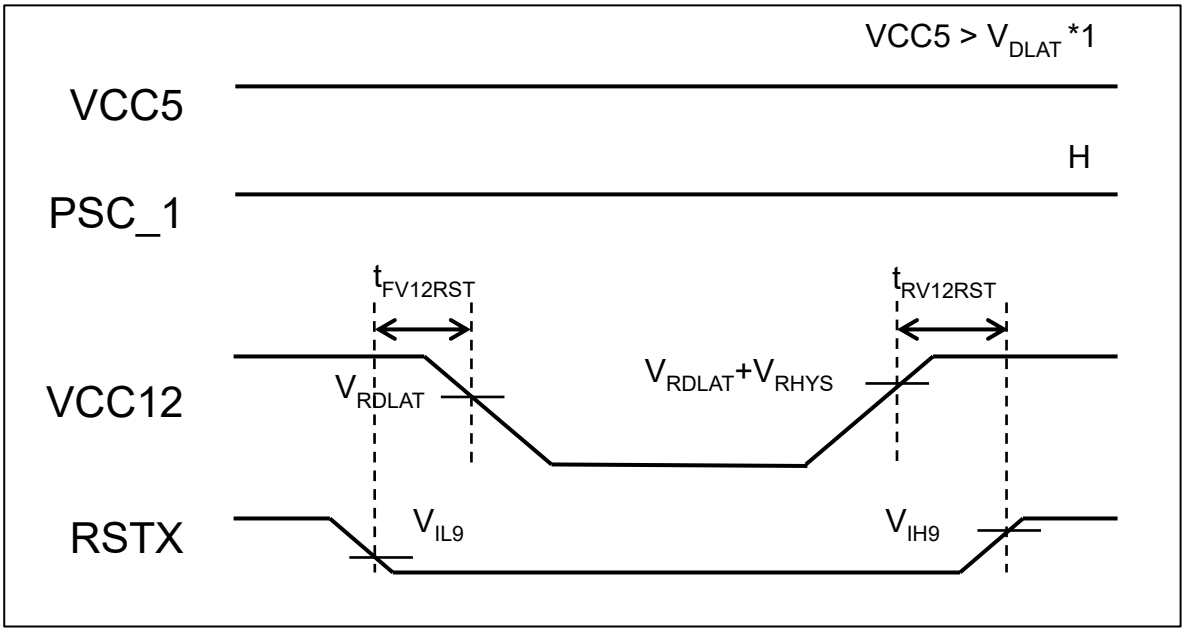
- *VCC12 and AVCC5 controlled by PSC_1.*
- *VCC53, VCC3, AVCC3_DAC and DVCC controlled by PSC_1. Can be controlled by VCC5 GPIO also.*

**1: VCC12 can be fully depleted or not full depleted.*

VCC12 and RSTX Sequence

($T_A$: Recommended operating conditions, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RSTX -> VCC12 fall interval time | $t_{FV12RST}$ | VCC12, RSTX | - | 5 | - | us | - |
| VCC12 -> RSTX rise interval time | $t_{RV12RST}$ | VCC12, RSTX | | 35 | - | us | - |



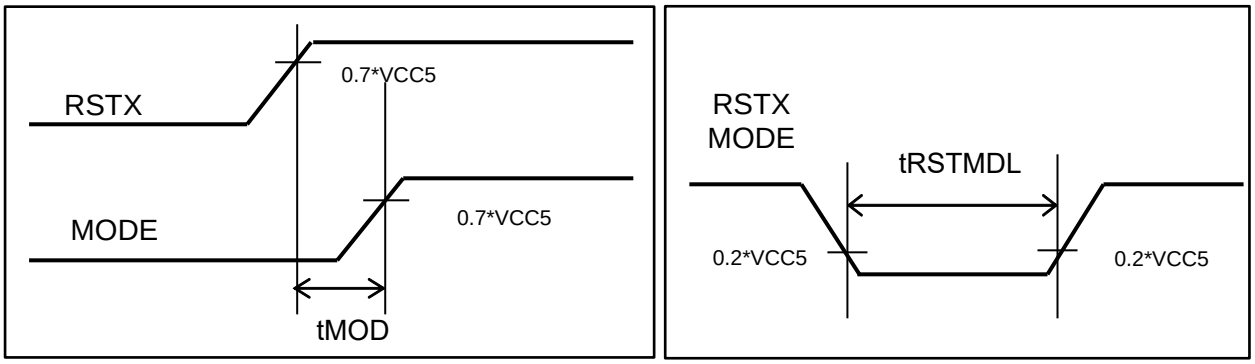

***Note:***

- *If the sequence given in "VCC5 and VCC12 sequence" cannot be applied, this sequence can be applied.*
- *VDLAT VRDLAT, VRDLAT and VRHYS are referred to "9.1.4.11 Low Voltage Detection (External Voltage)". VIL9 and VIH9 is referred to "9.1.3 DC Characteristics".*
- *This sequence is applied in case of VCC12 power on/off and assertion of RSTX is controlled by application.*
- *This sequence is applied under the condition VCC5 > VDLAT and PSC_1 = H.*

RSTX and MODE Sequence

($T_A$: Recommended operating conditions, Vcc5 = 5.0 V ± 10 % / 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RSTX ↑ -> MODE ↑ delay time | tMOD | RSTX, MODE | - | -5 | 5 | ns | – |
| Reset and mode input time | tRSTMDL | RSTX, MODE | - | 10 | - | us | – |
| Width for reset and mode input removal | | | | 1 | - | us | – |




***Note:***

- *If the sequence given in "VCC5 and VCC12 sequence" and "VCC12 and RSTX Sequence" cannot be applied, this sequence can be applied.*
- *Connect RSTX signal and MODE signal outside of the MCU and shorten the trace length between MCU and these two signal lines.*
- *The following assumptions are made with regard to the workaround described above.*
  1. *After the reset the MCU state is equivalent to the "cold start state" usually reached by power-on-reset.*
  2. *Debugger interface and PC writer interface are not enabled.*
  3. *The RAM retention cannot be guaranteed when applying this workaround*
  4. *Pin PSC_1 will be driven low while RSTX is active (RSTX at low level)*

### 9.1.5 A/D Converter

#### 9.1.5.1 Electrical Characteristics

($T_A$: Recommended operating conditions, $V_{CC}5$ = 5.0 V ± 10 %, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 12 | bit | – |
| Total Error | - | - | - | - | ±12 *6 | LSB | *3 |
| | | | - | - | ±15 *7 | LSB | - |
| Integral Non linearity | - | - | - | - | ±4.0 | LSB | *4 |
| Differential Non linearity | - | - | - | - | ±1.9 | LSB | *4 |
| Zero transition voltage | $V_{ZT}$ | AN0 to AN63 | AVRL -11.5LSB *6 | - | AVRL +12.5LSB *6 | V | *5 |
| | | | AVRL -14.5LSB *7 | - | AVRL +15.5LSB *7 | V | |
| Full-scale transition voltage | $V_{FST}$ | AN0 to AN63 | AVRH -13.5LSB *6 | - | AVRH +10.5LSB *6 | V | |
| | | | AVRH -16.5LSB *7 | - | AVRH +13.5LSB *7 | V | – |
| Sampling time | $t_{SMP}$ | - | 0.3 | - | - | µs | *1 |
| Compare time | $t_{CMP}$ | - | 0.8 | - | 26 | µs | *1 |
| A/D conversion time | $t_{CNV}$ | - | 1. 1 | - | - | µs | *1 |
| Resumption Time | - | - | - | - | 1 | µs | - |
| Analog port input current | $I_{AIN}$ | AN0 to AN30, AN32 to AN38 | -1.0 | - | 1.0 | µA | $AV_{SS}$≤ $V_{AIN}$ ≤ $AV_{CC}5$ |
| | | AN31, AN39 to AN63 | -2.0 | - | 2.0 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN63 | AVRL | - | AVRH | V | – |
| Reference voltage | AVRH | AVRH5 | 4.5 *6 | - | 5.5 *6 | V | AVcc5 ≥ AVRH |
| | | | 3.0 *7 | - | 3.6 *7 | | |
| | AVRL | AVRL5/AVSS | - | 0.0 | - | V | – |
| Power supply current | $I_A$ | AVCC5 | - | 500 | 900 (Target) | µA | 1 unit |
| | $I_{AH}$ | | - | 1.0 | 200 (Target) | µA | *2 |
| | $I_R$ | AVRH5 | - | 1.0 | 3.5 (Target) *6 | mA | 1 unit |
| | | | - | 1.0 | 2.5 (Target) *7 | mA | 1 unit |
| | $I_{RH}$ | | - | - | 9.0 (Target) | µA | *2 |
| Variation between channels | - | AN0 to AN63 | - | - | 4.0 | LSB | – |

*1: Time per channel

*2: Definition of the power supply current (when Vcc5 = AVcc5 = 5.0 V) while the A/D converter is not operating and in stop mode

*3: Total Error is a comprehensive static error that includes the linearity after trimming by software. 1 LSB = (AVRH-AVRL)/4096

*4: 1 LSB = (VFST-VZT)/4094

*5: 1 LSB = (AVRH-AVRL)/4096

*6: For S6J33xxxSx or S6J33xxxUx or S6J33xxxTx or S6J33xxxVx option.

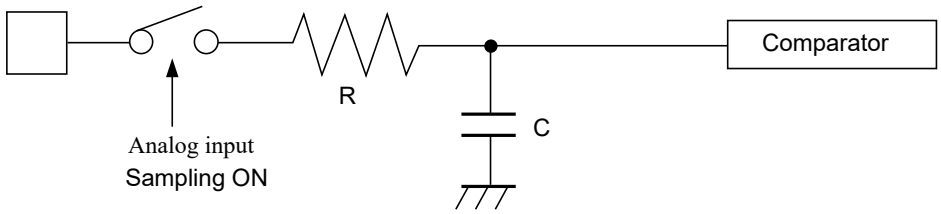
*7: For S6J33xxxAx or S6J33xxxBx or S6J33xxxCx or S6J33xxxDx or S6J33xxxEx or S6J33xxxFx or S6J33xxxGx or S6J33xxxHx option.

*9.1.5.2 Notes on A/D Converters*

**About the Output Impedance of an External Circuit for Analog Input**

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 µF) to an analog input pin.

Analog input circuit model




| R | C | | |
|---|---|---|---|
| 12-bit A/D | 3.9 kiloohms (max) | 11.0 pF (max) | (4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V) |

Note: Use the numerical values provided here simply as a guide.

### 9.1.5.3 Glossary

Resolution: Analog change that can be identified by an A/D converter

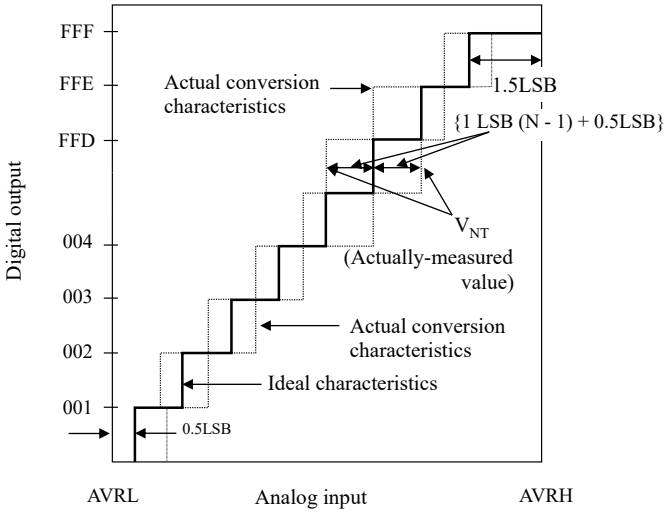
Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics

includes zero transition error, full-scale transition error, and non linearity error.

Differential linearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB

Total error: Difference between the actual value and the theoretical value. The total error

Total error




$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + 0.5\text{LSB}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$1\text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{4096}\ [\text{V}]$$

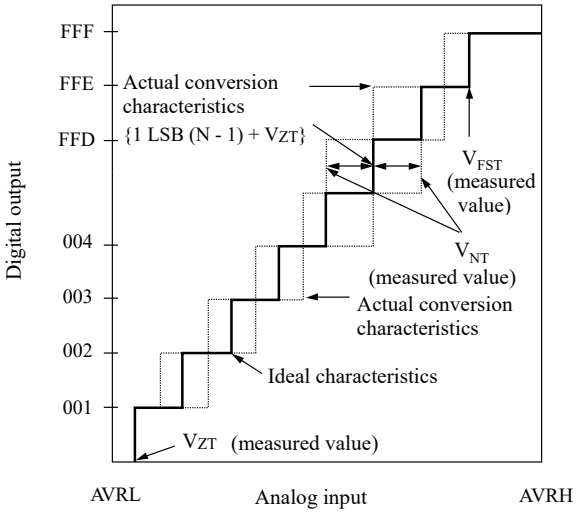
N: A/D converter digital output value.

$V_{ZT}$ (Ideal value) = AVRL + 0.5LSB[V]

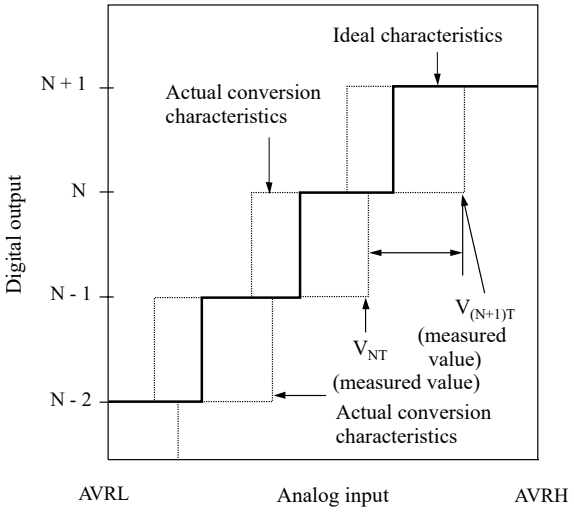
$V_{FST}$ (Ideal value) = AVRH - 1.5LSB[V]

$V_{NT}$: Voltage at which the digital output changes from "(N – 1)" to "N".

Integral linearity error




Differential linearity error




$$\text{Integral linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{ZT}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}\ [\text{V}]$$

$V_{ZT}$: Voltage for which digital output changes from "0x000" to "0x001"

$V_{FST}$: Voltage for which digital output changes from "0xFFE" to "0xFFF".

### 9.1.6 Audio DAC

#### 9.1.6.1 Electrical Characteristics

($T_A$: Recommended operating conditions, $AV_{CC}3_DAC$ = 3.3 V ± 0.3 V, $V_{CC}12$ = 1.15 V ± 0.06 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions *1 | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| system clock frequency | $F_{CLKDA0}$ | - | - | 2.048 | - | 18.432 | MHz | - |
| sampling clock | fs | - | - | 8 | - | 48 | kHz | - |
| Analog output load resistance *2 | $R_L$ | DAC_L DAC_R | - | 20 | - | - | kΩ | - |
| Analog output load capacitance *2 | $C_L$ | | - | - | - | 100 | pF | - |
| capacitance | - | C_L C_R | - | 1.1 | 2.2 | 10 | µF | - |
| Analog output single-end output range (±full scale) | - | DAC_L DAC_R | $R_L$ = 20 kΩ $C_L$ = 100 pF | - | 0.673 $AV_{CC}3_DAC$ | - | $V_{P-P}$ | - |
| Analog output voltage (zero) | - | | - | - | 0.5 $AV_{CC}3_DAC$ | - | V | - |
| THD+N *3 | - | - | signal frequency: 1 kHz LPF (fc: 20 kHz) | - | -82 | -72 | dB | - |
| SNR *3 | - | - | signal frequency: 1 kHz LPF (fc: 20 kHz)—— A-weighting filter | 85 | 89 | - | dB | - |
| Dynamic range *3 | - | - | | 83 | 86 | - | dB | - |
| Out-of-Band Energy | - | - | 20 kHz to 64 fs | - | - | -33 | dB | - |
| Channel Separation | - | - | - | - | 80 | - | dB | - |
| Output impedance | - | - | - | 150 | 200 | 250 | Ω | - |
| PSRR | - | - | digital input: zero, noise 50 Hz | - | -35 | - | dB | - |
| | | | digital input: zero, noise 1 kHz | - | -50 | - | dB | - |
| | | | digital input: zero, noise 20 kHz | - | -40 | - | dB | - |
| | | | digital input: full scale sine | - | -13 | - | dB | - |
| Supply current normal operation | - | AVCC3_DAC | - | - | 2.2 | 3.2 | mA | - |
| Supply current power-down | - | AVCC3_DAC | - | - | - | 100 | µA | - |
| Startup Time *4 | - | - | DAE↑ | - | 650 *6 | - | ms | - |

*1: All parameters specified fs = 44.1 kHz, system clock 256 fs and 16-bit data, RL-20 kΩ, CL = 100 pF, unless otherwise noted.

*2: Refer to notes *5

*3: These values do not include the noise caused by the analog power supply. (Refer to *7. Use examples)

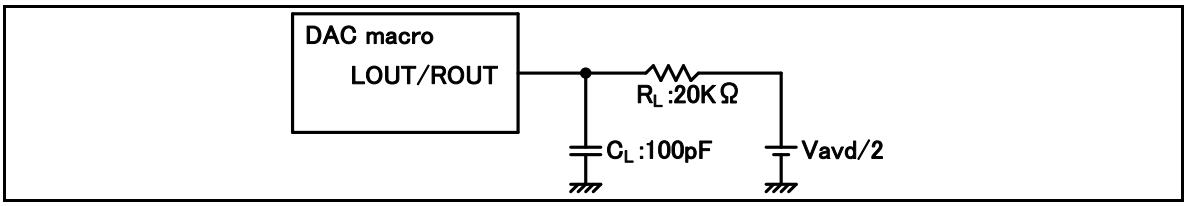
*4: 2.2 µF is connected to C_L, C_R.

*5: Load connection

$R_L$ is connected to AVCC3_DAC /2 (Figure 9.1).

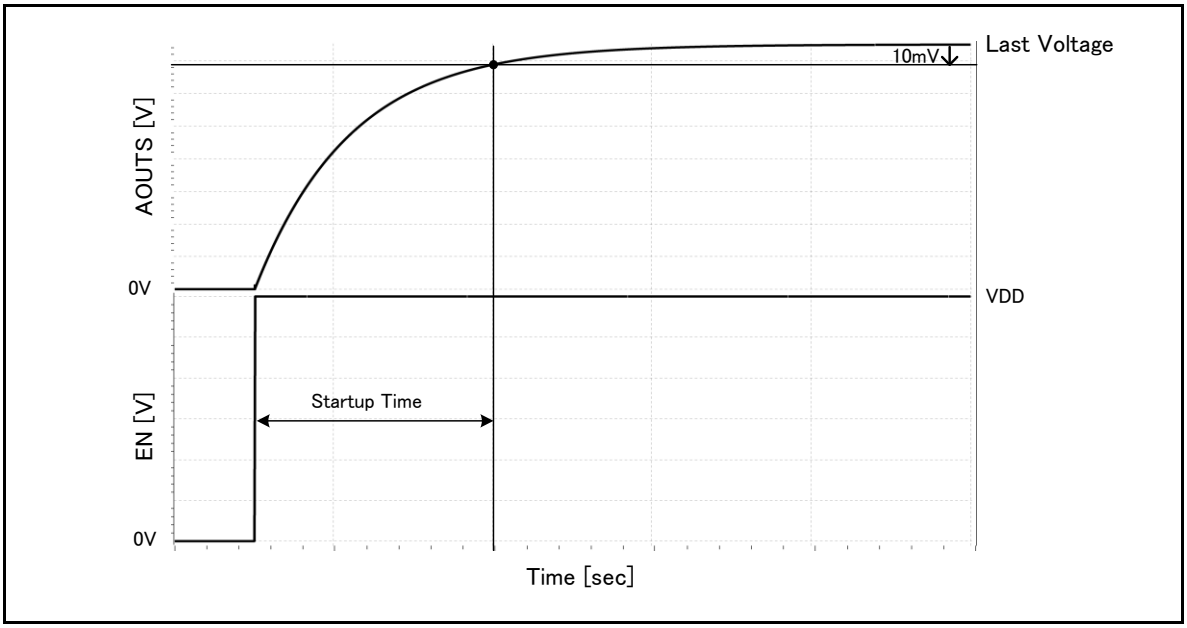
If $R_L$ is connected to ground, the coupling capacitance must be inserted as shown in (Figure 9.3)

**Figure 9-1: Connection between $R_L$ and AVCC_DAC/2 (Example)**




*6: Start up time

**Figure 9-2: Startup Time**




*Start up time can be calculated as follows.

1.Start up time (TYP) = 650[ms] (*4)

2.CCOM = 10 µF × (1 ± α/100)

CCOM is a capacitor connected to Terminal C_L/C_R including capacitance variance.

α = Capacitance variance[%]

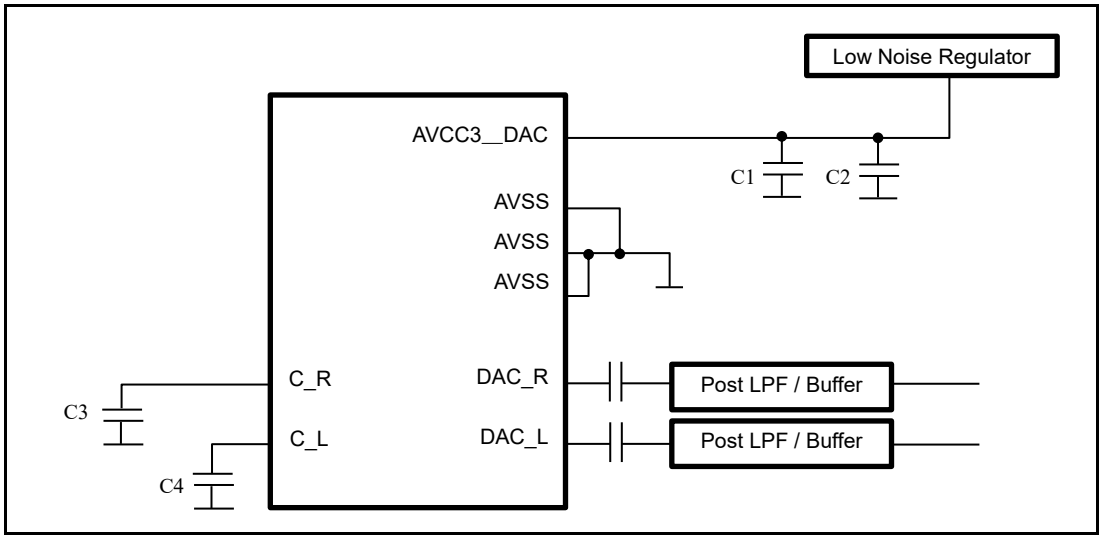
3.Start up time = Start up time (TYP) × (1±α) [ms]

For example, CCOM = 2.42 µF then α = (2.42 µF - 2.2 µF)/2.2 µF = 10[%]

So, Start up time = 650 ms × (1+10/100) = 715[ms]

*7 Use examples

**Figure 9-3: Coupling Capacitance (Example)**




***Notes:***

- *C1: more than 10 µF low ESR capacitors*
- *C2: 0.1 µF ceramic capacitors*
- *C3,C4: 2.2 µF low ESR capacitors*
- *Impedance of each power line must be as low as possible.*

***Notes:***

- *When DAC is not used in your system, the related pins should be*
- *AVCC3_DAC = GND and AVSS = GND*
- *C_L = OPEN and C_R = OPEN*
- *DAC_L = OPEN and DAC_R = OPEN*

### *9.1.7 FLASH Memory*

#### *9.1.7.1 Electrical Characteristics*

| Parameter | Rating | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 120 | 180 | ms | Large sector*1<br>Internal preprogramming time included |
| | - | 120 | 180 | ms | 8 kB sector*1<br>Internal preprogramming time included |
| | - | 120 | 180 | ms | 4 kB sector*2<br>Internal preprogramming time included |
| 16-bit write time (Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 32-bit write time (Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 64-bit write time (Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 256-bit write time (Program) | - | 40 | 70 | µs | System-level overhead time excluded*1 |
| Page mode write time (Program) | - | 320 | 600 | µs | System-level overhead time excluded*1 |
| 32-bit write time (Work) | - | 30 | 60 | µs | System-level overhead time excluded*2 |
| Erase count / Data retention time (Program) | 1,000/20 years | - | - | - | Temperature at write/erase time Average temperature $T_A$ = +85 degrees Celsius |
| Erase count / Data retention time (Work) | 1,000/20 years<br>10,000/10 years<br>100,000/5 years | - | - | - | Temperature at write/erase time Average temperature $T_A$ = +85 degrees Celsius |

*1: Guaranteed value for up to 1,000 erases

*2: Guaranteed value for up to 100,000 erases

#### *9.1.7.2 Notes*

While the Flash memory is written or erased, shutdown of the external power (Vcc5) is prohibited.

In the application system where Vcc5 might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage ($V_{DL}$), hold Vcc5 at 2.7 V or more within the duration calculated by the following expression:

Td*1 [µs] + ( 1 / $F_{CRF}$*2[MHz] ) x 1029 + 25 [µs]

*1: See "9.1.4.11 Low Voltage Detection (External Voltage)"

*2: See "9.1.4.1 Source Clock Timing"

## 10. Acronyms

| Acronym | Description |
|---|---|
| A/D converter | Analog digital converter |
| ADC | Analog digital converter |
| AHB | Advanced high performance bus |
| AMBATM | Advanced microcontroller bus architecture |
| APB | Advanced peripheral bus |
| ATCM | TCM-A port |
| AXI | Advanced extensible interface |
| B0TCM | TCM B0 port |
| B1TCM | TCM B1 port |
| BBU | Bit banding unit |
| BDR | Boot description record |
| BTL | Bridge-tied load |
| CAN | Control are network |
| CD | Clock domain |
| CPU | Central processing unit |
| CR | CR Oscillator |
| CRC | Cyclic redundancy check |
| CSV | Clock supervisor |
| DAC | Digital analog converter |
| DAP | Debug access port |
| DED | Dual error detection |
| DMA | Direct memory access |
| DMAC | DMA controller |
| EAM | Exclusive access memory |
| ECC | Error correction code |
| ETM | Embedded trace macro |
| EXT-IRC | External interrupt controller |
| FIQ | Fast interrupt request |
| FPU | Floating point unit |
| FRT | Free run timer |
| GPIO | General purpose I/O |
| HPM | High performance matrix |
| HW-WDT | Hardware watchdog timer |
| I/O | Input or output |
| I2S | Inter-IC sound |
| ICU | Input capture unit |
| IPCU | Inter-processor communication unit |
| IRC | Interrupt controller |
| IRQ | Interrupt request |
| ISR | Interrupt service routine |
| JTAG | Joint test action group |

| Acronym | Description |
|---|---|
| LLPP | Low latency peripheral port |
| LVD | Low voltage detector |
| MCU | Microcontroller unit |
| MFS | Multi-function serial interface |
| NF | Noise filter |
| NMI | Non maskable interrupt |
| OCU | Output compare unit |
| OSC | Oscillator |
| PCM | Pulse coded module |
| PLL | Phase locked loop |
| PONR | Power on reset |
| PPC | Port pin configuration |
| PSS | Power saving state |
| PWM | Pulse width modulation |
| RAM | Random access memory |
| RIC | Resource input configuration |
| ROM | Read only memory |
| RTC | Real time clock |
| RVD | Low voltage detection and reset for RAM retention |
| SCT | Source clock timer |
| SEC | Single error correction |
| SECDED | Single error correction and dual error detection |
| SHE | Secure Hardware Extension |
| SMC | Stepper motor controller |
| SMIX | Sound mixer |
| SRAM | Static RAM |
| SWFG | Sound waveform generator |
| SW-WDT | Software watchdog timer |
| SYSC | System controller |
| TCFLASH | FLASH connected to TCM |
| TCM | Tightly coupled memory |
| TCRAM | RAM connected to TCM |
| TPU | Timing protection unit |
| UDC | Up-down counter |
| VIC | Vectored interrupt controller |
| VRAM | Video RAM |
| WDR | Watchdog description record |
| WDT | Watchdog timer |
| WFG | Waveform generator |
| WorkFLASH | Work FLASH memory |

## 11. Ordering Information

| Part Number | Package |
|---|---|
| S6J331EKSESE20000 | 208-pin plastic TEQFP (LEW208) |
| S6J332CKSDSE20000 | 208-pin plastic TEQFP (LEW208) |
| S6J334CKSESE20000 | 208-pin plastic TEQFP (LEW208) |
| S6J331EJSESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J332EJBDSE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J332EJTDSE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J332EJBESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J332EJTESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J332DJEESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334BJDDSE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334EJBESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334EJTESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334EJEESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334DJTESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334DJEESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334CJBESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334CJEESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334BJDESE20000 | 176-pin plastic TEQFP (LEV176) |
| S6J334EJTCSE2000A | 176-pin plastic TEQFP (LEV176) |
| S6J334EJEDSE2000A | 176-pin plastic TEQFP (LEV176) |
| S6J332EHBESE20000 | 144-pin plastic TEQFP (LEX144, LEK144) |
| S6J334EHEESE20000 | 144-pin plastic TEQFP (LEX144, LEK144) |
| S6J334DHEESE20000 | 144-pin plastic TEQFP (LEX144, LEK144) |
| S6J334DHFESE20000 | 144-pin plastic TEQFP (LEX144, LEK144) |
| S6J334CHEESE20000 | 144-pin plastic TEQFP (LEX144, LEK144) |
| S6J334CHFESE20000 | 144-pin plastic TEQFP (LEX144, LEK144) |

# 12. Errata

This section describes the errata for the S6J3310/3320/3330/3340 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

### Part Numbers Affected

| Part Number |
|---|
| S6J331xxxx<br>S6J332xxxx<br>S6J333xxxx<br>S6J334xxxx |

### S6J331/2/3/4 Qualification Status

Product Status: Production

### Errata Summary

The following table defines the errata applicability to available S6J3310/3320/3330/3340 Series devices.

| Items | Part Number | Fix Status |
|---|---|---|
| MCAN wrong message transmission | S6J331xxxx<br>S6J332xxxx<br>S6J333xxxx<br>S6J334xxxx | Not be planned. |

### 1. MCAN wrong message transmission

**■ Problem Definition**

There is a possibility a message with an ID (arbitration field) and a format and DLC (control field) is transmitted which was not configured by the application. The message itself is syntactically correct and can be received by other nodes.

The occurrence of the limitation requires a certain relationship in time between a transmission request for sending a message and the coincidence of noise in the 3rd bit of intermission field which is treated as the start of new message transmission (SoF).

**■ Trigger Condition**

Under the following conditions a message with wrong ID, format and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission.
- A new transmission is requested after sample point of 2nd bit of intermission but before the 3rd bit of Intermission is reached.
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2).

**■ Scope of Impact**

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message.
- The M_CAN will start arbitration with wrong ID, format, and DLC.

- In case the ID won arbitration, a CAN message with valid CRC is transmitted.
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus
- Neither an error is detected by the transmitting node nor at the receiving node.

**■ Workaround**

**Workaround 1:**

This workaround avoids submitting a transmission request in the critical time window of about one bit time before the sample point of the 3rd bit of intermission field when on other pending transmission request exists:

- Request a new transmission if another transmission is already pending or when the M_CAN / M_TTCAN is not in state "Receiver" (when PSR.ACT ≠ "10").
- If no pending transmission request exists, the application software needs to evaluate the Rx Interrupt flags IR.DRX, IR.RF0N, IR.RF1N which are set at the last bit of EoF when a received and accepted message gets valid.
- A new transmission may be requested by writing to TXBAR once the Rx interrupt occurred and the application waited another 3 bit times before submitting its Tx request. Note the Rx interrupt is generated at the last bit of EoF which is followed by three bits of Intermission.
- The application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

A supplemental action can be applied in order to detect messages which contain wrong ID and control filed information:

- A checksum covering arbitration and control fields can be added to the data field of the message to be transmitted, to detect frames transmitted with wrong arbitration and control fields.

**Workaround 2:**

This workaround ensures that always at least one pending Tx request exists. If that is the case, the application may launch its Tx requests at any time without suffering from the limitation.

- Define a low priority message with DLC = 0 that can be sent without harm. E.g. loses arbitration against all other application messages, does not pass any acceptance filter of nodes in the same network. DLC = 0 shall reduce latency for other application messages.
- Configure sufficient Tx buffers – at least two - for this message type thus that there is always another one waiting to be sent. E.g. an application that cannot react quickly enough with the time a single message of this type is sent, more than 2 Tx buffer may become necessary.
- The application uses the standard interfaces of the CAN / CAN FD stack to feed these messages.
- Whenever Tx confirmation is indicated for the second but last message of this type with pending Tx request, the application needs to submit at least one new Tx request. Note Tx confirmation is a standard feature in the AUTOSAR SW architecture.
- Before initially leaving INIT state of the M_CAN IP by clearing CCCR.INIT bit, make sure to activate a Tx request after having cleared CCCR.CCE. This will ensure that the conditions for the occurrence of the limitation when synchronizing to the CAN bus the first time after RESET are prevented.

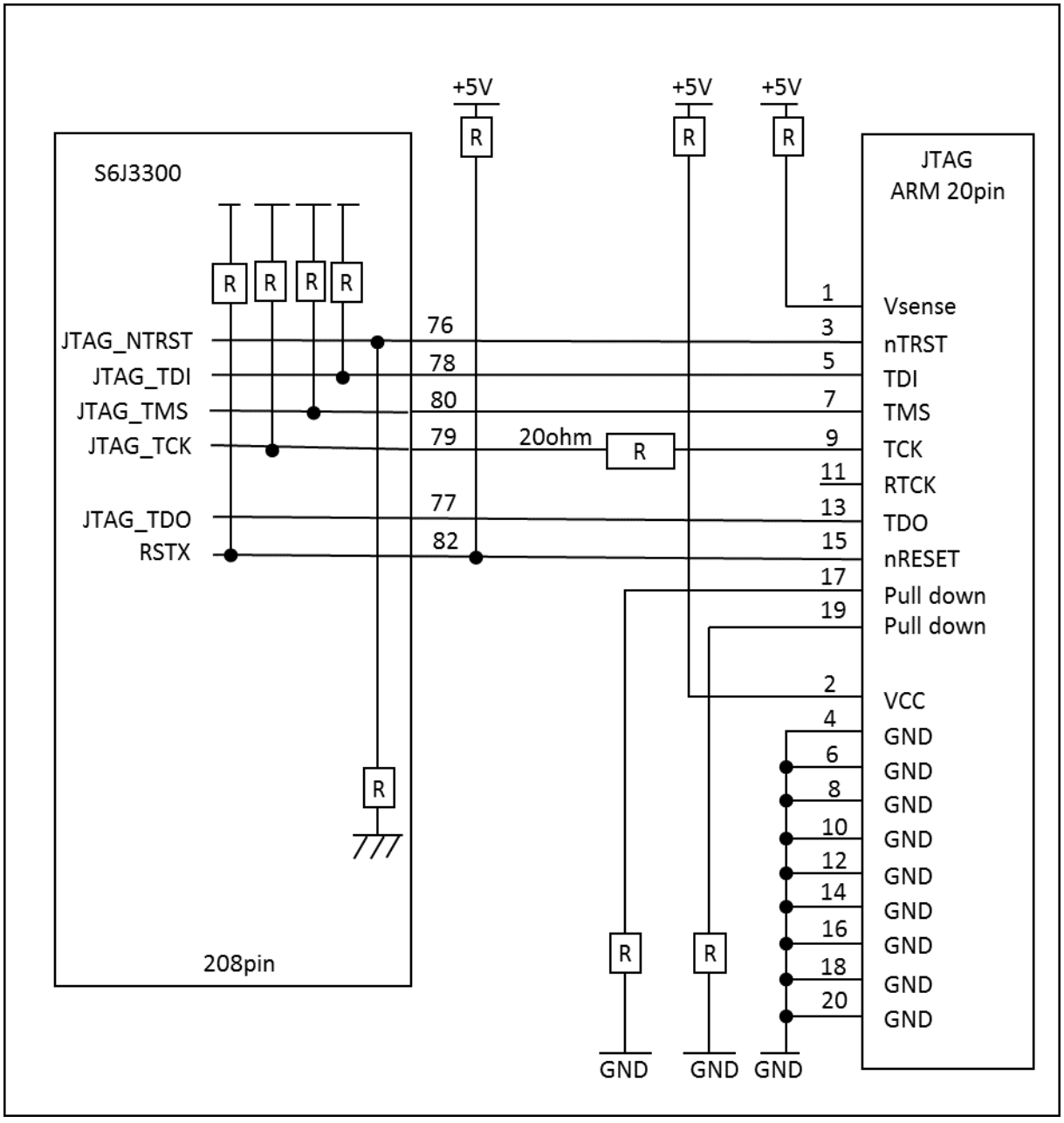
**■ Fix Status**

Not be planned.

# 13. Appendix

## 13.1 Application 1: JTAG Tool Connection

This is an application example of JTAG tool connection. See the relevant application note 002-03898 in detail.



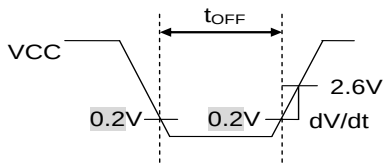
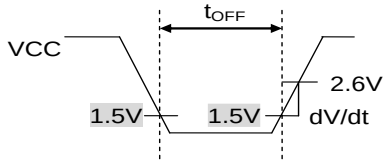
## 14. Major Changes

| Page | Section | Change Results |
|---|---|---|
| Rev. *A | | |
| 7 | 2.Function List<br>2.2Optional function | Revised CHIP-ID and Revision as below:<br>Error)<br>Function Digit Revision Chip ID<br>S,U,T,V B 0x10120000<br>A,C,E,G B 0x1012A000<br>B,D,F,H B 0x10122000<br><br>Correct)<br>Function Digit Revision Chip ID<br>S,U,T,V C 0x10122100<br>A,C,E,G C 0x10128100<br>B,D,F,H C 0x10120100 |
| 8 | 2.Function List<br>2.2Optional function | Revised as below:<br>Error)<br>TEQFP144<br>Analog input port(12bit-ADC)<br>AN4~7, AN10~11, AN14~15, AN19~20, AN22~23, AN25~30, AN33~38, AN48<br><br>Correct)<br>TEQFP144<br>Analog input port(12bit-ADC)<br>AN4~7, AN10~11, AN14~15, AN25~26, AN28~30 |
| 10 | 3.Product Description<br>3.2Product description | Revised 4MHz to 16MHz as below:<br>Error)<br>−A wide range of 3.6 - 4MHz is available for main oscillator<br><br>Correct)<br>−A wide range of 3.6 - 16MHz is available for main oscillator |
| 13 | 3. Product Description<br>3.2Product description | Added Note of a function as below:<br>Multi-Functional Serial (MFS)<br><br>Correct)<br>CTS/RTS is not mounted (hardware flow control is not supported for this series.) |
| 14 | 3. Product Description<br>3.2Product description | Revised Graphics Subsystem clock frequency as below:<br>Error)<br>200 MHz maximum clock frequency<br>Video modes up to 50 MHz pixel clock<br><br>Correct)<br>80 MHz maximum clock frequency<br>Video modes up to 25 MHz pixel clock |

| Page | Section | Change Results |
|---|---|---|
| 81 | 7. Port Configuration 7.1 Resource Input Configuration Module | Revised as below:<br>Error)<br>RIC_RESIN235(0x01D6)<br>OCU1_CK0, OCU1_CK1, OCU1_DOWNB0, OCU1_DOWNB1, OCU1_FCMD0, OCU1_FCMD1,<br>OCU1_MTSF0, OCU1_MTSF1, OCU1_T0[31:0], OCU1_T1[31:0]<br>RIC_RESIN236(0x01D8)<br>OCU1_ZTSF0, OCU1_ZTSF1, OCU1_MOD0<br><br>Correct)<br>RIC_RESIN235(0x01D6)<br>OCU1_CK0, OCU1_CK1, OCU1_DOWNB0, OCU1_DOWNB1, OCU1_FCMD0, OCU1_FCMD1,<br>OCU1_MTSF0, OCU1_MTSF1, OCU1_T0[31:0], OCU1_T1[31:0], OCU1_ZTSF0, OCU1_ZTSF1<br>RIC_RESIN236(0x01D8)<br>OCU1_MOD0 |
| 155 | 8.Precautions and Handling Devices 8.1.1Precautions for Product Design | Revised as below:<br>Error)<br>(1) Preventing Over-Voltage and Over-Current Conditions<br>Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.<br><br>Correct)<br>(1) Preventing Over-Voltage and Over-Current Conditions<br>Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage. |
| 156 | 8.Precautions and Handling Devices 8.1.2Precautions for Package Mounting | Revised as below:<br>Error)<br>Surface Mount Type<br><br>Correct)<br>**Surface Mount Type** |
| 159 | 9.Electric Characteristics 9.1.1 Absolute Maximum Rating | Deleted Remarks comment as below:<br>Error)<br>Supply voltage<br>Operation assurance range, $DV_{CC}$, Remarks “$DV_{CC} \leq V_{CC}5$”<br><br>Correct)<br>Power supply voltage, $DV_{CC}$, Remarks “” |
| 159 | 8.2Handling Devices | Added Note of a function as below:<br>Method to Switch off VCC12 during Power-off Sequence<br>During power-off sequence, it is necessary to switch off VCC12 by driving PSC1 pin low by entering PSS mode (power domain 2 off). If VCC12 needs to be switched off by other means, RSTX needs to be asserted before switching off VCC12 to inactivate the operation of VCC12 supplied domain below the operation assurance range. |

| Page | Section | Change Results |
|---|---|---|
| 159<br>160 | 9.Electric Characteristics<br>9.1.1 Absolute Maximum Rating | Added Note of a comment as below:<br>Maximum clamp current, Total maximum clamp current<br><br>Correct)<br>*13 VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating. |
| 161 | 9.Electric Characteristics<br>9.1.1 Absolute Maximum Rating | Revised Warning of a comment as below:<br>Error)<br>Note:<br>− Application of stress (e.g., voltage, current, temperature) exceeding the absolute maximum rating may cause damage to the semiconductor device. Therefore, make sure that nothing exceeds the rating.<br><br>Correct)<br>WARNING:<br>− Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings. |
| 162 | 9.Electric Characteristics<br>9.1.2Recommended operating condition | Revised Rating Min Spec as below:<br>Error)<br>Power supply voltage, $V_{CC}5$ , Rating, Min, 2.6<br>Power supply voltage, $V_{CC}3$ , Rating, Min, 2.6<br><br>Correct)<br>Power supply voltage, $V_{CC}5$ , Rating, Min, 2.7<br>Power supply voltage, $V_{CC}3$ , Rating, Min, 2.7 |
| 162<br>163 | 9.Electric Characteristics<br>9.1.2Recommended operating condition | Added comment as below:<br>Supply voltage Operation assurance range,VCC12, VCC12<br><br>Correct)<br>*5:When the voltage of Vcc12 is in the out of range against supply voltage operation assurance, the operation of circuit which<br>Vcc12 used as the power source becomes unstable status. In that case, the value of each registers including RESCAUSEUR<br>Register cannot be guaranteed, so these flags should don't care by software processing |
| 162<br>163<br>215<br>236 | 9.Electric Characteristics<br>9.1.2Recommended operating condition<br>9.1.4.11Low Voltage Detection (External Voltage)<br>9.1.5 A/D converter | Revised device revision from B to C as below:<br>Error)<br>S6J33xxxSB , S6J33xxxUB, S6J33xxxTB, S6J33xxxVB,<br>S6J33xxxBB, S6J33xxxDB, S6J33xxxFB, S6J33xxxHB,<br>S6J33xxxAB, S6J33xxxCB, S6J33xxxEB, S6J33xxxGB<br><br>Correct)<br>S6J33xxxSC, S6J33xxxUC, S6J33xxxTC, S6J33xxxVC,<br>S6J33xxxBC, S6J33xxxDC, S6J33xxxFC, S6J33xxxHC,<br>S6J33xxxAC, S6J33xxxCC, S6J33xxxEC, S6J33xxxGC |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>167</td><td>9.Electric Characteristics<br>9.1.3 DC characteristics</td><td>Deleted VOH25 Spec as below:<br>Error)<br>VOH25<br><br>Correct)<br>Non</td></tr>
<tr><td>169</td><td>9.Electric Characteristics<br>9.1.3 DC characteristics</td><td>Deleted VOL25 Spec as below:<br>Error)<br>VOL25<br><br>Correct)<br>Non</td></tr>
<tr><td>175</td><td>9.1 Electrical Characteristics<br>9.1.4 AC characteristics<br>9.1.4.3 Internal clock timing (S6J3310)</td><td>Revised as below:<br>Error)<br>Internal clock frequency, $F_{CLK_HAPP1B0}$, Value, Max *1, 60MHz<br><br>Correct)<br>Internal clock frequency, $F_{CLK_HAPP1B0}$, Value, Max *1, 80MHz</td></tr>
<tr><td>180</td><td>9.Electric Characteristics<br>9.1.4.5 Power-on Conditions</td><td>Revised as below:<br>Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Power off time</td><td>-</td><td>VCC5</td><td>-</td><td>50</td><td>-</td><td>-</td><td>ms</td><td>*2</td></tr>
<tr><td>Power ramp rate</td><td>dV/dt</td><td>VCC5</td><td>VCC5: 0.2V to 2.6V</td><td>-</td><td>-</td><td>1</td><td>V/µs</td><td>*3</td></tr>
<tr><td>Undetected power ramp rate</td><td>|dV/dt|</td><td>VCC5</td><td>VCC5: Between 2.4V and 4.5V</td><td>-</td><td>-</td><td>50</td><td>mV/µs</td><td>*4</td></tr>
</table>
Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Power off time</td><td>-</td><td>VCC5</td><td>-</td><td>100</td><td>-</td><td>-</td><td>µs</td><td>*2</td></tr>
<tr><td>Power ramp rate</td><td>dV/dt</td><td>VCC5</td><td>VCC5: 1.5V to 2.6V</td><td>-</td><td>-</td><td>1</td><td>V/µs</td><td>*3</td></tr>
<tr><td>Maximum ramp rate guaranteed to not generate power-on reset</td><td>|dV/dt|</td><td>VCC5</td><td>VCC5: Between 2.4V and 4.5V</td><td>-</td><td>-</td><td>50</td><td>mV/µs</td><td>*4</td></tr>
</table></td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 180 | 9.Electric Characteristics 9.1.4.5 Power-on Conditions | Revised device revision as below:<br>Error)<br>*1: This specification is at 1V/µs of power ramp rate.<br>*2: VCC5 must be held below 0.2V for a minimum period of tOFF.<br>*3: Power ramp rate must be 1V/us or less from 0.2V to 2.6V.<br>Power-on can detect by satisfying power ramp rate when power off time is satisfied.<br>*4: This specification is specified the power supply fluctuation after power on detection. When VCC5 voltage is between 2.4V and 4.5V, the power supply fluctuation is below 50mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5V and 5.5V.<br><br>***Notes:***<br>When using S6J3310/20/30/40, *2 and *3 must be satisfied. When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power up and any brownout event.<br>• **Power off time, Power ramp rate**<br>  <br><br><br>Correct)<br>*1: This specification is at 1V/µs of power ramp rate.<br>*2: VCC5 must be held below 1.5V for a minimum period of $t_{OFF}$.<br>*3: Power ramp rate must be 1V/us or less from 1.5V to 2.6V.<br>Power-on can detect by satisfying power ramp rate when power off time is satisfied.<br>*4: This specification is specified the power supply fluctuation after power on detection. When VCC5 voltage is between 2.4V and 4.5V, the power supply fluctuation is below 50mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5V and 5.5V.<br>***Notes:***<br>When using S6J3310/20/30/40, *2 and *3 must be satisfied. When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power up and any brownout event.<br>• **Power off time, Power ramp rate**<br>  <br> |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>185<br>186</td><td>9.Electric Characteristics 9.1.4.6Multi-Function Serial</td><td>Deleted Remarks comment as below:<br>(2) Normal synchronous transfer (SCR:SPI=0) and mark level "L" of serial clock output (SMR:SCINV=1)<br>Error)<br>Master Mode(CL=20pF, IOL=-5mA, IOH=5mA)<br>Master Mode(CL=20pF, IOL=-10mA, IOH=10mA)<br>@20MHz, @16MHz, 12.5MHz<br><br>Correct)<br>Non</td></tr>
<tr><td>215</td><td>9.Electric Characteristics 9.1.4.11 Low Voltage Detection (External Voltage)</td><td>Revised Max of Low-voltage detection time as below:<br>Low-voltage detection (external low-voltage detection)<br>Error)<br><table><tr><td>Low-voltage detection time</td><td>Td</td><td>-</td><td>-</td><td>-</td><td>-</td><td>30</td><td>µs</td><td></td></tr></table><br>Correct)<br><table><tr><td>Low-voltage detection time</td><td>Td</td><td>-</td><td>-</td><td>-</td><td>-</td><td>40</td><td>µs</td><td></td></tr></table></td></tr>
<tr><td>216</td><td>9.Electric Characteristics 9.1.4.11 Low Voltage Detection (External Voltage)</td><td>Revised as below:<br>Low-voltage detection (1.15 V power supply low-voltage detection)<br>Error)<br><table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>VCC12</td><td>*1</td><td>0.784<br>0.888</td><td>0.8125<br>0.95</td><td>0.841<br>0.984</td><td>V</td><td>When power-supply voltage falls Typ±3.5%</td></tr></table><br>Correct)<br><table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>VCC12</td><td>*1</td><td>0.7841</td><td>0.8125</td><td>0.8410</td><td>V</td><td>When power-supply voltage falls Typ±3.5%</td></tr></table></td></tr>
<tr><td>217</td><td>9.Electric Characteristics 9.1.4.12Low Voltage Detection (Internal Voltage)</td><td>Revised as below:<br>Low-voltage detection (internal low-voltage detection for LVDL0)<br>Error)<br><table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Hysteresis width</td><td>$V_{RHYS}$</td><td>-</td><td>-</td><td>-</td><td>100</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr></table><br>Correct)<br><table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Hysteresis width</td><td>$V_{RHYS}$</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr></table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>218</td><td>9.Electric Characteristics<br>9.1.4.12 Low Voltage Detection (Internal Voltage)</td><td>
Revised as below:<br>
Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Supply voltage range</td><td>$V_{RDP5}$</td><td>-</td><td>-</td><td>1.05</td><td>-</td><td>1.21</td><td>V</td><td></td></tr>
<tr><td>Detection voltage</td><td>$V_{RDL}$</td><td>-</td><td>*1</td><td>0.75</td><td>0.85</td><td>0.95</td><td>V</td><td>When power-supply voltage falls</td></tr>
<tr><td>Hysteresis width</td><td>$V_{RHYS}$</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr>
<tr><td>Low-voltage detection time</td><td>TRd</td><td>-</td><td>-</td><td>-</td><td>-</td><td>30</td><td>µs</td><td></td></tr>
</table>
*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be canceled after the supply voltage has passed the detection voltage range.<br><br>
Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Supply voltage range</td><td>$V_{RDP5}$</td><td>-</td><td>-</td><td>1.05</td><td>-</td><td>1.21</td><td>V</td><td></td></tr>
<tr><td>Detection voltage</td><td>$V_{RDL}$</td><td>-</td><td>*1</td><td>0.75</td><td>0.85</td><td>0.95</td><td>V</td><td>When power-supply voltage falls *2</td></tr>
<tr><td>Hysteresis width</td><td>$V_{RHYS}$</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr>
<tr><td>Low-voltage detection time</td><td>TRd</td><td>-</td><td>-</td><td>-</td><td>-</td><td>30</td><td>µs</td><td>*3</td></tr>
</table>
*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be canceled after the supply voltage has passed the detection voltage range.<br>
*2: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.<br>
*3: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>218</td><td>9.Electric Characteristics<br>9.1.4.12 Low Voltage Detection (Internal Voltage)</td><td>
Revised as below: Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Supply voltage range</td><td>$V_{RDP5}$</td><td>-</td><td>-</td><td>1.05</td><td>-</td><td>1.21</td><td>V</td><td></td></tr>
<tr><td>Detection voltage (before trimming)</td><td>$V_{RDLBT}$</td><td>-</td><td>*1</td><td>0.775</td><td>0.875</td><td>0.975</td><td>V</td><td>When power-supply voltage falls</td></tr>
<tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>-</td><td>*1</td><td>0.844</td><td>0.875</td><td>0.906</td><td>V</td><td>When power-supply voltage falls Typ±3.5%</td></tr>
<tr><td>Hysteresis width</td><td>$V_{RHYS}$</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr>
<tr><td>Low-voltage detection time</td><td>TRd</td><td>-</td><td>-</td><td>-</td><td>-</td><td>30</td><td>µs</td><td></td></tr>
</table>
*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be canceled after the supply voltage has passed the detection voltage range.<br>
Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Supply voltage range</td><td>$V_{RDP5}$</td><td>-</td><td>-</td><td>1.05</td><td>-</td><td>1.21</td><td>V</td><td></td></tr>
<tr><td>Detection voltage (before trimming)</td><td>$V_{RDLBT}$</td><td>-</td><td>*1</td><td>0.775</td><td>0.875</td><td>0.975</td><td>V</td><td>When power-supply voltage falls *3</td></tr>
<tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>-</td><td>*1</td><td>0.844</td><td>0.875</td><td>0.906</td><td>V</td><td>When power-supply voltage falls Typ±3.5% *2 *3</td></tr>
<tr><td>Hysteresis width</td><td>$V_{RHYS}$</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr>
<tr><td>Low-voltage detection time</td><td>TRd</td><td>-</td><td>-</td><td>-</td><td>-</td><td>30</td><td>µs</td><td>*4</td></tr>
</table>
*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be canceled after the supply voltage has passed the detection voltage range.<br>
*2: This detection voltage level setting is below the minimum operation assurance voltage .<br>
Between this detection voltage and the minimum operation assurance voltage,<br>
MCU functions are not guaranteed except for the low voltage detector.<br>
Note that although the detection level is below the minimum operation guarantee voltage,<br>
the LVD reset factor flag is set as the voltage drops below the detection level.<br>
*3: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.<br>
*4: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.
</td></tr>
</table>

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<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>219</td><td>9.Electric Characteristics<br>9.1.4.14 Display Controller</td><td>Revised as below:<br>Error)<br>(13-1) Display controller0 Timing (TTL mode)<br><br>Correct)<br>(1) Display controller0 Timing (TTL mode)</td></tr>
<tr><td>224</td><td>9.Electric Characteristics<br>9.1.4.16 DDR-HSSPI</td><td>Revised as below:<br>Error)<br>(16-1) DDR-HSSPI Interface Timing (SDR mode)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>HSSPI clock cycle</td><td>$t_{cyc}$</td><td>M_SCLK0</td><td rowspan="8">(CL = 20pF, $I_{OL}$=-10mA, $I_{OH}$=10mA),</td><td>10</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>M_SCLK↑ -> delayed sample clock↑</td><td>$t_{spcnt}$</td><td>-</td><td>0</td><td>tcyc</td><td>ns</td><td></td></tr>
<tr><td>M_SDATA -> delayed sample clock↑ Input setup time</td><td>$t_{isdata}$</td><td>M_SDATA0_0-3<br>M_SDATA1_0-3</td><td>3.5</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>delayed sample clock↑ -> M_SDATA Input hold time</td><td>$t_{ihdata}$</td><td>M_SDATA0_0-3<br>M_SDATA1_0-3</td><td>2.0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>M_SCLK↑ -> M_SDATA Output delay time</td><td>$t_{oddata}$</td><td>M_SDATA0_0-3<br>M_SDATA1_0-3</td><td>-</td><td>6.5</td><td>ns</td><td>$t_{cyc}$ -3.5ns</td></tr>
<tr><td>M_SCLK↑ -> M_SDATA Output hold time</td><td>$t_{ohdata}$</td><td>M_SDATA0_0-3<br>M_SDATA1_0-3</td><td>3.5</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>M_SCLK↑ -> M_SSEL Output delay time</td><td>$t_{odsel}$</td><td>M_SSEL0, 1</td><td>-</td><td>5.5</td><td>ns</td><td>$t_{cyc}$ -4.5ns</td></tr>
<tr><td>M_SCLK↑ -> M_SSEL Output hold time</td><td>$t_{ohsel}$</td><td>M_SSEL0, 1</td><td>4.5</td><td>-</td><td>ns</td><td></td></tr>
</table>
Notes: This is Target Spec.<br><br>Correct)<br>(1)DDR-HSSPI Interface Timing (SDR mode)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td rowspan="2">HSSPI clock cycle</td><td rowspan="2">$t_{cyc}$</td><td rowspan="2">M_SCLK0</td><td rowspan="9">(CL = 20pF, $I_{OL}$=-10mA, $I_{OH}$=10mA),</td><td>10</td><td>-</td><td rowspan="2">ns</td><td></td></tr>
<tr><td>20</td><td>-</td><td>when Quad Page Program</td></tr>
<tr><td>M_SCLK↑ -> delayed sample clock↑</td><td>$t_{spcnt}$</td><td>-</td><td>0</td><td>31.5</td><td>ns</td><td></td></tr>
<tr><td>M_SDATA -> M_SLCK↑ Input setup time</td><td>$t_{isdata}$</td><td>M_SDATA0_0-3<br>M_SDATA1_0-3</td><td>*1</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>M_SCLK↑ -> M_SDATA Input hold time</td><td>$t_{ihdata}$</td><td>M_SDATA0_0-3<br>M_SDATA1_0-3</td><td>*1</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>M_SCLK↑ -> M_SDATA Output delay time</td><td>$t_{oddata}$</td><td>M_SDATA0_0-3<br>M_SDATA1_0-3</td><td>-</td><td>$t_{cyc}$/2 + 2</td><td>ns</td><td></td></tr>
<tr><td>M_SCLK↑ -> M_SDATA Output hold time</td><td>$t_{ohdata}$</td><td>M_SDATA0_0-3<br>M_SDATA1_0-3</td><td>$t_{cyc}$/2 - 3</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>M_SCLK↑ -> M_SSEL Output delay time</td><td>$t_{odsel}$</td><td>M_SSEL0, 1</td><td>-12.00+ (SS2CD+0.5)* $t_{cyc}$</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>M_SCLK↑ -> M_SSEL Output hold time</td><td>$t_{ohsel}$</td><td>M_SSEL0, 1</td><td>$t_{cyc}$ - 2</td><td>-</td><td>ns</td><td></td></tr>
</table>
Notes: This is Target Spec.<br>– SS2CD [1:0] should be configured as 01, 10, or 11.<br>– For *1, the delay of the delay sample clock can be configured (DLP function)..</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 225 | 9.Electric Characteristics 9.1.4.16 DDR-HSSPI | Revised as below:<br>Error)<br>(16-2) DDR-HSSPI Interface Timing (DDR mode) |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| HSSPI clock cycle | $t_{cyc}$ | M_SCLK0 | (CL = 20pF, $I_{OL}$=-10mA, $I_{OH}$=10mA), | 10 | - | ns | |
| M_SCLK↑ -> delayed sample clock↑ | $t_{spcnt}$ | | | 0 | tcyc | ns | |
| M_SDATA -> delayed sample clock↑ Input setup time | $t_{isdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | 1.0 | - | ns | |
| delayed sample clock↑ -> M_SDATA Input hold time | $t_{ihdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | 1.0 | - | ns | |
| M_SCLK↑ -> M_SDATA Output delay time | $t_{oddata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | - | 3.5 | ns | $t_{cyc}$/2-1.5ns |
| M_SCLK↑ -> M_SDATA Output hold time | $t_{ohdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | 1.5 | - | ns | |
| M_SCLK↑ -> M_SSEL Output delay time | $t_{odsel}$ | M_SSEL0, 1 | | - | 7.0 | ns | $t_{cyc}$ -3.0ns |
| M_SCLK↑ -> M_SSEL Output hold time | $t_{ohsel}$ | M_SSEL0, 1 | | 3.0 | - | ns | |

***Notes: This is Target Spec.***

Correct)
(2)DDR-HSSPI Interface Timing (DDR mode)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| HSSPI clock cycle | $t_{cyc}$ | M_SCLK0 | (CL = 20pF, $I_{OL}$=-10mA, $I_{OH}$=10mA), | 12.5 | - | ns | |
| M_SCLK↑ -> delayed sample clock↑ | $t_{spcnt}$ | | | 0 | 31.5 | ns | |
| M_SDATA -> M_SLCK↑ Input setup time | $t_{isdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | *1 | - | ns | |
| M_SLCK↑ -> M_SDATA Input hold time | $t_{ihdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | *1 | - | ns | |
| M_SCLK↑ -> M_SDATA Output delay time | $t_{oddata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | - | $t_{cyc}$/4 + 1.5 | ns | |
| M_SCLK↑ -> M_SDATA Output hold time | $t_{ohdata}$ | M_SDATA0_0-3 M_SDATA1_0-3 | | Tcyc/4 - 1.0 | - | ns | |
| M_SCLK↑ -> M_SSEL Output delay time | $t_{odsel}$ | M_SSEL0, 1 | | -15.75+ (SS2CD+0.5)*$t_{cyc}$ | - | ns | |
| M_SCLK↑ -> M_SSEL Output hold time | $t_{ohsel}$ | M_SSEL0, 1 | | 0.75*$t_{cyc}$ - 2.0 | - | ns | |

***Notes: This is Target Spec.***

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured (DLP function)*

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>227</td><td>9.Electric Characteristics<br>9.1.4.17 Hyper BUS</td><td>
Revised as below:<br>
Error)<br>
(16-1) Hyper Bus Write Timing (HyperFlash)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>CS↑↓ -> CK↑<br>Chip Select setup time</td><td>$t_{CSS}$</td><td>M_CS#_1,2</td><td rowspan="2">(CL = 20pF, IOL=-10mA, IOH=10mA),</td><td>3.0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↓ -> CS↑<br>Chip select hold time</td><td>$t_{CSH}$</td><td>M_CS#_1,2</td><td>0</td><td>-</td><td>ns</td><td></td></tr>
</table>
Correct)<br>
(1)Hyper Bus Write Timing (HyperFlash)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>CS↑↓ -> CK↑<br>Chip Select setup time</td><td>$t_{CSS}$</td><td>M_CS#_1,2</td><td rowspan="2">(CL = 20pF, IOL=-10mA, IOH=10mA),</td><td>$t_{CKCYC}$ -2.0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↓ -> CS↑<br>Chip select hold time</td><td>$t_{CSH}$</td><td>M_CS#_1,2</td><td>$t_{CKCYC}/2$</td><td>-</td><td>ns</td><td></td></tr>
</table>
</td></tr>
<tr><td>228</td><td>9.Electric Characteristics<br>9.1.4.17 Hyper BUS</td><td>
Revised as below:<br>
Error)<br>
(16-2) Hyper Bus Write Timing (HyperRAM)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>CS↑↓ -> CK↑<br>Chip Select setup time</td><td>$t_{CSS}$</td><td>M_CS#_1,2</td><td rowspan="3">(CL = 20pF, $I_{OL}$=-10mA, $I_{OH}$=10mA),</td><td>3.0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↓ -> CS↑<br>Chip select hold time</td><td>$t_{CSH}$</td><td>M_CS#_1,2</td><td>0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>RWDS↓-> CK↓<br>Data Mask Valid</td><td>$t_{DMV}$</td><td>M_RWDS</td><td>0</td><td>-</td><td>ns</td><td></td></tr>
</table>
Correct)<br>
(2) Hyper Bus Write Timing (HyperRAM)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>CS↑↓ -> CK↑<br>Chip Select setup time</td><td>$t_{CSS}$</td><td>M_CS#_1,2</td><td rowspan="3">(CL = 20pF, $I_{OL}$=-10mA, $I_{OH}$=10mA),</td><td>$t_{CKCYC}$ - 2.0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↓ -> CS↑<br>Chip select hold time</td><td>$t_{CSH}$</td><td>M_CS#_1,2</td><td>$t_{CKCYC}/2$</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>RWDS↓-> CK↓<br>Data Mask Valid</td><td>$t_{DMV}$</td><td>M_RWDS</td><td>1</td><td>-</td><td>ns</td><td></td></tr>
</table>
</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 229 | 9.Electric Characteristics 9.1.4.17 Hyper BUS | Revised as below:<br>Error)<br>(16-3) Hyper Bus Read Timing (HyperFlash) |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CS↑↓ -> CK↑<br>Chip Select setup time | $t_{CSS}$ | M_CS#_1,2 | (CL = 20pF, $I_{OL}$=-10mA, $I_{OH}$=10mA), | 3.0 | - | ns | |
| DQ -> CK↑↓<br>Input setup time | $t_{IS}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↑↓ -> DQ<br>Input hold time | $t_{IH}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↓ -> CS↑<br>Chip select hold time | $t_{CSH}$ | M_CS#_1,2 | | 0 | - | ns | |
| RDS↑↓> DQ (valid)<br>RDS transition to DQ valid | $t_{DSS}$ | M_DQ7-0 | | -0.8 | +0.8 | ns | |
| RDS↑↓> DQ (invalid)<br>RDS transition to DQ invalid | $t_{DSH}$ | M_DQ7-0 | | -0.8 | +0.8 | ns | |

Correct)

(3) Hyper Bus Read Timing (HyperFlash)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CS↑↓ -> CK↑<br>Chip Select setup time | $t_{CSS}$ | M_CS#_1,2 | (CL = 20pF, $I_{OL}$=-10mA, $I_{OH}$=10mA), | $t_{RDSCYC}$ -2.0 | - | ns | |
| DQ -> CK↑↓<br>Setup time | $t_{IS}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↑↓ -> DQ<br>Hold time | $t_{IH}$ | M_DQ7-0 | | 1.25 | - | ns | |
| CK↓ -> CS↑<br>Chip select hold time | $t_{CSH}$ | M_CS#_1,2 | | $t_{RDSCYC}$ / 2 | - | ns | |
| RDS↑↓> DQ<br>Setup time | $t_{DSS}$ | M_DQ7-0 | | -0.8 | - | ns | |
| RDS↑↓> DQ<br>Hold time | $t_{DSH}$ | M_DQ7-0 | | -0.8 | - | ns | |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>230</td><td>9.Electric Characteristics<br>9.1.4.17 Hyper BUS</td><td>
Revised as below:<br>
Error)<br>
(16-4) Hyper Bus Read Timing (HyperRAM)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>CS↑↓ -> CK↑<br>Chip Select setup time</td><td>$t_{CSS}$</td><td>M_CS#_1,2</td><td rowspan="8">(CL = 20pF,<br>$I_{OL}$=-10mA,<br>$I_{OH}$=10mA),</td><td>3.0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>DQ -> CK↑↓<br>Input setup time</td><td>$t_{IS}$</td><td>M_DQ7-0</td><td>1.25</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↑↓ -> DQ<br>Input hold time</td><td>$t_{IH}$</td><td>M_DQ7-0</td><td>1.25</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↓ -> CS↑<br>Chip select hold time</td><td>$t_{CSH}$</td><td>M_CS#_1,2</td><td>0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>RWDS↑↓> DQ (valid)<br>RWDS transition to DQ valid</td><td>$t_{DSS}$</td><td>M_DQ7-0</td><td>-0.8</td><td>+0.8</td><td>ns</td><td></td></tr>
<tr><td>RWDS↑↓> DQ (invalid)<br>RWDS transition to DQ invalid</td><td>$t_{DSH}$</td><td>M_DQ7-0</td><td>-0.8</td><td>+0.8</td><td>ns</td><td></td></tr>
<tr><td>CK↑ -> RWDS↑↓<br>Refresh Indicator Valid</td><td>$t_{RIV}$</td><td>M_RWDS</td><td>-</td><td>6</td><td>ns</td><td></td></tr>
<tr><td>CK↑ -> RWDS(Hi-z)<br>Refresh Indicator Hold</td><td>$t_{RIH}$</td><td>M_RWDS</td><td>0</td><td>-</td><td>ns</td><td></td></tr>
</table>
Correct)<br>
(4) Hyper Bus Read Timing (HyperRAM)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>CS↑↓ -> CK↑<br>Chip Select setup time</td><td>$t_{CSS}$</td><td>M_CS#_1,2</td><td rowspan="8">(CL = 20pF,<br>$I_{OL}$=-10mA,<br>$I_{OH}$=10mA),</td><td>$t_{RDSCYC}$ -2.0</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>DQ -> CK↑↓<br>Setup time</td><td>$t_{IS}$</td><td>M_DQ7-0</td><td>1.25</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↑↓ -> DQ<br>Hold time</td><td>$t_{IH}$</td><td>M_DQ7-0</td><td>1.25</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↓ -> CS↑<br>Chip select hold time</td><td>$t_{CSH}$</td><td>M_CS#_1,2</td><td>$t_{RDSCYC}$ /2</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>RWDS↑↓> DQ (valid)<br>Setup time</td><td>$t_{DSS}$</td><td>M_DQ7-0</td><td>-0.8</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>RWDS↑↓> DQ (invalid)<br>Hold time</td><td>$t_{DSH}$</td><td>M_DQ7-0</td><td>-0.8</td><td>-</td><td>ns</td><td></td></tr>
<tr><td>CK↑ -> RWDS↑↓<br>Refresh Indicator Valid</td><td>$t_{RIV}$</td><td>M_RWDS</td><td>-</td><td>6</td><td>ns</td><td></td></tr>
<tr><td>CK↑ -> RWDS(Hi-z)<br>Refresh Indicator Hold</td><td>$t_{RIH}$</td><td>M_RWDS</td><td>0</td><td>-</td><td>ns</td><td></td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>234</td><td>9.Electric Characteristics<br>9.1.4.19 MediaLB</td><td>
Revised as below:<br>
Error)<br>
(19-1) MediaLB Input Timing
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>MLBCLK cycle</td><td>$t_{mckc}$</td><td>MLBCLK</td><td rowspan="2">-</td><td>19.53</td><td>-</td><td>ns</td><td rowspan="2">-</td></tr>
<tr><td>MLBSIG, MLBDAT Input hold</td><td>$t_{dhmcf}$</td><td>MLBSIG MLBDAT</td><td>0</td><td>-</td><td>ns</td></tr>
</table>
Notes: This is Target Spec.<br>
(19-2) MediaLB Output Timing
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>MLBCLK cycle</td><td>$t_{mckc}$</td><td>MLBCLK</td><td rowspan="3">(CL = 20pF, $I_{OL}$=-6mA, $I_{OH}$=6mA),</td><td>19.53</td><td>-</td><td>ns</td><td>-</td></tr>
<tr><td>MLBSIG, MLBDAT output stop</td><td>$t_{mcfdz}$</td><td>MLBSIG MLBDAT</td><td>10.73</td><td>-</td><td>ns</td><td>$t_{mckc}$ -8.8ns</td></tr>
<tr><td>MLBSIG, MLBDAT output delay</td><td>$t_{dout}$</td><td>MLBSIG MLBDAT</td><td>0</td><td>8.8</td><td>ns</td><td>-</td></tr>
</table>
Notes: This is Target Spec.<br><br>
Correct)<br>
(1) MediaLB Input Timing
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>MLBCLK cycle</td><td>$t_{mckc}$</td><td>MLBCLK</td><td rowspan="2">-</td><td>40.0</td><td>-</td><td>ns</td><td rowspan="2">-</td></tr>
<tr><td>MLBSIG, MLBDAT Input hold</td><td>$t_{dhmcf}$</td><td>MLBSIG MLBDAT</td><td>4.0</td><td>-</td><td>ns</td></tr>
</table>
Notes: This is Target Spec.<br>
– CLK_HAPP1B0(internal) frequency > MLBCLK(external) frequency<br>
(2) MediaLB Output Timing
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>MLBCLK cycle</td><td>$t_{mckc}$</td><td>MLBCLK</td><td rowspan="3">(CL = 20pF, $I_{OL}$=-6mA, $I_{OH}$=6mA),</td><td>40.0</td><td>-</td><td>ns</td><td>-</td></tr>
<tr><td>MLBSIG, MLBDAT output stop</td><td>$t_{mcfdz}$</td><td>MLBSIG MLBDAT</td><td>26.5</td><td>-</td><td>ns</td><td>$t_{mckc}$ - $t_{dout}$</td></tr>
<tr><td>MLBSIG, MLBDAT output delay</td><td>$t_{dout}$</td><td>MLBSIG MLBDAT</td><td>0</td><td>13.5</td><td>ns</td><td>-</td></tr>
</table>
Notes: This is Target Spec.<br>
– CLK_HAPP1B0(internal) frequency > MLBCLK(external) frequency
</td></tr>
<tr><td>246</td><td>11.Ordering Information</td><td>
Revised part number as below:<br>
Error)<br>
S6J331EKCB*******<br>
S6J331EKBB*******<br>
S6J331EKAB*******<br>
S6J331EJCB*******<br>
S6J332EJCB*******<br>
S6J331EJAB*******<br>
S6J332EJAB*******<br>
S6J332EHSB*******<br><br>
Correct)<br>
S6J331EKCC*******<br>
S6J331EKBC*******<br>
S6J331EKAC*******<br>
S6J331EJCC*******<br>
S6J332EJCC*******<br>
S6J331EJAC*******<br>
S6J332EJAC*******<br>
S6J332EHSC*******
</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| Rev. *B | | |
| 13 | 3.Product Description<br>3.2.Product description | Revised the below:<br>Error)<br>(None)<br>12bit resolution, 2 unit<br>48 channels of analog input for TEQFP208<br>48 channels of analog input for TEQFP176<br>35 channel of analog input for TEQFP144<br>24 channels of them are shared with the SMC for TEQFP208/176/144<br>External trigger and timer trigger are available.<br>The description of the A/D converter function should be referred in the S6J3300 hardware manual. Though the chapter of I/O port in Traveo™ Platform hardware manual describes another A/D converter function, do not refer it.<br><br>Correct)<br>12bit resolution, 2 unit(Unit0 is possible to select channels 4-31. Unit1 is possible to select channels 32-63.)<br>48 channels of analog input for TEQFP208<br>48 channels of analog input for TEQFP176<br>35 channel of analog input for TEQFP144<br>24 channels of them are shared with the SMC for TEQFP208/176/144<br>External trigger and timer trigger are available.<br>The description of the A/D converter function should be referred in the S6J3300 hardware manual. Though the chapter of I/O port in Traveo™ Platform hardware manual describes another A/D converter function, do not refer it.<br>A/D Channel Control Register (ADC12Bn_CHCTRL0)[bit5:0] ANIN[5:0] : Analog Input Selection bits.<br>This register setting is possible of channel 0-31 (the register value is 00_0000 to 01_1111). |
| 15 | 3.Product Description<br>3.2.Product description | Revised as below:<br>Correct)<br>Power Supply Control (PSC): PSC (PSC_1) output is used for external 1.2V power supply module control and automatically switched with the following condition.<br>"High": Request to supply VCC12<br>- "Power ON Reset" is released<br>- CPU wakes up from PSS shutdown mode<br>"Low": Request to stop supplying VCC12<br>- CPU transfers from RUN mode to PSS shutdown mode.<br><br>For timing chart of output signals include PSC in detail, see the "S6J3300 hardware manual" and chapter "State Transition" |
| 22<br>23 | 4.Package and Pin Assignment<br>4.2.Package Dimensions | Revised as below:<br>4.2.3.TEQFP144<br>Error)<br>Figure 4 6: TEQFP144<br>Figure 4 7: TEQFP144<br>The package dimension of TEQFP144 (0.4mm Pitch) is the provisional version.<br><br>Correct)<br>Figure 4 6: TEQFP144 (0.5mm Pitch)<br>Figure 4 7: TEQFP144 (0.4mm Pitch)<br>The package dimension of TEQFP144 (0.4mm Pitch) is the formal version. |
| 31<br>32 | 6.Port Description<br>6.1 Port Description list | Revised the below:<br>Error)<br>ADC Analog [4 to18, 21, 24 to 26, 28 to 32, 39 to 47, 49 to 63] input pin<br><br>Correct)<br>ADC Unit0 [ch.4 to ch.18, ch.21, ch.24 to ch.26, ch.28 to ch.31] input pin<br>ADC Unit1 [ch.32, ch.39 to ch.47, ch.49 to ch.63] input pin |

| Page | Section | Change Results |
|---|---|---|
| 155 | 8.Precautions and Handling Devices<br>8.1.1.Precautions for Product Design | Revised the below:<br>Error)<br>(1) Preventing Over-Voltage and Over-Current Conditions<br>Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.<br><br>Correct)<br>(1) Preventing Over-Voltage and Over-Current Conditions<br>Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage. |
| 159 | 8.Precautions and Handling Devices<br>8.2.Handling Devices | Revised as below:<br><br>Correct)<br>**Method to Switch Off VCC12 during Power-Off Sequence**<br>During power-off sequence, it is necessary to switch off VCC12 by driving PSC1 pin low by entering PSS mode (power domain 2 off). If VCC12 needs to be switched off by other means, RSTX needs to be asserted before switching off VCC12 to inactivate the operation of VCC12 supplied domain below the operation assurance range. |
| 164 | 9.Electric Characteristics<br>9.1.2 Recommended operating condition | Revised as below:<br>Error)<br>The detection/release threshold values of following LVD channels are potentially below supply range defined in 9.1.2 Recommended operating condition (refer to "9.1.4.11 Low Voltage Detection (External Voltage)" and "9.1.4.12 Low Voltage Detection (Internal Voltage)" for detection/release threshold values for these LVD channels):<br>LVDL0<br>LVDL1<br>LVDL2<br>LVDH0<br>LVDH1<br>LVDH2<br><br>Correct)<br>The detection/release threshold values of following LVD channels are potentially below supply range defined in 9.1.2 Recommended operating condition (refer to "9.1.4.11 Low Voltage Detection (External Voltage)" and "9.1.4.12 Low Voltage Detection (Internal Voltage)" for detection/release threshold values for these LVD channels):<br>LVDL0<br>LVDL1<br>LVDL2<br>LVDH0<br>LVDH1<br>LVDH2<br>Detection voltage of the external low voltage detection reset (initial) is 2.6V±3.5%*2 *3 or 4.0V±3.5%*1.<br>This detection voltage level setting is below the minimum operation assurance voltage (2.7V*2 *3 or 4.0V*1) .<br>Between this detection voltage and the minimum operation assurance voltage,<br>MCU functions are not guaranteed except for the low voltage detector.<br>Note that although the detection level is below the minimum operation guarantee voltage,<br>the LVD reset factor flag is set as the voltage drops below the detection level. |

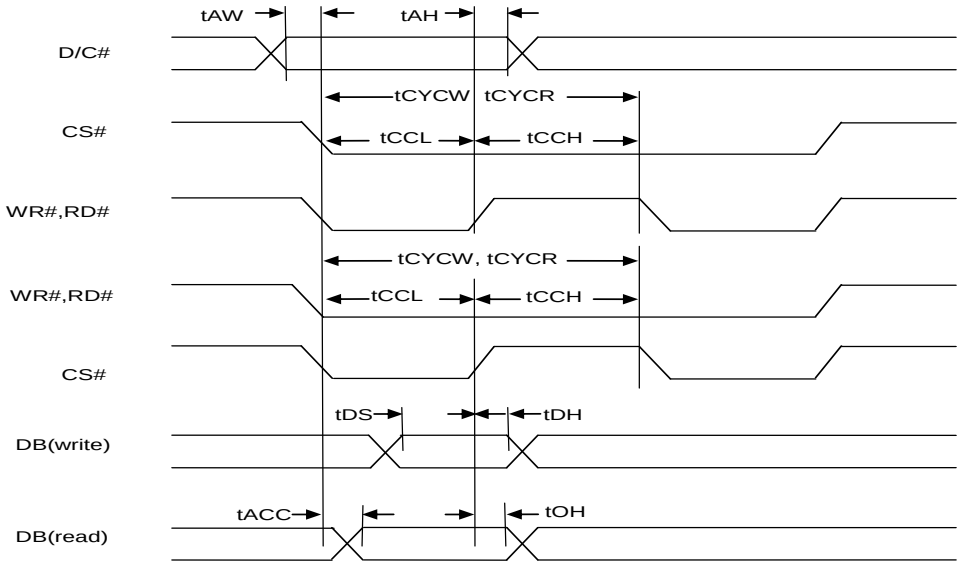
<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>174</td><td>9.Electric Characteristics<br>9.1.4.1.Source clock timing</td><td>Revised as below:<br>Error)<br>Notes:<br>− The maximum/minimum values have been standardized with the main clock and PLL clock in use.<br>− Jitter of source oscillator must be smaller than 300ppm.<br><br>Correct)<br>Notes:<br>− The maximum/minimum values have been standardized with the main clock and PLL clock in use.<br>− Jitter of source oscillator must be smaller than 300ppm.<br>− Enough evaluation and adjustment are recommended using oscillator on your system board.</td></tr>
<tr><td>177</td><td>9.Electric Characteristics<br>9.1.4.3.Internal clock timing</td><td>Revised as below:<br>Error)<br>- Note that Ta=125 condition is not supported in this product type.<br><br>When using SSCG_PLL output for these internal clock, the MAX value of frequency has the following restrictions.<br>- On the presumption that the modulation mode of SSCG_PLL is used with down spread,<br>the MAX value of the frequency is standardized.<br>- This means that MAX value of frequency is the maximum value when SSCG_PLL was modulated.<br><br>Correct)<br>- Note that Ta=125 condition is not supported in this product type.<br><br>When using SSCG_PLL output for these internal clock, the MAX value of frequency has the following restrictions.<br>- On the presumption that the modulation mode of SSCG_PLL is used with down spread,<br>the MAX value of the frequency is standardized.<br>- This means that MAX value of frequency is the maximum value when SSCG_PLL was modulated.<br>- "Unused" means a clock source which doesn't have any supply destinations. Configure it as disable with performing at the lower clock frequency than the described maximum.</td></tr>
<tr><td>179</td><td>9.Electric Characteristics<br>9.1.4.3.internal clock timing</td><td>Added Oscillation clock frequency as below:<br><br>Correct)<br>
<table>
<tr><th colspan="2" rowspan="3"></th><th colspan="8">Internal Operation Clock Frequency</th></tr>
<tr><th rowspan="2">Main Clock</th><th colspan="7">PLL Clock</th></tr>
<tr><th>Multiplied by 1</th><th>Multiplied by 2</th><th></th><th>Multiplied by 15</th><th>Multiplied by 30</th><th>Multiplied by 40</th><th>Multiplied by 60</th></tr>
<tr><td rowspan="3">Oscillation clock frequency [MHz]</td><td>4</td><td>2</td><td>4</td><td>8</td><td>…</td><td>60</td><td>120</td><td>160</td><td>240</td></tr>
<tr><td>8</td><td>4</td><td>8</td><td>16</td><td>…</td><td>120</td><td>240</td><td></td><td></td></tr>
<tr><td>16</td><td>8</td><td>16</td><td>32</td><td>…</td><td>240</td><td></td><td></td><td></td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>208</td><td>9.Electric Characteristics 9.1.4.6Multi-Function Serial</td><td>
Revised as below:<br>
Error)<br>
I²C timing (SMR:MD2-0=0b100)<br>
($T_A$: Recommended operating conditions, Vcc5=Vcc53=5.0 V ±10%, $V_{CC}$12=1.15V ±0.06V, $V_{SS}$=0.0 V)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Standard Mode</th><th colspan="2">High-Speed Mode</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th><th>Min</th><th>Max</th></tr>
<tr><td>SCL clock frequency</td><td>$f_{SCL}$</td><td>SCL0, SCL1, SCL4, SCL8 to SCL12, SCL16 to SCL17</td><td>$C_L$=50pF, R=(Vp/$I_{OL}$)*1</td><td>0</td><td>100</td><td>0</td><td>400</td><td>kHz</td><td></td></tr>
</table>
Correct)<br>
I²C timing (SMR:MD2-0=0b100)<br>
($T_A$: Recommended operating conditions, Vcc5=Vcc53=5.0 V ±10%, $V_{CC}$12=1.15V ±0.06V, $V_{SS}$=0.0 V)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Standard Mode</th><th colspan="2">Fast Mode</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th><th>Min</th><th>Max</th></tr>
<tr><td>SCL clock frequency</td><td>$f_{SCL}$</td><td>SCL0, SCL1, SCL4, SCL8 to SCL12, SCL16 to SCL17</td><td>$C_L$=50pF, R=(Vp/$I_{OL}$)*1</td><td>0</td><td>100</td><td>0</td><td>400</td><td>kHz</td><td></td></tr>
</table>
Error)<br>
*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "$t_{SUDAT}$ ≥ 250 ns".<br><br>
Correct)<br>
*3: A fast mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "$t_{SUDAT}$ ≥ 250 ns".
</td></tr>
<tr><td>216</td><td>9.Electric Characteristics 9.1.4.11.Low Voltage Detection (External Voltage)</td><td>
Added *5 and *5 sentences as below:<br><br>
Error)
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Pin Name</th><th>Conditions</th><th colspan="3">Value</th><th>Unit</th><th>Remarks</th></tr>
<tr><th></th><th></th><th></th><th></th><th>Min</th><th>Typ</th><th>Max</th><th></th><th></th></tr>
<tr><td rowspan="3">Detection voltage (after trimming)</td><td rowspan="3">$V_{DLAT}$</td><td rowspan="2">VCC5</td><td rowspan="2">*1</td><td>3.86 *3</td><td>4.0 *3</td><td>4.14 *3</td><td rowspan="2">V</td><td rowspan="3">When power-supply voltage falls and detection level is set initially Typ±3.5%</td></tr>
<tr><td>2.51 *4</td><td>2.6 *4</td><td>2.69 *4</td></tr>
<tr><td>VCC3</td><td>*1</td><td>2.51</td><td>2.6</td><td>2.69</td><td>V</td></tr>
</table>
Correct)
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Pin Name</th><th>Conditions</th><th colspan="3">Value</th><th>Unit</th><th>Remarks</th></tr>
<tr><th></th><th></th><th></th><th></th><th>Min</th><th>Typ</th><th>Max</th><th></th><th></th></tr>
<tr><td rowspan="3">Detection voltage (after trimming)</td><td rowspan="3">$V_{DLAT}$</td><td rowspan="2">VCC5</td><td rowspan="2">*1</td><td>3.86 *3</td><td>4.0 *3</td><td>4.14 *3</td><td rowspan="2">V</td><td rowspan="3">When power-supply voltage falls and detection level is set initially Typ±3.5% *5</td></tr>
<tr><td>2.51 *4</td><td>2.6 *4</td><td>2.69 *4</td></tr>
<tr><td>VCC3</td><td>*1</td><td>2.51</td><td>2.6</td><td>2.69</td><td>V</td></tr>
</table>
*5: This detection voltage level setting is below the minimum operation assurance voltage (2.7V*4 or 4.0V*3) .<br>
Between this detection voltage and the minimum operation assurance voltage,<br>
MCU functions are not guaranteed except for the low voltage detector.<br>
Note that although the detection level is below the minimum operation guarantee voltage,<br>
the LVD reset factor flag is set as the voltage drops below the detection level.
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>217</td><td>9.Electric Characteristics<br>9.1.4.11.Low Voltage Detection (External Voltage)</td><td>
Added *2 and *2 sentences as below:<br><br>
Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>VCC12</td><td>*1</td><td>0.7841</td><td>0.8125</td><td>0.8410</td><td>V</td><td>When power-supply voltage falls Typ±3.5%</td></tr>
</table>
Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>VCC12</td><td>*1</td><td>0.7841</td><td>0.8125</td><td>0.8410</td><td>V</td><td>When power-supply voltage falls Typ±3.5% *2</td></tr>
</table>
*2: This detection voltage level setting is below the minimum operation assurance voltage .<br>
Between this detection voltage and the minimum operation assurance voltage,<br>
MCU functions are not guaranteed except for the low voltage detector.<br>
Note that although the detection level is below the minimum operation guarantee voltage,<br>
the LVD reset factor flag is set as the voltage drops below the detection level.
</td></tr>
<tr><td>218</td><td>9.Electric Characteristics<br>9.1.4.12.Low Voltage Detection (Internal Voltage)</td><td>
Added *2 and *2 sentences as below:<br><br>
Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>-</td><td>*1</td><td>0.844</td><td>0.875</td><td>0.906</td><td>V</td><td>When power-supply voltage falls Typ±3.5%</td></tr>
</table>
Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>-</td><td>*1</td><td>0.844</td><td>0.875</td><td>0.906</td><td>V</td><td>When power-supply voltage falls Typ±3.5% *2</td></tr>
</table>
*2: This detection voltage level setting is below the minimum operation assurance voltage .<br>
Between this detection voltage and the minimum operation assurance voltage,<br>
MCU functions are not guaranteed except for the low voltage detector.<br>
Note that although the detection level is below the minimum operation guarantee voltage,<br>
the LVD reset factor flag is set as the voltage drops below the detection level.
</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 238<br>239<br>240<br>241 | 9.Electric<br>Characteristics<br>9.1.4.21<br>LCDCbus I/F | Added AC specification of LCD bus I/F as below.<br><br>Correct)<br>***9.1.4.21 LCDbus I/F***<br><br>**(1) Intel-8080**<br>(TA: Recommended operating conditions, Vcc3=3.3 V ±0.3V, VSS=DVSS=AVSS=0.0 V) |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Address hold time | tAH | D/C# | (CL = 20pF, $I_{OL}$=-5mA, $I_{OH}$=5mA), | 20 | - | ns | |
| Address setup time | tAW | D/C# | | 20 | - | ns | |
| Write cycle time | tCYCW | CS#, WR# | | 100 | - | ns | |
| Write, Enable pulse H width | tCCHW | CS#, WR# | | 35 | - | ns | |
| Write, Enable pulse L width | tCCLW | CS#, WR# | | 35 | - | ns | |
| Write data set time | tDS | DB | | 20 | - | ns | |
| Write data hold time | tDH | DB | | 20 | - | ns | |
| Read cycle time | tCYCR | CS#, RD# | | 255 | - | ns | |
| Read pulse H width | tCCHR | CS#, RD# | | 90 | - | ns | |
| Read pulse L width | tCCLR | CS#, RD# | | 150 | - | ns | |
| Read data access time | tACC | DB | | - | 145 | ns | |
| Read data disable time | tOH | DB | | 15 | - | ns | |

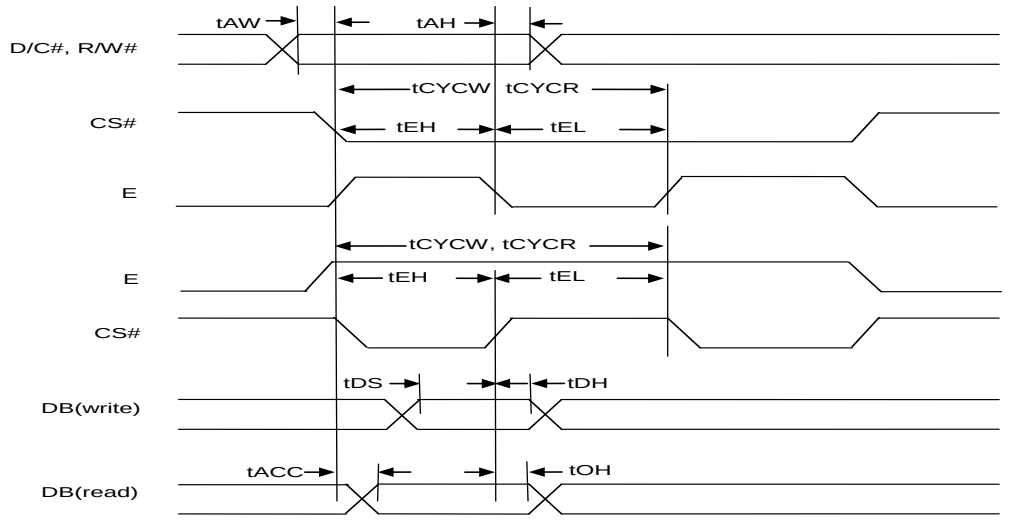


| Page | Section | Change Results |
|---|---|---|

**(2) Motorola-6800**

(TA: Recommended operating conditions, Vcc3=3.3 V ±0.3V, VSS=DVSS=AVSS=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Address hold time | tAH | D/C#, R/W# | (CL = 20pF, $I_{OL}$=-5mA, $I_{OH}$=5mA), | 20 | - | ns | |
| Address setup time | tAW | D/C#, R/W# | | 20 | - | ns | |
| Write cycle time | tCYCW | CS#, E | | 100 | - | ns | |
| Write, Enable pulse H width | tEH | CS#, E | | 35 | - | ns | |
| Write, Enable pulse H widthtEH | CS#, E | | 35 | - | ns | | |
| Write, Enable pulse L width | tEL | CS#,E | | 35 | - | ns | |
| Write data set time | tDS | DB | | 20 | - | ns | |
| Write data hold time | tDH | DB | | 20 | - | ns | |
| Read cycle time | tCYCR | CS#, E | | 255 | - | ns | |
| Read pulse H width | tEH | CS#, E | | 90 | - | ns | |
| Read pulse L width | tEL | CS#,E | | 150 | - | ns | |
| Read data access time | tACC | DB | | - | 145 | ns | |
| Read data disable time | tOH | DB | | 15 | - | ns | |



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<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td colspan="3">Rev. *C</td></tr>
<tr><td>1</td><td>Features</td><td>Error)<br>□ General purpose I/O port : up to 146<br>Correct)<br>□ General purpose I/O port : up to 148</td></tr>
<tr><td>4</td><td>1.Overview<br>1.2 Document definition</td><td>Error)
<table>
<tr><th>Document Type</th><th>Definition</th><th>Primary User</th><th>Document Code</th></tr>
<tr><td>S6J3310/20/30/40 Datasheet</td><td>The function and its characteristics are specified quantitatively.</td><td>Investigator and hardware engineer</td><td>002-10635</td></tr>
<tr><td>S6J3300 hardware manual</td><td>The function and its operation of S6J3300 series are described.</td><td>Software engineer</td><td>002-10185</td></tr>
<tr><td>Traveo™ Platform hardware manual</td><td>The function and its operation of CPU core platform are described.</td><td>Software engineer</td><td>002-07884</td></tr>
<tr><td>Application note</td><td>The reference software, sample application, the reference board design and so on are explained.</td><td>Software and hardware engineer</td><td>Under consideration</td></tr>
</table>
Correct)
<table>
<tr><th>Document Type</th><th>Definition</th><th>Primary User</th><th>Document Code</th></tr>
<tr><td>S6J3310/20/30/40 Datasheet</td><td>The function and its characteristics are specified quantitatively.</td><td>Investigator and hardware engineer</td><td>002-10635</td></tr>
<tr><td>S6J3300 hardware manual</td><td>The function and its operation of S6J3300 series are described.</td><td>Software engineer</td><td>002-10185</td></tr>
<tr><td>Traveo™ Platform hardware manual</td><td>The function and its operation of CPU core platform are described.</td><td>Software engineer</td><td>002-07884</td></tr>
<tr><td>Application note</td><td>The reference software, sample application, the reference board design and so on are explained.</td><td>Software and hardware engineer</td><td>002-03898<br>002-04455<br>002-04446<br>002-09716<br>002-04452<br>002-04096<br>002-12061<br>002-02495</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>5<br>6</td><td>2.Function List<br>2.1 Product lineup</td><td>
Error)
<table>
<tr><th>Function</th><th>S6J3310</th><th>S6J3320</th><th>S6J3330</th><th>S6J3340</th><th>Remark</th></tr>
<tr><td>Sound waveform generator</td><td colspan="4">1 unit x 5 outputs</td><td>See 2.2.1</td></tr>
<tr><td>I2S</td><td colspan="4">2 ch</td><td>One only supports an output as a function of the sound system.</td></tr>
</table>
Correct)
<table>
<tr><th>Function</th><th>S6J3310</th><th>S6J3320</th><th>S6J3330</th><th>S6J3340</th><th>Remark</th></tr>
<tr><td>Sound waveform generator</td><td colspan="2">1 unit x 5 outputs</td><td colspan="2">No</td><td>See 2.2.1</td></tr>
<tr><td>I2S</td><td colspan="2">2 ch</td><td colspan="2">1ch</td><td>One only supports an output as a function of the sound system.</td></tr>
</table>
</td></tr>
<tr><td>5<br>6</td><td>2.Function List<br>2.1 Product lineup</td><td>
Error)
<table>
<tr><th>Function</th><th>S6J3310</th><th>S6J3320</th><th>S6J3330</th><th>S6J3340</th><th>Remark</th></tr>
<tr><td>General Purpose I/O</td><td colspan="4">Option</td><td>See 2.2.2</td></tr>
<tr><td>12bit-A/D converter</td><td colspan="4">2 unit - 48 input ports (Max)</td><td>See 2.2.2</td></tr>
<tr><td>LCD controller</td><td colspan="4">4COM x 32 SEG (Max)</td><td>See 2.2.2</td></tr>
</table>
Correct)
<table>
<tr><th>Function</th><th>S6J3310</th><th>S6J3320</th><th>S6J3330</th><th>S6J3340</th><th>Remark</th></tr>
<tr><td>General Purpose I/O</td><td colspan="4">Option</td><td>See 2.2.3</td></tr>
<tr><td>12bit-A/D converter</td><td colspan="4">2 unit - 48 input ports (Max)</td><td>See 2.2.3</td></tr>
<tr><td>LCD controller</td><td colspan="4">4COM x 32 SEG (Max)</td><td>See 2.2.3</td></tr>
</table>
</td></tr>
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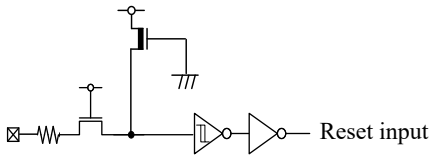
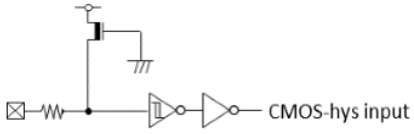
<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>8</td><td>2.Function List<br>2.2.2 ID</td><td>Error)
<table>
<tr><td>Function Digit</td><td>Revision</td><td>Chip ID</td><td>JTAG ID</td></tr>
<tr><td>S,U,T,V</td><td>C</td><td>0x10122100</td><td>0x1000B5CF</td></tr>
<tr><td>A,C,E,G</td><td>C</td><td>0x10128100</td><td>0x1000B5CF</td></tr>
<tr><td>B,D,F,H</td><td>C</td><td>0x10120100</td><td>0x1000B5CF</td></tr>
</table>
Correct)
<table>
<tr><td>Function Digit</td><td>Revision</td><td>Chip ID</td><td>JTAG ID</td></tr>
<tr><td rowspan="2">S,U,T,V</td><td>C</td><td>0x10122100</td><td rowspan="6">0x1000B5CF</td></tr>
<tr><td>D</td><td>0x10122200</td></tr>
<tr><td rowspan="2">A,C,E,G</td><td>C</td><td>0x10128100</td></tr>
<tr><td>D</td><td>0x10128200</td></tr>
<tr><td rowspan="2">B,D,F,H</td><td>C</td><td>0x10120100</td></tr>
<tr><td>D</td><td>0x10120200</td></tr>
</table></td></tr>
<tr><td>10</td><td>3.Product Description<br>3.2 Product description</td><td>Error)<br>Power Domain (PD)<br>The product series supports the power off control of PD1, PD2 (including PD3 and 5) and PD6.<br><br>Correct)<br>Power Domain (PD)<br>The product series supports the power off control of PD1, PD2 (including PD3 and 5), PD4_0, PD4_1 and PD6.</td></tr>
<tr><td>17<br>18<br>19<br>20</td><td>4.Package and Pin Assignment<br>4.1.1 TEQFP-208 Pin Assignment</td><td>Error)<br>4.1.1 TEQFP-208 Pin Assignment(S6J3310)<br>Figure 4 1: TEQFP-208<br>Correct)<br>4.1.1 TEQFP-208 Pin Assignment<br>Figure 4-1: TEQFP-208 (S6J331xKyz)<br>Figure 4-2: TEQFP-208 (S6J332xKyz) add<br>Figure 4-3: TEQFP-208 (S6J333xKyz) add<br>Figure 4-4: TEQFP-208 (S6J334xKyz) add</td></tr>
<tr><td>21<br>22<br>23<br>24</td><td>4. Package and Pin Assignment<br>4.1.2 TEQFP-176 Pin Assignment</td><td>Error)<br>4.1.2 TEQFP-176 Pin Assignment(S6J3310)<br>Figure 4-2: TEQFP-176<br>Correct)<br>4.1.2 TEQFP-176 Pin Assignment<br>Figure 4-5: TEQFP-176 (S6J331xJyz)<br>Figure 4-6: TEQFP-176 (S6J332xJyz) add<br>Figure 4-7: TEQFP-176 (S6J333xJyz) add<br>Figure 4-8: TEQFP-176 (S6J334xJyz) add</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 25<br>26<br>27<br>28 | 4.Package and Pin Assignment<br>4.1.3 TEQFP-144 Pin Assignment | Error)<br>4.1.3 TEQFP-144 Pin Assignment(S6J3310)<br>Figure 4-2: TEQFP-144<br>Correct)<br>4.1.3 TEQFP-144 Pin Assignment<br>Figure 4-9: TEQFP-144 (S6J331xHyz)<br>Figure 4-10: TEQFP-144 (S6J332xHyz) add<br>Figure 4-11: TEQFP-144 (S6J333xHyz) add<br>Figure 4-12: TEQFP-144 (S6J334xHyz) add |
| 29 | 4.Package and Pin Assignment<br>4.2.1 TEQFP208 | Error)<br>-<br>Correct)<br>Revised PKG figure.<br>Added PKG Code. |
| 30 | 4.Package and Pin Assignment<br>4.2.2 TEQFP176 | Error)<br>-<br>Correct)<br>Revised PKG figure.<br>Added PKG Code. |
| 31<br>32 | 4.Package and Pin Assignment<br>4.2.3 TEQFP144 | Error)<br>-<br>Correct)<br>Revised PKG figure.<br>Added PKG Code. |
| 35 | 5.IO Circuit Type<br>5.1. I/O Circuit Type | Error)<br>Type N<br>  <br><br>Correct)<br>Type N<br>  <br> |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>170</td><td>9. Electric Characteristics 9.1.1 Absolute Maximum Ratin<sub>g</sub></td><td>
Error)
<table>
<tr><td>Power consumption</td><td>$P_D$</td><td>-</td><td>1500</td><td>mW</td><td></td></tr>
<tr><td rowspan="2">Operating temperature</td><td rowspan="2">$T_A$</td><td>-40</td><td>105</td><td>°C</td><td>$P_D$≤2000mW</td></tr>
<tr><td>-40</td><td>125</td><td>°C</td><td>$P_D$≤1200mW</td></tr>
</table>
Correct)
<table>
<tr><td rowspan="2">Power consumption</td><td rowspan="2">$P_D$</td><td>-</td><td>2000</td><td>mW</td><td>-40°C≤$T_A$≤105°C</td></tr>
<tr><td>-</td><td>1100</td><td>mW</td><td>-40°C≤$T_A$≤125°C</td></tr>
<tr><td rowspan="2">Operating temperature</td><td rowspan="2">$T_A$</td><td>-40</td><td>105</td><td>°C</td><td>$P_D$≤2000mW</td></tr>
<tr><td>-40</td><td>125</td><td>°C</td><td>$P_D$≤1100mW</td></tr>
</table>
</td></tr>
<tr><td>172</td><td>9. Electric Characteristics 9.1.2 Recommended operating condition</td><td>
Error)
<table>
<tr><td rowspan="2">Operating temperature</td><td>TA</td><td>-</td><td>-40</td><td>105</td><td>°C</td><td>PD≤2000mW</td></tr>
<tr><td>TA</td><td>-</td><td>-40</td><td>125</td><td>°C</td><td>PD≤1200mW</td></tr>
</table>
Correct)
<table>
<tr><td rowspan="2">Operating temperature</td><td>$T_A$</td><td>-</td><td>-40</td><td>105</td><td>°C</td><td>$P_D$≤2000mW</td></tr>
<tr><td>$T_A$</td><td>-</td><td>-40</td><td>125</td><td>°C</td><td>$P_D$≤1100mW</td></tr>
</table>
</td></tr>
<tr><td>172</td><td>9.Electric Characteristics 9.1.2Recommended operating condition</td><td>
Error)<br>
S6J33xxxSC, S6J33xxxUC, S6J33xxxTC, S6J33xxxVC,<br>
S6J33xxxBC, S6J33xxxDC, S6J33xxxFC, S6J33xxxHC,<br>
S6J33xxxAC, S6J33xxxCC, S6J33xxxEC, S6J33xxxGC<br>
Correct)<br>
S6J33xxxSx, S6J33xxxUx, S6J33xxxTx, S6J33xxxVx,<br>
S6J33xxxBx, S6J33xxxDx, S6J33xxxFx, S6J33xxxHx,<br>
S6J33xxxAx, S6J33xxxCx, S6J33xxxEx, S6J33xxxGx
</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 173 | 9. Electric Characteristics 9.1.2 Recommended operating condition | Error)<br>LVDL0<br>LVDL1<br>LVDL2<br>LVDH0<br>LVDH1<br>LVDH2<br>Detection voltage of the external low voltage detection reset (initial) is 2.6V±3.5%*2 *3 or 4.0V±3.5%*1.<br>This detection voltage level setting is below the minimum operation assurance voltage (2.7V*2 *3 or 4.0V*1) .<br>Between this detection voltage and the minimum operation assurance voltage,<br>MCU functions are not guaranteed except for the low voltage detector.<br>Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.<br><br>Correct)<br>LVDL0<br>LVDL1<br>LVDL2<br>LVDH0<br>LVDH1<br>LVDH2<br>When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative.The initial detection voltage of the external low voltage detection is 2.6V±3.5%*2 *3(LVDH1/LVDH2) or 0.8V±3.5%(LVDL2).<br>This LVD setting and internal LVD (LVDL0/LVDL1) cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation<br>voltage. |

| Page | Section | Change Results |
|---|---|---|
| 181<br>182 | 9. Electric Characteristics<br>9.1.3 DC characteristics | Error) |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{CCT5}$ | VCC5 | Timer mode | - | 370 | 810 | µA | $T_A$=25°C. Power only supplies to Backup RAM and system controllers. When using 4MHz crystal for main oscillator. |
| | | | - | 360 | 780 | µA | $T_A$=25°C. Power only supplies to Backup RAM and system controllers. When shutting down 16kB Backup RAM and using 4MHz crystal for main oscillator. |
| $I_{CCH5}$ | | Stop mode | - | 100 | 400 | µA | $T_A$=25°C. Power only supplies to Backup RAM and system controllers. |

Correct)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{CCT5}$ | VCC5 | Timer mode | - | 370 | 810 | µA | $T_A$=25°C. 4MHz crystal for main oscillator<br>PD1=ON, PD4_0=ON, PD4_1=ON |
| | | | - | 360 | 780 | µA | $T_A$=25°C. 4MHz crystal for main oscillator.<br>PD1=ON, PD4_0=ON or PD4_1=ON |
| | | | - | 350 | 750 | µA | $T_A$=25°C. 4MHz crystal for main oscillator.<br>PD1=ON |
| | | | - | 450 | 890 | µA | $T_A$=25°C. 8MHz crystal for main oscillator<br>PD1=ON, PD4_0=ON, PD4_1=ON |
| | | | - | 440 | 860 | µA | $T_A$=25°C. 8MHz crystal for main oscillator.<br>PD1=ON, PD4_0=ON or PD4_1=ON |
| | | | - | 430 | 830 | µA | $T_A$=25°C. 8MHz crystal for main oscillator.<br>PD1=ON |
| | | | - | 110 | 430 | µA | $T_A$=25°C. 32kHz crystal for sub oscillator<br>PD1=ON, PD4_0=ON, PD4_1=ON |
| | | | - | 100 | 400 | µA | $T_A$=25°C. 32kHz crystal for sub oscillator.<br>PD1=ON, PD4_0=ON or PD4_1=ON |
| | | | - | 90 | 370 | µA | $T_A$=25°C. 32kHz crystal for sub oscillator.<br>PD1=ON |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{CCH5}$ | VCC5 | Stop mode | - | 100 | 400 | µA | $T_A$=25°C.<br>PD1=ON, PD4_0=ON, PD4_1=ON |
| | | | - | 90 | 370 | µA | $T_A$=25°C.<br>PD1=ON, PD4_0=ON or PD4_1=ON |
| | | | - | 80 | 340 | µA | $T_A$=25°C.<br>PD1=ON |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>191</td><td>9. Electric Characteristics<br>9.1.4.5 Power-on Conditions</td><td>Error)<br><table><tr><td>Power off time</td><td></td><td>VCC5</td><td>-</td><td>100</td><td>-</td><td>-</td><td>µs</td><td>*2</td></tr></table><br>Correct)<br><table><tr><td>Power off time</td><td>$t_{OFF}$</td><td>VCC5</td><td>-</td><td>100</td><td>-</td><td>-</td><td>µs</td><td>*2</td></tr></table></td></tr>
<tr><td>226<br>253</td><td>9.Electric Characteristics<br>9.1.4.11Low Voltage Detection (External Voltage)<br>9.1.5 A/D converter</td><td>Error)<br>S6J33xxxSC, S6J33xxxUC, S6J33xxxTC, S6J33xxxVC,<br>S6J33xxxAC, S6J33xxxBC, S6J33xxxCC, S6J33xxxDC,<br>S6J33xxxEC, S6J33xxxFC, S6J33xxxGC, S6J33xxxHC<br>Correct)<br>S6J33xxxSx, S6J33xxxUx, S6J33xxxTx, S6J33xxxVx,<br>S6J33xxxAx, S6J33xxxBx, S6J33xxxCx, S6J33xxxDx,<br>S6J33xxxGx, S6J33xxxFx, S6J33xxxGx, S6J33xxxHx</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 226 | 9. Electric Characteristics 9.1.4.11 Low Voltage Detection (External Voltage) | Low-voltage detection (external low-voltage detection)<br>Error) |

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply voltage range | $V_{DP5}$ | VCC5 | - | 3.5 *3 | - | 5.5 *3 | V | |
| | | | | 2.7 *4 | - | 3.6 *4 | | |
| Detection voltage (before trimming) | $V_{DLBT}$ | VCC5 | *1 | 3.6 *3 | 4.0 *3 | 4.4 *3 | V | When power-supply voltage falls and detection level is set initially |
| | | | | 2.3 *4 | 2.6 *4 | 2.9 *4 | | |
| | | VCC3 | *1 | 2.3 | 2. 6 | 2.9 | V | |
| Detection voltage (after trimming) | $V_{DLAT}$ | VCC5 | *1 | 3.86 *3 | 4.0 *3 | 4.14 *3 | V | When power-supply voltage falls and detection level is set initially Typ±3.5% *5 |
| | | | | 2.51 *4 | 2.6 *4 | 2.69 *4 | | |
| | | VCC3 | *1 | 2.51 | 2.6 | 2.69 | V | |

*5: This detection voltage level setting is below the minimum operation assurance voltage (2.7V*4 or 4.0V*3) .Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector.
Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.

Correct)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply voltage range | $V_{DP5}$ | VCC5 | - | 3.5 *3 | - | 5.5 *3 | V | |
| | | | | 2.7 *4 | - | 3.6 *4 | | |
| | $V_{DP3}$ | VCC3 | - | 2.7 | - | 3.6 | V | |
| Detection voltage (before trimming) | $V_{DLBT}$ | VCC5 | *1 | 3.6 *3 | 4.0 *3 | 4.4 *3 | V | When power-supply voltage falls and detection level is set initially |
| | | | *1 *5 | 2.3 *4 | 2.6 *4 | 2.9 *4 | | |
| | | VCC3 | *1 *5 | 2.3 | 2. 6 | 2.9 | V | |
| Detection voltage (after trimming) | $V_{DLAT}$ | VCC5 | *1 | 3.86 *3 | 4.0 *3 | 4.14 *3 | V | When power-supply voltage falls and detection level is set initially Typ±3.5% |
| | | | *1 *5 | 2.51 *4 | 2.6 *4 | 2.69 *4 | | |
| | | VCC3 | *1 *5 | 2.51 | 2.6 | 2.69 | V | |

*5: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage(2.7V).

| Page | Section | Change Results |
|---|---|---|
| 227 | 9. Electric Characteristics 9.1.4.11 Low Voltage Detection (External Voltage) | Low-voltage detection (1.15 V power supply low-voltage detection)<br>Error) |

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply voltage range | $V_{RDP12}$ | VCC12 | - | 1.09 | - | 1.21 | V | |
| Detection voltage (before trimming) | $V_{RDLBT}$ | VCC12 | *1 | 0.7125 | 0.8125 | 0.9125 | V | When power-supply voltage falls |
| Detection voltage (after trimming) | $V_{RDLAT}$ | VCC12 | *1 | 0.7841 | 0.8125 | 0.841 | V | When power-supply voltage falls Typ±3.5% *2 |

*2: This detection voltage level setting is below the minimum operation assurance voltage . Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.

Correct)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply voltage range | $V_{RDP12}$ | VCC12 | - | 1.09 | - | 1.21 | V | |
| Detection voltage (before trimming) | $V_{RDLBT}$ | VCC12 | *1 *2 | 0.7125 | 0.8125 | 0.9125 | V | When power-supply voltage falls |
| Detection voltage (after trimming) | $V_{RDLAT}$ | VCC12 | *1 *2 | 0.7841 | 0.8125 | 0.841 | V | When power-supply voltage falls Typ±3.5% |

*2: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (1.09V).

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>228</td><td>9. Electric Characteristics<br>9.1.4.12 Low Voltage Detection (Internal Voltage)</td><td>Low-voltage detection (internal low-voltage detection for LVDL1) Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Supply voltage range</td><td>$V_{RDP5}$</td><td>-</td><td>-</td><td>1.05</td><td>-</td><td>1.21</td><td>V</td><td></td></tr>
<tr><td>Detection voltage</td><td>$V_{RDLBT}$</td><td>-</td><td>*1</td><td>0.775</td><td>0.875</td><td>0.975</td><td>V</td><td>When power-supply voltage falls *3</td></tr>
<tr><td>Detection voltage</td><td>$V_{RDLAT}$</td><td>-</td><td>*1</td><td>0.844</td><td>0.875</td><td>0.906</td><td>V</td><td>When power-supply voltage falls Typ±3.5% *2 *3</td></tr>
<tr><td>Hysteresis width</td><td>$V_{RHYS}$</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr>
<tr><td>Low-voltage detection time</td><td>TRd</td><td>-</td><td>-</td><td>-</td><td>-</td><td>30</td><td>µs</td><td>*4</td></tr>
</table>
*2: This detection voltage level setting is below the minimum operation assurance voltage .<br>Between this detection voltage and the minimum operation assurance voltage,<br>MCU functions are not guaranteed except for the low voltage detector.<br>Note that although the detection level is below the minimum operation guarantee voltage,<br>the LVD reset factor flag is set as the voltage drops below the detection level.<br>*3: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.<br>*4: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td></td><td></td><td>Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Supply voltage range</td><td>$V_{RDP5}$</td><td>-</td><td>-</td><td>1.05</td><td>-</td><td>1.21</td><td>V</td><td></td></tr>
<tr><td>Detection voltage (before trimming)</td><td>$V_{RDLBT}$</td><td>-</td><td>*1 *2</td><td>0.775</td><td>0.875</td><td>0.975</td><td>V</td><td>When power-supply voltage falls</td></tr>
<tr><td>Detection voltage (after trimming)</td><td>$V_{RDLAT}$</td><td>-</td><td>*1 *2</td><td>0.844</td><td>0.875</td><td>0.906</td><td>V</td><td>When power-supply voltage falls<br>Typ±3.5%</td></tr>
<tr><td>Hysteresis width</td><td>$V_{RHYS}$</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr>
<tr><td>Low-voltage detection time</td><td>TRd</td><td>-</td><td>-</td><td>-</td><td>-</td><td>30</td><td>µs</td><td>*3</td></tr>
</table>
*2: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.<br>*3: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.</td></tr>
<tr><td>248</td><td>9. Electric Characteristics<br>9.1.4.21 LCD bus I/F</td><td>Error)<br>-<br>Correct)<br>All change</td></tr>
<tr><td>249<br>250<br>251<br>252</td><td>9. Electric Characteristics<br>9.1.4.22 Power and Reset Sequence</td><td>Error)<br>-<br>Correct)<br>Newly added</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>263</td><td>11. Ordering Information</td><td>Error)
<table>
<tr><th>Part Number</th><th>Package</th></tr>
<tr><td>S6J331EKCC*******</td><td>208-pin plastic TEQFP (TEQFP208)</td></tr>
<tr><td>S6J331EKBC*******</td><td>208-pin plastic TEQFP (TEQFP208)</td></tr>
<tr><td>S6J331EKAC*******</td><td>208-pin plastic TEQFP (TEQFP208)</td></tr>
<tr><td>S6J331EJCC*******</td><td>176-pin plastic TEQFP (TEQFP176)</td></tr>
<tr><td>S6J332EJCC*******</td><td>176-pin plastic TEQFP (TEQFP176)</td></tr>
<tr><td>S6J331EJAC*******</td><td>176-pin plastic TEQFP (TEQFP176)</td></tr>
<tr><td>S6J332EJAC*******</td><td>176-pin plastic TEQFP (TEQFP176)</td></tr>
<tr><td>S6J332EHSC*******</td><td>144-pin plastic TEQFP (TEQFP144)</td></tr>
<tr><td>S6J332EHSC*******</td><td>144-pin plastic TEQFP (TEQFP144)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td></td><td></td><td>Correct)
<table>
<tr><th>Part Number *1</th><th>Package</th></tr>
<tr><td>S6J331EKEx*******</td><td>208-pin plastic TEQFP<br>(LEW208)</td></tr>
<tr><td>S6J332CKSx*******</td><td>208-pin plastic TEQFP<br>(LEW208)</td></tr>
<tr><td>S6J334CKSx*******</td><td>208-pin plastic TEQFP<br>(LEW208)</td></tr>
<tr><td>S6J331EJAx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J332CJBx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J332CJTx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J332EJBx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334BJDx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334CJEx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334CJTx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334DJEx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334DJTx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334EJAx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334EJEx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334EJTx*******</td><td>176-pin plastic TEQFP<br>(LEW176)</td></tr>
<tr><td>S6J334CHBx*******</td><td>144-pin plastic TEQFP<br>(LEX144, LEK144)</td></tr>
</table>
*1: x is selected from the following parameter.<br>x : C, D (Revision)</td></tr>
<tr><td colspan="3">Rev. *E</td></tr>
<tr><td>6</td><td>2. Function List<br>2.1 Function list</td><td>Revised the below:<br><br>CAN-FD RAM (ECC supported)<br>Error)<br>16KB/ch<br>It equivalents to 128 message buffer per channel of CCAN module<br><br>Correct)<br>16KB/ch<br>It equivalents to 128 message buffer per channel of MCAN module</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>12</td><td>3. Product Description<br>3.2 Product description</td><td>Error)<br><table><tr><td>Power Supply</td><td>3V external power supply should be controlled by GPIO.</td></tr></table>Correct)<br><table><tr><td>Power Supply</td><td>3V external power supply could be controlled by GPIO.</td></tr></table></td></tr>
<tr><td>61</td><td>7. Port configuration<br>7.1 Resource Input Configuration Module</td><td>Error)<br>-<br>Correct)<br>The Resource which are available through only one port does not have the multiplexer implemented i.e. No RIC_RESIN register.</td></tr>
<tr><td>169</td><td>9. Electric Characteristics<br>9.1.1 Absolute Maximum Rating</td><td>Error)<br><table><tr><td>Power supply voltage*1, *2</td><td>$V_{CC}12$</td><td>$V_{SS}$-0.3</td><td>$V_{SS}$+1.8</td><td>V</td><td>$V_{CC}12 \leq V_{CC}53$<br>$V_{CC}12 \leq V_{CC}3$<br>$V_{CC}12 \leq DV_{CC}$<br>$V_{CC}12 \leq AV_{CC}5$</td></tr></table>Correct)<br><table><tr><td>Power supply voltage*1, *2</td><td>$V_{CC}12$</td><td>$V_{SS}$-0.3</td><td>$V_{SS}$+1.8</td><td>V</td><td>$V_{CC}12 \leq AV_{CC}5$</td></tr></table></td></tr>
<tr><td>169</td><td>9. Electric Characteristics<br>9.1.1 Absolute Maximum Rating</td><td>Error)<br><table><tr><td>Total maximum clamp current</td><td>$\Sigma\lvert I_{CLAMP}\rvert$</td><td>-</td><td>50</td><td>mA</td><td>SPECIAL SPEC*A</td></tr></table>Correct)<br><table><tr><td>Total maximum clamp current</td><td>$\Sigma\lvert I_{CLAMP}\rvert$</td><td>-</td><td>90</td><td>mA</td><td>*B</td></tr><tr><td>Total maximum clamp current</td><td>$\Sigma\lvert I_{CLAMP}\rvert$</td><td>-</td><td>65</td><td>mA</td><td>*C</td></tr></table></td></tr>
<tr><td>170</td><td>9. Electric Characteristics<br>9.1.1 Absolute Maximum Rating</td><td>Error)<br>-<br>Correct)<br><table><tr><td rowspan="4">System Thermal Resistance</td><td>Theta j-a1</td><td>-</td><td>17</td><td>°C/W</td><td>TEQFP 208</td><td rowspan="4">The minimum value depends on the system specification of heat radiation. The described value is estimated under the condition which is specified at “9.1.2 Recommended Operating Conditions”.</td></tr><tr><td>Theta j-a2</td><td>-</td><td>19</td><td>°C/W</td><td>TEQFP 176</td></tr><tr><td>Theta j-a3</td><td>-</td><td>20</td><td>°C/W</td><td>TEQFP 144 (0.5mm Pitch)</td></tr><tr><td>Theta j-a4</td><td>-</td><td>22</td><td>°C/W</td><td>TEQFP 144 (0.4mm Pitch)</td></tr><tr><td rowspan="4">Package Thermal Resistance</td><td>Psi j-t1</td><td>-</td><td>0.6</td><td>°C/W</td><td colspan="2">TEQFP208</td></tr><tr><td>Psi j-t2</td><td>-</td><td>1.0</td><td>°C/W</td><td colspan="2">TEQFP176</td></tr><tr><td>Psi j-t3</td><td>-</td><td>2.0</td><td>°C/W</td><td colspan="2">TEQFP144 (0.5mm Pitch)</td></tr><tr><td>Psi j-t4</td><td>-</td><td>2.0</td><td>°C/W</td><td colspan="2">TEQFP144 (0.4mm Pitch)</td></tr></table></td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 172<br>173<br>174 | 9. Electric Characteristics<br>9. 1 Electric Characteristics | Error)<br>-<br>Correct)<br>Newly added<br>*B Relevant pins: All general-purpose ports and analog input pins<br>*C Relevant pins: All general-purpose ports and analog input pins |
| 176 | 9. Electric Characteristics<br>9.1.2 Recommended operating condition | Error)<br>− In the case of use in VCC5 = AVCC5 = DVCC of conditions, please launch the power supply in the following sequence.<br>Required power supply sequence is the following:<br>VCC5 -> [DVCC or VCC53 or AVCC5 or VCC3 or AVCC3_DAC] -> VCC12<br>Note that power supplies inside "[ ]" can be turned on in arbitrary order.<br>Corresponding Part number is S6J33xxxSC or S6J33xxxUC or S6J33xxxTC or S6J33xxxVC or S6J33xxxBC or S6J33xxxDC or S6J33xxxFC or S6J33xxxHC.<br>− In the case of use in VCC5 = AVCC5 < DVCC of conditions, please launch the power supply in the following sequence.<br>Required power supply sequence is the following:<br>VCC5 -> DVCC -> [VCC53 or AVCC5 or VCC3 or AVCC3_DAC] -> VCC12.<br>Note that power supplies inside "[ ]" can be turned on in arbitrary order.<br>Corresponding Part number is S6J33xxxAC or S6J33xxxCC or S6J33xxxEC or S6J33xxxGC.<br><br>Correct)<br>- Required power supply sequence is the following:<br>{VCC5 -> AVCC5} -> [DVCC, VCC12, VCC3, AVCC3_DAC]<br>Note that power supplies inside "[ ]" can be turned on in arbitrary order and "{ }" can be turned on in shown sequence or simultaneously. |

| Page | Section | Change Results |
|---|---|---|
| 177 | 9. Electric Characteristics 9.1.2 Recommended operating condition | Error)<br>-<br>Correct)<br>Note:<br>−TA: Ambient temperature (JEDEC)<br>−TC: Case temperature (JEDEC), the maximum measured temperature of package case top.<br>−Both rating of TA and TC should simultaneously be satisfied as maximum operation temperature.<br>−The following condition should be satisfied in order to facilitate heat dissipation.<br>1. Four or more layers PCB should be used.<br>2. The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)<br>3. One layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.<br>4. 35% or more of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.<br>5. The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.<br>Example thermal via holes on PCB<br><Figure><br><br>− The above figure is a schematic diagram showing PCB in section.<br>− Thermal via holes should closely be placed and aligned with lands.<br>− It is recommended to connect the land pattern to the VSS-ground level (GND plan of inner layer bellow the MCU) as thermal heat sink. |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>185</td><td>9. Electric Characteristics<br>9.1.3 DC characteristics</td><td>
Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="3">Power supply current</td><td rowspan="2">$I_{CC12}$</td><td rowspan="3">VCC 12</td><td>Normal operation</td><td>-</td><td>500</td><td>1000</td><td>mA</td><td>$T_A$=-40 ~ 105°C<br>CPU:240MHz,<br>HPM:120MHz<br>(CPU:200MHz,<br>HPM:200MHz)<br>GDC : 200MHz</td></tr>
<tr><td>Flash write/erase</td><td>-</td><td>550</td><td>1050</td><td>mA</td><td>$T_A$=-40 ~ 105°C<br>CPU:240MHz,<br>HPM:120MHz<br>(CPU:200MHz,<br>HPM:200MHz)<br>GDC : 200MHz</td></tr>
<tr><td>$I_{CCH12}$</td><td>Timer/ Stop Mode</td><td>-</td><td>-</td><td>650</td><td>mA</td><td></td></tr>
</table>
Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="4">Power supply current</td><td rowspan="3">$I_{CC12}$</td><td rowspan="4">VCC 12</td><td rowspan="2">Normal operation</td><td>-</td><td>320</td><td>800</td><td>mA</td><td>$T_A$=-40 ~ 105°C<br>CPU:240MHz,<br>HPM:120MHz<br>(CPU:200MHz,<br>HPM:200MHz)<br>GDC : 200MHz</td></tr>
<tr><td>-</td><td>-</td><td>395</td><td>mA</td><td>Example use case *1<br>$T_A$=-40 ~ 105°C<br>CPU:60MHz,<br>HPM:60MHz<br>GDC : 60MHz</td></tr>
<tr><td>Flash write/erase</td><td>-</td><td>350</td><td>850</td><td>mA</td><td>$T_A$=-40 ~ 105°C<br>CPU:240MHz,<br>HPM:120MHz<br>(CPU:200MHz,<br>HPM:200MHz)<br>GDC : 200MHz</td></tr>
<tr><td>$I_{CCH12}$</td><td>Timer/ Stop Mode</td><td>-</td><td>-</td><td>430</td><td>mA</td><td></td></tr>
</table>
</td></tr>
<tr><td>186</td><td>9. Electric Characteristics<br>9.1.3 DC characteristics</td><td>
Error)<br>-<br>Correct)<br>*1 : Example use case at following condition<br>CPU:60MHz, HPM:60MHz, GDC : 60MHz<br>Peripherals:<br>- DMAC active (WorkFlash => SystemRAM)<br>- All timers active<br>- 6 SMCs, 1 CAN, 2LIN, 1SPI, PWMs, ADCs<br>Display controller:<br>- 2 (= all) layers active (60 MHz, noise RGBA, 32 bpp, 2048 x 5 pixels)<br>- Any other resources inactive<br>- IOs no toggle
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>254<br>255<br>256</td><td>9. Electric Characteristics<br>9.1.4.22 Power and Reset Sequence</td><td>Error)<br>-<br>Correct)<br>Newly added<br>Case-1, Case2-1 and Case2-2</td></tr>
<tr><td>266</td><td>9. Electric Characteristics<br>9.1.7.1 Electrical Characteristics</td><td>Error)
<table>
<tr><th rowspan="2">Parameter</th><th colspan="3">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max*3</th></tr>
<tr><td rowspan="3">Sector erase time</td><td>-</td><td>120</td><td>480</td><td>ms</td><td>Large sector*1<br>Internal preprogramming time included</td></tr>
<tr><td>-</td><td>120</td><td>480</td><td>ms</td><td>8kB sector*1<br>Internal preprogramming time included</td></tr>
<tr><td>-</td><td>120</td><td>480</td><td>ms</td><td>4kB sector*1<br>Internal preprogramming time included</td></tr>
<tr><td>16bit write time(Program)</td><td>-</td><td>30</td><td>384</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>32bit write time(Program)</td><td>-</td><td>30</td><td>384</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>64bit write time(Program)</td><td>-</td><td>30</td><td>384</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>256bit write time(Program)</td><td>-</td><td>40</td><td>512</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>Page mode write time(Program)</td><td>-</td><td>320</td><td>4096</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>32bit write time(Work)</td><td>-</td><td>30</td><td>384</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
</table>
Correct)
<table>
<tr><th rowspan="2">Parameter</th><th colspan="3">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max*3</th></tr>
<tr><td rowspan="3">Sector erase time</td><td>-</td><td>120</td><td>180</td><td>ms</td><td>Large sector*1<br>Internal preprogramming time included</td></tr>
<tr><td>-</td><td>120</td><td>180</td><td>ms</td><td>8kB sector*1<br>Internal preprogramming time included</td></tr>
<tr><td>-</td><td>120</td><td>180</td><td>ms</td><td>4kB sector*1<br>Internal preprogramming time included</td></tr>
<tr><td>16bit write time(Program)</td><td>-</td><td>30</td><td>60</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>32bit write time(Program)</td><td>-</td><td>30</td><td>60</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>64bit write time(Program)</td><td>-</td><td>30</td><td>60</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>256bit write time(Program)</td><td>-</td><td>40</td><td>70</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>Page mode write time(Program)</td><td>-</td><td>320</td><td>600</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
<tr><td>32bit write time(Work)</td><td>-</td><td>30</td><td>60</td><td>µs</td><td>System-level overhead time excluded*1</td></tr>
</table></td></tr>
</table>

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<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>270</td><td>12. Appendix<br>12.1<br>Application 1:<br>JTAG tool<br>connection</td><td>Error)<br>-<br>Correct)<br>Newly added this section</td></tr>
<tr><td colspan="3">Rev. *F</td></tr>
<tr><td>4</td><td>1. Overview<br>1.2 Document<br>Definition</td><td>Error)<br>Table 1-1<br><br>Correct)<br>Table 1-1: Document Definition</td></tr>
<tr><td>5</td><td>2. Function List<br>2.1 Function<br>List</td><td>Error)<br>Table 2-1<br><br>Correct)<br>Table 2-1: Function Lineup</td></tr>
<tr><td>7</td><td>2. Function List<br>2.2.1 Basic<br>option</td><td>Error)<br>Figure 2-1<br><br>Correct)<br>Figure 2-1: Option and Part Number for S6J3310/20/30/40 Series</td></tr>
<tr><td>7</td><td>2. Function List<br>2.2.1 Basic<br>option</td><td>Error)<br>Revision: Revision version<br><br>Correct)<br>Revision:<br><table><tr><th>Digit</th><th>Description</th></tr><tr><td>C</td><td>Fixed Operation frequency of embedded Program Flash and CPU,<br>Fixed Stabilization time for sub oscillator</td></tr><tr><td>D</td><td>Fixed TCFLASH Sector Write Permission and Data Retention after Reset</td></tr><tr><td>E</td><td>Leakage current improvement</td></tr></table></td></tr>
<tr><td>8</td><td>2. Function List<br>2.2.3<br>Restriction</td><td>Error)<br>Table 2-2<br><br>Correct)<br>Table 2-2: Pin Restriction</td></tr>
<tr><td>10</td><td>3. Product<br>Description<br>3.2 Product<br>Description</td><td>Error)<br>Table 3-1<br><br>Correct)<br>Table 3-1: Product Features</td></tr>
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| Page | Section | Change Results |
|---|---|---|
| 17 | 4. Package | Error) |
| 18 | and Pin | z : C, D (Revision) |
| 19 | Assignment | |
| 20 | 4.1 Pin | Correct) |
| 21 | Assignment | z : C, D, E (Revision) |
| 22 | | |
| 23 | | |
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| 28 | | |

| Page | Section | Change Results |
|---|---|---|
| 185 | 9. Electric Characteristics 9.1.3 DC characteristics | |

Error)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CC12}$ | VCC12 | Normal operation | - | 320 | 800 | mA | $T_A$=-40 ~ 105°C CPU:240MHz, HPM:120MHz (CPU:200MHz, HPM:200MHz) GDC : 200MHz |
| | | | | - | - | 395 | mA | Example use case *1 $T_A$=-40 ~ 105°C CPU:60MHz, HPM:60MHz GDC : 60MHz |
| | | | Flash write/erase | - | 350 | 850 | mA | $T_A$=-40 ~ 105°C CPU:240MHz, HPM:120MHz (CPU:200MHz, HPM:200MHz) GDC : 200MHz |
| | $I_{CCH12}$ | | Timer/ Stop Mode | - | - | 430 | mA | |
| | $I_{CC5}$ | VCC5 | Normal operation | - | 45 | 85 | mA | |
| | | | Flash write/erase | - | - | 100 | mA | |

Correct)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CC12}$ | VCC12 | Normal operation | - | 315 | 775 | mA | $T_A$=-40 ~ 105 °C CPU: 240 MHz, HPM: 120 MHz (CPU: 200 MHz, HPM: 200 MHz) GDC: 200 MHz |
| | | | | - | - | 395 | mA | Example use case *1 $T_A$=-40 ~ 105 °C CPU:60 MHz, HPM:60 MHz GDC : 60 MHz |
| | | | Flash write/erase | - | 320 | 780 | mA | $T_A$=-40 ~ 105°C CPU: 240 MHz, HPM: 120 MHz (CPU: 200 MHz, HPM: 200 MHz) GDC : 200 MHz |
| | $I_{CCH12}$ | | Timer/ Stop Mode | - | - | 420 | mA | |
| | $I_{CC5}$ | VCC5 | Normal operation | - | 25 | 45 | mA | |
| | | | Flash write/erase | - | - | 60 | mA | |

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<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>187</td><td>9. Electric Characteristics<br>9.1.3 DC characteristics</td><td>Error)<br>-<br><br>Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="11">Power supply current *</td><td rowspan="9">$I_{CCT5}$</td><td rowspan="12">VCC5</td><td rowspan="9">Timer mode</td><td>-</td><td>345</td><td>630</td><td>µA</td><td>$T_A$=25 °C. 4 MHz crystal for main oscillator PD1=ON, PD4_0=ON, PD4_1=ON</td></tr>
<tr><td>-</td><td>340</td><td>625</td><td>µA</td><td>$T_A$=25 °C. 4 MHz crystal for main oscillator. PD1=ON, PD4_0=ON or PD4_1=ON</td></tr>
<tr><td>-</td><td>335</td><td>620</td><td>µA</td><td>$T_A$=25°C. 4 MHz crystal for main oscillator. PD1=ON</td></tr>
<tr><td>-</td><td>420</td><td>705</td><td>µA</td><td>$T_A$=25 °C. 8 MHz crystal for main oscillator PD1=ON, PD4_0=ON, PD4_1=ON</td></tr>
<tr><td>-</td><td>415</td><td>700</td><td>µA</td><td>$T_A$=25 °C. 8 MHz crystal for main oscillator. PD1=ON, PD4_0=ON or PD4_1=ON</td></tr>
<tr><td>-</td><td>410</td><td>695</td><td>µA</td><td>$T_A$=25 °C. 8 MHz crystal for main oscillator. PD1=ON</td></tr>
<tr><td>-</td><td>80</td><td>135</td><td>µA</td><td>$T_A$=25 °C. 32 kHz crystal for sub oscillator PD1=ON, PD4_0=ON, PD4_1=ON</td></tr>
<tr><td>-</td><td>75</td><td>130</td><td>µA</td><td>$T_A$=25 °C. 32 kHz crystal for sub oscillator. PD1=ON, PD4_0=ON or PD4_1=ON</td></tr>
<tr><td>-</td><td>70</td><td>125</td><td>µA</td><td>$T_A$=25 °C. 32 kHz crystal for sub oscillator. PD1=ON</td></tr>
<tr><td rowspan="3">$I_{CCH5}$</td><td rowspan="3">Stop mode</td><td>-</td><td>75</td><td>130</td><td>µA</td><td>$T_A$=25 °C. PD1=ON, PD4_0=ON, PD4_1=ON</td></tr>
<tr><td>-</td><td>70</td><td>125</td><td>µA</td><td>$T_A$=25 °C. PD1=ON, PD4_0=ON or PD4_1=ON</td></tr>
<tr><td>-</td><td>65</td><td>120</td><td>µA</td><td>$T_A$=25 °C. PD1=ON</td></tr>
</table>
* Electric Characteristics for S6J33xxxxE.</td></tr>
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<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>264<br>265</td><td>9. Electric Characteristics<br>9.1.6 Audio DAC</td><td>Error)<br>Figure 9-1<br>Figure 9-2<br>Figure 9-3<br><br>Correct)<br>Figure 9-1: Connection between $R_L$ and AVCC_DAC/2 (Example)<br>Figure 9-2: Startup Time<br>Figure 9-3: Coupling Capacitance (Example)</td></tr>
<tr><td>270</td><td>11. Ordering Information</td><td>Error)<br>x : C,D (Revision)<br><br>Correct)<br>x : C,D, E (Revision)</td></tr>
<tr><td colspan="3">Rev. *G</td></tr>
<tr><td>6</td><td>2. Function List<br>2.1. Function List</td><td>Function: CRC<br>Error)<br>1 unit<br><br>Correct)<br>4 units</td></tr>
<tr><td>6</td><td>2. Function List<br>2.1. Function List</td><td>Function: DDR HSSPI<br>Error)<br>2 ch<br><br>Correct)<br>1 ch</td></tr>
<tr><td>8</td><td>2. Function List<br>2.2.2 ID</td><td>Error)
<table>
<tr><th>Function Digit</th><th>Revision</th><th>Chip ID</th><th>JTAG ID</th></tr>
<tr><td>S,U,T,V</td><td>C</td><td>0x10122100</td><td>0x1000B5CF</td></tr>
<tr><td></td><td>D</td><td>0x10122200</td><td></td></tr>
<tr><td>A,C,E,G</td><td>C</td><td>0x10128100</td><td></td></tr>
<tr><td></td><td>D</td><td>0x10128200</td><td></td></tr>
<tr><td>B,D,F,H</td><td>C</td><td>0x10120100</td><td></td></tr>
<tr><td></td><td>D</td><td>0x10120200</td><td></td></tr>
</table>
Correct)
<table>
<tr><th>Function Digit</th><th>Revision</th><th>Chip ID</th><th>JTAG ID</th></tr>
<tr><td>S,U,T,V</td><td>C</td><td>0x10122100</td><td>0x1000B5CF</td></tr>
<tr><td></td><td>D, E</td><td>0x10122200</td><td></td></tr>
<tr><td>A,C,E,G</td><td>C</td><td>0x10128100</td><td></td></tr>
<tr><td></td><td>D, E</td><td>0x10128200</td><td></td></tr>
<tr><td>B,D,F,H</td><td>C</td><td>0x10120100</td><td></td></tr>
<tr><td></td><td>D, E</td><td>0x10120200</td><td></td></tr>
</table></td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 10 | 3: Product Description<br>3.2. Product Description | Feature: Clock<br>Error)<br>-<br><br>Correct)<br>Main Oscillation Stabilization Wait Time (at 4 MHz):8.19ms (Initial value) |
| 10 | 3: Product Description<br>3.2. Product Description | Error)<br>-<br><br>Correct)<br>Feature: Embedded CR oscillation<br>See the TraveoTM Platform hardware manual in detail.<br>Stabilization time is as followings.<br>− 0.35 ms to 0.8 ms for 4 MHz (Fast clock)<br>− 0.43 ms to 1.28 ms for 100 kHz (Slow clock) |
| 11 | 3: Product Description<br>3.2. Product Description | Feature: Reset<br>Error)<br>Based on Cortex R5F platform<br>Following resets are not mounted on this device.<br>− INITX<br>− SRSTX<br><br>Correct)<br>RSTX pin + MD pin simultaneous assert INITX (Same as INITX pin input)<br>− Occurrence factor: Simultaneously inputting “L” level to RSTX pin and inputting “L” level to MD pin<br>− Release factor: Inputting “H” level to RSTX pin<br>See the TraveoTM Platform hardware manual in detail.<br>Following resets are not mounted on this device.<br>− SRSTX (and nSRST pin)<br>The product series does not support EX5VRST and writing EX5VRSTCNT bits in SYSC0_SPECFGR has no effect. |
| 11 | 3: Product Description<br>3.2. Product Description | Feature: PLL / SSCG PLL<br>Error)<br>Down spread mode is only supported and available.<br><br>Correct)<br>Product supports down spread and center spread modes with the conditions defined in 9.1.4.3 "Internal Clock Timing". |
| 12 | 3: Product Description<br>3.2. Product Description | Feature: Embedded Program/Work Flash Memory<br>Error)<br>Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less.<br>7-wait-cycle: 80MHz or less.<br>13-wait-cycle: 160MHz or less.<br><br>Correct)<br>Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less.<br>6-wait-cycle: 80MHz or less.<br>12-wait-cycle: 160MHz or less. |

| Page | Section | Change Results |
|---|---|---|
| 13 | 3: Product Description<br>3.2. Product Description | Feature: I2S<br>Error)<br>− I2S has its own PPU, but the function is fixed to disable.<br>Correct)<br>- |
| 14 | 3: Product Description<br>3.2. Product Description | Feature: Multi-Functional Serial (MFS)<br>Error)<br>Some ports of MFS have the dedicated I/O for $I^2C$.<br>See Port description list in detail.<br>When the voltage supply of $I^2C$ interface is 5.0 V, it cannot use the I/O cells of 3.3 V voltage supply for the $I^2C$ terminal.<br>CTS/RTS is not mounted (hardware flow control is not supported for this series.)<br><br>Correct)<br>Only 2 ports of MFS have the dedicated I/O for $I^2C$.<br>See $I^2C$ timing in 9.1.4.6 Multi-Function Serial in detail.<br>The $I^2C$ is not designed to be hot swappable.<br>CTS/RTS is not mounted (hardware flow control is not supported for this series.) |
| 14 | 3: Product Description<br>3.2. Product Description | Feature: Hyper BUS I/F<br>Error)<br>The following register is not supported and cannot be used.<br>− Controller Status Register (HYPERBUSIn_CSR)<br>− Interrupt Status Register (HYPERBUSIn_ISR)<br>− Write Protection Register (HYPERBUSIn_WPR)<br>− Test Register (HYPERBUSIn_TEST)<br><br>Correct)<br>The following register is not supported and cannot be used.<br>− Controller Status Register (HYPERBUSIn_CSR)<br>− Interrupt Enable Register (HYPERBUSIn_IEN)<br>− Interrupt Status Register (HYPERBUSIn_ISR)<br>− Write Protection Register (HYPERBUSIn_WPR)<br>− Test Register (HYPERBUSIn_TEST) |

| Page | Section | Change Results |
|---|---|---|
| 266 | 9. Electric Characteristics<br>9.1.7.1 Electrical Characteristics | Error) |

| Parameter | Rating | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max*3 | | |
| Sector erase time | - | 120 | 180 | ms | Large sector*1<br>Internal preprogramming time included |
| | - | 120 | 180 | ms | 8kB sector*1<br>Internal preprogramming time included |
| | - | 120 | 180 | ms | 4kB sector*1<br>Internal preprogramming time included |
| 16bit write time(Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 32bit write time(Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 64bit write time(Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 256bit write time(Program) | - | 40 | 70 | µs | System-level overhead time excluded*1 |
| Page mode write time(Program) | - | 320 | 600 | µs | System-level overhead time excluded*1 |
| 32bit write time(Work) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| Erase count / Data retention time(Program)*3 | 1,000/20 years | - | - | - | Temperature at write/erase time<br>Average temperature $T_A$=+85 degrees Celsius |
| Erase count / Data retention time(Work)*3 | 1,000/20 years<br>10,000/10 years<br>100,000/5 years | - | - | - | Temperature at write/erase time<br>Average temperature $T_A$=+85 degrees Celsius |

*1: Guaranteed value for up to 1,000 erases

*2: Guaranteed value for up to 100,000 erases

*3: Target Value

Correct)

| Parameter | Rating | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 120 | 180 | ms | Large sector*1<br>Internal preprogramming time included |
| | - | 120 | 180 | ms | 8 kB sector*1<br>Internal preprogramming time included |
| | - | 120 | 180 | ms | 4 kB sector*2<br>Internal preprogramming time included |
| 16-bit write time (Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 32-bit write time (Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 64-bit write time (Program) | - | 30 | 60 | µs | System-level overhead time excluded*1 |
| 256-bit write time (Program) | - | 40 | 70 | µs | System-level overhead time excluded*1 |
| Page mode write time (Program) | - | 320 | 600 | µs | System-level overhead time excluded*1 |
| 32-bit write time (Work) | - | 30 | 60 | µs | System-level overhead time excluded*2 |
| Erase count / Data retention time (Program) | 1,000/20 years | - | - | - | Temperature at write/erase time<br>Average temperature $T_A$ = +85 degrees Celsius |
| Erase count / Data retention time (Work) | 1,000/20 years<br>10,000/10 years<br>100,000/5 years | - | - | - | Temperature at write/erase time<br>Average temperature $T_A$ = +85 degrees Celsius |

*1: Guaranteed value for up to 1,000 erases

*2: Guaranteed value for up to 100,000 erases

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td colspan="3">Rev. *H</td></tr>
<tr><td>4</td><td>1. Overview<br>1.2 Document Definition</td><td>Added the Document Definition as below.<br><br>Error<br><table><tr><th>Document Type</th><th>Definition</th><th>Primary User</th><th>Document Code</th></tr><tr><td>S6J3310/20/30/40 Datasheet</td><td>The function and its characteristics are specified quantitatively.</td><td>Investigator and hardware engineer</td><td>002-10635</td></tr><tr><td>S6J3300 Hardware Manual</td><td>The function and its operation of S6J3300 series are described.</td><td>Software engineer</td><td>002-10185</td></tr><tr><td>Traveo™ Platform Hardware Manual</td><td>The function and its operation of CPU core platform are described.</td><td>Software engineer</td><td>002-07884</td></tr></table><br>Correct<br><table><tr><th>Document Type</th><th>Definition</th><th>Primary User</th><th>Document Code</th></tr><tr><td>S6J3310/20/30/40 Datasheet</td><td>This document.<br><br>The function and its characteristics are specified quantitatively.</td><td>Investigator and hardware engineer</td><td>002-10635</td></tr><tr><td>S6J3300 Hardware Manual</td><td>S6J3300 Series 32-bit Microcontroller Traveo™ Family Hardware Manual<br><br>The function and its operation of S6J3300 series are described.</td><td>Software engineer</td><td>002-10185</td></tr><tr><td>Traveo™ Platform Hardware Manual</td><td>32-Bit Microcontroller Traveo™ Family S6J33xx, S6J34xx, S6J35xx Series Hardware Manual Platform Part<br><br>The function and its operation of CPU core platform are described.</td><td>Software engineer</td><td>002-07884</td></tr></table></td></tr>
<tr><td>14</td><td>3: Product Description<br>3.2. Product Description</td><td>Deleted as below.<br><br>-Note: The description of the preliminary documentation will be changed without any notification.</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 175 | 9. Electric Characteristics<br>9.1.3 DC Characteristics | Added the Hysteresis voltage as below.<br><br>Correct) |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Hysteresis voltage | $V_{HYS1}$ | P0_00 to P0_20, P2_09 to P2_19, P3_00 to P3_07, P3_24 to P3_31, P4_00 to P4_07 | CMOS hysteresis input level is selected | - | $0.05 \times V_{CC}53$ | - | V | |
| | $V_{HYS2}$ | | Automotive input level is selected | - | $0.03 \times V_{CC}53$ | - | V | |
| | $V_{HYS3}$ | | TTL input level is selected | - | 0.035 | - | V | |
| | $V_{HYS4}$ | P1_03 to P1_16, P3_08 to P3_23, P4_08 to P4_23 | CMOS hysteresis input level is selected | - | $0.05 \times V_{CC}5$ | - | V | |
| | $V_{HYS5}$ | | Automotive input level is selected | - | $0.03 \times V_{CC}5$ | - | V | |
| | $V_{HYS6}$ | P1_09, P1_10, P1_15, P1_16 | TTL input level is selected | - | 0.035 | - | V | |
| | $V_{HYS7}$ | P1_17 to P1_31, P2_00 to P2_08, P4_24 to P4_31 | CMOS hysteresis input level is selected | - | $0.05 \times DV_{CC}$ | - | V | |
| | $V_{HYS8}$ | | Automotive input level is selected | - | $0.03 \times DV_{CC}$ | - | V | |
| | $V_{HYS9}$ | RSTX NMIX | - | - | $0.05 \times V_{CC}5$ | - | V | |
| | $V_{HYS10}$ | MD | - | - | $0.05 \times V_{CC}5$ | - | V | |
| | $V_{HYS11}$ | JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS | - | - | 0.035 | - | V | |
| | $V_{HYS12}$ | P0_21 to P0_31, P1_00 to P1_02 | CMOS hysteresis input level is selected | - | $0.05 \times V_{CC}3$ | - | V | |
| | $V_{HYS13}$ | P0_21 to P0_31 | TTL input level is selected | - | 0.035 | - | V | |
| | $V_{HYS14}$ | P1_00 to P1_02 | - | - | 0.080 | - | V | MediaL B |

| Page | Section | Change Results |
|---|---|---|
| 187 | 9. Electric Characteristics 9.1.4.3 Internal Clock Timing | Added the *4 in “Remarks” column<br><br>Error)<br>SSCG0 output clock<br>SSCG1 output clock<br>SSCG2 output clock<br>SSCG3 output clock<br>PLL0 output clock<br>PLL1 output clock<br>PLL2 output clock<br>PLL3 output clock<br><br>Correct)<br>SSCG0 output clock *4<br>SSCG1 output clock *4<br>SSCG2 output clock *4<br>SSCG3 output clock *4<br>PLL0 output clock *4<br>PLL1 output clock *4<br>PLL2 output clock *4<br>PLL3 output clock *4 |
| 188 | 9. Electric Characteristics 9.1.4.3 Internal Clock Timing | Added the below *4 sentence.<br><br>Error)<br>(none)<br><br>Correct)<br>*4: The PLLx/SSCGx cannot set under 200MHz. |
| 195, 198, 201, 204, 207, 210, 213, 216, 249 | 9. Electric Characteristics 9.1.4 AC Characteristics | Modified the shading document name as below.<br><br>Error)<br>*For details, see the hardware manual.*<br><br>Correct)<br>*For details, see the Traveo™ Platform Hardware Manual.* |
| 227 | 9. Electric Characteristics 9.1.4 AC Characteristics | Modified the shading document name as below.<br><br>Error)<br>*Please refer to Product Hardware Manual for available list.*<br><br>Correct)<br>*Please refer to S6J3300 series Hardware Manual for available list.* |

<table>
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<tr><td>265</td><td>11. Ordering Information</td><td>Revised as below.<br><br>Error)
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<tr><th>Part Number *1</th><th>Package</th></tr>
<tr><td>S6J331EKEx*******</td><td>208-pin plastic TEQFP (LEW208)</td></tr>
<tr><td>S6J332CKSx*******</td><td>208-pin plastic TEQFP (LEW208)</td></tr>
<tr><td>S6J334CKSx*******</td><td>208-pin plastic TEQFP (LEW208)</td></tr>
<tr><td>S6J331EJAx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J332CJBx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J332CJTx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J332EJBx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334BJDx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334CJEx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334CJTx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
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<tr><td>S6J334DJTx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334EJAx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334EJEx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334EJTx*******</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334CHBx*******</td><td>144-pin plastic TEQFP (LEX144, LEK144)</td></tr>
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<tr><td>265</td><td>11. Ordering Information</td><td>Correct)
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<tr><td>S6J331EKSESE20000</td><td>208-pin plastic TEQFP (LEW208)</td></tr>
<tr><td>S6J332CKSDSE20000</td><td>208-pin plastic TEQFP (LEW208)</td></tr>
<tr><td>S6J334CKSESE20000</td><td>208-pin plastic TEQFP (LEW208)</td></tr>
<tr><td>S6J331EJSESE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J332EJBDSE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J332EJTDSE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J332EJBESE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
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<tr><td>S6J334EJBESE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334EJTESE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
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<tr><td>S6J334DJEESE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334CJBESE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334CJEESE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334BJDESE20000</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334EJTCSE2000A</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J334EJEDSE2000A</td><td>176-pin plastic TEQFP (LEV176)</td></tr>
<tr><td>S6J332EHBESE20000</td><td>144-pin plastic TEQFP (LEX144, LEK144)</td></tr>
<tr><td>S6J334EHEESE20000</td><td>144-pin plastic TEQFP (LEX144, LEK144)</td></tr>
<tr><td>S6J334DHEESE20000</td><td>144-pin plastic TEQFP (LEX144, LEK144)</td></tr>
<tr><td>S6J334DHFESE20000</td><td>144-pin plastic TEQFP (LEX144, LEK144)</td></tr>
<tr><td>S6J334CHEESE20000</td><td>144-pin plastic TEQFP (LEX144, LEK144)</td></tr>
<tr><td>S6J334CHFESE20000</td><td>144-pin plastic TEQFP (LEX144, LEK144)</td></tr>
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<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>11</td><td>3. Product Description<br>3.2 Product Description<br>Table 3-1: Product Features</td><td>Added the below<br><br>Correct)
<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td>A/D Converter</td><td>AN39 to AN63 are not support for S6J33xxxAx, S6J33xxxCx, S6J33xxxEx, and S6J33xxxGx option.</td></tr>
</table>
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| | | |
|---|---|---|
| 14 | CHAPTER 3: Product Description<br>3.2.1. Ethernet | Deleted the shading parts as below:<br><br>Error) |

| Functions | Remark |
|---|---|
| Direct Memory Access Interface.<br>- partial store and forward<br>- force max amba burst tx/rc<br>- Priority Queueing (Screening) | |
| External FIFO Interface | |
| Additional Low Latency TX FIFO Interface for DMA configurations | |
| MAC Transmit Block<br>- half-duplex<br>- collision<br>- back_pressure | |
| MAC Filtering Block<br>- external address match<br>- VLAN tag<br>- Wakeup On Lan | |
| IEEE 1588 and IEEE 802.1AS Support | |
| MAC PFC Priority Based Pause Frame Support | |
| Energy Efficient Ethernet support | |
| LPI Operation in Cadence IP | |
| 802.1Qav Support – Credit Based Shaping | |
| PHY Interface<br>- GMII<br>- SGMII<br>- TBI | |
| 10/100/1000 Operation<br>- 10 M<br>- 1000 M | |
| SGMII Operation | |
| Jumbo Frames | |
| Physical Control Sub-Layer | |

Correct)

| Functions | Remark |
|---|---|
| External FIFO Interface | |
| Additional Low Latency TX FIFO Interface for DMA configurations | |
| MAC Transmit Block<br>- half-duplex<br>- collision<br>- back_pressure | |
| MAC Filtering Block<br>- external address match<br>- Wakeup On Lan | |
| Energy Efficient Ethernet support | |
| LPI Operation in Cadence IP | |
| PHY Interface | |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td></td><td></td><td>
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<tr><td>- GMII<br>- SGMII<br>- TBI</td><td></td></tr>
<tr><td>10/100/1000 Operation<br>- 1000 M</td><td></td></tr>
<tr><td>SGMII Operation</td><td></td></tr>
<tr><td>Jumbo Frames</td><td></td></tr>
<tr><td>Physical Control Sub-Layer</td><td></td></tr>
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</td></tr>
<tr><td>46</td><td>6. Port Description<br>6.1 Port Description List<br>Table 6-1<br>S6J3310 Series</td><td>Revised the below<br><br>Error)
<table>
<tr><th rowspan="2">Port Name</th><th rowspan="2">Description</th><th colspan="3">Package Pin Number</th><th rowspan="2">Remark</th></tr>
<tr><th>TEQFP 144</th><th>TEQFP 176</th><th>TEQFP 208</th></tr>
<tr><td>PPG0_TOUT0_1</td><td>Base timer 1 output pin (1)</td><td>8</td><td>8</td><td>11</td><td></td></tr>
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Correct)
<table>
<tr><th rowspan="2">Port Name</th><th rowspan="2">Description</th><th colspan="3">Package Pin Number</th><th rowspan="2">Remark</th></tr>
<tr><th>TEQFP 144</th><th>TEQFP 176</th><th>TEQFP 208</th></tr>
<tr><td>PPG0_TOUT0_1</td><td>Base timer 0 output pin (1)</td><td>8</td><td>8</td><td>11</td><td></td></tr>
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</td></tr>
<tr><td>47</td><td>6. Port Description<br>6.1 Port Description List<br>Table 6-1<br>S6J3310 Series</td><td>Revised the below<br><br>Error)
<table>
<tr><th rowspan="2">Port Name</th><th rowspan="2">Description</th><th colspan="3">Package Pin Number</th><th rowspan="2">Remark</th></tr>
<tr><th>TEQFP 144</th><th>TEQFP 176</th><th>TEQFP 208</th></tr>
<tr><td>PPG5_TOUT0_1</td><td>Base timer 11 output pin (1)</td><td>-</td><td>21</td><td>27</td><td></td></tr>
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<tr><th>TEQFP 144</th><th>TEQFP 176</th><th>TEQFP 208</th></tr>
<tr><td>PPG5_TOUT0_1</td><td>Base timer 10 output pin (1)</td><td>-</td><td>21</td><td>27</td><td></td></tr>
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<tr><td>47</td><td>6. Port Description<br>6.1 Port Description List<br>Table 6-1<br>S6J3310 Series</td><td>Revised the below<br><br>Error)
<table>
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<tr><th>TEQFP 144</th><th>TEQFP 176</th><th>TEQFP 208</th></tr>
<tr><td>PPG10_TOUT0_1</td><td>Base timer 21 output pin (1)</td><td>-</td><td>98</td><td>114</td><td></td></tr>
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<tr><td>PPG10_TOUT0_1</td><td>Base timer 20 output pin (1)</td><td>-</td><td>98</td><td>114</td><td></td></tr>
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<tr><td>47</td><td>6. Port Description<br>6.1 Port Description List<br>Table 6-1<br>S6J3310 Series</td><td>Revised the below<br><br>Error)
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<tr><th rowspan="2">Port Name</th><th rowspan="2">Description</th><th colspan="3">Package Pin Number</th><th rowspan="2">Remark</th></tr>
<tr><th>TEQFP 144</th><th>TEQFP 176</th><th>TEQFP 208</th></tr>
<tr><td>PPG15_TOUT0_1</td><td>Base timer 31 output pin (1)</td><td>-</td><td>163</td><td>195</td><td></td></tr>
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<tr><th>TEQFP 144</th><th>TEQFP 176</th><th>TEQFP 208</th></tr>
<tr><td>PPG15_TOUT0_1</td><td>Base timer 30 output pin (1)</td><td>-</td><td>163</td><td>195</td><td></td></tr>
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<tr><td>263 to 264</td><td>12. Errata</td><td>Added section “12. Errata”</td></tr>
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## Document History

**Document Title: S6J3310 Series/S6J3320 Series/S6J3330 Series/S6J3340 Series, 32-bit Microcontroller Traveo™ Family**
**Document Number: 002-10635**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 5063970 | TMOR | 01/25/2016 | New Spec. |
| *A | 5203759 | TMOR | 04/06/2016 | Correct device revision, Chip ID, LVD spec, DDR-HSSPI spec, Hyper BUS spec, and MediaLB spec<br>For detail, see “Major Changes”. |
| *B | 5371697 | TMOR | 07/25/2016 | Additional Handling Devices comments(Method to Switch off VCC12 during Power-off Sequence), LCD BUS I/F AC spec, Internal operation clock frequency comments, LVD comments, and ADC Units vs channel comments<br>The package dimension of TEQFP144 (0.4mm Pitch) correct from the provisional version to the formal version.<br>TYPO: $I^2C$ Fast Mode<br>For detail, see “Major Changes” |
| *C | 5622186 | MATO | 02/07/2017 | - ID add<br>-$I_{CCT}$, $I_{CCH}$ spec add<br>-LCD bus I/F spec revise<br>-Power and RSTX sequence add<br>-Ordering Information revise<br>For detail, see “Major Changes” |
| *D | 5691761 | HARA | 04/27/2017 | Updated logo and copyright. |
| *E | 5782663 | MATO | 06/26/2017 | -Special spec of total maximum clamp current add<br>-Icc12, Icch12 spec change<br>-Power sequence add<br>-Flash write/erase spec change<br>For detail, see “Major Changes” |
| *F | 5947678 | MATO | 10/27/2017 | -Revision change<br>-Power supply current for S6J33xxxxE add<br>-Ordering Information change<br>For detail, see “Major Changes” |
| *G | 5969954 | MATO | 11/20/2017 | -Function list and Product Description change<br>For detail, see “Major Changes” |
| *H | 6136290 | GSHI | 04/17/2018 | -Document Definition change<br>-Hysteresis voltage add in DC Characteristics<br>-PLLx/SSCGx minimum clock frequencies add in Internal Clock Timing<br>-Ordering Information change |

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | | | | For detail, see “Major Changes” |
| *I | 6300353 | GSHI | 09/05/2018 | - Add an option limitation for Description of A/D Converter of Product Description.<br>- Update Ethernet Support Functions.<br>- Update Base timer allocation<br>- Added 12. Errata<br>For detail, see “Major Changes” |

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