

1.1 V to 5.5 V, Slew Rate Controlled Load Switch

DESCRIPTION

SiP32408 and SiP32409 are slew rate controlled load switches designed for 1.1 V to 5.5 V operation.

These devices guarantee low switch on-resistance at 1.2 V input. They feature a controlled soft-on slew rate of typical 2.5 ms that limits the inrush current for designs of heavy capacitive load and minimizes the resulting voltage droop at the power rails.

SiP32408 and SiP32409 feature a low voltage control logic interface (On/Off interface) that can interface with low voltage control signals without extra level shifting circuit.

Both SiP32408 and SiP32409 have exceptionally low shutdown current and provide reverse blocking to prevent high current flowing into the power source.

SiP32409 integrates a output discharge circuit for fast turn off.

Both SiP32408 and SiP32409 are available in TDFN4 package of 1.2 mm by 1.6 mm.

FEATURES

- 1.1 V to 5.5 V operation voltage range
- Flat row R_{ON} down to 1.2 V
- 42 m Ω typical from 1.5 V to 5 V
- Slew rate controlled turn-on: 2.5 ms at 3.6 V
- Low guiescent current < 1 µA when disabled 10.5 μ A typical at $V_{IN} = 1.2 \text{ V}$
- Reverse current blocking when switch is off
- Output discharge (SiP32409)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- PDAs/smart phones
- Notebook/netbook computers
- Tablet PC
- Portable media players
- Digital camera
- GPS navigation devices
- Data storage devices
- Optical, industrial, medical, and healthcare devices

TYPICAL APPLICATION CIRCUIT

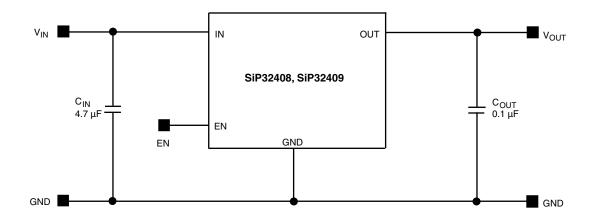


Figure 1 - SiP32408, SiP32409 Typical Application Circuit



SiP32408, SiP32409

Vishay Siliconix



ORDERING INFORMATION	ORDERING INFORMATION				
Temperature Range	Package	Marking	Part Number		
- 40 °C to 85 °C	TDFN4 1.2 mm x 1.6 mm	Jx	SiP32408DNP-T1-GE4		
- 40 0 10 83 0	101114 1.2 111111 X 1.0 111111	Kx	SiP32409DNP-T1-GE4		

Notes:

x = Lot code

GE4 denotes halogen-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS				
Parameter	Limit	Unit		
Supply Input Voltage (V _{IN})	- 0.3 to 6			
Enable Input Voltage (V _{EN})	- 0.3 to 6	V		
Output Voltage (V _{OUT})	- 0.3 to 6			
Maximum Continuous Switch Current (I _{max.}) ^c	3.5			
Maximum Repetitive Pulsed Current (1 ms, 10 % Duty Cycle) ^c	6	Α		
Maximum Non-Repetitive Pulsed Current (100 μs, EN = Active) ^c	12			
ESD Rating (HBM)	7000	V		
Junction Temperature (T _J)	- 40 to 150	°C		
Thermal Resistance $(\theta_{JA})^a$	170	°C/W		
Power Dissipation (P _D) ^{a,b}	735	mW		

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE		
Parameter	Limit	Unit
Input Voltage Range (V _{IN})	1.1 to 5.5	V
Operating Junction Temperature Range (T _J)	- 40 to 125	°C

a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout.

b. Derate 5.9 mW/°C above $T_A = 25$ °C, see PCB layout.

c. T_A = 25 °C, see PCB layout

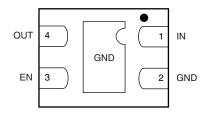


SPECIFICATIONS							
		Test Conditions Unless Specified V _{IN} = 5 V, T _A = - 40 °C to 85 °C	Limits - 40 °C to 85 °C				
Parameter	Symbol	(Typical values are at T _A = 25 °C)	Min. ^a	Typ.b	Max. ^a	Unit V	
Operating Voltage ^c	V _{IN}		1.1	-	5.5	٧	
		V _{IN} = 1.2 V, EN = active	-	10.5	17		
		V _{IN} = 1.8 V, EN = active	-	21	30	1	
Ovice and Oversent		V _{IN} = 2.5 V, EN = active	-	34	50	1	
Quiescent Current	IQ	V _{IN} = 3.6 V, EN = active	-	54	90	1	
		V _{IN} = 4.3 V, EN = active	-	68	110	μΑ	
		V _{IN} = 5 V, EN = active	-	105	180	1	
Off Supply Current	I _{Q(off)}	EN = inactive, OUT = open	-	-	1	1	
Off Switch Current	I _{DS(off)}	EN = inactive, OUT = GND	-	-	1	1	
Reverse Blocking Current	I _{RB}	V _{OUT} = 5 V, V _{IN} = 0 V, V _{EN} = inactive	-	-	10	1	
		V _{IN} = 1.2 V, I _L = 100 mA, T _A = 25 °C	-	45	52		
		V _{IN} = 1.8 V, I _L = 100 mA, T _A = 25 °C	-	42	50	1	
On Basistana	_	V _{IN} = 2.5 V, I _L = 100 mA, T _A = 25 °C	-	42	50	1	
On-Resistance	R _{DS(on)}	V _{IN} = 3.6 V, I _L = 100 mA, T _A = 25 °C	-	42	50	- mΩ -	
		V _{IN} = 4.3 V, I _L = 100 mA, T _A = 25 °C	-	42	50		
		$V_{IN} = 5 \text{ V}, I_{L} = 100 \text{ mA}, T_{A} = 25 ^{\circ}\text{C}$	-	44	50		
On-Resistance TempCoefficient	TC _{RDS}		-	3300	-	ppm/°C	
		V _{IN} = 1.2 V	-	-	0.3	-	
		V _{IN} = 1.8 V	-	-	0.4 ^d		
	.,	V _{IN} = 2.5 V	-	-	0.5 ^d	1	
EN Input Low Voltage ^c	V _{IL}	V _{IN} = 3.6 V	-	-	0.6 ^d		
		V _{IN} = 4.3 V	-	-	0.7 ^d		
		V _{IN} = 5 V	-	-	0.8 ^d	1 ,,	
	V _{IH}	V _{IN} = 1.2 V	0.9 ^d	-	-	V	
		V _{IN} = 1.8 V	1.2 ^d	-	-		
		V _{IN} = 2.5 V	1.4 ^d	-	-		
EN Input High Voltage ^c		V _{IN} = 3.6 V	1.6 ^d	-	-		
		V _{IN} = 4.3 V	1.7 ^d	-	-		
		V _{IN} = 5 V	1.8	-	-		
EN Input Leakage	I _{SINK}	V _{EN} = 5.5 V	- 1	-	1	μΑ	
Output Pulldown Resistance	R _{PD}	EN = inactive, T _A = 25 °C, (for SiP32409 only)	-	217	280	Ω	
Output Turn-On Delay Time	t _{d(on)}		-	1.8	-		
Output Turn-On Rise Time	t _(on)	$V_{IN} = 3.6 \text{ V}, R_{LOAD} = 10 \Omega, T_A = 25 \text{ °C}$	1.2	2.5	3.8	ms	
Output Turn-Off Delay Time	t _{d(off)}		-	-	0.001	1	

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. For V_{IN} outside this range consult typical EN threshold curve.
- d. Not tested, guarantee by design.

PIN CONFIGURATION





Bottom View Figure 2 - TDFN4 1.2 mm x 1.6 mm Package

PIN DESCRIPTION		
Pin Number	Name	Function
1	IN	This is the input pin of the switch
2	GND	Ground connection
3	EN	Enable input
4	OUT	This is the output pin of the switch

BLOCK DIAGRAM

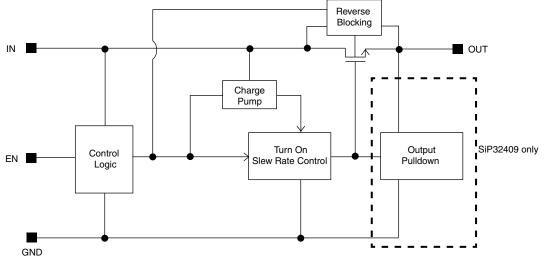
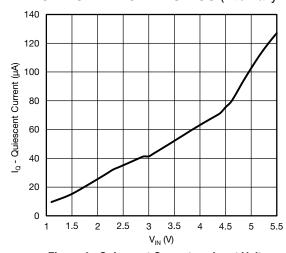


Figure 3 - Functional Block Diagram





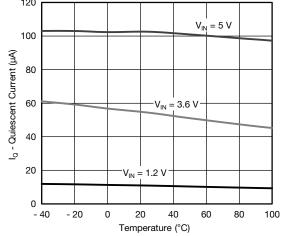


Figure 5 - Quiescent Current vs. Temperature



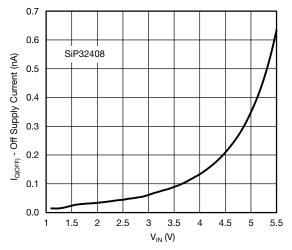


Figure 6 - Off Supply Current vs. Input Voltage

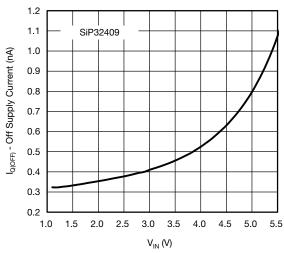


Figure 7 - Off Supply Current vs. Input Voltage

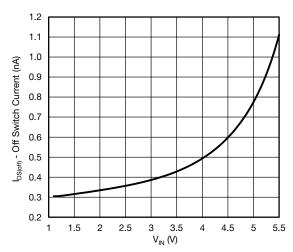


Figure 8 - Off Switch Current vs. Input Voltage

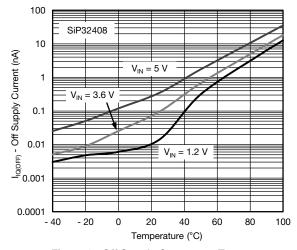


Figure 9 - Off Supply Current vs. Temperature

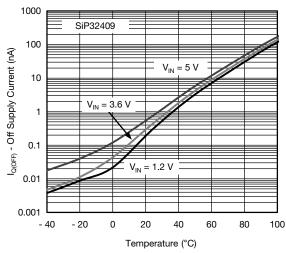


Figure 10 - Off Supply Current vs. Temperature

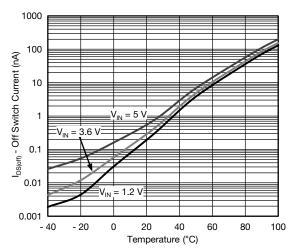


Figure 11 - Off Switch Current vs. Temperature

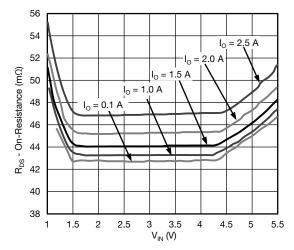


Figure 12 - $R_{DS(on)}$ vs. V_{IN}

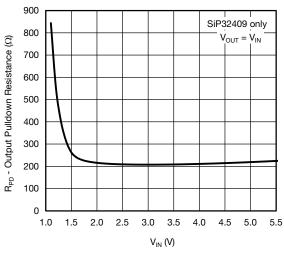


Figure 13 - Output Pulldown Resistance vs. Input Voltage

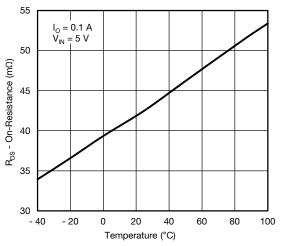


Figure 14 - R_{DS(on)} vs. Temperature

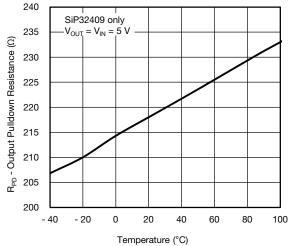


Figure 15 - Output Pulldown Resistance vs. Temperature



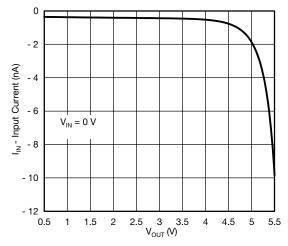


Figure 16 - Reverse Blocking Current vs. Output Voltage

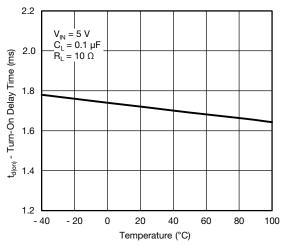


Figure 18 - Turn-On Delay Time vs. Temperature

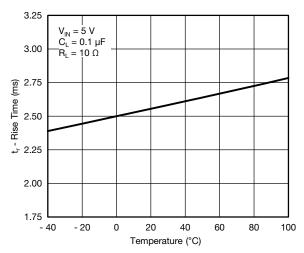


Figure 17 - Rise Time vs. Temperature

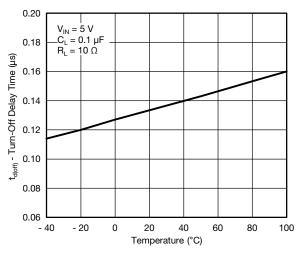


Figure 19 - Turn-Off Delay Time vs. Temperature

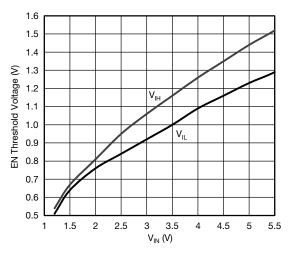


Figure 20 - EN Threshold Voltage vs. Input Voltage

TYPICAL WAVEFORMS



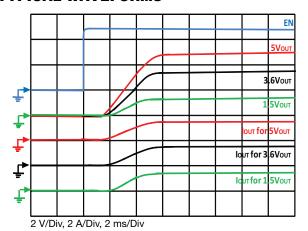


Figure 21 - Typical Turn-on Delay, Rise Time C_{OUT} = 0.1 $\mu F,\,C_{IN}$ = 4.7 $\mu F,\,I_{OUT}$ = 1.5 A

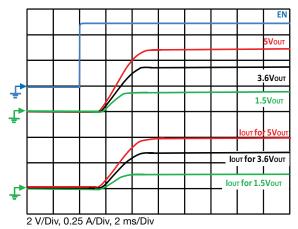


Figure 22 - Typical Turn-on Delay, Rise Time C_{OUT} = 0.1 $\mu F,\,C_{IN}$ = 4.7 $\mu F,\,R_{OUT}$ = 10 Ω

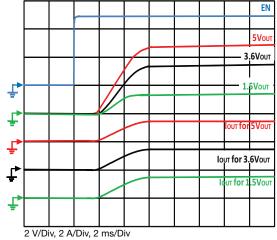


Figure 23 - Typical Turn-on Delay, Rise Time C_{OUT} = 200 $\mu F,\,C_{IN}$ = 4.7 $\mu F,\,I_{OUT}$ = 1.5 A

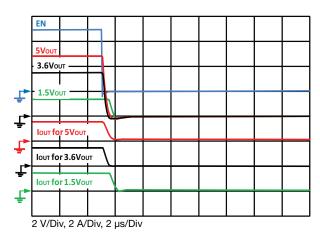


Figure 24 - Typical Fall Time C_{OUT} = 0.1 $\mu F,\,C_{IN}$ = 4.7 $\mu F,\,I_{OUT}$ = 1.5 A

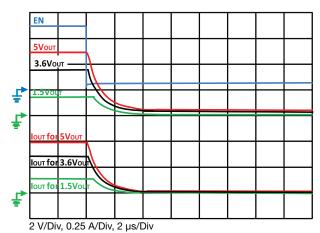


Figure 25 - Typical Fall Time C_{OUT} = 0.1 $\mu F,~C_{IN}$ = 4.7 $\mu F,~R_{OUT}$ = 10 Ω

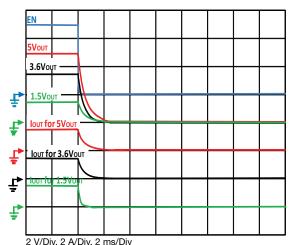


Figure 26 - Typical Fall Time C_{OUT} = 200 μ F, C_{IN} = 4.7 μ F, I_{OUT} = 1.5 A



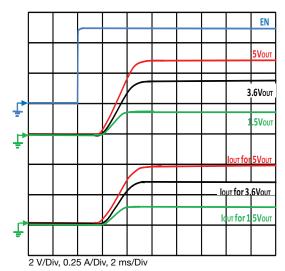


Figure 27 - Typical Turn-on Delay, Rise Time C_{OUT} = 200 μ F, C_{IN} = 4.7 μ F, R_{OUT} = 10 Ω

DETAILED DESCRIPTION

SiP32408 and SiP32409 are advanced slew rate controlled high side load switches consisted of a n-channel power switch. When the device is enable the gate of the power switch is turned on at a controlled rate to avoid excessive inrush current. Once fully on the gate to source voltage of the power switch is biased at a constant level. The design gives a flat on resistance throughout the operating voltages. When the device is off, the reverse blocking circuitry prevents current from flowing back to input if output is raised higher than input. The reverse blocking mechanism also works in case of no input applied.

APPLICATION INFORMATION

Input Capacitor

SiP32408 and SiP32409 do not require an input capacitor. To limit the voltage drop on the input supply caused by transient inrush currents, an input bypass capacitor is recommended. A 2.2 µF ceramic capacitor placed as close to the V_{IN} and GND should be enough. Higher values capacitor can help to further reduce the voltage drop. Ceramic capacitors are recommended for their ability to withstand input current surge from low impedance sources such as batteries in portable devices.

Output Capacitor

While these devices works without an output capacitor, an 0.1 μF or larger capacitor across V_{OUT} and GND is recommended to accommodate load transient condition. It also help to prevent parasitic inductance forces V_{OUT} below GND when switching off. Output capacitor has minimal affect on device's turn on slew rate time. There is no requirement on capacitor type and its ESR.

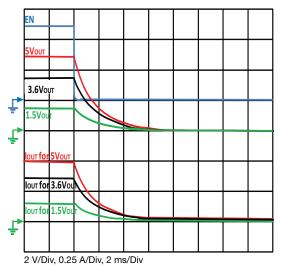


Figure 28 - Typical Fall Time $C_{OUT} = 200 \mu F$, $C_{IN} = 4.7 \mu F$, $R_{OUT} = 10 \Omega$

Enable

The EN pin is compatible with both TTL and CMOS logic voltage levels. Enable pin voltage can be above IN once it is within the absolute maximum rating range.

Protection Against Reverse Voltage Condition

SiP32408 and SiP32409 contain a reverse blocking circuitry to protect the current from going to the input from the output in case where the output voltage is higher than the input voltage when the main switch is off. Reverse blocking works for input voltage as low as 0 V.

Thermal Considerations

SiP32408 and SiP32409 are designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 3.5 A, as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 170 °C/W) the power pad of the device should be connected to a heat sink on the printed circuit board. Figure 21 shows a typical PCB layout. All copper traces and vias for the IN and OUT pins should be sized adequately to carry the maximum continuous current.

The maximum power dissipation in any application is dependant on the maximum junction temperature, $T_{J(max.)}$ = 125 °C, the junction-to-ambient thermal resistance for the TDFN4 1.2 mm x 1.6 mm package, θ_{J-A} = 170 °C/W, and the ambient temperature, TA, which may be formulaically

P (max.) =
$$\frac{T_J (max.) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{170}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 324 mW.

So long as the load current is below the 3.5 A limit, the maximum continuous switch current becomes a function of two things: the package power dissipation and the R_{DS(on)} at the ambient temperature.

As an example let us calculate the worst case maximum load current at $T_A = 70$ °C. The worst case $R_{DS(on)}$ at 25 °C occurs at an input voltage of 1.2 V and is equal to 52 m Ω . The R_{DS(on)} at 70 °C can be extrapolated from this data using the following formula:

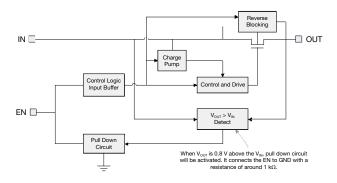
$$R_{DS(on)}$$
 (at 70 °C) = $R_{DS(on)}$ (at 25 °C) x (1 + T_C x DT) Where T_C is 3300 ppm/°C. Continuing with the calculation

$$R_{DS(on)}$$
 (at 70 °C) = 52 m Ω x (1 + 0.0033 x (70 °C - 25 °C)) = 60 m Ω

The maximum current limit is then determined by

$$I_{LOAD}$$
 (max.) $< \sqrt{\frac{P \text{ (max.)}}{R_{DS(ON)}}}$

which in this case is 2.3 A. Under the stated input voltage condition, if the 2.3 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.



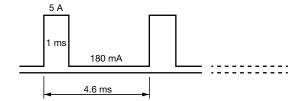
Active EN Pull Down for Reverse Blocking

When an internal circuit detects the condition of VOLIT 0.8 V higher than V_{IN}, it will turn on the pull down circuit connected to EN, forcing the switching OFF. The pull down value is about 1 k Ω .

Pulse Current Capability

The device is mounted on the evaluation board shown in the PCB layout section. It is loaded with pulses of 5 A and 1 ms for periods of 4.6 ms.





SiP32408 and SiP32409 can safely support 5 A pulse current repetitively at 25 °C.

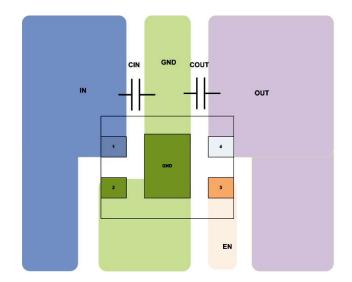
Switch Non-Repetitive Pulsed Current

SiP32408 and SiP32409 can withstand inrush current of up to 12 A for 100 µs at 25 °C when heavy capacitive loads are connected and the part is already enabled.

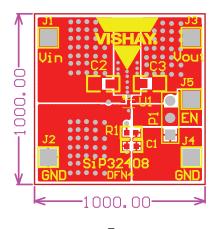
Recommended Board Layout

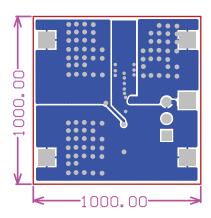
For the best performance, all traces should be as short as possible to minimize the inductance and parasitic effects. The input and output capacitors should be kept as close as possible to the input and output pins respectively.

Connecting the central exposed pad to GND, using wide traces for input, output, and GND help reducing the case to ambient thermal impedance.



EVALUATION BOARD LAYOUT



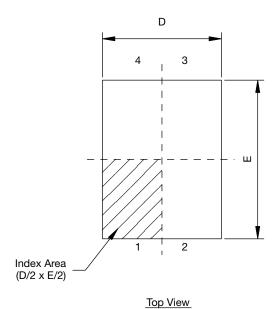


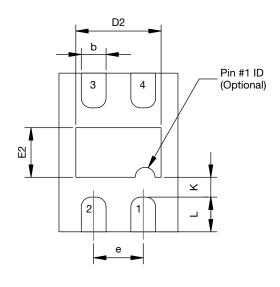
Top **Bottom**

Figure 29 - Evaluation board Layout for TDFN4 1.2 mm x 1.6 mm (type: FR4, size: 1" x 1", thickness: 0.062", copper thickness: 2 oz.)

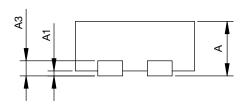
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TDFN4 1.2 x 1.6 Case Outline





Bottom View



Side View

DWG: 5995

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	-	0.05	0.00	-	0.002
A3		0.15 REF.			0.006	
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.15	1.20	1.25	0.045	0.047	0.049
D2	0.81	0.86	0.91	0.032	0.034	0.036
е		0.50 BSC		0.020		
Е	1.55	1.60	1.65	0.061	0.063	0.065
E2	0.45	0.50	0.55	0.018	0.020	0.022
K	0.25 TYP.			0.010 TYP.		
L	0.25	0.30	0.35	0.010	0.012	0.014

Revision: 07-Nov-11 Document Number: 65734



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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

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OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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