



150-mA LOW-NOISE LDO WITH IN-RUSH CURRENT CONTROL FOR USB APPLICATION

FEATURES

- 150-mA Low-Dropout Regulator
- Available in 2.5 V, 3.3 V
- Programmable Slew Rate Control
- Output Noise Typically 56 µV_{RMS}
- Only 17 µA Quiescent Current at 150 mA
- 1 μA Quiescent Current in Standby Mode
- Dropout Voltage Typically 150 mV at 150 mA (TPS78833)
- Over Current Limitation
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package





DESCRIPTION

The TPS78825 and TPS78833 are very small (SOT-23) package, low-noise LDOs that regulate the output voltage to 2.5 V and 3.3 V with input voltage ranging from 2.7 V to an absolute maximum of 13.5 V. These devices output 150 mA with a peak current of 350 mA (typ). The TPS788xx family uses the SR pin to program the output voltage slew rate to control the in-rush current. This is specifically used in the USB application where large load capacitance is present at start-up. The TPS788xx devices use only 17 μ A of quiescent current and exhibit only 56 μ V_{RMS} of output voltage noise using a 10 μ F output capacitor.

The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, typically 150 mV at 150 mA of load current, and is directly proportional to the load current.

The TPS788xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μ A typical at T_J = 25°C.





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TPS78825, TPS78833

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AVAILABLE OPTIONS									
ТJ	VOLTAGE	PACKAGE	E PART NUMBER SYM						
4000 10 40500	2.5 V	SOT-23	TPS78825DBVT [†]	TPS78825DBVR [‡]	PGZI				
–40°C to 125°C	3.3 V	(DBV)	TPS78833DBVT	TPS78833DBVR	PGTI				

[†] The DBVT indicates tape and reel of 250 parts.[‡] The DBVR indicates tape and reel of 3000 parts.

functional block diagram



Terminal Functions

TERMIN	AL		DESCRIPTION					
NAME	NO.	1/0	DESCRIPTION					
EN	3	I	Active low enable					
GND	2		Regulator ground					
IN	1	I	The IN terminal is the input to the device.					
OUT	5	0	The OUT terminal is the regulated output of the device.					
SR	4	Ι	The SR terminal is used to control the in-rush current.					

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Input voltage range (see Note 1)	0.3 V to 13.5 V
Voltage range at EN	\dots –0.3 V to V _I + 0.3 V
Voltage on OUT	
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T _J	$\dots -40^{\circ}C$ to $150^{\circ}C$
Operating ambient temperature range, T _A	$\dots -40^{\circ}C$ to $85^{\circ}C$
Storage temperature range, T _{stg}	$\ldots \ldots \ldots -65^\circ C$ to $150^\circ C$

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$\textbf{R}_{\theta \textbf{JC}}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T _A = 25°C	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
Low K [¶]	DBV	65.8°C/W	259°C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K [#]	DBV	65.8°C/W	180°C/W	5.6 mW/°C	555 mW	305 mW	222 mW

If The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.



TPS78825, TPS78833

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PARAMETER	TEST CO	MIN	TYP	MAX	UNIT					
VI Input voltage (see Note 2)			2.7		10	V				
IO Continuous output current (see N	lote 3)			0		150	mA			
T _J Operating junction temperature				-40		125	°C			
	TDC70005	Tj = 25°C			2.5		<u> </u>			
Output voltogo	1P576625	10 μA< IO < 150 mA,	3.5 V < V _I < 10 V	2.425		2.575	V			
Output voltage	TDC70022	T _J = 25°C			3.3		v			
	19576633	10 μA< IO < 150 mA,	3.8 V < VJ < 10 V	3.201		3.399				
		10 μA< IO < 450 mA,	T _J = 25°C		17					
Quescent current (GND current)		10 μA< I _O < 150 mA				28	μΑ			
Load regulation		10 μA< I _O < 200 mA,	$T_J = 25^{\circ}C$		12		mV			
Output voltage line regulation ($\Delta V_O/V_O$)		$V_{O} + 1 V < V_{I} \le 10 V_{,}$	$T_J = 25^{\circ}C$		0.04		9/ /\ /			
(see Note 5)		V_{O} + 1 V < $V_{I} \le 10 V$				0.1	70/ V			
Output noise voltage (TPS78833)	$\begin{array}{l} BW = 200 \text{ Hz to } 100 \text{ H} \\ I_O = 150 \text{ mA}, \\ T_J = 25^\circ\text{C}, \\ C_O = 10 \ \mu\text{F}, \\ C(\text{SR}) = 0.47 \ \mu\text{F} \end{array}$		56		^{μV} RMS					
		$R_{I} = 22 \Omega_{i}$	$C_{(byp)} = 0.01 \ \mu F$		10					
Time, start-up (TPS78833)		$C_0 = 10 \mu F$,	$C_{(byp)} = 0.1 \mu F$		50		ms			
		TJ = 25°C	$C_{(byp)} = 0.47 \ \mu F$		300					
Output current limit		$V_{O} = 0 V$ (see Note 4	.)		350	750	mA			
Standby current	EN = 0 V, 2.7 V < V _I <		1	2	μA					
High level enable input voltage	2.7 V < V _I < 10 V	1.7			V					
Low level enable input voltage	2.7 V < V _I < 10 V				0.9	V				
Input current (EN)	EN = 0	-1		1	μA					
Power supply ripple rejection	TPS78833	f = 1 kHz, T _J = 25°C, C ₀ = 10 μ F	C _(SL) = 0.01 μF, I _O = 150 mA,		70		dB			
	TD070000	I _O = 150 mA, T _J = 25	S°C		150					
Dropoul voltage (see Note 6)	I _O = 150 mA			300	mv					

electrical characteristics over recommended operating free-air temperature range $\overline{EN} = 0$, T_J = -40 to 125 °C, V_I = V_{O(tvp)} + 1 V, I_O = 1 mA, C_o = 4.7 μ F, C_(SR) = 0.01 μ F (unless otherwise noted)

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula: $V_I(min) = V_O(max) + V_{DO}(max load)$

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

The minimum IN operating voltage is 2.7 V or V_{O(typ)} + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. The maximum output current is 200 mA.

5. If $V_0 \le 2.5$ V then $V_{Imin} = 2.7$ V, $V_{Imax} = 5.5$ V:

Line regulation (mV) =
$$(\%/V) \times \frac{V_O(V_{Imax} - 2.7 V)}{100} \times 1000$$

If $V_O > 2.5$ V then $V_{Imin} = V_O + 1$ V, $V_{Imax} = 5.5$ V.

6. IN voltage equals VO(typ) – 100 mV









0.1

0

60

90

Figure 13

IO - Output Current - mA

120

150

0.1

0

60

90

IO - Output Current - mA Figure 14

120

150

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

The TPS788xx family of low-dropout (LDO) regulators has been optimized for use in battery-operated equipment. It features extremely low dropout voltages, low output noise, low quiescent current (17 μ A typically), and enable inputs to reduce supply currents to 1 μ A when the regulator is turned off. A typical application circuit is shown in Figure 15.



Figure 15. Typical Application Circuit

external capacitor requirements

Although not required, a 0.047- μ F or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS788xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS788xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μ F. The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω . to ensure stability. Capacitor values larger than 4.7 μ F are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 μ F are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μ F surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

PART NO.	MFR.	VALUE	MAX ESR [†]	SIZE (H \times L \times W) [†]
T494B475K016AS	Kemet	4.7 μF	1.5 Ω	$1.9\times3.5\times2.8$
195D106x0016x2T	Sprague	10 μF	1.5 Ω	$1.3 \times 7.0 \times 2.7$
695D106x003562T	Sprague	10 μF	1.3 Ω	$2.5\times7.6\times2.5$
TPSC475K035R0600	AVX	4.7 μF	0.6 Ω	$2.6\times6.0\times3.2$

CAPACITOR SELECTION

[†] Size is in mm. The ESR maximum resistance is in Ohms at 100 kHz and $T_A = 25^{\circ}$ C. Contact the manufacturer for the minimum ESR values.



APPLICATION INFORMATION

external capacitor requirements (continued)

The external bypass capacitor, used in conjunction with an internal resistor to form a low-pass filter, should be a low ESR ceramic capacitor. For example, the TPS78833 exhibits only 56 μ V_{RMS} of output voltage noise using a 0.01 μ F ceramic bypass capacitor and a 10- μ F ceramic output capacitor. Note that the output will start up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 150-k Ω resistor and external capacitor.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_{D} , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

T_Jmax is the maximum allowable junction temperature.

 $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$\mathsf{P}_{\mathsf{D}} = \left(\mathsf{V}_{\mathsf{I}} - \mathsf{V}_{\mathsf{O}}\right) \times \mathsf{I}_{\mathsf{O}}$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

regulator protection

The TPS788xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS788xx features internal current limiting and thermal protection. During normal operation, the TPS78833 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.





PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TPS78825DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	PGZI	Samples
TPS78825DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	PGZI	Samples
TPS78825DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	PGZI	Samples
TPS78833DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	PGTI	Samples
TPS78833DBVRG4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	0 to 70		Samples
TPS78833DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	PGTI	Samples
TPS78833DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	PGTI	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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PACKAGE OPTION ADDENDUM

6-Jul-2015

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78825DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS78825DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS78833DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS78833DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78825DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS78825DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TPS78833DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS78833DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0

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