

SPREAD SPECTRUM CLOCK SYNTHESIZER

IDT5P50901/2/3/4

Description

The IDT5P50901/2/3/4 is a family of 1.8V low power, spread spectrum clock generators capable of reducing EMI radiation from an input clock. Spread spectrum technique is capable of reducing the harmonic frequency amplitude peaks by several dB.

Ordering Information
Input Frequency

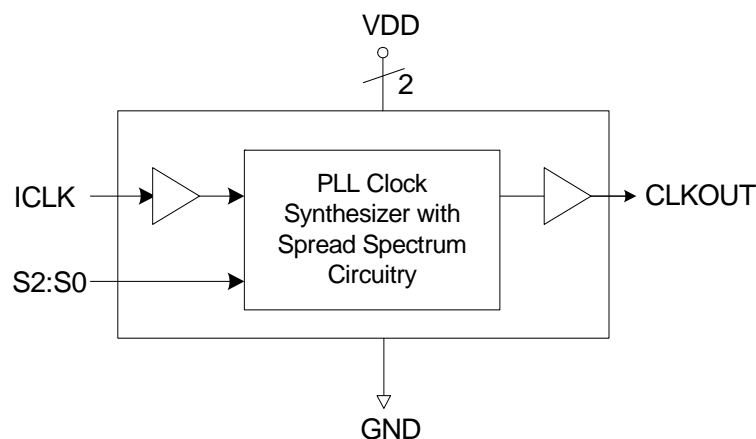
10 to 25 MHz - 5P50901NBI/5P50901DVG1
 20 to 50 MHz - 5P50902NBI/5P50902DVG1
 40 to 100 MHz - 5P50903NBI/5P50903DVG1
 80 to 170 MHz - 5P50904NBI/5P50904DVG1

Features

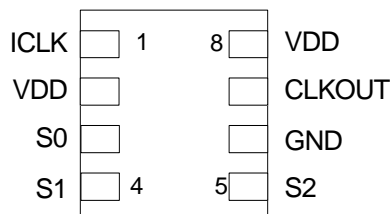
- 8-pin DFN package (2x2mm)
8-pin MSOP package (3x4.9mm)
- Provides a spread spectrum output clock
- Input frequency range of 10 to 170 MHz
- Output frequency range of 10 to 170 MHz
- Center and down spread
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- Operating voltage of 1.8 V, 2.5 or 3.3V
- RoHS 6 compliant package

Spread Modulation Frequency Table

| Part Number | Input (MHz) | Modulation (kHz) | Input (MHz) | Modulation (kHz) | Modulation Frequency (kHz) |
|-------------|-------------|------------------|-------------|------------------|----------------------------|
| 5P50901 | 10 | 27 | 25 | 67.5 | $ICLK * 27 / 10000$ |
| 5P50902 | 20 | 27 | 50 | 67.5 | $ICLK * 27 / 20000$ |
| 5P50903 | 40 | 27 | 100 | 67.5 | $ICLK * 27 / 40000$ |
| 5P50904 | 80 | 27 | 170 | 57.4 | $ICLK * 27 / 80000$ |

Block Diagram


Pin Assignment



8-pin DFN

Spread Direction and Percentage Select Table

| S2 | S1 | S0 | Spread Direction | Spread Percentage |
|----|----|----|------------------|-------------------|
| 0 | 0 | 0 | OFF | -- |
| 0 | 0 | 1 | Center | ± 0.25 |
| 0 | 1 | 0 | Center | ± 0.5 |
| 0 | 1 | 1 | Center | ± 1.0 |
| 1 | 0 | 0 | Center | ± 1.5 |
| 1 | 0 | 1 | Center | ± 2.0 |
| 1 | 1 | 0 | Down | -0.5 |
| 1 | 1 | 1 | Down | -1.0 |

Pin Description

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | ICLK | Input | Input clock. |
| 2 | VDD | Power | Voltage supply. Connect to 1.8 V ± 0.1 V, 2.5 V $\pm 10\%$ or 3.3 V $\pm 10\%$, |
| 3 | S0 | Input | Function select 0 input. Selects spread amount and direction per table above. Internal pull-down resistor. |
| 4 | S1 | Input | Function select 1 input. Selects spread amount and direction per table above. Internal pull-down resistor. |
| 5 | S2 | Input | Function select 2 input. Selects spread amount and direction per table above. Internal pull-down resistor. |
| 6 | GND | Power | Connect to ground. |
| 7 | CLKOUT | Output | Clock output. |
| 8 | VDD | Power | Voltage supply. Connect to 1.8 V ± 0.1 V, 2.5 V $\pm 10\%$ or 3.3 V $\pm 10\%$ |

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the IDT5P50901/2/3/4 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of $0.01\mu\text{F}$ must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω .

External Clock Input

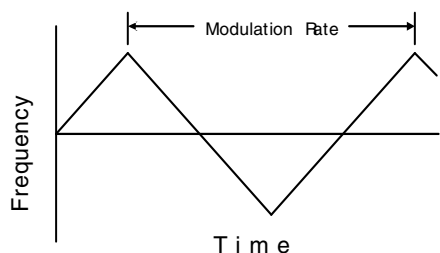
This device operates from an external clock input and as such does not have a on chip oscillator circuit.

Spread Spectrum Profile

The IDT5P50901/2/3/4 is a low EMI clock generator using an optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices.

The modulation rate is directly relate to the input clock frequency.

For input frequency ICLK, then use the modulation frequency indicated for the part below.



PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) The $0.01\mu\text{F}$ decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.
- 2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.
- 3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDT5P50901/2/3/4. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P50901/2/3/4. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|----------------------|
| Supply Voltage, VDD | -0.5 V to 5.0 V |
| All Inputs | -0.5 V to VDD +0.5 V |
| Ambient Operating Temperature | -40 to +85° C |
| Storage Temperature | -50 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature | -40 | | +85 | °C |
| Power Supply Voltage VDD (measured in respect to GND) | +1.7 | +1.8 | +1.9 | V |
| | +2.25 | +2.5 | +2.75 | V |
| | +2.97 | +3.3 | +3.63 | V |

DC Electrical Characteristics

Unless stated otherwise, **VDD = 1.8 V ±0.1 V**. Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------|--------------------------|------------------|------|------------|-------|
| Operating Voltage | VDD | | 1.7 | 1.8 | 1.9 | V |
| Input High Voltage | V _{IH} | ICLK, S2:S0 | VDD x 0.8 | | VDD + 0.3 | V |
| Input Low Voltage | V _{IL} | ICLK, S2:S0 | GND | | VDD x 0.2 | V |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | VDD x 0.75 | VDD | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA | | GND | VDD x 0.25 | V |
| IDD | | No load | See table page 6 | | | |
| Input Capacitance | | | | 5 | | pF |
| Load Capacitance | | | | 5 | | pF |
| Internal Pull-down Resistor | R _{PD} | S1:S0 | | 200 | 260 | kΩ |

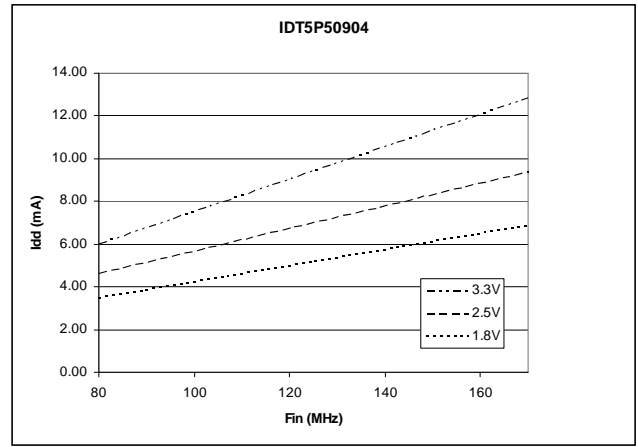
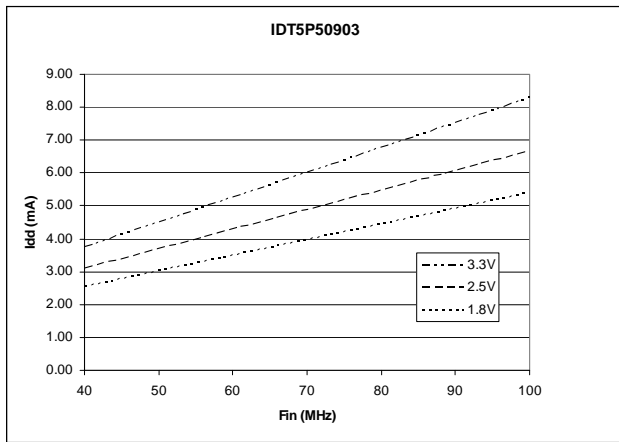
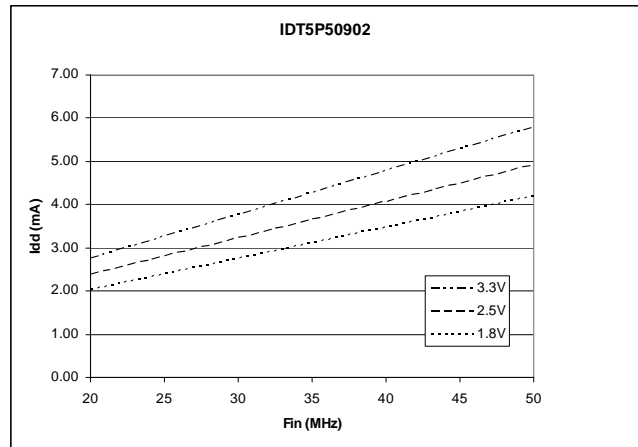
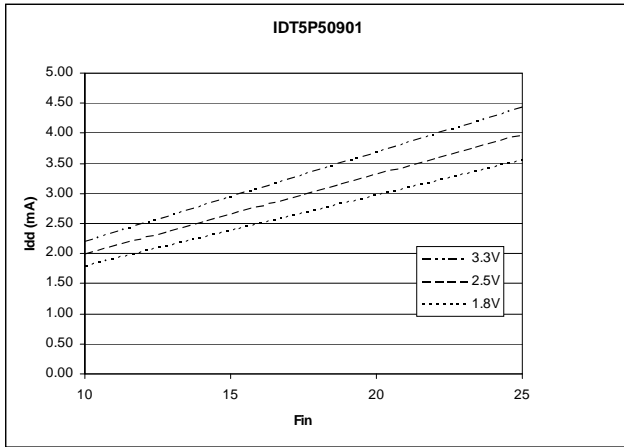
Unless stated otherwise, **VDD = 2.5 V ±10%**. Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------|--------------------------|------------------|------|-----------|-------|
| Operating Voltage | VDD | | 2.25 | 2.5 | 2.75 | V |
| Input High Voltage | V _{IH} | ICLK, S2:S0 | VDD x 0.8 | | VDD + 0.3 | V |
| Input Low Voltage | V _{IL} | ICLK, S2:S0 | GND | | VDD x 0.2 | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | VDD x 0.9 | VDD | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25 mA | | GND | VDD x 0.1 | V |
| IDD | | No load | See table page 6 | | | |
| Input Capacitance | | | | 5 | | pF |
| Load Capacitance | | | | 5 | | pF |
| Internal Pull-down Resistor | R _{PD} | S1:S0 | | 200 | 260 | kΩ |

Unless stated otherwise, **VDD = 3.3 V ±10%**. Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------|--------------------------|------------------|------|-----------|-------|
| Operating Voltage | VDD | | 2.97 | 3.3 | 3.63 | V |
| Input High Voltage | V _{IH} | ICLK, S2:S0 | VDD x 0.8 | | VDD + 0.3 | V |
| Input Low Voltage | V _{IL} | ICLK, S2:S0 | GND | | VDD x 0.2 | V |
| Output High Voltage | V _{OH} | I _{OH} = -33 mA | VDD x 0.9 | VDD | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 33 mA | | GND | VDD x 0.1 | V |
| IDD | | No load | See table page 6 | | | |
| Input Capacitance | | | | 5 | | pF |
| Load Capacitance | | | | 5 | | pF |
| Internal Pull-down Resistor | R _{PD} | S1:S0 | | 200 | 260 | kΩ |

Operational IDD



AC Electrical Characteristics

Unless stated otherwise, VDD = 1.8 V ±0.1 V, 2.5 V ±10% or 3.3 V ±10%. Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|-----------------|----------------------------------|------|------|------|-------|
| Output Clock Duty Cycle | | | 45 | 50 | 55 | % |
| | | 1.8V ±0.1V, >130MHz | 40 | 50 | 60 | |
| Output Rise Time | t _{OR} | 20% to 80%, Note 1 | | 1.2 | | ns |
| Output Fall Time | t _{OF} | 80% to 20%, Note 1 | | 1.2 | | ns |
| Spread Spectrum Modulation Rate | | 10 to 25 MHz input (IDT5P50901) | 27 | | 67.5 | kHz |
| | | 20 to 50 MHz input (IDT5P50902) | 27 | | 67.5 | kHz |
| | | 40 to 100 MHz input (IDT5P50903) | 27 | | 67.5 | kHz |
| | | 80 to 170 MHz input (IDT5P50904) | 27 | | 57.3 | kHz |
| Jitter Cycle to Cycle | | Cycle to cycle jitter | | 150 | | ps |
| Output Settling Time | | Note 2 | | | 3.0 | ms |

Note 1: Measured with 5 pF load

Note 2: Time between VDD rising above minimum operating voltage and stable frequency output

Package Outline and Package Dimensions (8-pin DFN 2x2mm, 0.5mm pitch)

Package dimensions are kept current with JEDEC Publication No. 95,



| Symbol | Millimeters | |
|----------------|----------------|------|
| | Min | Max |
| A | 0.80 | 1.00 |
| A1 | 0 | 0.05 |
| A3 | 0.20 Reference | |
| b | 0.20 | 0.30 |
| N | 8 | |
| N _D | 4 | |
| N _E | 0 | |
| D | 2.00 BASIC | |
| E | 2.00 BASIC | |
| e | 0.50 BASIC | |
| D2 | 1.05 | 1.25 |
| E2 | 0.45 | 0.65 |
| L | 0.20 | 0.40 |
| aaa | 0.15 | |
| bbb | 0.10 | |
| ccc | 0.10 | |

Marking Diagram (8DFN)

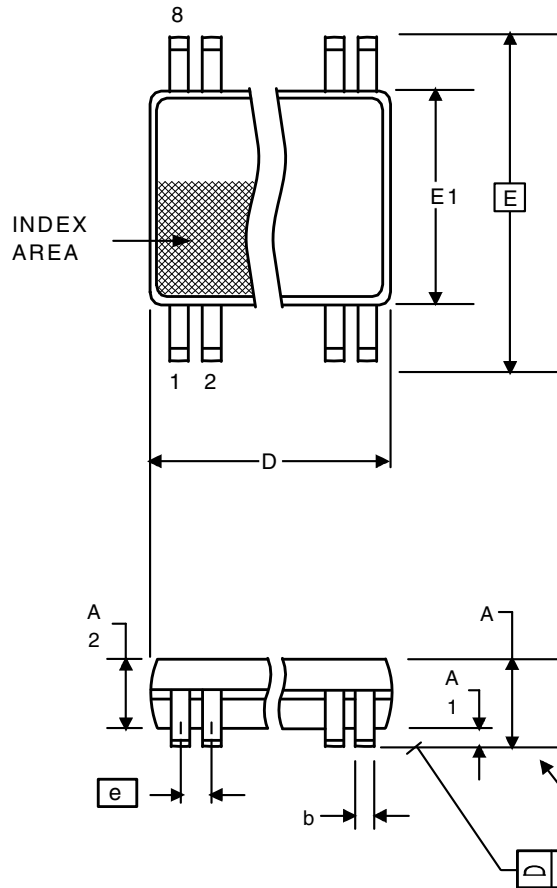


Notes:

- ##### is the last four numbers of the lot number.
- Dot indicates pin 1.
- “G” designates Pb (lead) free package.

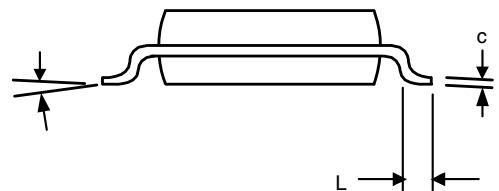
Package Outline and Package Dimensions (8-pin MSOP, 3.00 mm Body)

Package dimensions are kept current with JEDEC Publication No. 95

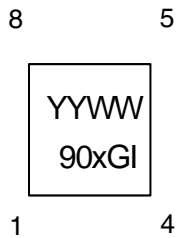


| Symbol | Millimeters | | Inches* | |
|----------|-------------|------|--------------|-------|
| | Min | Max | Min | Max |
| A | -- | 1.10 | -- | 0.043 |
| A1 | 0 | 0.15 | 0 | 0.006 |
| A2 | 0.79 | 0.97 | 0.031 | 0.038 |
| b | 0.22 | 0.38 | 0.008 | 0.015 |
| C | 0.08 | 0.23 | 0.003 | 0.009 |
| D | 3.00 BASIC | | 0.118 BASIC | |
| E | 4.90 BASIC | | 0.193 BASIC | |
| E1 | 3.00 BASIC | | 0.118 BASIC | |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.40 | 0.80 | 0.016 | 0.032 |
| α | 0° | 8° | 0° | 8° |
| aaa | - | 0.10 | - | 0.004 |

*For reference only. Controlling dimensions in mm.



Marking Diagram (8 MSOP)



Notes:

1. YYWW is the assembly date code.
2. Dot indicates pin 1.
3. "G" designates Pb (lead) free package.
4. "I" designates industrial temperature range.

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|---------------|--------------------|------------|------------------|
| 5P50901NBSG18 | see pages 7,8 | Tape and Reel | 8-pin DFN | -40° C to +85° C |
| 5P50901DVS18 | | Tube | 8-pin MSOP | -40° C to +85° C |
| 5P50901DVS18 | | Tape and Reel | 8-pin MSOP | -40° C to +85° C |
| 5P50902NBSG18 | | Tape and Reel | 8-pin DFN | -40° C to +85° C |
| 5P50902DVS18 | | Tube | 8-pin MSOP | -40° C to +85° C |
| 5P50902DVS18 | | Tape and Reel | 8-pin MSOP | -40° C to +85° C |
| 5P50903NBSG18 | | Tape and Reel | 8-pin DFN | -40° C to +85° C |
| 5P50903DVS18 | | Tube | 8-pin MSOP | -40° C to +85° C |
| 5P50903DVS18 | | Tape and Reel | 8-pin MSOP | -40° C to +85° C |
| 5P50904NBSG18 | | Tape and Reel | 8-pin DFN | -40° C to +85° C |
| 5P50904DVS18 | | Tube | 8-pin MSOP | -40° C to +85° C |
| 5P50904DVS18 | | Tape and Reel | 8-pin MSOP | -40° C to +85° C |

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

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Revision History

| Rev. | Date | Originator | Description of Change |
|------|----------|------------|--|
| A | 6/28/11 | R. Willner | Initial release. |
| B | 6/30/11 | R. Willner | Correct modulation rate on 5P50904, rise/fall time definition. |
| C | 07/29/11 | R. Willner | Added "Internal Pull-down Resistor" spec to DC char tables |
| D | 10/07/11 | R. Willner | Correct typographical errors. |
| E | 05/14/12 | R. Willner | Changed max Supply Voltage VDD rating from 7.0V to 5.0V |
| F | 08/21/12 | R. Willner | 1. Changed "Output High/Low Voltage" specs; conditions and min/max values for 1.8V DC electrical characteristics 2. Added an additional line for "Output Clock Duty Cycle" in AC char table to include conditions and values for 1.8V |

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