

ZXMC3F31DN8

30V SO8 Complementary dual enhancement mode MOSFET

Summary

Device	$V_{(BR)DSS}$ (V)	Q_G (nC)	$R_{DS(on)}$ (Ω)	I_D (A)
Q1	30	12.9	0.024 @ $V_{GS} = 10V$	7.3
			0.039 @ $V_{GS} = 4.5V$	5.7
Q2	-30	12.7	0.045 @ $V_{GS} = -10V$	5.3
			0.080 @ $V_{GS} = -4.5V$	4



Description

This new generation Trench MOSFET from Zetex has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance making it ideal for power management and battery charging functions.

Features

- Low on-resistance
- 4.5V gate drive capability
- Low profile SOIC package

Applications

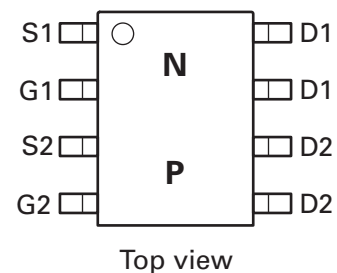
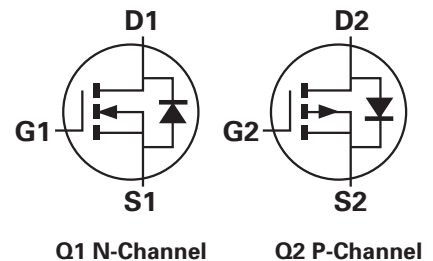
- DC-DC Converters
- SMPS
- Load switching switches
- Motor control
- Backlighting

Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMC3F31DN8TA	7	12	500

Device marking

ZXMC
3F31



ZXMC3F31DN8

Absolute maximum ratings

Parameter	Symbol	N-channel Q1	P-channel Q2	Unit
Drain-Source voltage	V_{DSS}	30	-30	V
Gate-Source voltage	V_{GS}	± 20	± 20	V
Continuous Drain current @ $V_{GS}=10V$; $T_A=25^\circ C$ (b)(d)	I_D	7.3	5.3	A
@ $V_{GS}=10V$; $T_A=70^\circ C$ (b)(d)		5.9	4.3	
@ $V_{GS}=10V$; $T_A=25^\circ C$ (a)(d)		5.7	4.1	
@ $V_{GS}=10V$; $T_A=25^\circ C$ (a)(e)		6.8	4.9	
@ $V_{GS}=10V$; $T_L=25^\circ C$ (f)(d)		7.8	5.7	
Pulsed Drain current (c)	I_{DM}	33	23	A
Continuous Source current (Body diode) (b)(d)	I_S	3.5	3.2	A
Pulsed Source current (Body diode) (c)(d)	I_{SM}	33	23	A
Power dissipation at $T_A=25^\circ C$ (a)(d) Linear derating factor	P_D	1.25		W
		10		mW/ $^\circ C$
Power dissipation at $T_A=25^\circ C$ (a)(e) Linear derating factor	P_D	1.8		W
		14		mW/ $^\circ C$
Power dissipation at $T_A=25^\circ C$ (b)(d) Linear derating factor	P_D	2.1		W
		17		mW/ $^\circ C$
Power dissipation at $T_L=25^\circ C$ (f) (d) Linear derating factor	P_D	2.35		W
		19		mW/ $^\circ C$
Operating and storage temperature range	T_j, T_{stg}	-55 to 150		$^\circ C$

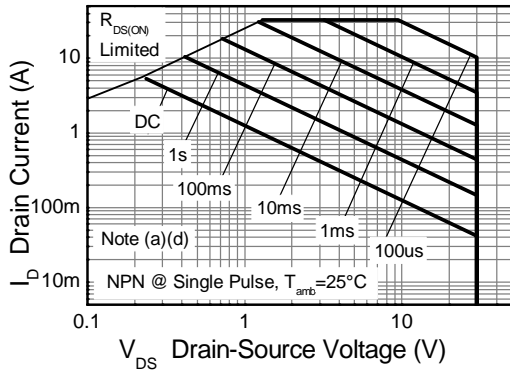
Thermal resistance

Parameter	Symbol	Value	Unit
Junction to ambient (a)(d)	$R_{\theta JA}$	100	$^\circ C/W$
Junction to ambient (a)(e)	$R_{\theta JA}$	70	$^\circ C/W$
Junction to ambient (b)(d)	$R_{\theta JA}$	60	$^\circ C/W$
Junction to lead (f) (d)	$R_{\theta JL}$	53	$^\circ C/W$

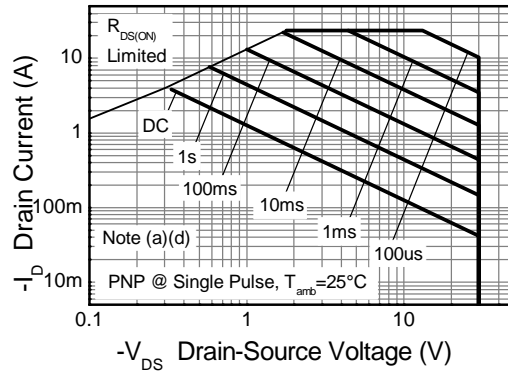
NOTES:

- (a) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions.
- (b) Mounted on FR4 PCB measured at $t \leq 10$ sec.
- (c) Repetitive rating on 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300us – pulse width limited by maximum junction temperature.
- (d) For a device with one active die.
- (e) For a device with two active die running at equal power.
- (f) Thermal resistance from junction to solder-point (at the end of the drain lead).

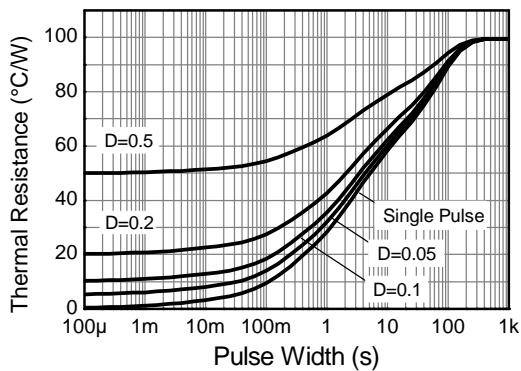
Thermal characteristics



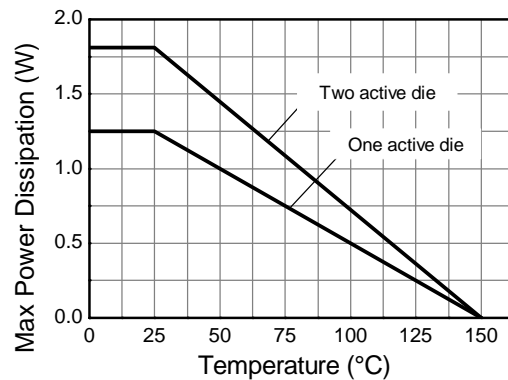
N-channel Safe Operating Area



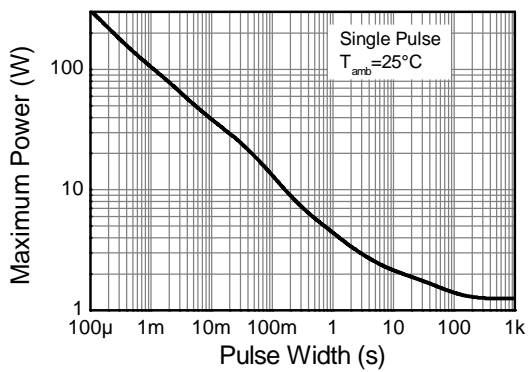
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

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Q1 N-channel electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	30			V	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero Gate voltage Drain current	I_{DSS}			0.5	μA	$V_{DS} = 30\text{V}$, $V_{GS} = 0\text{V}$
Gate-Body leakage	I_{GSS}			100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	1.0		3.0	V	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source on-state resistance (*)	$R_{DS(on)}$			0.024 0.039	Ω	$V_{GS} = 10\text{V}$, $I_D = 7.0\text{A}$ $V_{GS} = 4.5$, $I_D = 6.0\text{A}$
Forward Transconductance (*) (†)	g_{fs}		16.5		S	$V_{DS} = 15\text{V}$, $I_D = 7.0\text{A}$
Dynamic (†)						
Input capacitance	C_{iss}		608		pF	$V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	C_{oss}		132		pF	
Reverse transfer capacitance	C_{rss}		72		pF	
Switching (‡) (†)						
Turn-on-delay time	$t_{d(on)}$		2.9		ns	$V_{DD} = 15\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 1\text{A}$ $R_G \cong 6.0\Omega$,
Rise time	t_r		3.3		ns	
Turn-off delay time	$t_{d(off)}$		16		ns	
Fall time	t_f		8		ns	
Total Gate charge	Q_g		12.9		nC	$V_{DS} = 15\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 7\text{A}$
Gate-Source charge	Q_{gs}		2.5		nC	
Gate-Drain charge	Q_{gd}		2.52		nC	
Source-Drain diode						
Diode forward voltage (*)	V_{SD}		0.82	1.2	V	$I_S = 1.7\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time (‡)	t_{rr}		12		ns	$I_S = 2.2\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge (‡)	Q_{rr}		4.8		nC	

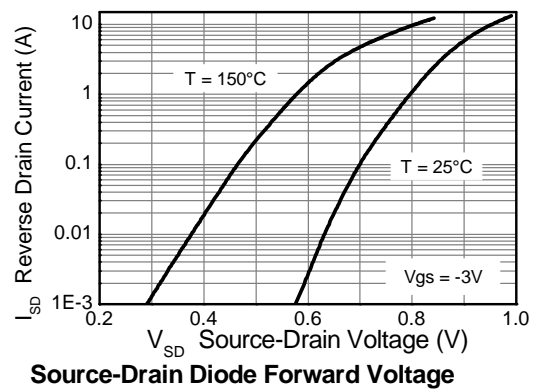
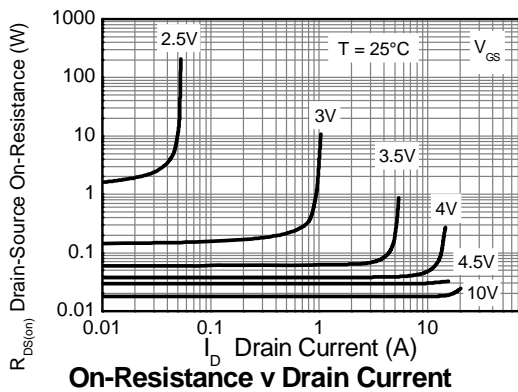
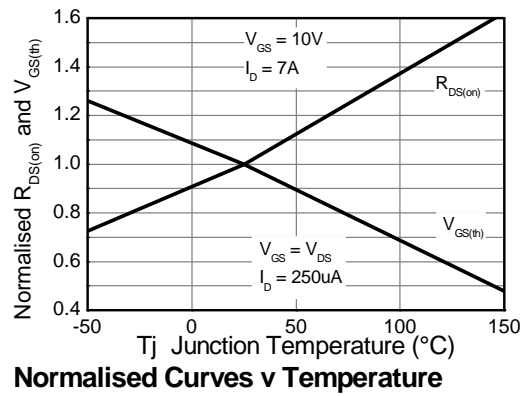
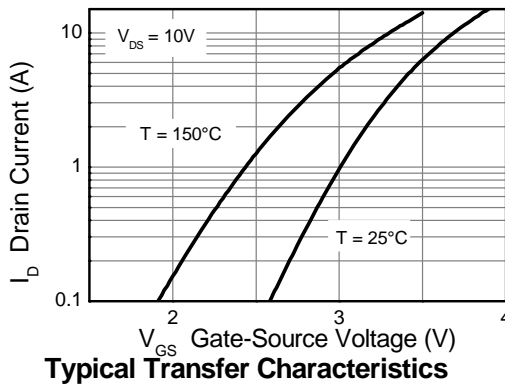
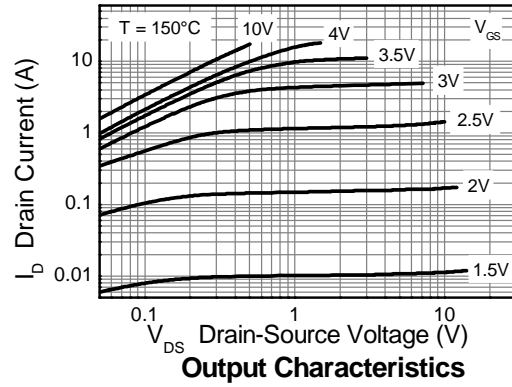
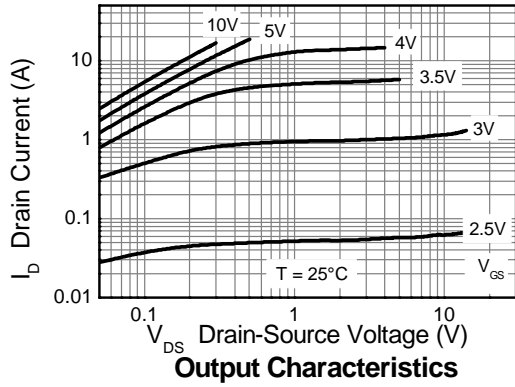
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

(†) Switching characteristics are independent of operating junction temperature.

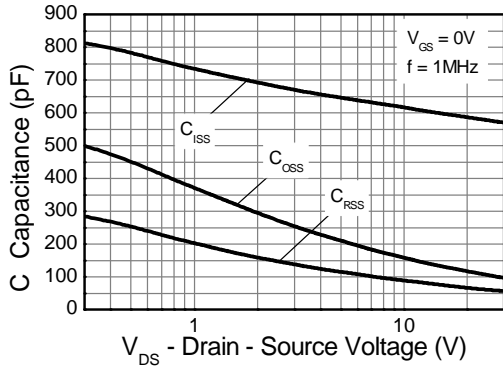
(‡) For design aid only, not subject to production testing

Q1 Typical characteristics

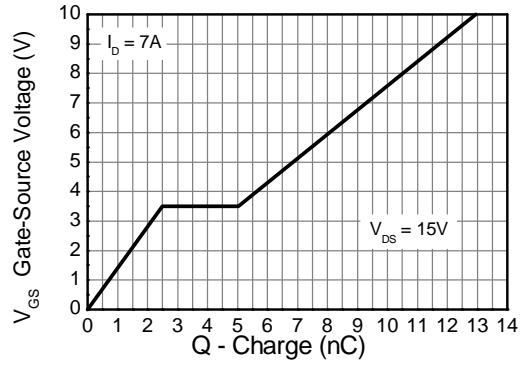


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Q1 Typical characteristics –cntd.

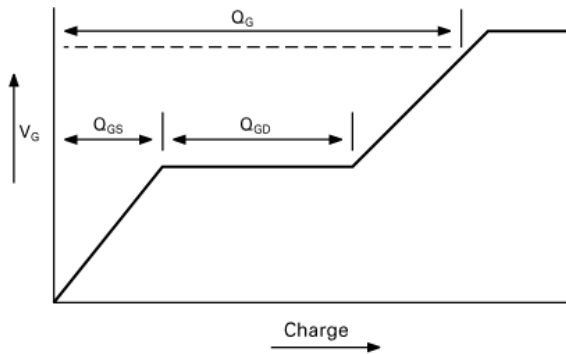


Capacitance v Drain-Source Voltage

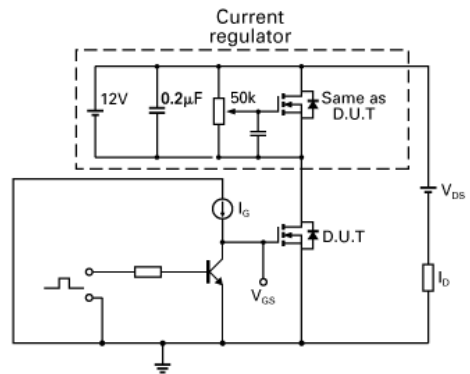


Gate-Source Voltage v Gate Charge

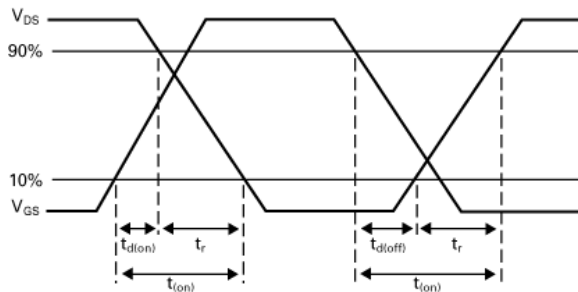
Test circuits



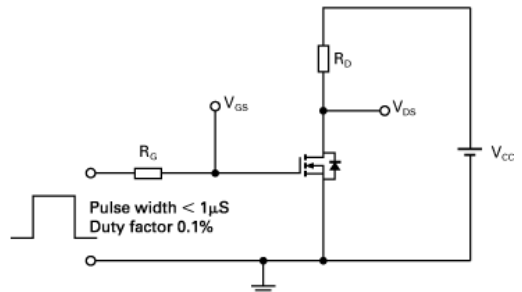
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

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Q2 P-channel electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	-30			V	$I_D = -250\mu\text{A}$, $V_{GS}=0\text{V}$
Zero Gate voltage Drain current	I_{DSS}			-5.0	μA	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$
Gate-Body leakage	I_{GSS}			-100	nA	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	-1.0		-3.0	V	$I_D = -250\mu\text{A}$, $V_{DS}=V_{GS}$
Static Drain-Source on-state resistance (*)	$R_{DS(on)}$			0.045 0.080	Ω	$V_{GS} = -10\text{V}$, $I_D = -5.0\text{A}$ $V_{GS} = -4.5\text{V}$, $I_D = -4.0\text{A}$
Forward Transconductance (*) (†)	g_{fs}		14		S	$V_{DS} = -15\text{V}$, $I_D = -5.0\text{A}$
Dynamic (†)						
Input capacitance	C_{iss}		670		pF	$V_{DS} = -15\text{V}$, $V_{GS}=0\text{V}$ $f=1\text{MHz}$
Output capacitance	C_{oss}		126		pF	
Reverse transfer capacitance	C_{rss}		70		pF	
Switching (‡) (†)						
Turn-on-delay time	$t_{d(on)}$		1.9		ns	$V_{DD} = -15\text{V}$, $V_{GS} = -10\text{V}$ $I_D = -1\text{A}$ $R_G \cong 6.0\Omega$,
Rise time	t_r		3		ns	
Turn-off delay time	$t_{d(off)}$		30		ns	
Fall time	t_f		21		ns	
Total Gate charge	Q_g		12.7		nC	$V_{DS} = -15\text{V}$, $V_{GS} = -10\text{V}$ $I_D = -5\text{A}$
Gate-Source charge	Q_{gs}		2		nC	
Gate-Drain charge	Q_{gd}		2.4		nC	
Source-Drain diode						
Diode forward voltage (*)	V_{SD}		-0.82	-1.2	V	$I_S = -2\text{A}$, $V_{GS}=0\text{V}$
Reverse recovery time (‡)	t_{rr}		16.5		ns	$I_S = -2.1\text{A}$, $di/dt=100\text{A}/\mu\text{s}$
Reverse recovery charge (‡)	Q_{rr}		11.5		nC	

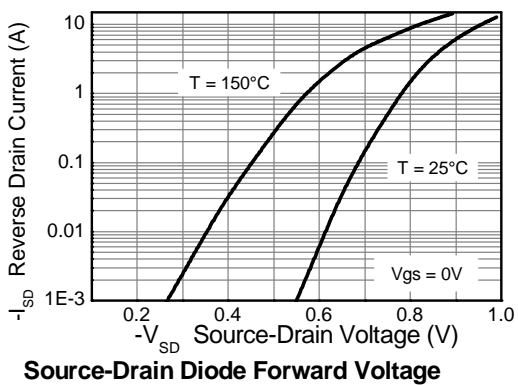
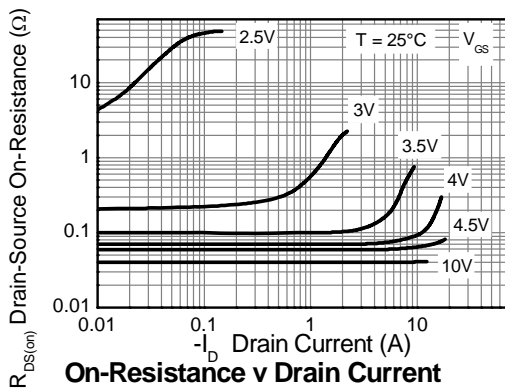
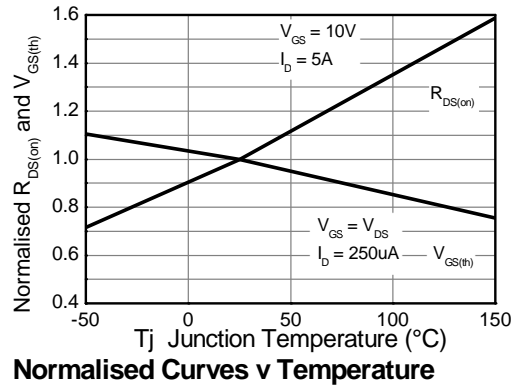
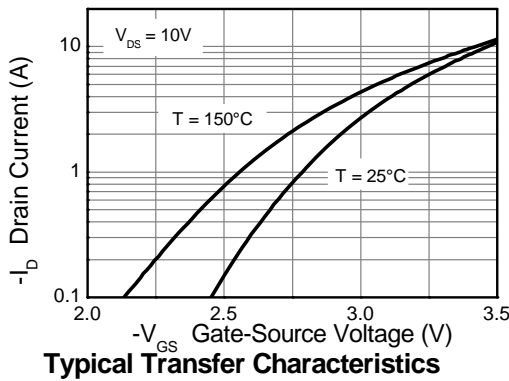
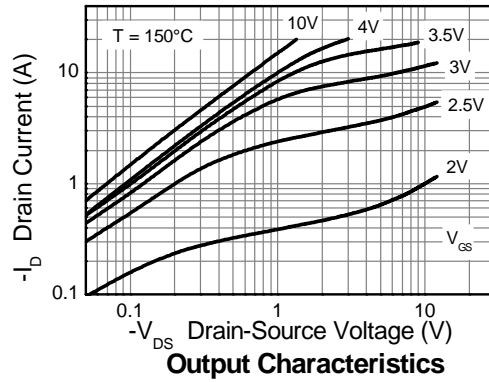
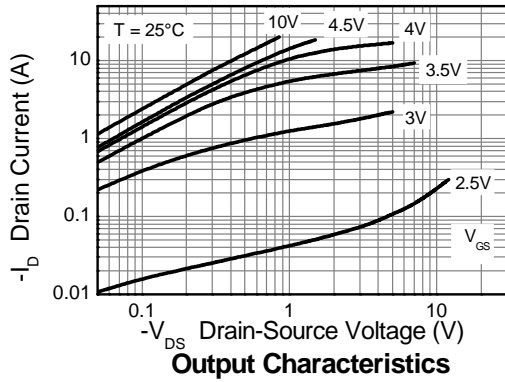
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

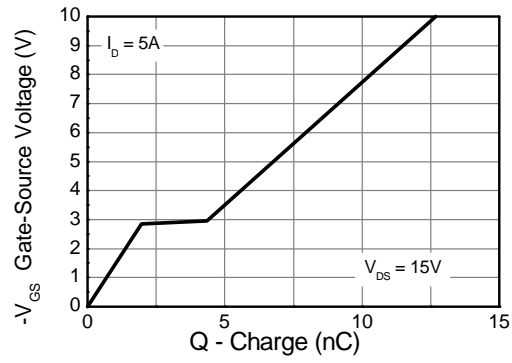
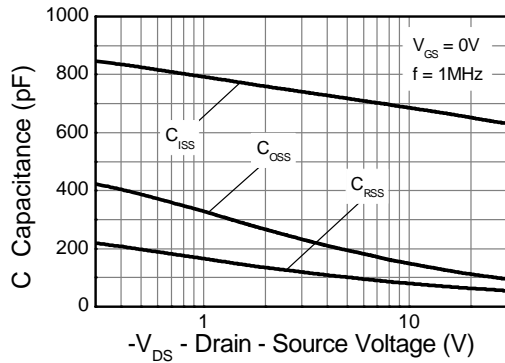
(†) Switching characteristics are independent of operating junction temperature.

(‡) For design aid only, not subject to production testing

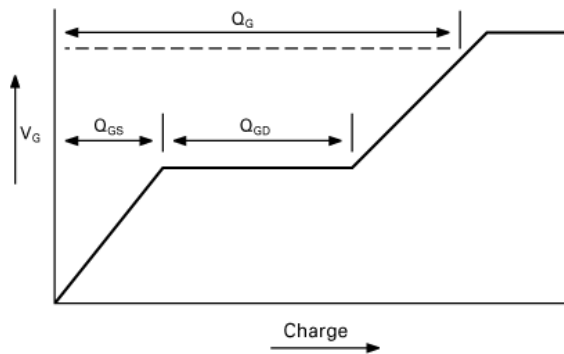
Typical characteristics



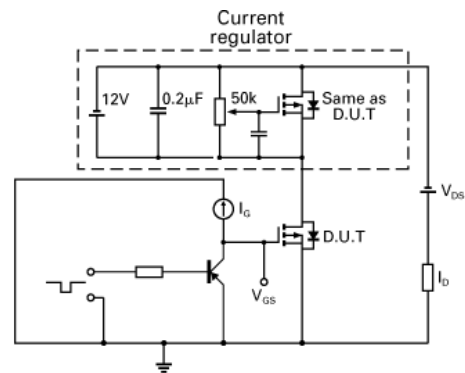
Typical characteristics



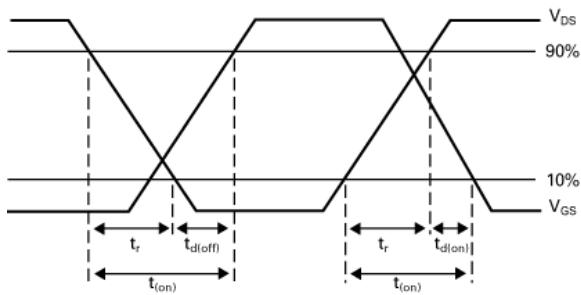
Test circuits



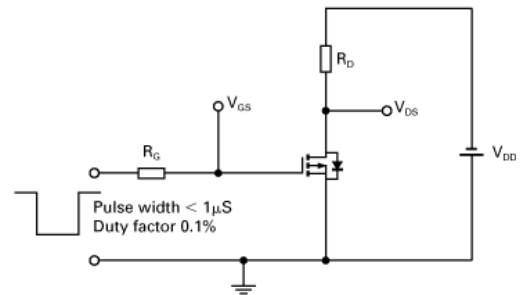
Basic gate charge waveform



Gate charge test circuit



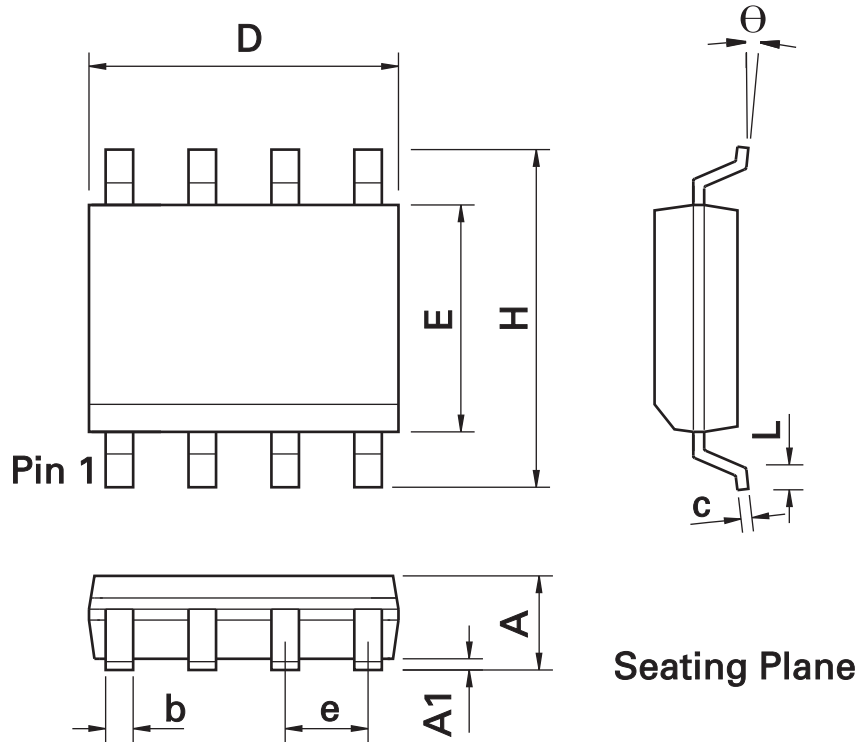
Switching time waveforms



Switching time test circuit

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Package outline SO8



SO8 Package Information

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	U	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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"Active"	Product status recommended for new designs
"Last time buy (LTB)"	Device will be discontinued and last time buy period and delivery is in effect
"Not recommended for new designs"	Device is still in production to support existing designs and production
"Obsolete"	Production has been discontinued

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"Provisional version"	This term denotes a pre-release datasheet. It provides a clear indication of anticipated performance. However, changes to the test conditions and specifications may occur, at any time and without notice.
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Diodes Zetex sales offices

Europe	Americas	Asia Pacific	Corporate Headquarters
Zetex GmbH Kustermann-park Balanstraße 59 D-81541 München Germany Telefon: (49) 89 45 49 49 0 Fax: (49) 89 45 49 49 49 europe.sales@zetex.com	Zetex Inc 700 Veterans Memorial Highway Hauppauge, NY 11788 USA Telephone: (1) 631 360 2222 Fax: (1) 631 360 8222 usa.sales@zetex.com	Diodes Zetex (Asia) Ltd 3701-04 Metroplaza Tower 1 Hing Fong Road, Kwai Fong Hong Kong Telephone: (852) 26100 611 Fax: (852) 24250 494 asia.sales@zetex.com	Diodes Incorporated 15660 N. Dallas Parkway Suite 850, Dallas TX75248, USA Telephone (1) 972 385 2810 www.diodes.com

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- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru