XDPL8218 Digital Flyback Controller IC

XDP™ Digital Power

Data Sheet
Revision 1.0

Features

- Single stage flyback controller with ***Power Factor Correction (PFC)***
- ***Secondary Side Regulated (SSR) Constant Voltage (CV)*** output
- Supports universal AC input (90 V_{rms} to 305 V_{rms}) and DC input
- High power quality from 33% to 100% load, with AC input up to 277 V_{rms}
- Typical ***Power Factor (PF)*** > 0.98 and ***Total Harmonic Distortion (THD)*** < 10%
- High efficiency with ***Quasi-Resonant Mode, switching in valley 1 (QRM1)*** at high output power and frequency controlled ***Discontinuous Conduction Mode (DCM)*** at medium output power
- Typical efficiency > 90%
- Low standby power with ***Active Burst Mode (ABM)***
- Typical standby power < 100 mW (under flyback output no load condition)
- Low audible noise in ***ABM***
- Input overvoltage and undervoltage (Brown-in / Brown-out) protection
- Power limitation during brown-out, to better protect primary components from overheating and saturation
- Output power limitation and output undervoltage protection
- Output overvoltage protection and *VCC* overvoltage protection
- Configurable parameters, e.g. brown-out power limitation slope, protection thresholds and reaction (auto-restart / latch-mode)
- Supports design of Class 2 drivers
- Low Bill of Materials

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Potential applications

- Front-stage ***PFC*** converter of the Electronic Control Gear for LED luminaires

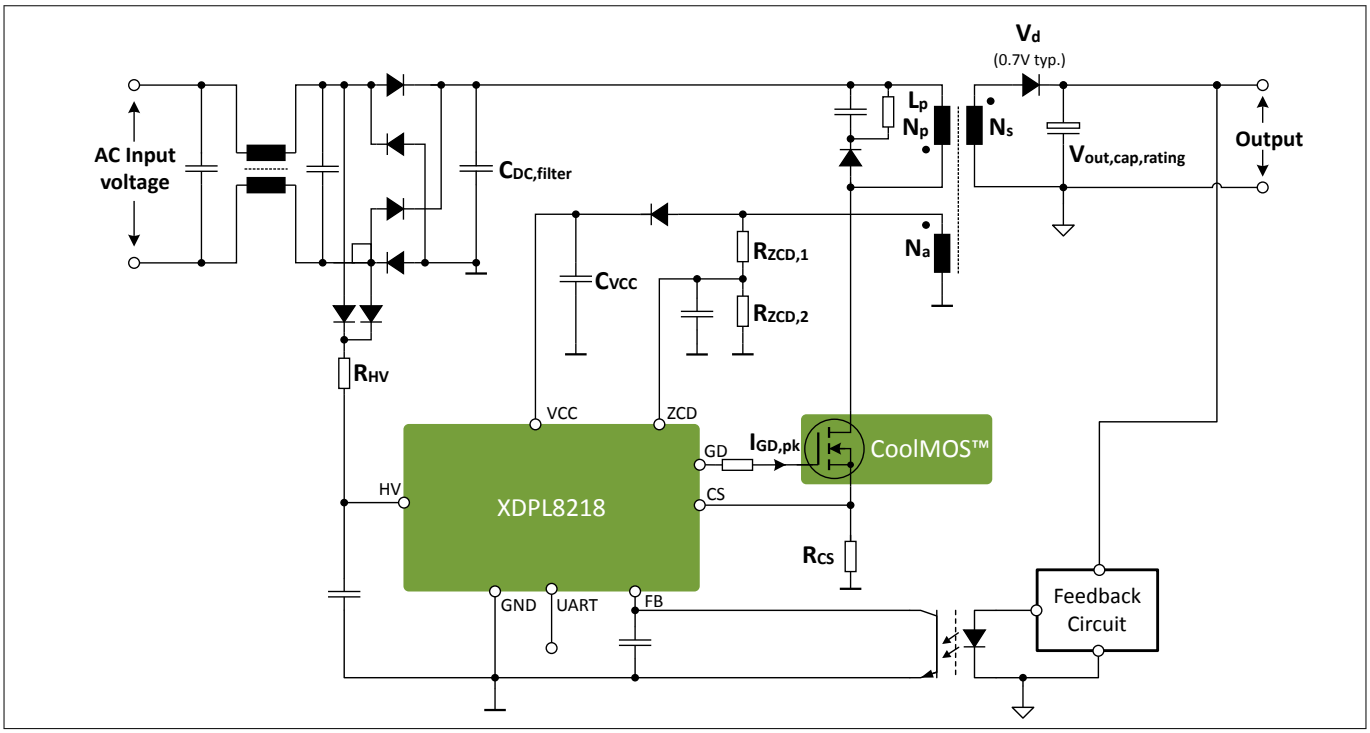

Figure 1 Typical Application for XDPL8218

*Note: The **SSR CV** output in **Figure 1** should not be used to directly drive the LEDs. For LED lighting application, it should be converted to constant current output by a second-stage DC-DC switching or linear regulator.*

Product type	Package	Marking	Firmware version	Ordering code
XDPL8218	PG-DSO-8	L8218	0.1.1.7	SP001707258

Description

The XDPL8218 is a high performance configurable single-stage ***SSR*** flyback controller with high power factor, excellent standby power performance (< 100 mW typ.) and constant voltage output.

The digital core of the XDPL8218 and its advanced control algorithms provide multiple operation modes such as ***QRM1***, ***DCM*** or ***ABM***. In addition, XDPL8218 includes an enhanced ***PFC*** function which can partially compensate the effect of the input capacitance on power factor and harmonic distortion. With this functionality and smooth transition between the operation modes, the controller delivers high efficiency, high power factor and low harmonic distortion over wide load range.

Operating parameters such as protection features are digitally configurable. Infineon offers a user friendly ***Graphic User Interface (GUI)*** for ***Personal Computer (PC)***s, allowing rapid engineering changes without the need for complex component design iterations. Functionality can be defined at the end of the production line. Multiple different power supplies can be built with the same hardware using different XDPL8218 parameter sets.

Note: By default, the configurable parameters of a new XDPL8218 chip from Infineon are empty, so it is necessary to configure them before any application testing.

The system performance and efficiency can be optimized using Infineon *CoolMOS P7 power MOSFETs*.

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1 Pin configuration

Pin assignments and basic pin description information are shown below.

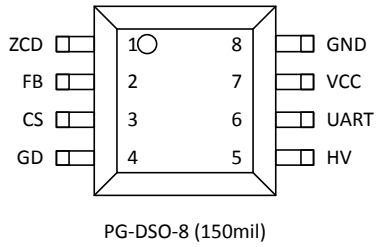

Figure 2 Pinning of XDPL8218

Table 1 Pin definitions and functions

Name	Pin	Type	Function
ZCD	1	I	Zero-crossing detection: The *ZCD* pin is connected to the transformer auxiliary winding via external resistors divider. It is used for zero-crossing detection, primary-side output voltage sensing and input voltage sensing
FB	2	I	Secondary Side Feedback: The *FB* pin is used as a feedback pin for ***SSR***.
CS	3	I	Current sensing: The *CS* pin is used for Flyback MOSFET current sensing via external shunt resistor
GD	4	O	Gate driver: The *GD* pin is used for Flyback MOSFET gate drive control via external series resistor.
HV	5	I	High voltage: The *HV* pin is connected to the rectified input voltage via external series resistor. The *HV* pin is used to charge *VCC* pin voltage during startup and protection, via an internal 600 V startup cell. In addition, it is also used for line synchronization.
UART	6	I/O	***Universal Asynchronous Receiver Transmitter (UART)*** configuration: The *UART* pin is used as the digital interface for IC parameter configuration.
VCC	7	I	Operating voltage supply and sensing
GND	8	-	***Integrated Circuit (IC)*** grounding

2 Functional block diagram

The functional block diagram shows the basic data flow from input pins via signal processing to the output pins.

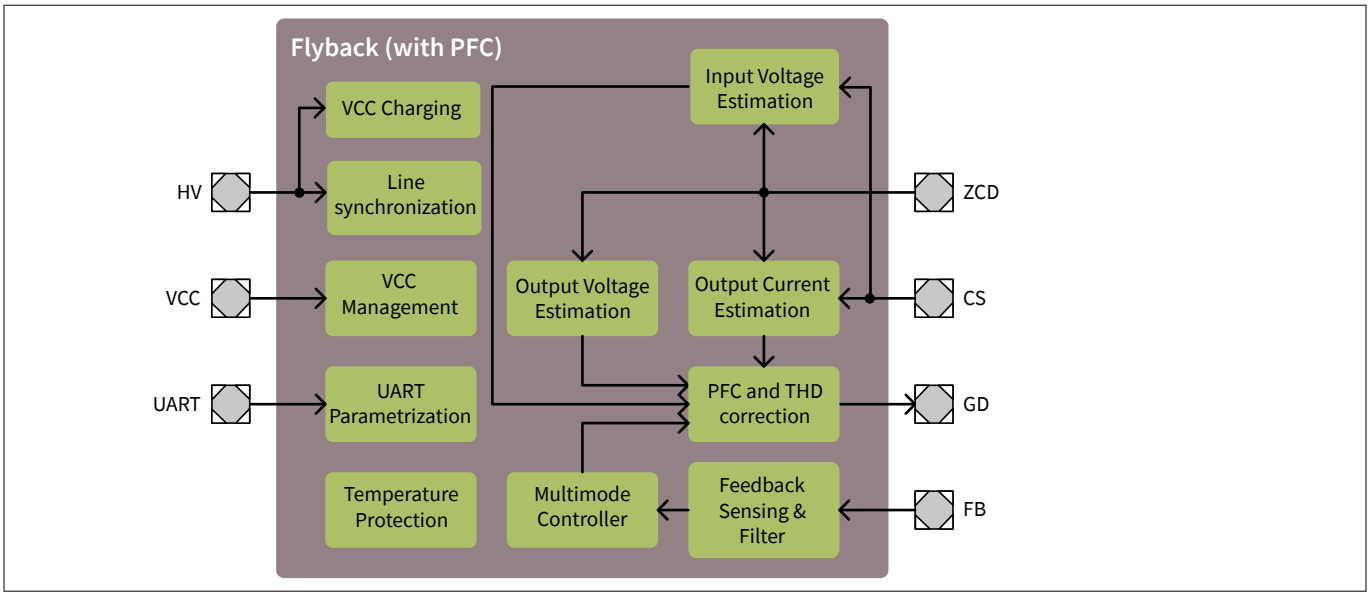

Figure 3 XDPL8218 functional block diagram

3 Functional description

The functional description provides an overview about the integrated functions and features as well as their relationship. The mentioned parameters and equations are based on typical values at T_A = 25°C. The corresponding min. and max. values are shown in the electrical characteristics.

3.1 Regulated mode

In regulated mode, the *FB* pin voltage is periodically sampled and digitally filtered. Based on the filtered feedback voltage $V_{FB,filtered}$ mapping, the mode of operation (***QRM1***, ***DCM*** or ***ABM***) and the respective switching parameters (on-time, minimum switching period, pulse number) are selected. Whenever the regulated mode is entered after the startup phase, the filtered feedback voltage maximum limit $V_{FB,filtered,max}$ ramp is applied initially on the voltage mapping to prevent excessive output rise overshoot.

FB pin voltage sampling

To have a high signal-to-noise ratio, the *FB* pin voltage is sampled instantly after the leading edge blanking time $t_{CS,LEB}$, with the sampling rate based on the mode of operation.

- ***QRM1***/***DCM***:

  With the line synchronization established, the *FB* pin voltage is sampled 64 times per the synchronized AC input half sine wave period. For instance, with AC input frequency of 50 Hz, the synchronized half sine wave period should be approximately 10 ms. If the line synchronization is not established while operating in these modes, for example with DC input, the sampling rate would be 64 times per 9.823 ms.
- ***ABM***:

  During ***ABM*** sleep, the *FB* pin voltage cannot be sampled as the *FB* pin internal pull-up is deactivated in power saving mode PSMD2. During ***ABM*** active time, the pull-up is re-enabled at a timing (based on n_{wakeup} parameter) before the start of both burst pulsing and *FB* pin voltage sampling. If the line synchronization was established before ***ABM*** entering, the sampling rate during burst pulsing would be 64 times per the last synchronized AC input half sine wave period. Otherwise, it would be 64 times per 9.823 ms.

Feedback voltage filtering

The filtering of the sampled feedback voltage depends on the mode of operation:

- ***QRM1***/***DCM***:

  After the controller is synchronized to the AC input half sine wave period for at least a duration based on $n_{notch,blank}$ parameter, the sampled feedback voltage is processed by a digital notch-filter with quality factor based on $N_{quality}$ parameter, to suppress the double AC input frequency component of the feedback voltage. The notch filter has a transfer function of:

$$N(s) = \frac{s^2 + \omega^2}{s^2 + \frac{\omega}{N_{quality}} s + \omega^2} \quad \text{with} \quad \omega = 2\pi \cdot 2f_{line}$$

  Equation 1

  Whenever the condition above for notch filter activation is not met, the sampled feedback voltage is processed by a digital low pass filter. This low pass filter reduces the high frequency component, but cannot suppress the double AC input frequency component of the feedback voltage.
- ***ABM***:

  In this mode, the sampled feedback voltage is processed by a digital low pass filter during the ***ABM*** burst pulsing, to reduce the high frequency component.

Filtered feedback voltage mapping

Figure 4 shows how the filtered feedback voltage $V_{FB,filtered}$ is mapped to the mode of operation (***QRM1***, ***DCM***, ***ABM***) and switching parameters (on-time, minimum switching period, pulse number).

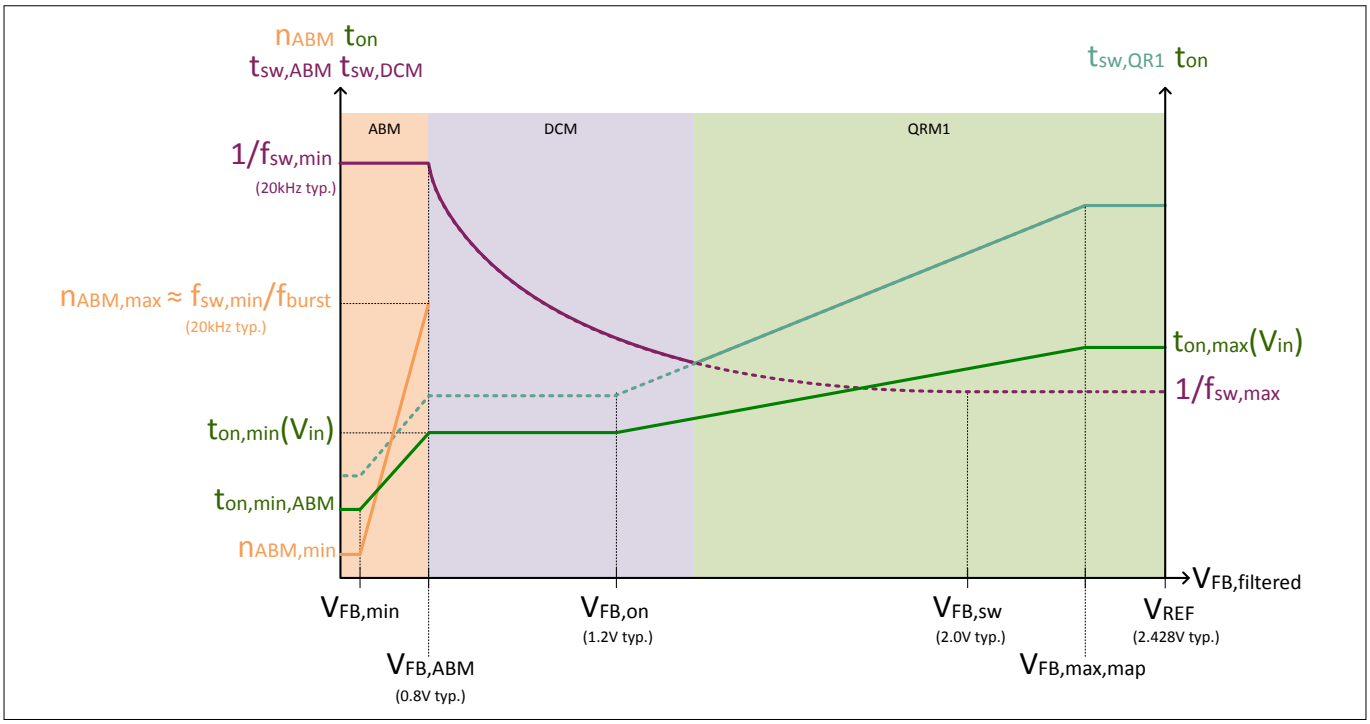

Figure 4 Filtered feedback voltage mapping

*Note: With the enhanced **PFC** feature enabled and $V_{FB,filtered}$ being stable, in **QRM1** and **DCM**, the $V_{FB,filtered}$ mapped on-time is not constant, but modulated with a function based on the estimated input voltage V_{in}, estimated output voltage V_{out}, estimated output current, phase angle and a gain parameter named C_{EMI}. For more details, see **Power factor correction**.*

- ***QRM1***:

  This mode maximizes the efficiency by switching on the MOSFET at the 1st valley of the primary auxiliary winding voltage V_{AUX}, as shown in ***Figure 5***.

  When $V_{FB,filtered}$ is $V_{FB,on}$ (1.2 V) or more, and its corresponding minimum switching period (based on the purple curve in ***Figure 4***) is lower than the system 1st valley switching period $t_{sw,QR1}$ (see cyan curve in ***Figure 4*** as an example), the controller operates in ***QRM1*** and the power transfer is controlled by regulating the on-time.

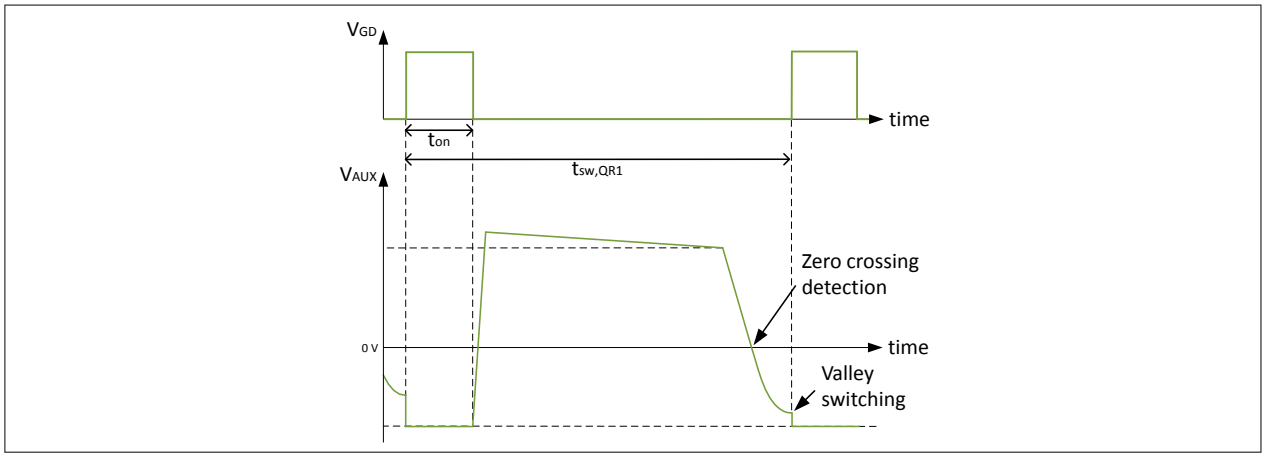

Figure 5 Switching waveforms in QRM1

- ***DCM***:

  This mode switches on the MOSFET after the 1st valley of the primary auxiliary winding voltage V_{AUX}, as shown in ***Figure 6***.

When $V_{FB,filtered}$ is between $V_{FB,ABM}$ (0.8 V) and $V_{FB,on}$ (1.2 V), the ***DCM*** power transfer is controlled by regulating the switching period(frequency), with minimum on-time of $t_{on,min}(V_{in})$ which is adapted based on the estimated input voltage V_{in}.

When $V_{FB,filtered}$ is $V_{FB,on}$ (1.2 V) or more, and its corresponding minimum switching period (based on the purple curve in ***Figure 4***) is higher than the system 1st valley switching period $t_{sw,QR1}$ (see cyan curve in ***Figure 4*** as an example), the controller operates in ***DCM*** and the power transfer is controlled by regulating the on-time and switching period(frequency).

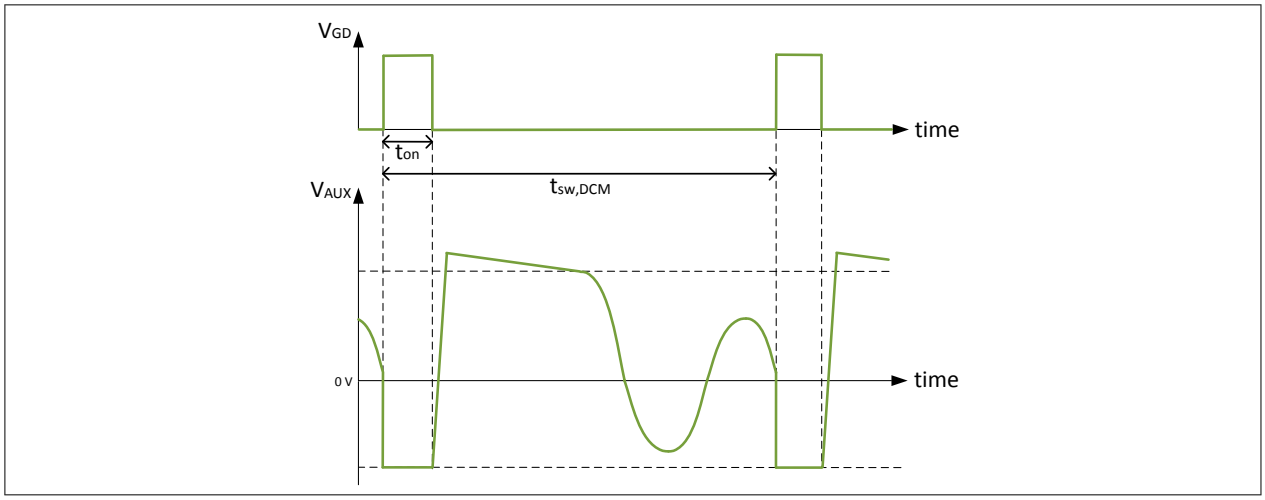

Figure 6 Switching waveforms in DCM

- ***ABM***:

During ***DCM*** or ***QRM1***, if $V_{FB,filtered}$ is below $V_{FB,ABM}$ (0.8 V) for at least a duration based on $t_{blank,ABM}$ parameter, the controller enters ***ABM***. In ***ABM***, the switching period $t_{sw,ABM}$ is fixed to a maximum value (50 µs) based on $f_{sw,min}$ (20 kHz), while the burst frequency is fixed based on f_{burst} parameter to minimize the audible noise.

The power transfer in ***ABM*** is controlled by regulating the pulse number and the on-time, based on $V_{FB,filtered}$ taken at the last pulse of previous burst cycle, as shown in ***Figure 7***. If $V_{FB,filtered}$ exceeds $V_{FB,ABM}$ (0.8 V), the controller enters ***DCM*** or ***QRM1***.

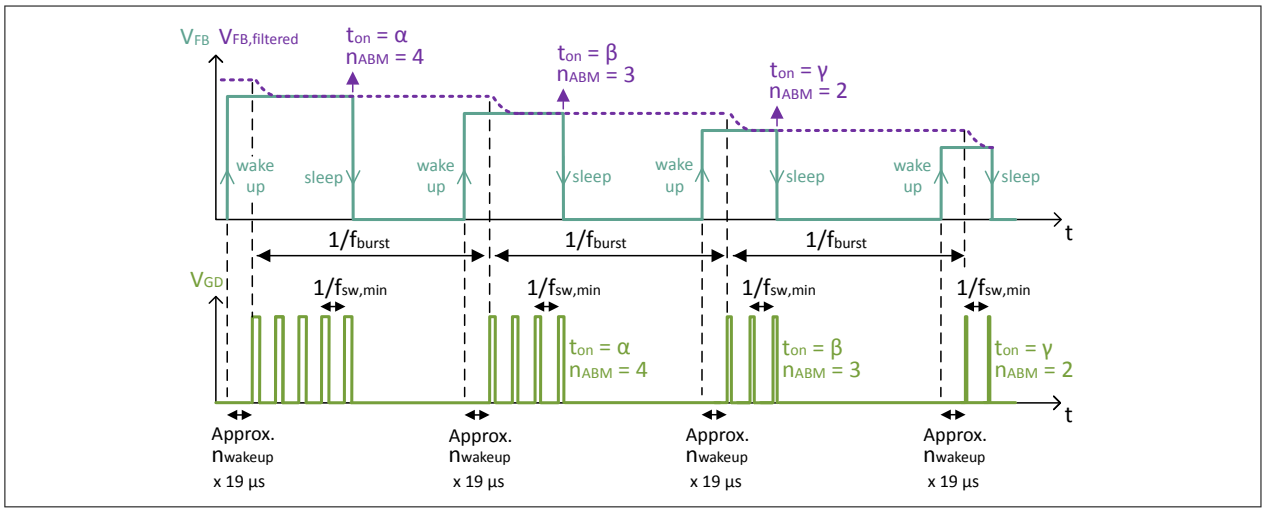

Figure 7 Switching waveforms in ABM

When $V_{FB,filtered}$ is $V_{FB,min}$ or lower, the power transfer is minimum with ABM minimum on-time $t_{on,min,ABM}$ and minimum number of pulses per burst cycle $n_{ABM,min}$ being applied. As $t_{on,min,ABM}$ could be too short to ensure sufficient transformer demagnetization time, the output and input voltages may not be reflected and sensed correctly via *ZCD* pin. Hence, the output voltage protections are not available in ***ABM*** and the input voltage protections can optionally be enabled using $EN_{Vin,ABM}$ parameter.

On-time limits adaptation based on estimated input voltage

In ***DCM*** and ***QRM1***, $t_{on,min,V,out,sense}(V_{in})$ variable is scaled to allow a desired minimum transformer demagnetization time based on $t_{min,demag}$ parameter at the peak of input voltage $V_{in,peak}$ for output voltage sensing up to the output overvoltage level parameter V_{outOV} via *ZCD* pin.

$$t_{on,\,min,\,V,\,out,\,sense}(V_{in}) = t_{min,\,demag} \cdot \frac{N_p}{N_s} \cdot \frac{V_{outOV}}{V_{in,\,peak}}$$

Equation 2

In ***DCM*** and ***QRM1***, the minimum on-time of $t_{on,min}(V_{in})$ in ***Figure 4*** is based on $t_{on,min}$ parameter or $t_{on,min,V,out,sense}(V_{in})$ variable, whichever is higher, as shown in ***Figure 8***.

$$t_{on} > t_{on,\,min}(V_{in}) = \max\left[t_{on,\,min,\,V,\,out,\,sense}(V_{in}),\ t_{on,\,min}\right]$$

Equation 3

In ***DCM*** and ***QRM1***, for estimated input voltage V_{in} between lowest operational input voltage parameter $V_{in,low}$ and input overvoltage protection level parameter V_{inOV}, the maximum on-time of $t_{on,max}(V_{in})$ in ***Figure 4*** is scaled to compensate the influence of input voltage on feedback gain, based on:

$$t_{on} < t_{on,\,max}(V_{in}) = t_{on,\,max,\,at,\,V,\,in,\,low} \cdot \frac{V_{in,\,low}}{V_{in}}$$

Equation 4

Also, in ***DCM*** and ***QRM1***, for estimated input voltage V_{in} below $V_{in,low}$, the maximum on-time of $t_{on,max}(V_{in})$ in ***Figure 4*** is scaled based on the maximum on-time foldback gain parameter $P_{foldback,gain}$, for power limitation during brown-out.

$$t_{on} < t_{on,\,max}(V_{in}) = t_{on,\,max,\,at,\,V,\,in,\,low} \cdot \left(1 - P_{foldback,\,gain} \cdot \frac{V_{in,\,low} - V_{in}}{V_{in,\,low}}\right)$$

Equation 5

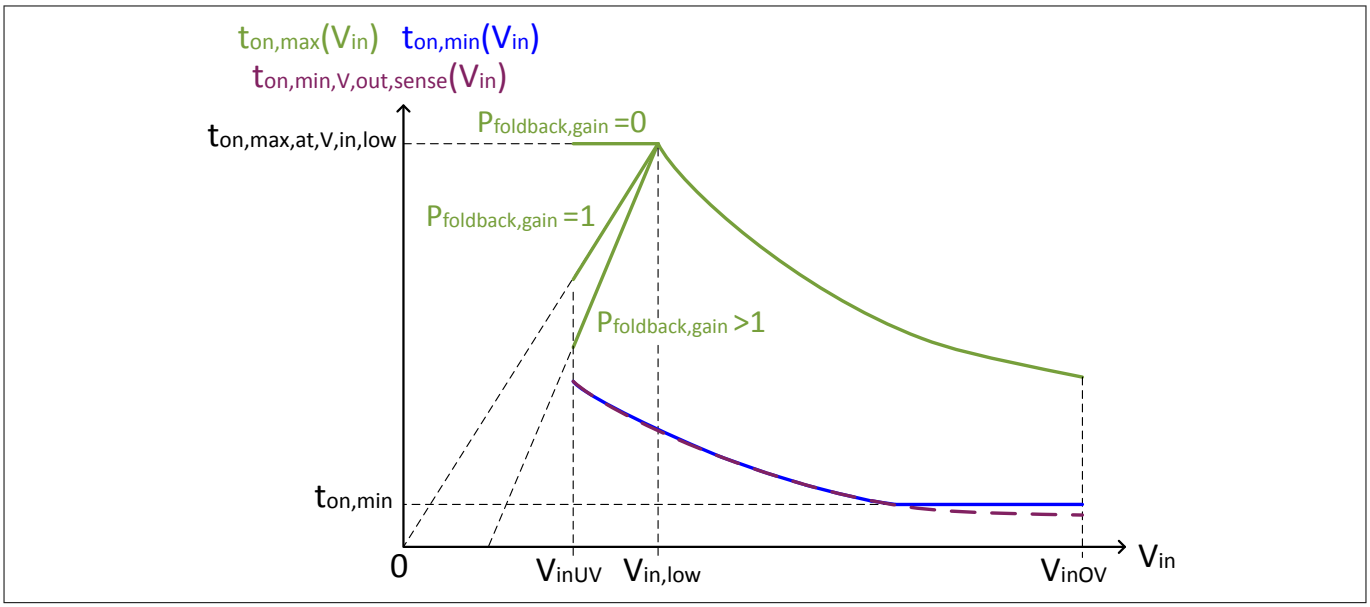

Figure 8 On-time limit adaptation based on estimated input voltage

Note: *$t_{on,min}(V_{in})$ and $t_{on,max}(V_{in})$ are adapted once per half sine wave period. The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operation conditions, as explained in **Line synchronization**.*

Minimum switching period based on filtered feedback voltage

In ***DCM*** and ***QRM1***, the minimum switching period or maximum switching frequency is not constant but dependent on the filtered feedback voltage $V_{FB,filtered}$, as shown in the purple curve in ***Figure 4***. $f_{sw,max}$ parameter denotes the maximum switching frequency when $V_{FB,filtered}$ is same as or higher than than $V_{FB,sw}$ (2.0 V).

When $V_{FB,filtered}$ is increased from $V_{FB,ABM}$ (0.8 V) to $V_{FB,sw}$ (2.0 V), the minimum switching period reduces from $1/f_{sw,min}$ (50 µs) to $1/f_{sw,max}$. During this change, the ***DCM*** switching period $t_{sw,DCM}$ follows the minimum switching period, and the transition from ***DCM*** to ***QRM1*** occurs when the minimum switching period becomes lower than the system 1^{st} valley switching period $t_{sw,QR1}$.

MOSFET maximum current cycle by cycle limit adaptation based on estimated input voltage

For estimated input voltage V_{in} between the lowest operational input voltage parameter $V_{in,low}$ and highest operational input voltage parameter $V_{in,high}$, the regulated mode *CS* voltage level 1 for MOSFET maximum current cycle by cycle limit $V_{OCP1}(V_{in})$ is scaled between $V_{OCP1,at,V,in,low}$ and $V_{OCP1,at,V,in,high}$ parameters based on:

$$V_{OCP1}(V_{in}) = V_{OCP1,at,V,in,low} - \left(V_{OCP1,at,V,in,low} - V_{OCP,at,V,in,high}\right) \cdot \frac{V_{in} - V_{in,low}}{V_{in,high} - V_{in,low}}$$

Equation 6

For estimated input voltage V_{in} below $V_{in,low}$ and above $V_{in,high}$, $V_{OCP1}(V_{in})$ is $V_{OCP1,at,V,in,low}$ and $V_{OCP1,at,V,in,high}$ respectively.

When $V_{FB,filtered}$ is same as or higher than $V_{FB,max,map}$ parameter in ***Figure 4***, the power transfer is maximum, with the primary peak current based on maximum on-time of $t_{on,max}(V_{in})$ or *CS* voltage limit of $V_{OCP1}(V_{in})$.

By configuring $V_{OCP1,at,V,in,high}$ lower than $V_{OCP1,at,V,in,low}$, as shown in ***Figure 9***, the maximum output power can be better limited at high input voltage.

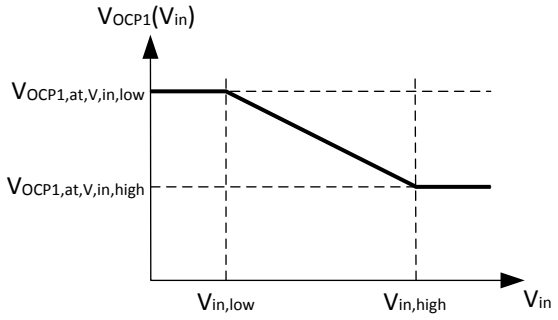

Figure 9 Adaptive CS pin voltage level 1 for MOSFET maximum current cycle by cycle limit based on estimated input voltage

Note: *A typical leading edge blanking time $t_{CS,LEB}$ of 480 ns applies on $V_{OCP1}(V_{in})$.*

Note: *$V_{OCP1}(V_{in})$ is adapted once per half sine wave period. The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operation conditions, as explained in **Line synchronization**.*

Feedback voltage maximum limit

Whenever the regulated mode is entered, the filtered feedback voltage maximum limit $V_{FB,filtered,max}$ is ramped up from $V_{FB,limit,start}$ (1.2 V) to V_{REF} (2.428 V), with incremental voltage step based on $V_{FB,limit,step}$ parameter and time step based on the half sine wave period.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operation conditions, as explained in **Line synchronization**.*

As shown in ***Figure 10***, when $V_{FB,filtered}$ is higher than $V_{FB,filtered,max}$ initially in the regulated mode entering, the feedback voltage mapping is based on $V_{FB,filtered,max}$ ramp, in order to prevent excessive output rise overshoot during startup. When $V_{FB,filtered}$ gets lower than $V_{FB,filtered,max}$, the feedback voltage mapping is then based on $V_{FB,filtered}$.

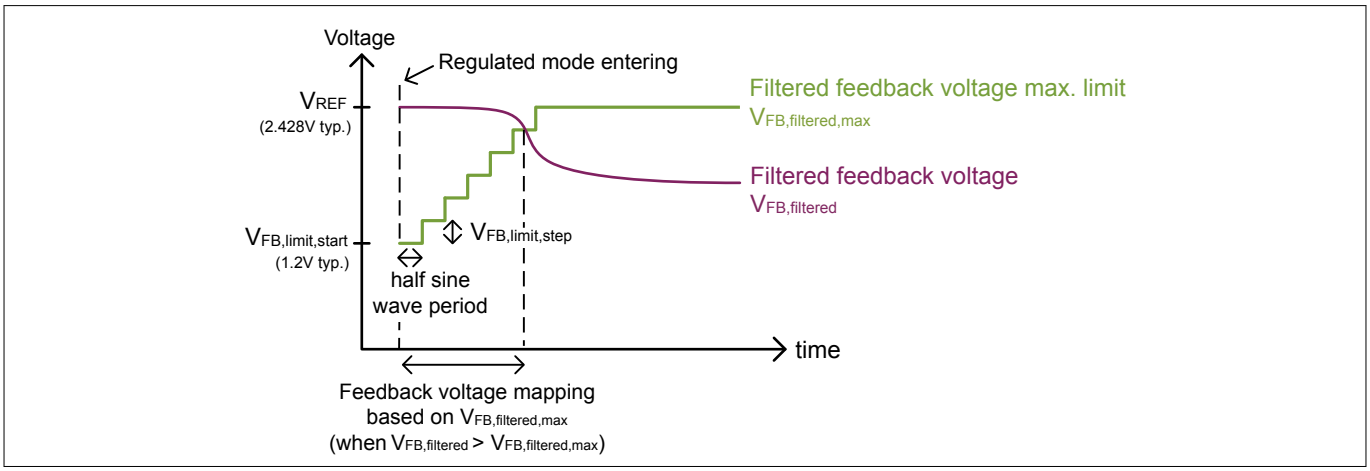

Figure 10 Feedback voltage maximum limit

3.2 Configurable gate voltage rising slope at GD pin

The gate drive peak voltage $V_{GD,pk}$ is 12 V with sufficient Vcc voltage supply. To achieve a good balance of switching loss and ***Electro-Magnetic Interference (EMI)***, the gate voltage rising slope which determines the MOSFET switching on speed can be controlled, by configuring the gate driver peak source current $I_{GD,pk}$ parameter (Configurable range: 30 mA to 180 mA). This saves two components (see $D_{fastoff}$, R_{slowon} in ***Figure 11***), which are conventionally added for the same purpose.

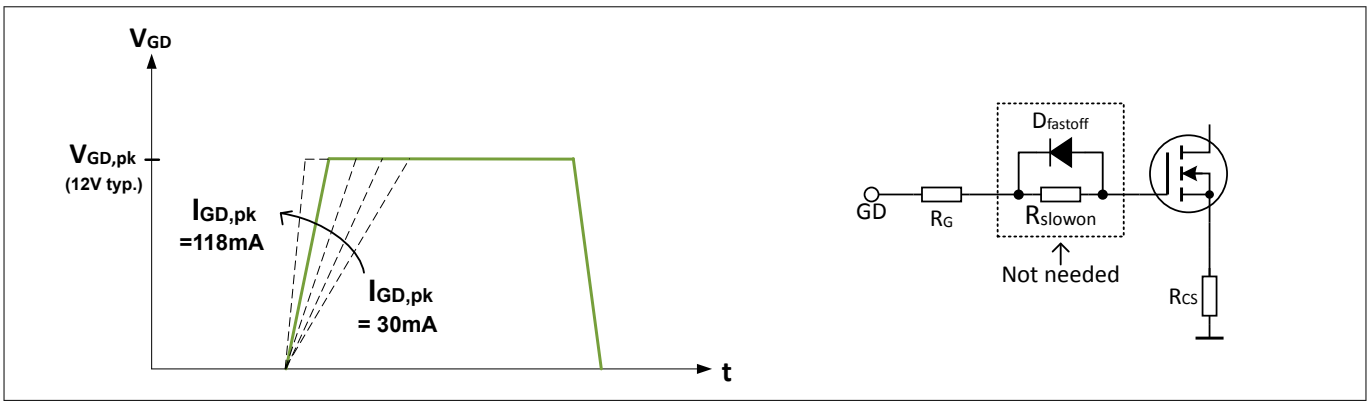

Figure 11 Configurable gate voltage rising slope and component saving

3.3 Startup

The startup phase is entered upon checking the startup conditions (e.g. input voltage, ***IC*** temperature) are within limits. During the startup phase, the soft start phase is initiated and followed by the output charging phase. After the startup phase is ended without any protection triggering, the regulated mode is entered for output regulation based on the feedback voltage mapping.

To estimate the input voltage level before startup, *ZCD* pin signal is measured during a single pulse generated on GD pin. This single pulse has an on-time based on the pre-start *CS* pin maximum voltage limit of $V_{OCP1,init}$ or 8 times of the leading edge blanking time $t_{CS,LEB}$ (e.g. 8 * 480 ns = 3.84 µs typ.). If the estimated input voltage or any other startup conditions are not within limits, startup phase is not entered and this single pulse will be generated again after an auto-restart duration.

The startup phase consists of soft start phase and output charging phase. The soft start phase is to minimize the component stress during startup, while the output charging phase is to fast charge the output voltage for fast *VCC* voltage self supply takeover from the primary auxiliary winding.

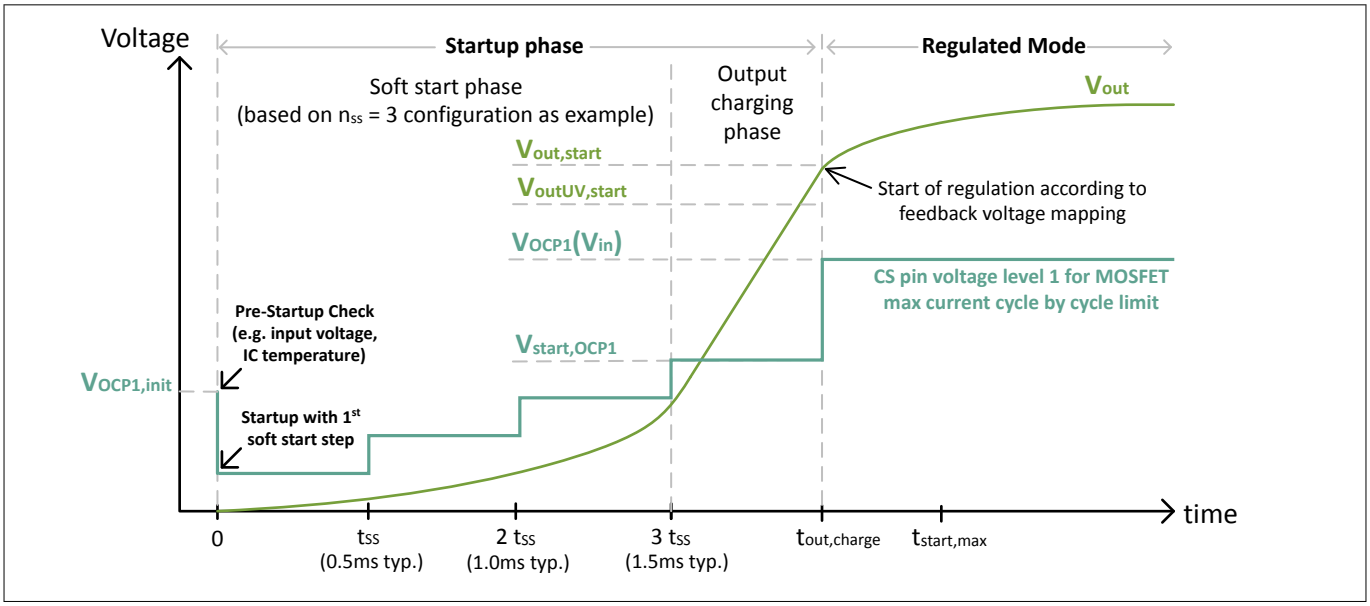

Figure 12 Startup phase with soft start step n_{ss}=3

During soft start phase, the switching frequency is fixed as 20 kHz. The MOSFET current is limited in the first soft start step based on *CS* pin maximum voltage limit of $V_{start,OCP1}/(n_{ss} + 1)$, where $V_{start,OCP1}$ is the parameter for the output charging phase *CS* pin maximum voltage limit and n_{ss} is the parameter for the number of soft start steps. The soft start phase CS pin maximum voltage limit is increased by $V_{start,OCP1}/(n_{ss} + 1)$ after each soft start step until $V_{start,OCP1}$ is reached, and the typical duration of each soft start step is 0.5 ms.

During output charging phase, the output voltage is fast charged with MOSFET switching pulses based on either the output charging phase *CS* pin maximum voltage limit of $V_{start,OCP1}$ or the maximum on time of $t_{on,max}(V_{in})$ in ***QRM1***. To exit the startup phase and enter the regulated mode without triggering the startup output undervoltage protection, the *ZCD* pin estimated output voltage V_{out} has to either reach the output charging voltage set-point of $V_{out,start}$ before the maximum allowable startup phase duration of $t_{start,max}$ is reached (see example in ***Figure 12***), or reach at least the startup output undervoltage protection level of $V_{outUV,start}$ at the timing of $t_{start,max}$.

$t_{start,max}$ parameter can be indirectly configured with *VCC* capacitance parameter C_{VCC}, based on:

$$t_{start,\,max} = 967 \cdot C_{VCC}$$

Equation 7

Note: A typical leading edge blanking time $t_{CS,LEB}$ of 480 ns applies on $V_{OCP1,init}$, $V_{start,OCP1}$ and the CS pin maximum voltage limit for every soft start step starting from $V_{start,OCP1}/(n_{ss} + 1)$.

3.4 Line synchronization

In ***QRM1*** and ***DCM***, the XDPL8218 synchronizes most of its operation to the AC input half sine wave period or the rectified AC input frequency, via the *HV* pin. For instance, based on AC input frequency of 50 Hz, the line synchronization should be based on the rectified AC input frequency of 100 Hz or AC input half sine wave period of 10 ms. Such line synchronization is necessary for the digital notch filter in suppressing the double AC input frequency component of the feedback voltage, to achieve good ***PFC***. It is also used for the enhanced ***PFC*** in compensating the input current displacement caused by the line filter and DC link filter capacitor. If the line synchronization is not established while operating in these modes, for example with DC input or during startup, the controller would synchronize its operation based on an internally preset half sine wave period of approximately 9.823 ms.

Line synchronization is not possible while the controller operates in ***ABM***, due to the sleep mode entering for power saving. In ***ABM***, the controller would synchronize its operation based on an internally preset half sine wave period of approximately 9.823 ms.

***Attention**: For proper line synchronization, the VCC voltage needs to be below V_{SELF}, while the AC input should be a stable sine wave with frequency between 45 Hz and 66 Hz. Additionally, the rectified AC input connected to the HV pin via external resistor also should not have excessive noise.*

3.5 Input voltage and output voltage estimation

XDPL8218 estimates the input voltage and output voltage based on the *ZCD* pin switching signal. As shown in the waveform example in ***Figure 13***, the transformer primary auxiliary winding voltage V_{AUX} contains information on the reflected input voltage and reflected output voltage, which can be measured at *ZCD* pin using a resistor divider.

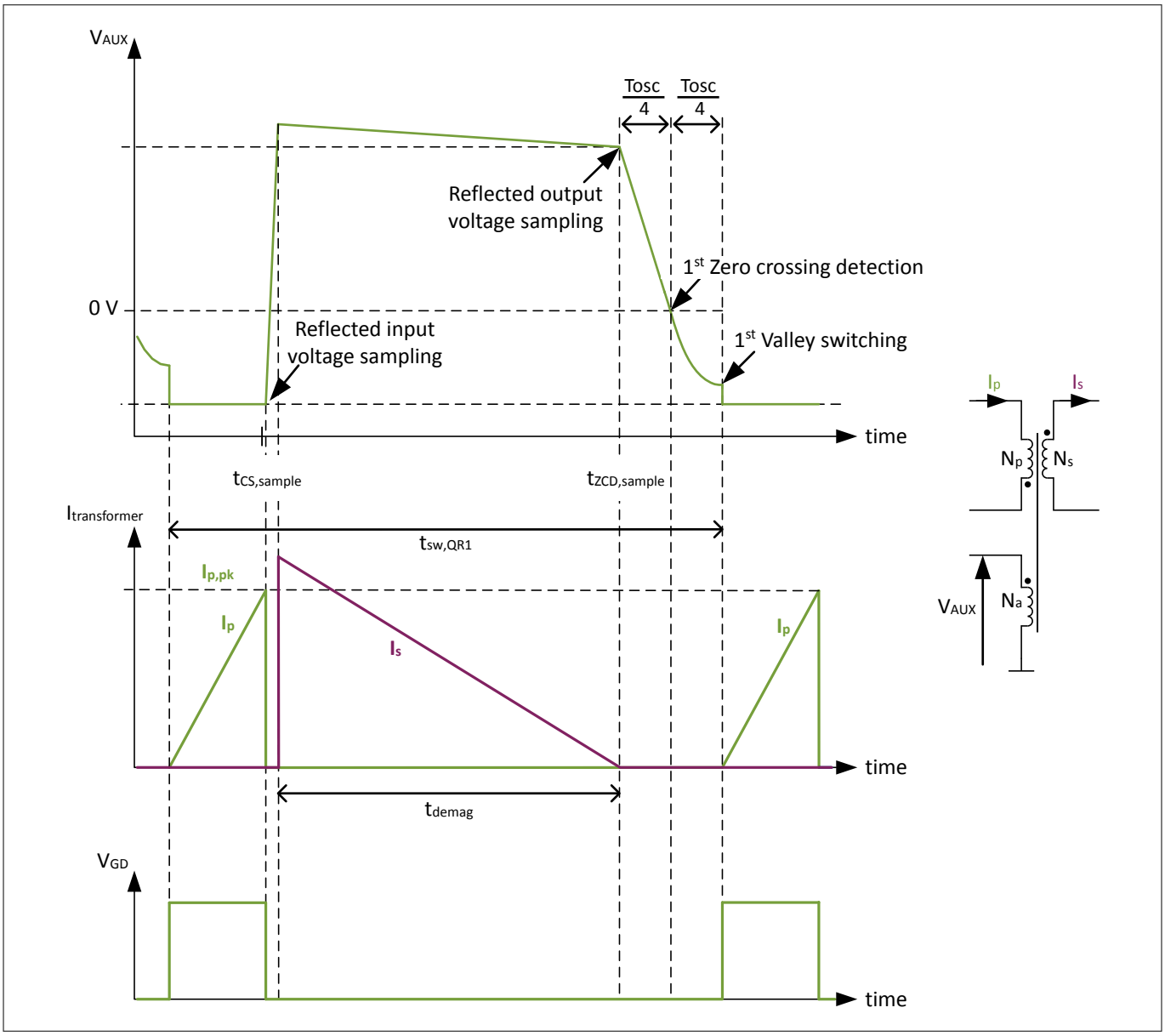

Figure 13 Flyback switching waveform example in QRM1

3.5.1 Output voltage estimation

The output voltage is estimated by sensing the reflected output voltage signal from the transformer primary auxiliary winding voltage V_{AUX}, when the MOSFET is switched off and near the end of transformer demagnetization. A resistor divider with $R_{ZCD,1}$ and $R_{ZCD,2}$ adapts the voltage at *ZCD* pin based on its operational range, while a *ZCD* pin filter capacitor C_{ZCD} is needed for noise filtering, as shown in ***Figure 14***.

Based on the sampled *ZCD* pin voltage $V_{ZCD,SH}$ at the timing of $t_{ZCD,sample}$ shown in ***Figure 13***, which is approximately a quarter of oscillation period ($T_{osc}/4$) before the 1st zero crossing of V_{AUX}, a ratio of the reflected output voltage signal from V_{AUX} is sensed. The interval of each $V_{ZCD,SH}$ sampling is approximately 1/64 of the half sine wave period, while the oscillation period T_{osc} is measured once before startup and updated every 7th half sine wave period after entering the regulated mode.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

Note: *As V_{AUX} zero crossing can only be detected by the **IC** via ZCD pin upon its internal analog delay plus external delay caused by C_{ZCD}, t_{ZCDPD} parameter fine-tuning is needed to compensate such delays, to have the proper timing of $t_{ZCD,sample}$ for output voltage estimation.*

Attention**: **Please note that the transformer demagnetization time t_{demag} has to be longer than 2.0 µs to ensure that the reflected output voltage can be sensed properly at the ZCD pin.

The estimated output voltage V_{out} is based on:

$$V_{out} = V_{ZCD,SH} \cdot \frac{R_{ZCD,1} + R_{ZCD,2}}{R_{ZCD,2}} \cdot \frac{N_s}{N_a} - V_d$$

Equation 8

Where N_s is the transformer secondary main winding turns, N_a is the transformer primary auxiliary winding turns and V_d is the secondary main output diode forward voltage (assumed by the controller as 0.7 V).

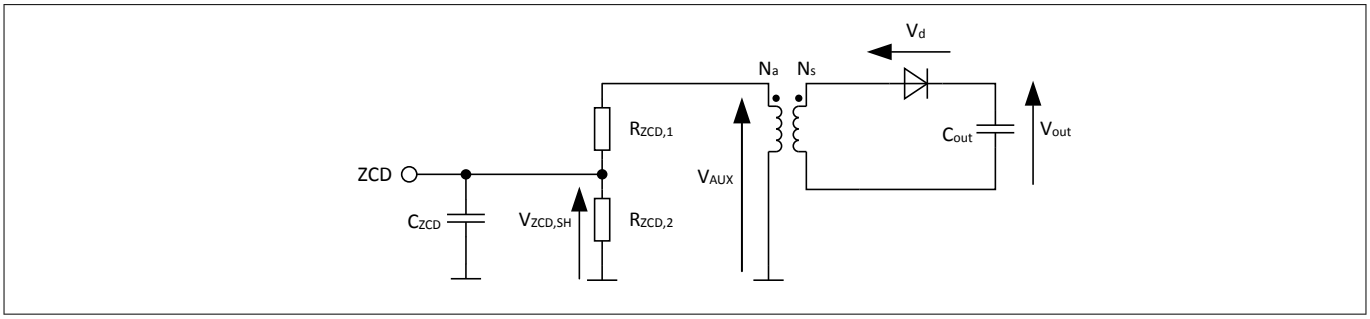

Figure 14 Output voltage estimation based on $V_{ZCD,SH}$

The estimated output voltage V_{out} is used for output voltage protections and the enhanced ***PFC*** (EPFC). Therefore, it is important to ensure that ***IC*** parameters $R_{ZCD,1}$, $R_{ZCD,2}$, N_s and N_a are configured as per the actual system hardware dimensioning.

Attention**: **Output voltage estimation and its related protections are not available while the controller operates in ABM. As an indirect overvoltage protection for the output, the VCC overvoltage protection can be used.

3.5.2 Input voltage estimation

The input voltage is estimated by sensing the reflected input voltage signal from the transformer primary auxiliary winding voltage V_{AUX}, when the MOSFET is switched on. As the reflected input voltage signal is a negative voltage which cannot be sensed directly, the voltage at *ZCD* pin is clamped to a negative voltage of V_{INPCLN}. A resistor divider with $R_{ZCD,1}$ and $R_{ZCD,2}$ adapts $-I_{IV}$ which is the clamping current flowing out of *ZCD* pin, based on its operational range, while a *ZCD* pin filter capacitor C_{ZCD} is needed for noise filtering, as shown in ***Figure 15***.

Based on the sampled clamping current $-I_{IV}$ at the timing of $t_{CS,sample}$ shown in ***Figure 13***, which is at the end of on-time, the reflected input voltage signal from V_{AUX} is sensed. The interval of each $-I_{IV}$ sample is approximately 1/64 of the half sine wave period.

Note: *The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operation conditions, as explained in **Line synchronization**.*

The estimated peak input voltage $V_{in,peak}$ over a half sine wave period is based on:

$$V_{\text{in, peak}} = \max\left\{\frac{N_p}{N_a} \cdot \left[\left(-I_{\text{IV}} - \frac{V_{\text{INPCLN}}}{R_{\text{ZCD, 2}}}\right) \cdot R_{\text{ZCD, 1}} - V_{\text{INPCLN}}\right] + \frac{R_{\text{in}}}{R_{\text{CS}}} \cdot V_{\text{CS, peak}}\right\}$$

Equation 9

Where N_p is the primary main winding turns, N_a is the primary auxiliary winding turns, R_{CS} is the *CS* pin shunt resistor value, $V_{CS,peak}$ is the peak *CS* pin voltage, and R_{in} is the fine-tuning parameter for input voltage sensing accuracy improvement by compensating the switching frequency voltage ripple on $C_{DC,filter}$.

Regardless of the actual input voltage is AC or DC, the estimated input voltage V_{in} in rms value is assumed by the controller as 0.707 of $V_{in,peak}$. The update rate of V_{in} is once per half sine wave period.

$$V_{\text{in}} = 0.707 \cdot V_{\text{in, peak}}$$

Equation 10

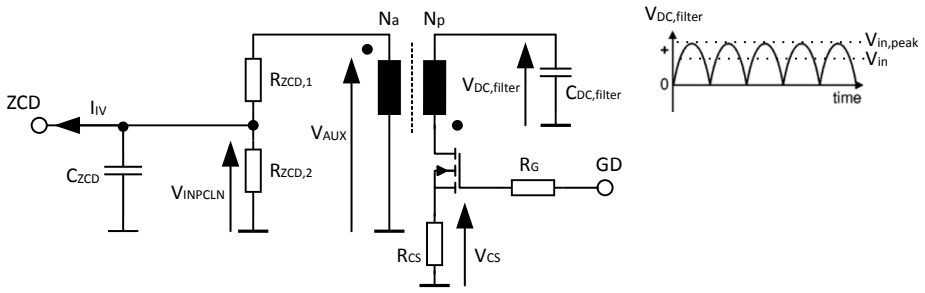

Figure 15 Input voltage estimation based on $-I_{IV}$

The estimated input voltage V_{in} is used for input voltage protections and the enhanced ***PFC*** (EPFC). Therefore, it is important to ensure that ***IC*** parameters $R_{ZCD,1}$, $R_{ZCD,2}$, N_p, N_a and R_{CS} are configured as per the actual system hardware dimensioning.

***Attention**: Input voltage protections in **ABM** can optionally be enabled using $EN_{Vin,ABM}$ parameter.*

3.6 Power factor correction

Upon the line synchronization is established in ***QRM1*** and ***DCM*** for at least a duration based on $n_{notch,blank}$ parameter, the double AC input frequency component of the feedback voltage is suppressed by the digital notch filter, to achieve good ***PFC***, while regulating the output based on Voltage Mode Control. The notch filter quality factor is based on $N_{quality}$ parameter.

For better ***PFC***, the patented enhanced ***PFC*** (EPFC) feature can be enabled by configuring C_{EMI} parameter value above zero and fine-tuning the value, to compensate the input current displacement effect which is mainly caused by the DC link filter capacitor $C_{DC,filter}$. With this feature enabled and $V_{FB,filtered}$ being stable, in ***QRM1*** and ***DCM***, the $V_{FB,filtered}$ mapped on-time is not constant, but modulated with a function based on the estimated input voltage V_{in}, estimated output voltage V_{out}, estimated output current, phase angle and modulation gain of C_{EMI} parameter value.

The enhanced ***PFC*** (EPFC) feature can also be disabled by configuring C_{EMI} parameter as zero.

3.7 Protection features

Protections ensure the operation of the controller under restricted conditions. The protection monitoring signal(s) sampling rate, protection triggering condition(s) and protection reaction are described in this section.

***Attention**: The sampled protection monitoring signal accuracy is subjective to the digital quantization, tolerances of components (including IC) and estimations with indirect sensing (e.g. input and output voltage estimations based on ZCD, CS pin signals), while the protection level triggering accuracy is subjective to the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. reflected output voltage signal cannot be sensed by ZCD pin near AC input phase angle of 0° and 180°) and blanking time.*

3.7.1 Primary MOSFET overcurrent protection

V_{OCP2} denotes the *CS* pin voltage level 2 for primary MOSFET overcurrent protection. Under the single fault condition of shorted primary main winding, the primary MOSFET overcurrent protection is triggered when the *CS* pin voltage exceeds V_{OCP2} for longer than a blanking time based on t_{CSOCP2} parameter. The level of V_{OCP2} is automatically selected out of 0.6 V, 0.8 V, 1.2 V and 1.6 V, whichever is higher than and the closest to the $V_{OCP1,at,V,in,low}$ parameter value.

The reaction of primary MOSFET overcurrent protection is fixed as auto-restart.

3.7.2 Output undervoltage protection

In case of a short or an overload on the output, the output voltage may drop to a low level. The output undervoltage protection can be triggered, if the condition is met by monitoring the estimated output voltage V_{out} based on the *ZCD* pin switching signal (see ***Output voltage estimation*** for details).

$EN_{UVP,Vout}$ parameter refers to the enable switch for the regulated mode output undervoltage protection. In regulated mode, if $EN_{UVP,Vout}$ parameter is enabled and the estimated output voltage V_{out} is lower than V_{outUV} parameter for longer than a blanking time of $t_{VoutUV,blank}$ parameter, the regulated mode output undervoltage protection is triggered. The reaction of regulated mode output undervoltage protection is configurable to either auto-restart or latch mode based on $Reaction_{UVP,Vout}$ parameter.

***Attention**: Regulated mode output undervoltage protection is not available while the controller operates in ABM.*

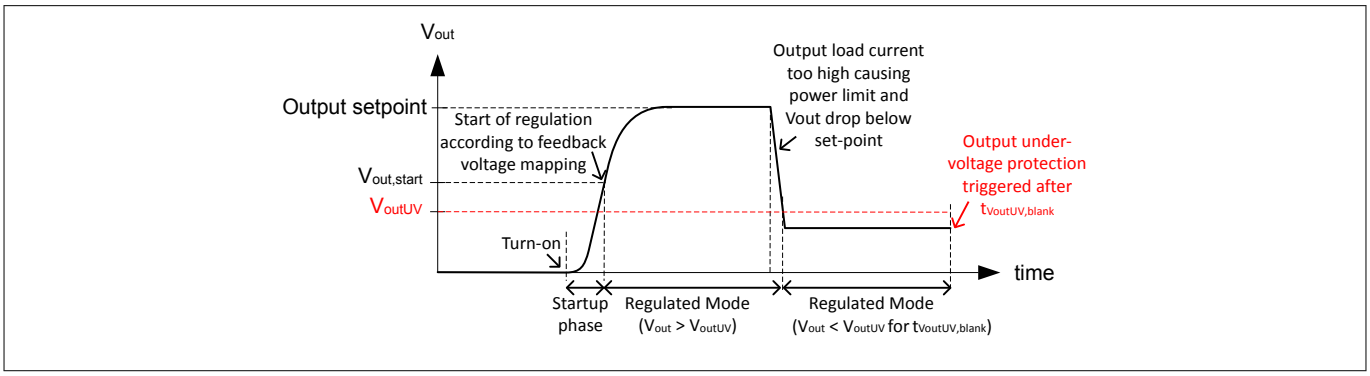

Figure 16 Regulated mode output undervoltage protection

In startup phase, if the estimated output voltage V_{out} is lower than $V_{outUV,start}$ parameter over a timeout period of $t_{start,max}$ parameter, the startup output undervoltage protection is triggered. $t_{start,max}$ parameter refers to the maximum allowable duration of the startup phase, which consists of soft-start phase and output charging phase. It can be indirectly configured with *VCC* capacitance parameter C_{VCC}, based on ***Equation 7***.

The reaction of startup output undervoltage protection is fixed as auto-restart.

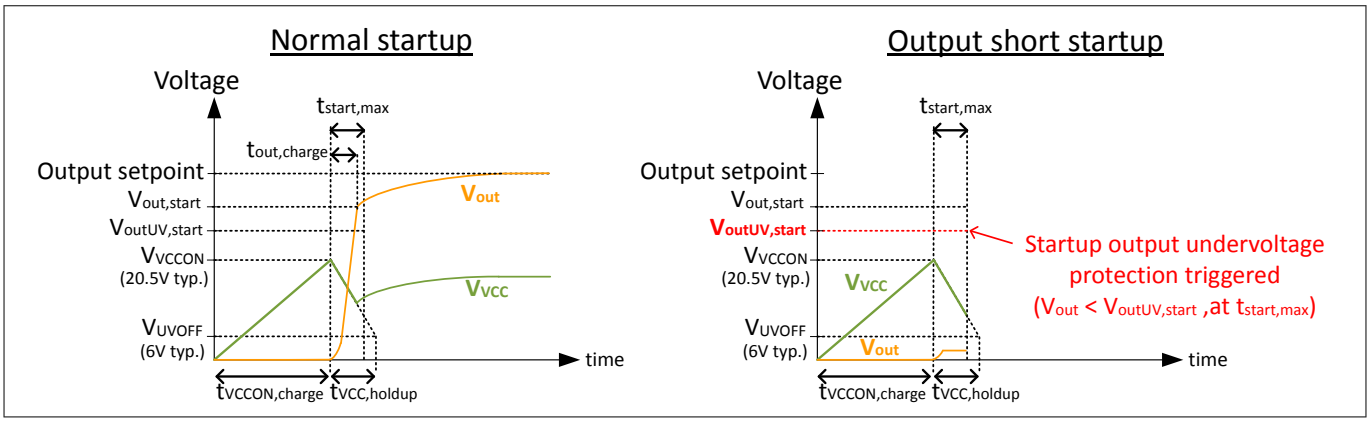

Figure 17 Normal startup and startup output undervoltage (short) protection waveforms

3.7.3 Output overvoltage protection

In case of *FB* pin open, the output voltage may rise to a high level. The output overvoltage protection can be triggered, if the condition is met by monitoring the estimated output voltage V_{out} based on the *ZCD* pin switching signal (see ***Output voltage estimation*** for details).

If the estimated output voltage V_{out} is higher than V_{outOV} for longer than a blanking time, the output overvoltage protection is triggered. The output overvoltage protection blanking time is typically a quarter of the half sine wave period. The reaction of the output overvoltage protection is configurable to auto-restart or latch-mode based on $Reaction_{OVP,Vout}$ parameter.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

Attention**: **Output overvoltage protection is not available while the controller operates in ABM.

Attention**: **It is mandatory to ensure that V_{outOV} is configured well below the actual output capacitor voltage rating $V_{out,cap,rating}$,while the $V_{out,cap,rating}$ is not exceeded in actual testing with all the necessary test conditions. The protection level triggering accuracy is subjective to the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. reflected output voltage signal cannot be sensed by ZCD pin near AC input phase angle of 0° and 180°) and blanking time.

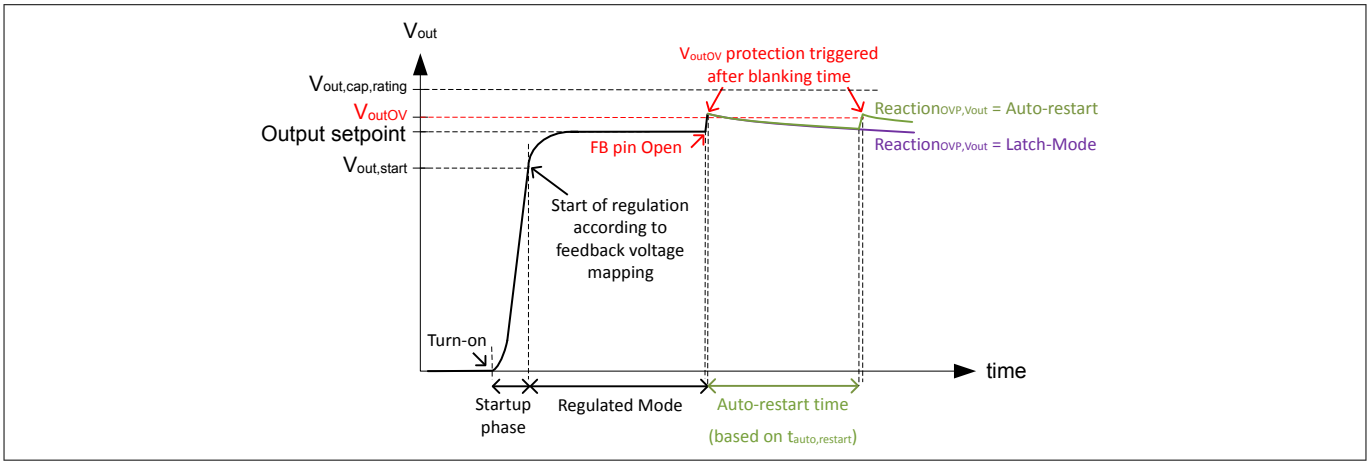

Figure 18 Output overvoltage protection

3.7.4 Transformer demagnetization time shortage protection

In case of insufficient transformer demagnetization time, the reflected output voltage signal cannot be properly sensed via the *ZCD* pin. If such condition presents for longer than 50% of a half sine wave period, the protection will be triggered. The reaction of this protection is fixed as auto-restart.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

Attention**: **Transformer demagnetization time shortage protection is not available while the controller operates in ABM.

3.7.5 Minimum input voltage startup check and input undervoltage protection

By monitoring the estimated input voltage V_{in} based on the *ZCD* pin and *CS* pin switching signals (see ***Input voltage estimation*** for details), the minimum input voltage startup check can be performed, and the input undervoltage protection can be triggered if the condition is met.

$EN_{UVP,In}$ parameter refers to the enable switch for the minimum input voltage startup check (based on $V_{in,start,min}$) and input undervoltage protection (based on V_{inUV}).

Note: $V_{in,start,min}$ parameter refers to the minimum input voltage level for startup, while V_{inUV} parameter refers to the input undervoltage protection level.

During pre-startup check, if $EN_{UVP,In}$ parameter is enabled and the estimated input voltage V_{in} is lower than $V_{in,start,min}$, the startup phase will not be entered and the protection reaction of auto-restart will be performed.

Upon startup and in the regulated mode, the input undervoltage protection triggering condition depends on the operating mode:

- ***QRM1*/*DCM***:

  If $EN_{UVP,In}$ parameter is enabled and the estimated input voltage V_{in} is lower than V_{inUV} for longer than a blanking time, the input undervoltage protection will be triggered. The blanking time of the input undervoltage protection is typically 10 half sine wave periods.

  *Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

- ***ABM***:

  If $EN_{UVP,In}$ parameter is enabled, $EN_{VIN,ABM}$ parameter is enabled and the estimated input voltage V_{in} is lower than V_{inUV} for longer than a blanking time, the input undervoltage protection will be triggered. The blanking time of the input undervoltage protection is typically 10 burst periods.

  Note: $EN_{VIN,ABM}$ refers to the enable switch for input voltage protections in Active Burst Mode (ABM).

The reaction of the input undervoltage protection is fixed as auto-restart.

3.7.6 Maximum input voltage startup check and input overvoltage protection

By monitoring the estimated input voltage V_{in} based on the *ZCD* pin and *CS* pin switching signals (see ***Input voltage estimation*** for details), the maximum input voltage startup check can be performed, and the input overvoltage protection can be triggered if the condition is met.

$EN_{OVP,In}$ parameter refers to the enable switch for the maximum input voltage startup check (based on $V_{in,start,max}$) and input overvoltage protection (based on V_{inOV}).

Note: *$V_{in,start,max}$ parameter refers to the maximum input voltage level for startup, while V_{inOV} parameter refers to the input overvoltage protection level.*

During pre-startup check, if $EN_{OVP,In}$ parameter is enabled and the estimated input voltage V_{in} is higher than $V_{in,start,max}$, the startup phase will not be entered and the protection reaction of auto-restart will be performed.

Upon startup and in the regulated mode, the input overvoltage protection triggering condition depends on the operating mode:

- ***QRM1*/*DCM***:

  If $EN_{OVP,In}$ parameter is enabled and the estimated input voltage V_{in} is higher than V_{inOV} for longer than a blanking time, the input overvoltage protection will be triggered. The blanking time of the input overvoltage protection is typically 10 half sine wave periods.

  Note: *The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

- ***ABM***:

  If $EN_{OVP,In}$ parameter is enabled, $EN_{VIN,ABM}$ parameter is enabled and the estimated input voltage V_{in} is higher than V_{inOV} for longer than a blanking time, the input overvoltage protection will be triggered. The blanking time of the input overvoltage protection is typically 10 burst periods.

  Note: *$EN_{VIN,ABM}$ refers to the enable switch for input voltage protections in Active Burst Mode (ABM)*

The reaction of the input overvoltage protection is fixed as auto-restart.

3.7.7 VCC undervoltage lockout

The ***Undervoltage Lockout (UVLO)*** is implemented in the hardware. It ensures the enabling and disabling of the ***IC*** operation based on the defined thresholds of the operating supply voltage V_{VCC} at the *VCC* pin.

The ***UVLO*** contains a hysteresis with the voltage thresholds V_{VCCon} for enabling the controller and V_{UVOFF} for disabling the controller. Once the mains input voltage is applied, current flows through an external resistor into the *HV* pin via the integrated depletion cell and diode to the *VCC* pin. The controller is enabled once V_{VCC} exceeds the V_{VCCon} threshold and V_{VCC} will then start to drop. For normal startup, V_{VCC} supply should be taken over by either external supply or the self-supply via the auxiliary winding before V_{VCC} drops to V_{UVOFF}.

3.7.8 VCC undervoltage protection

In regulated mode, if $EN_{VCC,UVP}$ parameter is enabled and the sampled *VCC* voltage is lower than the *VCC* undervoltage protection level $V_{VCC,min}$ for longer than the blanking time of $t_{VCCUV,blank}$ parameter, the *VCC* undervoltage protection will be triggered. The *VCC* undervoltage protection reaction is fixed as auto-restart.

The *VCC* voltage is sampled 63 times per half sine wave period.

Note: *The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

3.7.9 VCC overvoltage protection

If the sampled *VCC* voltage is higher than the *VCC* overvoltage protection level $V_{VCC,max}$, the *VCC* overvoltage protection will be triggered. The *VCC* overvoltage protection reaction is configurable to auto-restart or latch-mode based on $Reaction_{VCC,OVP}$ parameter.

The *VCC* voltage is sampled 63 times per half sine wave period.

Note: *The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

3.7.10 IC overtemperature protection

If the sampled ***IC*** junction temperature T_j is higher than $T_{critical}$ parameter, the ***IC*** overtemperature protection will be triggered. The protection reaction is fixed as auto-restart, while the maximum junction temperature for startup and restart $T_{start,max}$ is fixed as 4°C below $T_{critical}$.

The ***IC*** junction temperature T_j is sampled 1 time per half sine wave period.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

If $T_{critical}$ is configured above 119°C, the maximum switching frequency parameter $f_{sw,max}$ cannot be configured above 136.4 kHz. If $T_{critical}$ is 119°C or below, the maximum configurable $f_{sw,max}$ value is 180.8 kHz.

Attention: IC lifetime is not guaranteed when operating junction temperature is above 125°C, which is possible if $T_{critical}$ is configured above 119°C, with temperature sensing tolerance of ± 6°C.

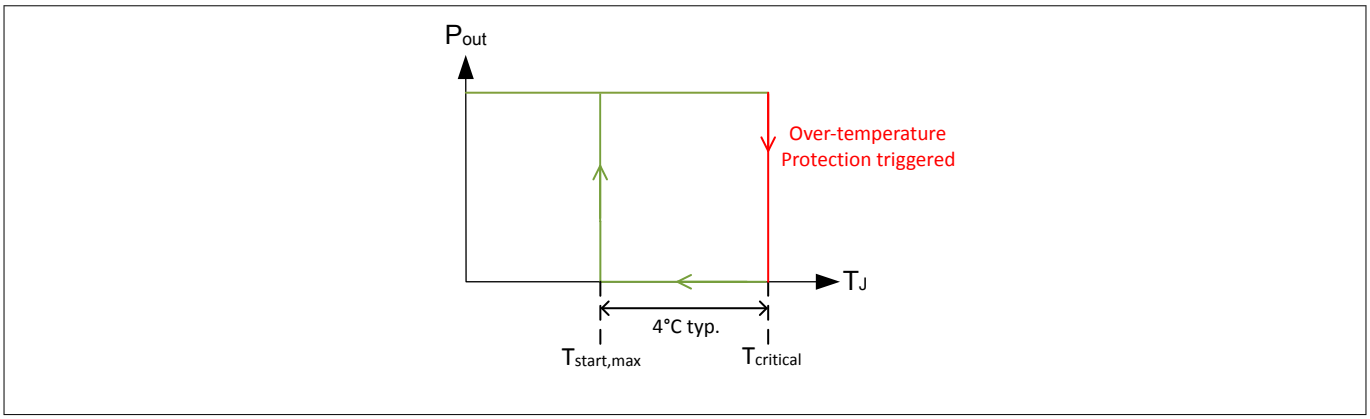

Figure 19 IC overtemperature protection

3.7.11 Other protections

- A hardware weak pull-up protects against an open *CS* pin. The reaction of this protection reaction is auto-restart.
- A firmware watchdog triggers a protection if the ADC hardware cannot provide all necessary information within a defined time period. This may occur if timing requirements for the ADC are exceeded. The reaction of this protection is fast auto-restart.
- A hardware watchdog checks correct execution of firmware. A protection is triggered in the event that the firmware does not service the watchdog within a defined period. The reaction of this protection is auto-restart.
- A hardware parity check triggers a protection if a bit in the memory changes unintentionally. The reaction of this protection is auto-restart.
- A firmware ***Cyclic Redundancy Check (CRC)*** at each startup verifies the integrity of firmware and parameters. The reaction of this protection is stop mode.
- A firmware task execution watchdog triggers a protection if the firmware tasks are not executed as expected. The reaction of this protection is auto-restart.
- A protection is triggered if the configurable parameter values are empty at startup. The reaction of this protection is stop mode.
- A protection is triggered if no reflected input voltage signal sensed from the *ZCD* pin at startup. The reaction of this protection is stop mode.

3.7.12 Protection reactions

The sequence of a protection reaction (not including hardware restart reaction) is as follows:

1. Upon triggering a protection, the gate driver is disabled within a maximum time, which is 1/512 of the half sine wave period.

   *Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

2. The reaction depends on the triggered protection:
   - In case of latch mode, the application will enter latch mode at this time. No further sequence is done until *VCC* voltage drops below V_{UVOFF}.
   - In case of auto-restart reaction, the controller will enter power saving mode PSMD2 with the auto-restart time based on $t_{auto,restart}$ parameter.
   - In case of fast auto-restart reaction, the controller will enter power saving mode PSMD2 with the fast auto-restart time of 0.4 sec.

   Note: For latch mode, auto-restart and fast auto-restart reactions, the internal HV startup cell is automatically enabled and disabled during this sequence, in order to keep the VCC voltage between the V_{UVLO} and V_{OVLO} thresholds.

   Note: For stop mode, if there is no external voltage supply for the VCC, the VCC voltage will drain to V_{UVOFF} and a hardware restart will be performed.

3. After the (fast) auto-restart time is expired, the controller executes a single discharge pulse of duration t_{pw}. This pulse partially discharges the capacitance after the bridge rectifier to improve accuracy of the next pre-startup input voltage check.
4. Any auto restart may include a new *VCC* charging cycle. The recharging time of *VCC* via *HV* pin current depends on the input voltage level and *VCC* level at the time when the (fast) auto-restart time is expired.
5. The power stage will enable its gate driver for pre-startup check. If the conditions for pre-startup check are within limits, the startup phase is entered and followed by the regulated mode. During this time, if any protection is triggered, the sequence of a protection reaction (not including hardware restart reaction) starts again from step number 1 above.

3.8 Debug mode

If an unexpected system protection was triggered during testing, the $Debug_{Mode}$ parameter can be enabled to enter stop mode reaction upon the protection triggering (except for *VCC* undervoltage lockout), to read out the firmware status code. For example in ***Figure 20***, the firmware status code readout in the ***GUI*** shows a number of 0040_H (in red color), which indicates that the input undervoltage protection has been triggered.

Note: If there is no protection being triggered, the firmware status code should be 0000_H (in black color).

Note: $Debug_{Mode}$ parameter should only be enabled for debugging purpose. For actual application running, it has to be disabled.

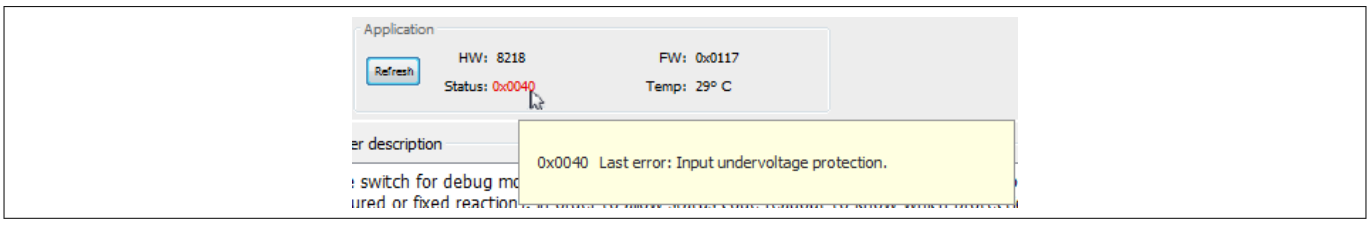

Figure 20 Firmware status code readout for debugging

Please refer the design guide for the recommended setup & procedures to read out the firmware status code in debug mode.

4 List of Parameters

This list provides information about the configurable and fixed parameters.

This document uses symbols to ease the readability of formulas. As some tools do not support this format, the symbols are translated into plain text using underscores. For example, the parameter $f_{sw,max}$ translates to f_sw_max.

All parameter values are typical settings. The accuracy might vary due to digital quantization and tolerances.

Note: By default, the configurable parameters of a new XDPL8218 chip from Infineon are empty, so it is necessary to configure them before any application testing.

List of configurable parameters

Table 2 Configurable parameters for hardware configuration

Symbol	Basic description	Example	Minimum value	Maximum value
N_p	Transformer primary main winding turns	32	1	300
N_s	Transformer secondary main winding turns	10	1	300
N_a	Transformer primary auxiliary winding turns	3	1	300
L_p	Transformer nominal primary main winding inductance	0.544 mH	Refer GUI	3 mH
R_{CS}	Current sense resistor value	0.2 Ω	0.1 Ω	3 Ω
$R_{ZCD,1}$	*ZCD* series resistor value	27 kΩ	Refer GUI	Refer GUI
$R_{ZCD,2}$	*ZCD* shunt resistor value	3.9 kΩ	Refer GUI	Refer GUI
C_{VCC}	*VCC* capacitor value	22 µF	Refer GUI	100 µF
$V_{out,cap,rating}$	Main output capacitor voltage rating	80 V	10 V	450 V
R_{HV}	*HV* series resistor value	52 kΩ	Refer GUI	255 kΩ
$I_{GD,pk}$	Gate driver peak source current	30 mA	30 mA	108 mA

Table 3 Configurable parameters for startup

Symbol	Basic description	Example	Minimum value	Maximum value
n_{ss}	Number of soft start steps	3	1	Refer GUI
$V_{out,start}$	Output charging phase output voltage set-point	27 V	$V_{outUV,start}$	V_{outOV}
$V_{start,OCP1}$	Output charging phase *CS* pin voltage level 1 for MOSFET max. current cycle by cycle limit	0.52 V	Refer GUI	$V_{OCP1,at,V,in,low}$
$V_{OCP1,init}$	Initial *CS* pin voltage level 1 for MOSFET max. current limit on the input voltage measurement pulse before startup	0.3 V	Refer GUI	$V_{start,OCP1}$

Table 4 Configurable parameters for protections

Symbol	Basic description	Example	Minimum value	Maximum value
$t_{auto,restart}$	Auto-restart time	1.2 s	0.4 s	4 s

Table 4 Configurable parameters for protections (continued)

Symbol	Basic description	Example	Minimum value	Maximum value
$V_{OCP1,at,V,in,low}$	Regulated mode *CS* pin voltage level 1 for MOSFET max. current cycle by cycle limit at lowest operational input voltage ($V_{in,low}$)	0.52 V	Refer GUI	1.08 V
$V_{OCP1,at,V,in,high}$	Regulated mode *CS* pin voltage level 1 for MOSFET max. current cycle by cycle limit at highest operational input voltage ($V_{in,high}$)	0.34 V	Refer GUI	$V_{OCP1,at,V,in,low}$
$V_{in,low}$	Lowest operational input voltage (rms in case of AC input)	82 V	V_{inUV}	$V_{in,high}$
$V_{in,high}$	Highest operational input voltage (rms in case of AC input)	325 V	$V_{in,low}$	V_{inOV}
t_{CSOCP2}	MOSFET overcurrent protection blanking time	240 ns	100 ns	Refer GUI
$Reaction_{OVP,Vout}$	Output overvoltage protection reaction	Auto-Restart	Auto-Restart	Latch-Mode
V_{outOV}	Output overvoltage protection threshold	65 V	$V_{out,start}$	Refer GUI
$V_{outUV,start}$	Startup output undervoltage protection threshold	27 V	Refer GUI	$V_{out,start}$
$EN_{UVP,Vout}$	Enable switch for regulated mode output undervoltage protection	Enabled	Enabled	Disabled
$Reaction_{UVP,Vout}$	Regulated mode output undervoltage protection reaction	Auto-Restart	Auto-Restart	Latch-Mode
V_{outUV}	Regulated mode output undervoltage protection threshold	33 V	Refer GUI	Refer GUI
$t_{VoutUV,blank}$	Blanking time for regulated mode output undervoltage protection	500 ms	5 ms	1000 ms
$EN_{OVP,In}$	Enable switch for maximum input voltage startup check and input overvoltage protection	Enabled	Enabled	Disabled
$EN_{UVP,In}$	Enable switch for minimum input voltage startup check and input undervoltage protection	Enabled	Enabled	Disabled
$EN_{VIN,ABM}$	Enable switch for ***ABM*** input voltage protections	Enabled	Enabled	Disabled
V_{inOV}	Input overvoltage protection threshold (rms in case of AC input)	350 V	$V_{in,start,max}$	Refer GUI
$V_{in,start,max}$	Maximum input voltage for startup (rms in case of AC input)	325 V	$V_{in,start,min}$	V_{inOV}
$V_{in,start,min}$	Minimum input voltage at startup (rms in case of AC input)	82 V	V_{inUV}	$V_{in,start,max}$
V_{inUV}	Input undervoltage protection threshold (rms in case of AC input)	70 V	Refer GUI	$V_{in,start,min}$
$P_{foldback,gain}$	Maximum on-time foldback gain for power limitation at brown-out	1	0	Refer GUI
$Reaction_{VCC,OVP}$	*VCC* overvoltage protection reaction	Latch-Mode	Auto-Restart	Latch-Mode
$V_{VCC,max}$	*VCC* overvoltage protection threshold	23 V	23 V	24.9 V

List of Parameters

Table 4 Configurable parameters for protections (continued)

Symbol	Basic description	Example	Minimum value	Maximum value
$EN_{VCC,UVP}$	Enable switch for regulated mode *VCC* undervoltage protection	Enabled	Enabled	Disabled
$V_{VCC,min}$	Regulated mode *VCC* undervoltage protection threshold	7.5 V	6.3 V	$V_{VCC,max}$
$t_{VCCUV,blank}$	Blanking time for regulated mode VCC undervoltage protection	1.5 ms	0 s	Refer GUI
$T_{critical}$	Temperature threshold for IC overtemperature protection	119°C	Refer GUI	143°C
$Debug_{Mode}$	Enable switch for debug mode	Disabled	Enabled	Disabled

Table 5 Configurable parameters for multimode

Symbol	Basic description	Example	Minimum value	Maximum value
$R_{FB,pull,up}$	*FB* pin internal pull-up resistor value	5.5 kohm	2.25 kohm	7.5 kohm
$N_{quality}$	Quality factor of the notch filter	1.6	0	2.0
$n_{notch,blank}$	Number of half sine wave period as a timeout between the line synchronization being established and the notch filter output being applied as the filtered feedback voltage. [1)]	2	1	10
$f_{sw,max}$	Maximum switching frequency when $V_{FB,filtered}$ is $V_{FB,sw}$ (2.0 V) or above	136 kHz	20 kHz	Refer GUI
$t_{on,min}$	Minimum on-time $t_{on,min}(V_{in})$ value when $t_{on,min,V,out,sense}(V_{in})$ is lower than $t_{on,min}$	1.38 µs	Refer GUI	$t_{on,max,at,V,in,low}$
$t_{min,demag}$	Minimum transformer demagnetizing time value used for $t_{on,min,V,out,sense}(V_{in})$ variable calculation internally	4 µs	3 µs	5 µs
$t_{on,max,at,V,in,low}$	Maximum on-time when V_{in} is $V_{in,low}$	15 µs	Refer GUI	30 µs
f_{burst}	ABM burst frequency	130 Hz	130 Hz	400 Hz
$n_{ABM,min}$	Minimum number of pulses per burst	1	1	Refer GUI
$t_{on,min,ABM}$	Minimum on-time in ***ABM***	1 µs	Refer GUI	$t_{on,min}$
$t_{ABM,blank}$	Timeout for ***ABM*** entrance	6.5 ms	0 ms	Refer GUI
n_{wakeup}	Number of scheduler intervals between wakeup and start of the burst	5	1	20
$V_{FB,max,map}$	$V_{FB,filtered}$ threshold which represents the maximum power transfer of the system	2.0 V	Refer GUI	2.428 V
$V_{FB,min}$	$V_{FB,filtered}$ threshold which represents the minimum power transfer of the system	0.3 V	0.2 V	0.5 V

1 It is essential for the notch filter to have line synchronization in order to work properly. This timeout enables the notch filter to converge. During this timeout, a low pass filter is used as the feedback voltage filtration.

List of Parameters

Table 5 Configurable parameters for multimode (continued)

Symbol	Basic description	Example	Minimum value	Maximum value
$V_{FB,limit,step}$	Voltage step size of filtered feedback voltage max. limit $V_{FB,filtered,max}$ ramp	800 mV	Refer GUI	Refer GUI

Table 6 Configurable parameters for power factor correction

Symbol	Basic description	Default	Minimum value	Maximum value
C_{EMI}	Input current displacement compensation gain parameter for enhanced PFC	0.2 µF	0 µF	1 µF

Table 7 Configurable parameters for fine tuning

Symbol	Basic description	Default	Minimum value	Maximum value
t_{ZCDPD}	*ZCD* pin propagation delay compensation parameter	370 ns	0 s	1000 ns
R_{in}	DC link filter capacitor voltage ripple compensation parameter to improve input voltage estimation accuracy	10.5 Ω	0 Ω	30 Ω

Table 8 Configurable parameters for user ID

Symbol	Basic description	Default	Minimum value	Maximum value
$User_{ID,A}$	User ID A	0	-	-

List of Fixed Parameters

Table 9 Fixed parameters for hardware configuration

Symbol	Basic description	Default	Minimum value	Maximum value
V_d	Secondary main output diode forward voltage assumption for output voltage estimation	0.7 V	-	-
V_{GD}	*GD* pin peak voltage	12 V	-	-

Table 10 Fixed parameters for protections

Symbol	Basic description	Default	Minimum value	Maximum value
$T_{start,max}$	Maximum IC junction temperature for startup	$T_{critical}$ - 4°C	-	-

Table 11 Fixed parameters for startup

Symbol	Basic description	Default	Minimum value	Maximum value
t_{ss}	Soft start time step	0.5 ms	-	-

Table 11 Fixed parameters for startup (continued)

Symbol	Basic description	Default	Minimum value	Maximum value
$V_{FB,limit,start}$	Start voltage for filtered feedback voltage max. limit $V_{FB,filtered,max}$ ramp	1.2 V	-	-

Table 12 Fixed parameters for multimode

Symbol	Basic description	Default	Minimum value	Maximum value
$V_{FB,ABM}$	$V_{FB,filtered}$ threshold for the ***ABM***/***DCM*** transition	800 mV	-	-
$V_{FB,sw}$	$V_{FB,filtered}$ threshold for the end of the maximum switching frequency ramp up	2 V	-	-
$V_{FB,on}$	$V_{FB,filtered}$ threshold for the start of the on-time ramp up	1.2 V	-	-
$f_{sw,min}$	Minimum switching frequency	20 kHz	-	-

Table 13 Fixed parameters for power factor correction

Symbol	Basic description	Default	Minimum value	Maximum value
$V_{EPFC,off}$	Above this $V_{FB,filtered}$ threshold, the enhanced ***PFC*** is fully enabled.	1.2 V	-	-
$V_{EPFC,off}$	Below this $V_{FB,filtered}$ threshold, the enhanced ***PFC*** is disabled.	0.8 V	-	-
$t_{on,min,EPFC}$	Minimum on time for enhanced ***PFC*** modulation	$t_{CS,LEB} + 24/f_{MCLK}$	-	-
$t_{on,max,EPFC}$	Maximum on time for enhanced ***PFC*** modulation	$1.5^{*}t_{on,max,at,V,in,low}$	-	-

Table 14 Other fixed parameters

Symbol	Basic description	Default	Minimum value	Maximum value
$t_{CS,LEB}$	*CS* leading edge blanking time	480 ns	-	-
$t_{ZCD,ring}$	*ZCD* ringing suppression	1.2 µs	-	-
t_{pw}	Discharge pulse duration	1.5 µs	-	-
$n_{OSC,ZCD}$	Selection of zero-crossings for the oscillation period measurement at pre-startup	Second and Third zero-crossings	-	-
$T_{OSC,max}$	Maximum limit of the measured oscillation period (If exceeded at pre-startup, $T_{OSC,preset}$ is used; If exceeded after startup, the last valid measured oscillation period is used)	6.6 µs	-	-
$T_{OSC,preset}$	Oscillation period used by the controller if the measured oscillation period at pre-startup exceeds $T_{OSC,max}$	3.3 µs	-	-

5 Electrical Characteristics and Parameters

All signals are measured with respect to the ground pin, GND. The voltage levels are valid provided other ratings are not violated.

5.1 Package Characteristics

Table 15 Package Characteristics

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Thermal resistance for PG-DSO-8-58	R_{thJA}	—	178	K/W	JEDEC 1s0p for 140 mW power dissipation

5.2 Absolute Maximum Ratings

Attention**: **Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.

Table 16 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Voltage externally supplied to pin VCC	V_{VCCEXT}	–0.5	26	V	voltage that can be applied to pin VCC by an external voltage source
Voltage at pin GDx	V_{GDx}	–0.5	V_{VCC} + 0.3	V	if gate driver is not configured for digital I/O
Junction temperature	T_J	–40	125	°C	max. operating frequency 66 MHz f_{MCLK}
Junction temperature	T_J	–40	150[1]	°C	$f_{sw,max} \leq 136$ kHz
Storage temperature	T_S	–55	150	°C	
Soldering temperature	T_{SOLD}	—	260	°C	Wave Soldering [2]
Latch-up capability	I_{LU}	—	150	mA	[3] Pin voltages acc. to abs. max. ratings
ESD capability HBM	V_{HBM}	—	1500	V	[4][5]
ESD capability CDM	V_{CDM}	—	500	V	[6]

1 Auto-restart may be delayed at low input voltage condition when junction temperature is above 125°C. The lifetime is not guaranteed when IC operating junction temperature is above 125°C.
2 According to JESD22-A111 Rev A.
3 Latch-up capability according to JEDEC JESD78D, T_A= 85°C.
4 ESD-HBM according to ANSI/ESDA/JEDEC JS-001-2012.
5 product resp. package specific rating up to 2000 V
6 ESD-CDM according to JESD22-C101F.

Table 16 Absolute Maximum Ratings (continued)

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Input Voltage Limit	V_{IN}	–0.5	3.6	V	Voltage externally supplied to pins GPIO, MFIO, CS, ZCD, GPIO, VS, GDx (if GDx is configured as digital I/O). (If not stated different)
Maximum permanent negative clamping current for ZCD and CS	$-I_{CLN\_DC}$	—	2.5	mA	RMS
Maximum transient negative clamping current for ZCD and CS	$-I_{CLN\_TR}$	—	10	mA	pulse < 500ns
Maximum negative transient input voltage for ZCD	$-V_{IN\_ZCD}$	—	1.5	V	pulse < 500ns
Maximum negative transient input voltage for CS	$-V_{IN\_CS}$	—	3.0	V	pulse < 500ns
Maximum permanent positive clamping current for CS	I_{CLP_DC}	—	2.5	mA	RMS
Maximum transient positive clamping current for CS	I_{CLP_TR}	—	10	mA	pulse < 500ns
Maximum current into pin VIN	I_{AC}	—	10	mA	for charging operation
Maximum sum of input clamping high currents for digital input stages of device	I_{CLH_sum}	—	300	µA	limits for each individual digital input stage have to be respected
Voltage at HV pin	V_{HV}	-0.5	600	V	

5.3 Operating Conditions

The recommended operating conditions are shown for which the DC Electrical Characteristics are valid.

Table 17 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Ambient temperature	T_A	–40	85	°C	
Junction Temperature	T_J	–40	125	°C	max. 66 MHz f_{MCLK}
Lower VCC limit	V_{VCC}	V_{UVOFF}	—	V	device is held in reset when $V_{VCC} < V_{UVOFF}$
Voltage externally supplied to VCC pin	V_{VCCEXT}	—	24	V	maximum voltage that can be applied to pin VCC by an external voltage source
Gate driver pin voltage	V_{GD}	–0.5	V_{VCC} + 0.3	V	
Line frequency	f_{in}	45	66	Hz	

5.4 DC Electrical Characteristics

The electrical characteristics provide the spread of values applicable within the specified supply voltage and junction temperature range, T_J from -40 °C to +125 °C.

Devices are tested in production at T_A = 25 °C. Values have been verified either with simulation models or by device characterization up to 125 °C.

Typical values represent the median values related to T_A = 25 °C. All voltages refer to GND, and the assumed supply voltage is V_{VCC} = 18 V if not otherwise specified.

Note: Not all values given in the tables are tested during production testing. Values not tested are explicitly marked.

Table 18 Power Supply Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC_ON threshold	V_{VCCon}	—	V_{SELF}	—	V	Self-powered startup (default)
VCC_ON_SELF threshold	V_{SELF}	19	20.5	22	V	dV_{VCC}/dt = 0.2 V/ms
VCC_ON_SELF delay	t_{SELF}	—	—	2.1	µs	Reaction time of V_{VCC} monitor
VCC_UVOFF current	$I_{VCCUVOFF}$	5	20	40	µA	$V_{VCC} < V_{SELF}$(min) - 0.3 V or $V_{VCC} < V_{EXT}$(min) - 0.3 V[7)]
UVOFF threshold	V_{UVOFF}	—	6.0	—	V	SYS_CFG0.SELUVTHR = 0_B
UVOFF threshold tolerance	Δ_{UVOFF}	—	—	±5	%	This value defines the tolerance of V_{UVOFF}
UVOFF filter constant	t_{UVOFF}	600	—	—	ns	1V overdrive
UVLO (UVWAKE) threshold	V_{UVLO}	—	V_{UVOFF} · 1.25	—	V	
UVWAKE threshold tolerance	Δ_{UVLO}	—	—	±5	%	This value defines the tolerance of V_{UVLO}
UVLO (UVWAKE) filter constant	t_{UVLO}	0.6	—	2.2	µs	1 V overdrive
OVLO (OVWAKE) threshold	V_{OVLO}	—	V_{SELF}	—	V	
OVLO (OVWAKE) filter constant	t_{OVLO}	0.6	—	2.4	µs	1 V overdrive
VDDP voltage	V_{VDDP}	3.04	3.20	3.36	V	At PMD0/PSMD1. Some internal values refer to V_{VDDP} / V_{VDDA} and V_{VDDPPS} / V_{VDDAPS} respectively.

7 Tested at V_{VCC} = 5.5 V

Table 18 Power Supply Characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDDA voltage	V_{VDDA}	3.20	3.31	3.42	V	At PMD0/PSMD1. Some internal values refer to V_{VDDP} / V_{VDDA} and V_{VDDPPS} / V_{VDDAPS} respectively.
Nominal range 0% to 100%	V_{ADCVCC}	0	—	V_{REF}	V	$V_{ADCVCC} = 0.09 \cdot V_{VCC}$ [8]
Reduced VCC range for ADC measurement	R_{ADCVCC}	8	—	92	%	[9][10]
Maximum error for ADC measurement (8-bit result)	$TET0_{VCC}$	—	—	3.8	LSB_8	
Maximum error for ADC measurement (8-bit result)	$TET256_{VCC}$	—	—	5.2	LSB_8	
Gate driver current consumption excl. gate charge current	I_{VCCGD}	—	0.26	0.35	mA	$T_j \leq 125°C$
VCC quiescent current in PMD0	$I_{VCCPMD0}$	—	3.5	4.7	mA	All registers have reset values, clock is active, CPU is stopped
VCC quiescent current in PSMD2	$I_{VCCPSMD2}$	—	0.3	0.48	mA	$T_j \leq 85$ °CWU_PWD_CFG = $2C_H$
VCC quiescent current in PSMD2	$I_{VCCPSMD2}$	—	—	1.2	mA	$T_j \leq 125$ °CWU_PWD_CFG = $2C_H$
VCC quiescent current in power saving mode PSDM4 with standby logic active	$I_{VCCPSMD4}$	—	0.13	0.18	mA	$T_j \leq 125$ °C WU_PWD_CFG = 00_H

Table 19 Electrical Characteristics of the GD Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	µA	only digital input
Input clamping current, high	I_{CLH}	—	—	100	µA	only digital input

8 Theoretical minimum value, real minimum value is related to V_{UVOFF} threshold.
9 Operational values.
10 Note that the system is turned off if $V_{VCC} < V_{UFOFF}$.

Table 19 Electrical Characteristics of the GD Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	V_{APD}	—	—	1.6	V	I_{GD} = 5 mA
R_{PPD} value	R_{PPD}	—	600	—	kΩ	Permanent pull-down resistor inside gate driver
R_{PPD} tolerance	Δ_{PPD}	—	—	±25	%	Permanent pull-down resistor inside gate driver
Driver output low impedance	R_{GDL}	—	—	7.0	Ω	$T_J \leq 125$ °C, I_{GD} = 0.1 A
Nominal output high voltage in PWM mode	V_{GDH}	—	12	—	V	GDx_CFG.VOL = 2, I_{GDH} = –1 mA
Output voltage tolerance	Δ_{VGDH}	—	—	±5	%	Tolerance of programming options if V_{GDH} > 10 V, I_{GDH} = –1 mA
Rail-to-rail output high voltage	V_{GDHRR}	V_{VCC}– 0.5	—	V_{VCC}	V	If V_{VCC} < programmed V_{GDH} and output at high state
Output high current in PWM mode for GD0	$-I_{GDH}$	—	100	—	mA	GDx_CFG.CUR = 8
Output high current tolerance in PWM mode	Δ_{IGDH}	—		±15	%	Calibrated [11]
Discharge current for GD0	I_{GDDIS}	800	—	—	mA	V_{GD} = 4 V and driver at low state
Output low reverse current	$-I_{GDREVL}$	—	—	100	mA	Applies if V_{GD} < 0 V and driver at low state
Output high reverse current in PWM mode	I_{GDREVH}	—	1/6 of I_{GDH}	—		Applies if V_{GD} > V_{GDH} + 0.5 V (typ) and driver at high state

Table 20 Electrical Characteristics of the CS Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.0	V	

11 referred to GDx_CFG.CUR = 16

Table 20 Electrical Characteristics of the CS Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	1.6	—	V	SYS_CFG0.OCP2 = 00_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	1.2	—	V	SYS_CFG0.OCP2 = 01_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	0.8	—	V	SYS_CFG0.OCP2 = 10_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	0.6	—	V	SYS_CFG0.OCP2 = 11_B
Threshold voltage tolerance	Δ_{VOCP2}	—	—	±5	%	Voltage divider tolerance
Comparator propagation delay	t_{OCP2PD}	15	—	35	ns	
Minimum comparator input pulse width	t_{OCP2PW}	—	—	30	ns	
OCP2F comparator propagation delay	$t_{OCP2FPD}$	70	—	170	ns	dV_{CS}/dt = 100 V/µs
Delay from V_{CS} crossing V_{CSOCP2} to begin of GDx turn-off (I_{GD0} > 2mA)	$t_{CSGDxOCP2}$	125	135	190	ns	dV_{CS}/dt = 100 V/µs; f_{MCLK} = 66 MHz. GDx driven by QR_GATE FIL_OCP2.STABLE = 3
OCP1 operating range	V_{OCP1}	0	—	$V_{REF}/2$	V	RANGE =00_B
OCP1 threshold at full scale setting (CS_OCP1LVL=FF_H)	V_{OCP1FS}	1187	1209	1243	mV	RANGE =00_B
Delay from V_{CS} crossing V_{CSOCP1} to CS_OCP1 rising edge, 1.2 V range	t_{CSOCP1}	90	170	250	ns	Input signal slope dV_{CS}/dt = 150 mV/µs. This slope represents a use case of a switch-mode power supply with minimum input voltage.

Table 20 Electrical Characteristics of the CS Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Delay from CS_OCP1 rising edge to QR_GATE falling edge	$t_{OCP1GATE}$	—	—	130	ns	
Delay from QR_GATE falling edge to start of GDx turn-off	$t_{GATEGDx}$	1	3	5	ns	GDx driven by QR_GATE. Measured up to I_{GDx} > 2 mA
OCP1 comparator input single pulse width filter	t_{OCP1PW}	60	—	95	ns	Shorter pulses than min. are suppressed, longer pulses than max. are passed
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/2$	V	CS_ICR.RANGE =00_B
Reduced S&H operating range	RR_{CVSH}	8	—	92	%	CS_ICR.RANGE =00_B Operational values
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET0_{CS0S}$	—	—	4.7	LSB	CS_ICR.RANGE =00_B
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET256_{CS0S}$	—	—	6.0	LSB	CS_ICR.RANGE =00_B
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/6$	V	CS_ICR.RANGE =11_B
Reduced S&H operating range	RR_{CVSH}	20	—	80	%	CS_ICR.RANGE =11_B Operational values
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET0_{CS0S}$	—	—	8.0	LSB	CS_ICR.RANGE =11_B
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET256_{CS0S}$	—	—	8.7	LSB	CS_ICR.RANGE =11_B
S&H delay of input buffer	t_{CSHST}	—	—	510	ns	Referring to jump in input voltage. Limits the minimum gate driver T_{on} time.

Table 21 Electrical Characteristics of the ZCD Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.3	V	
Input clamping current, high	I_{CLH}	—	—	100	µA	
Zero-crossing threshold	V_{ZCTHR}	15	40	70	mV	
Comparator propagation delay	t_{ZCPD}	30	50	70	ns	dV_{ZCD}/dt = 4 V/µs
Input voltage negative clamping level	$-V_{INPCLN}$	140	180	220	mV	Analog clamp activated
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	0.5	mA	CRNG =11_BGain = 4800 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	1	mA	CRNG =10_BGain = 2400 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	2	mA	CRNG =01_BGain = 1200 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	4	mA	CRNG =00_B Gain = 600 mV/mA
Reduced I/V-conversion operating range	RR_{IV}	5	—	80	%	
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{IV}$	—	—	4.1	LSB_8	CRNG =00_B
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{IV}$	—	—	9.7	LSB_8	CRNG =00_B
Maximum deviation between ZCD clamp voltage and trim result stored in OTP	E_{ZCDClp}	—	—	±5	%	$-I_{IV}$ > 0.25 mA
IV-conversion delay of input buffer	t_{IVST}	—	—	900	ns	Refers to jump in input current[12)]

12 Limits the minimum gate driver T_{on} time.

Table 21 Electrical Characteristics of the ZCD Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Nominal S&H input voltage range 0% to 100%	V_{ZSH}	0	—	$2/3 \cdot V_{REF}$	V	SHRNG $=0_B$
Nominal S&H input voltage range 0% to 100%	V_{ZSH}	$V_{REF}/2$	—	$7/6 \cdot V_{REF}$	V	SHRNG $=1_B$
Reduced S&H input voltage range	RR_{ZVSH}	4	—	95	%	
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{ZVS0}$	—	—	3.7	LSB_8	SHRNG $=0_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{ZVS0}$	—	—	4.9	LSB_8	SHRNG $=0_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{ZVS1}$	—	—	4.2	LSB_8	SHRNG $=1_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{ZVS1}$	—	—	5.8	LSB_8	SHRNG $=1_B$
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.0	µs	SHRNG $=0_B T_j \le 125$ °C
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.6	µs	SHRNG $=1_B T_j \le 125$ °C

Table 22 Electrical Characteristics of the HV Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Current for V_{CC} cap charging	I_{LD}	3.0	5	7.5	mA	$V_{HV} = 30$ V; $V_{VCC} < V_{VCCon} - 0.3$ V; $T_j \ge 0$°C
Current for V_{CC} cap charging	I_{LD}	2.4	5	7.5	mA	$V_{HV} = 30$ V; $V_{VCC} < V_{VCCon} - 0.3$ V;-25°C < T_j < 0°C
Current for V_{CC} cap charging	I_{LD}	2.0	5	7.5	mA	$V_{HV} = 30$ V; $V_{VCC} < V_{VCCon} - 0.3$ V;T_j < -25°C

Table 22 Electrical Characteristics of the HV Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	9.6	mA	CURRNG = 11_B
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	4.8	mA	CURRNG = 10_B
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	1.6	mA	CURRNG = 01_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	15	20	25	%	COMPTHR= 00_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	25	30	35	%	COMPTHR= 01_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	45	50	55	%	COMPTHR= 11_B

Table 23 Electrical Characteristics of the FB Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
MFIO reference voltage	$V_{MFIOREF}$	—	V_{REF}	—	V	Selection = V_{REF}
Nominal range 0% to 100%	V_{MFIO}	0	—	V_{REF}	V	Gain = 1
Reduced operating range	RR_{VMFIO}	4	—	96	%	Gain = 1. Operational values.
Maximum error for corrected measurement (8-bit result)	$TET0_{MFI0}$	—	—	4.0	LSB_8	Gain = 1
Maximum error for corrected measurement (8-bit result)	$TET256_{MFI0}$	—	—	4.8	LSB_8	Gain = 1
Delay of input buffer	t_{MFIOST}	—	—	2.7	µs	Refers to jump in input voltage 0% to 90%. Applicable for MFIO0 and MFIO1 only.

Table 24 Electrical Characteristics of the UART Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	µA	only digital input
Input clamping current, high	I_{CLH}	—	—	100	µA	only digital input
Input capacitance	C_{INPUT}	—	—	25	pF	
Input low voltage	V_{IL}	—	—	1.0	V	
Input high voltage	V_{IH}	2.1	—	—	V	
Input low current with active weak pull-up WPU	$-I_{LPU}$	30	—	90	µA	Measured at max. V_{IL}
Max. input frequency	f_{INPUT}	15	—	—	MHz	
Output low voltage	V_{OL}	—	—	0.8	V	I_{OL} = 2 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA
Output sink current	I_{OL}	—	—	2	mA	
Output source current	$-I_{OH}$	—	—	2	mA	
Output rise time (0 → 1)	t_{RISE}	—	—	50	ns	20 pF load, push/pull output
Output fall time (1 → 0)	t_{FALL}	—	—	50	ns	20 pF load, push/pull or open-drain output
Max. output switching frequency	f_{SWITCH}	10	—	—	MHz	
UART baudrate	f_{UART}	-10%	57600	+10%	baud	

Table 25 Electrical Characteristics of the A/D Converter

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Integral non-linearity	INL	—	—	1	LSB_8	13)

Table 26 Electrical Characteristics of the Reference Voltage

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Reference voltage	V_{REF}	—	2.428	—	V	
VREF overall tolerance	Δ_{VREF}	—	—	±1.5	%	Trimmed, $T_j \leq 125$ °C and aging

13 ADC capability measured via channel MFIO without errors due to switching of neighbouring pins, e.g. gate drivers, measured with STC = 5. MFIO buffer non-linearity masked out by taking ADC output values ≥ 30 only.

Table 27 Electrical Characteristics of the OTP Programming

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OTP programming voltage at the VCC pin for range $C000_H$ to $CFFF_H$	V_{PP}	7.35	7.5	7.65	V	Operational values
OTP programming current	I_{PP}	—	1.6	—	mA	Programming of 4 bits in parallel

Table 28 Electrical Characteristics of the Clock Oscillators

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Master clock oscillation period including all variations	t_{MCLK}	15.0	15.8	16.6	ns	In reference to 66 MHz f_{MCLK}
Main clock oscillator frequency variation of stored DPARAM frequency	Δ_{MCLK}	–3.2	—	+3.5	%	Temperature drift and aging only, 66 MHz f_{MCLK}
Standby clock oscillator frequency	f_{STBCLK}	96	100	104	kHz	Trimming tolerance at T_A = 25 °C
Standby clock oscillator frequency	f_{STBCLK}	90	100	110	kHz	Overall tolerance, $T_j \leq$ 125 °C

Table 29 Electrical Characteristics of the Temperature Sensor

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Temperature sensor ADC output operating range	ADC_{TEMP}	0	—	190	LSB	ADC_{TEMP} = 40 + temperature / °C)
Temperature sensor tolerance	Δ_{TEMP}	—	—	±6	K	Incl. ADC conversion accuracy at 3 σ

6 Package Dimensions

The package dimensions of PG-DSO-8 are provided.

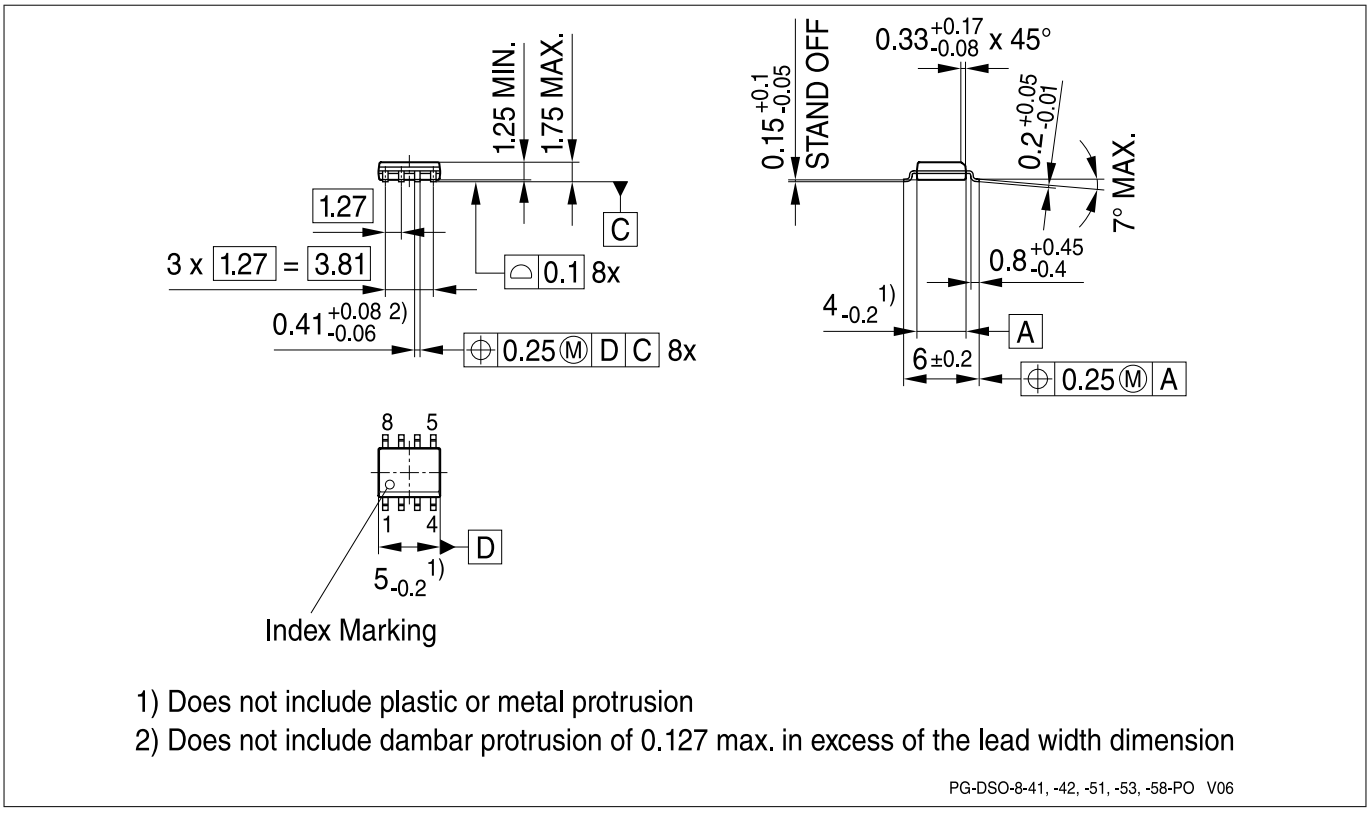

Figure 21 Package Dimensions for PG-DSO-8

Note: Dimensions in mm.

Note: You can find all of our packages, packing types and other package information on our Infineon Internet page “Products”: http://www.infineon.com/products.

7 References

1. Infineon: *XDPL8218 Design Guide*
2. Infineon: *XDPL8218 Reference Board Engineering Report*
3. Infineon: *CoolMOS P7 power MOSFETs*, ***http://www.infineon.com/P7***
4. Infineon: *.dp Vision User Manual*
5. Infineon: *.dp Interface Gen2* which can be ordered at ***http://www.ehitex.de/en/programmer/2527/.dp-interface-board-gen2.dp-digital-power-2.0-infineon***
6. Infineon: *.dp Interface Gen2 User Manual*
7. Infineon: *Programming manual for XDPL controllers with PG-DSO-8 package*

Revision History

Major changes since previous revision

Revision History

Revision	Description
1.0	• Initial version

Glossary

ABM
Active Burst Mode (ABM)

Active Burst Mode is an operating mode of a switched-mode power supply for very light load conditions. The controller switches in bursts of pulses with a pause between bursts in which no switching is done.

CCM
Continuous Conduction Mode (CCM)

Continuous Conduction Mode is an operational mode of a switching power supply in which the current is continuously flowing and does not return to zero.

CRC
Cyclic Redundancy Check (CRC)

A cyclic redundancy check is an error-detecting code commonly used to detect accidental changes to raw data.

CV
Constant Voltage (CV)

Constant Voltage is a mode of a power supply in which the output voltage is kept constant regardless of the load.

DCM
Discontinuous Conduction Mode (DCM)

Discontinuous Conduction Mode is an operational mode of a switching power supply in which the current starts and returns to zero.

ECG
Electronic Control Gear (ECG)

An electronic control gear is a power supply which provides one or more light module(s) with the appropriate voltage or current.

Glossary

EMI
Electro-Magnetic Interference (EMI)

Also called Radio Frequency Interference (RFI), this is a (usually undesirable) disturbance that affects an electrical circuit due to electromagnetic radiation emitted from an external source. The disturbance may interrupt, obstruct, or otherwise degrade or limit the effective performance of the circuit.

GUI
Graphic User Interface (GUI)

A graphical user interface is a type of interface that allows users to interact with electronic devices through graphical icons and visual indicators.

IC
Integrated Circuit (IC)

A miniaturized electronic circuit that has been manufactured in the surface of a thin substrate of semiconductor material. An IC may also be referred to as micro-circuit, microchip, silicon chip, or chip.

LED
Light Emitting Diode (LED)

A light-emitting diode is a two-lead semiconductor light source which emits light when activated.

OCP1
Overcurrent Protection Level 1 (OCP1)

The Overcurrent Protection Level 1 is limiting the current in a switched-mode power supply to limit the power delivered to the output of the power supply.

PC
Personal Computer (PC)

A personal computer is a general-purpose computer whose size, capabilities, and original sale price make it useful for individuals, and is intended to be operated directly by an end-user with no intervening computer time-sharing models that allowed larger, more expensive minicomputer and mainframe systems to be used by many people, usually at the same time.

PF
Power Factor (PF)

Power factor is the ratio between the real power and the apparent power.

PFC
Power Factor Correction (PFC)

Power factor correction increases the power factor of an AC power circuit closer to 1 which corresponds to minimizing the reactive power of the power circuit.

QRM1
Quasi-Resonant Mode, switching in valley 1 (QRM1)

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by switching at the occurrence of the first valley of a signal which corresponds to a time when switching losses are low.

SSR
Secondary Side Regulated (SSR)

A Secondary Side Regulated power supply is controls its operation based on feedback from the secondary side of an isolated power supply.

THD
Total Harmonic Distortion (THD)

The total harmonic distortion of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

Glossary

UART
Universal Asynchronous Receiver Transmitter (UART)

A universal asynchronous receiver transmitter is used for serial communications over a peripheral device serial port by translating data between parallel and serial forms.

USB
Universal Serial Bus (USB)

Universal Serial Bus is an industry standard that defines cables, connectors and communications protocols used in a bus for connection, communication, and power supply between computers and electronic devices.

UVLO
Undervoltage Lockout (UVLO)

The Undervoltage-Lockout is an electronic circuit used to turn off the power of an electronic device in the event of the voltage dropping below the operational value.

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Edition 2018-06-06

Published by

Infineon Technologies AG

81726 Munich, Germany

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Email: erratum@infineon.com

Document reference
IFX-nvt1488278225586

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