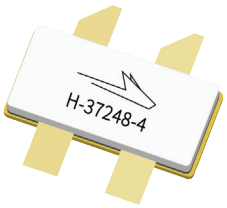
PXAC261212FC

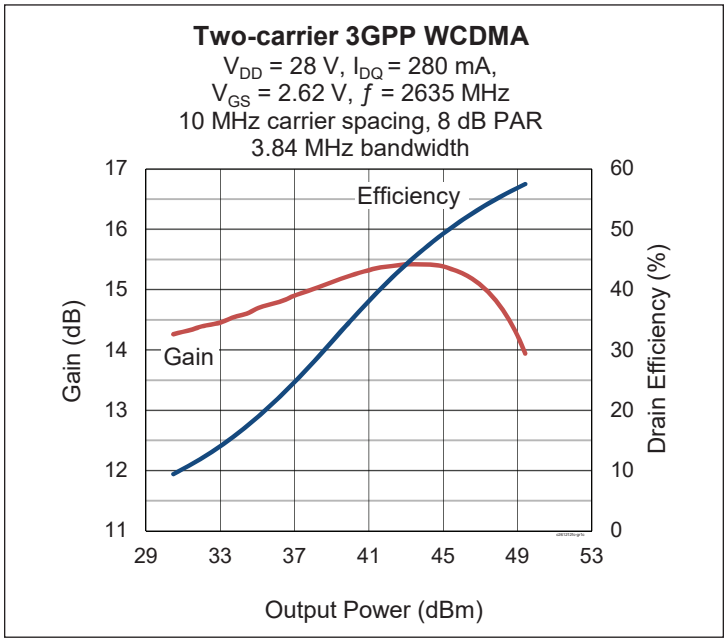
Thermally-Enhanced High Power RF LDMOS FET
120 W, 28 V, 2496 – 2690 MHz

Description

The PXAC261212FC is a 120-watt LDMOS FET with an asymmetric designed for use in multi-standard cellular power amplifier applications in the 2496 to 2690 MHz frequency band. It features dual-path design, input and output matching, and a thermally-enhanced package with earless flange. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PXAC261212FC
Package H-37248-4



Features

- Broadband internal matching
- Asymmetric design
  - Main P_{1dB} = 50 W
  - Peak P_{1dB} = 75 W
- CW performance in Doherty configuration, 2635 MHz, 28 V
  - Output power at P_{1dB} = 107 W
  - Gain = 14.4 dB
  - Efficiency = 57%
- Integrated ESD protection: Human Body Model, class 1C (per JESD22-A114)
- Capable of handling 10:1 VSWR @28 V, 120 W (CW) output power
- Low thermal resistance
- Pb-free and RoHS-compliant

RF Characteristics

Two-carrier WCDMA Specifications (tested in Wolfspeed Doherty test fixture)

V_{DD} = 28 V, $V_{GS(peak)}$ = 1.3 V, I_{DQ} = 280 mA, P_{OUT} = 28 W average, f_1 = 2630 MHz, f_2 = 2640 MHz. 3GPP WCDMA signal: 3.84 MHz bandwidth, 8 dB PAR @0.01% CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_{ps}	14.2	15.0	—	dB
Drain Efficiency	η_D	45	48	—	%
Intermodulation Distortion	IMD	—	–25	–22	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current		V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
		V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
Gate Leakage Current		V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA
On-state Resistance	(main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.19	—	Ω
	(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.16	—	Ω
Operating Gate Voltage	(main)	V_{DS} = 28 V, I_{DQ} = 280 mA	V_{GS}	2.1	2.6	3.1	V
	(peak)	V_{DS} = 28 V, I_{DQ} = 0 A	V_{GS}	0.80	1.3	1.8	V

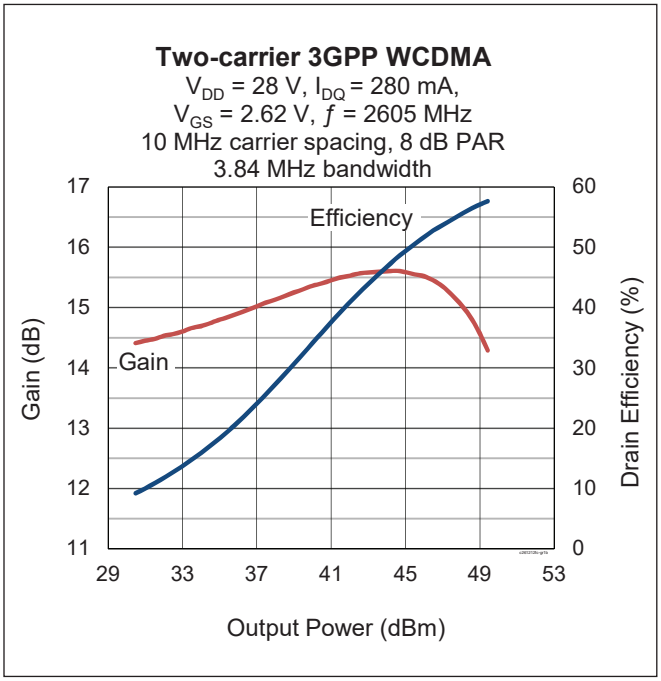
Maximum Ratings

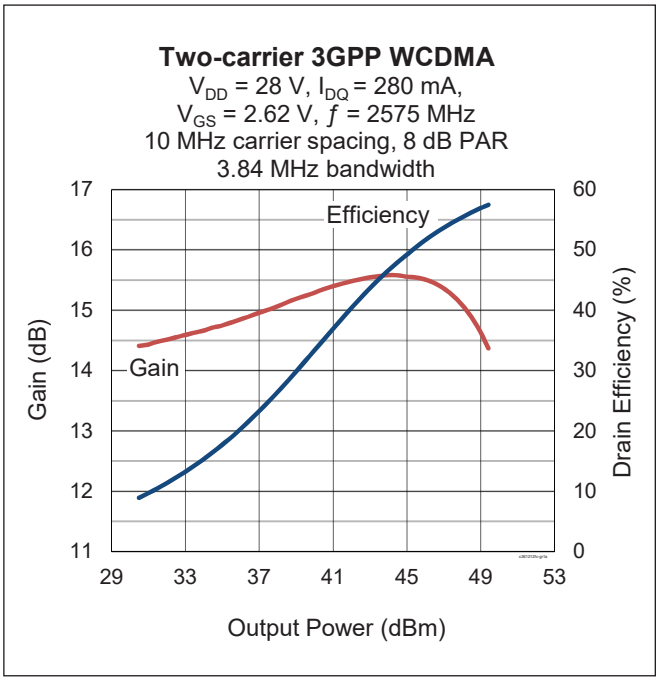
Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	65	V
Gate-source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 100 W CW)	$R_{\theta JC}$	0.61	°C/W

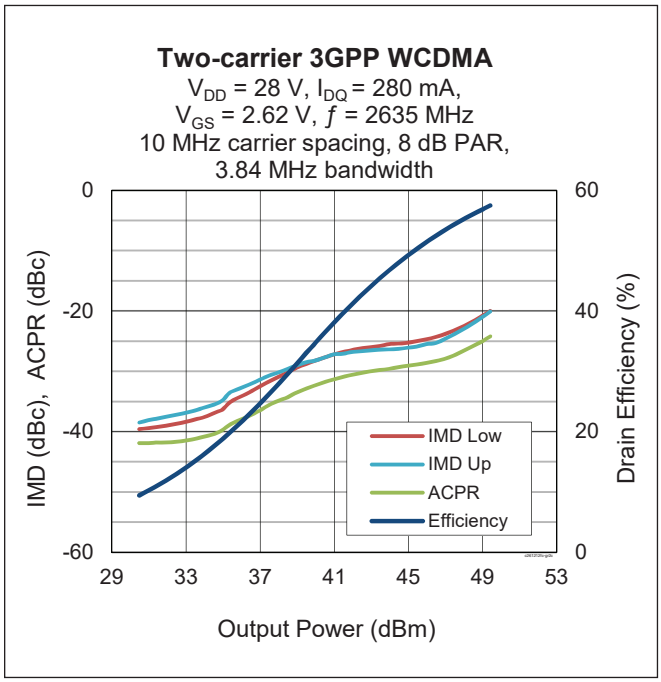
Ordering Information

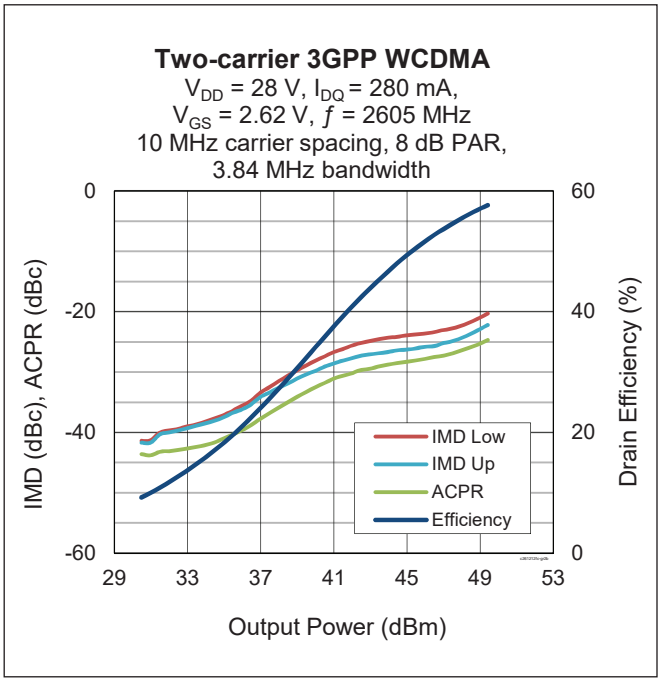
Type and Version	Order Code	Package and Description	Shipping
PXAC261212FC V1 R0	PXAC261212FC-V1-R0	H-37248-4, ceramic open-cavity, earless	Tape & Reel, 50 pcs
PXAC261212FC V1 R250	PXAC261212FC-V1-R250	H-37248-4, ceramic open-cavity, earless	Tape & Reel, 250 pcs

Typical Performance (data taken in Wolfspeed Doherty reference test fixture)



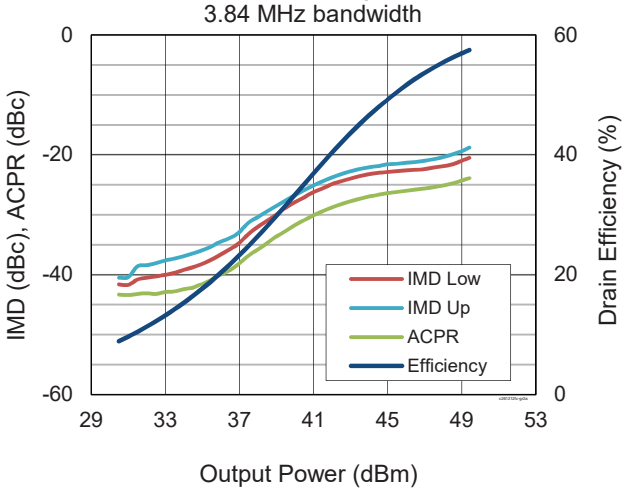




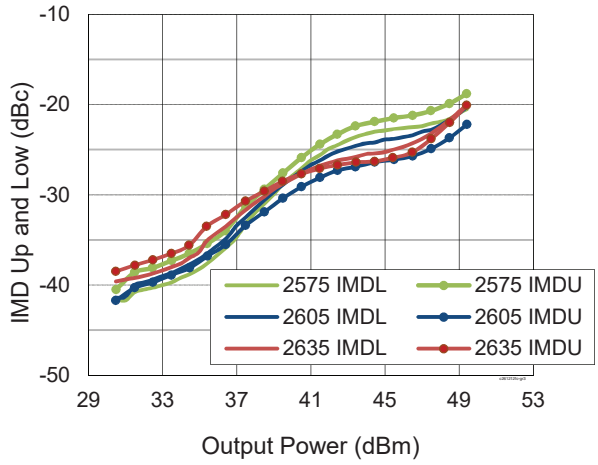


Typical Performance (cont.)

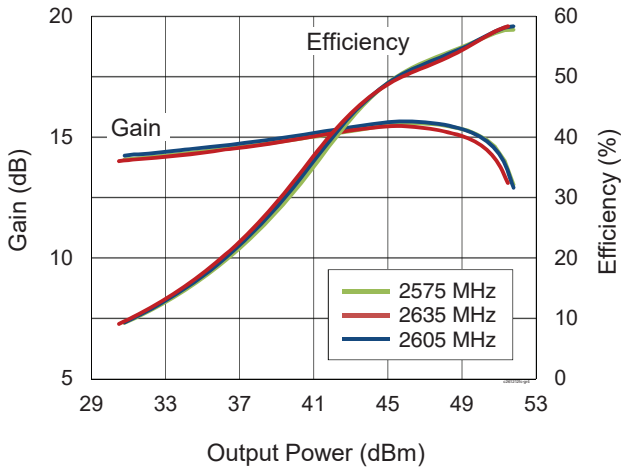
Two-carrier 3GPP WCDMA
V_{DD} = 28 V, I_{DQ} = 280 mA,
V_{GS} = 2.62 V, f = 2575 MHz
10 MHz carrier spacing, 8 dB PAR,
3.84 MHz bandwidth



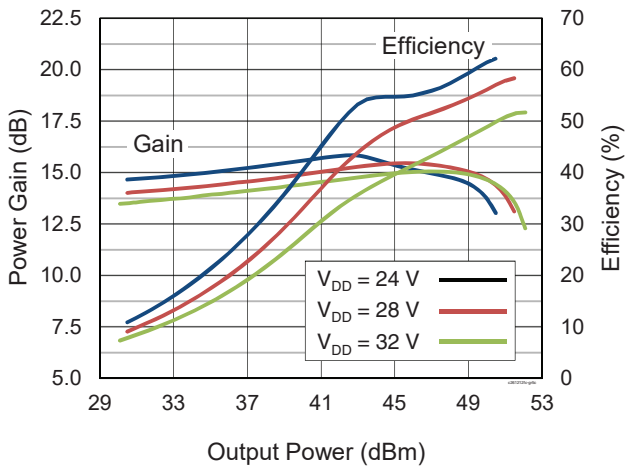
Two-carrier WCDMA Drive-up
V_{DD} = 28 V, I_{DQ} = 280 mA, V_{GS} = 2.62V,
3GPP WCDMA signal, 8 dB PAR,
10 MHz carrier spacing, 3.84 MHz BW



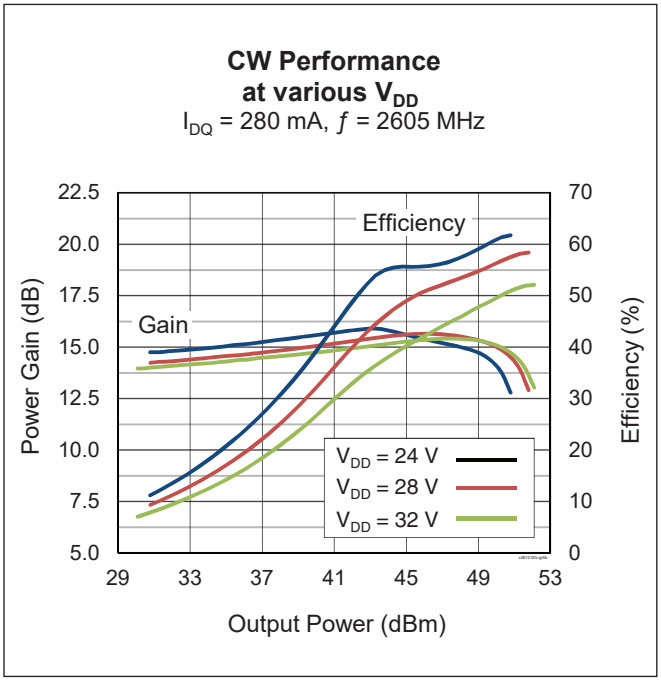
CW Performance
V_{DD} = 28 V, I_{DQ} = 280 mA

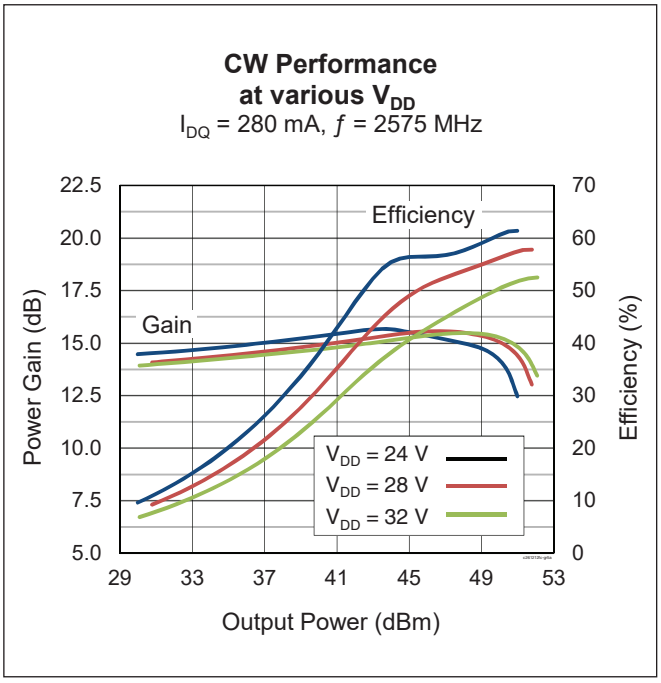


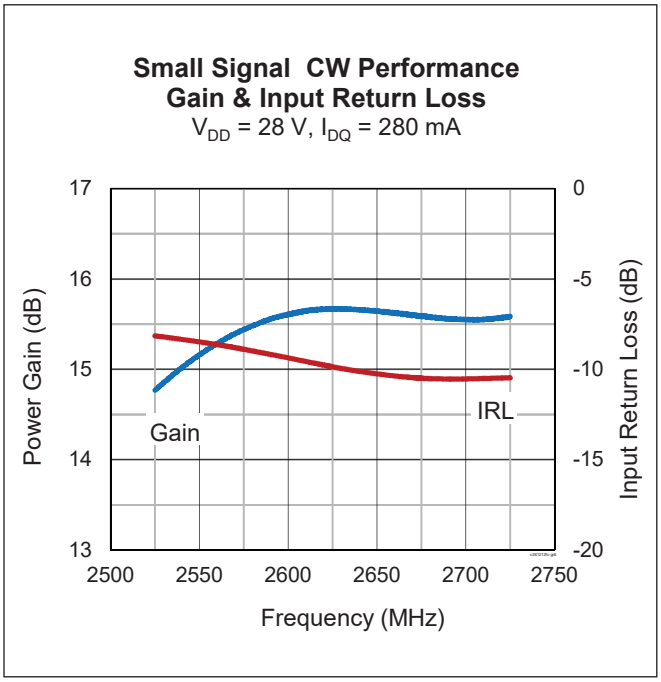
CW Performance
at various V_{DD}
I_{DQ} = 280 mA, f = 2635 MHz



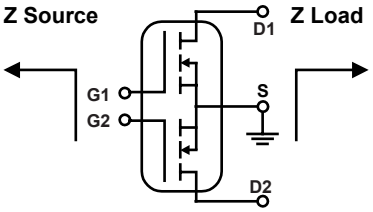
Typical Performance (cont.)







Load Pull Performance



Main side pulsed CW signal: 160 µsec, 10% duty cycle; 28 V, V_{GS} = 1.4 V, I_{DQ} = 250 mA

Class AB		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2490	5.1 – j14.5	2.8 – j5.8	16.9	48.53	71.3	52.8	6.0 – j4.2	19.1	46.90	49.0	62.4
2590	6.8 – j16.6	2.8 – j6.2	17.0	48.30	67.6	50.4	5.5 – j3.6	19.4	46.68	46.6	61.1
2690	12.9 – j17.8	2.9 – j6.0	17.2	48.30	67.6	50.4	4.5 – j3.3	19.5	46.76	47.4	60.4

Peak side pulsed CW signal: 160 µsec, 10% duty cycle; 28 V, V_{GS} = 1.4 V

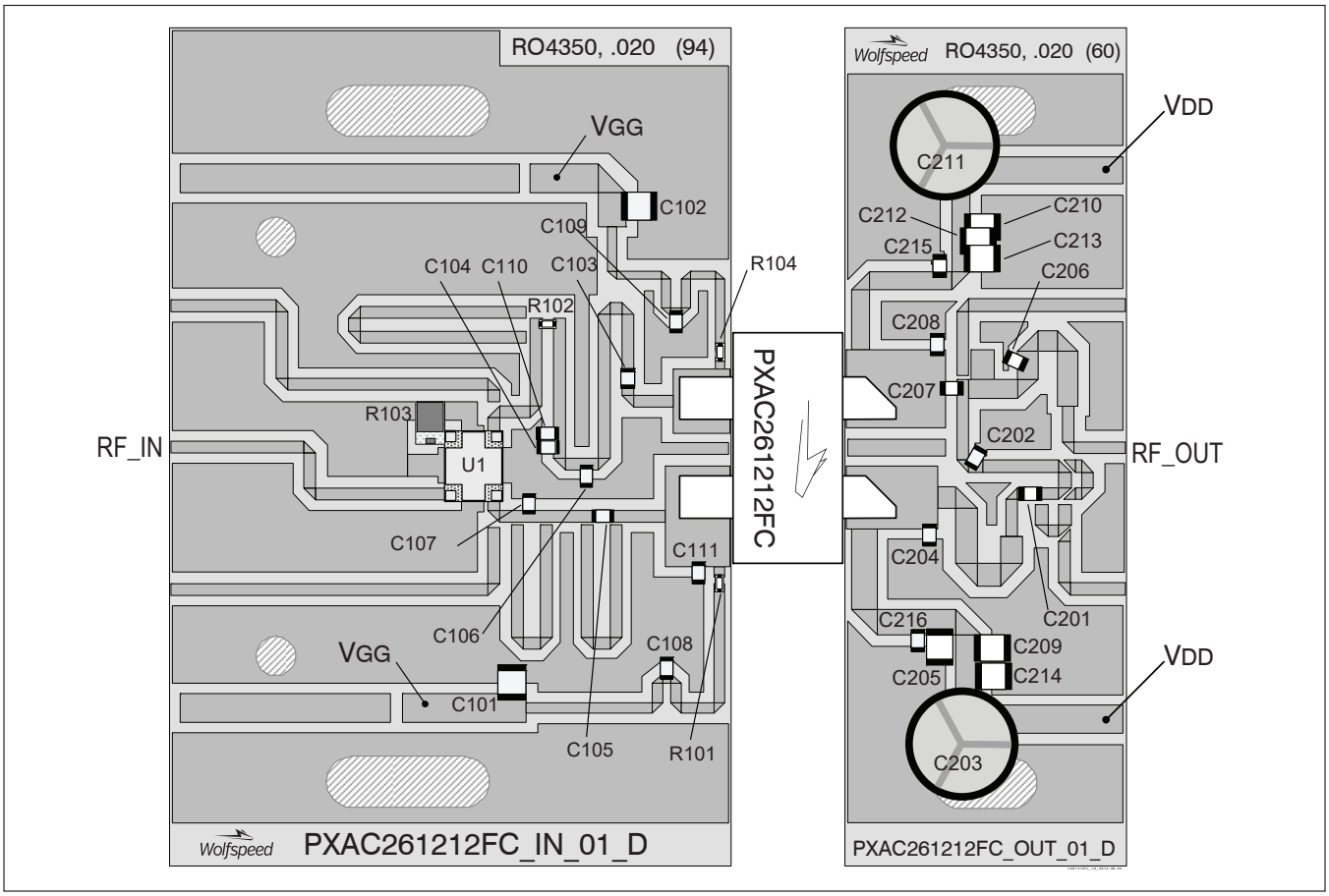
Class C		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2490	4.5 – j11.4	11.2 – j7.5	13.0	50.27	106.4	55.6	4.3 – j5.4	14.1	48.40	69.2	65.3
2590	4.7 – j12.9	13.1 – j6.3	13.4	50.08	101.9	54.1	6.0 – j6.3	14.6	48.60	72.4	63.2
2690	9.2 – j14.5	14.1 – j3.4	13.7	50.03	100.7	55.5	8.0 – j7.0	14.7	48.70	74.1	62.0

Reference Circuit, tuned for 2575 – 2675 MHz

DUT	PXAC261212FC
Test Fixture Part No.	LTA/PXAC261212FC V1
PCB	Rogers 4350, 0.508 mm [.020"] thick, 2 oz. copper, ε_r = 3.66

Find Gerber files for this reference fixture on the Wolfspeed Web site at (**www.wolfspeed.com/RF**)

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)

Assembly Information

Component	Description	Manufacturer	P/N
Input			
C101, C102	Chip capacitor, 4.7 µF	Murata Electronics North America	GRM32ER71H475KA88L
C103, C105, C108, C109	Chip capacitor, 10 pF	ATC	ATC600F100JW250T
C104	Chip capacitor, 0.4 pF	ATC	ATC600F0R4CW250T
C106, C107	Chip capacitor, 0.8 pF	ATC	ATC600F0R8AW250T
C110	Chip capacitor, 0.2 pF	ATC	ATC600F0R2AW250T
C111	Chip capacitor, 0.3 pF	ATC	ATC600F0R3CW250T
R101, R104	Resistor, 10 Ohm	Panasonic – ECG	ERJ-3GEYJ100V
R102	Resistor, 5.1k Ohm	Panasonic – ECG	ERJ-3GEYJ512V
R103	Resistor, 50 Ohm	Anaren	RFP-060120A15Z50
U1	90° RF hybrid coupler	Anaren	XC2650P-03S

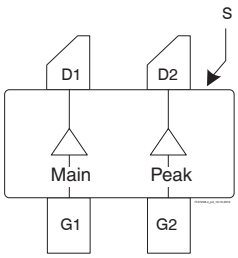
(table continued next page)

Reference Circuit (cont.)

Assembly Information (cont.)

Component	Description	Manufacturer	P/N
Output			
C201, C215, C216	Chip capacitor, 10 pF	ATC	ATC600F100JW250T
C202, C204, C211, C208	Chip capacitor, 0.5 pF	ATC	ATC600F0R5CW250T
C203	Capacitor, 220 µF	Cornell Dubilier Electronics (CDE)	SK221M050ST
C205, C209, C210, C212, C213, C214	Chip capacitor, 4.7 µF	Murata Electronics North America	GRM32ER71H475KA88L
C206	Chip capacitor, 0.3 pF	ATC	ATC600F0R3CW250T
C207	Chip capacitor, 3.9 pF	ATC	ATC600F3R9CW250T

Pinout Diagram (top view)



Pin	Description
D1	Drain device 1 (main)
D2	Drain device 2 (peak)
G1	Gate device 1 (main)
G2	Gate device 2 (peak)
S	Source (flange)

Package Outline Specifications

Package H-37248-4

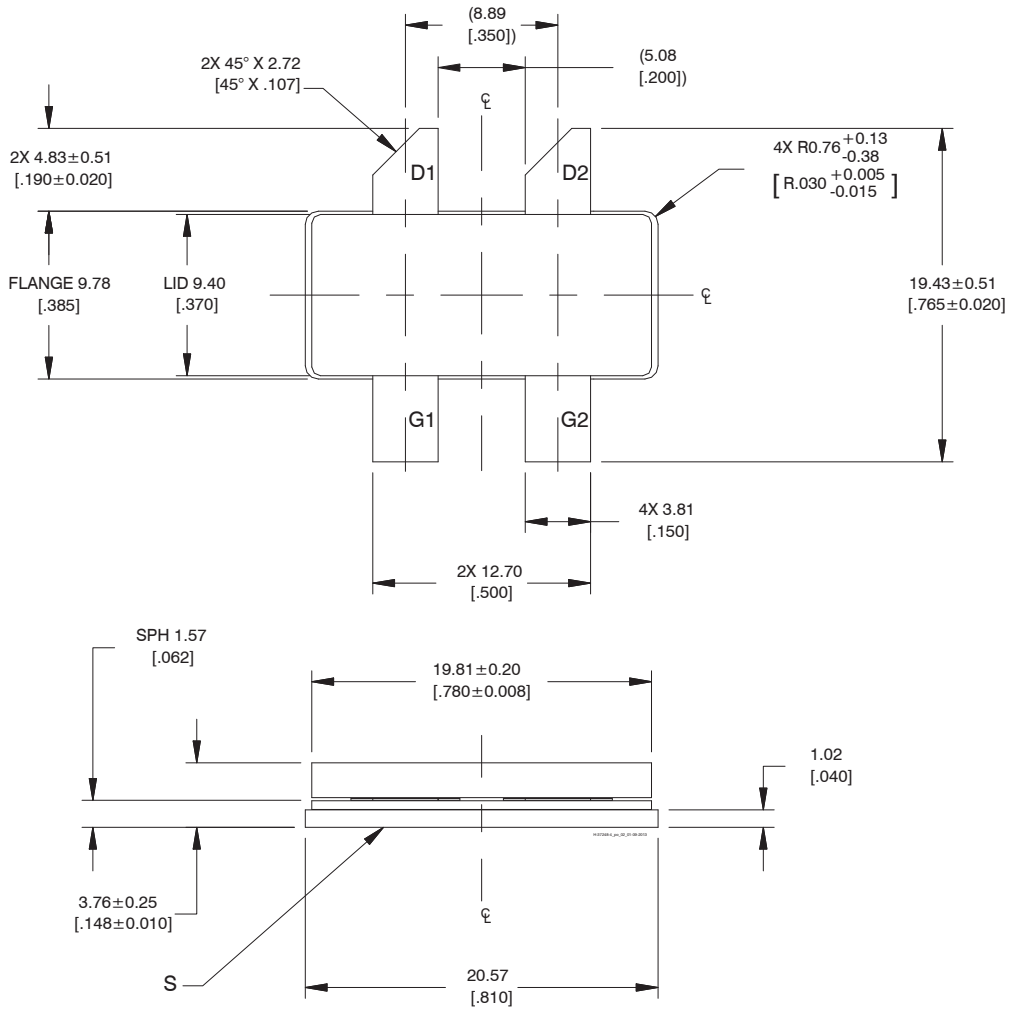


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005].
4. Pins: D1, D2 – drain, G1, G2 – gate, S – source.
5. Lead thickness: 0.10 +0.076/–0.025 [.004 +.003/–.001].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2014-03-03	Advance	all	Proposed specification for new product development.
02	2014-06-12	Production	all	Specification for production-released device.
02.1	2014-06-30	Production	1	Corrected typo in features.
02.2	2016-06-22	Production	2	Updated ordering information
03	2018-07-03	Production	All	Converted to Wolfspeed Data Sheet

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Notes

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