XC6119 Series

ETR02016-004

Voltage Detector with Delay Time Adjustable

■GENERAL DESCRIPTION

The XC6119 series is a highly precise, low power consumption voltage detector, manufactured using CMOS and laser trimming technologies.
The device includes the built-in delay circuit. A release delay time can be set freely by connecting an external delay capacitor to the Cd pin.
The device using an ultra small package (USPN-4) is suited for high density mounting applications.
Both CMOS and N-channel open drain output configurations are available.

■APPLICATIONS

- ●Microprocessor reset circuitry
- ●Charge voltage monitors
- ●Memory battery back-up switch circuits
- ●Power failure detection circuits

■FEATURES

High Accuracy : ±2%
(Detection Voltage ≥1.5V)
±30mV
(Detection Voltage <1.5V)

Low Power Consumption : 0.5μA TYP. in detect state
(V_{DF}=1.0V, V_{IN}= 0.9V)
0.9μA TYP. in release state
(V_{DF}=1.0V, V_{IN}= 1.1V)

Detect Voltage Options : 0.8V ~ 5.0V (0.1V increments)

Operating Voltage Range : 0.7V ~ 6.0V

Detect Voltage Temperature Characteristics
: ±100ppm/ °C TYP.

Output Configuration : CMOS or
N-channel open drain

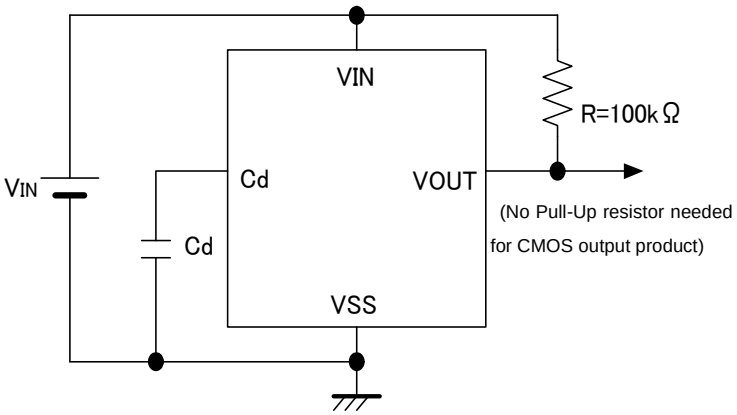
Built-In Delay Circuit : Delay Time Adjustable

Operating Ambient Temperature : -40 °C ~ +85 °C

Packages : SSOT-24, USPN-4

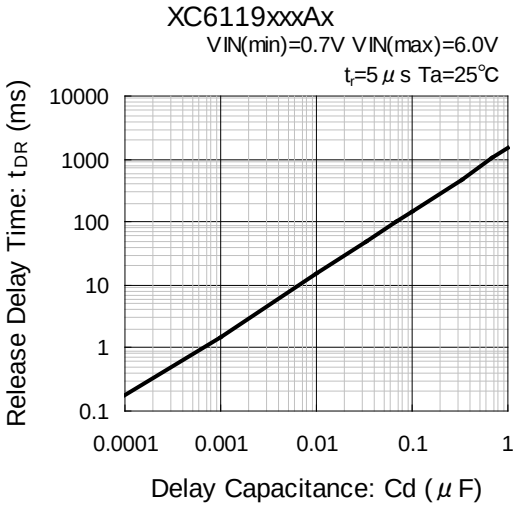
Environmentally Friendly : EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT



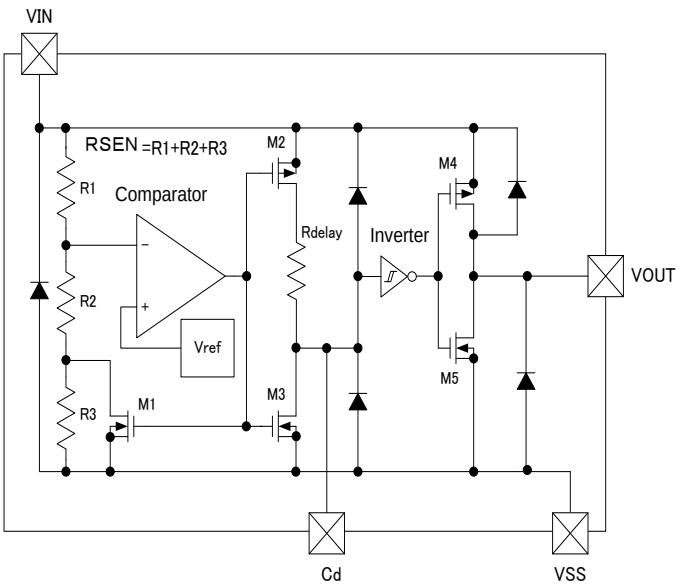
■TYPICAL PERFORMANCE CHARACTERISTICS

●Release Delay Time vs. Delay Capacitance

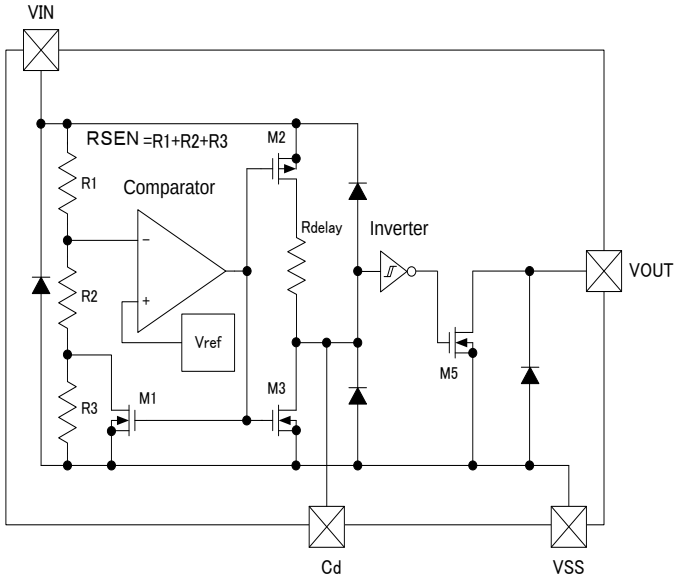


■BLOCK DIAGRAMS

(1) XC6119C (CMOS Output)



(2) XC6119N (N-ch Open Drain Output)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

■PRODUCT CLASSIFICATION

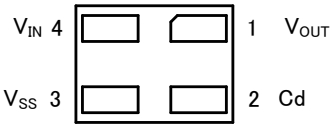
●Ordering Information

XC6119①②③④⑤⑥−⑦(*1)

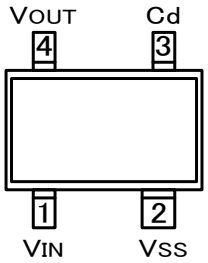
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
②③	Detect Voltage	08 ~ 50	e.g. 18→1.8V
④	Output Delay & Hysteresis	A	Built-in delay pin & hysteresis 5% (TYP.)
⑤⑥-⑦	Packages (Order Unit)	7R-G	USPN-4 (5,000pcs/Reel)
		NR-G	SSOT-24 (3,000pcs/Reel)

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

■PIN CONFIGURATION



USPN-4
(BOTTOM VIEW)



SSOT-24
（TOP VIEW）

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
USPN-4	SSOT-24		
1	4	V_{OUT}	Output (Detect ”L”)
2	3	Cd	Delay Capacitance
3	2	V_{SS}	Ground
4	1	V_{IN}	Input

■PIN FUNCTIOS ASSIGNMENT

V_{IN}	V_{CD}	V_{OUT} transition *		
		①		②
L	L	L	⇒	L
	H			
	L	H		
	H			
H	L	L	⇒	L
	H		⇒	H
	L	H	⇒	
	H			

∗ Function State Transition Example
1) When V_{OUT} is "L", V_{OUT} changes from "L" to "H" when V_{IN} = "H" ($V_{DR} \leq V_{IN}$) and V_{CD} = "H" ($V_{TCD} \leq V_{CD}$).
2) When V_{OUT} changes from "H" to "L" and V_{IN} = "H" and V_{CD} = "L" when V_{OUT} is "H", V_{OUT} holds "H".

●PIN LOGIC CONDITIONS

(1) XC6119C(CMOS)

PIN NAME	LOGIC	CONDITIONS
V_{IN}	L	$V_{IN} \leqq V_{DF}$
	H	$V_{IN} \geqq V_{DF}+V_{HYS}$
Cd	L	$0 < V_{CD} < V_{IN}/2 - 0.1$
	H	$V_{IN}/2 + 0.1 \leqq V_{CD} \leqq V_{IN}$
V_{OUT}	L	$V_{OUT} \leqq V_{IN} \times 0.1$
	H	$V_{OUT} \geqq V_{IN} \times 0.9$

(2) XC6119N(Nch open drain output)

PIN NAME	LOGIC	CONDITIONS
V_{IN}	L	$V_{IN} \leqq V_{DF}$
	H	$V_{IN} \geqq V_{DF}+V_{HYS}$
Cd	L	$0 < V_{CD} < V_{IN}/2 - 0.1$
	H	$V_{IN}/2 + 0.1 \leqq V_{CD} \leqq V_{IN}$
V_{OUT}	L	$V_{OUT} \leqq$ Pull-Up voltage × 0.1
	H	$V_{OUT} \geqq$ Pull-Up voltage × 0.9

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	V_{SS}-0.3～+7.0	V
Output Current		I_{OUT}	10	mA
Output Voltage	XC6119C (*1)	V_{OUT}	V_{SS}-0.3～V_{IN}+0.3	V
	XC6119N (*2)		V_{SS}-0.3～+7.0	
Delay Pin Voltage		V_{CD}	V_{SS}-0.3～V_{IN}+0.3	V
Delay Pin Current		I_{CD}	5.0	mA
Power Dissipation	USPN-4	Pd	100	mW
			600(40mm x 40mm Standard board) (*3)	
	SSOT-24		150	
			500 (40mm x 40mm Standard board) (*3)	
Operating Ambient Temperature		Ta	-40～+85	ºC
Storage Temperature		Tstg	-55～+125	ºC

NOTE:
(*1) CMOS output
(*2)N-ch open drain output
(*3)The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
Operating Voltage	V_{IN}	$V_{DF(T)}$=0.8～5.0V (*1)	0.7		6.0	V	-
Detect Voltage	V_{DF}	$V_{DF(T)}$=0.8～5.0V	E-1			V	①
Hysteresis Width	V_{HYS}	V_{IN}=1.0～6.0V	V_{DF} ×0.02	V_{DF} ×0.05	V_{DF} ×0.08	V	①
Supply Current 1	I_{SS1}	V_{IN}=V_{DF} ×0.9 $V_{DF(T)}$=0.8～1.9V $V_{DF(T)}$=2.0～3.9V $V_{DF(T)}$=4.0～5.0V		0.5 0.6 0.7	1.2 1.3 1.4	μA	②
Supply Current 2	I_{SS2}	V_{IN}=V_{DF} ×1.1 $V_{DF(T)}$=0.8～1.9V $V_{DF(T)}$=2.0～3.9V $V_{DF(T)}$=4.0～5.0V		0.9 1.1 1.2	1.8 2.0 2.2	μA	②
Output Current	I_{OUT1}	V_{IN}=0.7V V_{DS}=0.5V(Nch)	0.01	0.36		mA	③
		V_{IN}=1.0V(*2) V_{DS}=0.5V(Nch)	0.1	0.7			
		V_{IN}=2.0V(*3) V_{DS}=0.5V(Nch)	0.8	1.6			
		V_{IN}=3.0V(*4) V_{DS}=0.5V(Nch)	1.2	2.0			
		V_{IN}=4.0V(*5) V_{DS}=0.5V(Nch)	1.6	2.3			
	I_{OUT2} (*6)	V_{IN}=VDF ×1.1 V_{DS}=0.5V(Pch)	E-2			mA	④
Leakage Current: CMOS output (P-ch)	I_{LEAK}	V_{IN} = V_{DF} ×0.9V, V_{OUT} = 0V, Cd: Open		-0.20		μA	③
Leakage Current: N-ch Open Drain Output		V_{IN} = 6.0V, V_{OUT} = 6.0V, Cd: Open		0.20	0.40		
Temperature Characteristics	ΔV_{DF}/(ΔTa・V_{DF})	-40ºC≦T_a≦85ºC		±100		ppm/ºC	①
Delay Resistance (*7)	R_{DELAY}	V_{IN}=6.0V, Cd=0V	1.6	2.0	2.4	MΩ	⑤
Delay Pin Sink Current	I_{CD}	Cd=0.5V, V_{IN}=0.7V	8	60		μA	⑤
Delay Capacitance Pin Threshold Voltage	V_{TCD}	V_{IN}=1.0V	0.4	0.5	0.6	V	⑥
		V_{IN}=6.0V	2.9	3.0	3.1		
Unspecified Operating Voltage (*8)	V_{UNS}	V_{IN}=0～0.7V		0.3	0.4	V	⑦
Detect Delay Time (*9)	t_{DF0}	V_{IN}=6.0→0.7V Cd: Open		30	230	μs	⑧
Detect Delay Time (*9)	t_{DR0}	V_{IN}=0.7V→6.0V Cd: Open		30	200	μs	⑧

NOTE:

(*1) $V_{DF(T)}$: Setting Detect Voltage

(*2) $V_{DF(T)}$＞1.0V

(*3) $V_{DF(T)}$＞2.0V

(*4) $V_{DF(T}$＞3.0V

(*5) $V_{DF(T)}$＞4.0V

(*6) This numerical value is applied only to the XC6119C series (CMOS output).

(*7) Calculated from the voltage value and the current value of both ends of the resistor.

(*8) The maximum voltage of the V_{OUT} in the range of the V_{IN} 0 to 0.7V. This numerical value is applied only to the XC6119C series (CMOS output).

(*9) Time which ranges from the state of V_{IN} =V_{DF} to the V_{OUT} reaching 0.6V when the V_{IN} falls without connecting to the Cd pin.

(*10) Time which ranges from the state of V_{IN}= V_{DF} +V_{HYS} to the V_{OUT} reaching 5.4V when the V_{IN} rises without connecting to the Cd pin.

■VOLTAGE CHART

SYMBOL	E-1			E-2	
PARAMETER / SETTING DETECT VOLTAGE	DETECT VOLTAGE (*1) (V)			OUTPUT CURRENT (*2) (mA)	
$V_{DF(T)}$	V_{DF}			I_{OUT2}	
	MIN.	TYP.	MAX.	MIN.	TYP.
0.8	0.770	0.8	0.830	-0.40	-0.20
0.9	0.870	0.9	0.930		
1.0	0.970	1.0	1.030		
1.1	1.070	1.1	1.130	-0.60	-0.30
1.2	1.170	1.2	1.230		
1.3	1.270	1.3	1.330		
1.4	1.370	1.4	1.430		
1.5	1.470	1.5	1.530	-0.80	-0.40
1.6	1.568	1.6	1.632		
1.7	1.666	1.7	1.734		
1.8	1.764	1.8	1.836		
1.9	1.862	1.9	1.938		
2.0	1.960	2.0	2.040	-1.00	-0.50
2.1	2.058	2.1	2.142		
2.2	2.156	2.2	2.244		
2.3	2.254	2.3	2.346		
2.4	2.352	2.4	2.448		
2.5	2.450	2.5	2.550		
2.6	2.548	2.6	2.652		
2.7	2.646	2.7	2.754		
2.8	2.744	2.8	2.856		
2.9	2.842	2.9	2.958		
3.0	2.940	3.0	3.060	-1.20	-0.60
3.1	3.038	3.1	3.162		
3.2	3.136	3.2	3.264		
3.3	3.234	3.3	3.366		
3.4	3.332	3.4	3.468		
3.5	3.430	3.5	3.570		
3.6	3.528	3.6	3.672		
3.7	3.626	3.7	3.774		
3.8	3.724	3.8	3.876		
3.9	3.822	3.9	3.978		
4.0	3.920	4.0	4.080	-1.30	-0.65
4.1	4.018	4.1	4.182		
4.2	4.116	4.2	4.284		
4.3	4.214	4.3	4.386		
4.4	4.321	4.4	4.488		
4.5	4.410	4.5	4.590		
4.6	4.508	4.6	4.692		
4.7	4.606	4.7	4.794		
4.8	4.704	4.8	4.896		
4.9	4.802	4.9	4.998		
5.0	4.900	5.0	5.100		

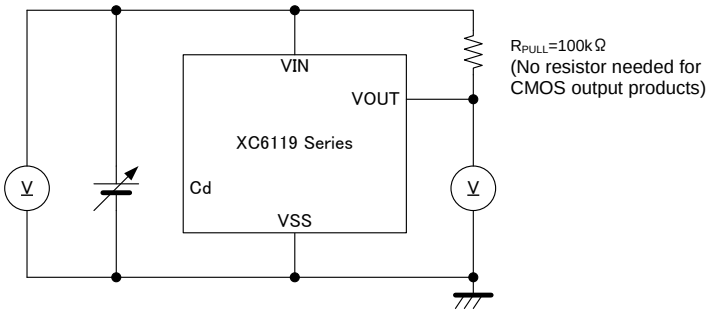
NOTE:

(*1) When $V_{DF(T)} \leqq 1.4V$, the detection accuracy is ±30mV. When $V_{DF(T)} \geqq 1.5V$, the detection accuracy is ±2%.

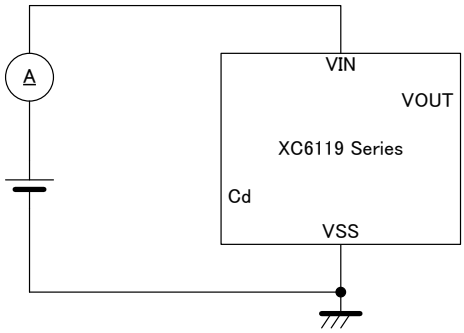
(*2) This numerical value is applied only to the XC6119C series (CMOS output).

■TEST CIRCUITS

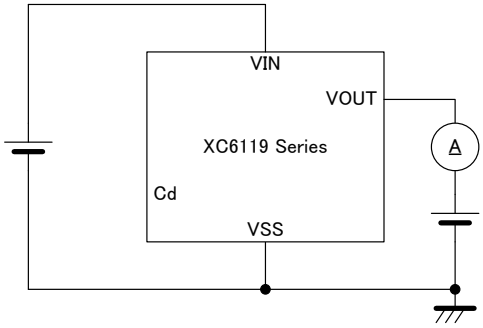
Circuit ①



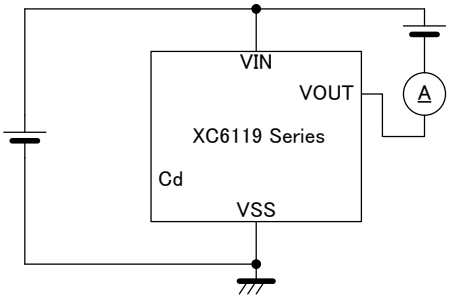
Circuit ②



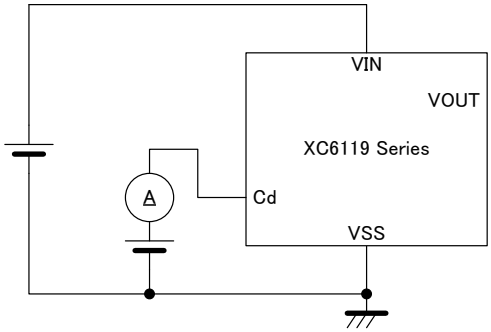
Circuit ③



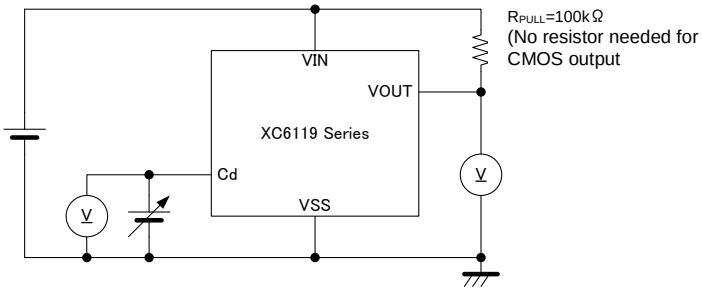
Circuit ④



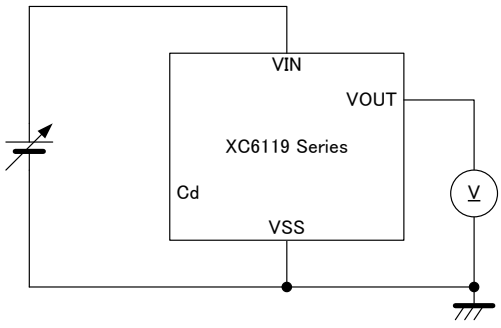
Circuit ⑤



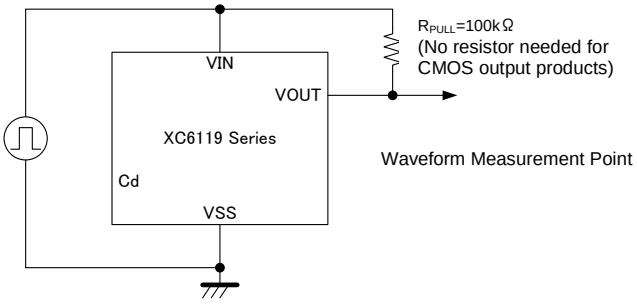
Circuit ⑥



Circuit ⑦



Circuit ⑧



■OPERATIONAL EXPLANATION

A typical circuit example is shown in Figure 1, and the timing chart of Figure 1 is shown in Figure 2 on the next page.

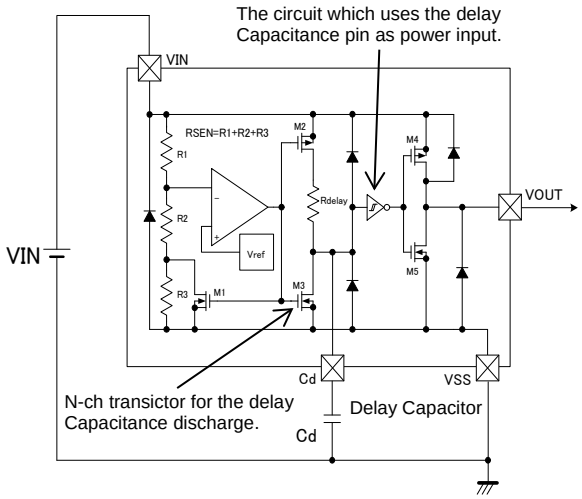


Figure 1: Typical application circuit example

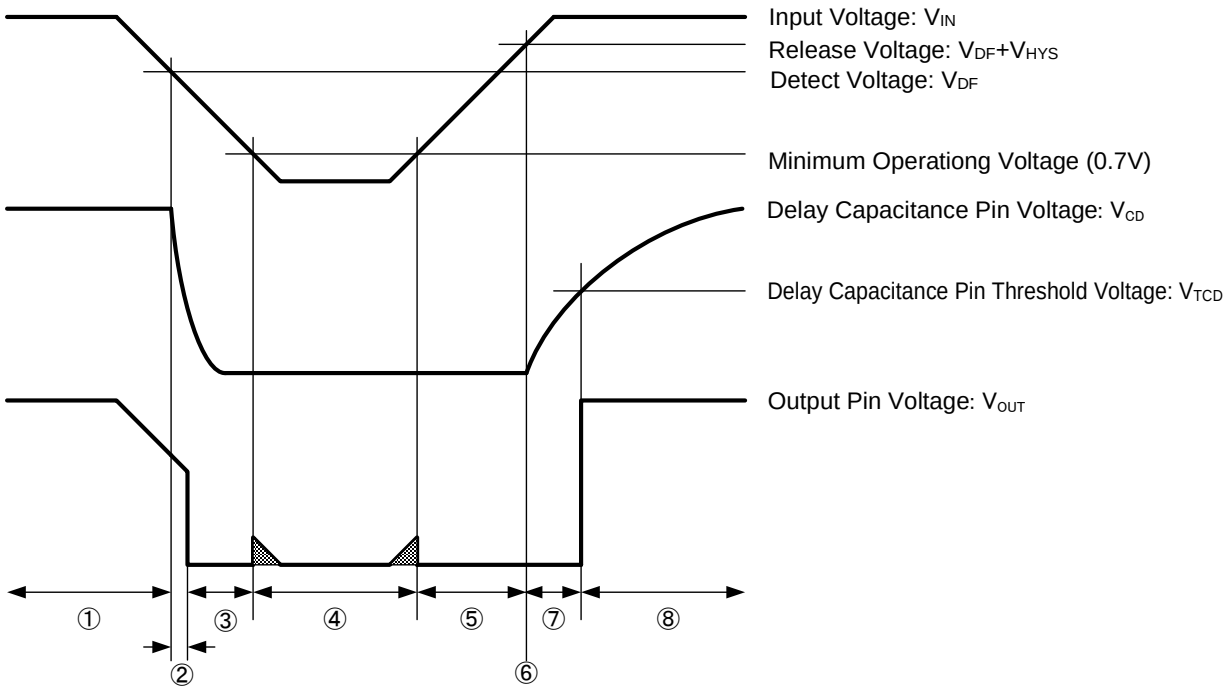


Figure 2: The timing chart of Figure 1

① As an early state, the input voltage pin is applied sufficiently high voltage to the release voltage and the delay capacitance (Cd) is charged to the input pin voltage. While the input pin voltage (V_{IN}) starts dropping to reach the detect voltage (V_{DF}) ($V_{IN} > V_{DF}$), the output voltage (V_{OUT}) keeps the "High" level (=V_{IN}).

② When the input pin voltage keeps dropping and becomes equal to the detect voltage ($V_{IN} = V_{DF}$), an N-ch transistor for the delay capacitance discharge is turned ON, and starts to discharge the delay capacitance. For the internal circuit, which uses the delay capacitance pin as power input, the reference voltage operates as a comparator of VIN, and the output voltage changes into the "Low" level ($\leqq V_{IN} \times 0.1$). The detect delay time (t_{DF}) is defined as time which ranges from $V_{IN} = V_{DF}$ to the V_{OUT} of "Low" level (especially, when the Cd pin is not connected: t_{DF0}).

③ While the input pin voltage keeps below the detect voltage, and 0.7V or more, the delay capacitance is discharged to the ground voltage (=V_{SS}) level. Then, the output voltage (V_{OUT}) maintains the "Low" level.

④ While the input pin voltage drops to less than 0.7V and it increases again to 0.7V or more, the output voltage may not be able to maintain the "Low" level. Such an operation is called "Unspecified Operation", and voltage which occurs at the output pin voltage is defined as unstable operating voltage (V_{UNS}).

■OPERATIONAL EXPLANATION (Continued)

⑤ While the input pin voltage increases more than 0.7V and it reaches to the release voltage level ($V_{IN} < V_{DF} + V_{HYS}$), the output voltage ($V_{OUT}$) maintains the “Low” level.

⑥ When the input pin voltage continues to increase more than 0.7V up to the release voltage level (= $V_{DF} + V_{HYS}$), the N-ch transistor for the delay capacitance discharge will be turned OFF, and the delay capacitance will be started discharging via a delay resistor (R_{DELAY}). The internal circuit, which uses the delay capacitance pin as power input, will operate as a hysteresis comparator (Rise Logic Threshold: $V_{TLH}=V_{TCD}$, Fall Logic Threshold: $V_{THL}=V_{SS}$) while the input pin voltage keeps higher than the detect voltage ($V_{IN} > V_{DF}$).

⑦ While the input pin voltage becomes equal to the release voltage or higher and keeps the detect voltage or higher, the delay capacitance (Cd) will be charged up to the input pin voltage. When the delay capacitance pin voltage (V_{CD}) reaches to the delay capacitance pin threshold voltage (V_{TCD}), the output voltage changes into the “High” (=V_{IN}) level. t_{DR} is defined as time which ranges from $V_{IN}=V_{DF}+V_{HYS}$ to the V_{OUT} of “High” level (especially when the Cd pin is not connected: t_{DR0}). t_{DR} can be given by the formula (1).

$$t_{DR} = -R_{DELAY} \times Cd \times In\,(1 - V_{TCD} / VIN) + t_{DR0} \quad \cdots(1)$$

* In = a natural logarithm

The release delay time can also be briefly calculated with the formula (2) because the delay resistance is 2.0MΩ (TYP.) and the delay capacitance pin threshold voltage is $V_{IN}/2$ (TYP.)

$$t_{DR}=R_{DELAY} \times Cd \times 0.69 \quad \cdots(2)$$

* R_{DELAY} is 2.0MΩ (TYP.)

As an example, presuming that the delay capacitance is 0.68μF, t_{DR} is :

$$2.0 \times 10^{6} \times 0.68 \times 10^{-6} \times 0.69 = 938(ms)$$

* Note that the release delay time may remarkably be short when the delay capacitance is not discharged to the ground (=V_{SS}) level because time described in ③ is short.

⑧ While the input pin voltage is higher than the detect voltage ($V_{IN} > V_{DF}$), therefore, the output voltage maintains the “High”(=V_{IN}) level.

●Release Delay Time Chart

Delay Capacitance [Cd] (μF)	Release Delay Time [t_{DR}] (TYP.) (ms)	Release Delay Time [t_{DR}] (MIN. ~ MAX.) *1 (ms)
0.01	13.8	11.0 ~ 16.6
0.022	30.4	24.3 ~ 36.4
0.047	64.9	51.9 ~ 77.8
0.1	138	110 ~ 166
0.22	304	243 ~ 364
0.47	649	519 ~ 778
1	1380	1100 ~ 1660

* The release delay time values above are calculate by using formula (2).

(*1)The release delay time (t_{DR}) is influenced by the release capacitance (Cd).

■NOTES ON USE

1. Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. The input pin voltage drops by the resistance between power supply and the V_{IN} pin, and by through current at operation of the IC. At this time, the operation may be wrong if the input pin voltage falls below the minimum operating voltage range. In CMOS output, for output current, drops in the input pin voltage similarly occur. Oscillation of the circuit may occur if the drops in voltage, which caused by through current at operation of the IC, exceed the hysteresis voltage. Note it especially when you use the IC with the V_{IN} pin connected to a resistor.
3. Note that a rapid and high fluctuation of the input pin voltage may cause a wrong operation.
4. Power supply noise may cause an operational function error. Care must be taken to put an external capacitor between V_{IN}-GND and test on the board carefully.
5. When there is a possibility of which the input pin voltage falls rapidly (e.g.: 6.0V to 0V) at release operation with the delay capacitance pin (Cd) connected to a capacitor, use a schottky barrier diode connected between the VIN pin and the Cd pin as the Figure 3 shown below.
6. When N-channel open drain output is used, output voltages V_{OUT} at voltage detection and release are determined by a pull-up resistor tied to the output pin. A resistance value of the pull-up resistor can be selected with referring to the followings. (Refer to Figure 4)

During detection, the formula is given as

$$V_{OUT}=V_{PULL}/(1+R_{PULL}/R_{ON})$$

where V_{PULL} is pull-up voltage and R_{ON} (*1) is ON resistance of N-channel driver M5 ($R_{ON}=V_{DS}/I_{OUT1}$ from the electrical characteristics table).

For example, when V_{IN}=2.0V (*2), $R_{ON} = 0.5/0.8\times10^{-3}=625\Omega$ (MIN.) and if you want to get V_{OUT} less than 0.1V when V_{PULL}=3.0V, R_{PULL} can be calculated as follows;

$$R_{PULL}=(V_{PULL}/V_{OUT}-1)\times R_{ON}=(3/0.1-1)\times 625\fallingdotseq 18\,k\,\Omega$$

Therefore, pull-up resistance should be selected 18kΩ or higher.

(*1) V_{IN} is smaller, R_{ON} is bigger

(*2) For the calculation, the lowest V_{IN} should be used among of the V_{IN} range

During release, the formula is given as

$$V_{OUT}=V_{PULL}/(1+R_{PULL}/R_{OFF})$$

where V_{PULL} is pull-up voltage R_{OFF} is OFF resistance of N-channel driver M5 ($R_{OFF}=V_{OUT}/I_{LEAK}$=15MΩ from the electrical characteristics table)

For examples, if you want to get V_{OUT} larger than 5.99V when V_{PULL} is 6.0V, R_{PULL} can be calculated as follows;

$$R_{PULL}=(V_{PULL}/V_{OUT}-1)\times R_{OFF}=(6/5.99-1)\times 15\times 10^{6}\fallingdotseq 25k\Omega$$

Therefore, pull-up resistance should be selected 25kΩ or below.

7. Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

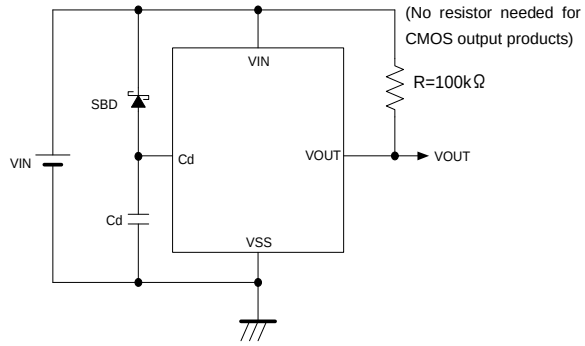
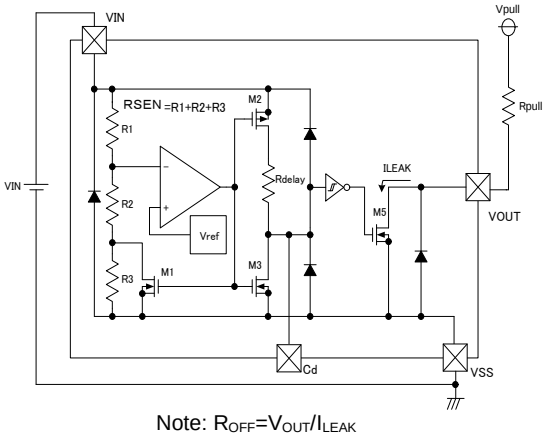


Figure 3: Circuit example with the delay capacitance pin (Cd) connected to a schottky barrier diode



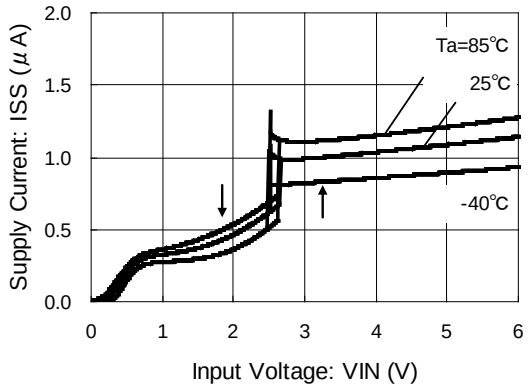
Note: $R_{OFF}=V_{OUT}/I_{LEAK}$

Figure 4: Circuit example of XC6109N Series

■TYPICAL PERFORMANCE CHARACTERISTICS

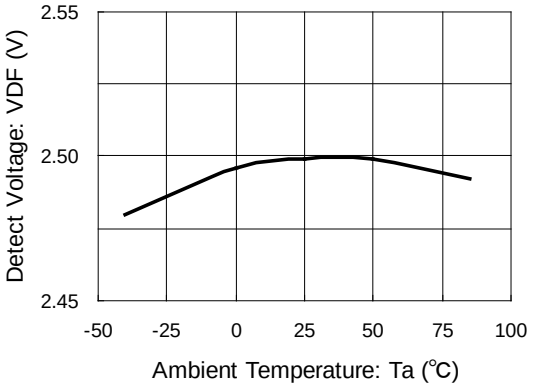
(1) Supply Current vs. Input Voltage

XC6119x25Ax



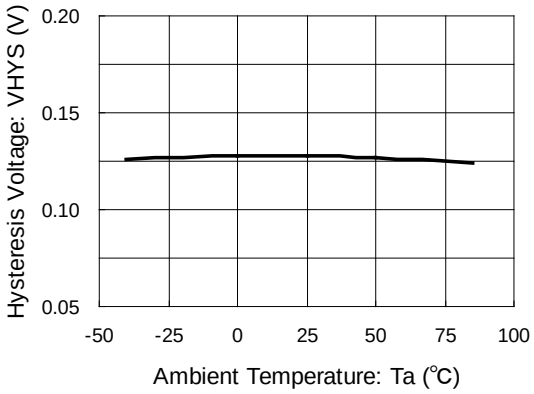
(2) Detect Voltage vs. Ambient Temperature

XC6119x25Ax



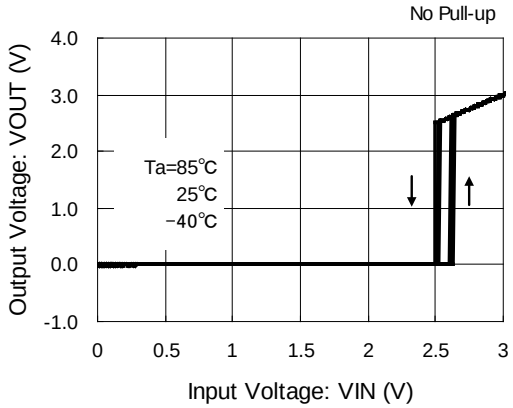
(3) Hysteresis Voltage vs. Ambient Temperature

XC6119x25Ax

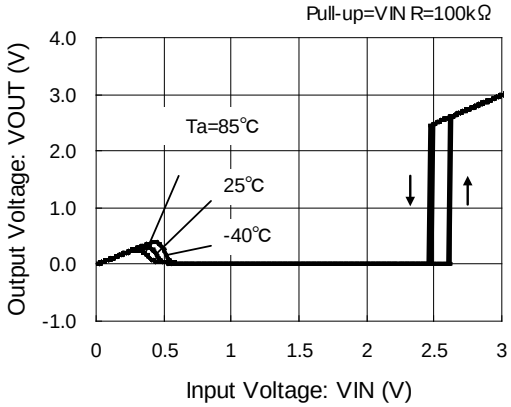


(4) Output Voltage vs. Input Voltage

XC6119C25Ax



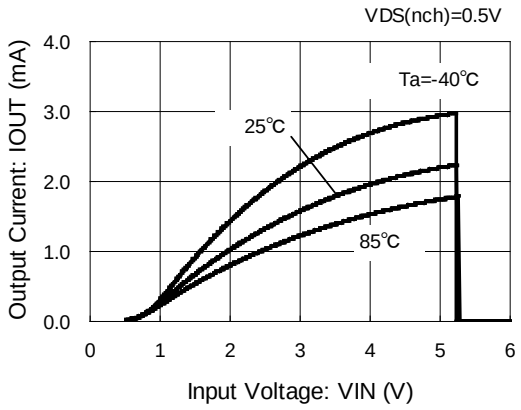
XC6119N25Ax



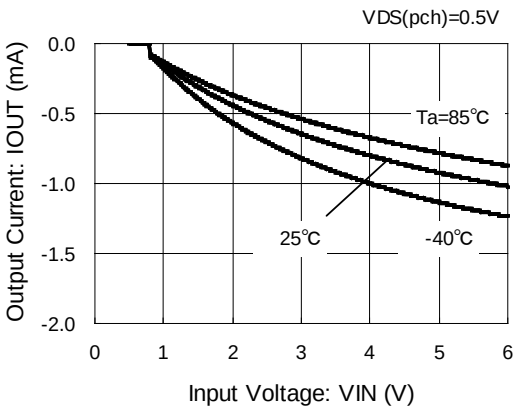
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(5) Output Current vs. Input Voltage

XC6119x50Ax

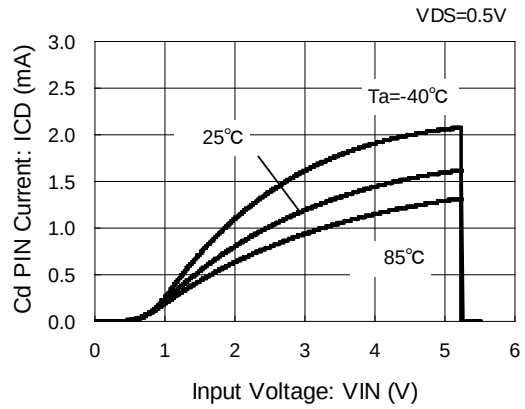


XC6119C08Ax



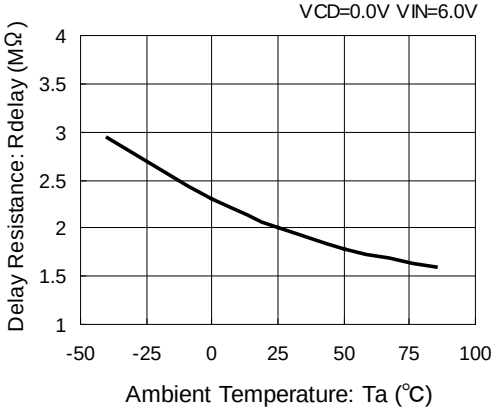
(6) Cd Pin Sink Current vs. Input Voltage

XC6119x50Ax



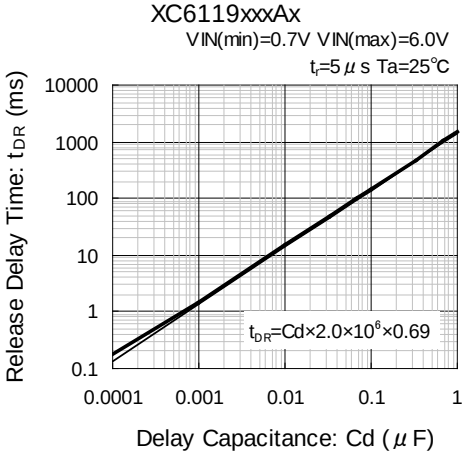
(7) Delay Resistance vs. Ambient Temperature

XC6119xxxAx



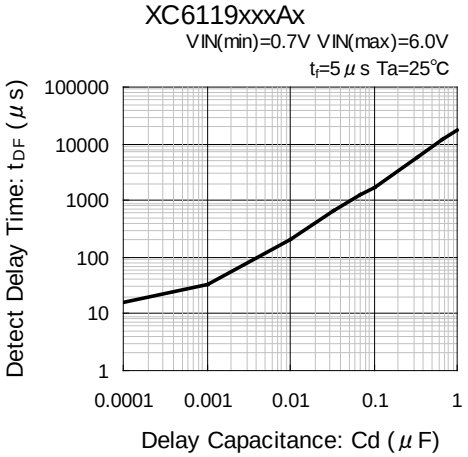
(8) Release Delay Time vs. Delay Capacitance

XC6119xxxAx



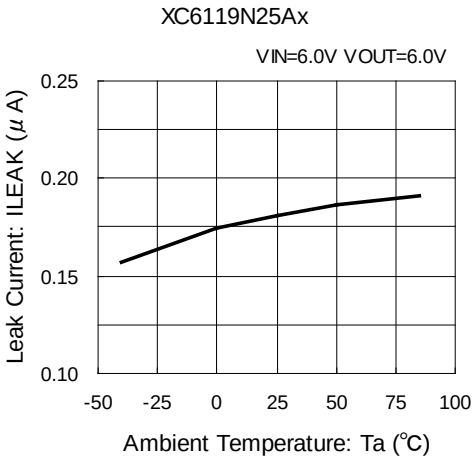
(9) Detect Delay Time vs. Delay Capacitance

XC6119xxxAx

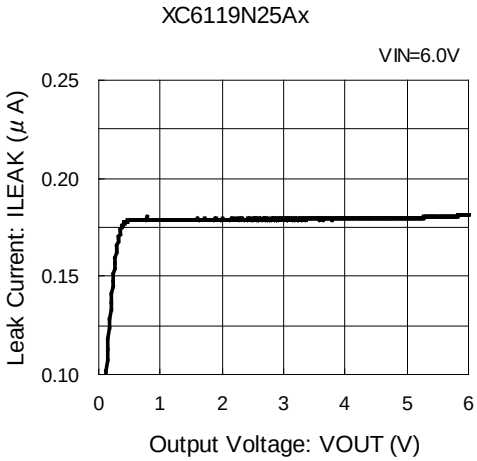


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(10) Leak Current vs. Ambient Temperature



(11) Leak Current vs. Supply Voltage



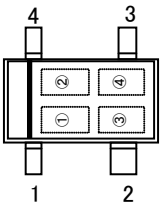
■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS	
SSOT-24	SSOT-24 PKG	Standard Board	SSOT-24 Power Dissipation
USPN-4	USPN-4 PKG	Standard Board	USPN-4 Power Dissipation

■MARKING RULE

●SSOT-24



SSOT-24
(TOP VIEW)

① represents output configuration and integer number of detect voltage

CMOS Output (XC6119C Series)

MARK	VOLTAGE (V)	PRODUCT SERIES
A	0.X	XC6119C0**N*
B	1.X	XC6119C1**N*
C	2.X	XC6119C2**N*
D	3.X	XC6119C3**N*
E	4.X	XC6119C4**N*
F	5.X	XC6119C5**N*

N-channel Open Drain Output (XC6119N Series)

MARK	VOLTAGE (V)	PRODUCT SERIES
H	0.X	XC6119N0**N*
K	1.X	XC6119N1**N*
L	2.X	XC6119N2**N*
M	3.X	XC6119N3**N*
N	4.X	XC6119N4**N*
P	5.X	XC6119N5**N*

② represents decimal number of detect voltage

MARK	VOLTAGE (V)	PRODUCT SERIES
N	X.0	XC6119**0*N*
P	X.1	XC6119**1*N*
R	X.2	XC6119**2*N*
S	X.3	XC6119**3*N*
T	X.4	XC6119**4*N*
U	X.5	XC6119**5*N*
V	X.6	XC6119**6*N*
X	X.7	XC6119**7*N*
Y	X.8	XC6119**8*N*
Z	X.9	XC6119**9*N*

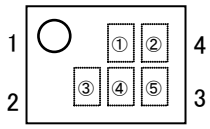
③④ represents production lot number
01 to 09, 0A to 0Z,11 to 9Z, A1 to A9,AA to Z9,ZA to ZZ repeated (G, I, J, O, Q, W excluded).
Note: No character inversion used.

■ MARKING RULE (Continued)

●USPN-4

① represents product series.

MARK	PRODUCT SERIES
B	XC6119******-G



USPN-4
(TOP VIEW)

② represents output configuration and integer number of detect voltage

CMOS Output (XC6119C Series)

MARK	VOLTAGE (V)	PRODUCT SERIES
A	0.X	XC6119C0**7*-G
B	1.X	XC6119C1**7*-G
C	2.X	XC6119C2**7*-G
D	3.X	XC6119C3**7*-G
E	4.X	XC6119C4**7*-G
F	5.X	XC6119C5**7*-G

N-channel Open Drain Output (XC6119N Series)

MARK	VOLTAGE (V)	PRODUCT SERIES
H	0.X	XC6119N0**7*-G
K	1.X	XC6119N1**7*-G
L	2.X	XC6119N2**7*-G
M	3.X	XC6119N3**7*-G
N	4.X	XC6119N4**7*-G
P	5.X	XC6119N5**7*-G

③ represents decimal number of detect voltage

MARK	VOLTAGE (V)	PRODUCT SERIES
N	X.0	XC6119**0*7*-G
P	X.1	XC6119**1*7*-G
R	X.2	XC6119**2*7*-G
S	X.3	XC6119**3*7*-G
T	X.4	XC6119**4*7*-G
U	X.5	XC6119**5*7*-G
V	X.6	XC6119**6*7*-G
X	X.7	XC6119**7*7*-G
Y	X.8	XC6119**8*7*-G
Z	X.9	XC6119**9*7*-G

④⑤ represents production lot number
01 to 09, 0A to 0Z,11 to 9Z, A1 to A9,AA to Z9,ZA to ZZ repeated (G, I, J, O, Q, W excluded).
Note: No character inversion used.

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5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

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TOREX SEMICONDUCTOR LTD.

LifeElectronics
Живое партнерство

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ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

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