



16 Ω, Low Parasitic Capacitance and Leakage, +12 V / +5 V / +3 V / ± 5 V Quad SPST Switches

DESCRIPTION

The DG411LE, DG412LE, and DG413LE are monolithic quad single-pole-single-throw analog switches. The DG411LE and DG412LE differ only in that they respond to opposite logic levels. The DG413LE has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, and one DPDT.

The DG411LE, DG412LE, and DG413LE offer low on resistance of 16 Ω, low parasitic capacitance of 15 pF switch on capacitance, and low charge injection over the signal swing range.

The DG411LE, DG412LE, and DG413LE operate on single and dual supplies. Single supply voltage ranges from 3 V to 16 V while dual supply operation is recommended with ± 3 V to ± 8 V. Each switch conducts equally well in both direction when on, and blocks input voltages up to the supply levels when off.

The DG411LE, DG412LE, and DG413LE are available in 16 lead TSSOP, SOIC, and PDIP packages.

FEATURES

- 3 V to 16 V single supply or ± 3 V to ± 8 V dual supply
- On-resistance $R_{DS(on)}$: 16 Ω
- Low parasitic capacitance:
 - $C_{D(ON)}$: 15 pF
 - $C_{S(OFF)}$: 5 pF
- Less than 8 pC charge injection over the full signal swing range
- Fast switching t_{ON} : 16 ns
 t_{OFF} : 9 ns
- TTL, CMOS compatible
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

BENEFITS

- Wide operation voltage range
- Low signal errors and distortion
- Fast switching time
- Minimized switching glitch

APPLICATIONS

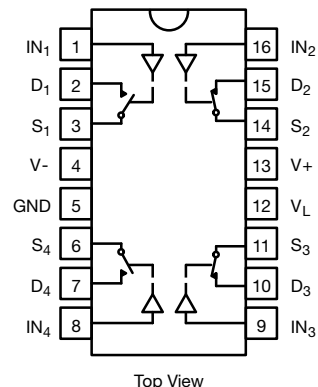
- Automatic test equipment
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Battery powered systems
- Computer peripherals
- Audio and video signal routing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG411LE, DG412LE
Dual-In-Line, TSSOP and SOIC



DG413LE
Dual-In-Line, TSSOP and SOIC





| TRUTH TABLE | | |
|-------------|---------|---------|
| LOGIC | DG411LE | DG412LE |
| 0 | ON | OFF |
| 1 | OFF | ON |

Logic "0" ≤ 0.8 VLogic "1" ≥ 2.4 V

| TRUTH TABLE | | |
|-------------|-----------------------------------|-----------------------------------|
| LOGIC | SW ₁ , SW ₄ | SW ₂ , SW ₃ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 0.8 VLogic "1" ≥ 2.4 V

| ORDERING INFORMATION | | | | |
|-------------------------------|------------------|------------------|------------------|-----------------------------|
| TEMP. RANGE | CONFIGURATION | PACKAGE | PART NUMBER | MIN. ORDER / PACK. QUANTITY |
| -40 °C to +85 °C Lead-free | DG411LE | 16-pin TSSOP | DG411LEDQ-GE3 | Tube 360 units |
| | | | DG411LEDQ-T1-GE3 | Tape and reel, 3000 units |
| | | 16-pin SOIC | DG411LEDY-GE3 | Tube 500 units |
| | | | DG411LEDY-T1-GE3 | Tape and reel, 2500 units |
| | | 16-pin PDIP | DG411LEDJ-GE3 | Tube 500 units |
| | | DG412LE | 16-pin TSSOP | DG412LEDQ-GE3 |
| | DG412LEDQ-T1-GE3 | | | Tape and reel, 3000 units |
| | 16-pin SOIC | | DG412LEDY-GE3 | Tube 500 units |
| | | | DG412LEDY-T1-GE3 | Tape and reel, 2500 units |
| | 16-pin PDIP | | DG412LEDJ-GE3 | Tube 500 units |
| | DG413LE | | 16-pin TSSOP | DG413LEDQ-GE3 |
| | | DG413LEDQ-T1-GE3 | | Tape and reel, 3000 units |
| | | 16-pin SOIC | DG413LEDY-GE3 | Tube 500 units |
| | | | DG413LEDY-T1-GE3 | Tape and reel, 2500 units |
| | | 16-pin PDIP | DG413LEDJ-GE3 | Tube 500 units |

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|--|-------------|----|
| PARAMETER | | UNIT | |
| V ₊ to V ₋ | -0.3 to +18 | V | |
| GND to V ₋ | 18 | | |
| V _L | (GND -0.3) to (V ₊) +0.3 | | |
| I _N ^a , V _S , V _D | -0.3 to (V ₊) +0.3 or 30 mA, whichever occurs first | | |
| Continuous Current (Any terminal) | 30 | mA | |
| Peak Current, S or D (Pulsed 1 ms, 10 % duty cycle) | 100 | | |
| Storage Temperature | (DQ, DY suffix) | -65 to +125 | °C |
| | (AK suffix) | -65 to +150 | |
| Power Dissipation (Packages) ^b | 16-pin TSSOP ^c | 450 | mW |
| | 16-pin SOIC ^d | 650 | |
| | 16-pin CerDIP ^e | 900 | |
| ESD Human Body Model (HBM); per ANSI / ESDA / JEDEC [®] JS-001 | 2500 | V | |
| Latch Up Current, per JESD78D | 400 | mA | |

Notes

- Signals on S_x, D_x, or I_{Nx} exceeding V₊ or V₋ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 7 mW/°C above 75 °C.
- Derate 7.6 mW/°C above 75 °C
- Derate 12 mW/°C above 75 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



| SPECIFICATIONS ^a (Single Supply 12 V) | | | | | | | | | |
|--|---------------------|--|--------------------|-------------------|---|-------------------|--|-------------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V ₊ = 12 V, V ₋ = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f | TEMP. ^b | TYP. ^c | A SUFFIX LIMITS -55 °C to +125 °C | | D SUFFIX LIMITS -40 °C to +85 °C | | UNIT |
| | | | | | MIN. ^d | MAX. ^d | MIN. ^d | MAX. ^d | |
| | | | | | Analog Switch | | | | |
| Analog Signal Range ^e | V _{ANALOG} | | Full | - | 0 | 12 | 0 | 12 | V |
| Drain-Source On-Resistance | R _{DS(on)} | V ₊ = 10.8 V, V ₋ = 0 V I _S = 10 mA, V _D = 2/9 V | Room | 16 | - | 26 | - | 26 | Ω |
| | | | Full | - | - | 40 | - | 35 | |
| Switch Off Leakage Current | I _{S(off)} | V _D = 1/11 V, V _S = 11/1 V | Room | - | -1 | 1 | -1 | 1 | nA |
| | | | Full | - | -15 | 15 | -10 | 10 | |
| | I _{D(off)} | | Room | - | -1 | 1 | -1 | 1 | |
| | | | Full | - | -15 | 15 | -10 | 10 | |
| Channel On Leakage Current | I _{D(on)} | V _S = V _D = 11/1 V | Room | - | -1 | 1 | -1 | 1 | |
| | | | Full | - | -15 | 15 | -10 | 10 | |
| Digital Control | | | | | | | | | |
| Input Current, VIN Low | I _{IL} | V _{IN} under test = 0.8 V | Full | 0.01 | -1.5 | 1.5 | -1 | 1 | μA |
| Input Current, VIN High | I _{IH} | V _{IN} under test = 2.4 V | Full | | -1.5 | 1.5 | -1 | 1 | |
| Dynamic Characteristics | | | | | | | | | |
| Turn-On Time | t _{ON} | R _L = 300 Ω, C _L = 35 pF, V _S = 5 V, see figure 2 | Room | 16 | - | 50 | - | 50 | ns |
| | | | Full | - | - | 70 | - | 60 | |
| Turn-Off Time | t _{OFF} | | Room | 9 | - | 30 | - | 30 | |
| | | | Full | - | - | 48 | - | 40 | |
| Break-Before-Make Time Delay | t _D | DG413L only, V _S = 5 V, R _L = 300 Ω, C _L = 35 pF | Room | 5 | - | - | - | - | |
| Charge Injection ^e | Q | V _g = 0 V, R _g = 0 Ω, C _L = 10 nF | Room | 6.6 | - | - | - | - | pC |
| Off-Isolation ^e | OIRR | R _L = 50 Ω, C _L = 5 pF, f = 1 MHz | Room | 68.4 | - | - | - | - | dB |
| Channel-to-Channel Crosstalk ^e | X _{TALK} | | Room | 114 | - | - | - | - | |
| Source Off Capacitance ^e | C _{S(off)} | | f = 1 MHz | Room | 5 | - | - | - | - |
| Drain Off Capacitance ^e | C _{D(off)} | Room | | 6 | - | - | - | - | |
| Channel-On Capacitance ^e | C _{D(on)} | Room | | 15 | - | - | - | - | |
| Power Supplies | | | | | | | | | |
| Positive Supply Current | I ₊ | V _{IN} = 0 V or 5 V | Room | 0.02 | - | 1 | - | 1 | μA |
| | | | Full | - | - | 7.5 | - | 5 | |
| Negative Supply Current | I ₋ | | Room | -0.002 | -1 | - | -1 | - | |
| | | | Full | - | -7.5 | - | -5 | - | |
| Logic Supply Current | I _L | | Room | 0.002 | - | 1 | - | 1 | |
| | | | Full | - | - | 7.5 | - | 5 | |
| Ground Current | I _{GND} | | Room | -0.002 | -1 | - | -1 | - | |
| | | | Full | - | -7.5 | - | -5 | - | |

Notes

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.
- g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.



| SPECIFICATIONS ^a (Dual Supply ± 5 V) | | | | | | | | | | |
|---|--------------|--|---|-------------------|---|-------------------|--|-------------------|----------|----|
| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 5$ V, $V_- = -5$ V $V_L = 5$ V, $V_{IN} = 2.4$ V, 0.8 V ^f | TEMP. ^b | TYP. ^c | A SUFFIX LIMITS -55 °C to +125 °C | | D SUFFIX LIMITS -40 °C to +85 °C | | UNIT | |
| | | | | | MIN. ^d | MAX. ^d | MIN. ^d | MAX. ^d | | |
| Analog Switch | | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | - | -5 | 5 | -5 | 5 | V | |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_+ = 5$ V, $V_- = -5$ V, $I_S = 10$ mA, $V_D = \pm 3.5$ V | Room | 18 | - | 30 | - | 30 | Ω | |
| | | | Full | - | - | 42 | - | 37 | | |
| Switch Off Leakage Current ^g | $I_{S(off)}$ | $V_+ = 5.5$, $V_- = -5.5$ V, $V_D = \pm 4.5$ V, $V_S = \pm 4.5$ V | Room | - | -1 | 1 | -1 | 1 | nA | |
| | | | Full | - | -15 | 15 | -10 | 10 | | |
| | Room | | - | -1 | 1 | -1 | 1 | | | |
| | Full | | - | -15 | 15 | -10 | 10 | | | |
| Channel On Leakage Current ^g | $I_{D(on)}$ | $V_+ = 5.5$ V, $V_- = -5.5$ V, $V_S = V_D = \pm 4.5$ V | Room | - | -1 | 1 | -1 | 1 | | |
| | | | Full | - | -15 | 15 | -10 | 10 | | |
| Digital Control | | | | | | | | | | |
| Input Current, V_{IN} Low ^e | I_{IL} | V_{IN} under test = 0.8 V | Full | 0.05 | -1.5 | 1.5 | -1 | 1 | μ A | |
| Input Current, V_{IN} High ^e | I_{IH} | V_{IN} under test = 2.4 V | Full | 0.05 | -1.5 | 1.5 | -1 | 1 | | |
| Dynamic Characteristics | | | | | | | | | | |
| Turn-On Time ^e | t_{ON} | $R_L = 300 \Omega$, $C_L = 35$ pF, $V_S = \pm 3.5$ V, see figure 2 | Room | 17 | - | 50 | - | 50 | ns | |
| | | | Full | - | - | 70 | - | 60 | | |
| Turn-Off Time ^e | t_{OFF} | | Room | 12 | - | 35 | - | 35 | | |
| | | | Full | - | - | 50 | - | 40 | | |
| Break-Before-Make Time Delay ^e | t_D | | DG413L only, $V_S = 3.5$ V, $R_L = 300 \Omega$, $C_L = 35$ pF | Room | 5 | - | - | - | | - |
| Charge Injection ^e | Q | | $V_g = 0$ V, $R_g = 0 \Omega$, $C_L = 10$ nF | Room | 5.8 | - | - | - | | - |
| Off Isolation ^e | OIRR | $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz | Room | 68 | - | - | - | - | dB | |
| Channel-to-Channel Crosstalk ^e | X_{TALK} | | Room | 113 | - | - | - | - | | |
| Source Off Capacitance ^e | $C_{S(off)}$ | | $f = 1$ MHz | Room | 5 | - | - | - | - | pF |
| Drain Off Capacitance ^e | $C_{D(off)}$ | Room | | 6 | - | - | - | - | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | Room | | 14 | - | - | - | - | | |
| Power Supplies | | | | | | | | | | |
| Positive Supply Current ^e | I_+ | $V_{IN} = 0$ V or 5 V | Room | 0.03 | - | 1 | - | 1 | μ A | |
| | | | Full | - | - | 7.5 | - | 5 | | |
| Negative Supply Current ^e | I_- | | Room | -0.002 | -1 | - | -1 | - | | |
| | | | Full | - | -7.5 | - | -5 | - | | |
| Logic Supply Current ^e | I_L | | Room | 0.002 | - | 1 | - | 1 | | |
| | | | Full | - | - | 7.5 | - | 5 | | |
| Ground Current ^e | I_{GND} | | Room | -0.002 | -1 | - | -1 | - | | |
| | | | Full | - | -7.5 | - | -5 | - | | |

Notes

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.
- g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.



| SPECIFICATIONS ^a (Single Supply 5 V) | | | | | | | | | |
|---|--------------|--|--------------------|-------------------|---|-------------------|--|-------------------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 5\text{ V}$, $V_- = 0\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^f | TEMP. ^b | TYP. ^c | A SUFFIX LIMITS -55 °C to +125 °C | | D SUFFIX LIMITS -40 °C to +85 °C | | UNIT |
| | | | | | MIN. ^d | MAX. ^d | MIN. ^d | MAX. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | - | - | 5 | - | 5 | V |
| Drain-Source On-Resistance ^e | $R_{DS(on)}$ | $V_+ = 4.5\text{ V}$, $I_S = 5\text{ mA}$, $V_D = 1\text{ V}$, 3.5 V | Room | 36 | - | 50 | - | 50 | Ω |
| | | | Full | - | - | 88 | - | 75 | |
| Dynamic Characteristics | | | | | | | | | |
| Turn-On Time ^e | t_{ON} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.5\text{ V}$, see figure 2 | Room | 27 | - | 50 | - | 50 | ns |
| | | | Hot | - | - | 90 | - | 60 | |
| Turn-Off Time ^e | t_{OFF} | | Room | 15 | - | 30 | - | 30 | |
| | | | Hot | - | - | 55 | - | 40 | |
| Break-Before-Make Time Delay ^e | t_D | DG413L only, $V_S = 3.5\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ | Room | 11 | - | - | - | - | |
| Charge Injection ^e | Q | $V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 10\text{ nF}$ | Room | 3.3 | - | - | - | - | pC |
| Power Supplies | | | | | | | | | |
| Positive Supply Current ^e | I+ | $V_{IN} = 0\text{ V or }5\text{ V}$ | Room | 0.02 | - | 1 | - | 1 | μA |
| | | | Hot | - | - | 7.5 | - | 5 | |
| Negative Supply Current ^e | I- | | Room | -0.002 | -1 | - | -1 | - | |
| | | | Hot | - | -7.5 | - | -5 | - | |
| Logic Supply Current ^e | I_L | | Room | 0.002 | - | 1 | - | 1 | |
| | | | Hot | - | - | 7.5 | - | 5 | |
| Ground Current ^e | I_{GND} | | Room | -0.002 | -1 | - | -1 | - | |
| | | | Hot | - | -7.5 | - | -5 | - | |

Notes

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.
- g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.



| SPECIFICATIONS ^a (Single Supply 3 V) | | | | | | | | | | |
|---|--------------|--|---|-------------------|--------------------------------------|-------------------|-------------------------------------|-------------------|---------------|----|
| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 3\text{ V}, V_- = 0\text{ V}$ $V_L = 3\text{ V}, V_{IN} = 0.4\text{ V}, 2.0\text{ V}$ ^f | TEMP. ^b | TYP. ^c | A SUFFIX LIMITS -55 °C to +125 °C | | D SUFFIX LIMITS -40 °C to +85 °C | | UNIT | |
| | | | | | MIN. ^d | MAX. ^d | MIN. ^d | MAX. ^d | | |
| Analog Switch | | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | - | 0 | 3 | 0 | 3 | V | |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_+ = 2.7\text{ V}, V_- = 0\text{ V},$ $I_S = 5\text{ mA}, V_D = 0.5, 2.2\text{ V}$ | Room | 106 | - | 130 | - | 130 | Ω | |
| | | | Full | - | - | 150 | - | 140 | | |
| Switch Off Leakage Current ^g | $I_{S(off)}$ | $V_+ = 3.3, V_- = 0\text{ V},$ $V_D = 1, 2\text{ V}, V_S = 2, 1\text{ V}$ | Room | - | -1 | 1 | -1 | 1 | nA | |
| | | | Full | - | -15 | 15 | -10 | 10 | | |
| | Room | | - | -1 | 1 | -1 | 1 | | | |
| | Full | | - | -15 | 15 | -10 | 10 | | | |
| Channel On Leakage Current ^g | $I_{D(on)}$ | $V_+ = 3.3\text{ V}, V_- = 0\text{ V},$ $V_S = V_D = 1, 2\text{ V}$ | Room | - | -1 | 1 | -1 | 1 | | |
| | | | Full | - | -15 | 15 | -10 | 10 | | |
| Digital Control | | | | | | | | | | |
| Input Current, V_{IN} Low | I_{IL} | V_{IN} under test = 0.4 V | Full | 0.005 | -1.5 | 1.5 | -1 | 1 | μA | |
| Input Current, V_{IN} High | I_{IH} | V_{IN} under test = 2.4 V | Full | 0.005 | -1.5 | 1.5 | -1 | 1 | | |
| Dynamic Characteristics | | | | | | | | | | |
| Turn-On Time | t_{ON} | $R_L = 300\ \Omega, C_L = 35\text{ pF},$ $V_S = 1.5\text{ V},$ see figure 2 | Room | 57 | - | 85 | - | 85 | ns | |
| | | | Full | - | - | 150 | - | 110 | | |
| Turn-Off Time | t_{OFF} | | Room | 25 | - | 60 | - | 60 | | |
| | | | Full | - | - | 100 | - | 85 | | |
| Break-Before-Make Time Delay | t_D | | DG413L only, $V_S = 1.5\text{ V},$ $R_L = 300\ \Omega, C_L = 35\text{ pF}$ | Room | 24 | - | - | - | | - |
| Charge Injection ^e | Q | | $V_g = 0\text{ V}, R_g = 0\ \Omega, C_L = 10\text{ nF}$ | Room | 2 | - | - | - | | - |
| Off Isolation ^e | OIRR | $R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$ | Room | 68 | - | - | - | - | dB | |
| Channel-to-Channel Crosstalk ^e | X_{TALK} | | Room | 107 | - | - | - | - | | |
| Source Off Capacitance ^e | $C_{S(off)}$ | | f = 1 MHz | Room | 6 | - | - | - | - | pF |
| Drain Off Capacitance ^e | $C_{D(off)}$ | Room | | 7 | - | - | - | - | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | Room | | 15 | - | - | - | - | | |

Notes

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- b. Room = 25 °C, full = as determined by the operating temperature suffix.
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- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.
- g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



$R_{DS(on)}$ vs. Drain Voltage (Single Supply)



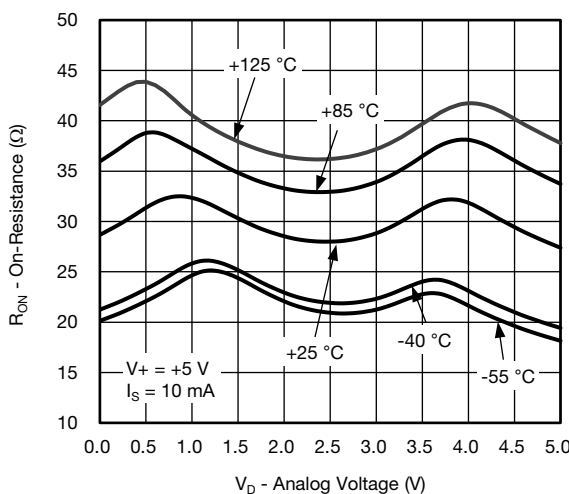
$R_{DS(on)}$ vs. Drain Voltage and Temperature (Single Supply)



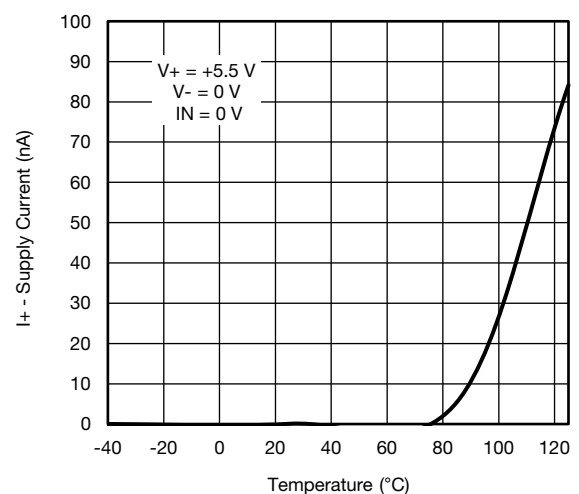
$R_{DS(on)}$ vs. Drain Voltage and Temperature



Supply Current vs. Temperature



$R_{DS(on)}$ vs. Drain Voltage and Temperature



Switching Time vs. Single Supply



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Leakage Current vs. Drain Voltage



Charge Injection vs. Drain Voltage



Switching Time vs. Single Supply Voltage



Threshold vs. Single Supply Current



Switching Time vs. Dual Supply Voltage

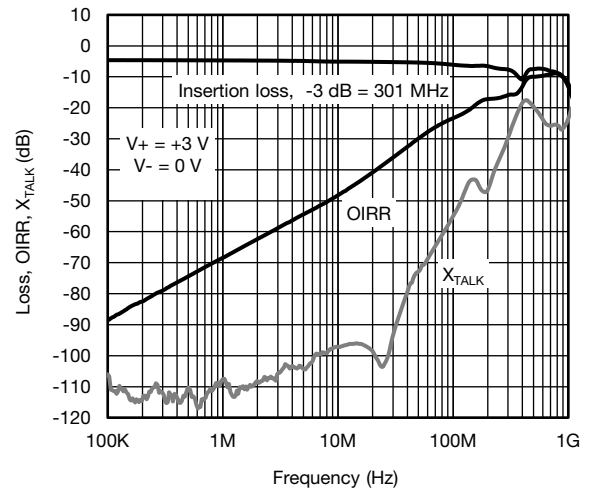


Drain Capacitance vs. Drain Voltage (Single Supply)

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Drain Capacitance vs. Drain Voltage (Dual Supply)



Insertion Loss, Off Isolation and Crosstalk vs. Frequency

SCHEMATIC DIAGRAM (Typical Channel)

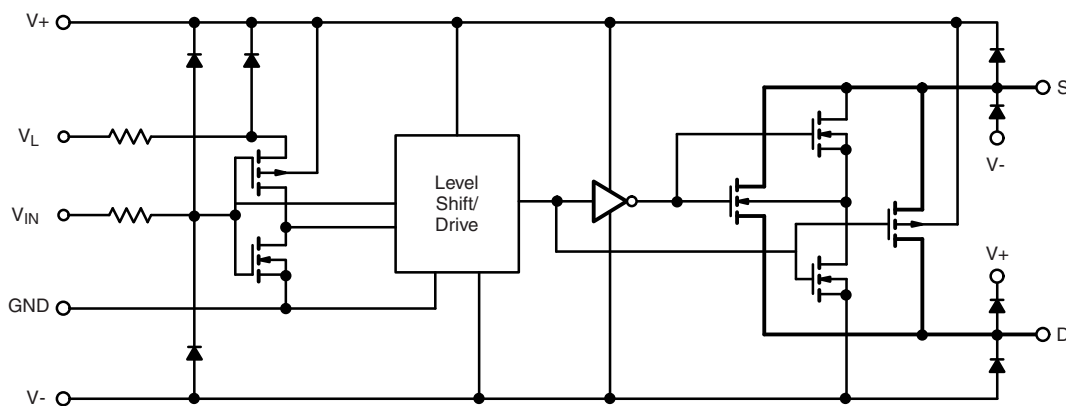


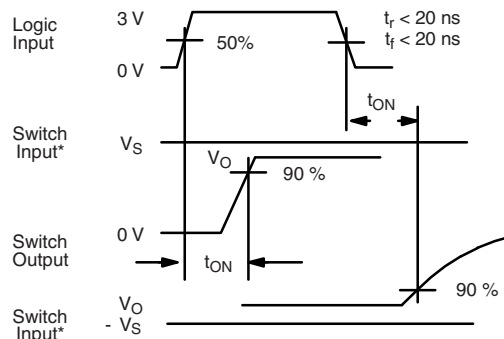
Fig. 1

TEST CIRCUITS



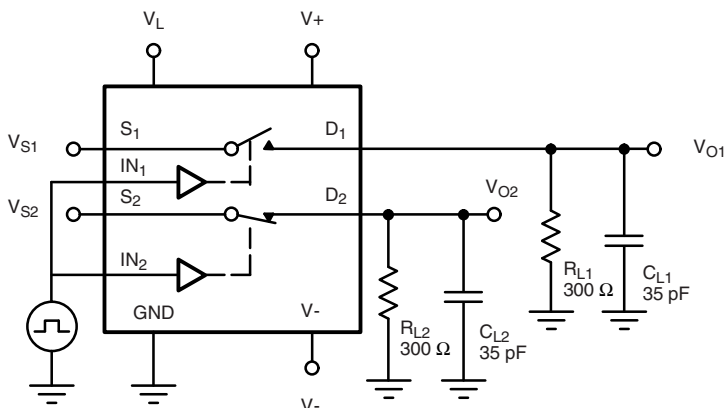
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 2 - Switching Time



C_L (includes fixture and stray capacitance)

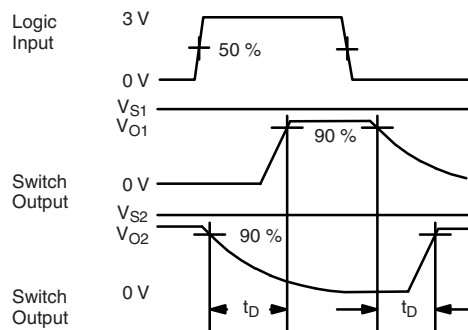
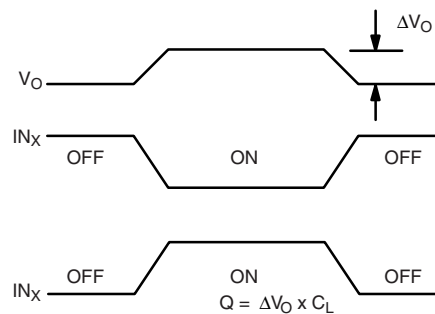
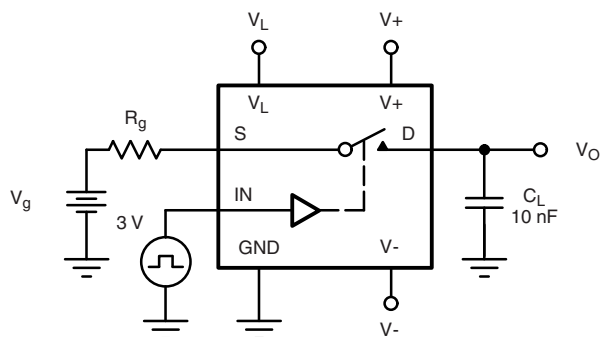


Fig. 3 - Break-Before-Make (DG413LE)



IN_x dependent on switch configuration Input polarity determined by sense of switch.

Fig. 4 - Charge Injection

TEST CIRCUITS

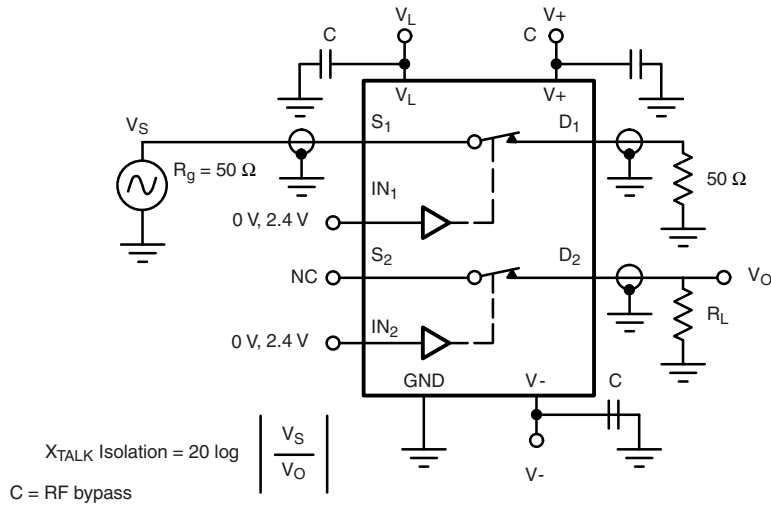


Fig. 5 - Crosstalk

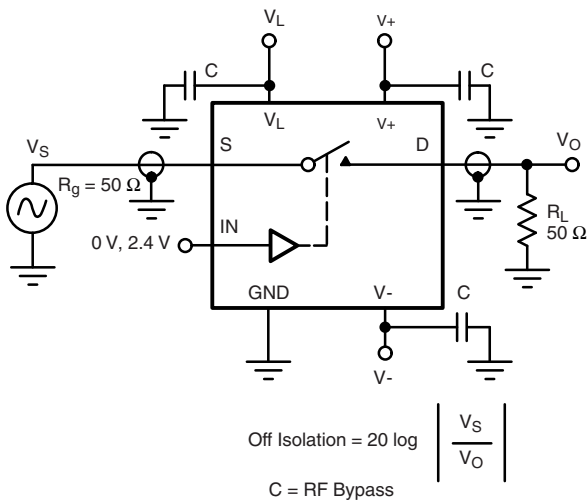


Fig. 6 - Off-Isolation

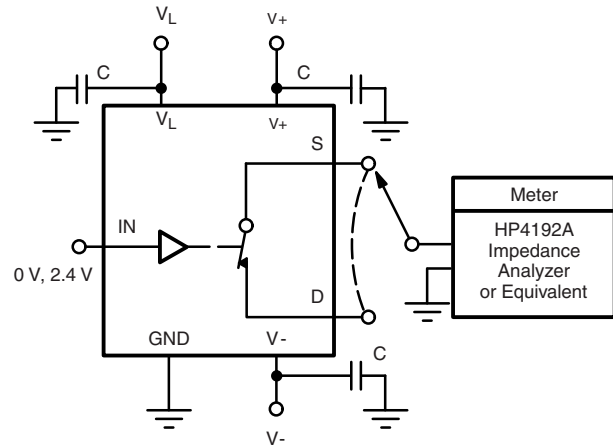


Fig. 7 - Source / Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?78091.



SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012



| Dim | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| C | 0.18 | 0.23 | 0.007 | 0.009 |
| D | 9.80 | 10.00 | 0.385 | 0.393 |
| E | 3.80 | 4.00 | 0.149 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| ∅ | 0° | 8° | 0° | 8° |

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



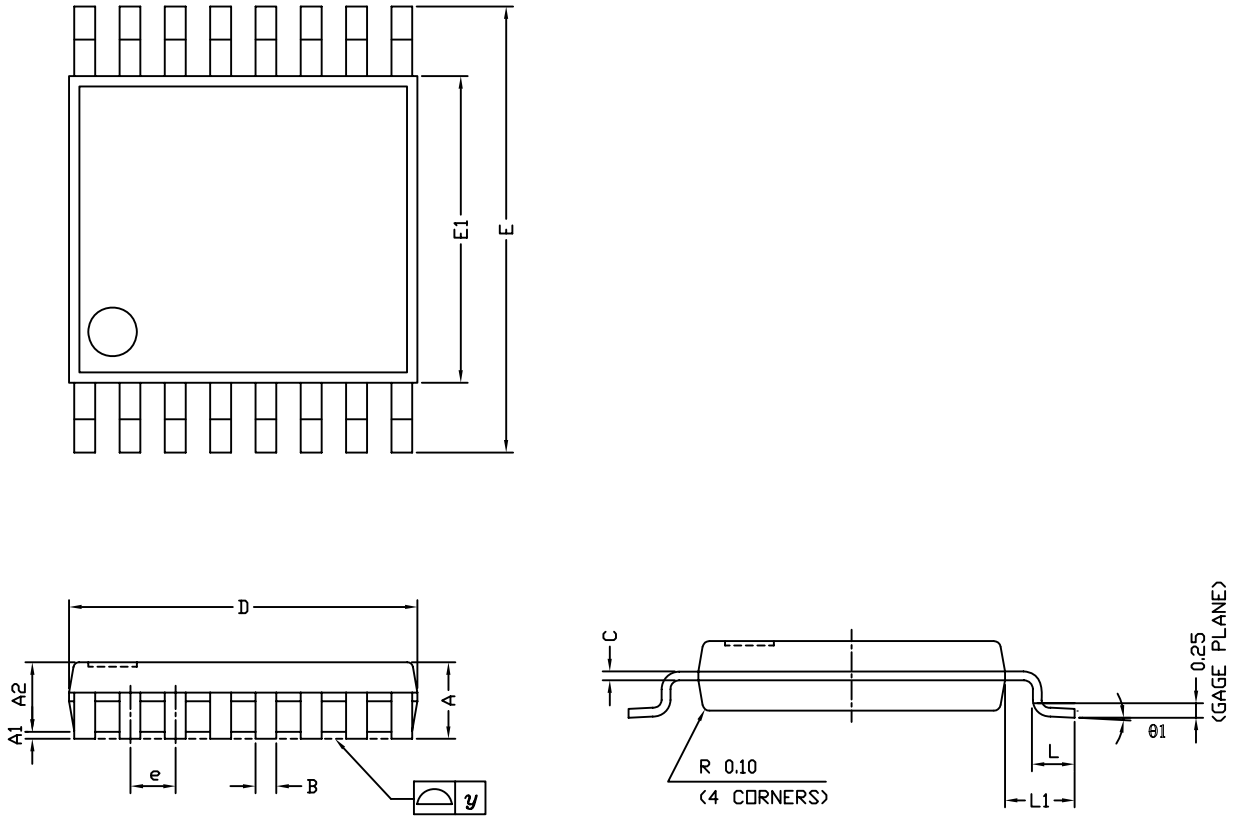
PDIP: 16-LEAD



| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|-------|--------|-------|
| | Min | Max | Min | Max |
| A | 3.81 | 5.08 | 0.150 | 0.200 |
| A₁ | 0.38 | 1.27 | 0.015 | 0.050 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| B₁ | 0.89 | 1.65 | 0.035 | 0.065 |
| C | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 18.93 | 21.33 | 0.745 | 0.840 |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E₁ | 5.59 | 7.11 | 0.220 | 0.280 |
| e₁ | 2.29 | 2.79 | 0.090 | 0.110 |
| e_A | 7.37 | 7.87 | 0.290 | 0.310 |
| L | 2.79 | 3.81 | 0.110 | 0.150 |
| Q₁ | 1.27 | 2.03 | 0.050 | 0.080 |
| S | 0.38 | 1.52 | .015 | 0.060 |

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

TSSOP: 16-LEAD



| Symbols | DIMENSIONS IN MILLIMETERS | | |
|---------|---------------------------|-------|------|
| | Min | Nom | Max |
| A | - | 1.10 | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | - | 1.00 | 1.05 |
| B | 0.22 | 0.28 | 0.38 |
| C | - | 0.127 | - |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.10 | 6.40 | 6.70 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | - | 0.65 | - |
| L | 0.50 | 0.60 | 0.70 |
| L1 | 0.90 | 1.00 | 1.10 |
| y | - | - | 0.10 |
| θ1 | 0° | 3° | 6° |

ECN: S-61920-Rev. D, 23-Oct-06
DWG: 5624



RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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