# 800 MHz, 4:1 Analog Multiplexer

# ADV3221/ADV3222

## FEATURES

- Excellent ac performance
  - −3 dB bandwidth
    - 800 MHz (200 mV p-p)
    - 750 MHz (2 V p-p)
  - Slew rate: 2400 V/µs
- Low power: 75 mW, $V_S$ = ±5 V
- Excellent video performance
  - 100 MHz, 0.1 dB gain flatness
  - 0.02% differential gain error/0.02° differential phase error ($R_L$ = 150 Ω)
- ADV3221 is a pin-for-pin upgrade to the HA4344
- Gain = +1 (ADV3221) or gain = +2 (ADV3222)
- Low all hostile crosstalk of −85 dB @ 5 MHz, and −58 dB @ 100 MHz
- Latched control lines for synchronous switching
- High impedance output disable allows connection of multiple devices without loading the output bus
- 16-lead SOIC

## APPLICATIONS

- Routing of high speed signals including
  - Video (NTSC, PAL, S, SECAM, YUV, RGB)
  - Compressed video (MPEG, wavelet)
  - 3-level digital video (HDB3)
- Data communications
- Telecommunications

## FUNCTIONAL BLOCK DIAGRAM

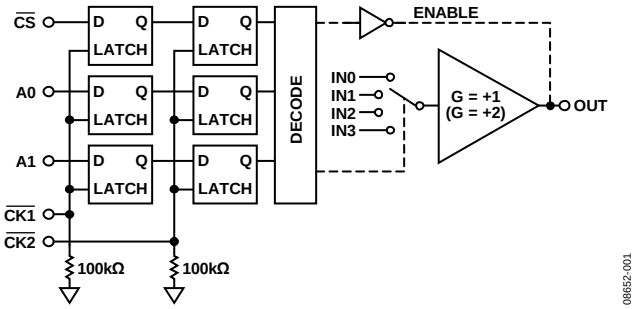


*Figure 1.*

## GENERAL DESCRIPTION

The ADV3221 and ADV3222 are high speed, high slew rate, buffered 4:1 analog multiplexers. They offer a −3 dB signal bandwidth greater than 800 MHz and channel switch times of less than 20 ns with 1% settling. With lower than −58 dB of crosstalk and −67 dB isolation (at 100 MHz), the ADV3221 and ADV3222 are useful in many high speed applications. The differential gain error of less than 0.02% and differential phase error of less than 0.02°, together with 0.1 dB gain flatness out to 100 MHz while driving a 75 Ω back terminated load, make the ADV3221 and ADV3222 ideal for all types of signal switching.

The ADV3221/ADV3222 include an output buffer that can be placed into a high impedance state. This allows multiple outputs to be connected together for cascading stages without the off channels loading the output bus. The ADV3221 has a gain of +1, and the ADV3222 has a gain of +2; they both operate on ±5 V supplies while consuming less than 7.5 mA of idle current. The channel switching is performed via latched control lines, allowing synchronous updating in a multiple ADV3221/ADV3222 environment.

The ADV3221/ADV3222 are offered in a 16-lead SOIC package and are available over the extended industrial temperature range of −40°C to +85°C.

**Rev. 0**

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
©2010 Analog Devices, Inc. All rights reserved.

# TABLE OF CONTENTS

Features ..... 1
Applications ..... 1
Functional Block Diagram ..... 1
General Description ..... 1
Revision History ..... 2
Specifications ..... 3
Timing and Logic Characteristics ..... 4
Absolute Maximum Ratings ..... 6
Thermal Resistance ..... 6
Power Dissipation ..... 6
ESD Caution ..... 6
Pin Configuration and Function Descriptions ..... 7
Typical Performance Characteristics ..... 8
Circuit Diagrams ..... 16
Theory of Operation ..... 17
Applications Information ..... 18
$\overline{CK1}$/$\overline{CK2}$ Operation ..... 18
Circuit Layout ..... 18
Termination ..... 18
Capacitive Load ..... 18
Outline Dimensions ..... 19
Ordering Guide ..... 19

## REVISION HISTORY

**3/10—Revision 0: Initial Version**

# SPECIFICATIONS

$V_S$ = ±5 V, $T_A$ = 25°C, $R_L$ = 150 Ω, $C_L$ = 2 pF, ADV3221 at G = +1, ADV3222 at G = +2, unless otherwise noted.

**Table 1.**

| | | ADV3221 | | | ADV3222 | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Test Conditions/Comments** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| DYNAMIC PERFORMANCE | | | | | | | | |
| −3 dB Bandwidth | 200 mV p-p | | 1000 | | | 800 | | MHz |
| | 2 V p-p | | 750 | | | 750 | | MHz |
| Gain Flatness | 0.1 dB, 200 mV p-p | | 100 | | | 100 | | MHz |
| | 0.1 dB, 2 V p-p | | 100 | | | 100 | | MHz |
| Propagation Delay | 2 V p-p | | 700 | | | 650 | | ps |
| Settling Time | 1%, 2 V step | | 5 | | | 5 | | ns |
| Slew Rate | 2 V step, peak | | 2400 | | | 2700 | | V/µs |
| NOISE/DISTORTION PERFORMANCE | | | | | | | | |
| Differential Gain Error | NTSC or PAL | | 0.01 | | | 0.02 | | % |
| Differential Phase Error | NTSC or PAL | | 0.01 | | | 0.02 | | Degrees |
| Crosstalk, All Hostile | f = 100 MHz | | −87 | | | −58 | | dB |
| | f = 5 MHz | | −100 | | | −85 | | dB |
| Off Isolation, Input to Output | f = 100 MHz, one channel | | −67 | | | −72 | | dB |
| Input Second-Order Intercept (ADV3222 Only) | f = 70 MHz, $R_L$ = 100 Ω | | | | | 54 | | dBm |
| Input Third-Order Intercept (ADV3222 Only) | f = 70 MHz, $R_L$ = 100 Ω | | | | | 17 | | dBm |
| Output 1 dB Compression Point (ADV3222 Only) | f = 70 MHz, $R_L$ = 100 Ω | | | | | 18.5 | | dBm |
| Input Voltage Noise | 10 MHz to 100 MHz | | 16 | | | 17 | | nV/√Hz |
| DC PERFORMANCE | | | | | | | | |
| Gain Error | No load | | | 1 | | | 1 | % |
| | $R_L$ = 150 Ω | | 0.75 | | | 0.75 | | % |
| Gain Matching | Channel-to-channel, no load | | 1 | | | 1 | | % |
| OUTPUT CHARACTERISTICS | | | | | | | | |
| Output Impedance | DC, enabled | | 0.02 | | | 0.04 | | Ω |
| | Disabled | 1 | | | 1 | | | MΩ |
| Output Disable Capacitance | Disabled | | 2.8 | | | 3 | | pF |
| Output Leakage Current | Disabled | | 2 | | | 2 | | µA |
| Output Voltage Range | No load | ±2.9 | ±3 | | ±2.9 | ±3 | | V |
| | $R_L$ = 150 Ω | ±2.8 | ±3 | | ±2.75 | ±3 | | V |
| Short-Circuit Current | | | 50 | | | 50 | | mA |
| INPUT CHARACTERISTICS | | | | | | | | |
| Input Offset Voltage | Worst case (all configurations) | | ±5 | ±21 | | ±5 | ±21 | mV |
| Input Offset Voltage Drift | | | ±10 | | | ±10 | | µV/°C |
| Input Voltage Range | | | ±3 | | | ±1.5 | | V |
| Input Capacitance | Any switch configuration | | 1.8 | | | 1.8 | | pF |
| Input Resistance | Output enabled | 1 | 10 | | 1 | 10 | | MΩ |
| Input Bias Current | Output enabled | | 5 | 12 | | 6 | 12 | µA |
| SWITCHING CHARACTERISTICS | | | | | | | | |
| Enable On Time | | | 15 | | | 15 | | ns |
| Switching Time, 2 V Step | 50% A0 to 1% settling | | 20 | | | 20 | | ns |
| Switching Transient (Glitch) | IN0 to IN1 switching | | 28 | | | 55 | | mV p-p |

| Parameter | Test Conditions/Comments | ADV3221 Min | ADV3221 Typ | ADV3221 Max | ADV3222 Min | ADV3222 Typ | ADV3222 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| POWER SUPPLIES | | | | | | | | |
| Supply Current | V+, output enabled, no load | | 7 | 8 | | 7.5 | 9 | mA |
| | V+, output disabled ($\overline{CS}$ high) | | 1.6 | 2.0 | | 1.8 | 2.2 | mA |
| | V−, output enabled, no load | | 7 | 8 | | 7.5 | 9 | mA |
| | V−, output disabled ($\overline{CS}$ high) | | 1.6 | 2.0 | | 1.8 | 2.2 | mA |
| Supply Voltage Range | | ±4.5 | | ±5.5 | ±4.5 | | ±5.5 | V |
| Power Supply Rejection (PSR) | f = 100 kHz | | −70 | | | −65 | | dB |
| | f = 1 MHz | | −60 | | | −55 | | dB |
| TEMPERATURE | | | | | | | | |
| Operating Temperature Range | Still air | −40 | | +85 | −40 | | +85 | °C |
| Junction-to-Ambient Thermal Impedance ($\theta_{JA}$) | Operating (still air) | | 81 | | | 81 | | °C/W |

## TIMING AND LOGIC CHARACTERISTICS

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| A0, A1, $\overline{CS}$ Setup Time | $t_1$ | 20 | | | ns |
| $\overline{CK1}$ Pulse Width | $t_2$ | 40 | | | ns |
| $\overline{CK1}$ to $\overline{CK2}$ Pulse Separation | $t_3$ | 40 | | | ns |
| $\overline{CK2}$ Pulse Width | $t_4$ | 40 | | | ns |
| A0, A1, $\overline{CS}$ Hold Time | $t_5$ | 20 | | | ns |

**Table 3. Logic Levels**

| $V_{IH}$ | $V_{IL}$ | $I_{IH}$ | $I_{IL}$ | $I_{IH}$ | $I_{IL}$ |
|---|---|---|---|---|---|
| A0, A1, $\overline{CK1}$, $\overline{CK2}$, $\overline{CS}$ | A0, A1, $\overline{CK1}$, $\overline{CK2}$, $\overline{CS}$ | A0, A1, $\overline{CS}$ | A0, A1, $\overline{CS}$ | $\overline{CK1}$, $\overline{CK2}$ | $\overline{CK1}$, $\overline{CK2}$ |
| +2.0 V min | +0.8 V max | ±2 µA max | ±2 µA max | +60 µA max | +10 µA max |

### *Timing and Programming Diagrams*

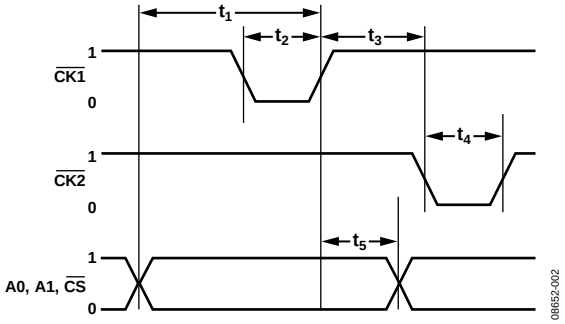


*Figure 2. Timing Diagram*

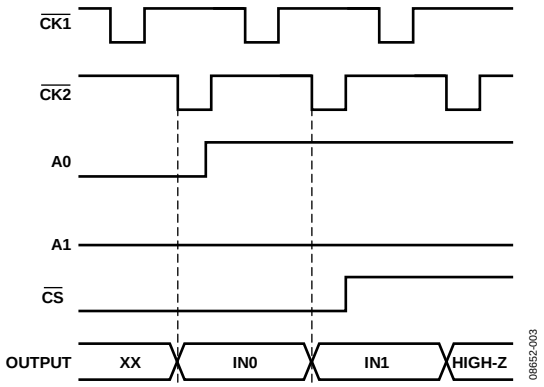


*Figure 3. Programming Example*

# ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | Rating |
|---|---|
| Supply Voltage (V+ – V–) | 12 V |
| Analog Input Voltage | V– to V+ |
| Digital Input Voltage | 0 V to V+ |
| Output Voltage (Disabled Output) | (V+ – 1 V) to (V– + 1 V) |
| Output Short-Circuit Duration | Momentary |
| Output Short-Circuit Current | 50 mA |
| Storage Temperature Range | –65°C to +150°C |
| Operating Temperature Range | –40°C to +85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 5. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 16-Lead Narrow-Body SOIC | 81 | 43 | °C/W |

## POWER DISSIPATION

The ADV3221/ADV3222 are operated with ±5 V supplies and can drive loads down to 150 Ω, resulting in a wide range of possible power dissipations. For this reason, extra care must be taken to adjust the operating conditions based on ambient temperature.

Packaged in a 16-lead narrow-body SOIC, the ADV3221 and ADV3222 junction-to-ambient thermal impedance ($\theta_{JA}$) is 81°C/W. For long-term reliability, the maximum allowed junction temperature of the die, $T_J$, should not exceed 125°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Figure 4 shows the range of the allowed internal die power dissipations that meet these conditions over the –40°C to +85°C ambient temperature range. When using Figure 4, do not include the external load power in the maximum power calculation, but do include the load current through the die output transistors.

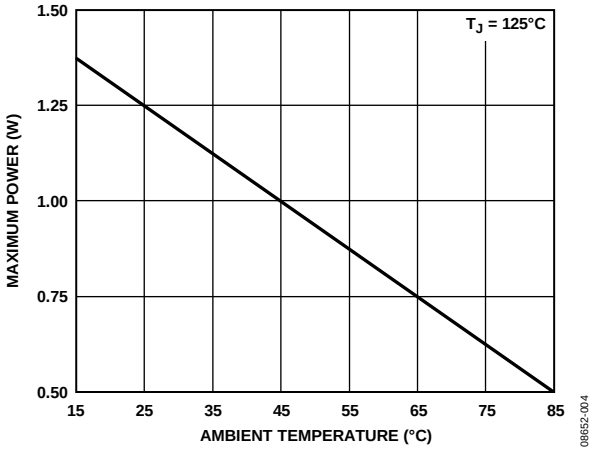


*Figure 4. Maximum Die Power Dissipation vs. Ambient Temperature*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

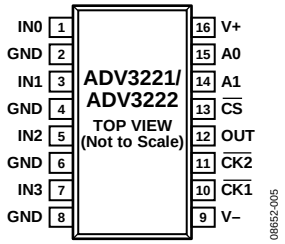


*Figure 5. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | IN0 | Analog Input |
| 2 | GND | Ground |
| 3 | IN1 | Analog Input |
| 4 | GND | Ground |
| 5 | IN2 | Analog Input |
| 6 | GND | Ground |
| 7 | IN3 | Analog Input |
| 8 | GND | Ground |
| 9 | V– | Negative Power Supply |
| 10 | $\overline{CK1}$ | First Rank Clock |
| 11 | $\overline{CK2}$ | Second Rank Clock |
| 12 | OUT | Analog Output |
| 13 | $\overline{CS}$ | Chip Select (Output Enable) |
| 14 | A1 | Select Address Most Significant Bit |
| 15 | A0 | Select Address Least Significant Bit |
| 16 | V+ | Positive Power Supply |

**Table 7. Truth Table**

| $\overline{CS}$ | A1 | A0 | $\overline{CK1}$ | $\overline{CK2}$ | Output |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | IN0 |
| 0 | 0 | 1 | 0 | 0 | IN1 |
| 0 | 1 | 0 | 0 | 0 | IN2 |
| 0 | 1 | 1 | 0 | 0 | IN3 |
| 1 | X[1] | X[1] | 0 | 0 | High-Z |

[1] X is don't care.

# TYPICAL PERFORMANCE CHARACTERISTICS

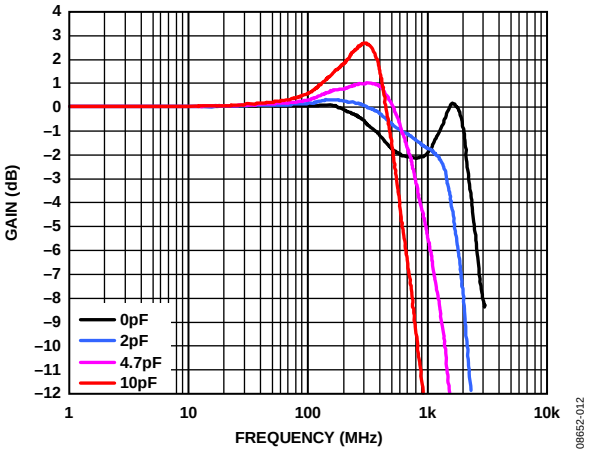


Figure 6. ADV3221 Small Signal Response vs. Capacitive Load, 200 mV p-p

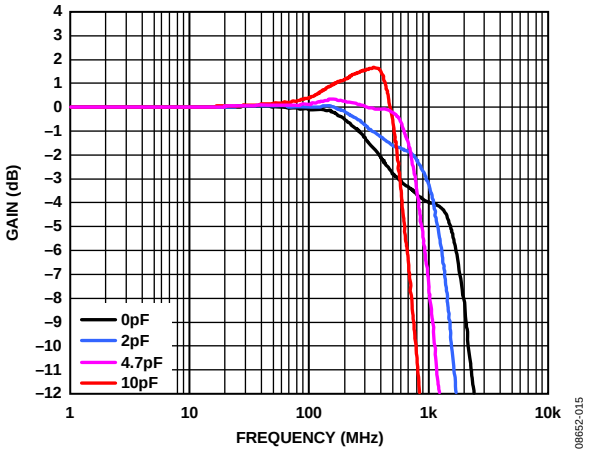


Figure 9. ADV3222 Small Signal Response vs. Capacitive Load, 200 mV p-p

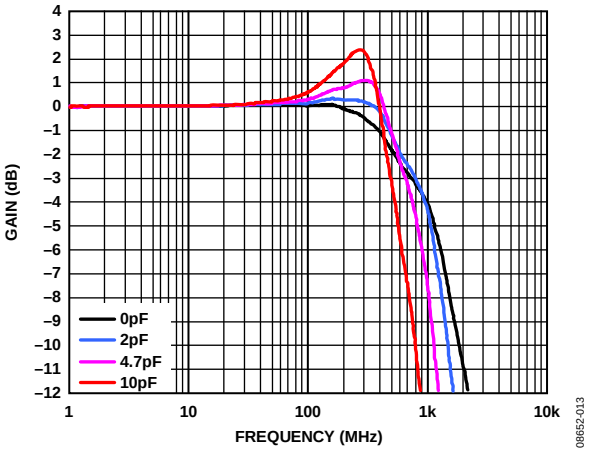


Figure 7. ADV3221 Large Signal Response vs. Capacitive Load, 2 V p-p

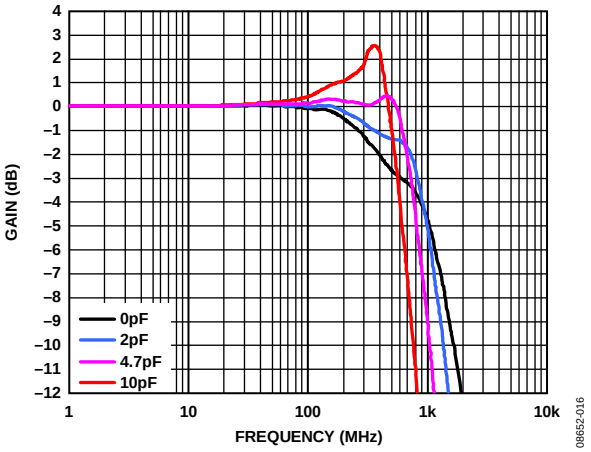


Figure 10. ADV3222 Large Signal Response vs. Capacitive Load, 2 V p-p

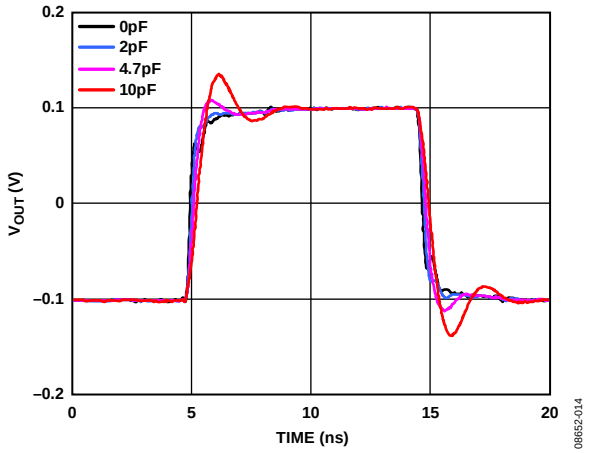


Figure 8. ADV3221 Small Signal Pulse Response vs. Capacitive Load, 200 mV p-p

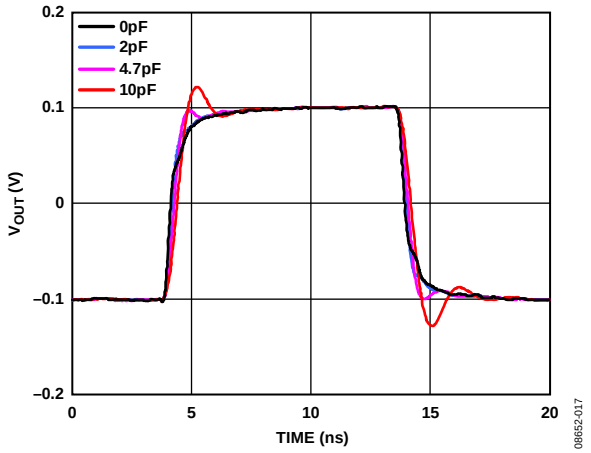


Figure 11. ADV3222 Small Signal Pulse Response vs. Capacitive Load, 200 mV p-p

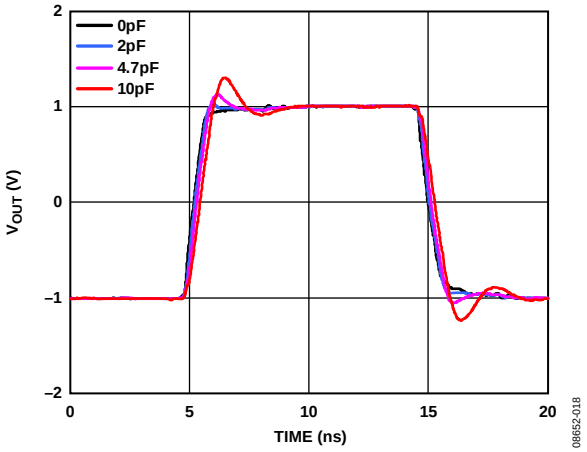


Figure 12. ADV3221 Large Signal Pulse Response vs. Capacitive Load, 2 V p-p

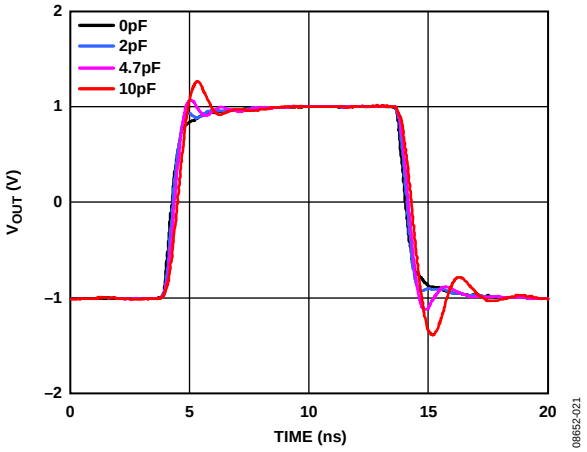


Figure 15. ADV3222 Large Signal Pulse Response vs. Capacitive Load, 2 V p-p

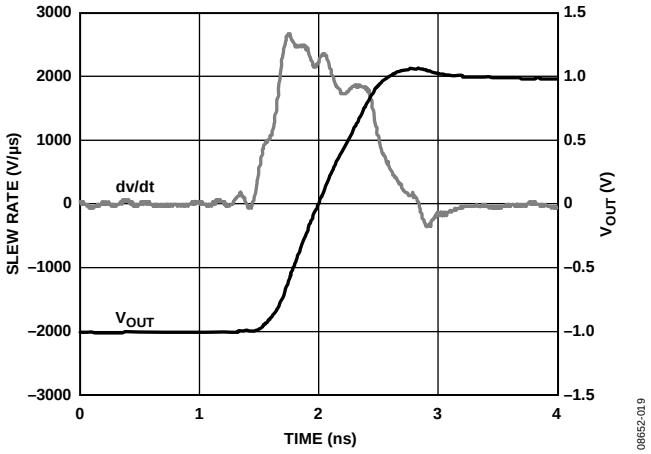


Figure 13. ADV3221 Large Signal Rising Slew Rate with 3 pF Load, 2 V p-p

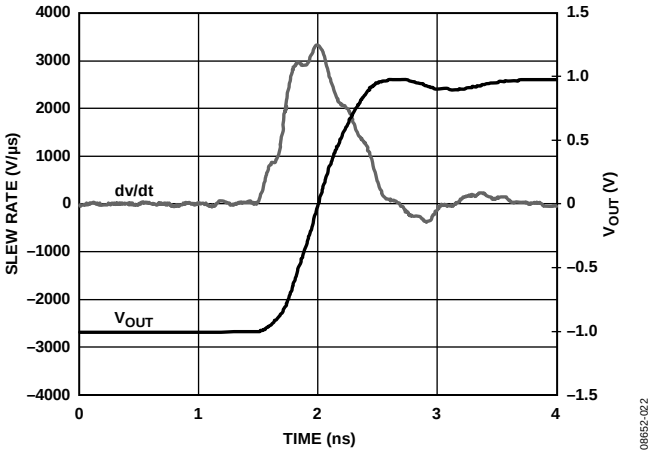


Figure 16. ADV3222 Large Signal Rising Slew Rate with 3 pF Load, 2 V p-p

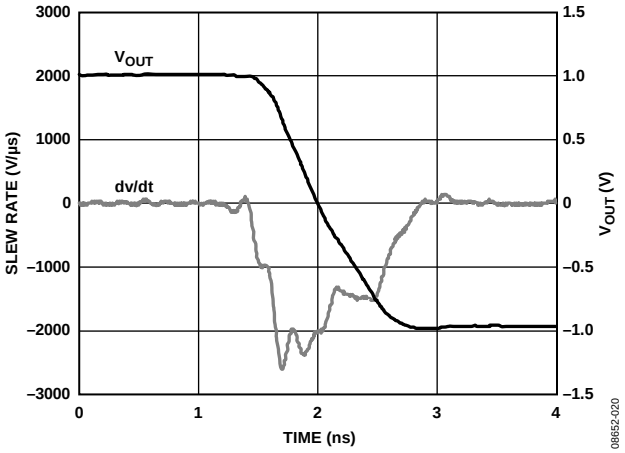


Figure 14. ADV3221 Large Signal Falling Slew Rate with 3 pF Load, 2 V p-p

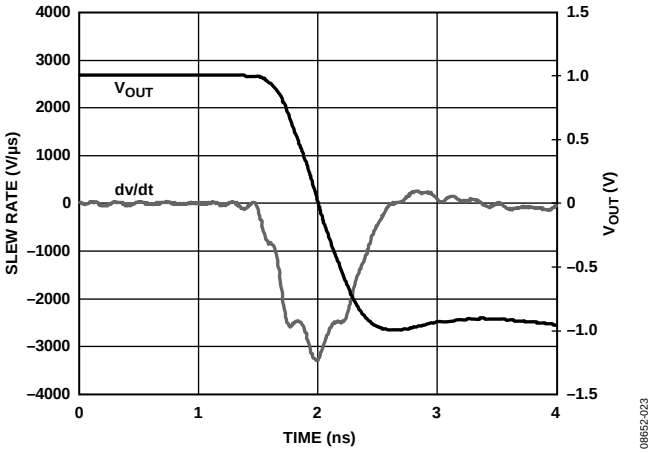


Figure 17. ADV3222 Large Signal Falling Slew Rate with 3 pF Load, 2 V p-p

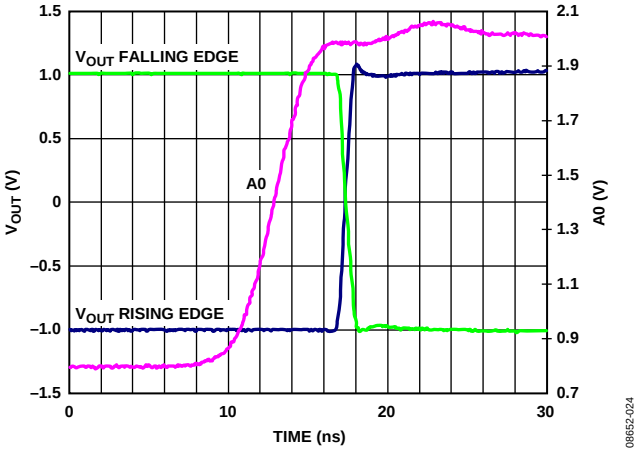


Figure 18. ADV3221 Switching Time

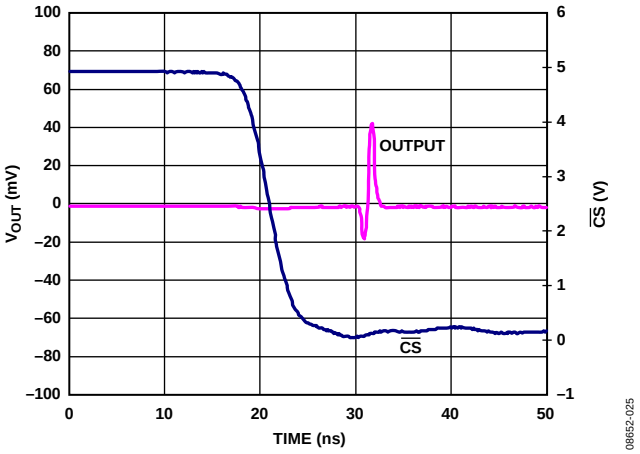


Figure 19. ADV3221 Enable Glitch

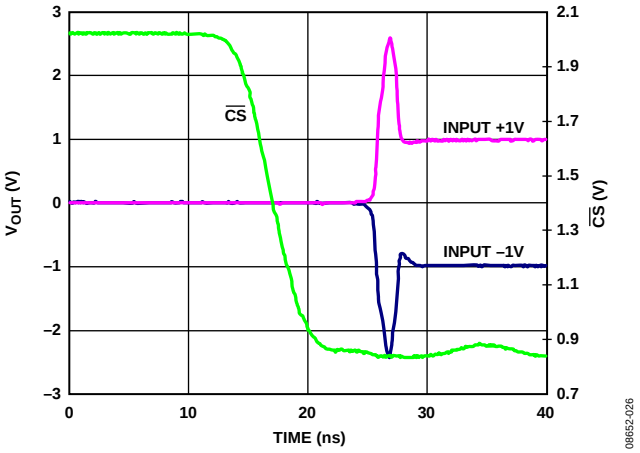


Figure 20. ADV3221 Enable On Timing

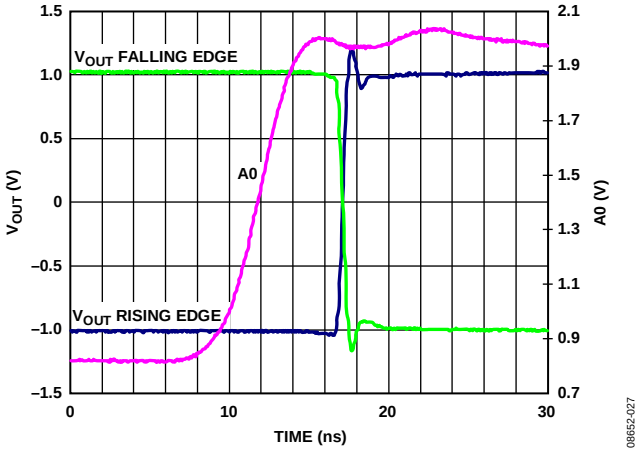


Figure 21. ADV3222 Switching Time

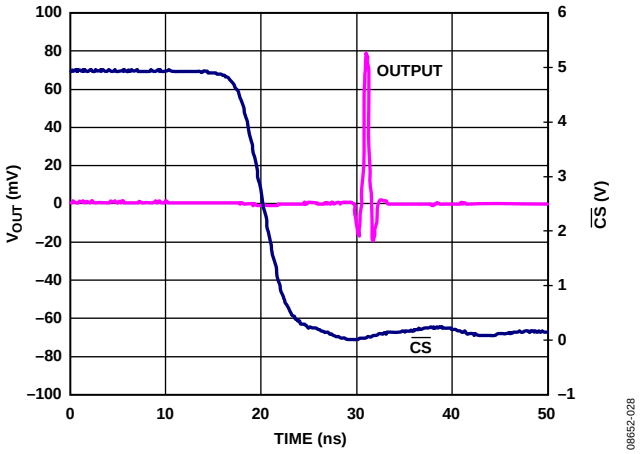


Figure 22. ADV3222 Enable Glitch

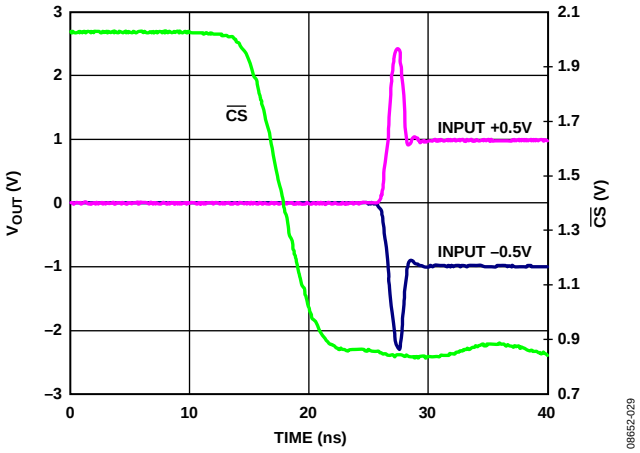


Figure 23. ADV3222 Enable On Timing

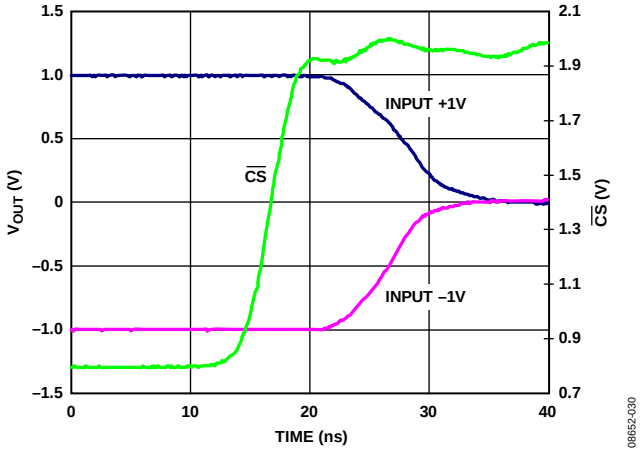


Figure 24. ADV3221 Disable Timing

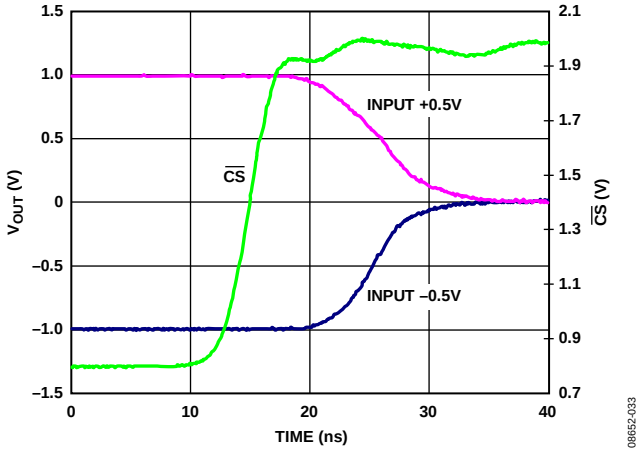


Figure 27. ADV3222 Disable Timing

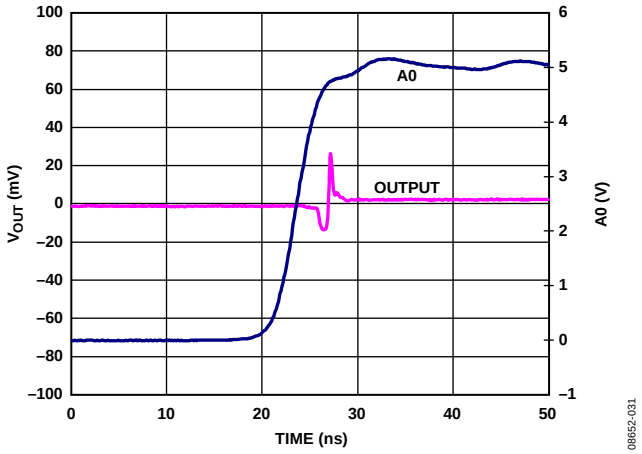


Figure 25. ADV3221 Switching Glitch Rising Edge

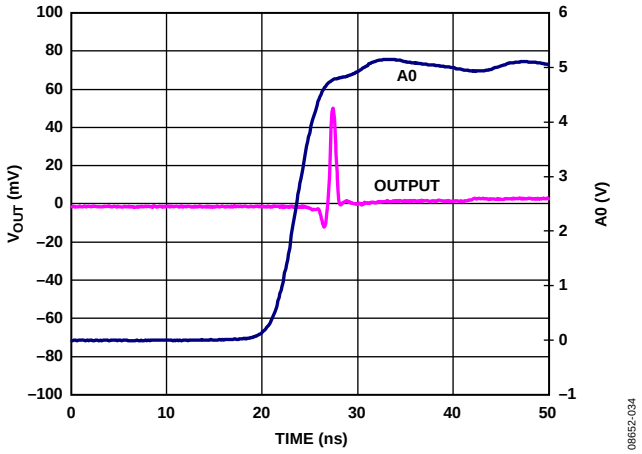


Figure 28. ADV3222 Switching Glitch Rising Edge

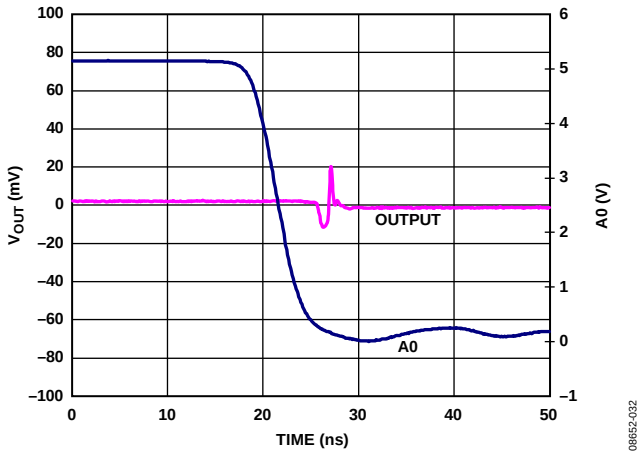


Figure 26. ADV3221 Switching Glitch Falling Edge

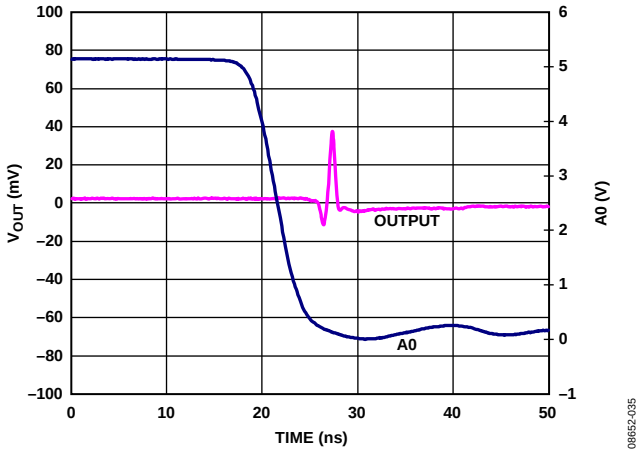


Figure 29. ADV3222 Switching Glitch Falling Edge

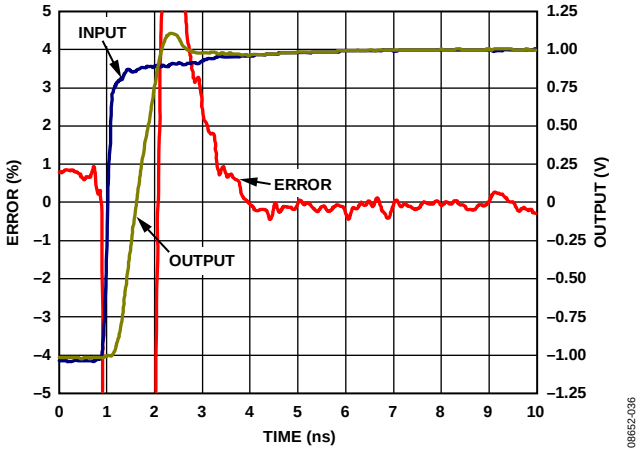


Figure 30. ADV3221 Settling Time, 2 V Step

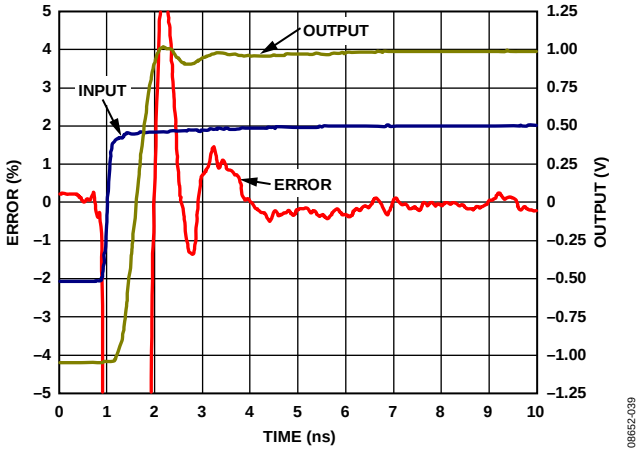


Figure 33. ADV3222 Settling Time, 2 V Step

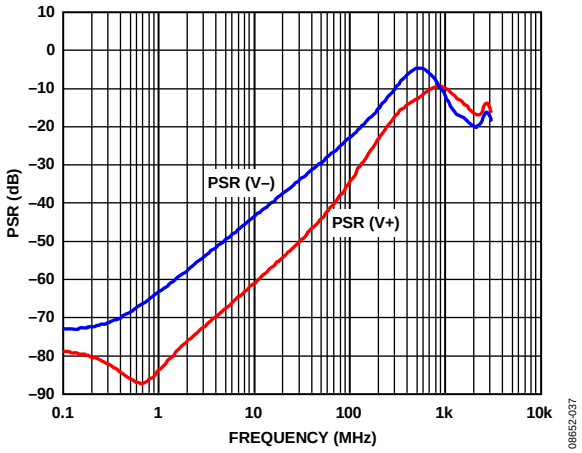


Figure 31. ADV3221 PSR

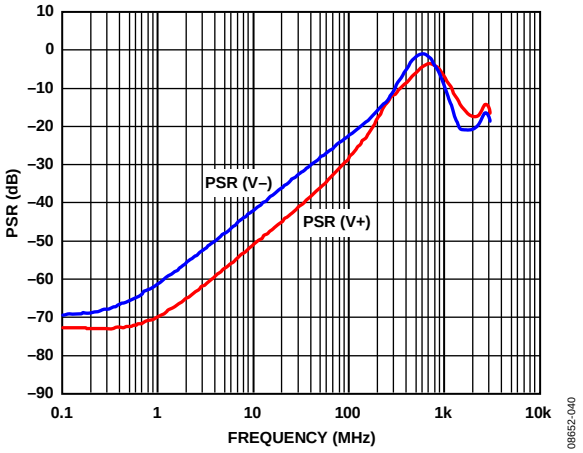


Figure 34. ADV3222 PSR

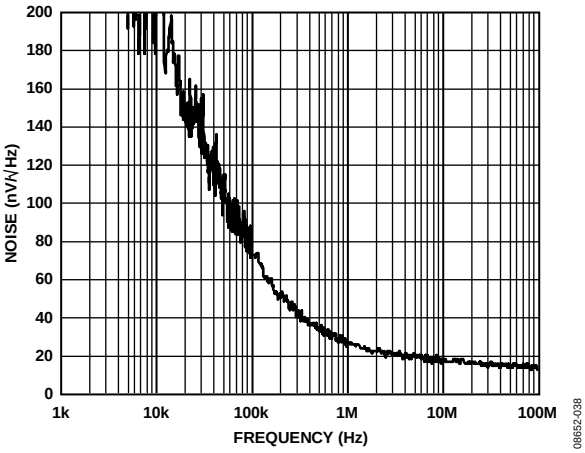


Figure 32. ADV3221 Output Noise vs. Frequency

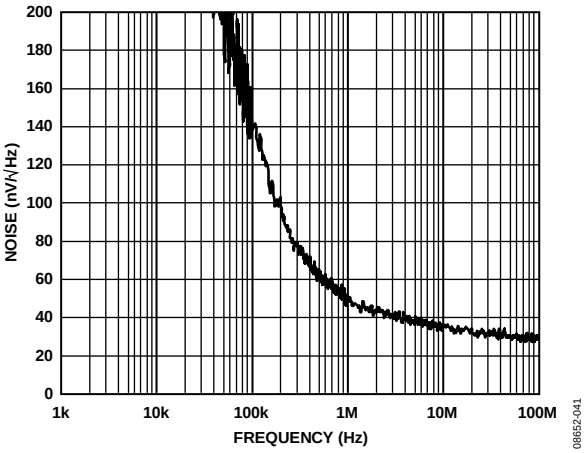


Figure 35. ADV3222 Output Noise vs. Frequency

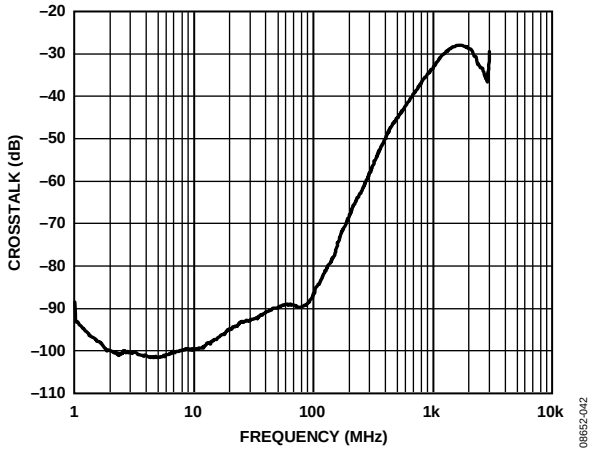


Figure 36. ADV3221 All Hostile Crosstalk

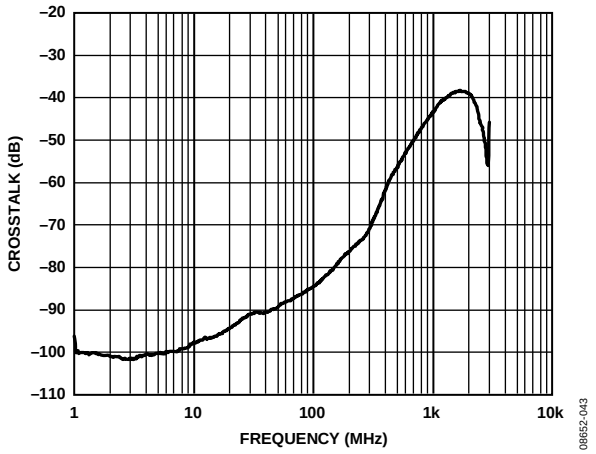


Figure 37. ADV3221 Crosstalk, Adjacent Channel

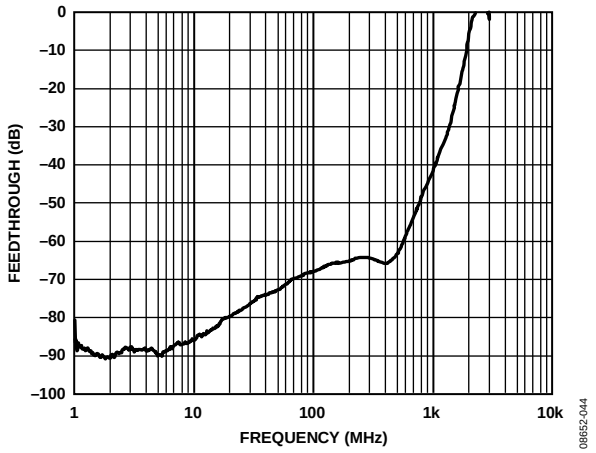


Figure 38. ADV3221 Off Isolation

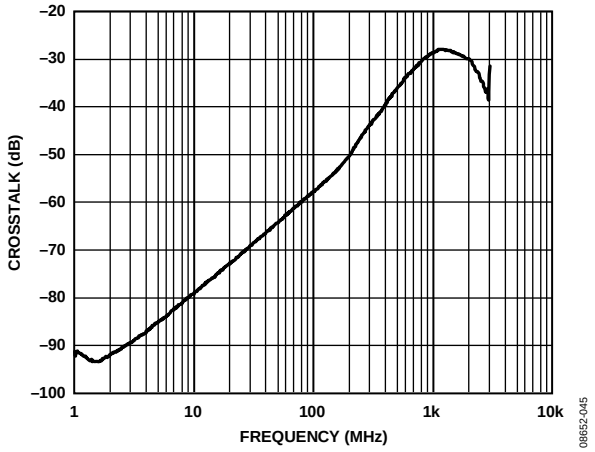


Figure 39. ADV3222 All Hostile Crosstalk

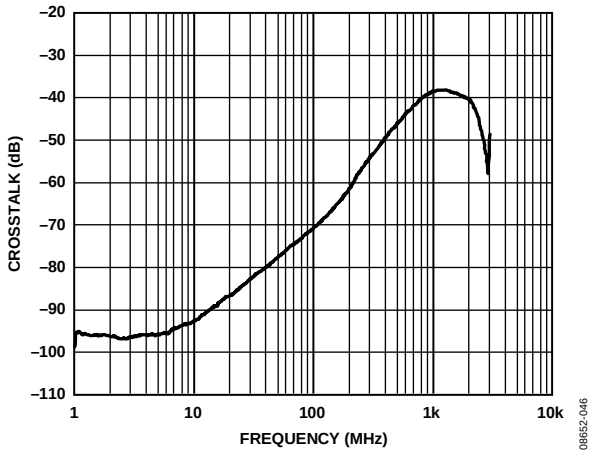


Figure 40. ADV3222 Crosstalk, Adjacent Channel

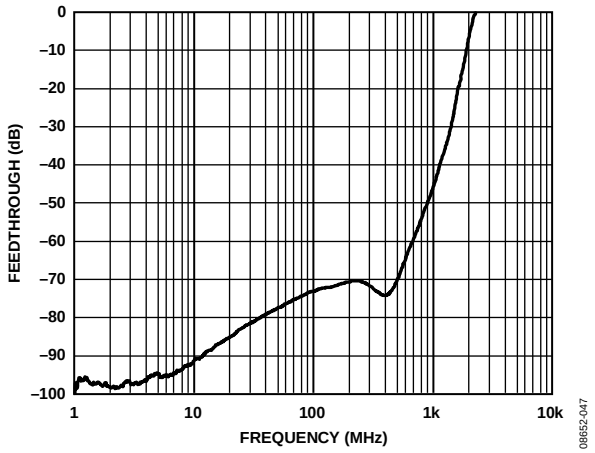


Figure 41. ADV3222 Off Isolation

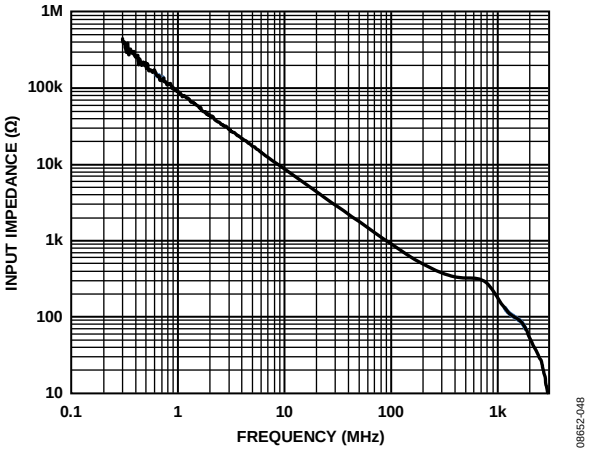


Figure 42. ADV3221/ADV3222 Input Impedance

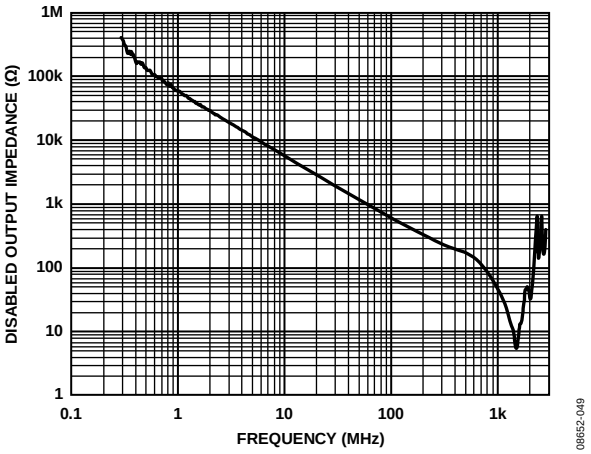


Figure 43. ADV3221 Disabled Output Impedance

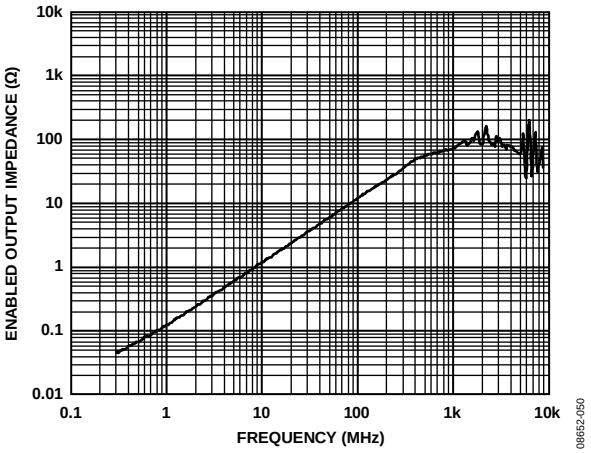


Figure 44. ADV3221 Enabled Output Impedance

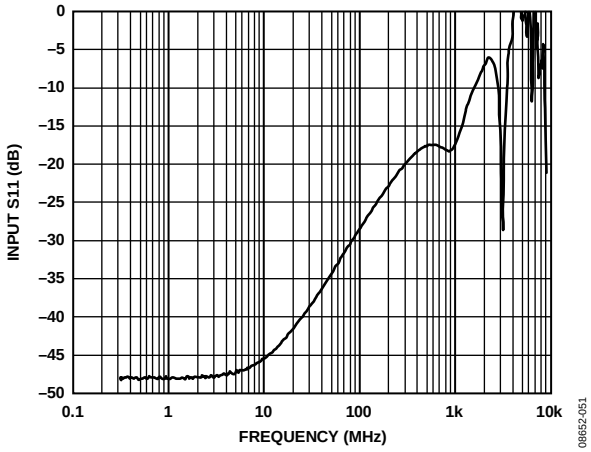


Figure 45. ADV3221/ADV3222 S11 (Including Evaluation Board)

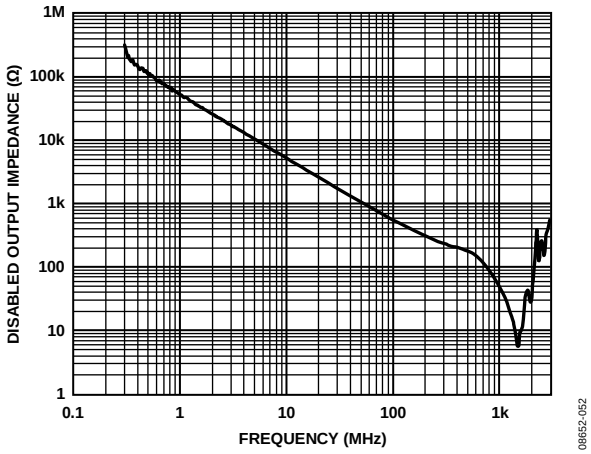


Figure 46. ADV3222 Disabled Output Impedance

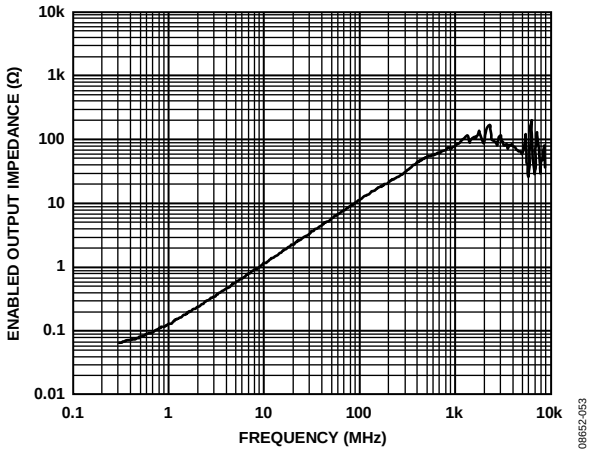


Figure 47. ADV3222 Enabled Output Impedance

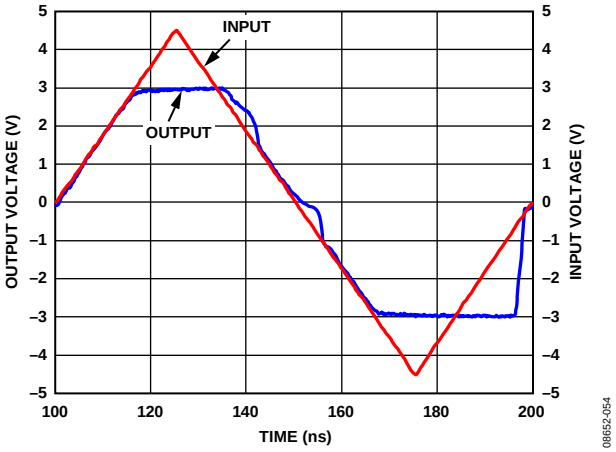


Figure 48. ADV3221 Overdrive Recovery

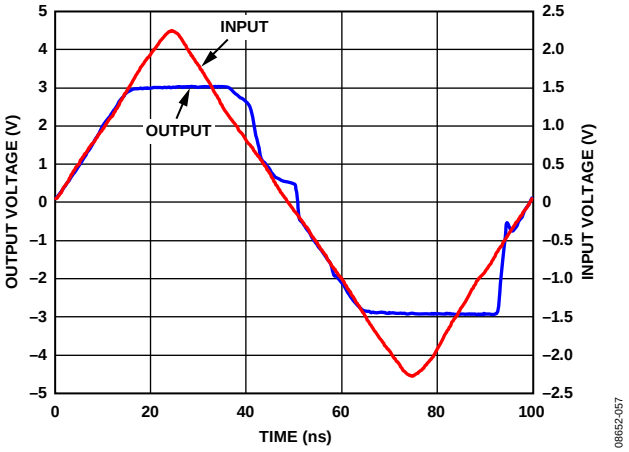


Figure 51. ADV3222 Overdrive Recovery

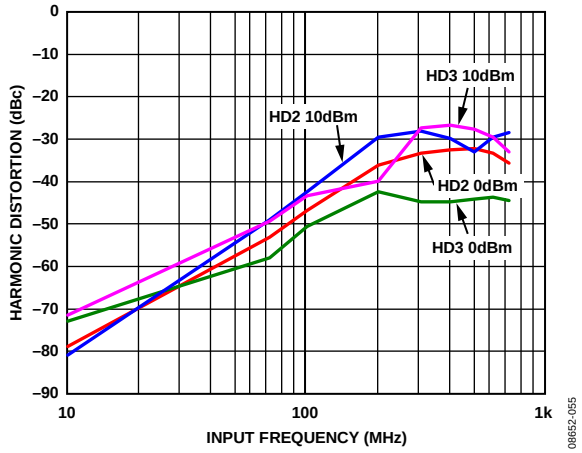


Figure 49. ADV3222 Harmonic Distortion, $R_L$ = 100 Ω, $C_L$ = 4 pF

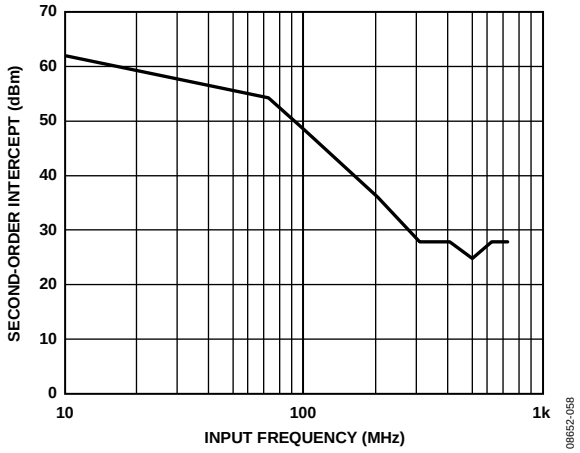


Figure 52. ADV3222 Input Second-Order Intercept, $R_L$ = 100 Ω, $C_L$ = 4 pF

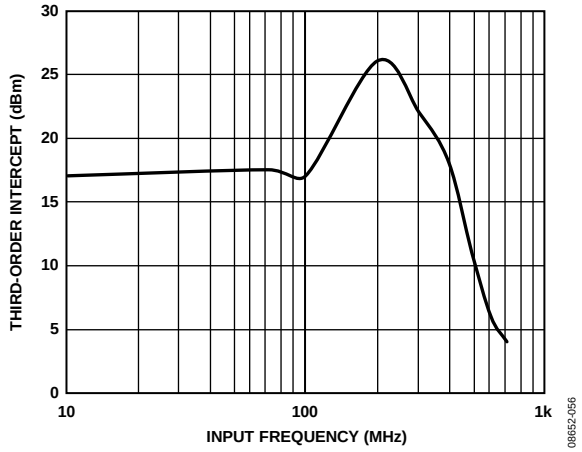


Figure 50. ADV3222 Input Third-Order Intercept, $R_L$ = 100 Ω, $C_L$ = 4 pF

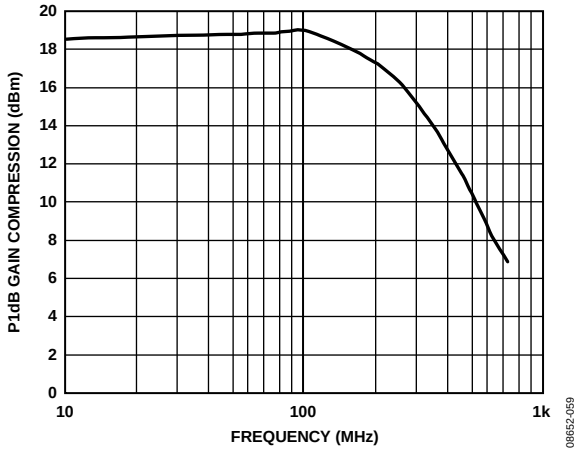


Figure 53. ADV3222 Output P1dB, $R_L$ = 100 Ω, $C_L$ = 4 pF

# CIRCUIT DIAGRAMS

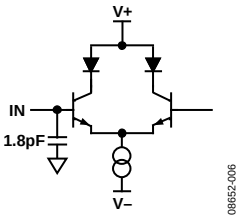


*Figure 54. ADV3221/ADV3222 Analog Input*

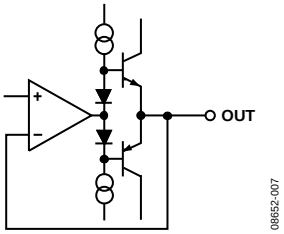


*Figure 55. ADV3221 Enabled Analog Output*

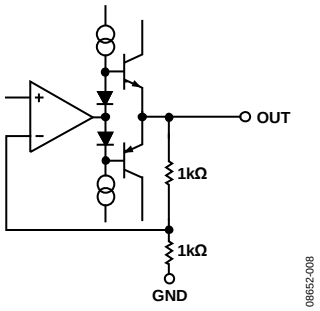


*Figure 56. ADV3222 Enabled Analog Output*

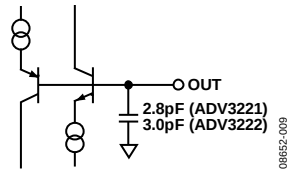


*Figure 57. ADV3221/ADV3222 Disabled Output*

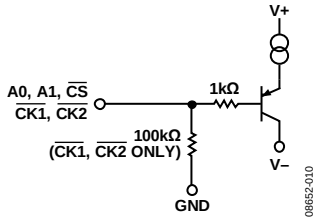


*Figure 58. ADV3221/ADV3222 Logic Input*

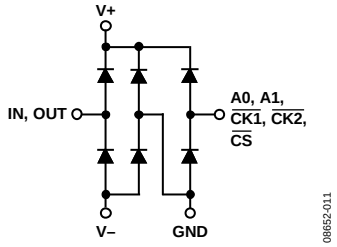


*Figure 59. ADV3221/ADV3222 ESD Schematic*

# THEORY OF OPERATION

The ADV3221/ADV3222 are dual-supply, high performance 4:1 analog multiplexers, optimized for switching between multiple video sources. High peak slew rates enable wide bandwidth operation for large input signals. Internal compensation provides for high phase margin, allowing low overshoot and fast settling for pulsed inputs. Low enabled and disabled power consumption make the ADV3221 and ADV3222 ideal for constructing larger arrays.

The ADV3221/ADV3222 are organized as four input transconductance stages tied in parallel with a single output transimpedance stage followed by a unity-gain buffer. Internal voltage feedback sets the gain. The ADV3221 is configured as a gain of 1, while the ADV3222 uses a resistive feedback network and ground buffer to realize gain-of-two operation (see Figure 60).

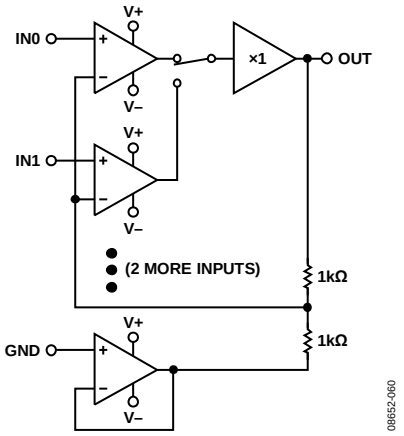


*Figure 60. Conceptual Diagram of ADV3222*

When not in use, the output can be placed in a low power, high impedance disabled mode via the $\overline{CS}$ logic input. This is useful when paralleling multiple ADV3221/ADV3222 devices in a system to create larger switching arrays.

Switching between the inputs is controlled with the A0, A1, and $\overline{CS}$ logic inputs, which are latched through two stages of asynchronous latches. $\overline{CK1}$ controls the first stage latch, and $\overline{CK2}$ controls the second stage latch. The latch state is dependent on the level of the $\overline{CK1}$ and $\overline{CK2}$ signals, and it is not edge triggered. When using multiple ADV3221/ADV3222 devices in a switch design, this double buffered logic allows the use of the $\overline{CK2}$ signal to simultaneously update all ADV3221/ADV3222 devices in a system. The A0 and A1 logic inputs select which input is connected to the output (A1 is the most significant bit, A0 is the least significant bit), and the $\overline{CS}$ logic input determines whether the output is enabled or disabled.

# APPLICATIONS INFORMATION

The ADV3221 and ADV3222 are high speed multiplexers used to switch video or RF signals. The low output impedance of the ADV3221/ADV3222 allows the output environment to be optimized for use in 75 Ω or 50 Ω systems by choosing the appropriate series termination resistor. For composite video applications, the ADV3222 (gain of +2) is typically used to provide compensation for the loss of the output termination.

## $\overline{CK1}$/$\overline{CK2}$ OPERATION

The ADV3221/ADV3222 provide a double latched architecture for the A0, A1 (channel selection) and $\overline{CS}$ (output enable) logic. This allows for simultaneous update of multiple devices in bank switching applications or large multiplexer systems consisting of multiple devices connected to common output busses.

Holding $\overline{CK1}$ and $\overline{CK2}$ low places the ADV3221/ADV3222 in a transparent mode. In transparent mode, all logic changes to A0, A1, and $\overline{CS}$ immediately affects the input selection and output enable/disable.

## CIRCUIT LAYOUT

Use of proper high speed design techniques is important to ensure optimum performance. Use a low inductance ground plane for power supply bypassing and to provide high quality return paths for the input and output signals. For best performance, it is recommended that power supplies be bypassed with 0.1 µF ceramic capacitors as close to the body of the device as possible. To provide stored energy for lower frequency, high current output driving, place 10 µF tantalum capacitors farther from the device.

The input and output signal paths should be stripline or microstrip controlled impedance. Video systems typically use 75 Ω characteristic impedance, whereas RF systems typically use 50 Ω. Various calculators are available to calculate the trace geometry required to produce the proper characteristic impedance.

## TERMINATION

For a controlled impedance situation, termination resistors are required at the inputs and output of the device. The input termination should be a shunt resistor to ground with a value matching the characteristic impedance of the input trace. To reduce reflections, place the input termination resistor as close to the device input pin as possible. To minimize the input-to-input crosstalk, it is important to utilize a low inductance shield between input traces to isolate each input. Consideration of ground current paths must be taken to minimize loop currents in the shields to prevent them from providing a coupling medium for crosstalk.

For proper matching, the output series termination resistor should be the same value as the characteristic impedance of the output trace and placed as close to the output of the device as possible. This placement reduces the high frequency effect of series parasitic inductance, which can affect gain flatness and −3 dB bandwidth.

## CAPACITIVE LOAD

A high frequency output can have difficulties when driving a large capacitive load, usually resulting in peaking in the frequency domain or overshoot in the time domain. If these effects become too large, oscillation can result.

The response of the device under various capacitive loads is shown in Figure 6 through Figure 12, and in Figure 15. If a condition arises where excessive load capacitance is encountered and the overshoot is too great or the device oscillates, a small series resistor of a few tens of ohms can be used to improve the performance.

# OUTLINE DIMENSIONS

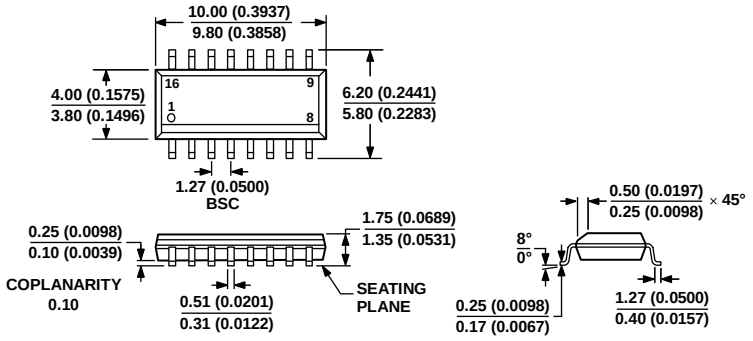


*Figure 61. 16-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*[R-16]*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADV3221ARZ | −40°C to +85°C | 16-Lead SOIC_N | R-16 |
| ADV3221ARZ-RL | −40°C to +85°C | 16-Lead SOIC_N, 13″ Reel | R-16 |
| ADV3221ARZ-R7 | −40°C to +85°C | 16-Lead SOIC_N, 7″ Reel | R-16 |
| ADV3222ARZ | −40°C to +85°C | 16-Lead SOIC_N | R-16 |
| ADV3222ARZ-RL | −40°C to +85°C | 16-Lead SOIC_N, 13″ Reel | R-16 |
| ADV3222ARZ-R7 | −40°C to +85°C | 16-Lead SOIC_N, 7″ Reel | R-16 |
| ADV3221-EVALZ | | Evaluation Board | |
| ADV3222-EVALZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

## NOTES

©2010 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D08652-0-3/10(0)

LifeElectronics
Живое партнерство

**ООО «ЛайфЭлектроникс»** **“LifeElectronics” LLC**

*ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703*

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

*Мы предлагаем:*

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

*В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.*

*Конструкторский отдел помогает осуществить:*

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

*Тел: +7 (812) 336 43 04 (многоканальный)*
*Email: org@lifeelectronics.ru*

***www.lifeelectronics.ru***