



# BUK6D81-80E

80 V, N-channel Trench MOSFET

4 April 2019

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Extended temperature range  $T_j = 175\text{ °C}$
- Side wettable flanks for optical solder inspection
- ElectroStatic Discharge (ESD) protection  $> 2\text{ kV HBM (class H2)}$
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

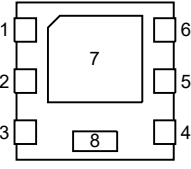
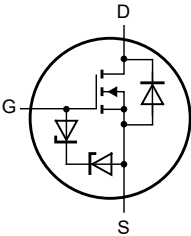
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	80	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25\text{ °C}$	-	-	9.8	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$	-	-	18.8	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 3.2\text{ A}; T_j = 25\text{ °C}$	-	62	81	m $\Omega$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	 <p>017aaa255</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6D81-80E	DFN2020MD-6	plastic, leadless thermal enhanced ultra thin small outline package; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6D81-80E	4W

## 8. Limiting values

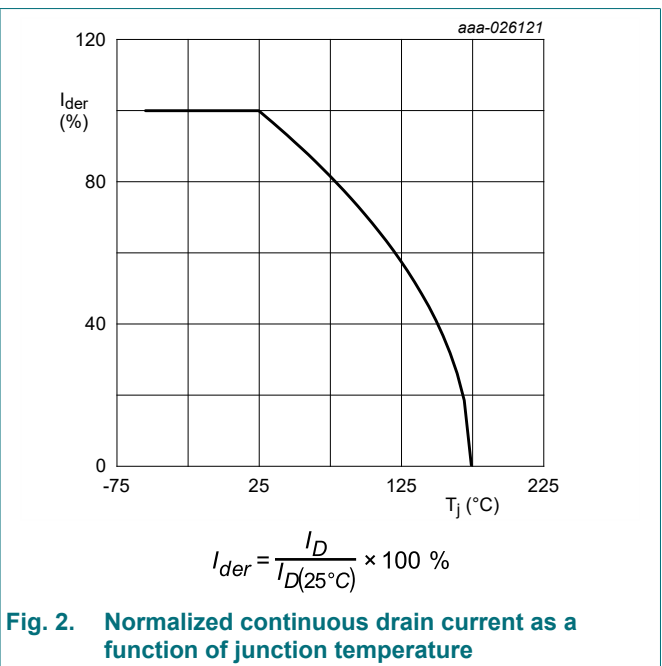
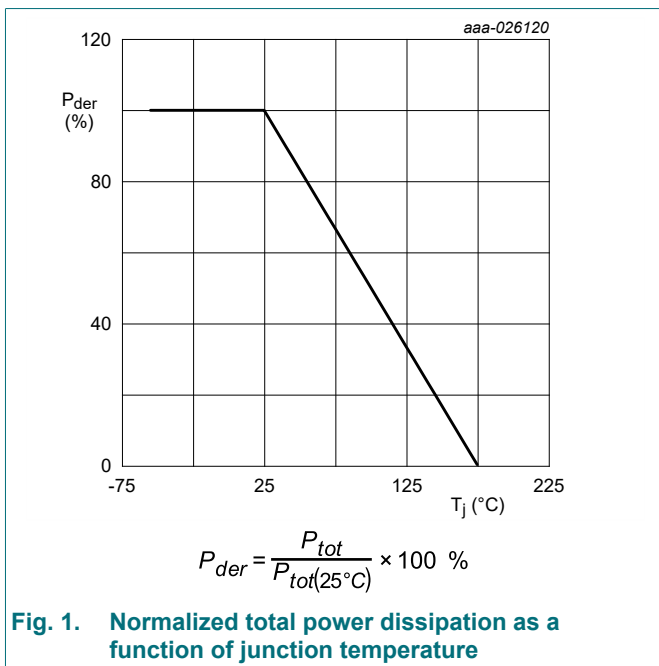
**Table 5. Limiting values**

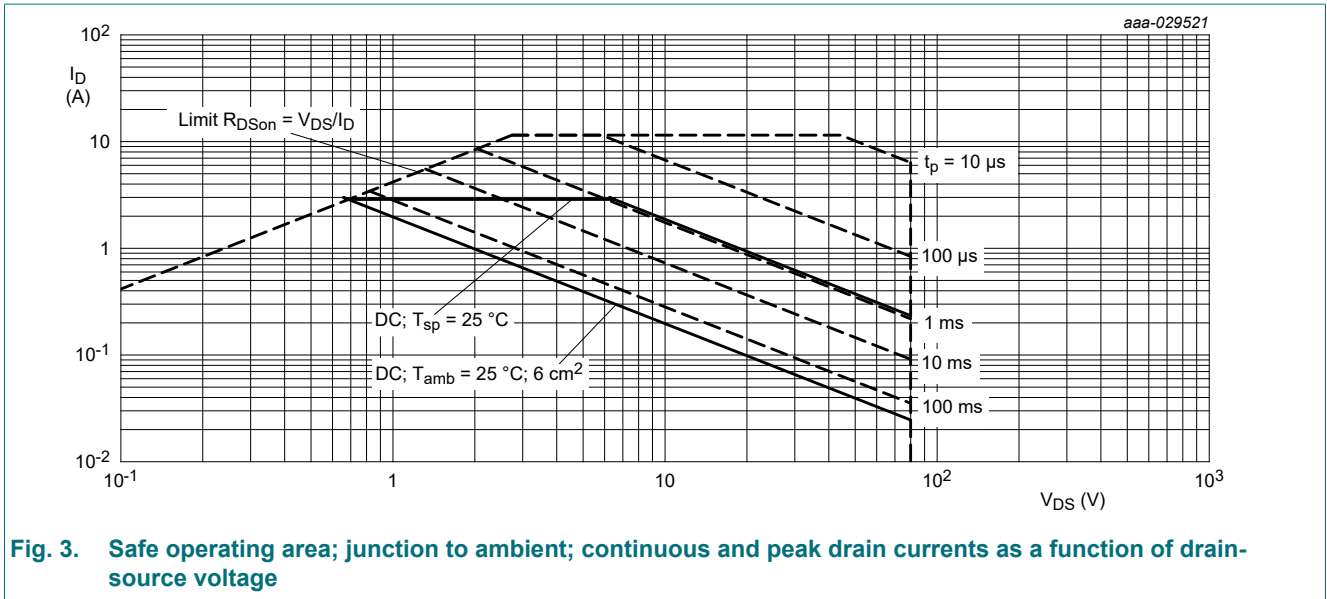
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	80	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 25 °C	-	9.8	A
		V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 100 °C	-	6.9	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	3.2	A
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs	-	39	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C	-	18.8	W
		T <sub>amb</sub> = 25 °C	[1]	2	W
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>amb</sub>	ambient temperature		-55	175	°C
T <sub>stg</sub>	storage temperature		-65	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C	-	6.9	A
		T <sub>amb</sub> = 25 °C	[1]	2	A
I <sub>SM</sub>	peak source current	single pulse; t <sub>p</sub> ≤ 10 μs; T <sub>sp</sub> = 25 °C	-	28	A
<b>ESD maximum rating</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[2]	2000	V
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 0.46 A; DUT in avalanche (unclamped)	-	19.3	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

[2] Measured between all pins.





### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	66	76	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	4	8	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

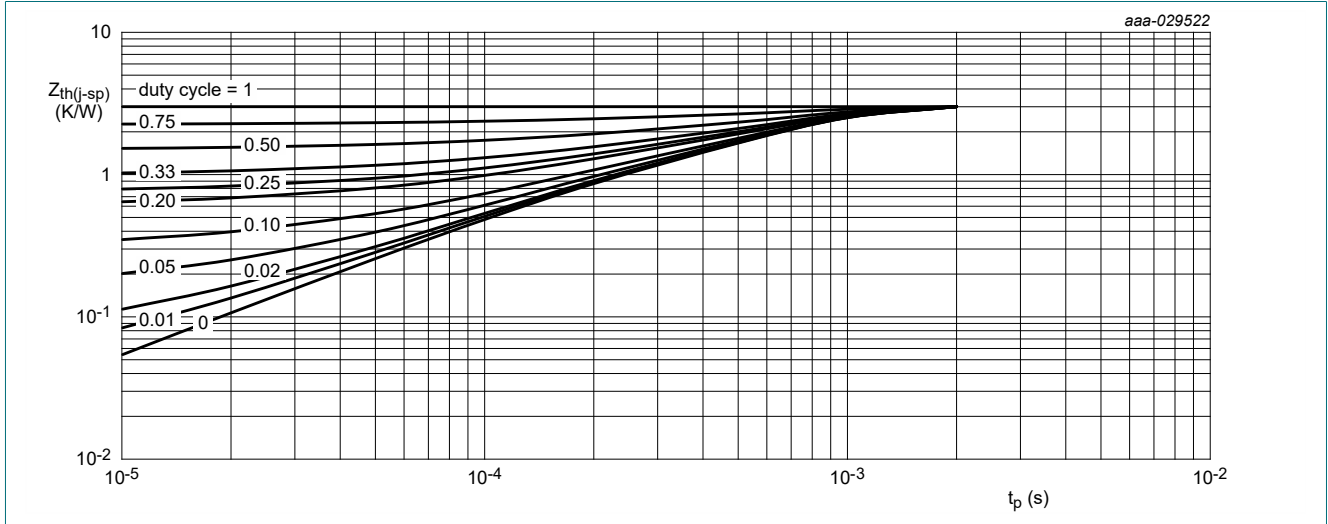


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values

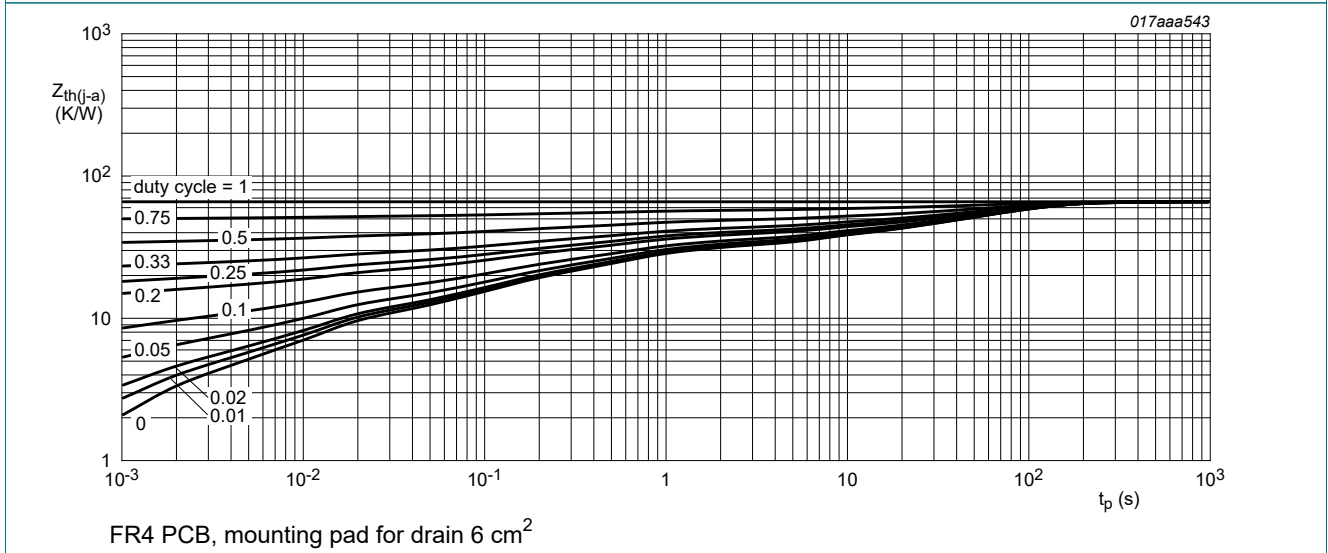


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	80	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1.3	1.7	2.7	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	20	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 3.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	62	81	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 3.2 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	151	197	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 2.9 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	70	97	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 3.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	13.3	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	4.7	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 40 \text{ V}; I_D = 3.2 \text{ A}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	9.9	14.9	nC
$Q_{GS}$	gate-source charge		-	1.2	-	nC
$Q_{GD}$	gate-drain charge		-	1.8	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 40 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	504	-	pF
$C_{oss}$	output capacitance		-	43	-	pF
$C_{rss}$	reverse transfer capacitance		-	26	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; I_D = 3.2 \text{ A}; V_{GS} = 10 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	5	-	ns
$t_r$	rise time		-	4	-	ns
$t_{d(off)}$	turn-off delay time		-	15	-	ns
$t_f$	fall time		-	7	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 2 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 1.9 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 40 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	12.4	-	ns
$Q_r$	recovered charge		-	5.4	-	nC

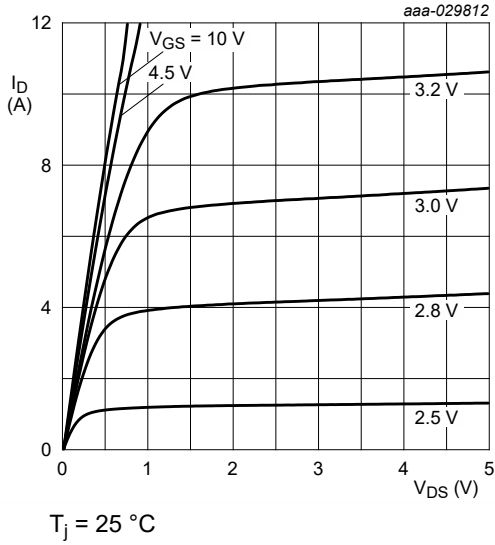


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

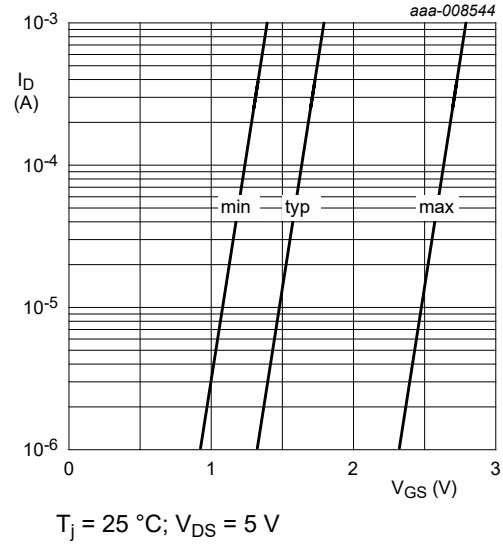


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

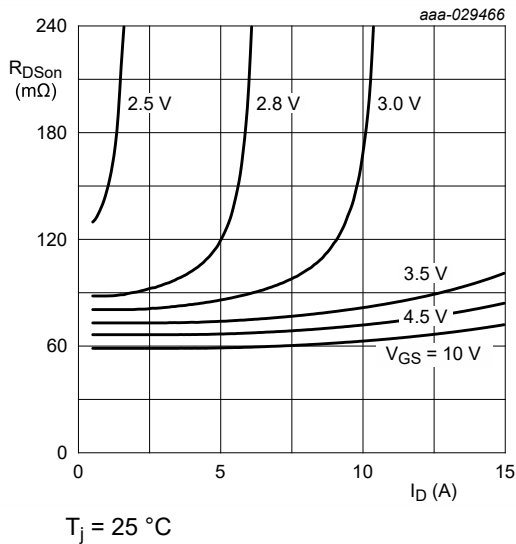


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

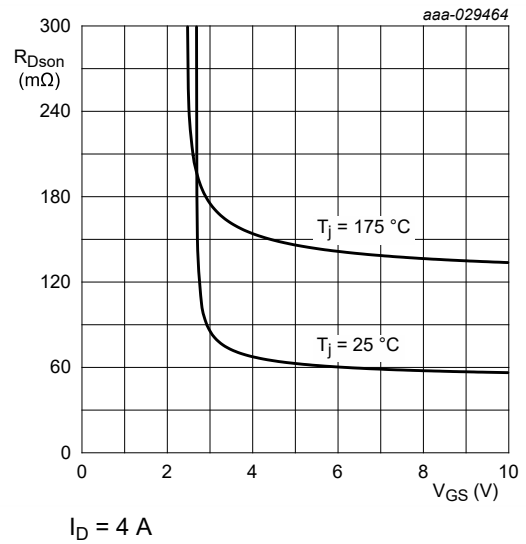
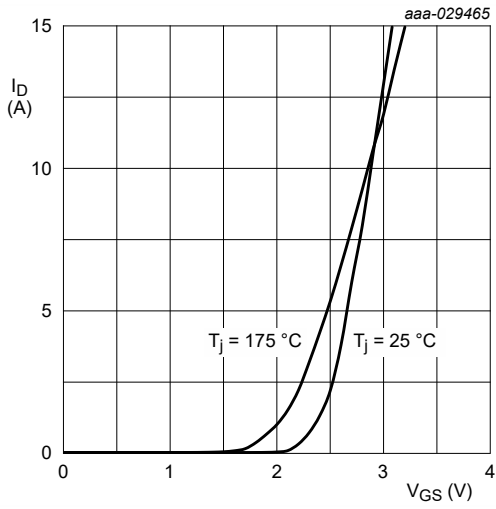
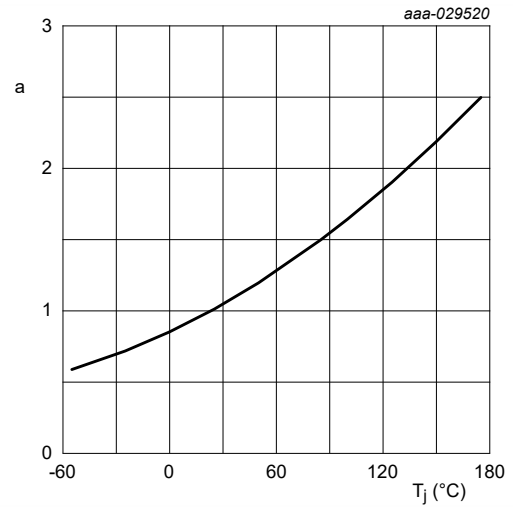


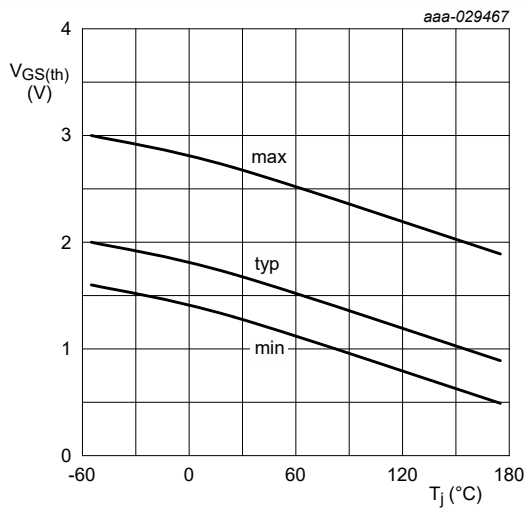
Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



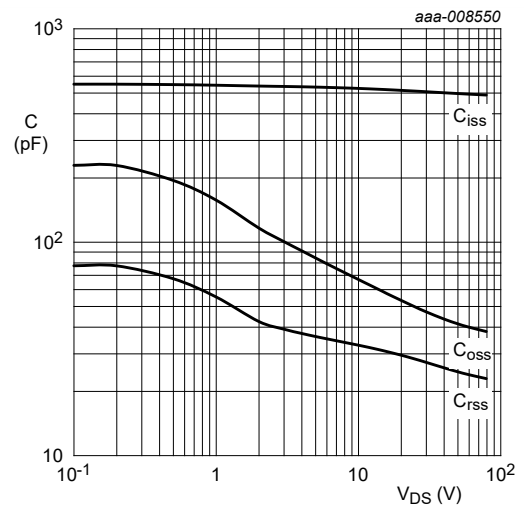
**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



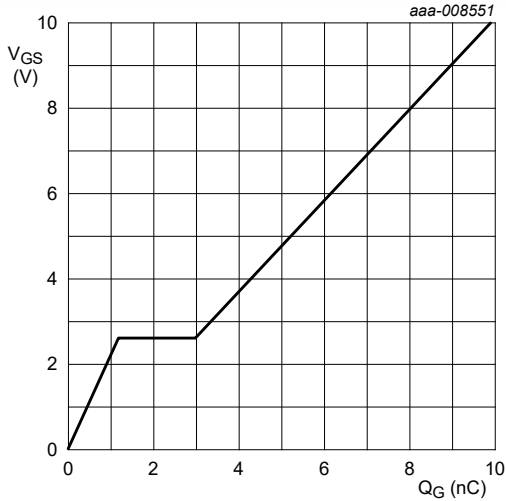
**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**



**Fig. 12. Gate-source threshold voltage as a function of junction temperature**



**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$I_D = 2.8 \text{ A}$ ;  $V_{DS} = 40 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

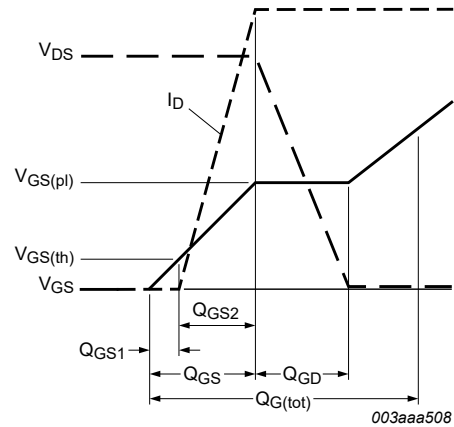
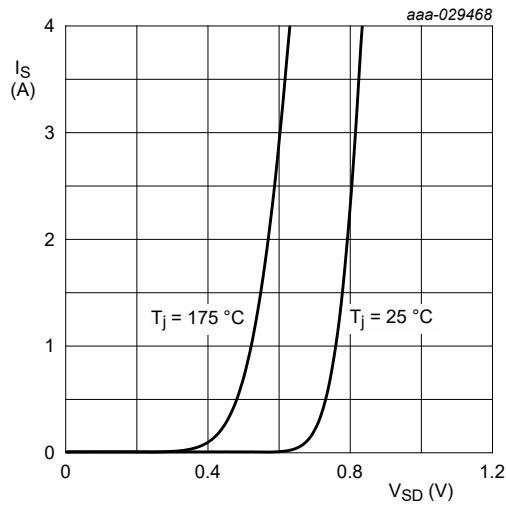


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

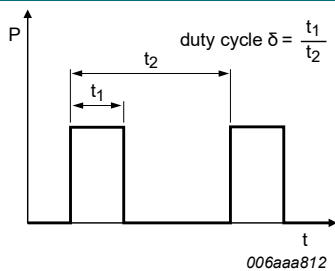


Fig. 17. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads;  
6 terminals; body 2 x 2 x 0.65 mm

SOT1220

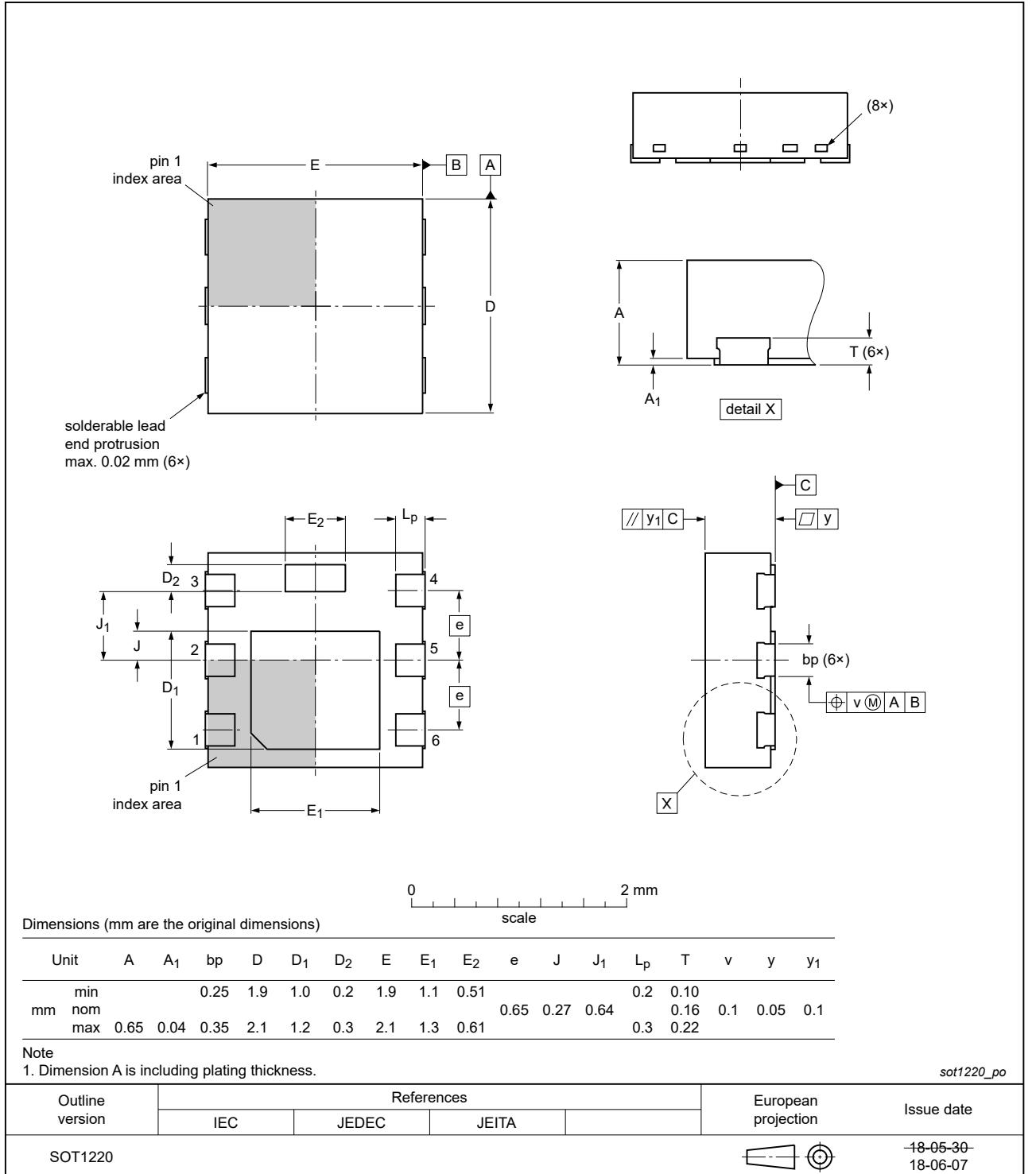


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

### 13. Soldering

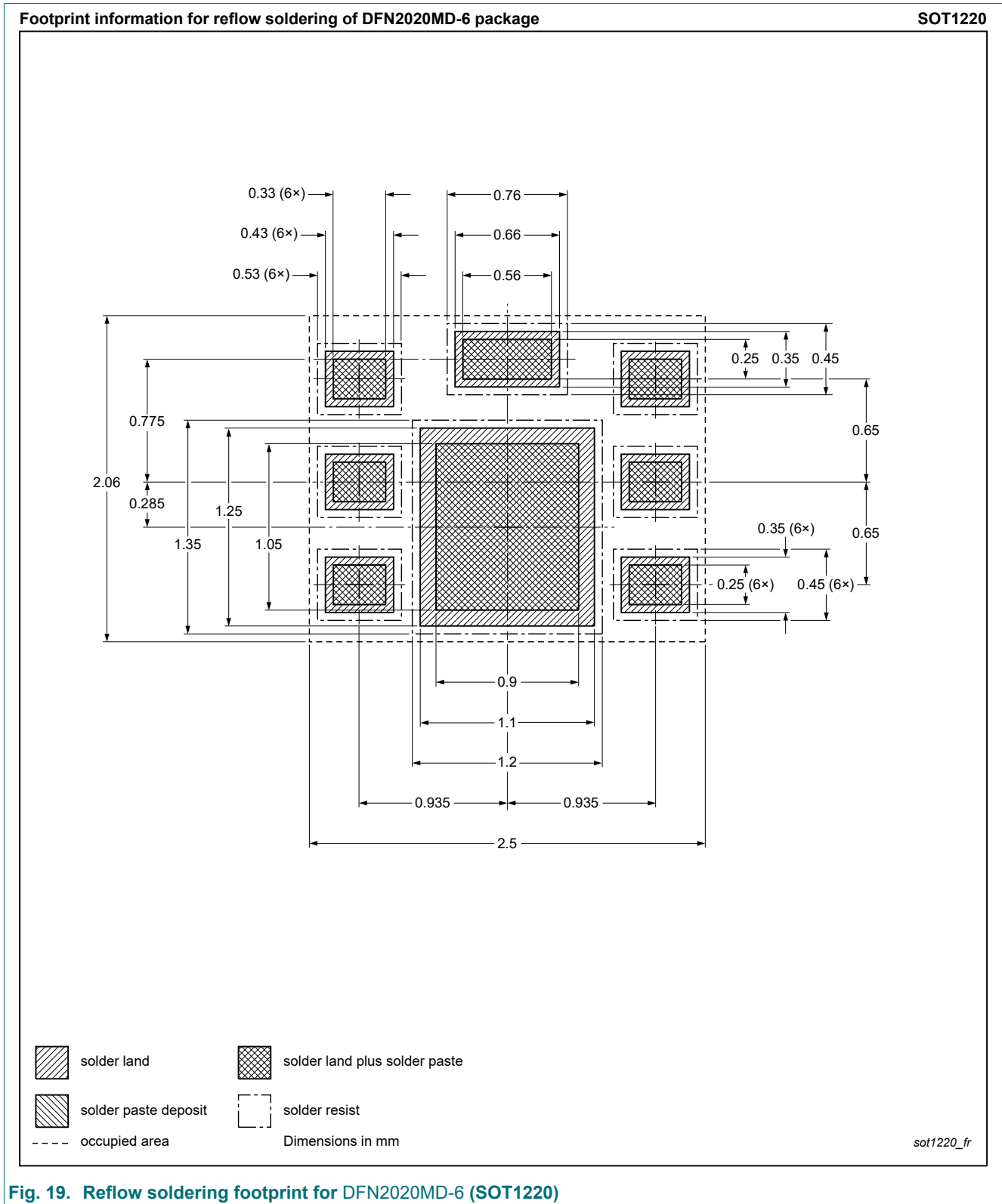


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6D81-80E v.1	20190404	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 4 April 2019

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