

Phase Control Thyristors (Hockey PUK Version), 910 A



TO-200AC (B-PUK)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AC (B-PUK)
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912


**RoHS
COMPLIANT**
TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY

Package	TO-200AC (B-PUK)
Diode variation	Single SCR
$I_{T(AV)}$	910 A
V_{DRM}/V_{RRM}	1200 V, 1600 V, 1800 V, 2000 V
V_{TM}	1.80 V
I_{GT}	100 mA
T_J	-40 °C to 125 °C

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		910	A
	T_{hs}	55	°C
$I_{T(RMS)}$		1857	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	15 700	A
	60 Hz	16 400	
I^2t	50 Hz	1232	kA ² s
	60 Hz	1125	
V_{DRM}/V_{RRM}		1200 to 2000	V
t_q	Typical	150	μs
T_J		-40 to 125	°C

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST700CL	12	1200	1300	80
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled		910 (355)	A
				55 (85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled		1857	A
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	15 700	
		t = 8.3 ms		16 400	
		t = 10 ms	100 % V_{RRM} reapplied	13 200	
		t = 8.3 ms		13 800	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied	1232	kA ² s
		t = 8.3 ms		1125	
		t = 10 ms	100 % V_{RRM} reapplied	871	
		t = 8.3 ms		795	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied		12 321	kA ² /s
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$, $T_J = T_J$ maximum)		1.00	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > $\pi \times I_{T(AV)}$, $T_J = T_J$ maximum)		1.13	
Low level value of on-state slope resistance	$r_{\theta 1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$, $T_J = T_J$ maximum)		0.40	mΩ
High level value of on-state slope resistance	$r_{\theta 2}$	(I > $\pi \times I_{T(AV)}$, $T_J = T_J$ maximum)		0.35	
Maximum on-state voltage	V_{TM}	$I_{pk} = 2000$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine pulse		1.80	V
Maximum holding current	I_H	$T_J = 25$ °C, anode supply 12 V resistive load		600	mA
Typical latching current	I_L			1000	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}		1000	A/μs
Typical delay time	t_d	Gate current 1 A, di _g /dt = 1 A/μs $V_d = 0.67$ % V_{DRM} , $T_J = 25$ °C		1.0	μs
Typical turn-off time	t_q	$I_{TM} = 750$ A, $T_J = T_J$ maximum, di/dt = 60 A/μs, $V_R = 50$ V, dV/dt = 20 V/μs, gate 0 V 100 Ω, $t_p = 500$ μs		150	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}		500	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied		50	mA



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS	
			Typ.	Max.		
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10.0		W	
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0			
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0		A	
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	20		V	
Maximum peak negative gate voltage	$-V_{GM}$		5.0			
DC gate current required to trigger	I_{GT}	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	$T_J = -40$ °C	200	-	mA
			$T_J = 25$ °C	100	200	
			$T_J = 125$ °C	50	-	
DC gate voltage required to trigger	V_{GT}	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	$T_J = -40$ °C	2.5	-	V
			$T_J = 25$ °C	1.8	3.0	
			$T_J = 125$ °C	1.1	-	
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	10		mA	
DC gate voltage not to trigger	V_{GD}		0.25		V	

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{Stg}		-40 to 150	
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.073	K/W
		DC operation double side cooled	0.031	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.011	
		DC operation double side cooled	0.006	
Mounting force, ± 10 %			14 700 (1500)	N (kg)
Approximate weight			255	g
Case style		See dimensions - link at the end of datasheet	TO-200AC (B-PUK)	

ΔR_{thJ-hs} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.009	0.009	0.006	0.006	$T_J = T_J$ maximum	K/W
120°	0.011	0.011	0.011	0.011		
90°	0.014	0.014	0.015	0.015		
60°	0.020	0.020	0.021	0.021		
30°	0.036	0.036	0.036	0.036		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC



Fig. 1 - Current Ratings Characteristics



Fig. 4 - Current Ratings Characteristics



Fig. 2 - Current Ratings Characteristics



Fig. 5 - On-State Power Loss Characteristics



Fig. 3 - Current Ratings Characteristics



Fig. 6 - On-State Power Loss Characteristics

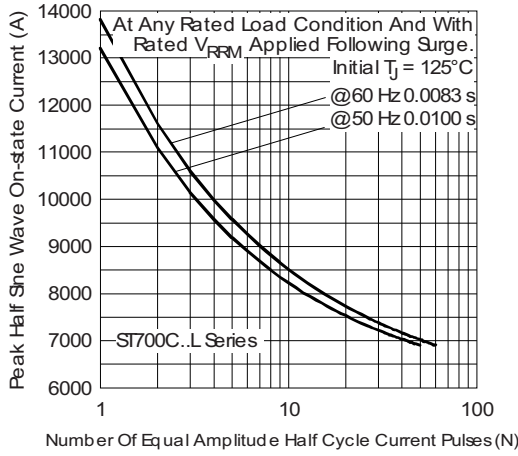


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled



Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled



Fig. 9 - On-State Voltage Drop Characteristics



Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics



Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code	VS-	ST	70	0	C	20	L	1	-
	①	②	③	④	⑤	⑥	⑦	⑧	⑨
	1	-	Vishay Semiconductors product	2	-	Thyristor	3	-	Essential part number
	4	-	0 = Converter grade	5	-	C = Ceramic PUK	6	-	Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
	7	-	L = PUK case TO-200AC (B-PUK)	8	-	0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)		1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)	2 = Eyelet terminals (gate and auxiliary cathode soldered leads)
								3 = Fast-on terminals (gate and auxiliary cathode soldered leads)	
	9	-	Critical dV/dt : • None = 500 V/ μs (standard selection)						• L = 1000 V/ μs (special selection)

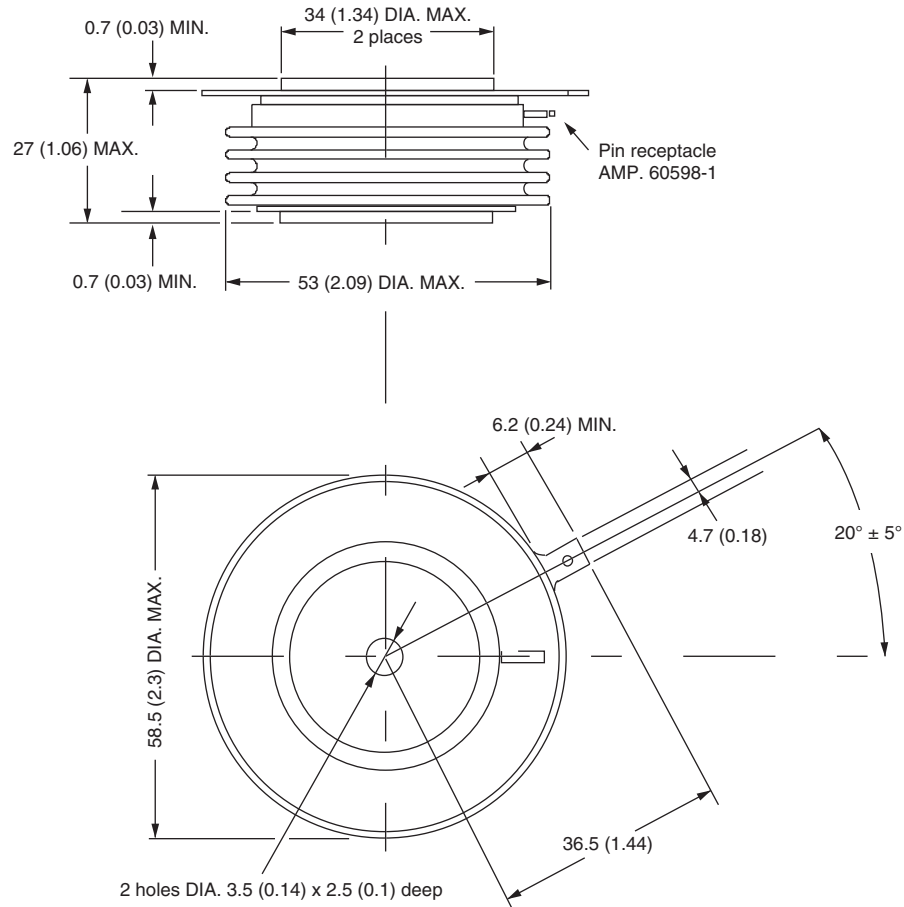
LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95076
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TO-200AC (B-PUK)

DIMENSIONS in millimeters (inches)

Creepage distance: 36.33 (1.430) minimum
 Strike distance: 17.43 (0.686) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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