STPAC01F2

IPAD™, RF detector for power amplifier control

Features

- STPAC01F2 has two outputs
  - one for the signal detection
  - one for the temperature compensation
- V_{DCout} = 0.88 V at 0.85 GHz at 10 dBm
- V_{DCout} = 1.07 V at 1.85 GHz at 10 dBm
- V_{supply} = 5 V max
- Lead-free package

Benefit

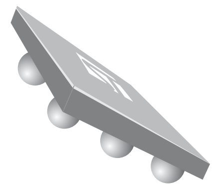
- The use of IPAD technology allows the RF front-end designer to save PCB area and to drastically reduce parasitic inductances.

Applications

Target applications are cellular phones and PDA using GSM, DCS, PCS, AMPS, TDMA, CDMA and 800 MHz to 1900 MHz frequency ranges.

Description

The STPAC01F2 is an integrated RF detector for the power control stage. It converts RF signal coming from the coupler into a DC signal usable by the digital stage. It is based on the use of two similar diodes, one providing the signal detection while the second one is used to provide temperature information to a thermal compensation stage. A biasing stage suppresses the detection diode drop voltage effect.



Flip Chip
(8 bumps)

Figure 1. Pin layout (bump side)

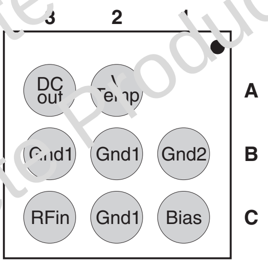
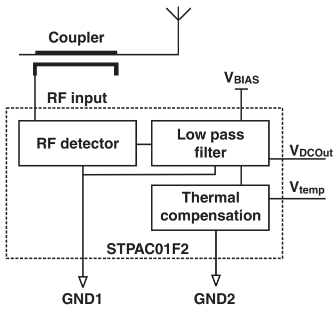


Figure 2. Functional diagram



TM: IPAD is a trademark of STMicroelectronics.

1 Characteristics

Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{BIAS}	Bias voltage	5	V
P_{RF}	RF power at the RF input	20	dBm
F_{OP}	Operating frequency range	0.8 to 2	GHz
V_{PP}	ESD level as per MIL-STD 883E method 3015.7 notice 8 (HBM)	250	V
T_{OP}	Operating temperature range	- 30 to + 85	°C
T_{STG}	Storage temperature range	- 55 to + 150	°C

Table 2. Parameters related to bias voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BIAS}	Operating bias voltage		2.2		3.2	V
I_{BIAS}	Bias current	V_{BIAS} = 3.2 V			0.5	mA

Table 3. Parameters related to detection function (V_{BIAS} + 2.7 V, DC output load = 100 kΩ)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DCout}	DC output voltage (see *Figure 1*, I_{DC} = 50 µA)	F = 1.85 GHz, P_{RF} = 10 dBm	0.97	1.07	1.17	V
		F = 1.85 GHz, P_{RF} = - 20 dBm	1.83	1.93	2.03	
		F = 0.85 GHz, P_{RF} = 10 dBm	0.78	0.88	0.98	
		F = 0.85 GHz, P_{RF} = - 20 dBm	1.83	1.93	2.03	
ΔV_{DCout}	DC output voltage variation (see *Figure 7*, I_{DC} = 50 µA)	0 < T_{amb} < 70 °C F = 1.85 GHz, P_{RF} = 10 dBm		0.09		V
		2.2 < V_{BIAS} < 3.2 V F = 1.85 GHz, P_{RF} = 10 dBm		0.44		

Table 4. Parameters related detection function

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{Temp}	Temperature output voltage (see *Figure 8*)	I_{DC} = 50 µA	1.83	1.93	2.03	V
ΔV_{Temp}	Temperature output voltage variation (see *Figure 8*)	I_{DC} = 50 µA, 0 < T_{amb} < 70 °C		0.09		V
		I_{DC} = 50 µA, 2.2 < V_{BIAS} < 3.2V		0.44		

Figure 3. V_{DCout} measurement circuit

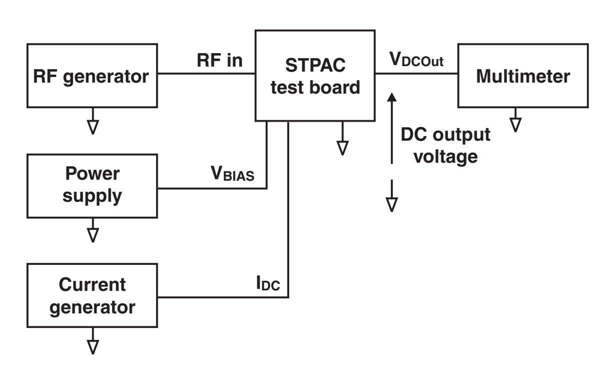


Figure 4. V_{DCout} versus RF input power

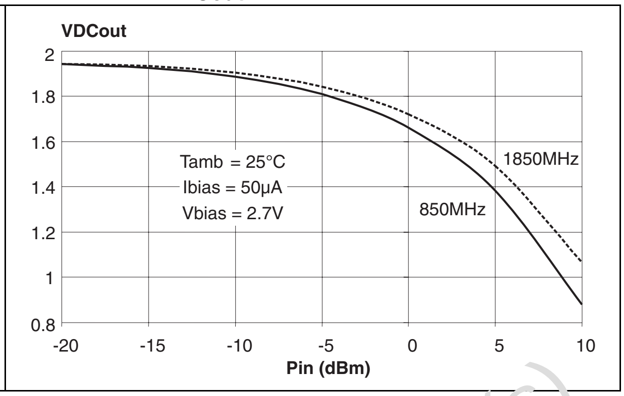


Figure 5. Relative variation of V_{DCout} versus frequency (from 800 to 900 MHz)

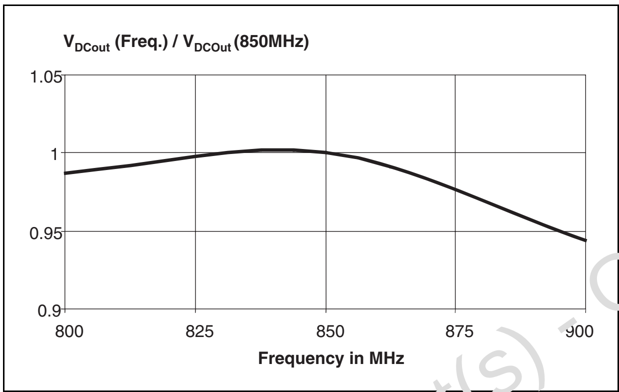


Figure 6. Relative variation of V_{DCout} versus frequency (from 1800 to 1900 MHz)

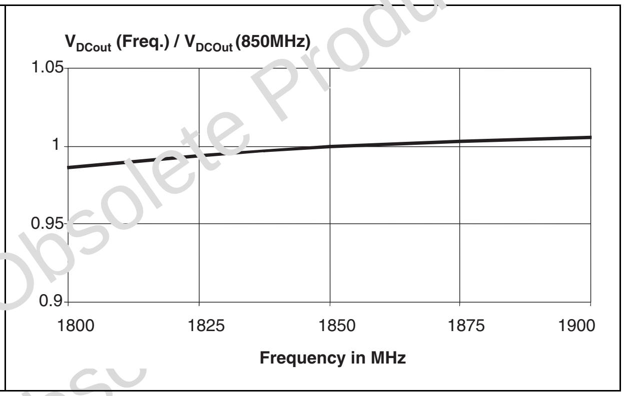


Figure 7. Temperature effect measurement circuit on V_{DCout}

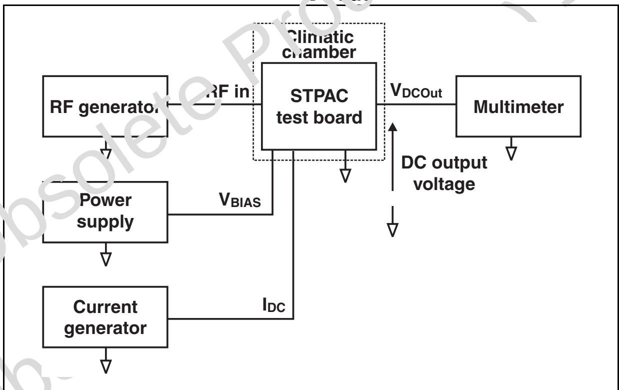


Figure 8. V_{temp} measurement circuit

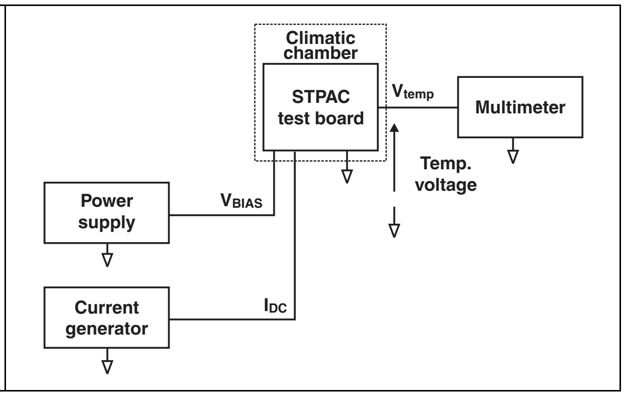
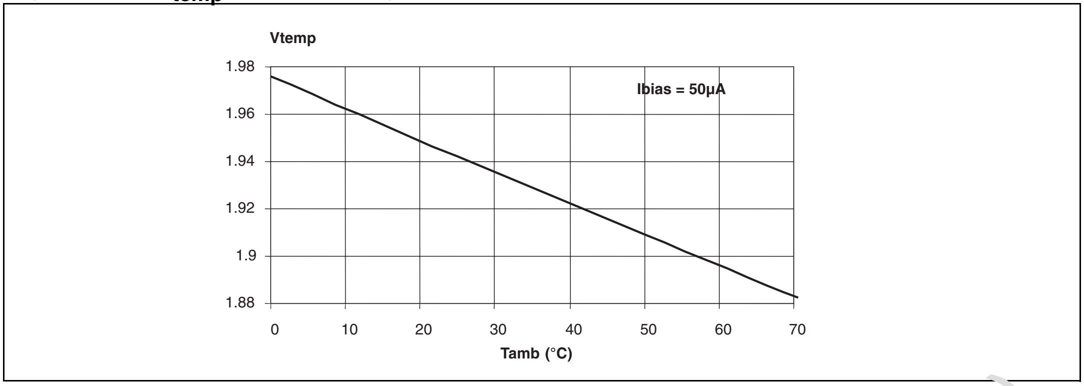
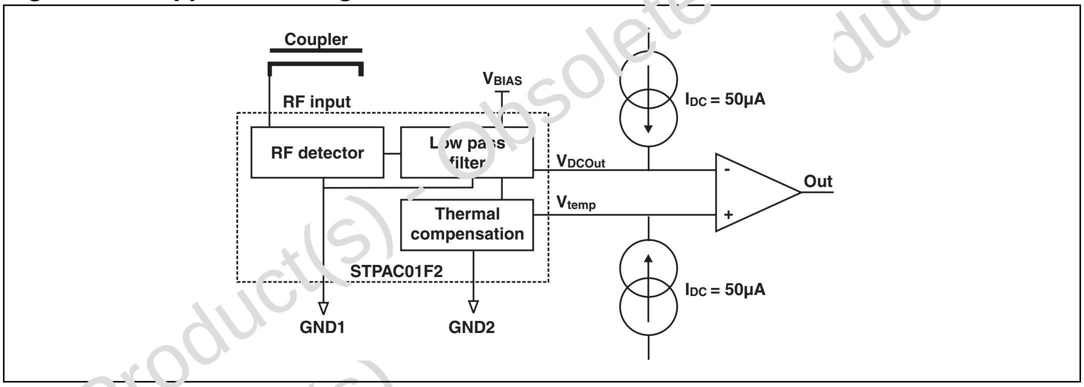


Figure 9. V_{temp} output voltage versus ambient temperature



2 Application information

Figure 10. Application diagram



The STPAC01 is the first part of the power amplifier stage and provides both RF power and die temperature measurements. *Figure 10* shows the basic circuit of RF detector.

A coupler located on the line between RF amplifier output and the antenna takes a part of the available power and applies it to STPAC01 RF input.

The RF detector and the low-pass filter provide a DC voltage depending on the input power. Thermal compensation provides a DC voltage depending on the ambient temperature. As the detection system and the thermal compensation are based on the same topology, VDCout will have the same temperature variation as Vtemp. Connected to a differential amplifier, the output will be a voltage directly linked to the RF input power. VDCout and Vtemp must be biased with 50 µA DC current.

This topology offers the most accurate output value as it is 100% compensated.

3 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 11. Flip Chip dimensions

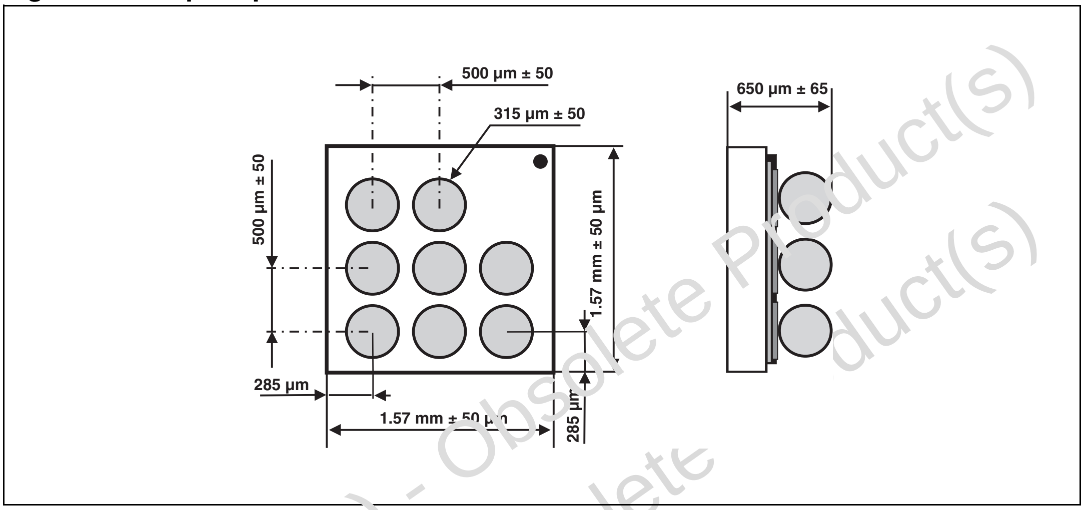


Figure 12. Footprint

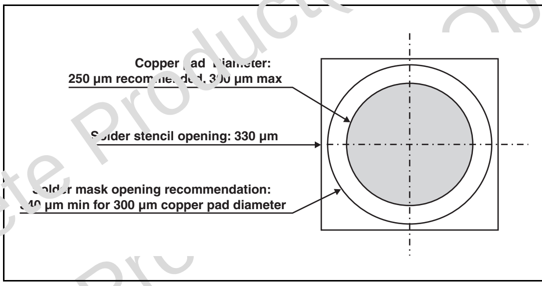


Figure 13. Marking

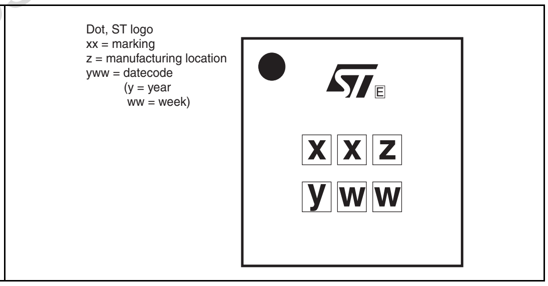
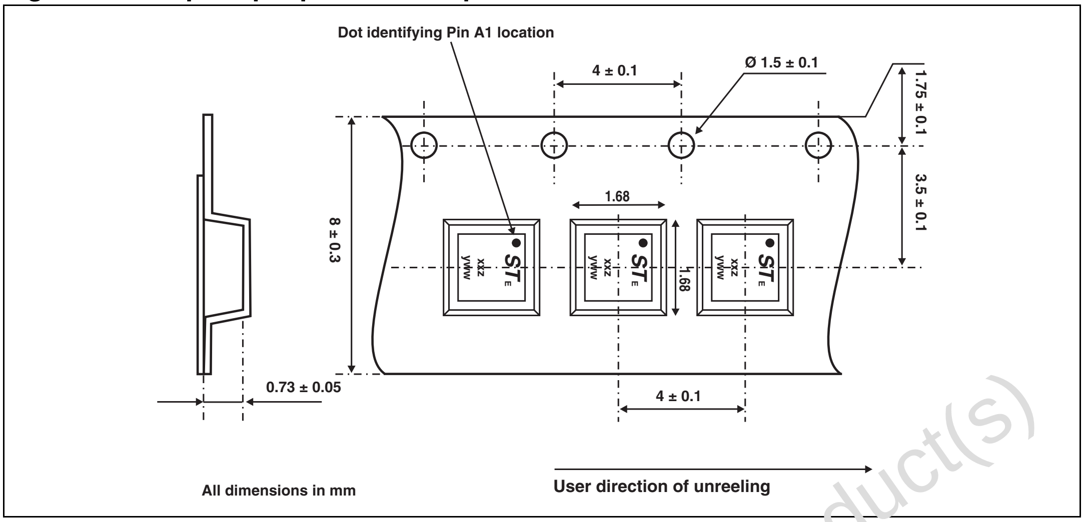


Figure 14. Flip Chip tape and reel specification



Note: More informations are available in the application notes:
AN1235:"Flip Chip: Package description and recommendations for use"
AN1751: “EMI filters: Recommendations and measurements”

4 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
STPAC01F2	RA	Flip Chip	3.3 mg	5000	Tape and reel 7”

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
21-Oct-2004	1	Initial release.
29-Apr-2008	2	Updated ECOPACK statement. Updated *Figure 11*, *Figure 12*, *Figure 13* and *Figure 14*. Reformatted to current standards.

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