

# MC14512B

## 8-Channel Data Selector

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

### Features

- Diode Protection on All Inputs
- Single Supply Operation
- 3-State Output (Logic “1”, Logic “0”, High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	$V_{DD}$	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	$V_{in}, V_{out}$	-0.5 to $V_{DD}$ + 0.5	V
Input or Output Current (DC or Transient) per Pin	$I_{in}, I_{out}$	$\pm 10$	mA
Power Dissipation, Per Package (Note 1)	$P_D$	500	mW
Ambient Temperature Range	$T_A$	-55 to +125	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}\text{C}$
Lead Temperature (8-Second Soldering)	$T_L$	260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### 1. Temperature Derating: Plastic “P and D/DW”

Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

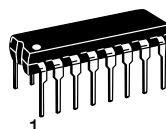
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



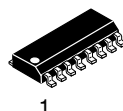
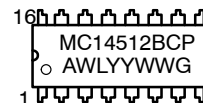
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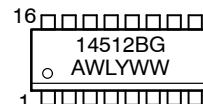
### MARKING DIAGRAMS



PDIIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



- A = Assembly Location
- WL = Wafer Lot
- YY, Y = Year
- WW = Work Week
- G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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## TRUTH TABLE

C	B	A	Inhibit	Disable	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	High Impedance

NOTE: X = Don't Care

## PIN ASSIGNMENT

X0	1 ●	16	V <sub>DD</sub>
X1	2	15	DIS
X2	3	14	Z
X3	4	13	C
X4	5	12	B
X5	6	11	A
X6	7	10	INH
V <sub>SS</sub>	8	9	X7

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14512BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14512BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14512BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0	“0” Level $V_{OL}$	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
$V_{in} = 0$ or $V_{DD}$	“1” Level $V_{OH}$	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
Input Voltage ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)	“0” Level $V_{IL}$	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	“1” Level $V_{IH}$	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)	Source $I_{OH}$	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mA c
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	Sink $I_{OL}$	5.0	0.64	–	0.51	0.88	–	0.36	–	mA c
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	$I_{in}$	15	–	$\pm 0.1$	–	$\pm 0.00001$	$\pm 0.1$	–	$\pm 1.0$	$\mu$ Adc
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	–	5.0	–	0.005	5.0	–	150	$\mu$ Adc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Note 3) (Note 4) (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0	$I_T = (0.8 \mu\text{A}/\text{kHz}) f + I_{DD}$						$\mu$ Adc	
		10	$I_T = (1.6 \mu\text{A}/\text{kHz}) f + I_{DD}$							
		15	$I_T = (2.4 \mu\text{A}/\text{kHz}) f + I_{DD}$							
3–State Leakage Current	$I_{TL}$	15	–	$\pm 0.1$	–	$\pm 0.0001$	$\pm 0.1$	–	$\pm 3.0$	$\mu$ Adc

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:  $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$  where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001$ .

## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ , See Figure 1)

Characteristic	Symbol	$V_{DD}$	All Types		Unit
			Typ (Note 6)	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns}/\text{pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns}/\text{pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns}/\text{pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0	100	200	ns
		10	50	100	
		15	40	80	
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	$t_{PLH}$	5.0	330	650	ns
		10	125	250	
		15	85	170	
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	$t_{PHL}$	5.0	330	650	ns
		10	125	250	
		15	85	170	
3–State Output Delay Times (Figure 3) “1” or “0” to High Z, and High Z to “1” or “0”	$t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}$	5.0	60	150	ns
		10	35	100	
		15	30	75	

5. The formulas given are for the typical characteristics only at 25°C.

6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

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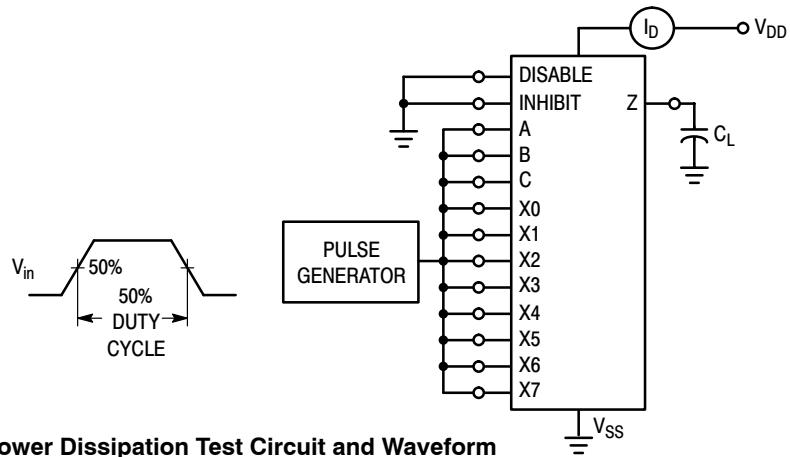


Figure 1. Power Dissipation Test Circuit and Waveform

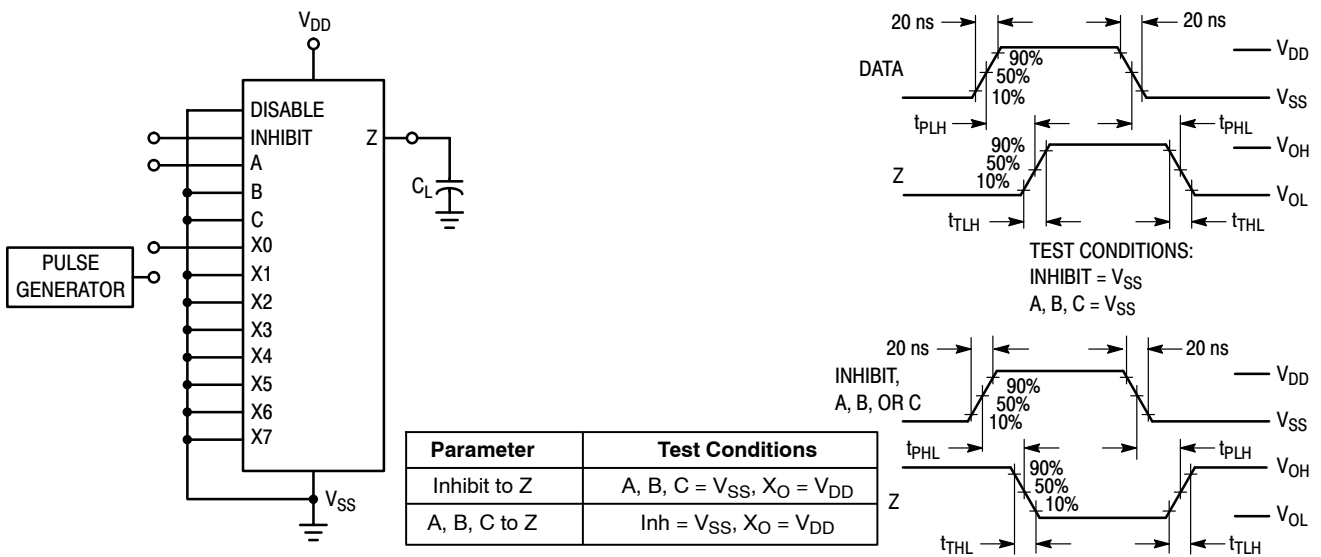


Figure 2. AC Test Circuit and Waveforms

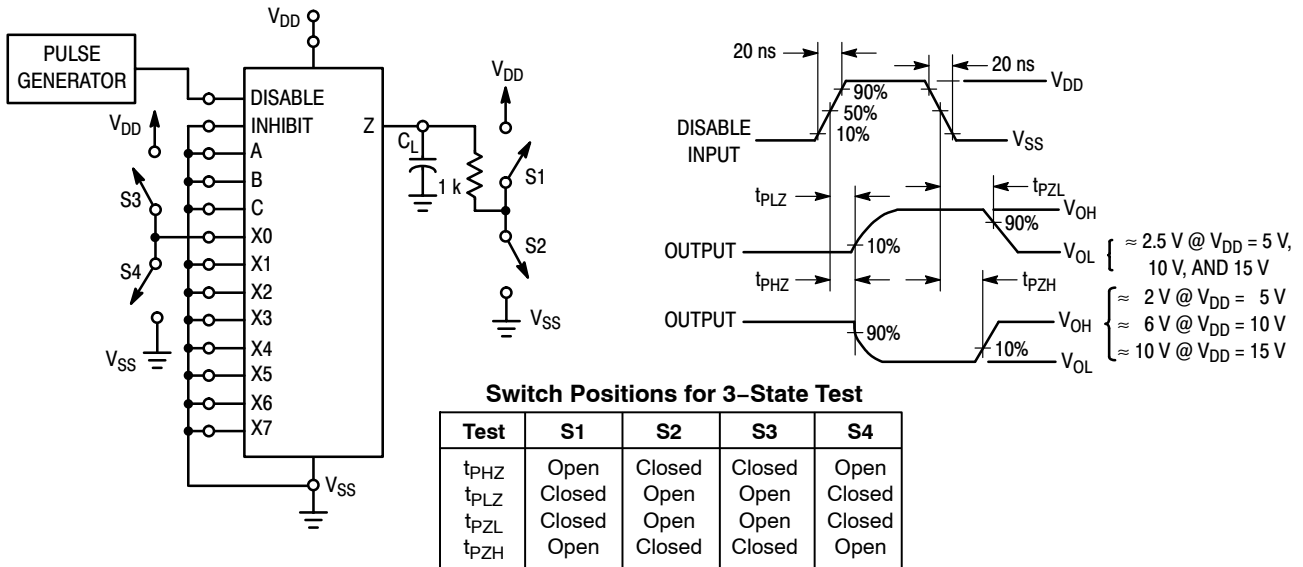
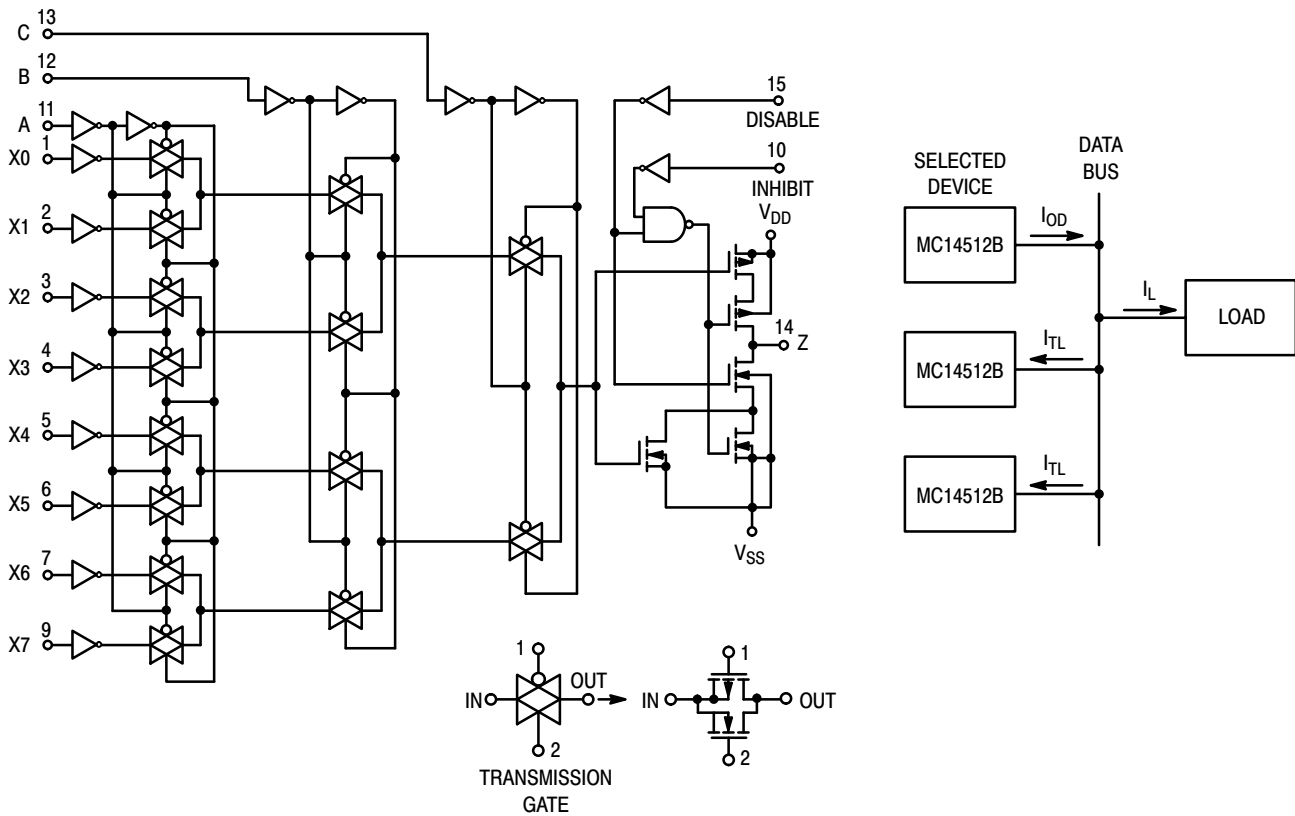


Figure 3. 3-State AC Test Circuit and Waveform

# MC14512B

## LOGIC DIAGRAM



### 3-STATE MODE OF OPERATION

Output terminals of several MC14512B 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high-impedance "off" state. The number of 8-bit data selectors,  $N$ , that may be connected to a bus line is determined from the output drive current,  $I_{OD}$ , 3-state or disable output leakage current,  $I_{TL}$ , and the load current,  $I_L$ , required to drive the bus line

(including fanout to other device inputs), and can be calculated by:

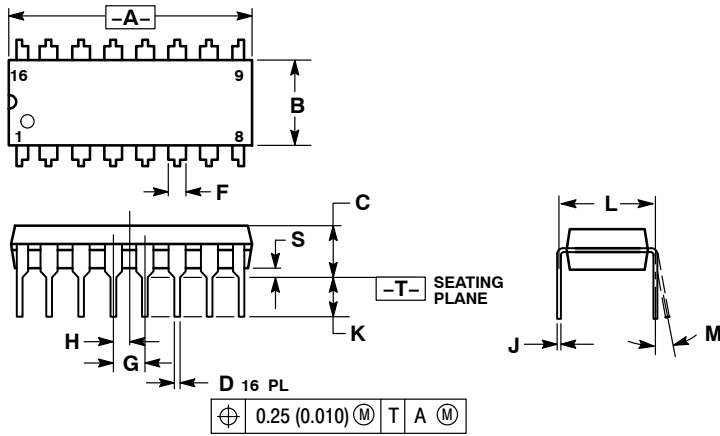
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

$N$  must be calculated for both high and low logic state of the bus line.

# MC14512B

## PACKAGE DIMENSIONS

PDIP-16  
CASE 648-08  
ISSUE T



NOTES:

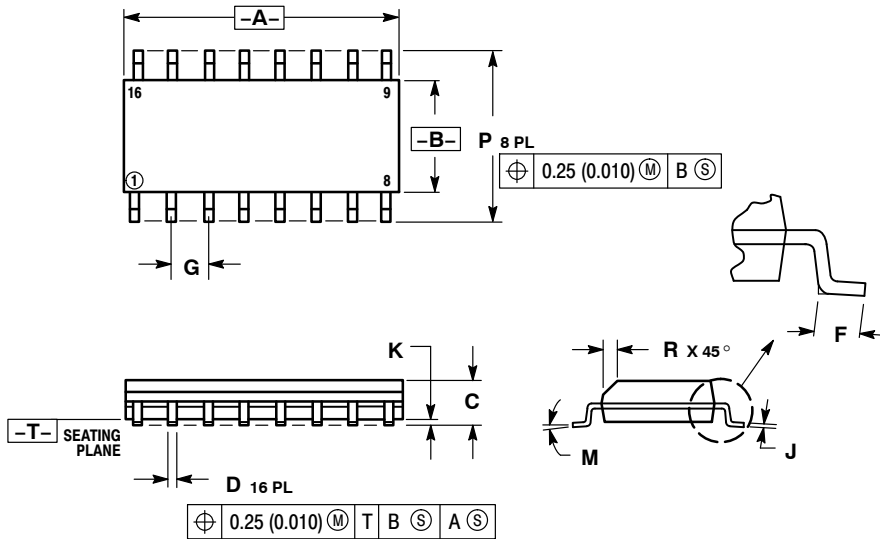
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

# MC14512B

## PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

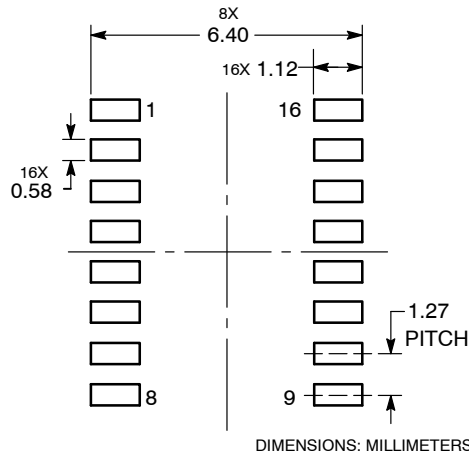


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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