25LC640A

64K SPI Bus Serial EEPROM Extended (M) Operating Temperatures

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25LC640A	2.5-5.5V	32 Byte	M	SN

Features:

- Max. Clock 10 MHz
- Low-Power CMOS Technology
 - Max. Write Current: 5 mA at 5.5V, 10 MHz
 - Read Current: 5 mA at 5.5V. 10 MHz
 - Standby Current: 5 µA at 5.5V, 125°C
- 8192 x 8-bit Organization
- · 32 Byte Page
- · Self-Timed Erase and Write Cycles (5 ms max.)
- · Block Write Protection
 - Protect none, 1/4, 1/2 or all of array
- Built-In Write Protection
 - Power-on/off data protection circuitry
 - Write enable latch
 - Write-protect pin
- · Sequential Read
- · High Reliability
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: > 200 years
 - ESD protection: > 4000V
- Temperature Ranges Supported:
 - Extended (M): -55°C to 125°C

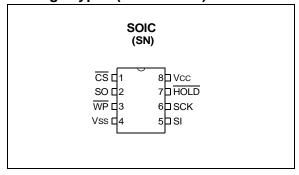
Description:

The Microchip Technology Inc. 25LC640A is a 64 kbit Serial Electrically Erasable PROM. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (CS) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25LC640A is available in 8-lead SOIC.

Package Types (not to scale)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Vcc	6.5V
All inputs and outputs w.r.t. Vss	0.6V to Vcc +1.0V
Storage temperature	65°C to 150°C
Ambient temperature under bias	55°C to 125°C
ESD protection on all pins	4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHA	ARACTERI	STICS	Extended (M): $TA = -55^{\circ}C$ to 12			25°C VCC = 2.5V to 5.5V
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
D001	VIH1	High-level input voltage	.7 Vcc	Vcc +1	V	
D002	VIL1	Low-level input	-0.3	0.3 Vcc	V	Vcc ≥ 2.7V
D003	VIL2	voltage	-0.3	0.2 Vcc	V	Vcc < 2.7V
D004	Vol	Low-level output	_	0.4	V	IOL = 2.1 mA
D005	Vol	voltage	_	0.2	V	IOL = 1.0 mA, VCC < 2.5V
D006	Voн	High-level output voltage	Vcc -0.5	_	V	ΙΟΗ = -400 μΑ
D007	ILI	Input leakage current	_	±1	μΑ	CS = Vcc, Vin = Vss or Vcc
D008	ILO	Output leakage current	_	±1	μА	CS = Vcc, Vout = Vss or Vcc
D009	CINT	Internal Capacitance (all inputs and outputs)	_	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V (Note)
D010	Icc Read		_	5	mA	VCC = 5.5V; FCLK = 10.0 MHz;
		Operating Current	_	2.5	mA	SO = Open VCC = 2.5V; FCLK = 5.0 MHz; SO = Open
D011	Icc Write		_	5	mA	Vcc = 5.5V
			_	3	mA	VCC = 2.5V
D012	Iccs	Standby Current	_ _	5	μА	CS = Vcc = 5.5V, Inputs tied to Vcc or Vss, 125°C
				1	μА	CS = Vcc = 5.5V, Inputs tied to Vcc or Vss, 85°C

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHA	RACTE	ERISTICS	Extended (N	Л): ТА =	-55°C to	125°C VCC = 2.5V to 5.5V
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
1	FCLK	Clock frequency	_	10 5	MHz MHz	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
2	Tcss	CS setup time	50 100	_	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
3	Тсѕн	CS hold time	100 200	_	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
4	TCSD	CS disable time	50	_	ns	_
5	Tsu	Data setup time	10 20	_ _	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
6	THD	Data hold time	20 40	_	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
7	TR	CLK rise time	_	100	ns	(Note 1)
8	TF	CLK fall time	_	100	ns	(Note 1)
9	Тні	Clock high time	50 100	_ _	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
10	TLO	Clock low time	50 100	_	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
11	TCLD	Clock delay time	50	_	ns	_
12	TCLE	Clock enable time	50	_	ns	_
13	Tv	Output valid from clock low	_ _	50 100	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
14	Тно	Output hold time	0		ns	(Note 1)
15	TDIS	Output disable time	_ _	40 80	ns ns	4.5V ≤ Vcc ≤ 5.5V(Note 1) 2.5V ≤ Vcc ≤ 4.5V(Note 1)
16	THS	HOLD setup time	20 40		ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
17	Тнн	HOLD hold time	20 40	_	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
18	THZ	HOLD low to output High-Z	30 60	_	ns ns	4.5V ≤ Vcc ≤ 5.5V(Note 1) 2.5V ≤ Vcc < 4.5V(Note 1)
19	THV	HOLD high to output valid	30 60		ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
20	Twc	Internal write cycle time	_	5	ms	(NOTE 3)
21	_	Endurance	1M	_	E/W Cycles	(NOTE 2)

Note 1: This parameter is periodically sampled and not 100% tested.

- 2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.
- **3:** Two begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

25LC640A

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:					
VLO = 0.2V	_				
VHI = VCC - 0.2V	(Note 1)				
VHI = 4.0V	(Note 2)				
CL = 100 pF	_				
Timing Measurement Reference Level					
Input	0.5 Vcc				
Output	0.5 Vcc				

Note 1: For $VCC \le 4.0V$

FIGURE 1-1: HOLD TIMING

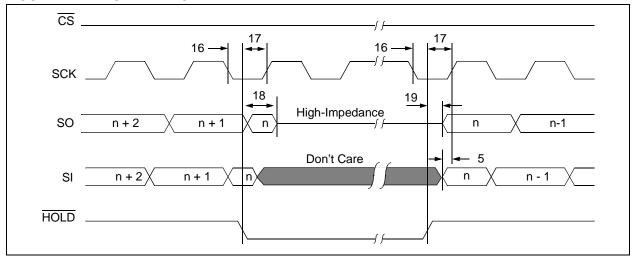


FIGURE 1-2: SERIAL INPUT TIMING

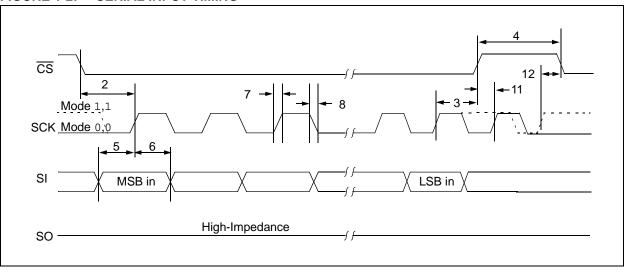
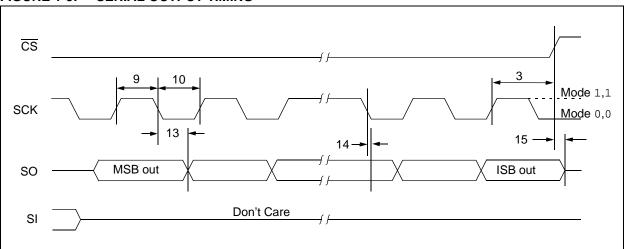


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25LC640A is a 8192-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25LC640A contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{\text{CS}}$ pin must be low and the $\overline{\text{HOLD}}$ pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred Most Significant Byte (MSB) first, Least Significant Byte (LSB) last.

Data $\underline{(SI)}$ is sampled on the first rising edge of SCK after \overline{CS} goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the \overline{HOLD} input and place the $\underline{25LC640A}$ in 'HOLD' mode. After releasing the \underline{HOLD} pin, operation will resume from the point when the \underline{HOLD} was asserted.

2.2 Read Sequence

The device is selected by pulling $\overline{\text{CS}}$ low. The 8-bit READ instruction is transmitted to the 25LC640A followed by the 16-bit address, with the three MSBs of the address being "don't care" bits. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFFh), the address counter rolls over to address 0000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{\text{CS}}$ pin (Figure 2-1).

2.3 Write Sequence

Prior to any attempt to write data to the 25LC640A, the write enable latch must be set by issuing the WREN instruction (Figure 2-4). This is done by setting $\overline{\text{CS}}$ low and then clocking out the proper instruction into the 25LC640A. After all eight bits of the instruction are transmitted, the $\overline{\text{CS}}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{\text{CS}}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{\text{CS}}$ low, issuing a WRITE instruction, followed by the 16-bit address, with the three MSBs of the address being "don't care" bits, and then the data to be written. Up to 32 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Note:

Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size - 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the $\overline{\text{CS}}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{\text{CS}}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 2-2 and Figure 2-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 2-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

BLOCK DIAGRAM

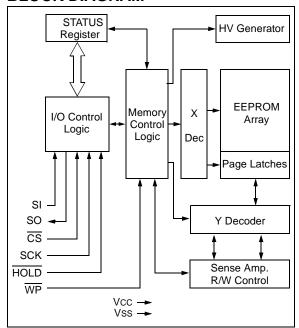


TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register

FIGURE 2-1: READ SEQUENCE

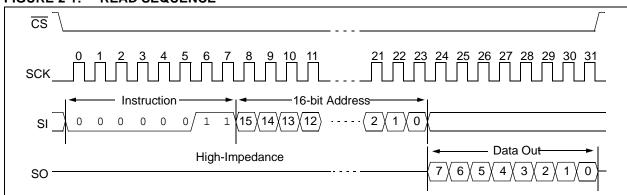


FIGURE 2-2: BYTE WRITE SEQUENCE

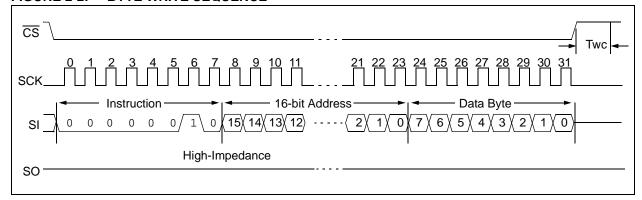
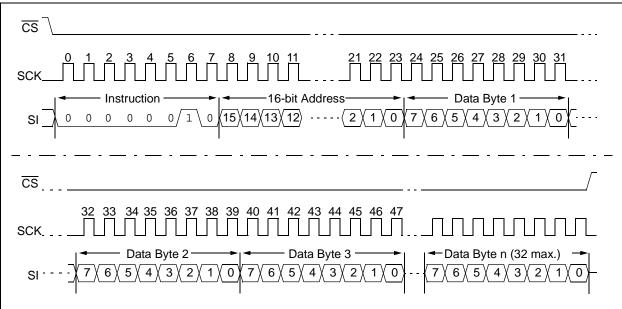


FIGURE 2-3: PAGE WRITE SEQUENCE



2.4 Write Enable (WREN) and Write Disable (WRDI)

The 25LC640A contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)

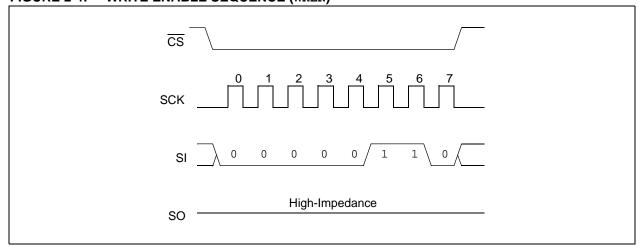
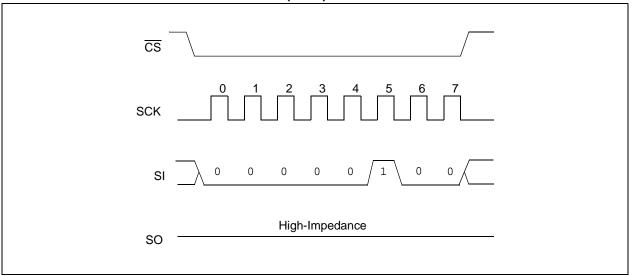


FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 2-2: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	_	-	-	W/R	W/R	R	R
WPEN	Χ	Χ	Χ	BP1	BP0	WEL	WIP
W/R = w	W/R = writable/readable. R = read-only.						

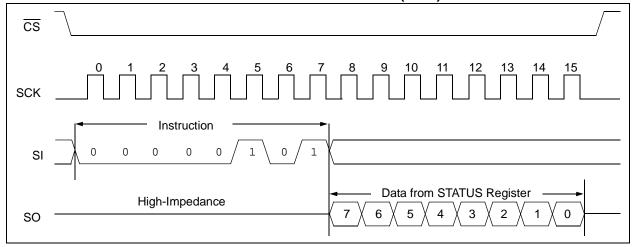
The **Write-In-Process (WIP)** bit indicates whether the 25LC640A is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 2-4 and Figure 2-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile, and are shown in Table 2-3.

See Figure 2-6 for the RDSR timing sequence.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 2-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as shown in Table 2-3.

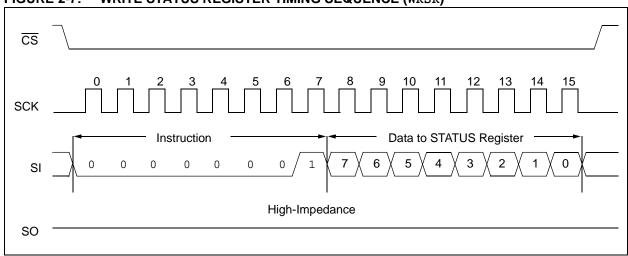
The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{\text{WP}}$ pin. The Write-Protect ($\overline{\text{WP}}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{\text{WP}}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{\text{WP}}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 2-4 for a matrix of functionality on the WPEN bit.

See Figure 2-7 for the WRSR timing sequence.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (1800h-1FFFh)
1	0	upper 1/2 (1000h-1FFFh)
1	1	all (0000h-1FFFh)

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



Note: An internal write cycle (Twc) is initiated on the rising edge of $\overline{\text{CS}}$ after a valid write STATUS register sequence.

2.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- CS must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.8 Power-On State

The 25LC640A powers on in the following state:

- The device is in low-power Standby mode (CS = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{\text{CS}}$ is required to enter active state

TABLE 2-4: WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7)	WP (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
0	x	x	Protected	Protected	Protected
1	0	x	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

x = don't care

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	Pin Number	Function	
CS	1	Chip Select Input	
SO	2	Serial Data Output	
WP	3	Write-Protect Pin	
Vss	4	Ground	
SI	5	Serial Data Input	
SCK	6	Serial Clock Input	
HOLD	7	Hold Input	
Vcc	8	Supply Voltage	

3.1 Chip Select (CS)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. If $\overline{\text{CS}}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{\text{CS}}$ after a valid write sequence initiates an internal write cycle. After powerup, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25LC640A. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Write-Protect (WP)

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When \overline{WP} is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When \overline{WP} is high, all functions, including writes to the nonvolatile bits in the STATUS register operate normally. If the WPEN bit is set, \overline{WP} low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, \overline{WP} going low will have no effect on the write.

The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25LC640A in a system with $\overline{\text{WP}}$ pin grounded and still be able to write to the STATUS register. The $\overline{\text{WP}}$ pin functions will be enabled when the WPEN bit is set high.

3.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.5 Serial Clock (SCK)

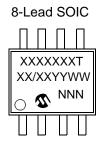
The SCK is used to synchronize the communication between a master and the 25LC640A. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

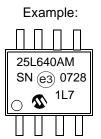
3.6 Hold (HOLD)

The HOLD pin is used to suspend transmission to the 25LC640A while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the HOLD pin may be pulled low to pause further serial communication without resetting the serial sequence. The HOLD pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-tolow transition. The 25LC640A must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, HOLD must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information





Legend: XX...X Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

e3 Pb-free JEDEC designator for Matte Tin (Sn)

* This package is Pb-free. The Pb-free JEDEC designator (e3)

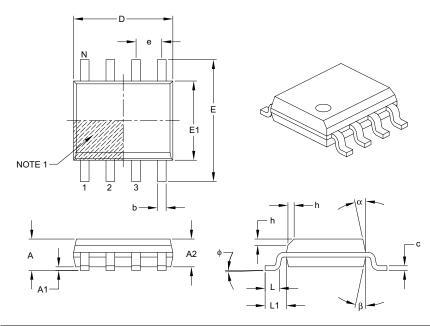
can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Custom marking available.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
D	imension Limits	MIN	NOM	MAX	
Number of Pins	N		8		
Pitch	е		1.27 BSC		
Overall Height	A	-	-	1.75	
Molded Package Thickness	A2	1.25	_	_	
Standoff §	A1	0.10	_	0.25	
Overall Width	E	6.00 BSC			
Molded Package Width	E1	3.90 BSC			
Overall Length	D		4.90 BSC		
Chamfer (optional)	h	0.25	-	0.50	
Foot Length	L	0.40	_	1.27	
Footprint	L1		1.04 REF		
Foot Angle	ф	0°	-	8°	
Lead Thickness	С	0.17	_	0.25	
Lead Width	b	0.31	_	0.51	
Mold Draft Angle Top	α	5°	_	15°	
Mold Draft Angle Bottom	β	5°	_	15°	

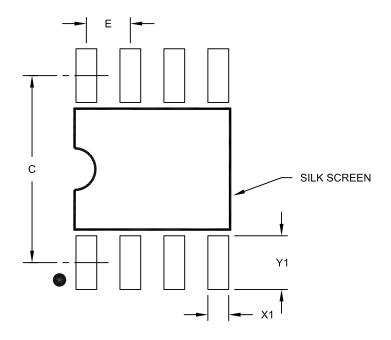
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch E		1.27 BSC		
Contact Pad Spacing	С		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

APPENDIX A: REVISION HISTORY

Revision A (03/2009)

Initial release of this document.

25LC640A

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- Product Support Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- General Technical Support Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- Business of Microchip Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- · Distributor or Representative
- · Local Sales Office
- Field Application Engineer (FAE)
- · Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

lo:	Technical Publications Manager	Total Pages Sent			
RE:	Reader Response				
Fron	m: Name				
A	Telephone: ()				
	lication (optional):				
Wou	uld you like a reply?YN				
Dev	ice: 25LC640A Lit	terature Number: DS22144A			
Que	estions:				
1.	What are the best features of this document?				
•					
2.	How does this document meet your har-	dware and software development needs?			
3.	Do you find the organization of this document easy to follow? If not, why?				
4.	What additions to the document do you think would enhance the structure and subject?				
5.	What deletions from the document could	d be made without affecting the overall usefulness?			
,					
6.	Is there any incorrect or misleading info	rmation (what and where)?			
7.	How would you improve this document?)			

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. Device		<u>X</u> e & Re	_ <u>X</u> <u>/XX</u> el Temp Range Package
Device:	25LC6	40A =	64k-bit, 2.5V, SPI Serial EEPROM
Tape & Reel:	Blank T	= =	Standard packaging Tape & Reel
Temperature Range:	М	=	-55°C to+125°C
Package:	SN	=	Plastic SOIC (3.90 mm body), 8-lead
•			

Examples:

- 25LC640A-M/SN = 64 Kbit, 2.5V Serial EEPROM, Extended temp., SOIC package 25LC640AT-M/SN = 64 Kbit, 2.5V Serial EEPROM, Extended temp., Tape and Reel, SOIC package

25LC640A

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the
 intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC, SmartShunt and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, nanoWatt XLP, PICkit, PICDEM, PICDEM.net, PICtail, PIC³² logo, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM

CERTIFIED BY DNV

ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277

http://support.microchip.com

Web Address: www.microchip.com

Technical Support:

Atlanta

Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455

Boston

Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088

Chicago Itasca. IL

Tel: 630-285-0071 Fax: 630-285-0075

Cleveland

Independence, OH Tel: 216-447-0464 Fax: 216-447-0643

Dallas

Addison, TX Tel: 972-818-7423 Fax: 972-818-2924

Detroit

Farmington Hills, MI Tel: 248-538-2250 Fax: 248-538-2260

Kokomo

Kokomo, IN Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608

Santa Clara

Santa Clara, CA Tel: 408-961-6444 Fax: 408-961-6445

Toronto

Mississauga, Ontario,

Canada

Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office

Suites 3707-14, 37th Floor Tower 6, The Gateway Harbour City, Kowloon Hong Kong

Tel: 852-2401-1200 Fax: 852-2401-3431

Australia - Sydney Tel: 61-2-9868-6733

Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8528-2100 Fax: 86-10-8528-2104

China - Chengdu Tel: 86-28-8665-5511 Fax: 86-28-8665-7889

China - Hong Kong SAR

Tel: 852-2401-1200 Fax: 852-2401-3431

China - Nanjing

Tel: 86-25-8473-2460 Fax: 86-25-8473-2470

China - Qingdao

Tel: 86-532-8502-7355 Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533 Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829 Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8203-2660 Fax: 86-755-8203-1760

China - Wuhan

Tel: 86-27-5980-5300 Fax: 86-27-5980-5118

China - Xiamen

Tel: 86-592-2388138 Fax: 86-592-2388130

China - Xian

Tel: 86-29-8833-7252 Fax: 86-29-8833-7256

China - Zhuhai

Tel: 86-756-3210040 Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore

Tel: 91-80-3090-4444 Fax: 91-80-3090-4080

India - New Delhi

Tel: 91-11-4160-8631 Fax: 91-11-4160-8632

India - Pune

Tel: 91-20-2566-1512 Fax: 91-20-2566-1513

Japan - Yokohama

Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea - Daegu

Tel: 82-53-744-4301 Fax: 82-53-744-4302

Korea - Seoul

Tel: 82-2-554-7200 Fax: 82-2-558-5932 or 82-2-558-5934

Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857 Fax: 60-3-6201-9859

Malaysia - Penang

Tel: 60-4-227-8870 Fax: 60-4-227-4068

Philippines - Manila

Tel: 63-2-634-9065 Fax: 63-2-634-9069

Singapore

Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-572-9526 Fax: 886-3-572-6459 Taiwan - Kaohsiung

Tel: 886-7-536-4818

Fax: 886-7-536-4803

Taiwan - Taipei

Tel: 886-2-2500-6610 Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351 Fax: 66-2-694-1350

EUROPE

Austria - Wels

Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen

Tel: 45-4450-2828 Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany - Munich

Tel: 49-89-627-144-0 Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611 Fax: 39-0331-466781

Netherlands - Drunen Tel: 31-416-690399

Fax: 31-416-690340 **Spain - Madrid**

Tel: 34-91-708-08-90 Fax: 34-91-708-08-91

UK - Wokingham Tel: 44-118-921-5869 Fax: 44-118-921-5820

02/04/09



OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный) Email: org@lifeelectronics.ru