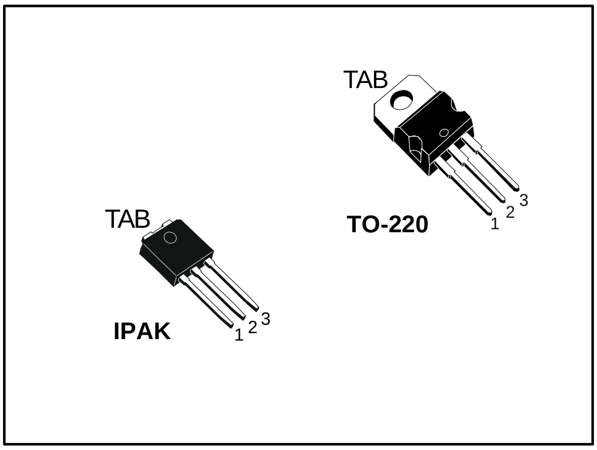
STP3LN80K5, STU3LN80K5

N-channel 800 V, 2.75 Ω typ., 2 A MDmesh™ K5 Power MOSFET in TO-220 and IPAK packages

Datasheet - production data



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STP3LN80K5	800 V	3.25 Ω	2 A
STU3LN80K5			

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFET are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Figure 1: Internal schematic diagram

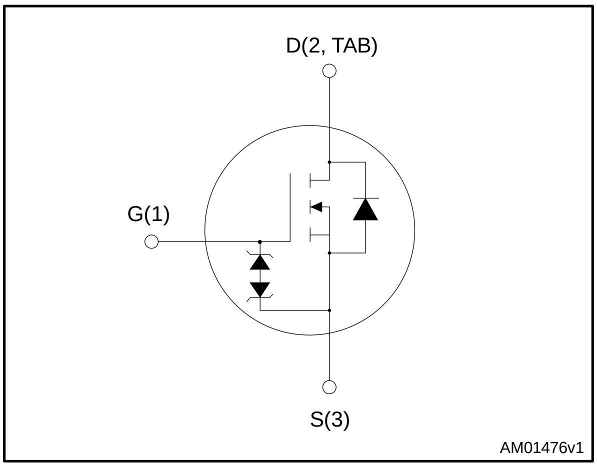


Table 1: Device summary

Order code	Marking	Package	Packing
STP3LN80K5	3LN80K5	TO-220	Tube
STU3LN80K5		IPAK	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	2	A
I_D	Drain current (continuous) at T_C = 100 °C	1.25	A
I_D (1)	Drain current (pulsed)	8	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 2 A, di/dt ≤ 100 A/μs; V_{DSpeak} < $V_{(BR)DSS}$, V_{DD} = 640 V.

(3)V_{DS} ≤ 640 V.

Table 3: Thermal data

Symbol	Parameter	Value		Unit
		TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case	2.78		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	100	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	0.7	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}; V_{DD} = 50 V)	155	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	800			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V, V_{GS} = 0 V			1	µA
		V_{DS} = 800 V, V_{GS} = 0 V, T_C = 125 °C[(1)]			50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ± 20 V, V_{GS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1 A		2.75	3.25	Ω

Notes:

[(1)]Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	102	-	pF
C_{oss}	Output capacitance		-	11	-	pF
C_{rss}	Reverse transfer capacitance		-	0.1	-	pF
C_{otr}[(1)]	Equivalent capacitance time related	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	20	-	pF
C_{oer}[(2)]	Equivalent capacitance energy related		-	7	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	12	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 2 A, V_{GS} = 10 V (see *Figure 17: "Test circuit for gate charge behavior"*)	-	2.63	-	nC
Q_{gs}	Gate-source charge		-	0.91	-	nC
Q_{gd}	Gate-drain charge		-	1.53	-	nC

Notes:

[(1)]Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

[(2)]Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 1 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16: "Test circuit for resistive load switching times"* and *Figure 21: "Switching time waveform"*)	-	6.2	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
t_f	Fall time		-	26	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2	A
I_{SDM}(1)	Source-drain current (pulsed)		-		8	A
V_{SD}(2)	Forward on voltage	I_{SD} = 2 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	210		ns
Q_{rr}	Reverse recovery charge		-	0.8		µC
I_{RRM}	Reverse recovery current		-	7.6		A
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C, (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	345		ns
Q_{rr}	Reverse recovery charge		-	1.2		µC
I_{RRM}	Reverse recovery current		-	7.2		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for TO-220

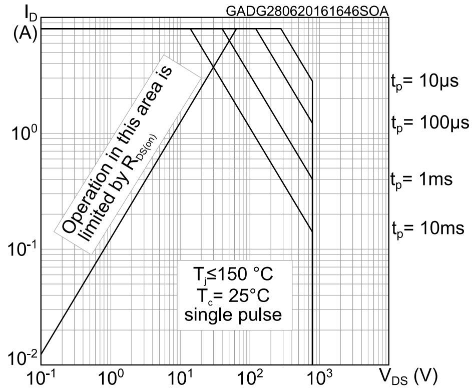


Figure 3: Thermal impedance for TO-220

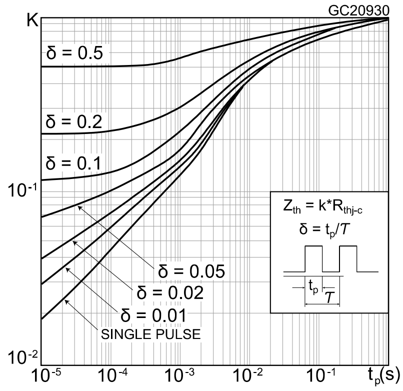


Figure 4: Safe operating area for IPAK

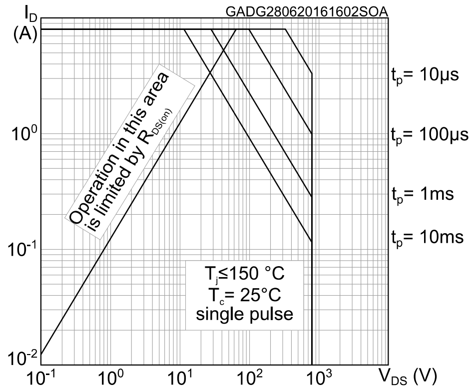


Figure 5: Thermal impedance for IPAK

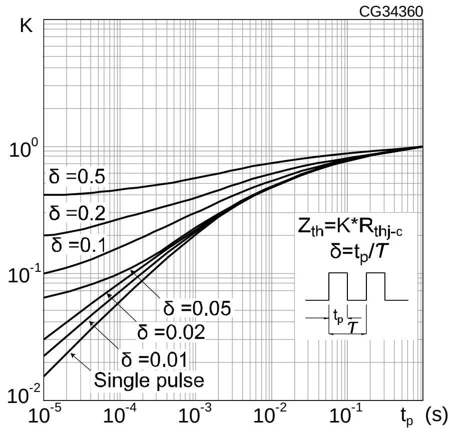


Figure 6: Output characteristics

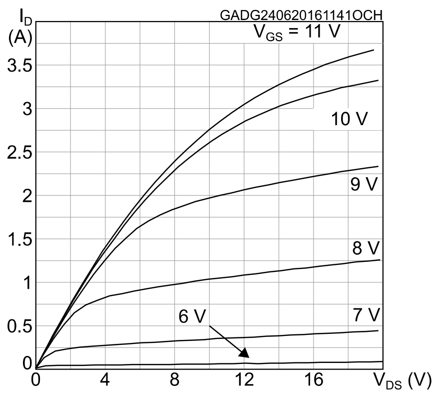


Figure 7: Transfer characteristics

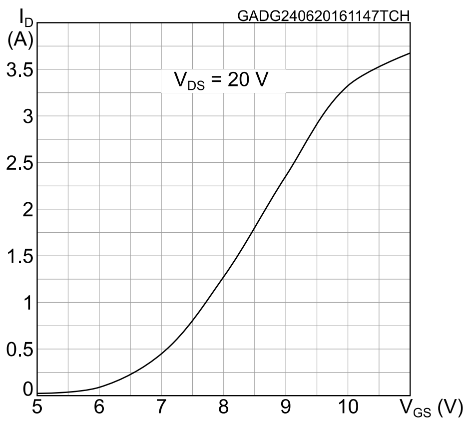


Figure 8: Gate charge vs gate-source voltage

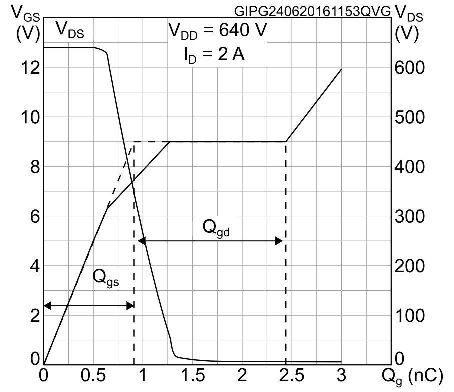


Figure 9: Static drain-source on-resistance

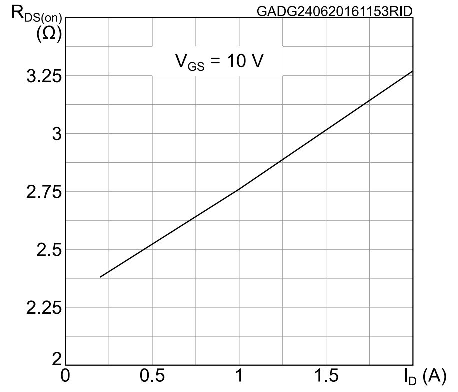


Figure 10: Capacitance variations

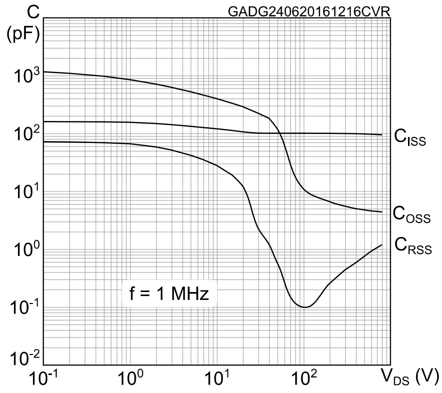


Figure 11: Source-drain diode forward characteristics

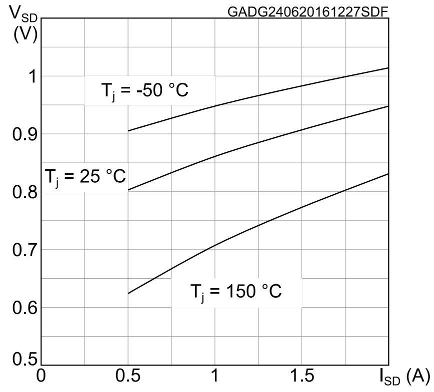


Figure 12: Normalized gate threshold voltage vs temperature

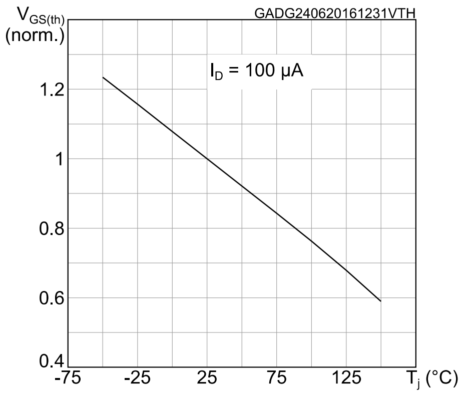


Figure 13: Normalized on-resistance vs temperature

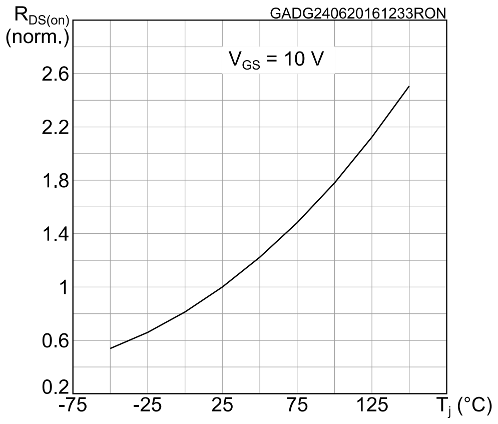


Figure 14: Normalized V(BR)DSS vs temperature

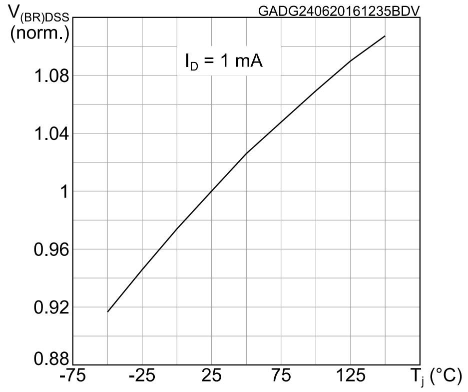
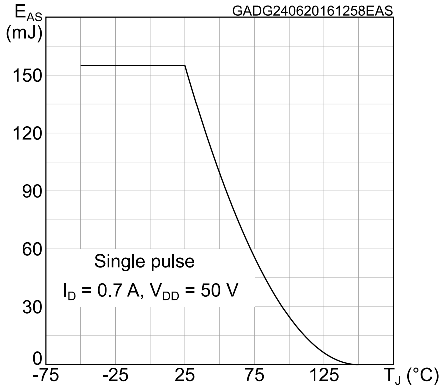


Figure 15: Maximum avalanche energy vs starting TJ



3 Test circuits

Figure 16: Test circuit for resistive load switching times

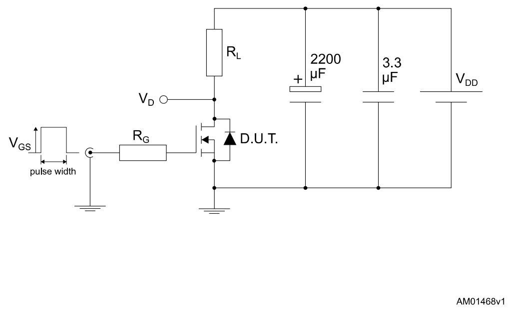


Figure 17: Test circuit for gate charge behavior

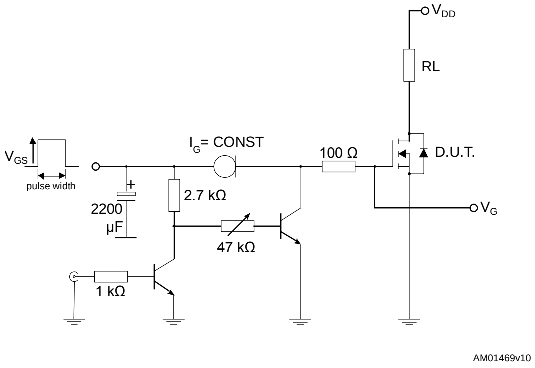


Figure 18: Test circuit for inductive load switching and diode recovery times

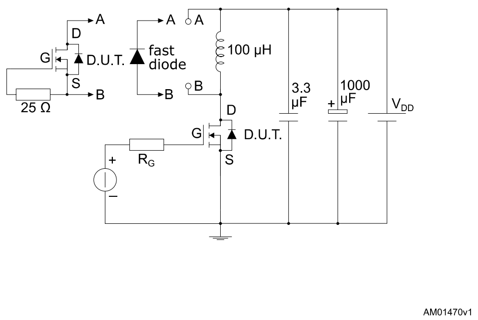


Figure 19: Unclamped inductive load test circuit

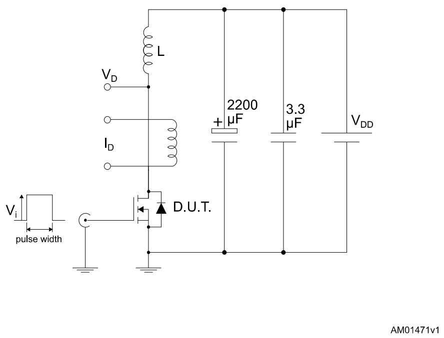


Figure 20: Unclamped inductive waveform

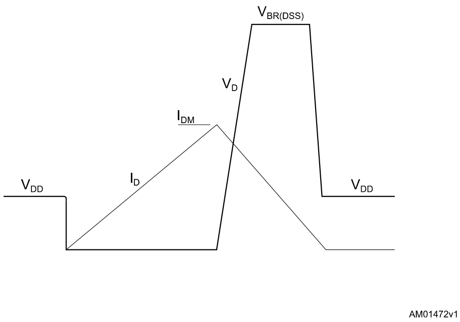
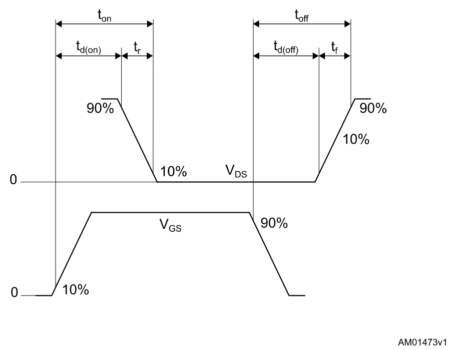


Figure 21: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 IPAK package information

Figure 22: IPAK (TO-251) type A package outline

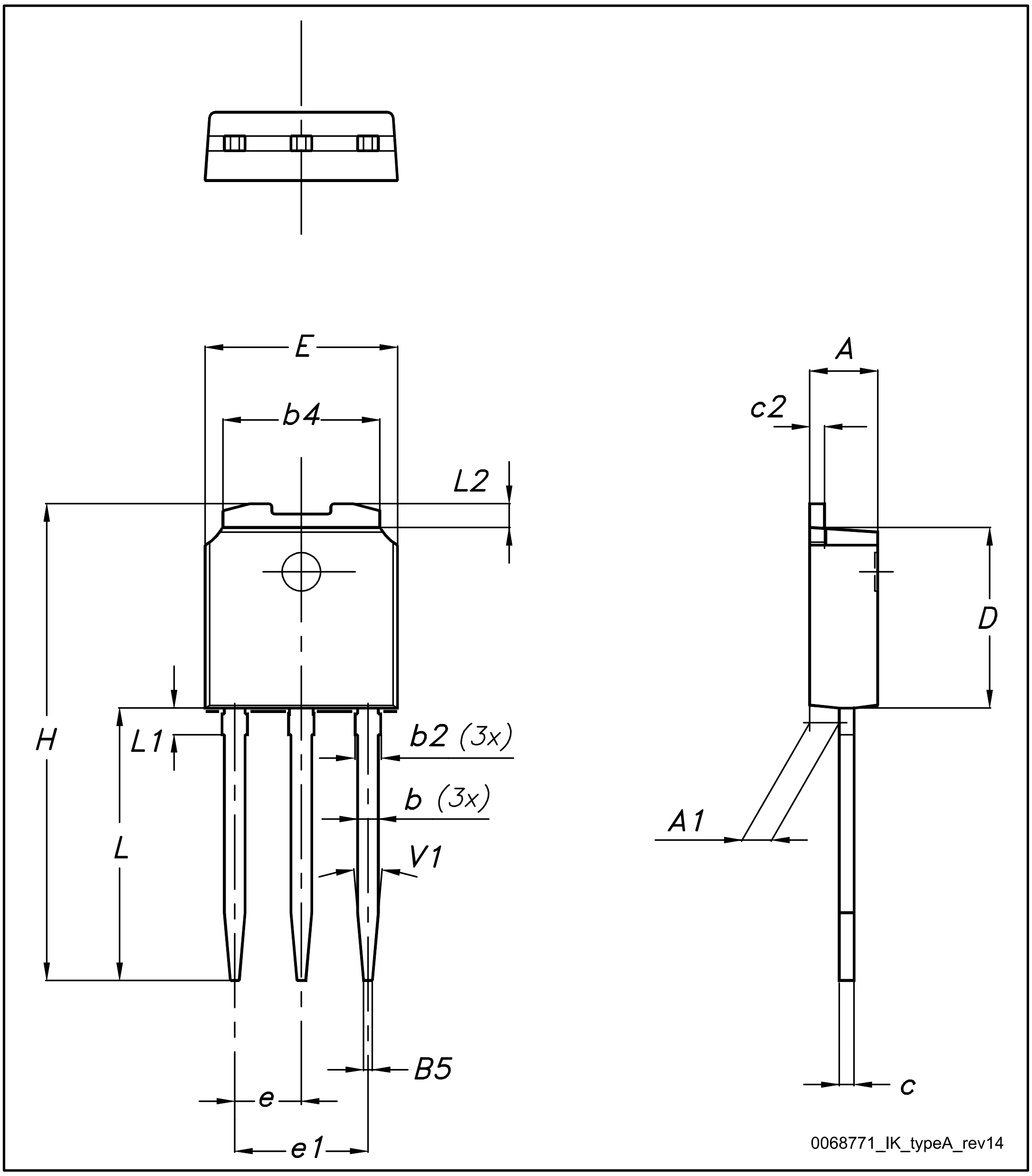


Table 10: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.2 TO-220 type A package information

Figure 23: TO-220 type A package outline

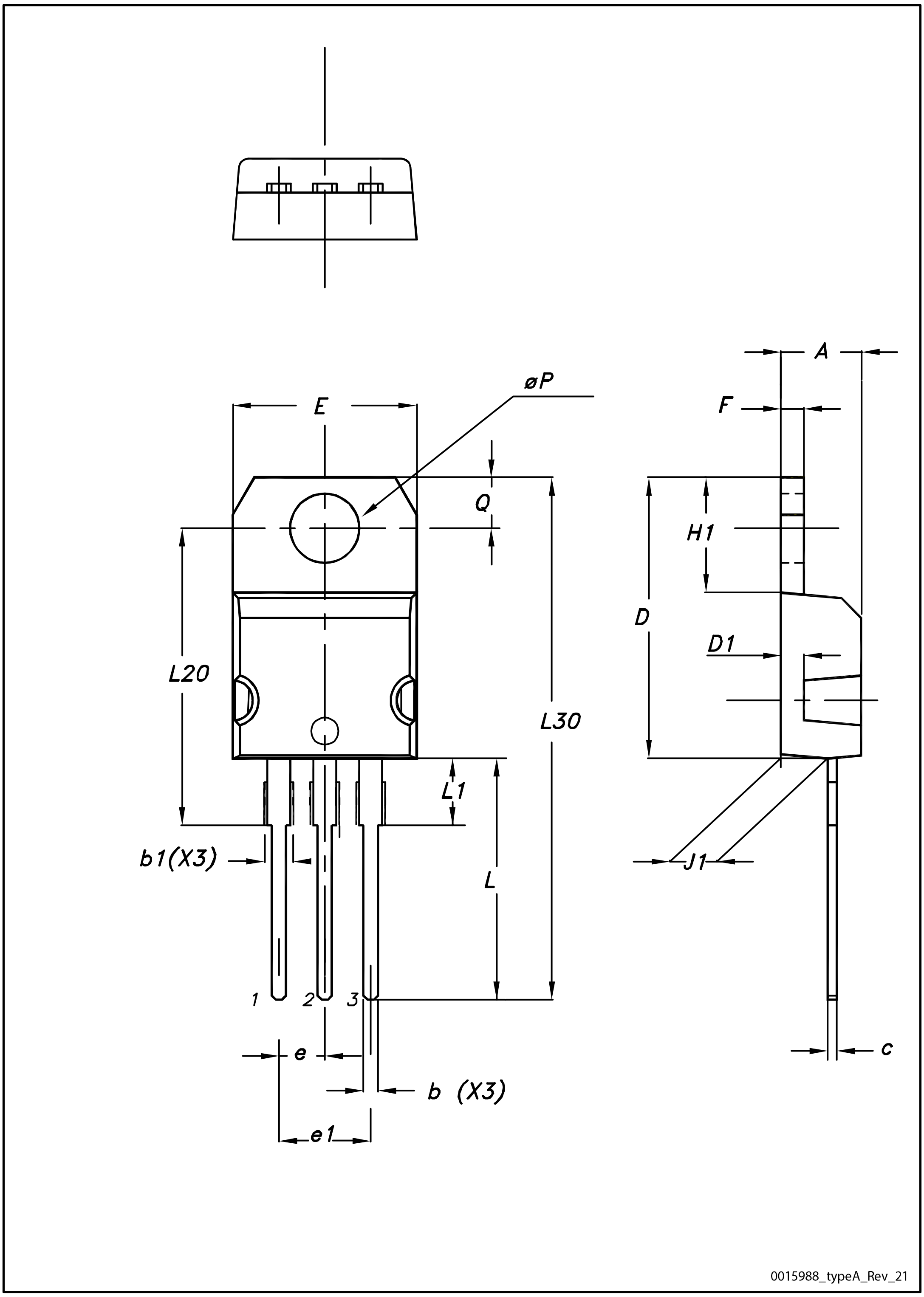


Table 11: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
09-Jul-2015	1	Initial release
28-Jun-2016	2	Updated title and features in cover page. Updated *Section 1: "Electrical ratings"*. Updated *Section 2: "Electrical characteristics"*. Added *Section 2.1: "Electrical characteristics (curves)"*. Document status promoted from preliminary to production data. Minor text changes.

LifeElectronics
Живое партнерство

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