74HC6323A; 74HCT6323A

Programmable ripple counter with oscillator; 3-state

Rev. 4 — 9 July 2018 **Product data sheet**

1 General description

The 74HC6323A; 74HCT6323A is an oscillator designed for quartz crystal combined with a programmable 3-state counter, a 3-state output buffer and an overriding asynchronous master reset ($\overline{MR}$). With the two select inputs S1 and S2 the counter can be switched in the divide-by-1, 2, 4 or 8 mode. If left floating the clock is divided by 8. The oscillator is designed to operate either in the fundamental or third overtone mode depending on the crystal and external components applied. On-chip capacitors minimize external component count for third overtone crystal applications. The oscillator may be replaced by an external clock signal at input X1. In this event the other oscillator pin (X2) must be floating. The counter advances on the negative-going transition of X1. A LOW level on $\overline{MR}$ resets the counter, stops the oscillator and sets the output buffer in the 3-state condition. $\overline{MR}$ can be left floating since an internal pull-up resistor will make the $\overline{MR}$ inactive.

The X1 input has CMOS input switching levels and may be driven by a TTL output using a pull-up resistor connected to V_{CC}. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Features and benefits

- Programmable 3-stage ripple counter
- Suitable for over-tone crystal application up to 50 MHz (V_{CC} = 5 V ± 10%)
- 3-state output buffer
- Two internal capacitors
- Recommended operating range for use with third overtone crystals 3 to 6 V
- Oscillator stop function ($\overline{MR}$)
- Input levels:
  - For 74HC6323: CMOS level
  - For 74HCT6323: TTL level
- ESD protection:
  - HBM JESD22-A114-A exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

nexperia

3 Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits
- CIO (Compact Integrated Oscillator)
- Third-overtone crystal operation

4 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC6323AD	-40 °C to +125 °C	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
74HCT6323AD				

5 Functional diagram

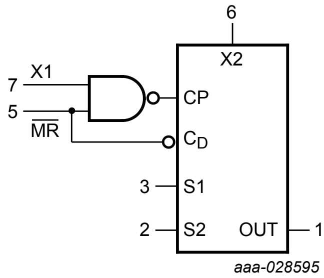


Figure 1. IEC logic symbol

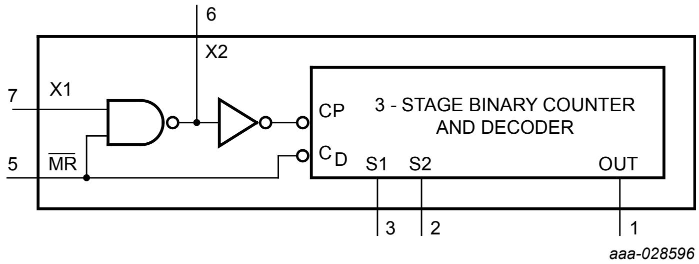
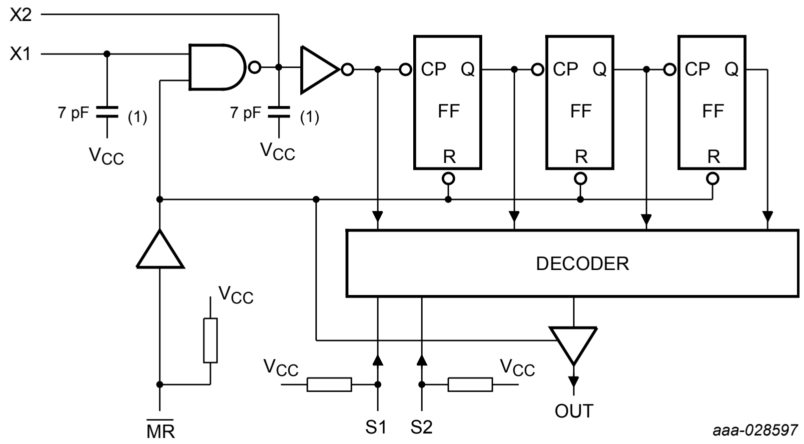


Figure 2. Functional diagram



(1) Internal capacitors typical 7 pF each.
Including stray capacitors on pin X1 and X2, total capacitance will be typical 12 pF per pin.

Figure 3. Logic diagram

6 Pinning information

6.1 Pinning

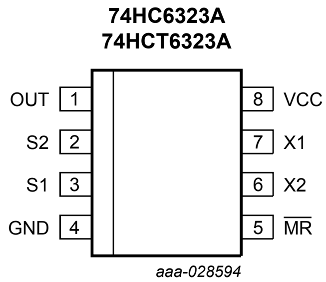


Figure 4. Pin configuration SOT96-1 (SO8)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OUT	1	counter output
S1, S2	3, 2	mode select inputs for divide by 1, 2, 4 or 8
GND	4	ground (0 V)
$\overline{MR}$	5	master reset input (active LOW)
X2	6	oscillator pin
X1	7	clock input /oscillator pin
V_{CC}	8	supply voltage

7 Functional description

Table 3.

Inputs		Outputs
S1	**S2**	**OUT**
0	0	f_i
0	1	$f_i/2$
1	0	$f_i/4$
1	1	$f_i/8$

8 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	-	±20	mA
I_O	output current	OUT output; -0.5 V < V_O < V_{CC} + 0.5 V	-	±35	mA
I_{CC}	supply current	OUT output	-	70	mA
I_{GND}	ground current	OUT output	-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [1]	-	500	mW

[1] P_{tot} derates linearly with 8 mW/K above 70 °C.

9 Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC6323A			74HCT6323A			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC6323A										
V_{IH}	HIGH-level input voltage	$\overline{MR}$, X1, S1, S2 input								
		V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$\overline{MR}$, X1, S1, S2 input								
		V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	X2 output								
		V_{CC} = 4.5 V; X1 = GND; $\overline{MR}$ = V_{CC}; I_O = -2.6 mA	3.98	-	-	3.84	-	3.7	-	V
		V_{CC} = 6.0 V; X1 = GND; $\overline{MR}$ = V_{CC}; I_O = -3.3 mA	5.48	-	-	5.34	-	5.2	-	V
		V_{CC} = 4.5 V; X1 = V_{CC}; $\overline{MR}$ = GND; I_O = -2.6 mA	3.98	-	-	3.84	-	3.7	-	V
		V_{CC} = 6.0 V; X1 = V_{CC}; $\overline{MR}$ = GND; I_O = -3.3 mA	5.48	-	-	5.34	-	5.2	-	V
		V_{CC} = 2.0 V; X1 = GND; $\overline{MR}$ = V_{CC}; I_O = -20 μA	1.9	2.0	-	1.9	-	1.9	-	V
		V_{CC} = 4.5 V; X1 = GND; $\overline{MR}$ = V_{CC}; I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		V_{CC} = 6.0 V; X1 = GND; $\overline{MR}$ = V_{CC}; I_O = -20 μA	5.9	6.0	-	5.9	-	5.9	-	V
		V_{CC} = 2.0 V; X1 = V_{CC}; $\overline{MR}$ = GND; I_O = -20 μA	1.9	2.0	-	1.9	-	1.9	-	V
		V_{CC} = 4.5 V; X1 = V_{CC}; $\overline{MR}$ = GND; I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		V_{CC} = 6.0 V; X1 = V_{CC}; $\overline{MR}$ = GND; I_O = -20 μA	5.9	6.0	-	5.9	-	5.9	-	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	OUT output; $V_I = V_{IH}$ or V_{IL}								
		V_{CC} = 2.0 V; I_O = -20 μA	1.9	2.0	-	1.9	-	1.9	-	V
		V_{CC} = 4.5 V; I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		V_{CC} = 6.0 V; I_O = -20 μA	5.9	6.0	-	5.9	-	5.9	-	V
		V_{CC} = 4.5 V; I_O = -6 mA	3.98	-	-	3.84	-	3.7	-	V
		V_{CC} = 6.0 V; I_O = -7.8 mA	5.48	-	-	5.34	-	5.2	-	V
V_{OL}	LOW level output voltage	X2 output								
		V_{CC} = 4.5 V; X1 = V_{CC}; $\overline{MR}$ = V_{CC}; I_O = 2.6 mA	-	-	0.26	-	0.33	-	0.4	V
		V_{CC} = 6.0 V; X1 = V_{CC}; $\overline{MR}$ = V_{CC}; I_O = 3.3 mA	-	-	0.26	-	0.33	-	0.4	V
		V_{CC} = 2.0 V; X1 = V_{CC}; $\overline{MR}$ = V_{CC}; I_O = 20 μA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 4.5 V; X1 = V_{CC}; $\overline{MR}$ = V_{CC}; I_O = 20 μA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 6.0 V; X1 = V_{CC}; $\overline{MR}$ = V_{CC}; I_O = 20 μA	-	0.0	0.1	-	0.1	-	0.1	V
V_{OL}	LOW level output voltage	OUT output; $V_I = V_{IH}$ or V_{IL}								
		V_{CC} = 2.0 V; I_O = 20 μA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 4.5 V; I_O = 20 μA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 6.0 V; I_O = 20 μA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 4.5 V; I_O = 6 mA	-	-	0.26	-	0.33	-	0.4	V
		V_{CC} = 6.0 V; I_O = 7.8 mA	-	-	0.26	-	0.33	-	0.4	V
I_I	input leakage current	X1 input; V_{CC} = 6.0 V; $\overline{MR}$ = V_{CC}; S1 = V_{CC}; S2 = V_{CC}	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{pu}	pull-up current	$\overline{MR}$, S1 and S2 inputs; V_{CC} = 6.0 V; V_I = GND; see Figure 13 and Figure 14.	-5	-30	-100	-	-	-	-	μA
I_{CC}	supply current	V_{CC} = 6.0 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	8	-	80	-	160	μA
C_I	input capacitance	$\overline{MR}$, S1 and S2 inputs	-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT6323A										
V_{IH}	HIGH-level input voltage	$\overline{MR}$, S1 and S2 inputs; V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
		X1 input								
		V_{CC} = 4.5 V	3.15	-	-	3.15	-	3.15	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	$\overline{MR}$, S1 and S2 inputs; V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
		X1 input								
		V_{CC} = 4.5 V	-	-	1.35	-	1.35	-	1.35	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	X2 output; V_{CC} = 4.5 V								
		X1 = GND; $\overline{MR}$ = V_{CC}; I_O = -2.6 mA	3.98	-	-	3.84	-	3.7	-	V
		X1 = V_{CC}; $\overline{MR}$ = GND; I_O = -2.6 mA	3.98	-	-	3.84	-	3.7	-	V
		X1 = GND; $\overline{MR}$ = V_{CC}; I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		X1 = V_{CC}; $\overline{MR}$ = GND; I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		OUT output; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}								
		I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -6 mA	3.98	-	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	X2 output; V_{CC} = 4.5 V; X1 = V_{CC}; $\overline{MR}$ = V_{CC}								
		I_O = 2.6 mA	-	-	0.26	-	0.33	-	0.4	V
		I_O = 20 μA	-	0.0	0.1	-	0.1	-	0.1	V
		OUT output; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}								
		I_O = 20 μA	-	0.0	0.1	-	0.1	-	0.1	V
		I_O = 6 mA	-	-	0.26	-	0.33	-	0.4	V
I_I	input leakage current	X1 input; V_{CC} = 5.5 V; $\overline{MR}$ = V_{CC}; S1 = V_{CC}; S2 = V_{CC}	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{pu}	pull-up current	$\overline{MR}$, S1 and S2 inputs; V_{CC} = 5.5 V; V_I = GND; see Figure 13 and Figure 14.	-5	-25	-100	-	-	-	-	μA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	8	-	80	-	160	μA
ΔI_{CC}	additional supply current	$\overline{MR}$, S1 and S2 inputs; V_{CC} = 5.5 V; V_I = V_{CC} or GND; other inputs at V_{CC} or GND; I_O = 0 A	-	40	144	-	180	-	196	μA
C_I	input capacitance	$\overline{MR}$, S1 and S2 inputs	-	3.5	-	-	-	-	-	pF

11 Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC6323A										
t_{pd}	propagation delay	X1 to OUT divide by 1; S1 = GND; S2 = GND; see Figure 5 [1]								
		V_{CC} = 2.0 V	-	61	185	-	230	-	275	ns
		V_{CC} = 4.5 V	-	22	37	-	46	-	55	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	19	31	-	39	-	47	ns
		X1 to OUT divide by 2; S1 = GND; S2 = V_{CC}; see Figure 5								
		V_{CC} = 2.0 V	-	74	235	-	290	-	350	ns
		V_{CC} = 4.5 V	-	27	47	-	58	-	70	ns
		V_{CC} = 6.0 V	-	23	40	-	49	-	60	ns
		X1 to OUT divide by 4; S1 = V_{CC}; S2 = GND; see Figure 5								
		V_{CC} = 2.0 V	-	91	285	-	355	-	425	ns
		V_{CC} = 4.5 V	-	33	57	-	71	-	85	ns
		V_{CC} = 6.0 V	-	28	48	-	60	-	72	ns
		X1 to OUT divide by 8; S1 = V_{CC}; S2 = V_{CC}; see Figure 5								
		V_{CC} = 2.0 V	-	105	335	-	415	-	500	ns
		V_{CC} = 4.5 V	-	38	67	-	83	-	100	ns
		V_{CC} = 6.0 V	-	32	57	-	71	-	85	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{MR}$ to OUT; see Figure 6								
		V_{CC} = 2.0 V	-	36	150	-	185	-	225	ns
		V_{CC} = 4.5 V	-	13	30	-	37	-	45	ns
		V_{CC} = 6.0 V	-	11	26	-	31	-	38	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{MR}$ to OUT; see Figure 6 [2]								
		V_{CC} = 2.0 V	-	61	200	-	250	-	300	ns
		V_{CC} = 4.5 V	-	22	40	-	50	-	60	ns
		V_{CC} = 6.0 V	-	19	34	-	43	-	51	ns
t_{dis}	disable time	$\overline{MR}$ to OUT; see Figure 6 [3]								
		V_{CC} = 2.0 V	-	75	150	-	185	-	225	ns
		V_{CC} = 4.5 V	-	15	30	-	37	-	45	ns
		V_{CC} = 6.0 V	-	13	26	-	31	-	38	ns

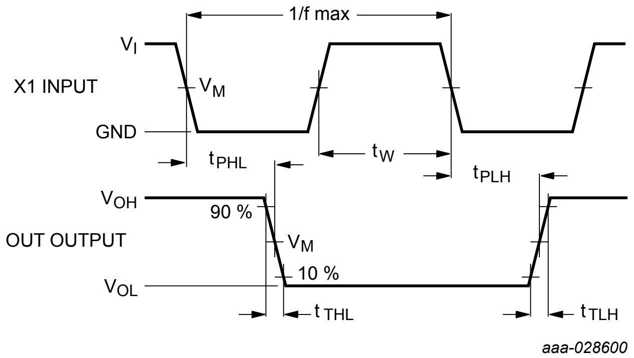
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_t	transition time	OUT; see Figure 5 [4]								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	19	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns
t_W	pulse width	X1 HIGH or LOW; see Figure 5								
		V_{CC} = 2.0 V	50	17	-	60	-	75	-	ns
		V_{CC} = 4.5 V	10	6	-	12	-	15	-	ns
		V_{CC} = 6.0 V	9	5	-	10	-	13	-	ns
		$\overline{MR}$ LOW; see Figure 7								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	7	-	17	-	20	-	ns
t_{rec}	recovery time	$\overline{MR}$ to X1; see Figure 7								
		V_{CC} = 2.0 V	100	19	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
f_{max}	maximum frequency	X1; see Figure 5								
		V_{CC} = 2.0 V	10	17	-	8	-	6.6	-	MHz
		V_{CC} = 4.5 V	50	85	-	40	-	33	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	90	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	59	100	-	47	-	39	-	MHz
C_{PD}	power dissipation capacitance	An external clock is applied to X1 with: $t_r = t_f \leq 6$ ns, V_I = GND to V_{CC}, $\overline{MR}$ = HIGH [5]								
		divide by 1; S1 = GND; S2 = GND	-	54	-	-	-	-	-	pF
		divide by 2; S1 = GND; S2 = V_{CC}	-	42	-	-	-	-	-	pF
		divide by 4; S1 = V_{CC}; S2 = GND	-	36	-	-	-	-	-	pF
		divide by 8; S1 = V_{CC}; S2 = V_{CC}	-	33	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT6323A										
t_{pd}	propagation delay	X1 to OUT divide by 1; S1 = GND; S2 = GND; see Figure 5 [1]								
		V_{CC} = 4..5 V	-	24	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		X1 to OUT divide by 2; S1 = GND; S2 = V_{CC}; see Figure 5								
		V_{CC} = 4.5 V	-	29	50	-	62	-	75	ns
		X1 to OUT divide by 4; S1 = V_{CC}; S2 = GND; see Figure 5								
		V_{CC} = 4.5 V	-	35	60	-	75	-	90	ns
		X1 to OUT divide by 8; S1 = V_{CC}; S2 = V_{CC}; see Figure 5								
		V_{CC} = 4.5 V	-	40	70	-	87	-	105	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{MR}$ to OUT; see Figure 6								
		V_{CC} = 4.5 V	-	16	30	-	37	-	45	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{MR}$ to OUT; see Figure 6 [2]								
		V_{CC} = 4.5 V	-	22	38	-	47	-	57	ns
t_{dis}	disable time	$\overline{MR}$ to OUT; see Figure 6 [3]								
		V_{CC} = 4.5 V	-	21	35	-	43	-	52	ns
t_t	transition time	OUT; see Figure 5 [4]								
		V_{CC} = 4.5 V	-	5	12	-	15	-	19	ns
t_W	pulse width	X1 HIGH or LOW; see Figure 5								
		V_{CC} = 4.5 V	10	6	-	12	-	15	-	ns
		$\overline{MR}$ LOW; see Figure 7								
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
t_{rec}	recovery time	$\overline{MR}$ to X1; see Figure 7								
		V_{CC} = 4.5 V	24	12	-	30	-	36	-	ns
f_{max}	maximum frequency	X1; see Figure 5								
		V_{CC} = 4.5 V	50	85	-	40	-	33	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	90	-	-	-	-	-	MHz

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	An external clock is applied to X1 with: $t_r = t_f \leq 6$ ns, V_i = GND to V_{CC}, $\overline{MR}$ = HIGH [5]								
		divide by 1; S1 = GND; S2 = GND	-	54	-	-	-	-	-	pF
		divide by 2; S1 = GND; S2 = V_{CC}	-	42	-	-	-	-	-	pF
		divide by 4; S1 = V_{CC}; S2 = GND	-	36	-	-	-	-	-	pF
		divide by 8; S1 = V_{CC}; S2 = V_{CC}	-	33	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{PZH} only applicable in the divide-by-1 mode and X1 must be HIGH.
[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[4] t_t is the same as t_{THL} and t_{TLH}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o) + (I_{pull\text{-}up} \times V_{CC})$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
$I_{pull\text{-}up}$ = pull-up currents in μA.
$I_{pull\text{-}up}$ is the summation of $-I_I$ (μA) of S1 and S2 inputs at the LOW state.

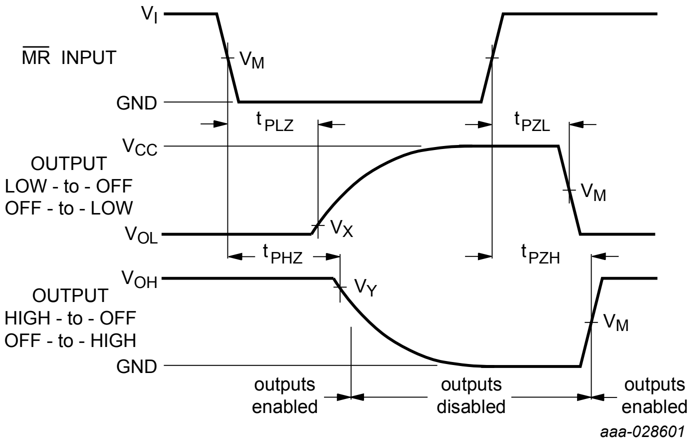
11.1 Waveforms and test circuit



Measurement points are given in Table 8

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

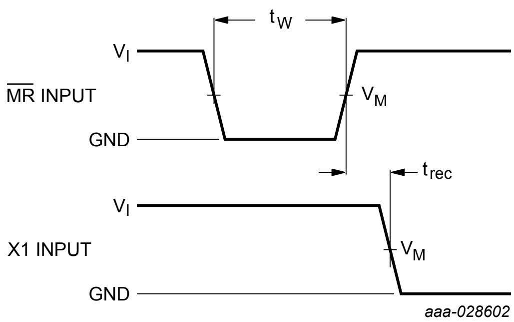
Figure 5. The clock (X1) to output (OUT) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.



Measurement points are given in Table 8

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. The input $\overline{MR}$ to output OUT, 3-state enable and disable times



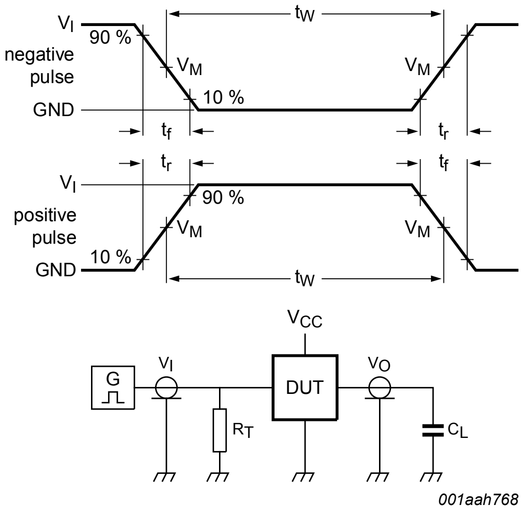
Measurement points are given in Table 8

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 7. The $\overline{MR}$ minimum pulse width and $\overline{MR}$ to X1 recovery time.

Table 8. Measurement points

Type	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
74HC6323A	GND to V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	0.1 x V_{CC}	0.9 x V_{CC}
74HCT6323A	GND to 3 V	1.3 V	1.3 V	0.1 x V_{CC}	0.9 x V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Figure 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC6323A	GND to V_{CC}	6 ns	15 pF, 50 pF
74HCT6323A	GND to 3 V	6 ns	15 pF, 50 pF

12 Application information

12.1 Typical Crystal Oscillator

In Figure 9, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

The oscillator has been designed to operate over a wide frequency spectrum, for quartz crystals operating in the fundamental mode and in the overtone mode. The circuit is a Pierce type oscillator and requires a minimum of external components. There are two on-chip capacitors, X1 and X2, of approximately 7 pF. Together with the stray and input capacitance the value becomes 12 pF for 8-pin SO packages. These values are convenient and make it possible to run the oscillator in the third overtone without external capacitors applied. If a certain frequency is chosen, the IC parameters, as forward transconductance, and the crystal parameters such as the motional resistances R1 (fundamental), R3 (third overtone) and R5 (fifth overtone), are of paramount importance. Also the values of the external components as R_s (series resistance) and the crystal load capacitances play an important role. Especially in overtone mode oscillations, R_b (bias resistance) and the load capacitance values are very important.

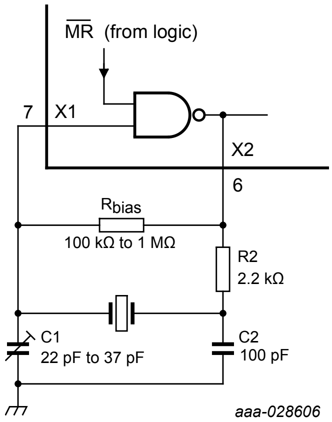
12.2 Considerations for Fundamental Oscillator:

In the fundamental oscillator mode, the R_b has only the function of biasing the inverter stage, so that it operates as an amplifier with a phase shift of approximately 180°. The value must be high, i.e. 100 kΩ up to 10 MΩ. The load capacitors C1 and C2, must have a value that is suitable for the crystal being used. The crystal is designed for a certain frequency having a specific load capacitance. C1 can be used to trim the oscillation frequency. The series resistance reduces the total loop gain. One function of it is therefore to reduce the power dissipation in the crystal. R_s also suppresses overtone oscillations and introduces a phase shift over a broad frequency range. This is of less concern provided R_s is not too high a value.

Note: A combination of a small load capacitor value and a small series resistance, may cause a third overtone oscillation.

12.3 Considerations for Third-overtone Oscillator:

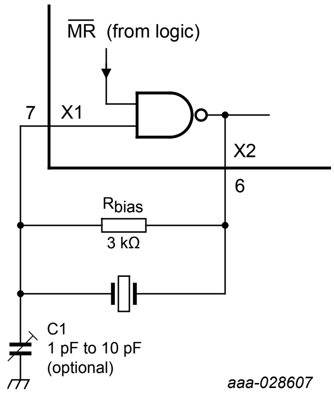
In the overtone configuration, series resistance is no longer applied. This is essential otherwise the gain for third overtone can be too small for oscillation. A simple solution to suppress the fundamental oscillation, is to spoil the crystal fundamental activity. By dramatically reducing the value of the bias resistor of the inverting stage, and applying small load capacitors, it is possible to have an insufficient phase in the total loop for fundamental oscillation. However the phase for third overtone is good. It can be explained by the $R_b \times C_l$ time constant. During oscillation the crystal with the load capacitors cause a phase shift of 180°. Because R_b is parallel with the crystal (no R_s), R_b spoils the phase for fundamental. $R_b \times C_l$ must be of a value, that it is not spoiling the phase for third overtone too much. Because third overtone is a 3 times higher frequency than the fundamental, the $R_b \times C_l$ cannot 'maintain' the higher third overtone frequency, which results in a less spoiled overtone phase.



Above 5 MHz replace R2 by a capacitor of half the value of C2.

C_L at which a crystal is specified (or adjusted) equals for this application C1 x C2/(C1 + C2)

Figure 9. Typical setup for a crystal oscillator operating in the fundamental mode (1 MHz to 25 MHz)

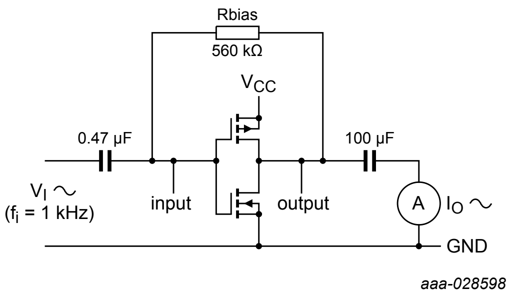


Applicable for third overtone crystals (lower damping resistance at the third harmonic frequency) at typical 50 MHz. For lower frequencies extra load capacitors must be supplied, or increase bias resistor.

Figure 10. Typical set-up for a crystal oscillator operating in the third overtone mode without the use of an inductor

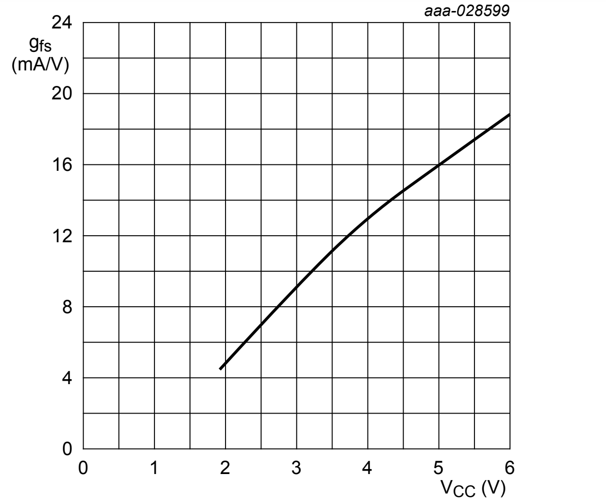
Table 10. Typical application values

Fundamental mode					Third overtone mode		
f (MHz)	R2 (kΩ)	C1 (pF)	C2 (pF)		f (MHz)	R_{bias} (kΩ)	C1 (pF)
1	4.7	47 to 68			50	3.0	4.7
10	2.2	47 to 68					
25	1	33	33				



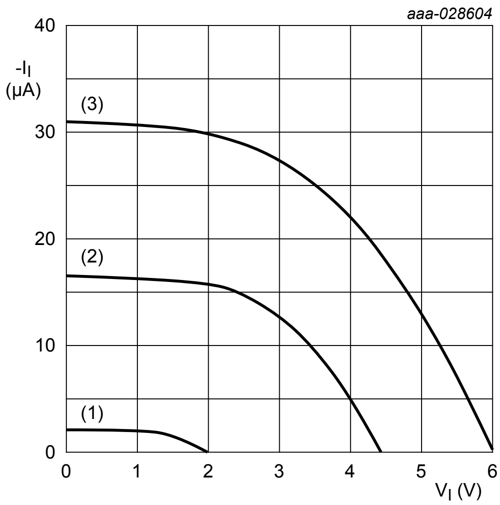
$g_{fs} = \Delta I_O / \Delta V_I$ at v_O is constant (see Figure 12) and $\overline{MR}$ = HIGH.

Figure 11. Test set-up for measuring forward transconductance



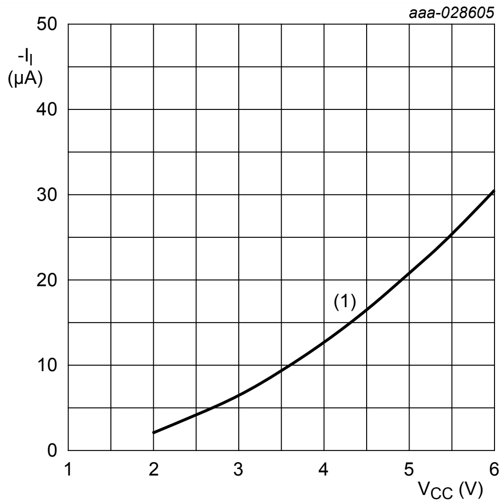
g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

Figure 12. Typical forward transconductance



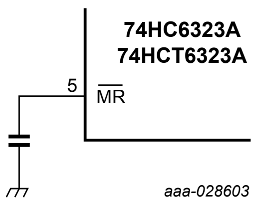
(1) V_{CC} = 2 V
(2) V_{CC} = 4.3 V
(3) V_{CC} = 6 V

Figure 13. Typical input pull-up current as a function of the input voltage



(1) V_I = 0 V

Figure 14. Typical input pull-up current as a function of the supply voltage (V_{CC})

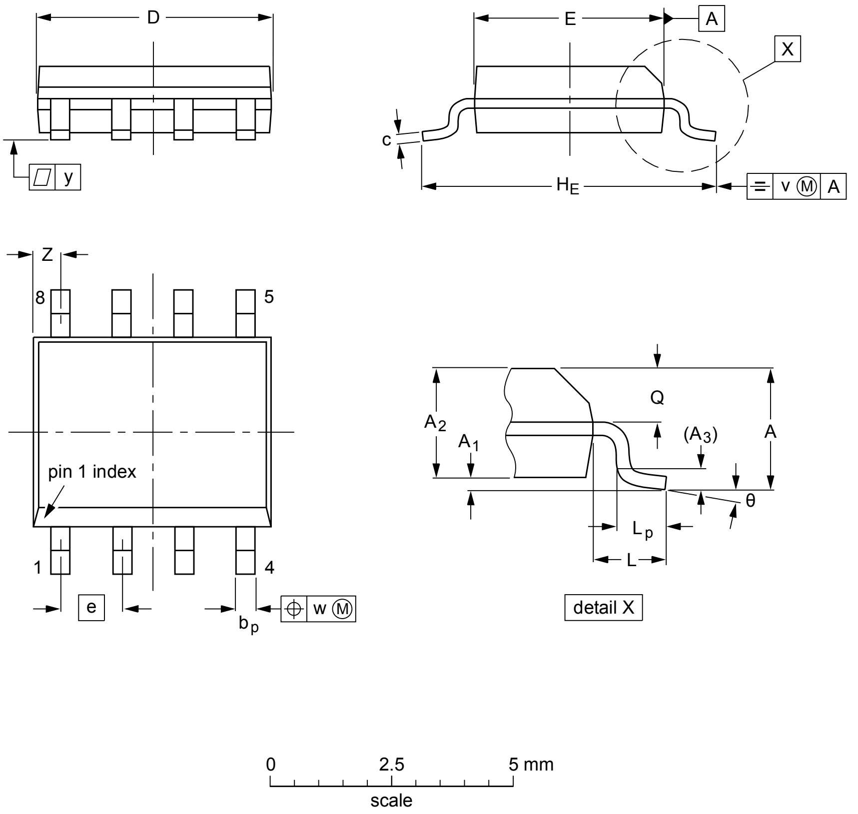


The input pull-up current is used to create a power-on delay time at $\overline{MR}$.

Figure 15. Power-on reset

13 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 16. Package outline SOT96-1 (SO8)

14 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT6323A v.4	20180709	Product data sheet	-	74HC_HCT6323A v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT6323A v.3	19930901	Product specification	-	74HC_HCT6323A v.2
74HC_HCT6323A v.2	19901201	Product specification	-	74HC_HCT6323A v.1

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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