

Operational Amplifiers / Comparators



Ground Sense Low Voltage Operation CMOS Operational Amplifiers

BU7461G, BU7461SG, BU7441G, BU7441SG, BU7462F/FVM/NUX, BU7462SF/FVM/NUX,
 BU7442F/FVM/NUX, BU7442SF/FVM/NUX, BU7464F, BU7464SF, BU7444F, BU7444SF,
 BU7465HFV, BU7465SHFV, BU7445HFV, BU7445SHFV

No.10049JET21

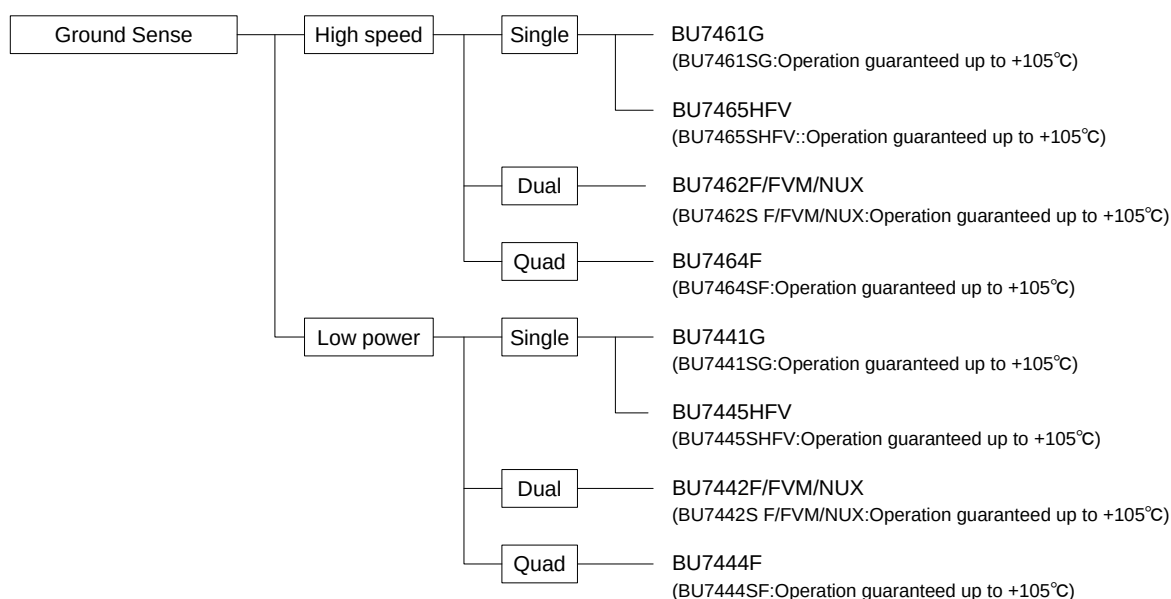
●Description

Low Voltage CMOS Op-Amp integrates one or two independent outputs full swing Op-Amps and phase compensation capacitors on a single chip. Especially, this series is operable with low voltage, low supply current and low input bias current.

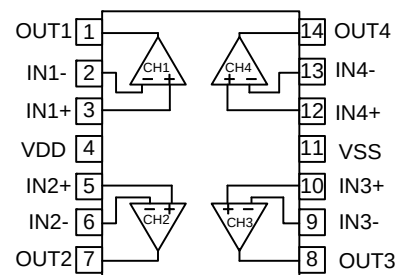
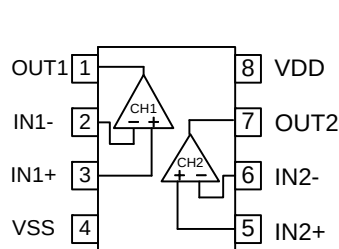
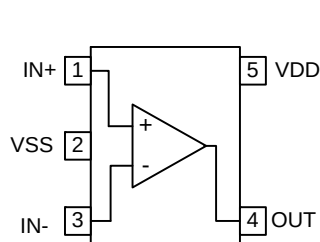
Ground Sense : BU7461 (BU7461S) family, BU7441 (BU7441S) family, BU7462 (BU7462S) family,
 BU7442 (BU7442S) family, BU7464 (BU7464S) family, BU7444 (BU7444S) family,
 BU7465 (BU7465S) family, BU7445 (BU7445S) family,

●Features

- | | |
|---|---|
| 1) Operable with low voltage
+1.7[V] ~ +5.5[V] (Single supply) :
BU7461/BU7441 family, BU7462/BU7442 family
BU7464/BU7444 family, BU7465/BU7445 family
2) Input Ground Sense, Output Full Swing
3) High speed operation (BU7461 family, BU7462 family)
4) Internal phase compensation
5) Wide temperature range
-40[°C] ~ +85[°C]
(BU7461G, BU7462 family, BU7464F, BU7465HFV)
(BU7441G, BU7442 family, BU7444F, BU7445HFV)
-40[°C] ~ +105[°C]
(BU7461SG, BU7462S family, BU7464SF, BU7465SHFV)
(BU7441SG, BU7442S family, BU7444SF, BU7445SHFV) | 6) High open loop voltage gain
7) Low supply current
(BU7441 family, BU7442 family)
(BU7445 family, BU7444 family)
8) Low input bias current 1[pA](Typ.)
9) ESD protection circuit
Human body mode (HBM) ±4000[V](Typ.) |
|---|---|



●Pin Assignments



SSOP5

HVSOF5

SOP8

MSOP8

VSON008X2030

SOP14

Input type	Package					
	SSOP5	HVSOF5	SOP8	VSON008X2030	MSOP8	SOP14
Ground Sense	BU7461G BU7461SG BU7441G BU7441SG	BU7465HFV BU7465SHFV BU7445HFV BU7445SHFV	BU7462F BU7462SF BU7442F BU7442SF	BU7462NUX BU7462SNUX BU7442NUX BU7442SNUX	BU7462FVM BU7462SFVM BU7442FVM BU7442SFVM	BU7464F BU7464SF BU7444F BU7444SF

●Absolute maximum rating (Ta=25[°C])

Parameter	Symbol	Rating		Unit
		BU7461G, BU7462F/FVM/NUX BU7441G, BU7442F/FVM/NUX BU7464F, BU7444F BU7445HFV, BU7465HFV	BU7461SG, BU7462S F/FVM/NUX BU7441SG, BU7442S F/FVM/NUX BU7464SF, BU7444SF BU7445SHFV, BU7465SHFV	
Supply Voltage	VDD-VSS	+7		V
Differential Input Voltage ^(*1)	Vid	VDD-VSS		V
Input Common-mode Voltage Range	Vicm	(VSS-0.3) ~ (VDD+0.3)		V
Operating Temperature	Topr	-40 ~ +85	-40 ~ +105	°C
Storage Temperature	Tstg	-55 ~ +125		°C
Maximum Junction Temperature	Tjmax	+125		°C

Note: Absolute maximum rating item indicates the condition which must not be exceeded.

Application of voltage in excess of absolute maximum rating or use out absolute maximum rated temperature environment may cause deterioration of characteristics.

(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input terminal voltage is set to more than VSS.

●Electrical characteristics

OBU7461 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7461G, BU7461SG				
			Min.	Typ.	Max.		
Input Offset Voltage ^(*)2)	Vio	25°C	-	1	6	mV	—
Input Offset Current ^(*)2)	Iio	25°C	-	1	-	pA	—
Input Bias Current ^(*)2)	Ib	25°C	-	1	-	pA	—
Supply Current ^(*)3)	IDD	25°C	-	150	350	μA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	-	-	450		
High Level Output Voltage	VOH	25°C	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	—
Output Source Current ^(*)4)	IOH	25°C	4	8	-	mA	VDD-0.4[V]
Output Sink Current ^(*)4)	IOL	25°C	6	12	-	mA	VSS+0.4[V]
Slew Rate	SR	25°C	-	1.0	-	V/μs	CL=25[pF]
Gain Band width	FT	25°C	-	1	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	-	50	-	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	-	0.05	-	%	VOUT=1[Vp-p] f=1[kHz]

(*2) Absolute value

(*3) Full range: BU7461: Ta=-40[°C] to +85[°C] BU7461S: Ta=-40[°C] to +105[°C]

(*4) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7462 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7462F/FVM/NUX BU7462S F/FVM/NUX				
			Min.	Typ.	Max.		
Input Offset Voltage ^(*5)	Vio	25°C	-	1	6	mV	—
Input Offset Current ^(*5)	Iio	25°C	-	1	-	pA	—
Input Bias Current ^(*5)	Ib	25°C	-	1	-	pA	—
Supply Current ^(*6)	IDD	25°C	-	300	700	μA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	-	-	900		
High Level Output Voltage	VOH	25°C	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	—
Output Source Current ^(*7)	IOH	25°C	4	8	-	mA	VDD-0.4[V]
Output Sink Current ^(*7)	IOL	25°C	6	12	-	mA	VSS+0.4[V]
Slew Rate	SR	25°C	-	1.0	-	V/μs	CL=25[pF]
Gain Band width	FT	25°C	-	1	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	-	50	-	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	-	0.05	-	%	VOUT=1[Vp-p] , f=1[kHz]
Channel Separation	CS	25°C	-	100	-	dB	AV=40[dB]

(*5) Absolute value

(*6) Full range: BU7261, BU7262: Ta=-40[°C] to +85[°C] BU7462S: Ta=-40[°C] to +105[°C]

(*7) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
 When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7464 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7464F BU7464SF				
			Min.	Typ.	Max.		
Input Offset Voltage ^{(*)5}	Vio	25°C	-	1	6	mV	—
Input Offset Current ^{(*)5}	Iio	25°C	-	1	-	pA	—
Input Bias Current ^{(*)5}	Ib	25°C	-	1	-	pA	—
Supply Current ^{(*)6}	IDD	25°C	-	600	1400	μA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	-	-	1800		
High Level Output Voltage	VOH	25°C	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	—
Output Source Current ^{(*)7}	IOH	25°C	4	8	-	mA	VDD-0.4[V]
Output Sink Current ^{(*)7}	IOL	25°C	6	12	-	mA	VSS+0.4[V]
Slew Rate	SR	25°C	-	1.0	-	V/μs	CL=25[pF]
Gain Band width	FT	25°C	-	1	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	-	50	-	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	-	0.05	-	%	VOUT=0.8[Vp-p], f=1[kHz]
Channel Separation	CS	25°C	-	100	-	dB	AV=40[dB]

(*)8 Absolute value

(*)9 Full range: BU7464: Ta=-40[°C] to +85[°C] BU7464S: Ta=-40[°C] to +105[°C]

(*)10 Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7465 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7465HFV BU7465SHFV				
			Min.	Typ.	Max.		
Input Offset Voltage ^{(*)5}	Vio	25°C	-	1	6	mV	—
Input Offset Current ^{(*)5}	Iio	25°C	-	1	-	pA	—
Input Bias Current ^{(*)5}	Ib	25°C	-	1	-	pA	—
Supply Current ^{(*)6}	IDD	25°C	-	120	300	μA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	-	-	400		
High Level Output Voltage	VOH	25°C	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	60	100	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	—
Output Source Current ^{(*)7}	IOH	25°C	4	8	-	mA	VDD-0.4[V]
Output Sink Current ^{(*)7}	IOL	25°C	9	18	-	mA	VSS+0.4[V]
Slew Rate	SR	25°C	-	1.0	-	V/μs	CL=25[pF]
Gain Band width	FT	25°C	-	1.2	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	-	60	-	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	-	0.05	-	%	VOUT=0.8[Vp-p], f=1[kHz]

(*)11) Absolute value

(*)12) Full range: BU7465: Ta=-40[°C] to +85[°C] BU7465S: Ta=-40[°C] to +105[°C]

(*)13) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7441 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7441G, BU7441SG				
			Min.	Typ.	Max.		
Input Offset Voltage ^(*14)	Vio	25°C	-	1	6	mV	—
Input Offset Current ^(*14)	Iio	25°C	-	1	-	pA	—
Input Bias Current ^(*14)	Ib	25°C	-	1	-	pA	—
Supply Current ^(*15)	IDD	25°C	-	50	120	μA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	-	-	240		
High Level Output Voltage	VOH	25°C	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	—
Output Source Current ^(*16)	IOH	25°C	3	6	-	mA	VDD-0.4[V]
Output Sink Current ^(*16)	IOL	25°C	5	10	-	mA	VSS+0.4[V]
Slew Rate	SR	25°C	-	0.3	-	V/μs	CL=25[pF]
Gain Band width	FT	25°C	-	0.6	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	-	50	-	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	-	0.05	-	%	VOUT=1[Vp-p], f=1[kHz]

(*14) Absolute value

(*15) Full range: BU7441: Ta=-40[°C] to +85[°C] BU7441S: Ta=-40[°C] to +105[°C]

(*16) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7442 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7442F/FVM/NUX BU7442S F/FVM/NUX				
			Min.	Typ.	Max.		
Input Offset Voltage ^(*17)	Vio	25°C	-	1	6	mV	—
Input Offset Current ^(*17)	Iio	25°C	-	1	-	pA	—
Input Bias Current ^(*17)	Ib	25°C	-	1	-	pA	—
Supply Current ^(*18)	IDD	25°C	-	100	240	μA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	-	-	480		
High Level Output Voltage	VOH	25°C	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	—
Output Source Current ^(*19)	IOH	25°C	3	6	-	mA	VDD-0.4[V]
Output Sink Current ^(*19)	IOL	25°C	5	10	-	mA	VSS+0.4[V]
Slew Rate	SR	25°C	-	0.3	-	V/μs	CL=25[pF]
Gain Band width	FT	25°C	-	0.6	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	-	50	-	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	-	0.05	-	%	VOUT=1[Vp-p], f=1[kHz]
Channel Separation	CS	25°C	-	100	-	dB	AV=40[dB]

(*17) Absolute value

(*18) Full range: BU7442: Ta=-40[°C] to +85[°C] BU7442S: Ta=-40[°C] to +105[°C]

(*19) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7444 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7444F, BU7444SF				
			Min.	Typ.	Max.		
Input Offset Voltage ^(*20)	Vio	25°C	-	1	6	mV	—
Input Offset Current ^(*20)	Iio	25°C	-	1	-	pA	—
Input Bias Current ^(*20)	Ib	25°C	-	1	-	pA	—
Supply Current ^(*21)	IDD	25°C	-	200	480	μA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	-	-	960		
High Level Output Voltage	VOH	25°C	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	—
Output Source Current ^(*22)	IOH	25°C	3	6	-	mA	VDD-0.4[V]
Output Sink Current ^(*22)	IOL	25°C	5	10	-	mA	VSS+0.4[V]
Slew Rate	SR	25°C	-	0.3	-	V/μs	CL=25[pF]
Gain Band width	FT	25°C	-	0.6	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	-	50	-	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	-	0.05	-	%	VOUT=0.8[Vp-p], f=1[kHz]
Channel Separation	CS	25°C	-	100	-	dB	AV=40[dB]

(*20) Absolute value

(*21) Full range: BU7444: Ta=-40[°C] to +85[°C] BU7444S: Ta=-40[°C] to +105[°C]

(*22) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7445 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7445HFV, BU7445SHFV				
			Min.	Typ.	Max.		
Input Offset Voltage ^(*23)	Vio	25°C	-	1	6	mV	—
Input Offset Current ^(*23)	Iio	25°C	-	1	-	pA	—
Input Bias Current ^(*23)	Ib	25°C	-	1	-	pA	—
Supply Current ^(*24)	IDD	25°C	-	40	90	μA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	-	-	120		
High Level Output Voltage	VOH	25°C	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	60	100	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	—
Output Source Current ^(*25)	IOH	25°C	4	8	-	mA	VDD-0.4[V]
Output Sink Current ^(*25)	IOL	25°C	9	18	-	mA	VSS+0.4[V]
Slew Rate	SR	25°C	-	0.25	-	V/μs	CL=25[pF]
Gain Band width	FT	25°C	-	0.4	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	-	60	-	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	-	0.05	-	%	VOUT=0.8[Vp-p], f=1[kHz]

(*23) Absolute value

(*24) Full range: BU7445: Ta=-40[°C] to +85[°C] BU7445S: Ta=-40[°C] to +105[°C]

(*25) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

●Reference data (BU7461 family)

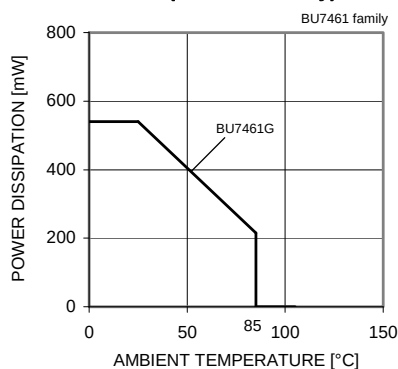


Fig.1
Derating curve

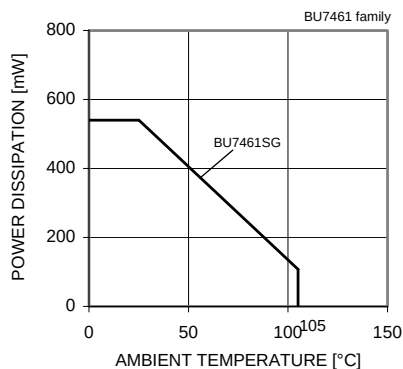


Fig.2
Derating curve

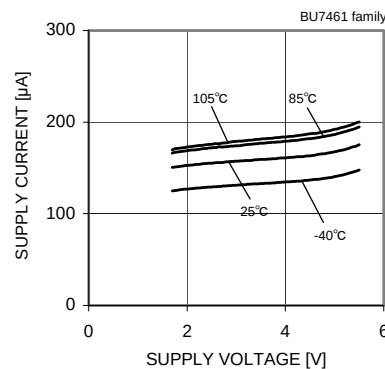


Fig.3
Supply Current – Supply Voltage

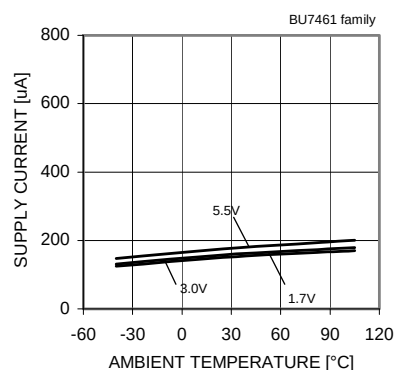


Fig.4
Supply Current – Ambient Temperature

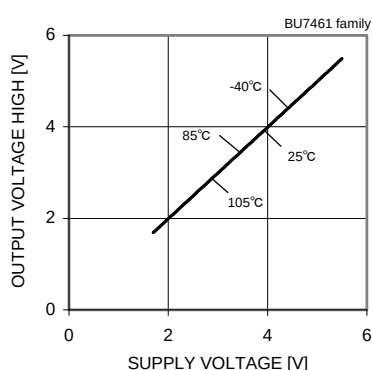


Fig.5
Output Voltage High – Supply Voltage
($R_L=10[k\Omega]$)

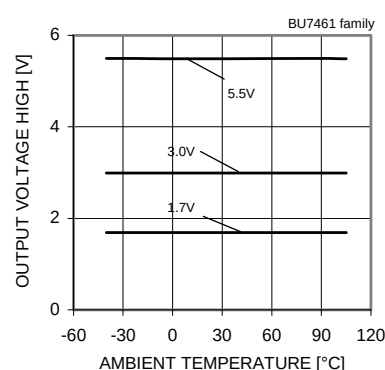


Fig.6
Output Voltage High – Ambient Temperature
($R_L=10[k\Omega]$)

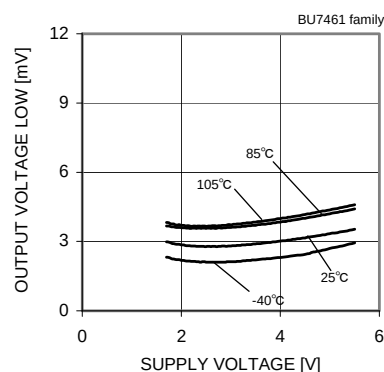


Fig.7
Output Voltage Low – Supply Voltage
($R_L=10[k\Omega]$)

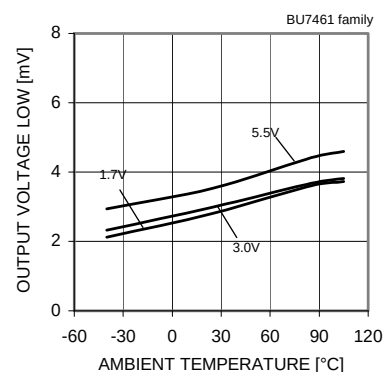


Fig.8
Output Voltage Low – Ambient Temperature
($R_L=10[k\Omega]$)

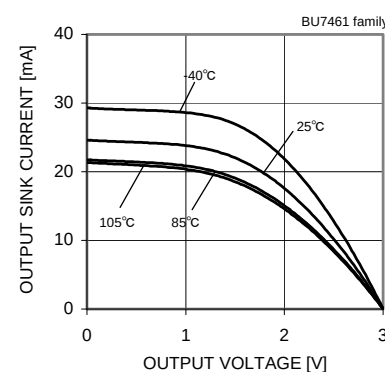


Fig.9
Output Source Current – Output Voltage
($V_{DD}=3.0[V]$)

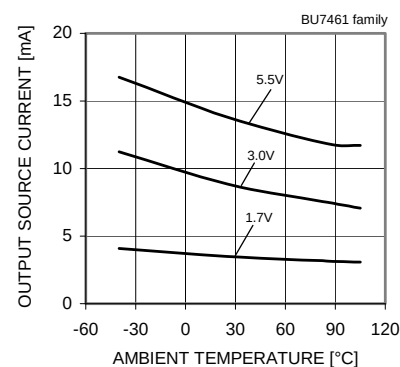


Fig.10
Output Source Current – Ambient Temperature
($V_{OUT}=V_{DD}-0.4[V]$)

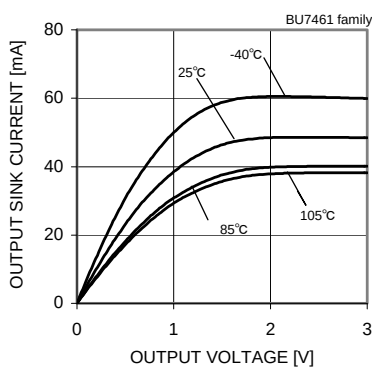


Fig.11
Output Sink Current – Output Voltage
($V_{DD}=3[V]$)

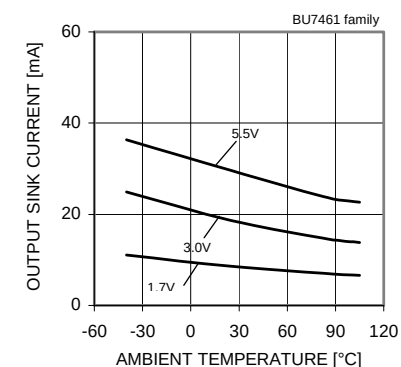


Fig.12
Output Sink Current – Ambient Temperature
($V_{OUT}=V_{SS}+0.4[V]$)

(*)The above data is ability value of sample, it is not guaranteed. BU7461G: -40[°C] ~ +85[°C] BU7461SG: -40[°C] ~ +105[°C]

●Reference data (BU7461 family)

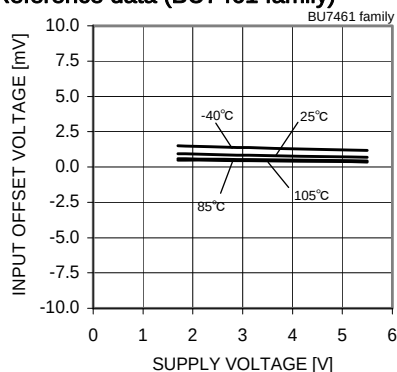


Fig.13
Input Offset Voltage – Supply Voltage
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

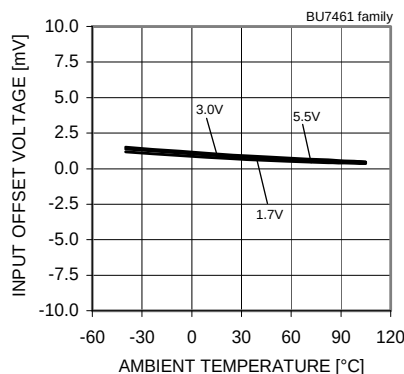


Fig.14
Input Offset Voltage – Ambient Temperature
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

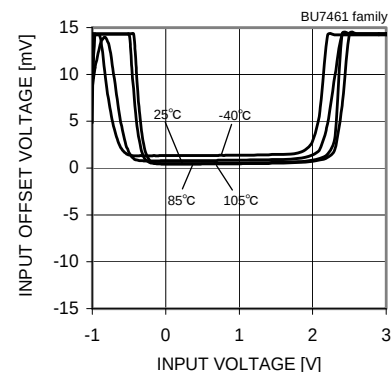


Fig.15
Input Offset Voltage – Input Voltage
($V_{DD} = 3[V]$)

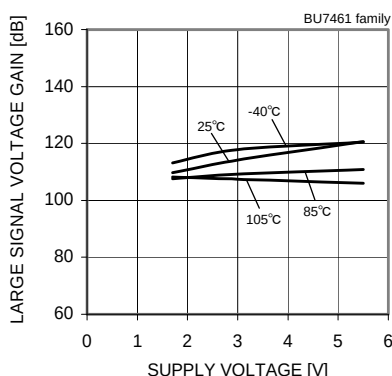


Fig.16
Large Signal Voltage Gain
– Supply Voltage

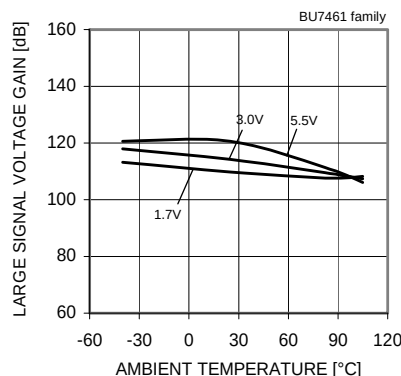


Fig.17
Power Supply Rejection Ratio
– Ambient Temperature

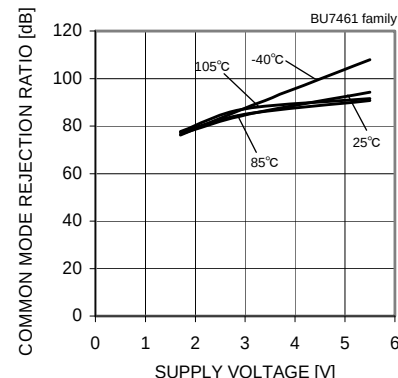


Fig.18
Common Mode Rejection Ratio
– Supply Voltage

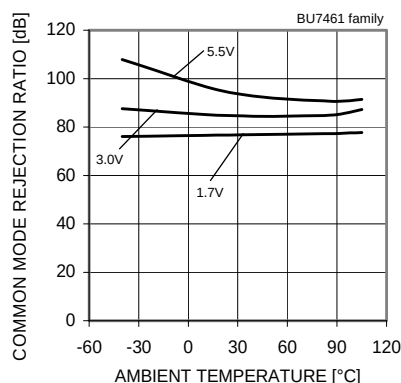


Fig.19
Common Mode Rejection Ratio
– Ambient Temperature

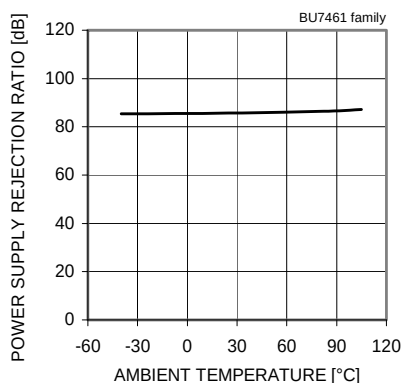


Fig.20
Large Signal Voltage Gain
– Ambient Temperature

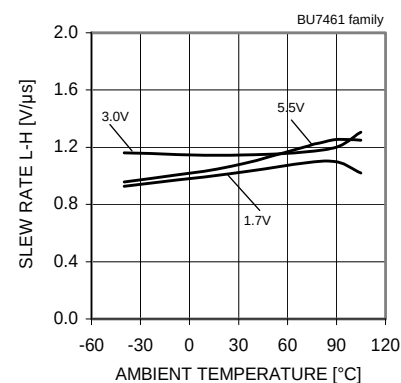


Fig.21
Slew Rate L-H – Ambient Temperature

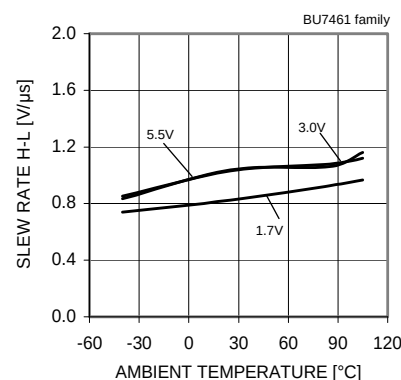


Fig.22
Slew Rate H-L – Ambient Temperature

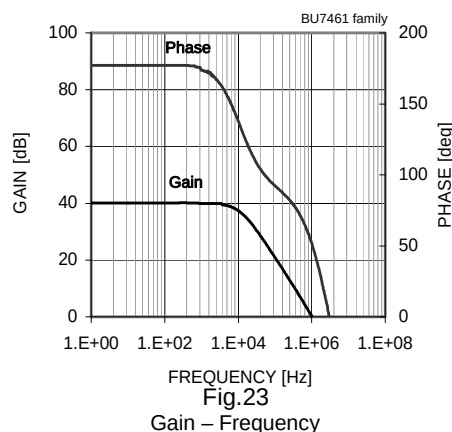


Fig.23
Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7461G: -40[°C] ~ +85[°C] BU7461SG: -40[°C] ~ +105[°C]

●Reference data (BU7462 family)

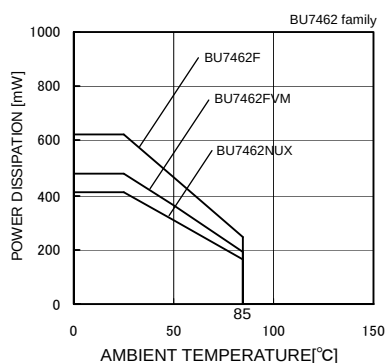


Fig.24
Derating curve

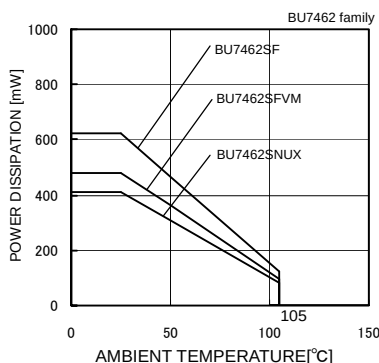


Fig.25
Derating curve

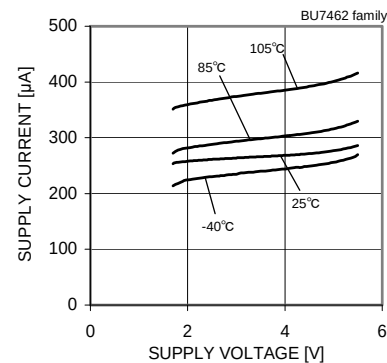


Fig.26
Supply Current – Supply Voltage

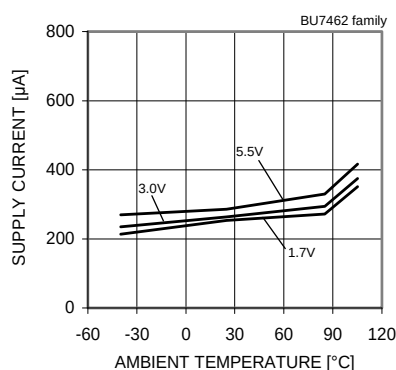


Fig.27
Supply Current – Ambient Temperature

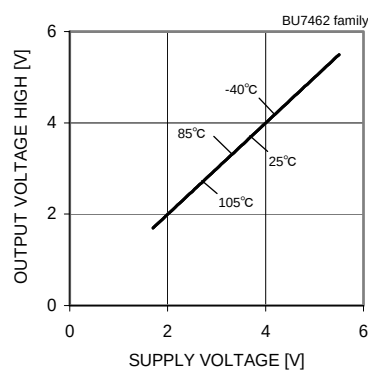


Fig.28
Output Voltage High – Supply Voltage
($R_L=10[k\Omega]$)

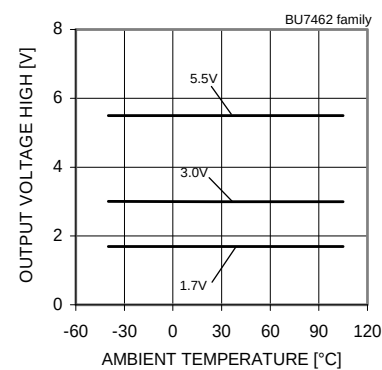


Fig.29
Output Voltage High – Ambient Temperature
($R_L=10[k\Omega]$)

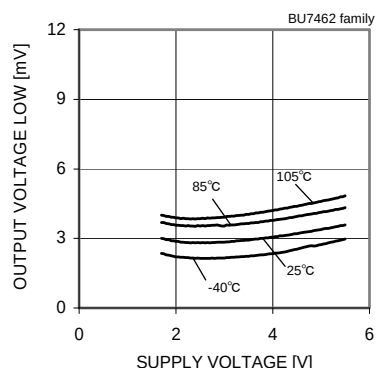


Fig.30
Output Voltage Low – Supply Voltage
($R_L=10[k\Omega]$)

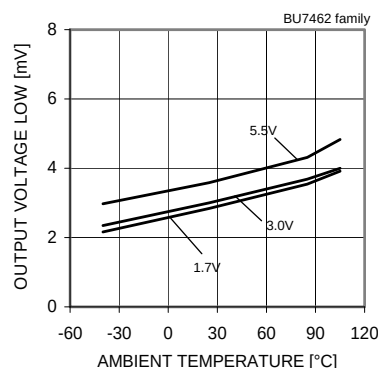


Fig.31
Output Voltage Low – Ambient Temperature
($R_L=10[k\Omega]$)

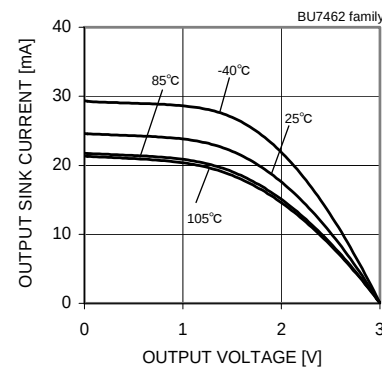


Fig.32
Output Source Current – Output Voltage
($V_{DD}=3.0[V]$)

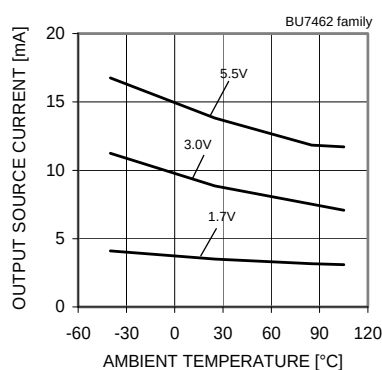


Fig.33
Output Source Current – Ambient Temperature
($V_{OUT}=V_{DD}-0.4[V]$)

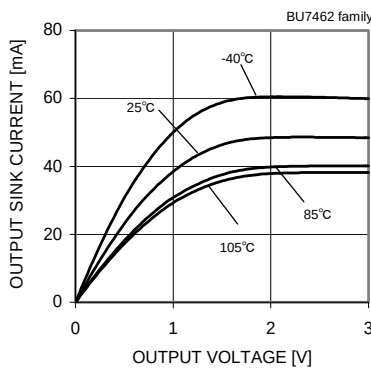


Fig.34
Output Sink Current – Output Voltage
($V_{DD}=3[V]$)

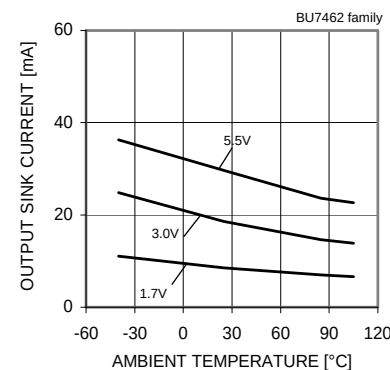


Fig.35
Output Sink Current – Ambient Temperature
($V_{OUT}=V_{SS}+0.4[V]$)

(*)The above data is ability value of sample, it is not guaranteed. BU7462F/FVM/NUX: -40[°C] ~ +85[°C] BU7462S F/FVM/NUX: -40[°C] ~ +105[°C]

●Reference data (BU7462 family)

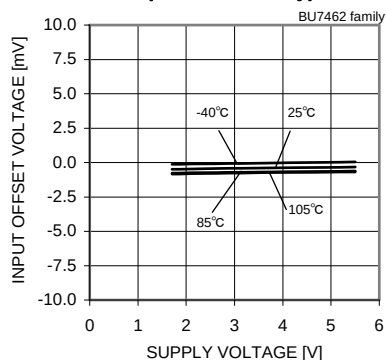


Fig.36

Input Offset Voltage – Supply Voltage
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

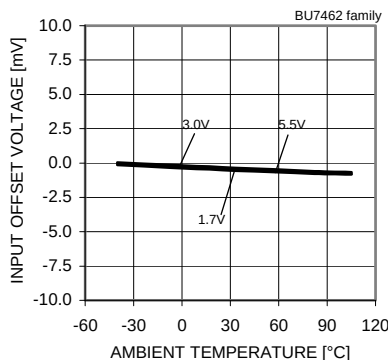


Fig.37

Input Offset Voltage – Ambient Temperature
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

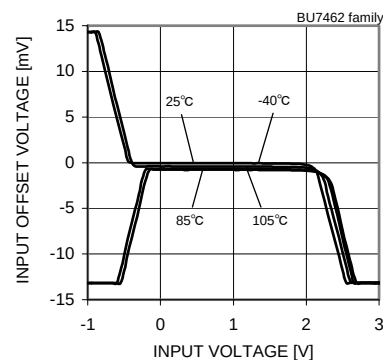


Fig.38

Input Offset Voltage – Input Voltage
($V_{DD} = 3[V]$)

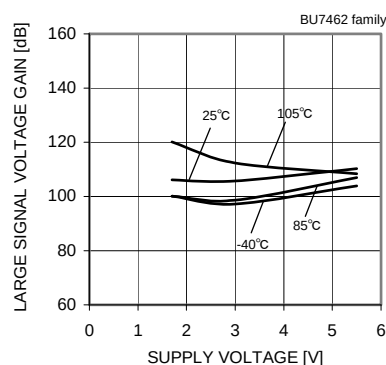


Fig.39

Large Signal Voltage Gain
– Supply Voltage

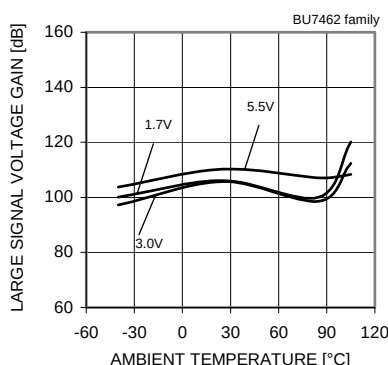


Fig.40

Large Signal Voltage Gain
– Ambient Temperature

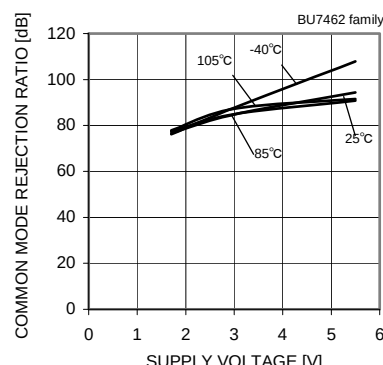


Fig.41

Common Mode Rejection Ratio
– Supply Voltage

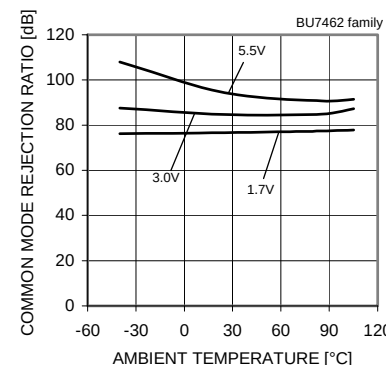


Fig.42

Common Mode Rejection Ratio
– Ambient Temperature

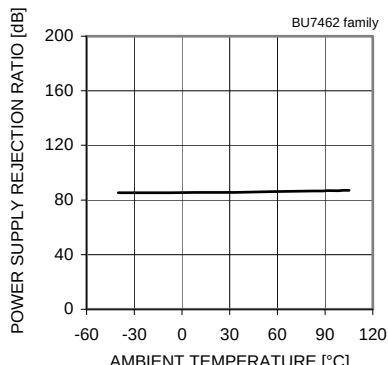


Fig.43

Power Supply Rejection Ratio
– Ambient Temperature

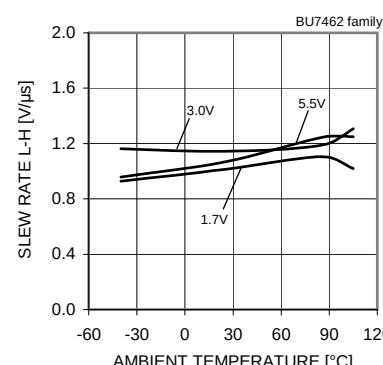


Fig.44

Slew Rate L-H – Ambient Temperature

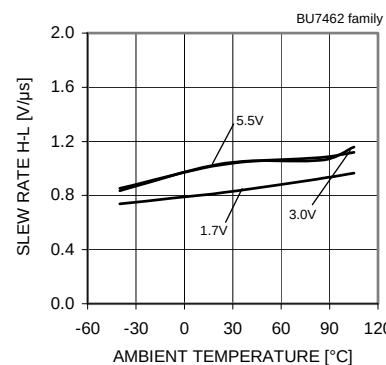


Fig.45

Slew Rate H-L – Ambient Temperature

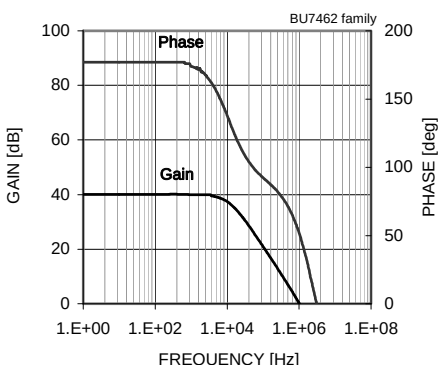


Fig.46

Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7462F/FVM/NUX: -40[°C] ~ +85[°C] BU7462S F/FVM/NUX: -40[°C] ~ +105[°C]

●Reference data (BU7464 family)

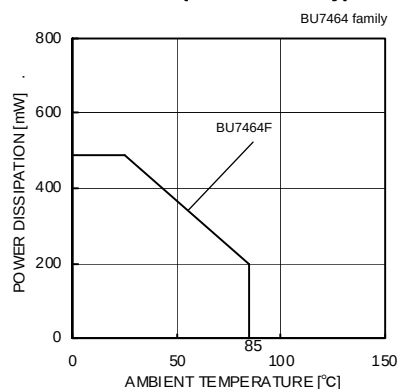


Fig.47

Derating curve

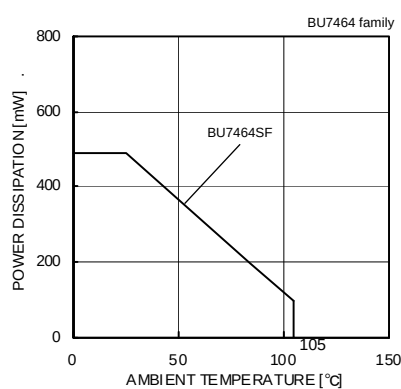


Fig.48

Derating curve

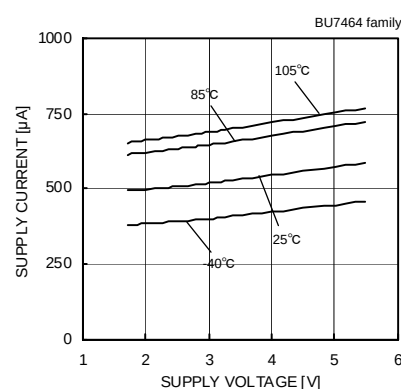


Fig.49

Supply Current – Supply Voltage

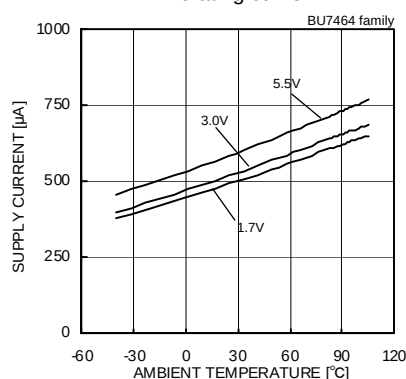


Fig.50

Supply Current – Ambient Temperature

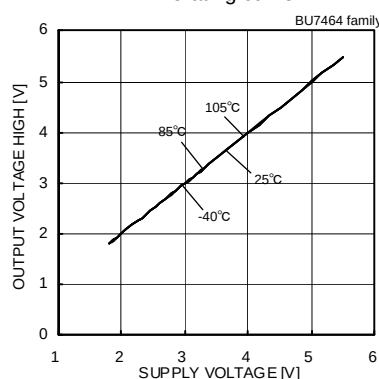


Fig.51

Output Voltage High – Supply Voltage
($R_L=10[k\Omega]$)

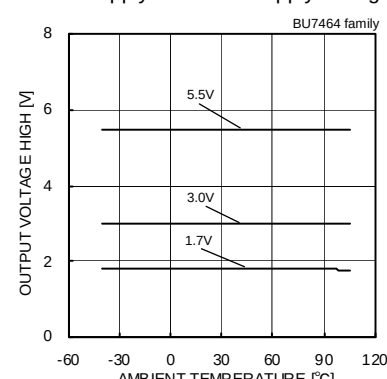


Fig.52

Output Voltage High – Ambient Temperature
($R_L=10[k\Omega]$)

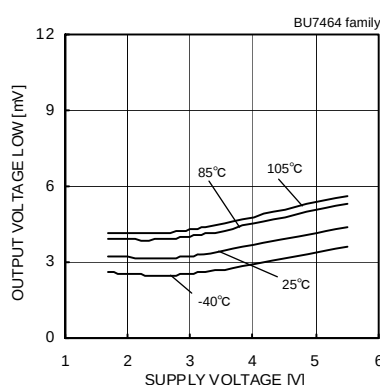


Fig.53

Output Voltage Low – Supply Voltage
($R_L=10[k\Omega]$)

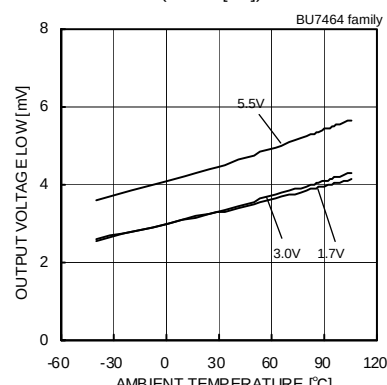


Fig.54

Output Voltage Low – Ambient Temperature
($R_L=10[k\Omega]$)

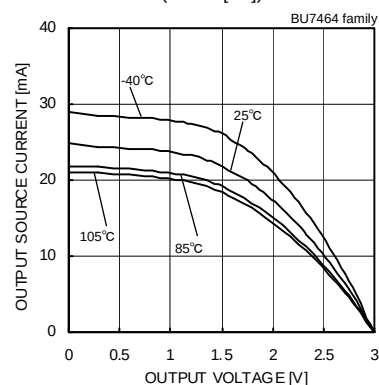


Fig.55

Output Source Current – Output Voltage
($V_{DD}=3.0[V]$)

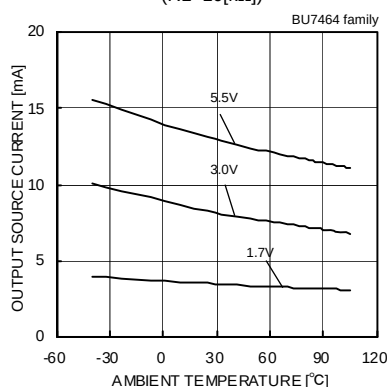


Fig.56

Output Source Current – Ambient Temperature
($V_{OUT}=V_{DD}-0.4[V]$)

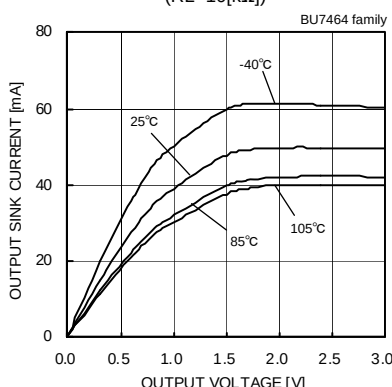


Fig.57

Output Sink Current – Output Voltage
($V_{DD}=3[V]$)

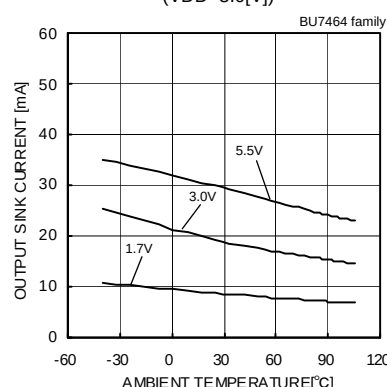


Fig.58

Output Sink Current – Ambient Temperature
($V_{OUT}=V_{SS}+0.4[V]$)

(*)The above data is ability value of sample, it is not guaranteed. BU7464F: $-40[^\circ\text{C}] \sim +85[^\circ\text{C}]$ BU7464SF: $-40[^\circ\text{C}] \sim +105[^\circ\text{C}]$

●Reference data (BU7464 family)

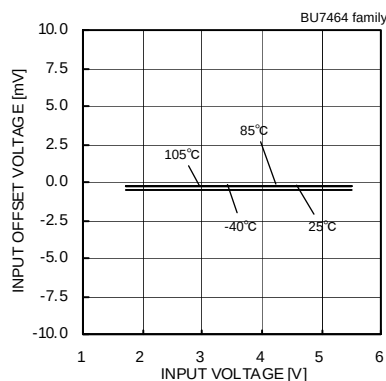


Fig.59

Input Offset Voltage – Supply Voltage
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

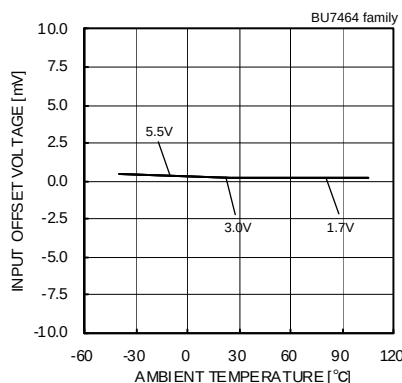


Fig.60

Input Offset Voltage – Ambient Temperature
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

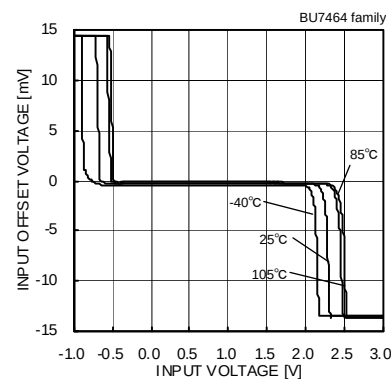


Fig.61

Input Offset Voltage – Input Voltage
($V_{DD} = 3[V]$)

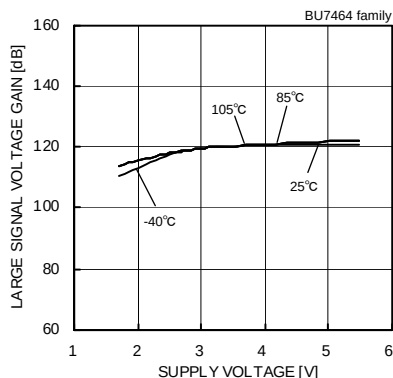


Fig.62

Large Signal Voltage Gain
– Supply Voltage

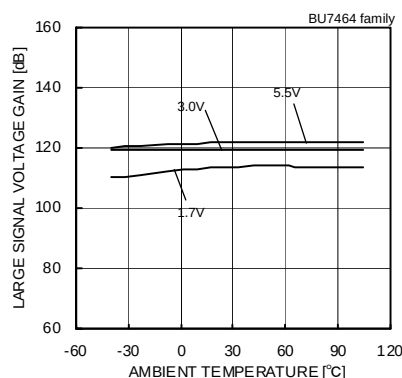


Fig.63

Large Signal Voltage Gain
– Ambient Temperature

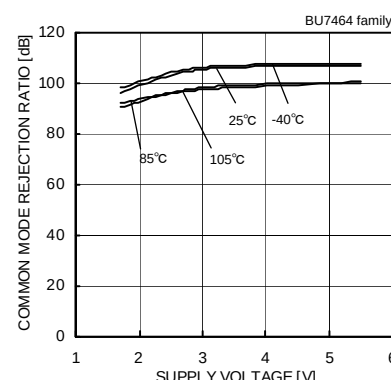


Fig.64

Common Mode Rejection Ratio
– Supply Voltage

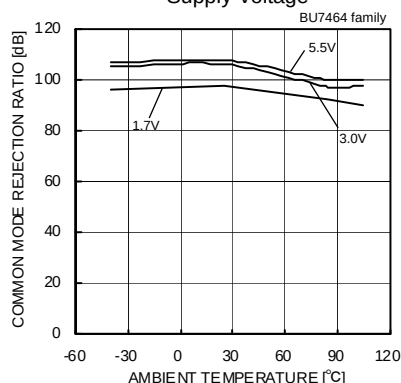


Fig.65

Common Mode Rejection Ratio
– Ambient Temperature

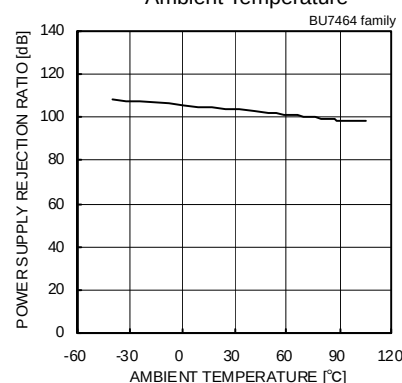


Fig.66

Power Supply Rejection Ratio
– Ambient Temperature

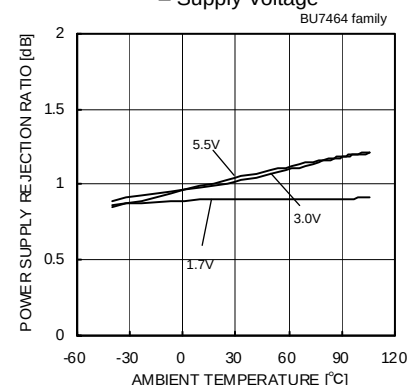


Fig.67

Slew Rate L-H – Ambient Temperature

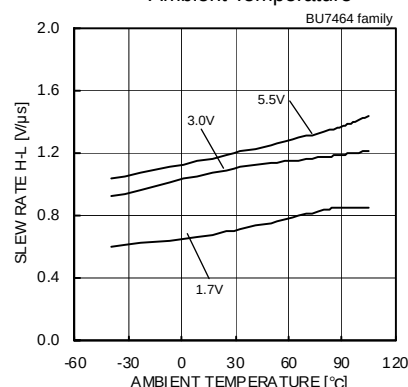


Fig.68

Slew Rate H-L – Ambient Temperature

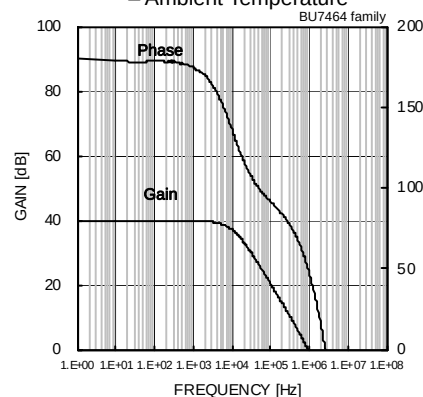


Fig.69

Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7464F: -40[°C] ~ +85[°C] BU7464SF: -40[°C] ~ +105[°C]

●Reference data (BU7465 family)

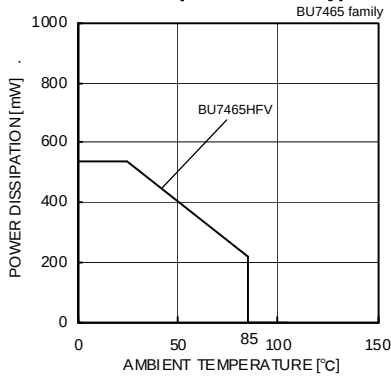


Fig.70

Derating curve

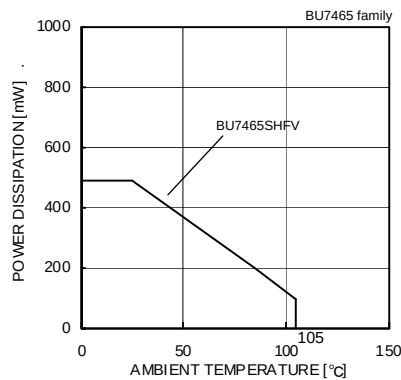


Fig.71

Derating curve

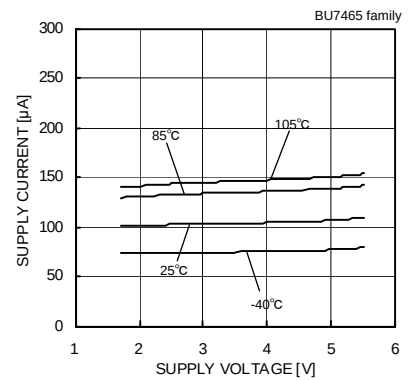


Fig.72

Supply Current – Supply Voltage

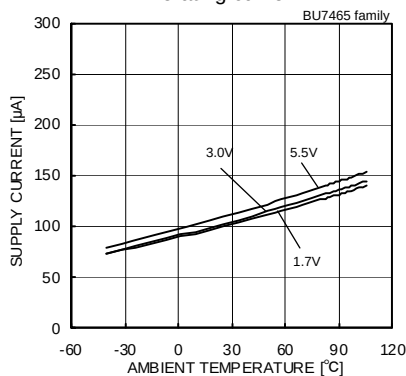


Fig.73

Supply Current – Ambient Temperature

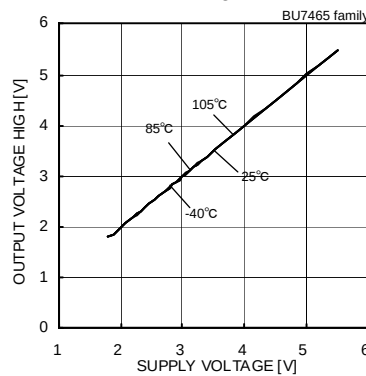


Fig.74

Output Voltage High – Supply Voltage
($R_L=10[k\Omega]$)

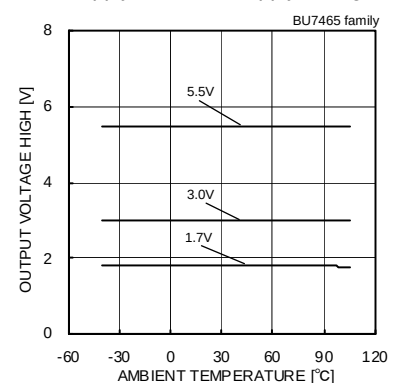


Fig.75

Output Voltage High – Ambient Temperature
($R_L=10[k\Omega]$)

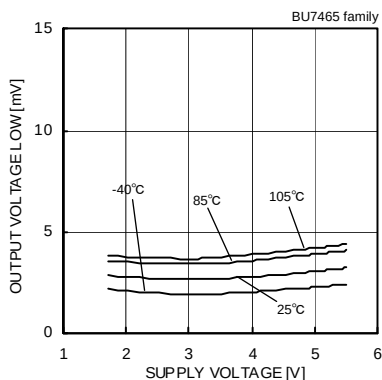


Fig.76

Output Voltage Low – Supply Voltage
($R_L=10[k\Omega]$)

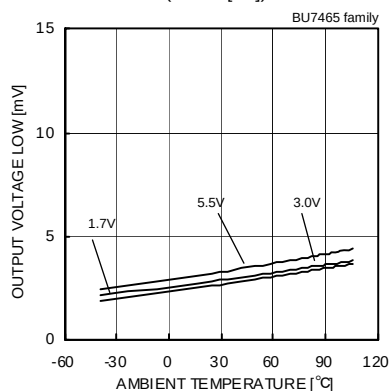


Fig.77

Output Voltage Low – Ambient Temperature
($R_L=10[k\Omega]$)

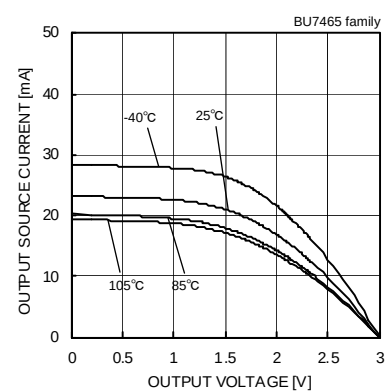


Fig.78

Output Source Current – Output Voltage
($V_{DD}=3[V]$)

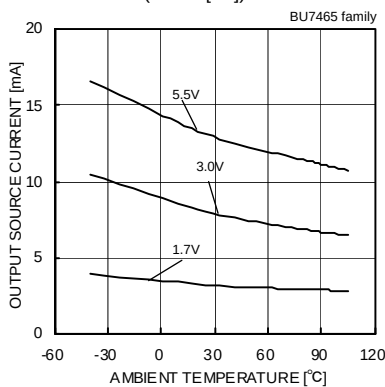


Fig.79

Output Source Current – Ambient Temperature
($V_{OUT}=V_{DD}-0.4[V]$)

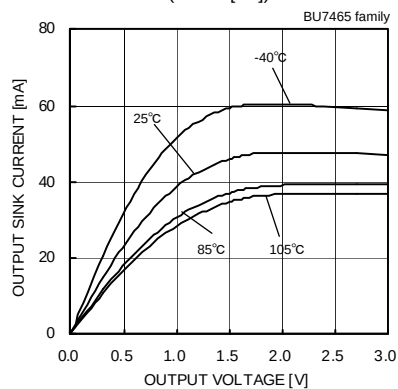


Fig.80

Output Sink Current – Output Voltage
($V_{DD}=3[V]$)

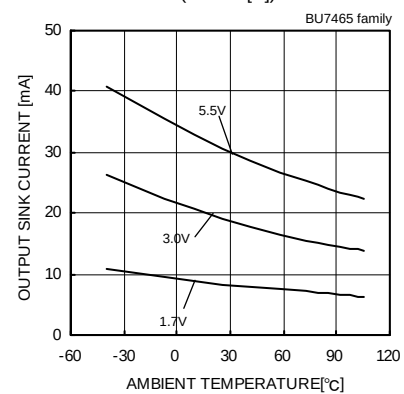


Fig.81

Output Sink Current – Ambient Temperature
($V_{OUT}=V_{SS}+0.4[V]$)

(*)The above data is ability value of sample, it is not guaranteed. BU7465HFV: $-40[^\circ\text{C}] \sim +85[^\circ\text{C}]$ BU7465SHFV: $-40[^\circ\text{C}] \sim +105[^\circ\text{C}]$

●Reference data (BU7465 family)

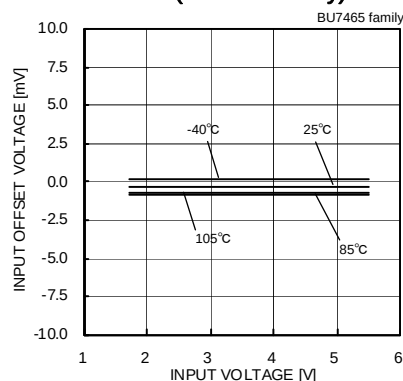


Fig.82

Input Offset Voltage – Supply Voltage
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

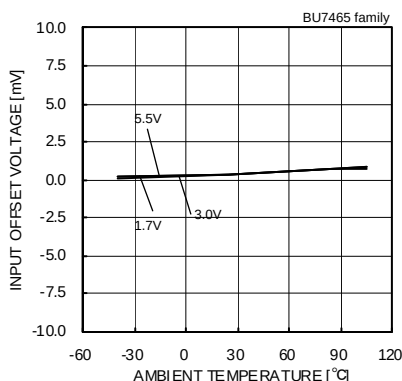


Fig.83

Input Offset Voltage – Ambient Temperature
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

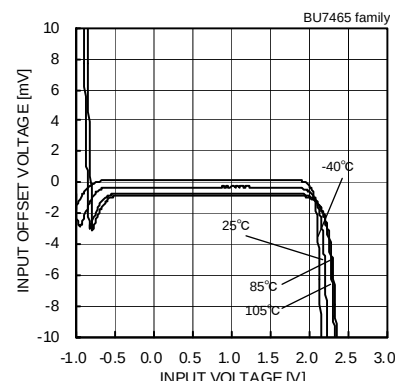


Fig.84

Input Offset Voltage – Input Voltage
($V_{DD} = 3[V]$)

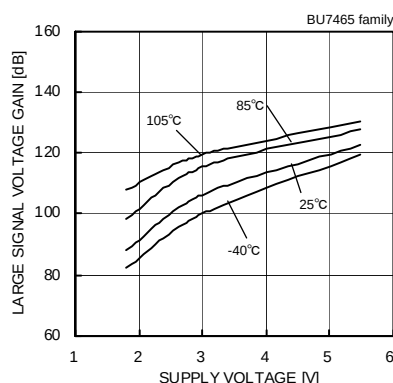


Fig.85

Large Signal Voltage Gain
– Supply Voltage

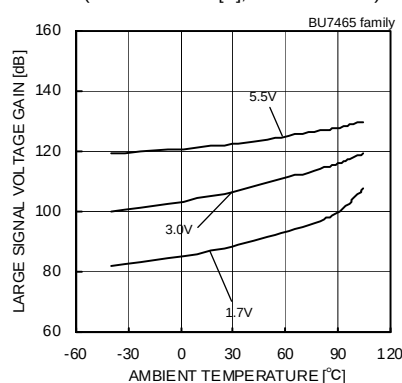


Fig.86

Large Signal Voltage Gain
– Ambient Temperature

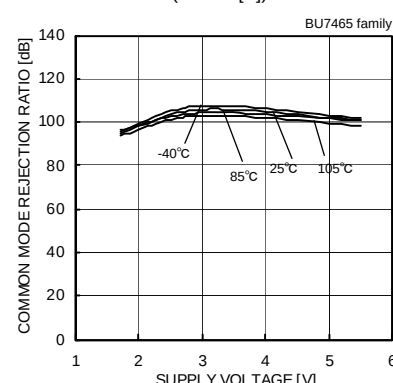


Fig.87

Common Mode Rejection Ratio
– Supply Voltage

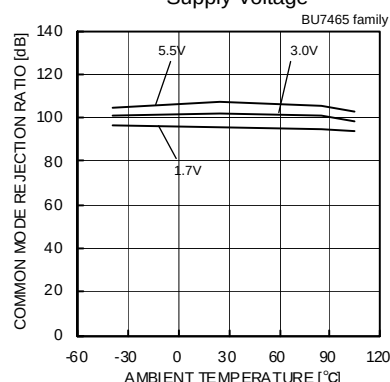


Fig.88

Common Mode Rejection Ratio
– Ambient Temperature

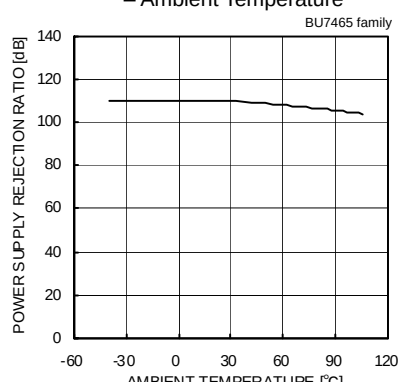


Fig.89

Power Supply Rejection Ratio
– Ambient Temperature

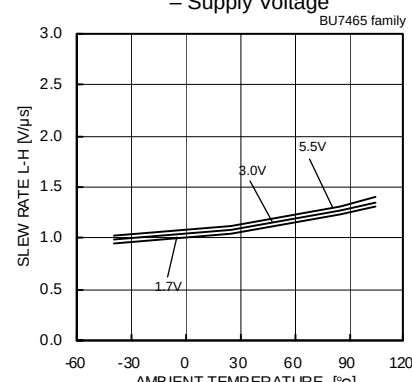


Fig.90

Slew Rate L-H – Ambient Temperature

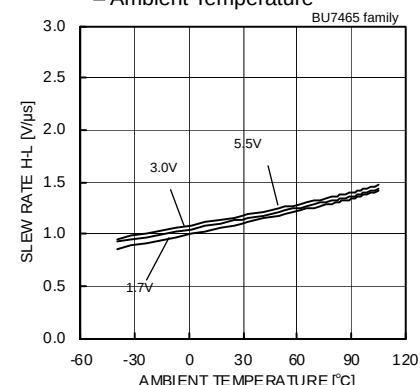


Fig.91

Slew Rate H-L – Ambient Temperature

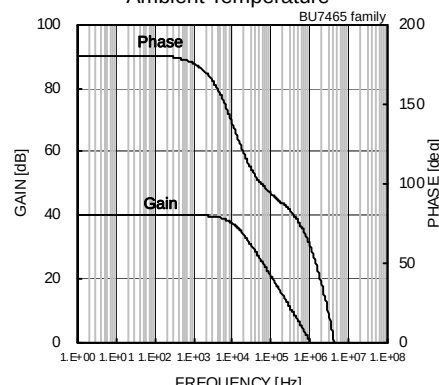


Fig.92

Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7465HFV: -40[°C] ~ +85[°C] BU7465SHFV: -40[°C] ~ +105[°C]

●Reference data (BU7441 family)

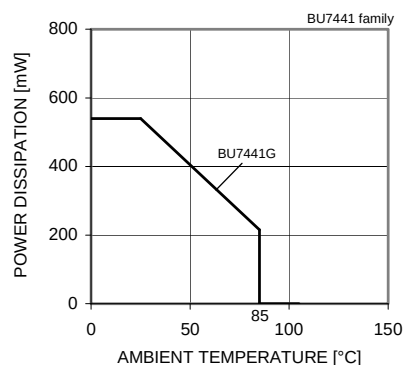


Fig.93
Derating curve

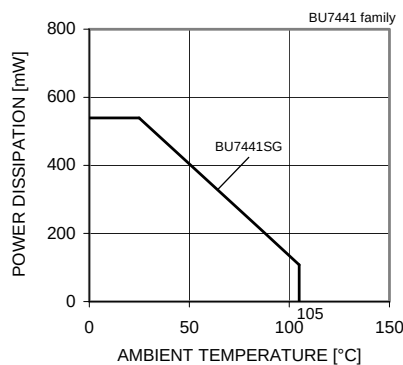


Fig.94
Derating curve

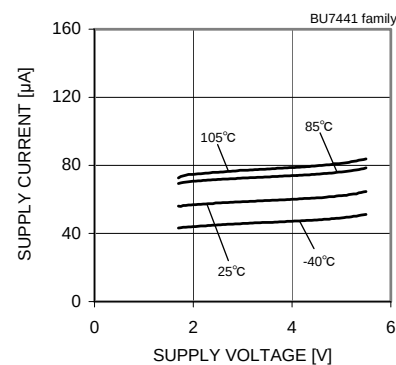


Fig.95
Supply Current – Supply Voltage

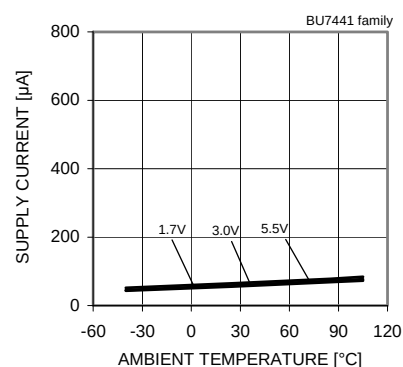


Fig.96
Supply Current – Ambient Temperature

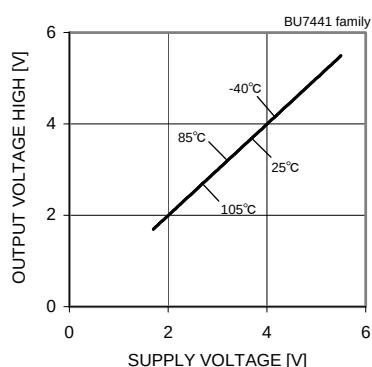


Fig.97
Output Voltage High – Supply Voltage
($R_L=10[k\Omega]$)

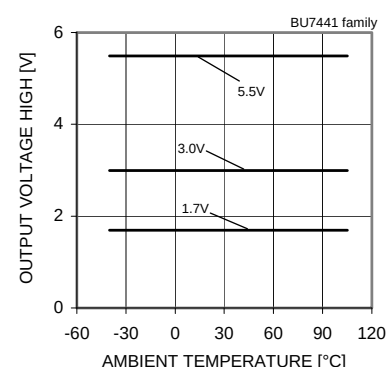


Fig.98
Output Voltage High – Ambient Temperature
($R_L=10[k\Omega]$)

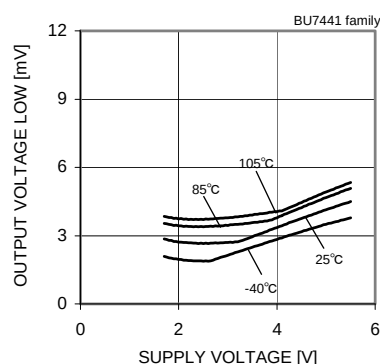


Fig.99
Output Voltage Low – Supply Voltage
($R_L=10[k\Omega]$)

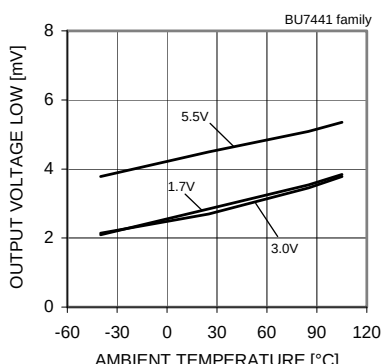


Fig.100
Output Voltage Low – Ambient Temperature
($R_L=10[k\Omega]$)

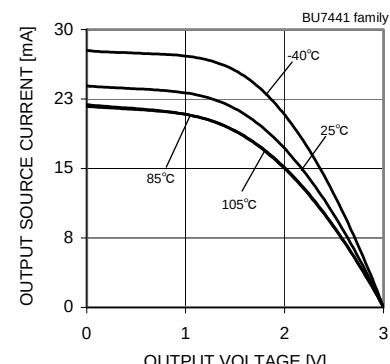


Fig.101
Output Source Current – Output Voltage
($V_{DD}=3[V]$)

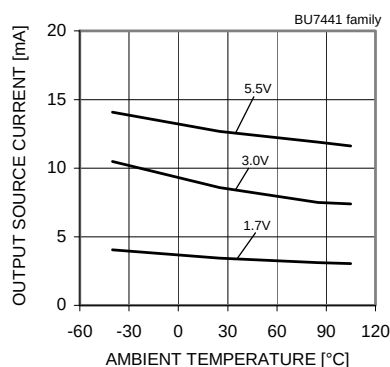


Fig.102
Output Source Current – Ambient Temperature
($V_{OUT}=V_{DD}-0.4[V]$)

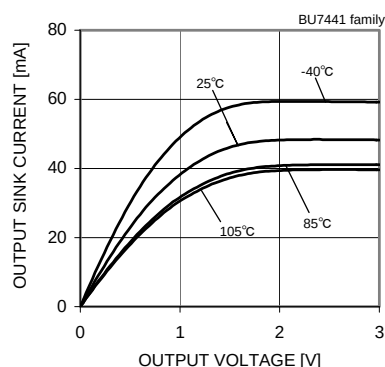


Fig.103
Output Sink Current – Output Voltage
($V_{DD}=3[V]$)

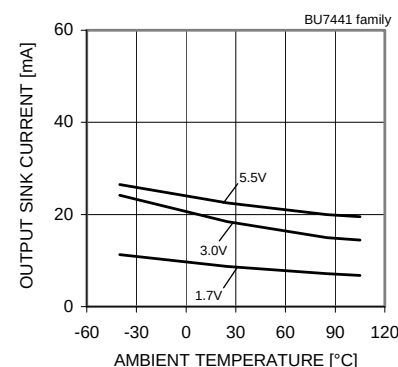


Fig.104
Output Sink Current – Ambient Temperature
($V_{OUT}=V_{SS}+0.4[V]$)

(*)The above data is ability value of sample, it is not guaranteed. BU7441G: -40[°C] ~ +85[°C] BU7441SG: -40[°C] ~ +105[°C]

●Reference data (BU7441 family)

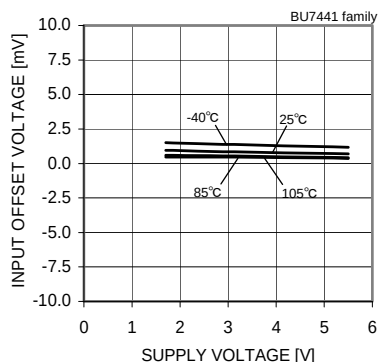


Fig.105

Input Offset Voltage – Supply Voltage
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

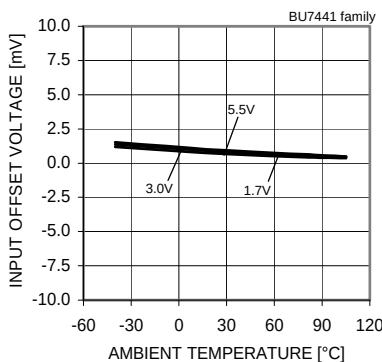


Fig.106

Input Offset Voltage – Ambient Temperature
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

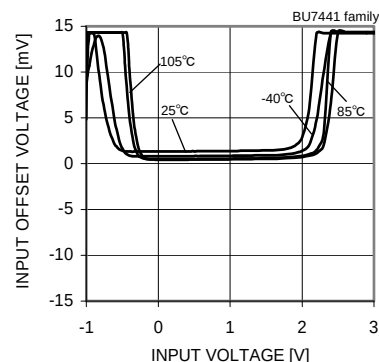


Fig.107

Input Offset Voltage – Input Voltage
($V_{DD} = 3[V]$)

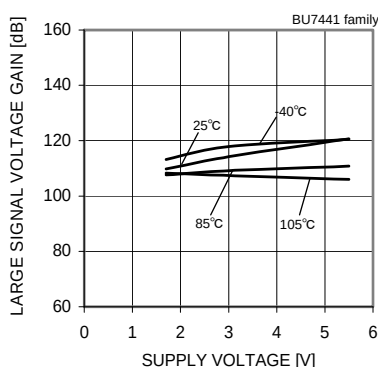


Fig.108

Large Signal Voltage Gain
– Supply Voltage

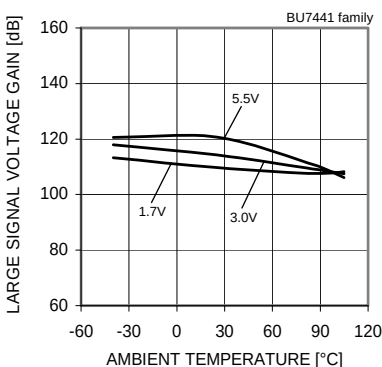


Fig.109

Large Signal Voltage Gain
– Ambient Temperature

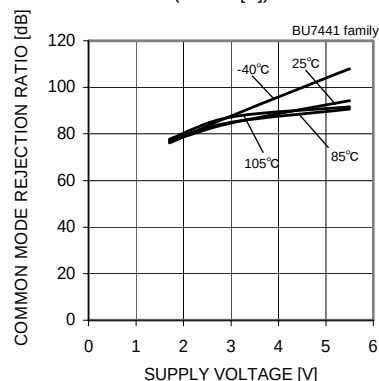


Fig.110

Common Mode Rejection Ratio
– Supply Voltage

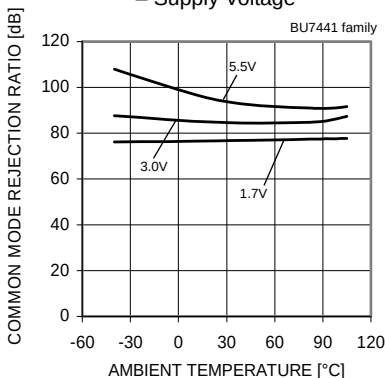


Fig.111

Common Mode Rejection Ratio
– Ambient Temperature

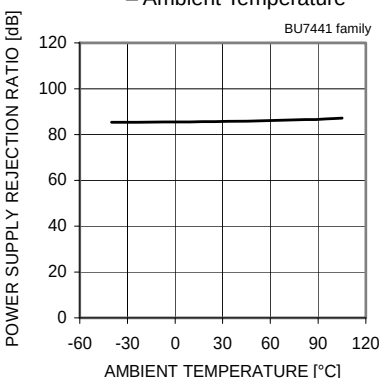


Fig.112

Power Supply Rejection Ratio
– Ambient Temperature

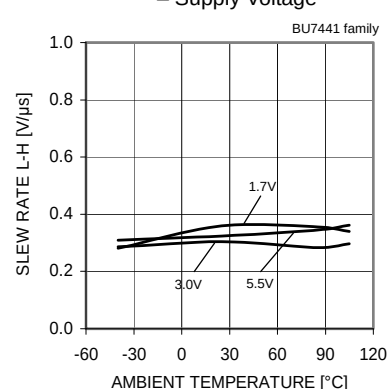


Fig.113

Slew Rate L-H – Ambient Temperature

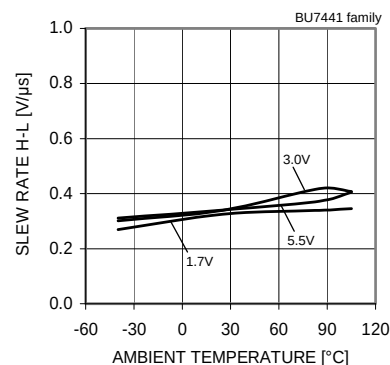


Fig.114

Slew Rate H-L – Ambient Temperature

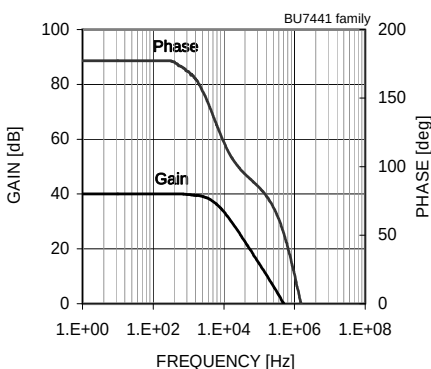


Fig.115

Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7441G: -40[°C] ~ +85[°C] BU7441SG: -40[°C] ~ +105[°C]

●Reference data (BU7442 family)

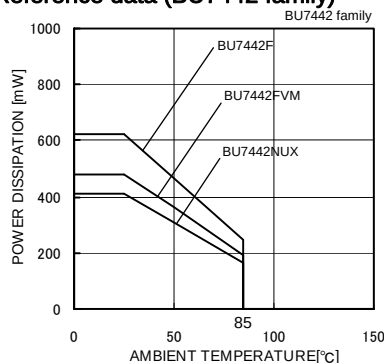


Fig.116

Derating curve

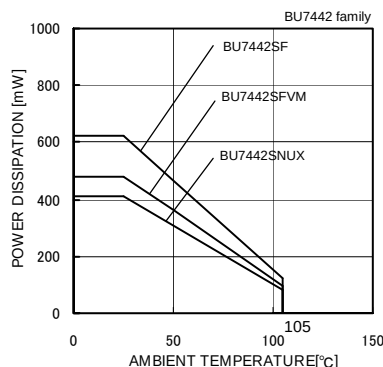


Fig.117

Derating curve

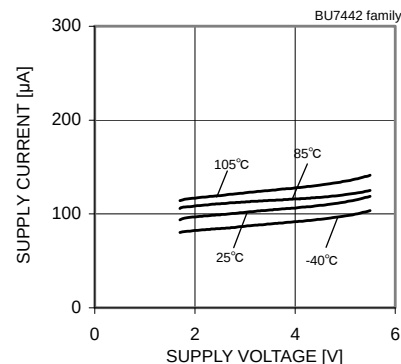


Fig.118

Supply Current – Supply Voltage

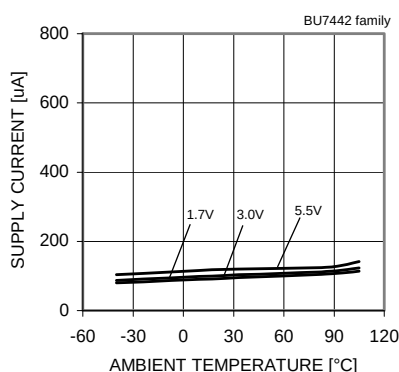


Fig.119

Supply Current – Ambient Temperature

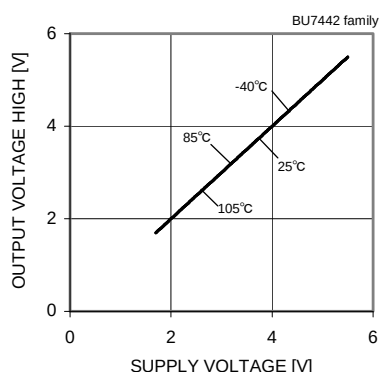


Fig.120

Output Voltage High – Supply Voltage
($R_L=10[k\Omega]$)

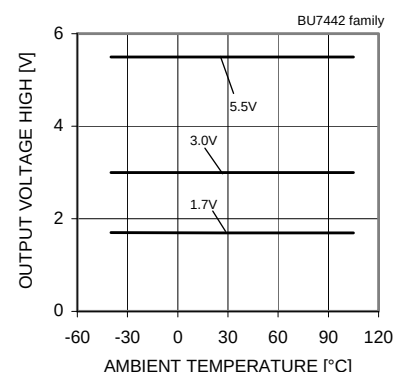


Fig.121

Output Voltage High – Ambient Temperature
($R_L=10[k\Omega]$)

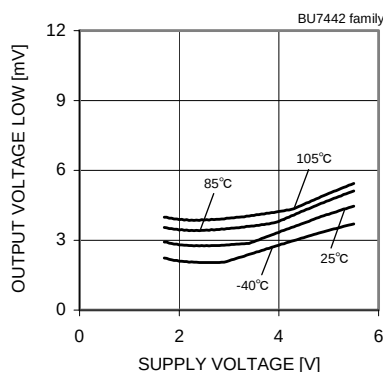


Fig.122

Output Voltage Low – Supply Voltage
($R_L=10[k\Omega]$)

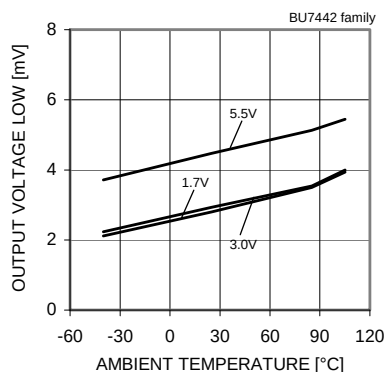


Fig.123

Output Voltage Low – Ambient Temperature
($R_L=10[k\Omega]$)

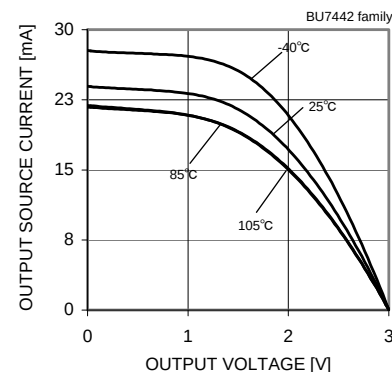


Fig.124

Output Source Current – Output Voltage
($V_{DD}=3.0[V]$)

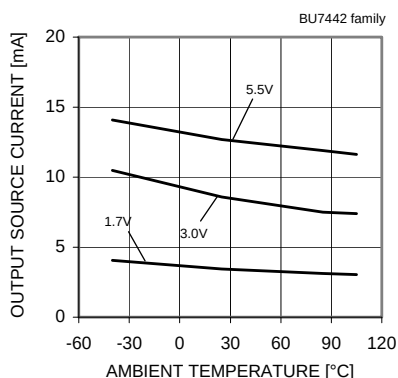


Fig.125

Output Source Current – Ambient Temperature
($V_{OUT}=V_{DD}-0.4[V]$)

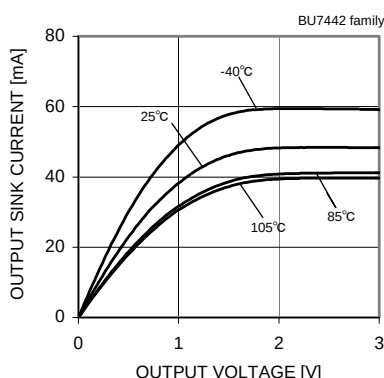


Fig.126

Output Sink Current – Output Voltage
($V_{DD}=3[V]$)

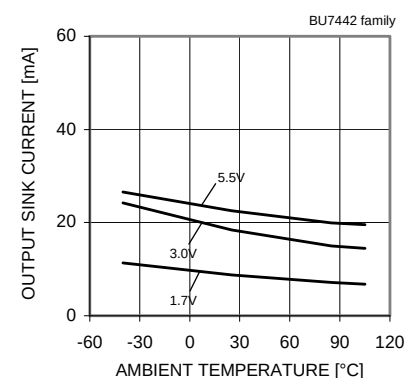


Fig.127

Output Sink Current – Ambient Temperature
($V_{OUT}=V_{SS}+0.4[V]$)

(*)The above data is ability value of sample, it is not guaranteed. BU7442F/FVM/NXX: -40[°C] ~ +85[°C]

BU7442S F/FVM/NXX: -40[°C] ~ +105[°C]

●Reference data (BU7442 family)

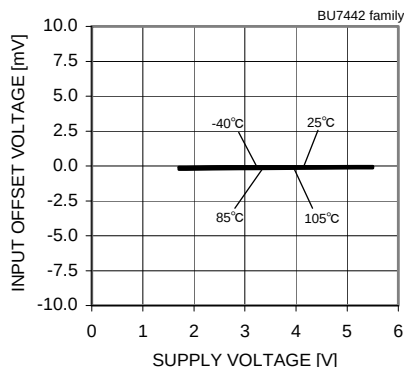


Fig.128

Input Offset Voltage – Supply Voltage
(Vicm= VDD-1.2[V], VOUT= VDD/2)

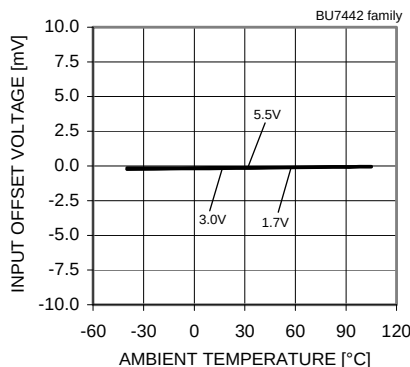


Fig.129

Input Offset Voltage – Ambient Temperature
(Vicm= VDD-1.2[V], VOUT= VDD/2)

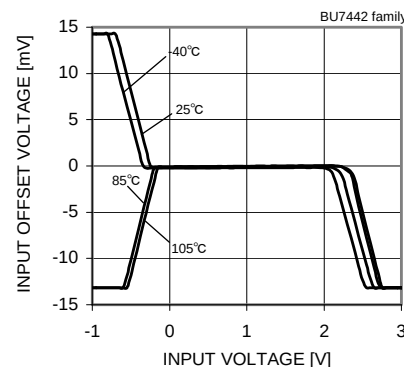


Fig.130

Input Offset Voltage – Input Voltage
(VDD=3[V])

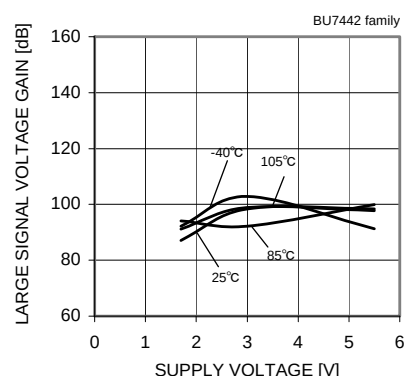


Fig.131

Large Signal Voltage Gain
– Supply Voltage

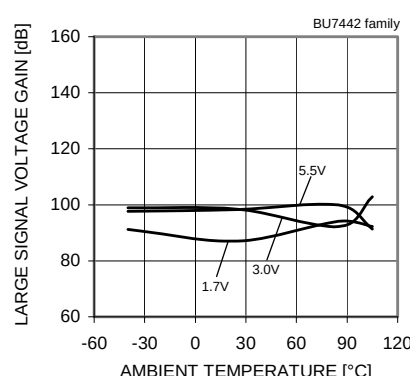


Fig.132

Large Signal Voltage Gain
– Ambient Temperature

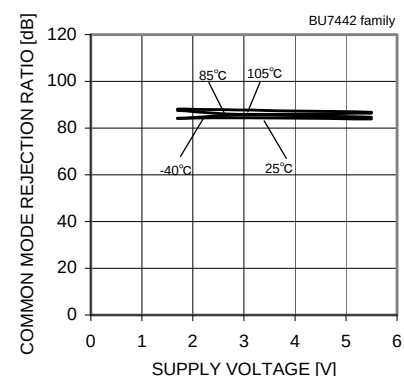


Fig.133

Common Mode Rejection Ratio
– Supply Voltage

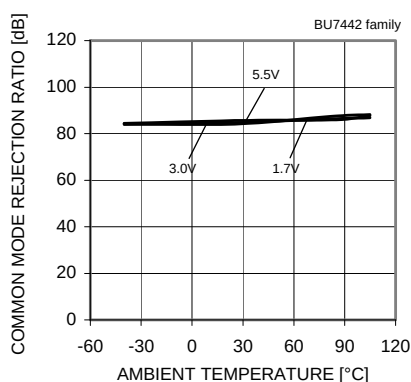


Fig.134

Common Mode Rejection Ratio
– Ambient Temperature

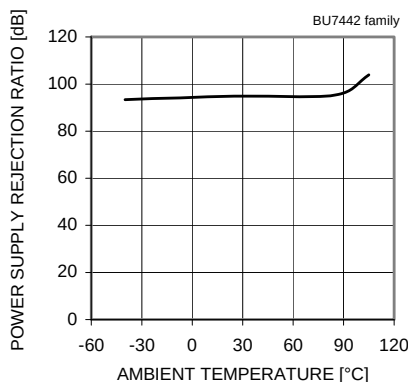


Fig.135

Power Supply Rejection Ratio
– Ambient Temperature

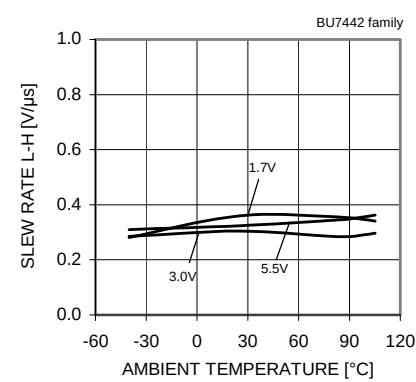


Fig.136

Slew Rate L-H – Ambient Temperature

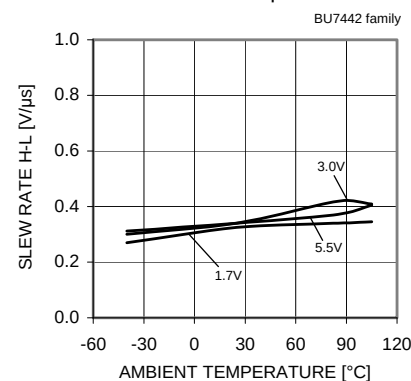


Fig.137

Slew Rate H-L – Ambient Temperature

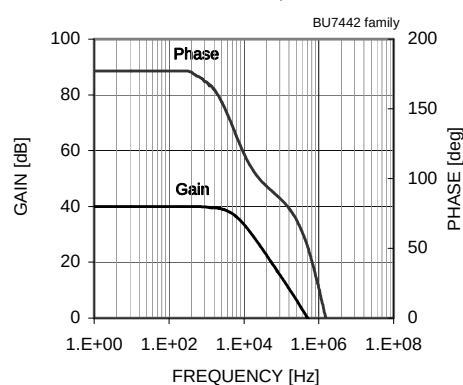


Fig.138

Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7442F/FVM/NUX: -40[°C] ~ +85[°C] BU7442S F/FVM/NUX: -40[°C] ~ +105[°C]

●Reference data (BU7444 family)

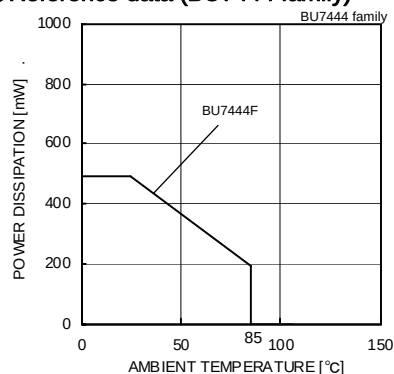


Fig.139
Derating curve

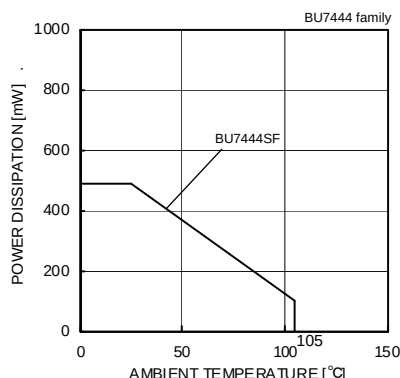


Fig.140
Derating curve

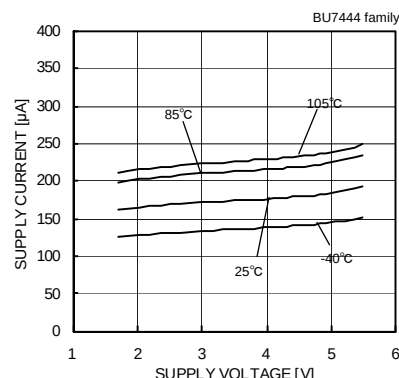


Fig.141
Supply Current – Supply Voltage

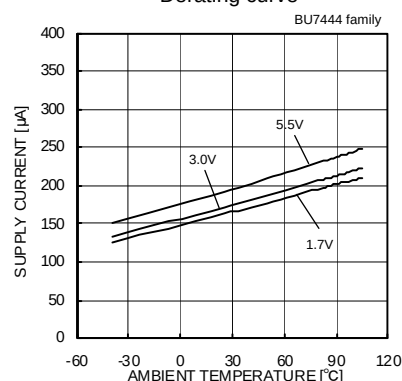


Fig.142
Supply Current – Ambient Temperature

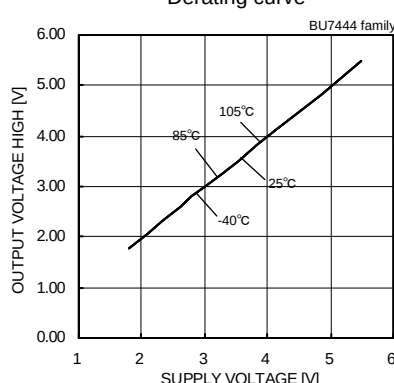


Fig.143
Output Voltage High – Supply Voltage
(RL=10[kΩ])

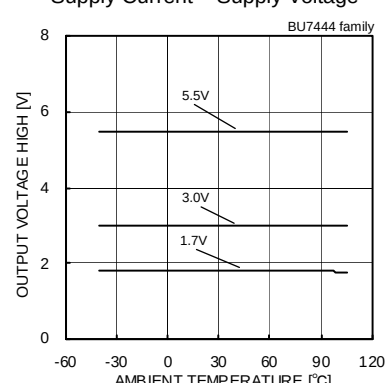


Fig.144
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

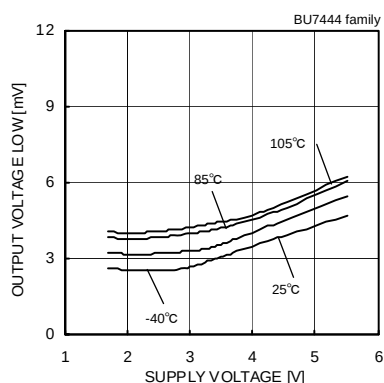


Fig.145
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

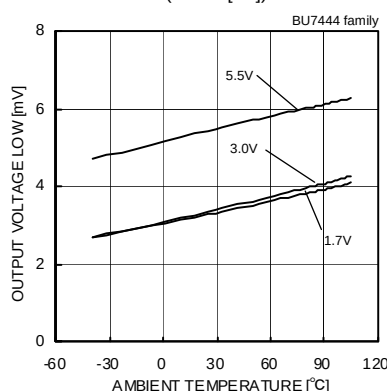


Fig.146
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

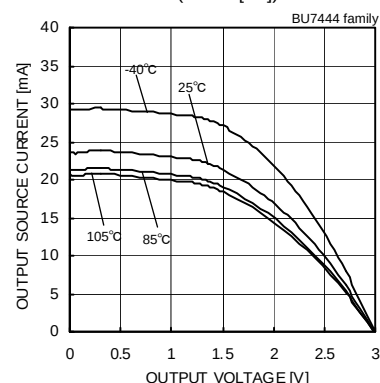


Fig.147
Output Source Current – Output Voltage
(VDD=3.0[V])

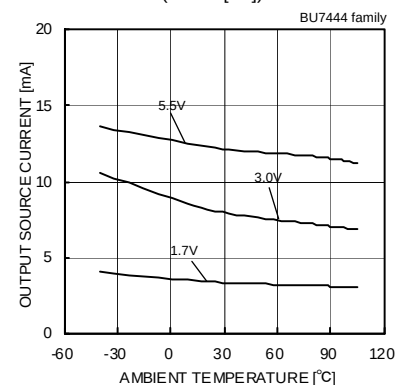


Fig.148
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

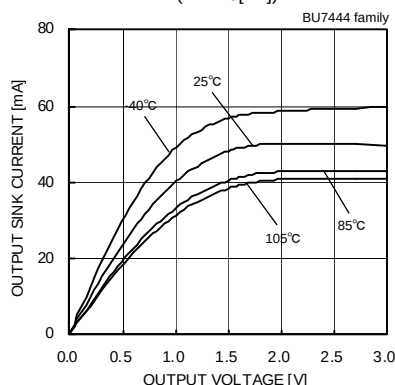


Fig.149
Output Sink Current – Output Voltage
(VDD=3[V])

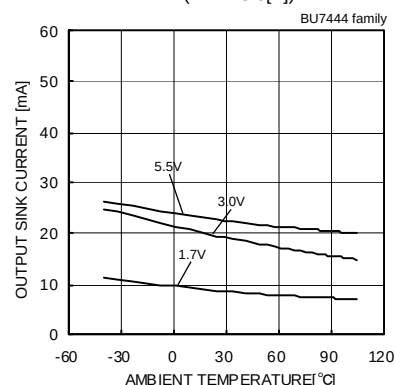


Fig.150
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*)The above data is ability value of sample, it is not guaranteed. BU7444F/FVM/NUX: -40[°C] ~ +85[°C] BU7444S F/FVM/NUX: -40[°C] ~ +105[°C]

●Reference data (BU7444 family)

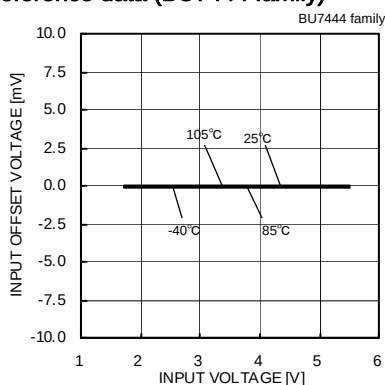


Fig.151
Input Offset Voltage – Supply Voltage
($V_{cm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

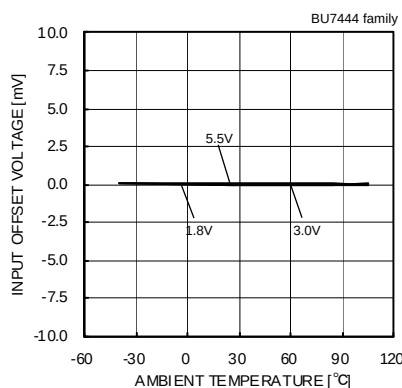


Fig.152
Input Offset Voltage – Ambient Temperature
($V_{cm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

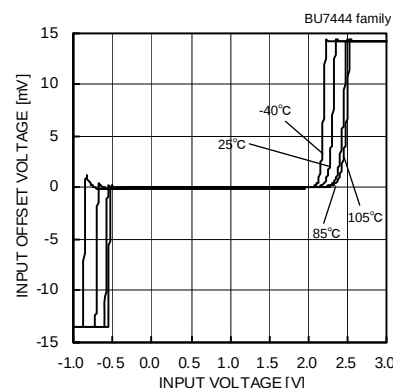


Fig.153
Input Offset Voltage – Input Voltage
($V_{DD} = 3[V]$)

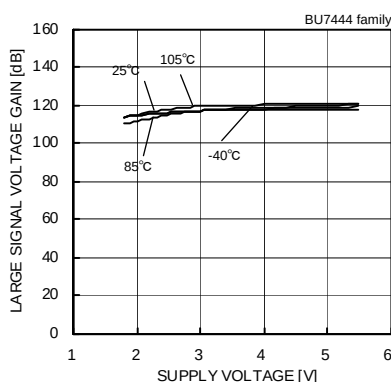


Fig.154
Large Signal Voltage Gain
– Supply Voltage

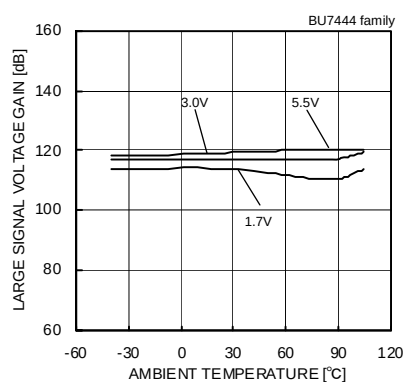


Fig.155
Large Signal Voltage Gain
– Ambient Temperature

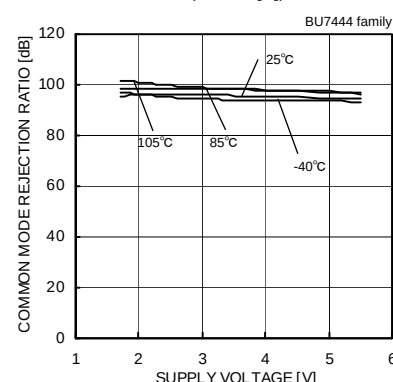


Fig.156
Common Mode Rejection Ratio
– Supply Voltage

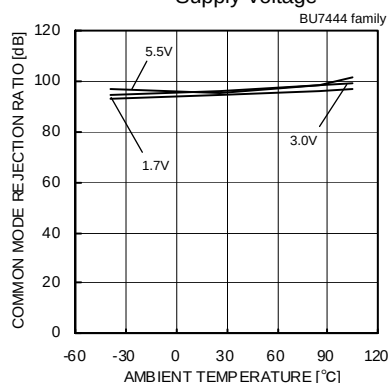


Fig.157
Common Mode Rejection Ratio
– Ambient Temperature

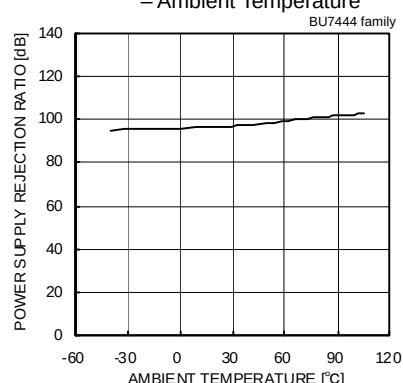


Fig.158
Power Supply Rejection Ratio
– Ambient Temperature

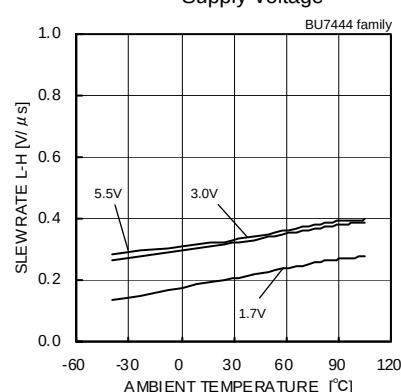


Fig.159
Slew Rate L-H – Ambient Temperature

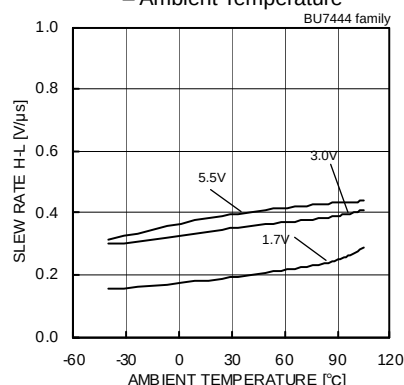


Fig.160
Slew Rate H-L – Ambient Temperature

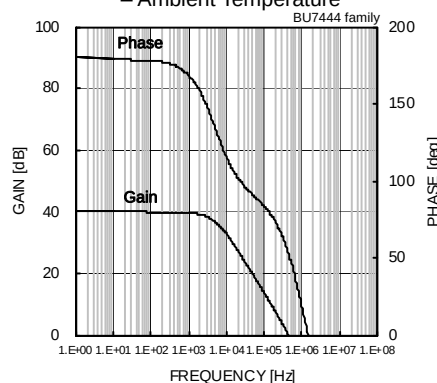


Fig.161
Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7444F/FVM/NUX: -40[°C] ~ +85[°C] BU7444S F/FVM/NUX: -40[°C] ~ +105[°C]

●Reference data (BU7445 family)

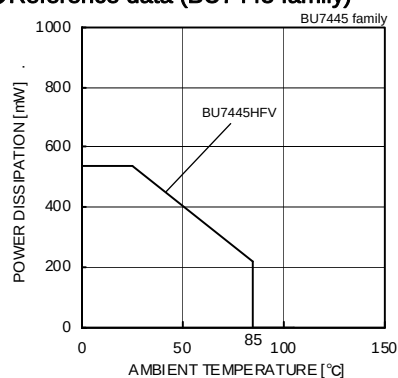


Fig.162
Derating curve

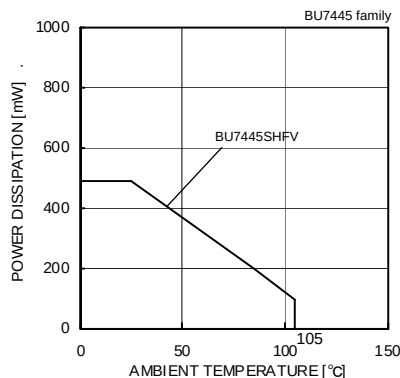


Fig.163
Derating curve

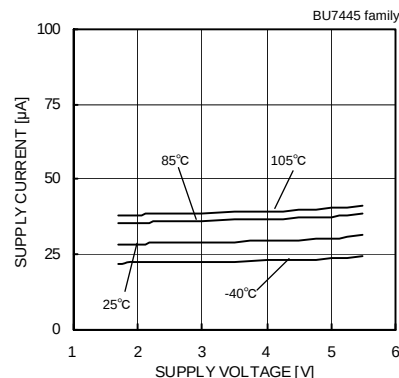


Fig.164
Supply Current – Supply Voltage

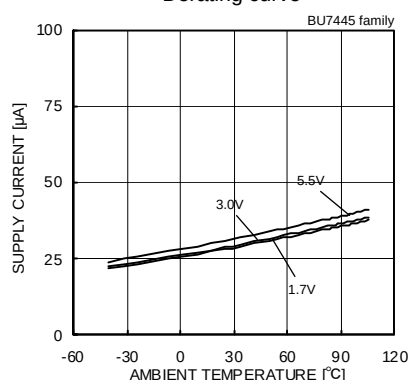


Fig.165
Supply Current – Ambient Temperature

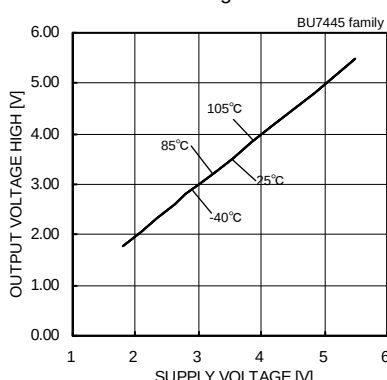


Fig.166
Output Voltage High – Supply Voltage
($R_L=10[k\Omega]$)

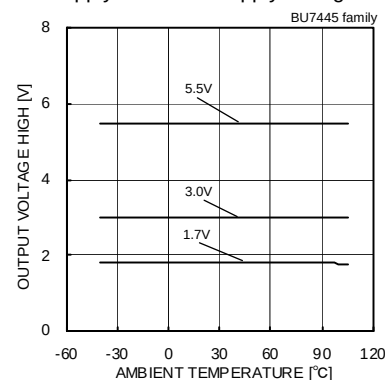


Fig.167
Output Voltage High – Ambient Temperature
($R_L=10[k\Omega]$)

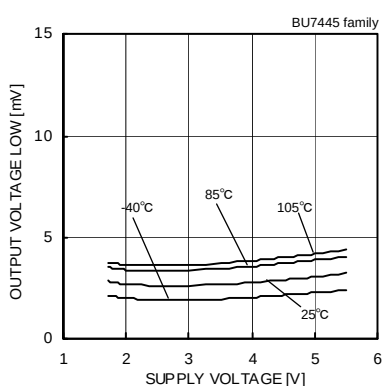


Fig.168
Output Voltage Low – Supply Voltage
($R_L=10[k\Omega]$)

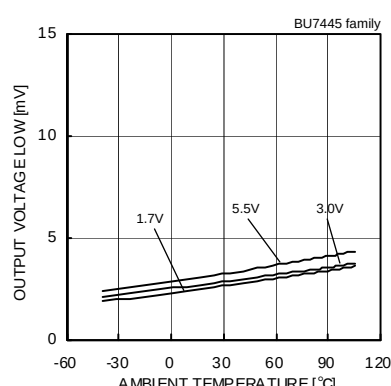


Fig.169
Output Voltage Low – Ambient Temperature
($R_L=10[k\Omega]$)

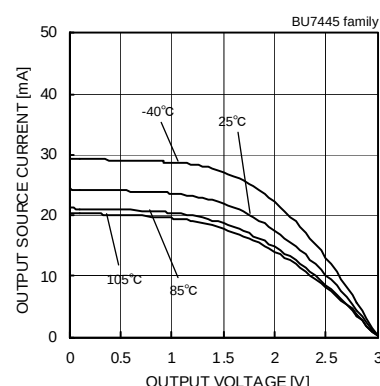


Fig.170
Output Source Current – Output Voltage
($V_{DD}=3.0[V]$)

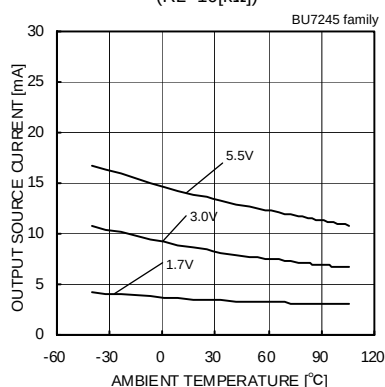


Fig.171
Output Source Current – Ambient Temperature
($V_{OUT}=V_{DD}-0.4[V]$)

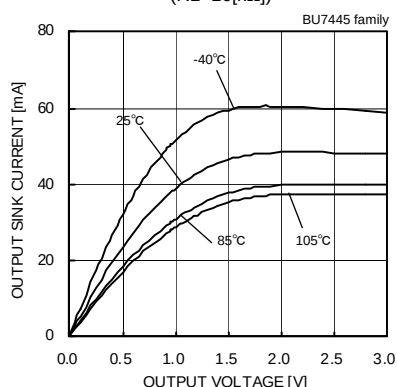


Fig.172
Output Sink Current – Output Voltage
($V_{DD}=3[V]$)

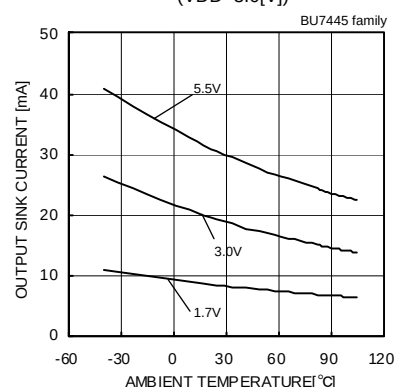


Fig.173
Output Sink Current – Ambient Temperature
($V_{OUT}=V_{SS}+0.4[V]$)

(*)The above data is ability value of sample, it is not guaranteed. BU7445HFV: -40[°C] ~ +85[°C] BU7445S HFV: -40[°C] ~ +105[°C]

●Reference data (BU7445 family)

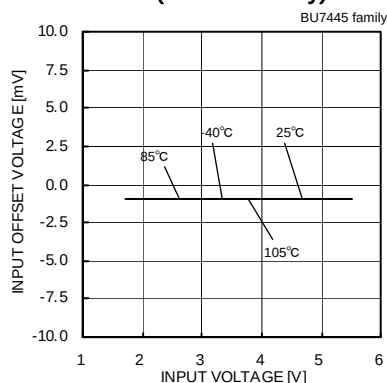


Fig.174
Input Offset Voltage – Supply Voltage
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

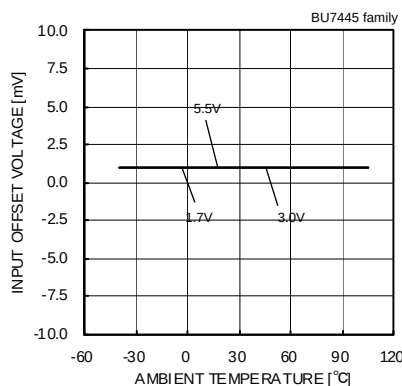


Fig.175
Input Offset Voltage – Ambient Temperature
($V_{icm} = V_{DD} - 1.2[V]$, $V_{OUT} = V_{DD}/2$)

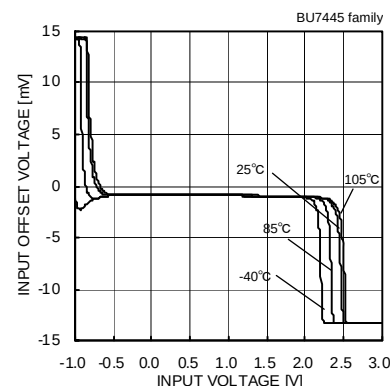


Fig.176
Input Offset Voltage – Input Voltage
($V_{DD} = 3[V]$)

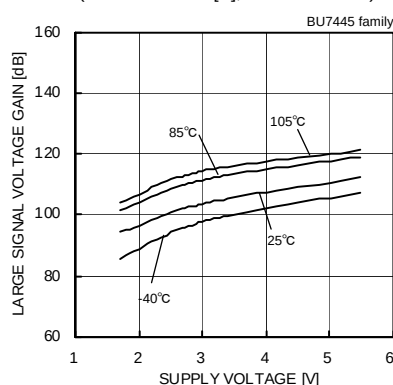


Fig.177
Large Signal Voltage Gain
– Supply Voltage

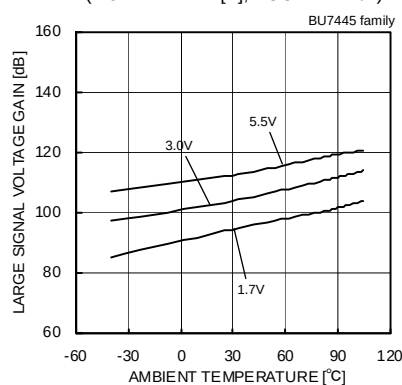


Fig.178
Large Signal Voltage Gain
– Ambient Temperature

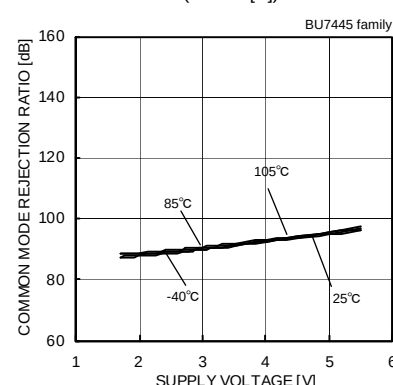


Fig.179
Common Mode Rejection Ratio
– Supply Voltage

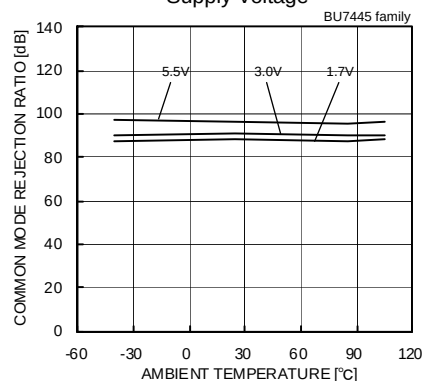


Fig.180
Common Mode Rejection Ratio
– Ambient Temperature

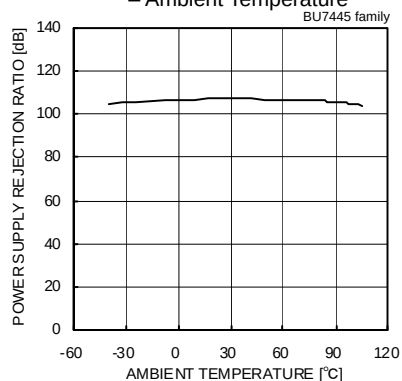


Fig.181
Power Supply Rejection Ratio
– Ambient Temperature

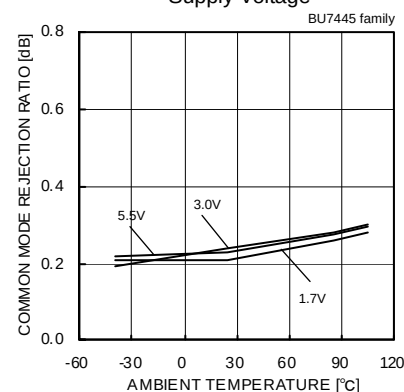


Fig.182
Slew Rate L-H – Ambient Temperature

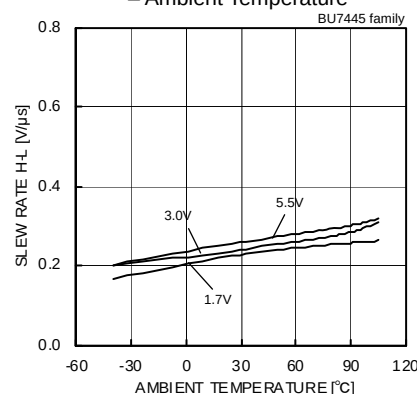


Fig.183
Slew Rate H-L – Ambient Temperature

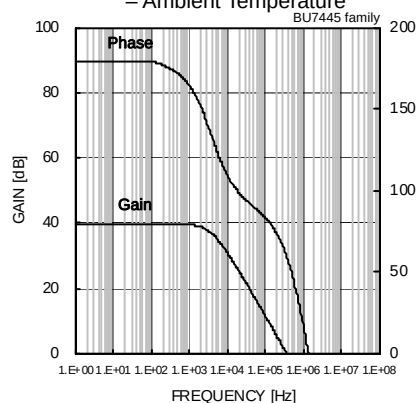


Fig.184
Gain – Frequency

(*)The above data is ability value of sample, it is not guaranteed. BU7445HFV: -40[°C] ~ +85[°C] BU7445S HFV: -40[°C] ~ +105[°C]

● Test circuit 1 NULL method

VDD, VSS, EK, Vicm Unit:[V]

Parameter	VF	S1	S2	S3	VDD	VSS	EK	Vicm	Calculation
Input Offset Voltage	VF1	ON	ON	OFF	3	0	-1.5	1.8	1
Large Signal Voltage Gain	VF2	ON	ON	ON	3	0	-0.5	0.9	2
	VF3						-2.5		
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	VF4	ON	ON	OFF	3	0	-1.5	0	3
	VF5						-1.5	1.8	
Power Supply Rejection Ratio	VF6	ON	ON	OFF	1.7	0	-0.9	0	4
	VF7				5.5				

— Calculation —

1. Input Offset Voltage (Vio)

$$V_{io} = \frac{|VF1|}{1 + R_f/R_s} [V]$$

2. Large Signal Voltage Gain(Av)

$$A_v = 20\text{Log} \frac{2 \times (1 + R_f/R_s)}{|VF2-VF3|} [dB]$$

3. Common-mode Rejection Ratio (CMRR)

$$\text{CMRR} = 20\text{Log} \frac{1.8 \times (1 + R_f/R_s)}{|VF4 - VF5|} [dB]$$

4. Power Supply Rejection Ratio (PSRR)

$$\text{PSRR} = 20\text{Log} \frac{3.8 \times (1 + R_f/R_s)}{|VF6 - VF7|} [dB]$$

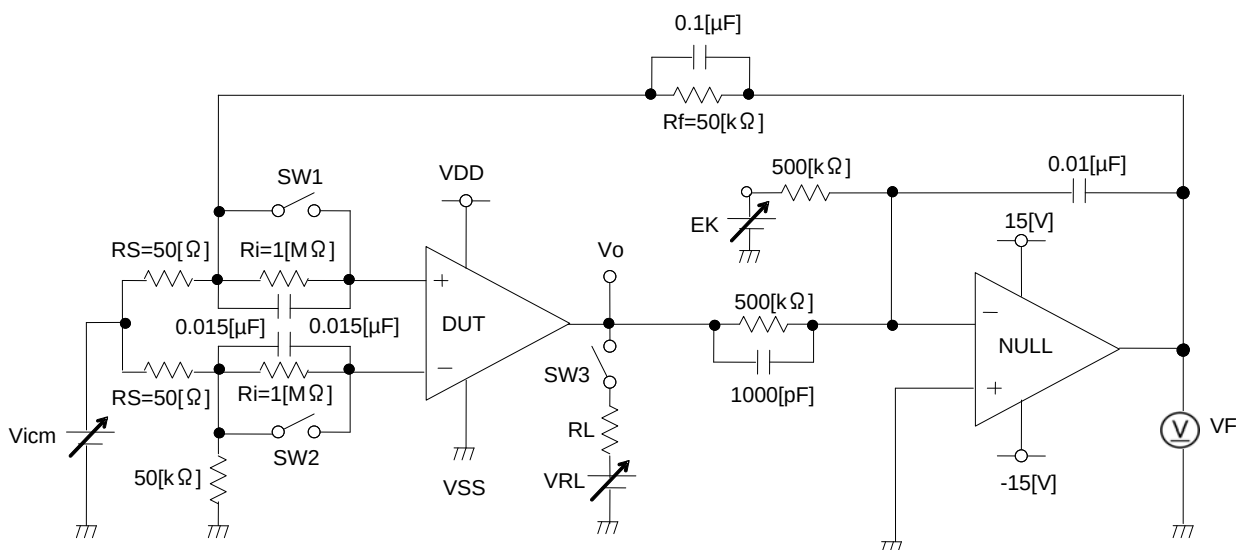


Fig.185 Test circuit 1 (one channel only)

● Test circuit 2 switch condition

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage RL=10 [kΩ]	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Maximum Frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

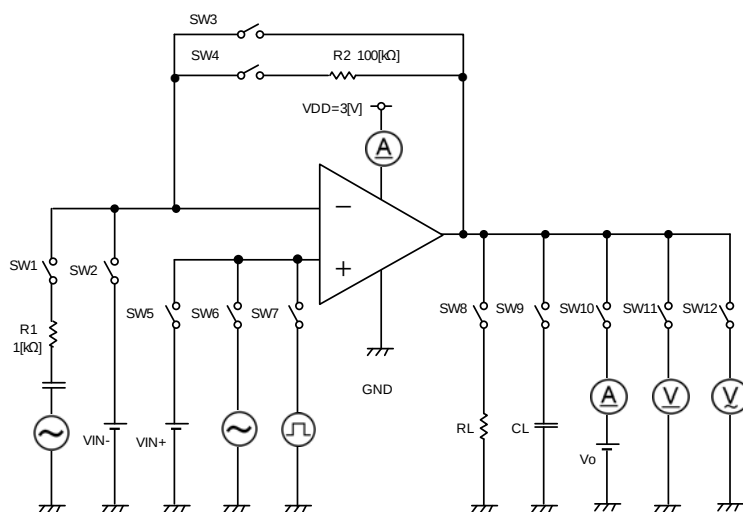


Fig.186 Test circuit 2

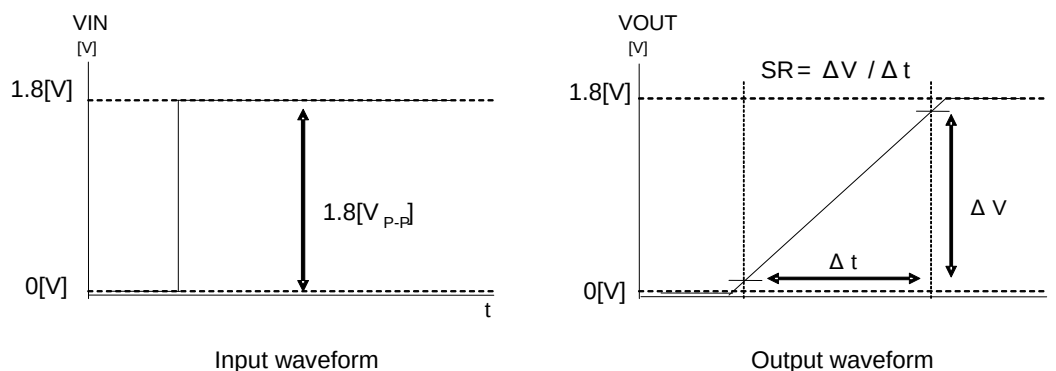


Fig.187 Slew rate input output wave

● Test circuit 3 Channel separation

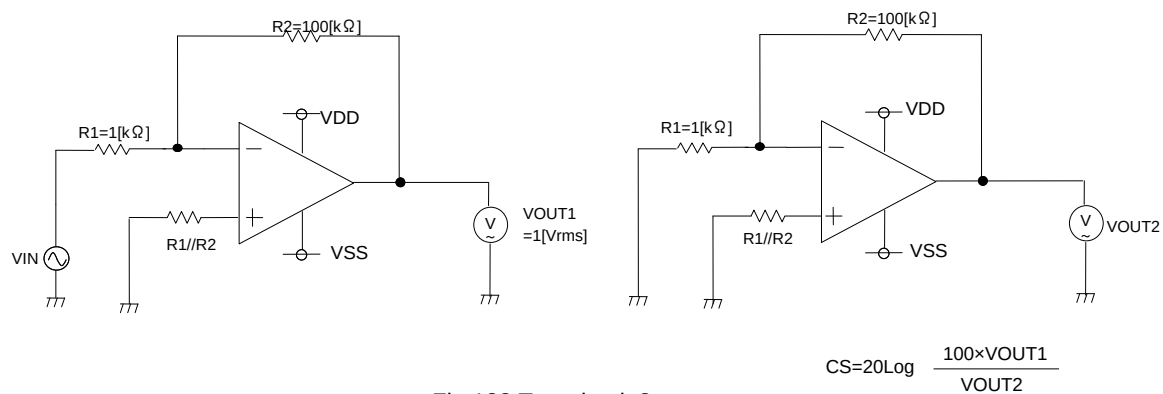


Fig.188 Test circuit 3

● Schematic diagram

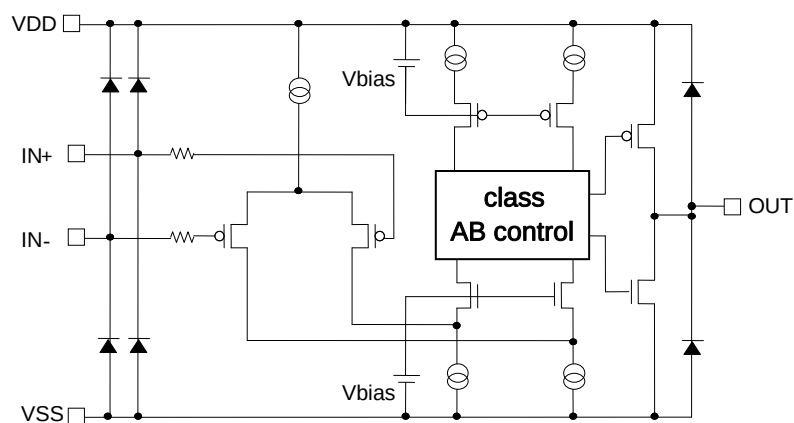
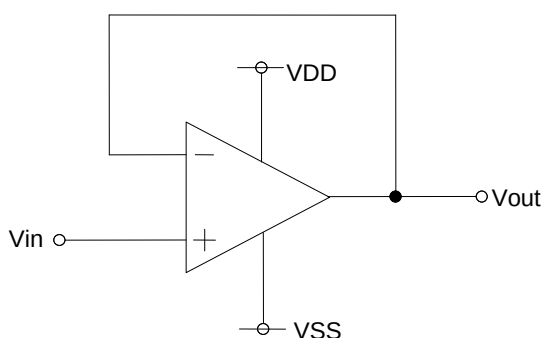


Fig.189 Schematic diagram

●Examples of circuit

○Voltage follower



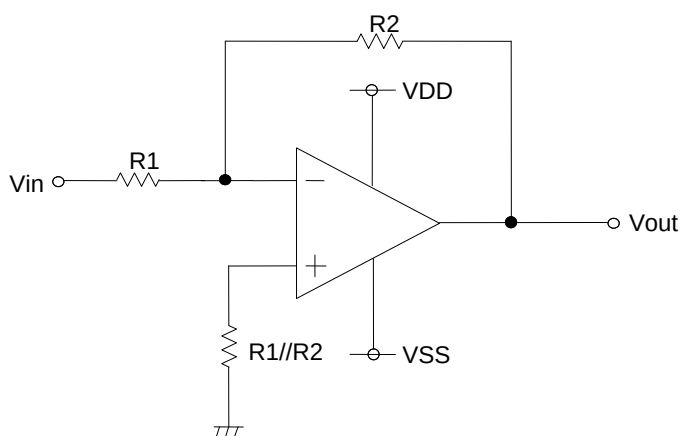
Voltage gain is 0 [dB].

This circuit controls output voltage (Vout) equal input voltage (Vin), and keeps Vout with stable because of high input impedance and low output impedance. Vout is shown next formula.

$$V_{out} = V_{in}$$

Fig.190 Voltage follower

○Inverting amplifier



For inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase reversed voltage is outputted.

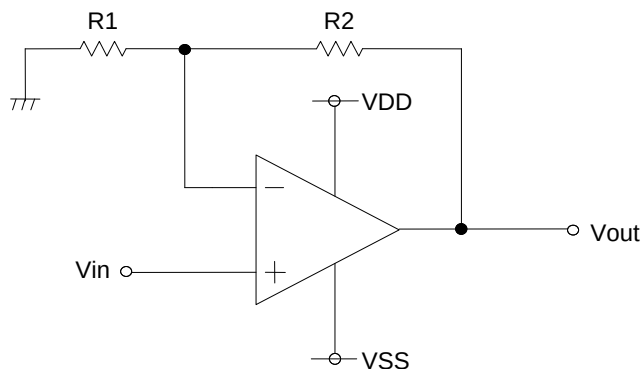
Vout is shown next formula.

$$V_{out} = -(R_2/R_1) \cdot V_{in}$$

Input impedance is R1.

Fig.191 Inverting amplifier

○Non-inverting amplifier



For non-inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase is same with Vin. Vout is shown next formula.

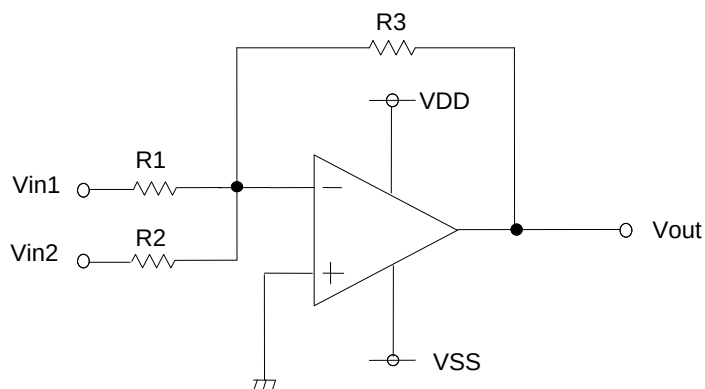
$$V_{out} = (1 + R_2/R_1) \cdot V_{in}$$

This circuit realizes high input impedance because Input impedance is operational amplifier's input Impedance.

Fig.192 Non-inverting amplifier

● Examples of circuit

○ Adder circuit



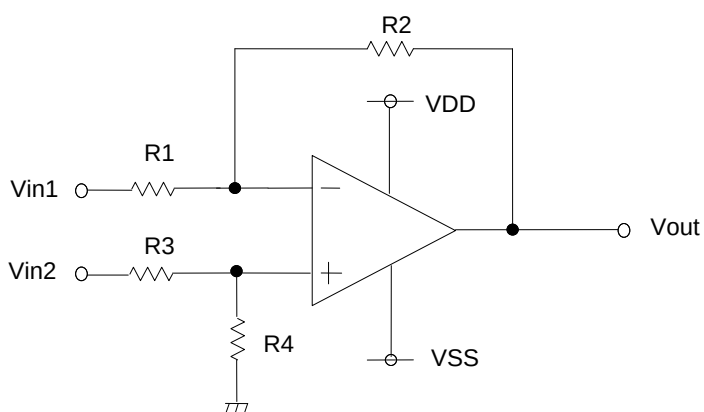
Adder circuit output the voltage that added up Input voltage. A phase of the output voltage turns over, because non-inverting circuit is used. Vout is shown next formula.

$$V_{out} = -R3(V_{in1}/R1 + V_{in2}/R2)$$

When three input voltage is as above, it connects with input through resistance like R1 and R2.

Fig.193 Adder circuit

○ Differential amplifier



Differential amplifier output the voltage that amplified a difference of input voltage. In the case of $R1=R3=R_a$, $R2=R4=R_b$ Vout is shown next formula.

$$V_{out} = -R_b/R_a(V_{in1} - V_{in2})$$

Fig.194 Differential amplifier

●Description of electrical characteristics

Described here are the terms of electric characteristics used in this technical note. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Power supply voltage (VDD/VSS)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (Vid)

Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range (Vicm)

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assures normal operation of IC. When normal Operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation (Pd)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25°C(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package.

2. Electrical characteristics item

2.1 Input offset voltage (Vio)

Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 [V].

2.2 Input offset current (Iio)

Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.3 Input bias current (Ib)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Circuit current (ICC)

Indicates the IC current that flows under specified conditions and no-load steady status.

2.5 High level output voltage / Low level output voltage (VOH/VOL)

Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into high-level output voltage and low-level output voltage. High-level output voltage indicates the upper limit of output voltage. Low-level output voltage indicates the lower limit.

2.6 Large signal voltage gain (AV)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.

$$A_v = (\text{Output voltage fluctuation}) / (\text{Input offset fluctuation})$$

2.7 Input common-mode voltage range (Vicm)

Indicates the input voltage range where IC operates normally.

2.8 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.

$$CMRR = (\text{Change of Input common-mode voltage}) / (\text{Input offset fluctuation})$$

2.9 Power supply rejection ratio (PSRR)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.

$$PSRR = (\text{Change of power supply voltage}) / (\text{Input offset fluctuation})$$

2.10 Channel separation (CS)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

2.11 Slew rate (SR)

Indicates the time fluctuation ratio of voltage output when step input signal is applied.

2.12 Unity gain frequency (ft)

Indicates a frequency where the voltage gain of Op-Amp is 1.

2.13 Total harmonic distortion + Noise (THD+N)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

2.14 Input referred noise voltage (Vn)

Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

Derating curve

Power dissipation (total loss) indicates the power that can be consumed by IC at $T_a=25^{\circ}\text{C}$ (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θ_{ja} [$^{\circ}\text{C}/\text{W}$]. The temperature of IC inside the package can be estimated by this thermal resistance. Fig.195 (a) shows the model of thermal resistance of the package. Thermal resistance θ_{ja} , ambient temperature T_a , junction temperature T_j , and power dissipation P_d can be calculated by the equation below:

$$\theta_{ja} = (T_j - T_a) / P_d \quad [^{\circ}\text{C}/\text{W}] \quad \dots \dots (1)$$

Derating curve in Fig.195(b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} . Thermal resistance θ_{ja} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig.196 (c)-(h) show a derating curve for an example Ground Sense Low Voltage Operation CMOS Operational Amplifiers series.

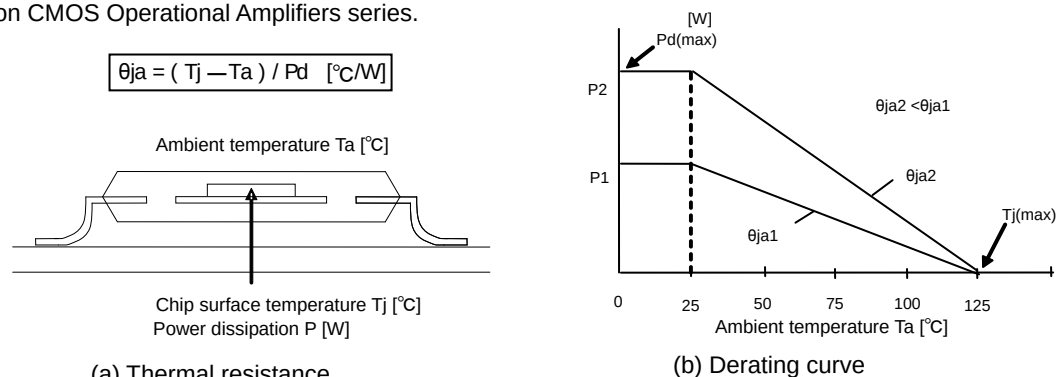
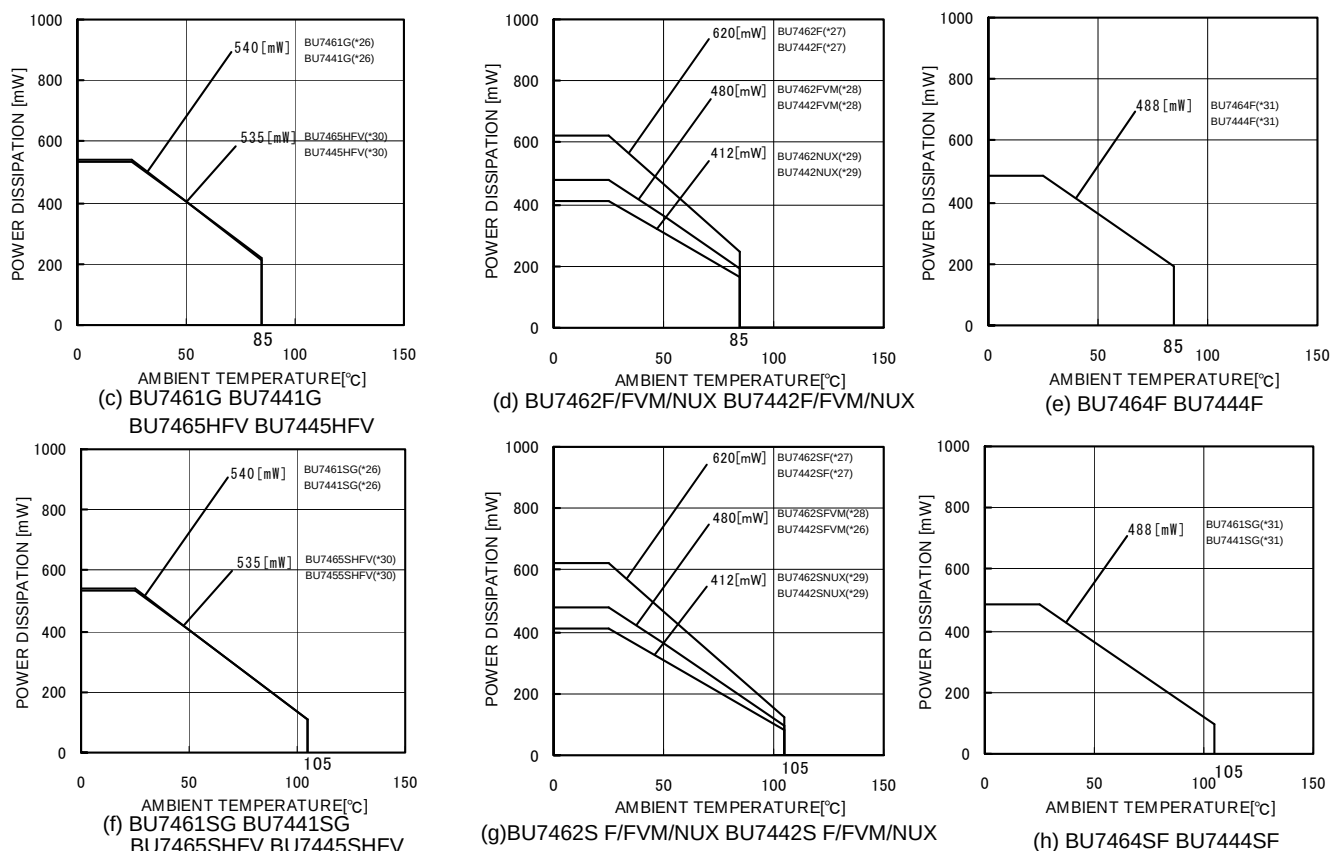


Fig.195 Thermal resistance and derating



(*26)	(*27)	(*28)	(*29)	(*30)	(*31)	Unit
5.4	6.2	4.8	4.12	5.35	4.88	[mW/°C]

When using the unit above $T_a=25^{\circ}\text{C}$, subtract the value above per degree[°C]. Permissible dissipation is the value.

When FR4 glass epoxy board 70[mm]×70[mm]×1.6[mm] (copper foil area below 3[%]) is mounted.

Fig.196 Thermal resistance and derating

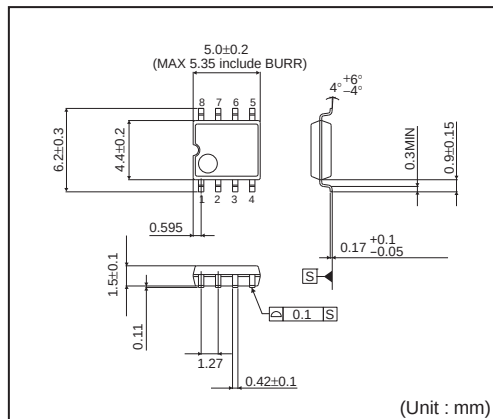
●Cautions on use

- 1) Absolute maximum ratings
Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal. However, it does not guarantee the circuit operation.
- 2) Applied voltage to the input terminal
For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage $V_{DD} + 0.3[V]$. Then, regardless of power supply voltage, $V_{SS}-0.3[V]$ can be applied to input terminals without deterioration or destruction of its characteristics.
- 3) Operating power supply (split power supply/single power supply)
The voltage comparator operates if a given level of voltage is applied between V_{DD} and V_{SS} . Therefore, the operational amplifier can be operated under single power supply or split power supply.
- 4) Power dissipation (pd)
If the IC is used under excessive power dissipation. An increase in the chip temperature will cause deterioration of the radical characteristics of IC. For example, reduction of current capability. Take consideration of the effective power dissipation and thermal design with a sufficient margin. Pd is reference to the provided power dissipation curve.
- 5) Short circuits between pins and incorrect mounting
Short circuits between pins and incorrect mounting when mounting the IC on a printed circuits board, take notice of the direction and positioning of the IC. If IC is mounted erroneously, It may be damaged. Also, when a foreign object is inserted between output, between output and V_{DD} terminal and V_{SS} terminal which causes short circuit, the IC may be damaged.
- 6) Using under strong electromagnetic field
Be careful when using the IC under strong electromagnetic field because it may malfunction.
- 7) Usage of IC
When stress is applied to the IC through warp of the printed circuit board, The characteristics may fluctuate due to the piezo effect. Be careful of the warp of the printed circuit board.
- 8) Testing IC on the set board
When testing IC on the set board, in cases where the capacitor is connected to the low impedance, make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress. When removing IC from the set board, it is essential to cut supply voltage. As a countermeasure against the static electricity, observe proper grounding during fabrication process and take due care when carrying and storage it.
- 9) The IC destruction caused by capacitive load
The transistors in circuits may be damaged when V_{DD} terminal and V_{SS} terminal is shorted with the charged output terminal capacitor. When IC is used as a operational amplifier or as an application circuit, where oscillation is not activated by an output capacitor, the output capacitor must be kept below $0.1[\mu F]$ in order to prevent the damage mentioned above.
- 10) Latch up
Be careful of input voltage that exceed the V_{DD} and V_{SS} . When CMOS device have sometimes occur latch up operation. And protect the IC from abnormaly noise
- 11) Decoupling capacitor
Insert the decoupling capacitance between V_{DD} and V_{SS} , for stable operation of operational amplifier.

●Ordering part number

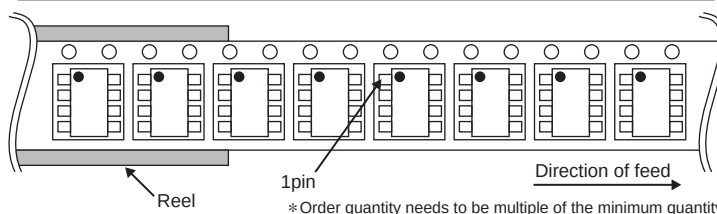
B	U	7	4	6	2	S	F	V	M	-	T	R
Part No.		Part No.					Package				Packaging and forming specification	
		• 7461 7461S • 7464 7464S • 7441 7441S • 7444 7444S • 7462 7462S • 7465 7465S • 7442 7442S • 7445 7445S					G : SSOP5 F : SOP8, SOP14 FVM : MSOP8 NUX : VSON008X2030 HFV : HVSOF5				E2: Embossed tape and reel (SOP8/SOP14) TR: Embossed tape and reel (SSOP5/MSOP8/VSON008X2030/HVSOF5)	

SOP8

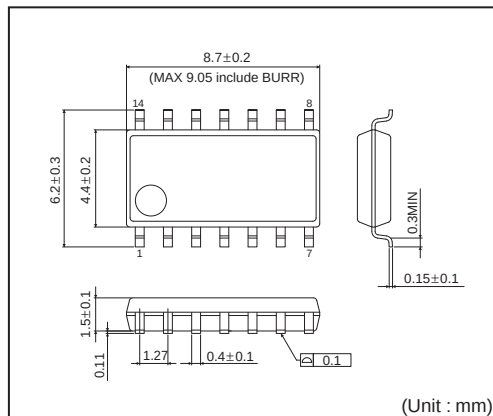


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

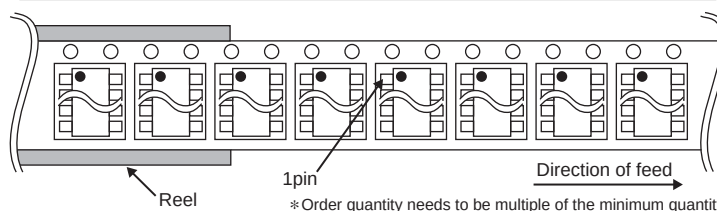


SOP14

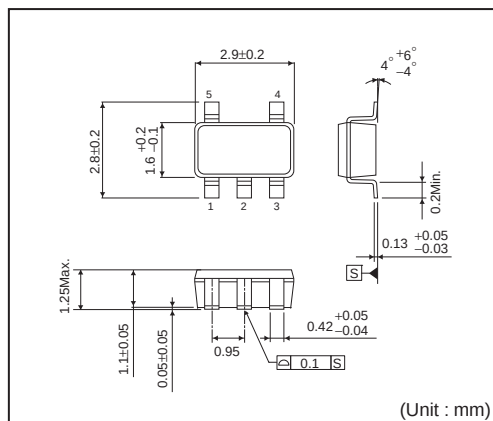


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

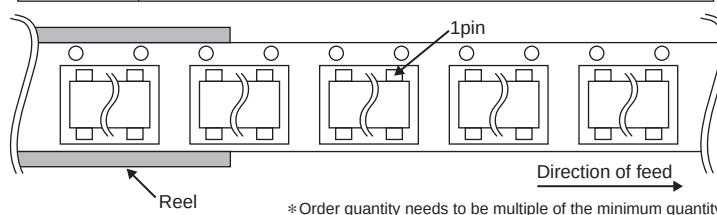


SSOP5



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

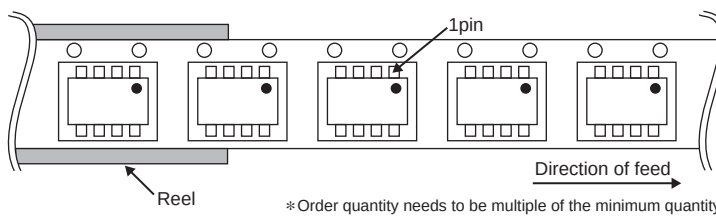


Technical drawing of a 1-pin connector showing dimensions in mm.

Top View:

- Overall width: 2.9 ± 0.1 (MAX 3.25 include BURR)
- Overall height: 4.0 ± 0.2
- Pin 1 location: 2.8 ± 0.1 from the left edge.
- Pin 1 diameter: 0.475
- Pin 1 to Pin 2 distance: 0.145
- Pin 2 to Pin 3 distance: 0.08 ± 0.05
- Pin 3 to Pin 4 distance: 0.08 ± 0.05
- Pin 4 to Pin 5 distance: 0.08 ± 0.05
- Pin 5 to Pin 6 distance: 0.08 ± 0.05
- Pin 6 to Pin 7 distance: 0.08 ± 0.05
- Pin 7 to Pin 8 distance: 0.08 ± 0.05
- Pin 8 to Pin 9 distance: 0.08 ± 0.05
- Pin 9 to Pin 10 distance: 0.08 ± 0.05
- Pin 10 to Pin 11 distance: 0.08 ± 0.05
- Pin 11 to Pin 12 distance: 0.08 ± 0.05
- Pin 12 to Pin 13 distance: 0.08 ± 0.05
- Pin 13 to Pin 14 distance: 0.08 ± 0.05
- Pin 14 to Pin 15 distance: 0.08 ± 0.05
- Pin 15 to Pin 16 distance: 0.08 ± 0.05
- Pin 16 to Pin 17 distance: 0.08 ± 0.05
- Pin 17 to Pin 18 distance: 0.08 ± 0.05
- Pin 18 to Pin 19 distance: 0.08 ± 0.05
- Pin 19 to Pin 20 distance: 0.08 ± 0.05
- Pin 20 to Pin 21 distance: 0.08 ± 0.05
- Pin 21 to Pin 22 distance: 0.08 ± 0.05
- Pin 22 to Pin 23 distance: 0.08 ± 0.05
- Pin 23 to Pin 24 distance: 0.08 ± 0.05
- Pin 24 to Pin 25 distance: 0.08 ± 0.05
- Pin 25 to Pin 26 distance: 0.08 ± 0.05
- Pin 26 to Pin 27 distance: 0.08 ± 0.05
- Pin 27 to Pin 28 distance: 0.08 ± 0.05
- Pin 28 to Pin 29 distance: 0.08 ± 0.05
- Pin 29 to Pin 30 distance: 0.08 ± 0.05
- Pin 30 to Pin 31 distance: 0.08 ± 0.05
- Pin 31 to Pin 32 distance: 0.08 ± 0.05
- Pin 32 to Pin 33 distance: 0.08 ± 0.05
- Pin 33 to Pin 34 distance: 0.08 ± 0.05
- Pin 34 to Pin 35 distance: 0.08 ± 0.05
- Pin 35 to Pin 36 distance: 0.08 ± 0.05
- Pin 36 to Pin 37 distance: 0.08 ± 0.05
- Pin 37 to Pin 38 distance: 0.08 ± 0.05
- Pin 38 to Pin 39 distance: 0.08 ± 0.05
- Pin 39 to Pin 40 distance: 0.08 ± 0.05
- Pin 40 to Pin 41 distance: 0.08 ± 0.05
- Pin 41 to Pin 42 distance: 0.08 ± 0.05
- Pin 42 to Pin 43 distance: 0.08 ± 0.05
- Pin 43 to Pin 44 distance: 0.08 ± 0.05
- Pin 44 to Pin 45 distance: 0.08 ± 0.05
- Pin 45 to Pin 46 distance: 0.08 ± 0.05
- Pin 46 to Pin 47 distance: 0.08 ± 0.05
- Pin 47 to Pin 48 distance: 0.08 ± 0.05
- Pin 48 to Pin 49 distance: 0.08 ± 0.05
- Pin 49 to Pin 50 distance: 0.08 ± 0.05
- Pin 50 to Pin 51 distance: 0.08 ± 0.05
- Pin 51 to Pin 52 distance: 0.08 ± 0.05
- Pin 52 to Pin 53 distance: 0.08 ± 0.05
- Pin 53 to Pin 54 distance: 0.08 ± 0.05
- Pin 54 to Pin 55 distance: 0.08 ± 0.05
- Pin 55 to Pin 56 distance: 0.08 ± 0.05
- Pin 56 to Pin 57 distance: 0.08 ± 0.05
- Pin 57 to Pin 58 distance: 0.08 ± 0.05
- Pin 58 to Pin 59 distance: 0.08 ± 0.05
- Pin 59 to Pin 60 distance: 0.08 ± 0.05
- Pin 60 to Pin 61 distance: 0.08 ± 0.05
- Pin 61 to Pin 62 distance: 0.08 ± 0.05
- Pin 62 to Pin 63 distance: 0.08 ± 0.05
- Pin 63 to Pin 64 distance: 0.08 ± 0.05
- Pin 64 to Pin 65 distance: 0.08 ± 0.05
- Pin 65 to Pin 66 distance: 0.08 ± 0.05
- Pin 66 to Pin 67 distance: 0.08 ± 0.05
- Pin 67 to Pin 68 distance: 0.08 ± 0.05
- Pin 68 to Pin 69 distance: 0.08 ± 0.05
- Pin 69 to Pin 70 distance: 0.08 ± 0.05
- Pin 70 to Pin 71 distance: 0.08 ± 0.05
- Pin 71 to Pin 72 distance: 0.08 ± 0.05
- Pin 72 to Pin 73 distance: 0.08 ± 0.05
- Pin 73 to Pin 74 distance: 0.08 ± 0.05
- Pin 74 to Pin 75 distance: 0.08 ± 0.05
- Pin 75 to Pin 76 distance: 0.08 ± 0.05
- Pin 76 to Pin 77 distance: 0.08 ± 0.05
- Pin 77 to Pin 78 distance: 0.08 ± 0.05
- Pin 78 to Pin 79 distance: 0.08 ± 0.05
- Pin 79 to Pin 80 distance: 0.08 ± 0.05
- Pin 80 to Pin 81 distance: 0.08 ± 0.05
- Pin 81 to Pin 82 distance: 0.08 ± 0.05
- Pin 82 to Pin 83 distance: 0.08 ± 0.05
- Pin 83 to Pin 84 distance: 0.08 ± 0.05
- Pin 84 to Pin 85 distance: 0.08 ± 0.05
- Pin 85 to Pin 86 distance: 0.08 ± 0.05
- Pin 86 to Pin 87 distance: 0.08 ± 0.05
- Pin 87 to Pin 88 distance: 0.08 ± 0.05
- Pin 88 to Pin 89 distance: 0.08 ± 0.05
- Pin 89 to Pin 90 distance: 0.08 ± 0.05
- Pin 90 to Pin 91 distance: 0.08 ± 0.05
- Pin 91 to Pin 92 distance: 0.08 ± 0.05
- Pin 92 to Pin 93 distance: 0.08 ± 0.05
- Pin 93 to Pin 94 distance: 0.08 ± 0.05
- Pin 94 to Pin 95 distance: 0.08 ± 0.05
- Pin 95 to Pin 96 distance: 0.08 ± 0.05
- Pin 96 to Pin 97 distance: 0.08 ± 0.05
- Pin 97 to Pin 98 distance: 0.08 ± 0.05
- Pin 98 to Pin 99 distance: 0.08 ± 0.05
- Pin 99 to Pin 100 distance: 0.08 ± 0.05
- Pin 100 to Pin 101 distance: 0.08 ± 0.05
- Pin 101 to Pin 102 distance: 0.08 ± 0.05
- Pin 102 to Pin 103 distance: 0.08 ± 0.05
- Pin 103 to Pin 104 distance: 0.08 ± 0.05
- Pin 104 to Pin 105 distance: 0.08 ± 0.05
- Pin 105 to Pin 106 distance: 0.08 ± 0.05
- Pin 106 to Pin 107 distance: 0.08 ± 0.05
- Pin 107 to Pin 108 distance: 0.08 ± 0.05
- Pin 108 to Pin 109 distance: 0.08 ± 0.05
- Pin 109 to Pin 110 distance: 0.08 ± 0.05
- Pin 110 to Pin 111 distance: 0.08 ± 0.05
- Pin 111 to Pin 112 distance: 0.08 ± 0.05
- Pin 112 to Pin 113 distance: 0.08 ± 0.05
- Pin 113 to Pin 114 distance: 0.08 ± 0.05
- Pin 114 to Pin 115 distance: 0.08 ± 0.05
- Pin 115 to Pin 116 distance: 0.08 ± 0.05
- Pin 116 to Pin 117 distance: 0.08 ± 0.05
- Pin 117 to Pin 118 distance: 0.08 ± 0.05
- Pin 118 to Pin 119 distance: 0.08 ± 0.05
- Pin 119 to Pin 120 distance: 0

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



Technical drawing of a mechanical part, showing three views: front, top, and side. The drawing includes dimensions and tolerances in millimeters (mm).

Front View Dimensions:

- Overall width: 1.6 ± 0.05
- Slot width: 1.0 ± 0.05
- Slot depth: 1.24 ± 0.05 (MAX 1.28 include BURR)
- Slot bottom width: 0.05
- Slot bottom depth: 0.05

Top View Dimensions:

- Overall width: 0.8
- Slot width: 0.3
- Slot depth: 0.91
- Slot bottom width: 0.43
- Slot bottom depth: 0.3
- Slot bottom width: 0.3
- Slot bottom depth: 0.1

Side View Dimensions:

- Overall height: 0.13 ± 0.05
- Slot depth: 0.2 MAX

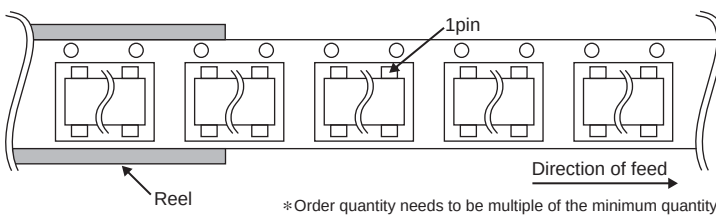
Other Dimensions and Tolerances:

- Overall height: 0.6 MAX
- Slot depth: 0.02
- Slot bottom width: 0.5
- Slot bottom depth: 0.1
- Slot bottom width: 0.22 ± 0.05
- Slot bottom depth: 0.08

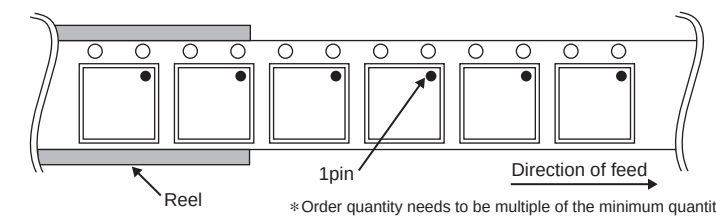
Notes:

- (MAX 1.28 include BURR)
- (Unit : mm)

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

[illegible]

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand



Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.



Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

<http://www.rohm.com/contact/>

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru

www.lifeelectronics.ru