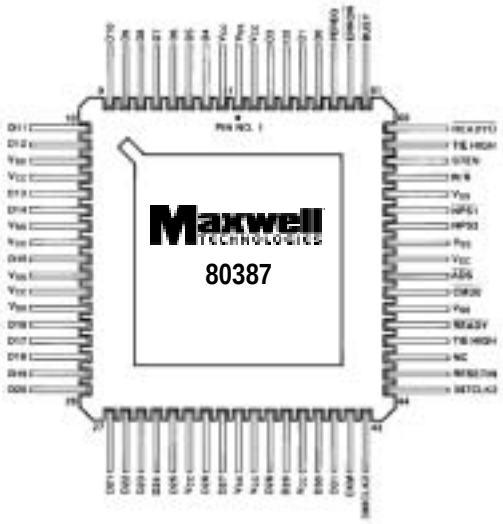
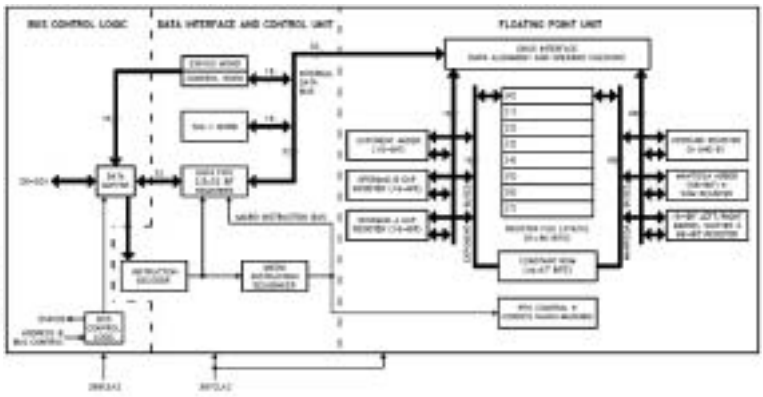
80387DX
Math Coprocessor





Logic Diagram

FEATURES:

- 80-Bit numeric processor
- RAD-PAK® radiation hardened against natural space radiation
- Total dose hardness:
  - > 100 krad (Si)
  - dependant upon space mission
- Single Event Effects:
  - SEU Threshold is ~ 3.38 MeV/mg/cm^2
  - SEL Threshold = 37.1 - 59.9 MeV/mg/cm^2
- Package: 68-pin RAD-PA® quad flat pack
- Eight 80-bit numeric registers, usable as individual addressable general registers or as a register stack
- Data types include:
  - 32-, 64-, 80-bit floating point
  - 32-, 64-bit integers
  - 18-digit BCD operands
- 5 V Only power
- Built-in exception handling
- Upward object code compatible with All 80X87DX microprocessors
- Full-range transcendental operations for SINE, COSINE, TANGENT, ARCTANGENT and LOGARITHM

DESCRIPTION:

Maxwell's 80387DX high speed microcircuit features a greater than 100 kilorad (Si) total dose tolerance. Using Maxwell's radiation hardened RAD-PAK® packaging technology, the 80387DX is a high-performance numerics processor that extends the 80386DX architecture with floating point, extended integer and BCD data types. The computing system fully conforms to the ANSI/IEEE floating-point standard. Using a numerics oriented architecture, the 80387DX adds over seventy mnemonics to the 80386DX instruction set, making the 80386DX/80387DX a complete solution for high-performance numerics processing.

Maxwell Technologies' patented RAD-PAK packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 12, 19, 21, 35, 49, 53, 56	V_{SS}	Ground
2, 13, 20, 32, 36, 39, 52, 68	V_{CC}	Positive Power Supply
3-11, 18, 22-31, 33, 34, 37, 38, 40, 41, 64-67	D4-D12, D15, D16-25, D26, D27, D28, D29, D30, D31, D0-D3	Data Bus
42	CKM	Clock Mode
43	386CLK2	386 CPU Clock 2
44	387CLK2	387 MCP Clock 2
45	RESETIN	System Reset
46	NC	Not Connected
47 59	Tie High	Tie High
48	$\overline{\text{READY}}$	Bus Ready Input
50	$\overline{\text{CMD0}}$	Command
51	$\overline{\text{ADS}}$	Address Strobe
54	NPS2	MCP Select #2
55	$\overline{\text{NPS1}}$	MCP Select #1
57	W/$\overline{\text{R}}$	Write/Read
58	STEN	Status Enable
60	$\overline{\text{READYO}}$	Ready Output
61	$\overline{\text{BUSY}}$	Busy Status
62	$\overline{\text{ERROR}}$	Error Status
63	PEREQ	Processor Extension Request

TABLE 2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage, any pin, with respect to Ground	V_{CC}	-0.5	V_{CC}+0.5	V
Power Dissipation	P_D	--	1.5	W
Storage Temperature Range	T_S	-65	150	˚C
Operating Temperature Range	T_A	-55	125	˚C
Lead Temperature (soldering 10 seconds)		--	260	˚C

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{LI}	± 1.5 µA
I_{LO}	±1.5 µA
I_{CC} CLK2 = 32 MHz	±25 mA
I_{CC} CLK2 = 50 MHz	±39 mA

TABLE 4. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	4.75	5.25	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC} +0.3	V
Operating Temperature	T_A	-55	125	°C

TABLE 5. 80387DX DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V TO 5.25V; T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Input Low Voltage	V_{IL}[1]		-- --	0.8 --	V
Input High Voltage	V_{IH}[1]		2.0	--	V
386 CLK2 Input Low Voltage	V_{CL}		--	0.8	V
386 CLK2 Input High Voltage	V_{CH}		3.7	--	V
Output Low Voltage	V_{OL}	I_{OL} = 4 mA, D0-D31, I_{OL} = 2.5 mA READYO , ERROR, BUSY, PEREQ	--	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA, D0-D31, I_{OH} = -0.6 mA READYO, READYO, ERROR, BUSY, PEREQ	2.4	--	V
Input Leakage Current	I_{LI}	$0V \le V_{IN} \le V_{CC}$		±15	µA
Output Leakage Current	I_{LO}	$0.45V \le V_{OUT} \le V_{CC}$	--	±15	µA
Power Supply Current	I_{CC}	CLK2 = 32 MHz CLK2 = 40 MHz CLK2 = 50 MHz[2]	-- -- --	250 310 390	mA
Input Capacitance[3]	C_{IN}	F_C = 1 MHz	--	10	pF
Output Capacitance[3]	C_O	F_C = 1 MHz	--	12	pF
CLK2 Capacitance[3]	C_{CLK}	F_C = 1 MHz	--	20	pF

1. This parameter is for all inputs, including 387CLK2 but excluding 386CLK2.
2. Icc is measured at steady state, maximum capacitive loading on the outputs, and worst-case DC level at the inputs; 386CLK2 at the same frequency as 387CLK2.
3. Guaranteed By Design

TABLE 6. 80387DX COMBINATIONS OF BUS INTERFACE AND EXECUTION SPEEDS

(V_{CC} = 4.75V TO 5.25V; T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Bus INterface Unit					MHz
-16			16	--	
-20			20	--	
-25			25	--	
Execution Unit					MHz
-16			16	--	
-20			20	--	
-25			25	--	

TABLE 7. 80387DX TIMING REQUIREMENTS OF THE EXECUTION UNIT

(V_{CC} = 4.75V TO 5.25V; T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
387CLK2 Period[1]	t_1	At 2V			ns
-16			31	125	
-20			25	125	
-25			20	125	
387CLK2 High Time	t_{2a}	At 2V			ns
-16			9	--	
-20			8	--	
-25			7	--	
387CLK2 High Time[1]	t_{2b}	At 3.7V			ns
-16			5	--	
-20			5	--	
-25			4	--	
387CLK2 Low Time	t_{3a}	At 2V			ns
-16			9	--	
-20			8	--	
-25			7	--	
387CLK2 Low Time[1]	t_{3b}	At 0.8V			ns
-16			7	--	
-20			6	--	
-25			5	--	
387CLK2 Fall Time[1]	t_4	At 3.7V to 0.8V			ns
-16			--	8	
-20			--	8	
-25			--	7	
387CLK2 Rise Time[1]	t_5	At 0.8V to 3.7V			ns
-16			--	8	
-20			--	8	
-25			--	7	

1. Guaranteed By Design

TABLE 8. 80387DX TIMING REQUIREMENTS OF THE BUS INTERFACE UNIT (OUTPUT TRIP LEVEL = 1.5V)

(V_{CC} = 4.75V TO 5.25V; T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
386CLK2 Period[1]	At 2.0V	t_1			ns
-16			31	125	
-20			25	125	
-25			20	125	
386CLK2 High Time	At 2.0V	t_{2a}			ns
-16			9	--	
-20			8	--	
-25			7	--	
386CLK2 High Time1	At 3.7V	t_{2b}			ns
-16			5	--	
-20			5	--	
-25			4	--	
386CLK2 Low Time	At 2V	t_{3a}			ns
-16			9	--	
-20			8	--	
-25			7	--	
386CLK2 Low Time[1]	At 0.8V	t_{3b}			ns
-16			7	--	
-20			6	--	
-25			5	--	
386CLK2 Fall Time[1]	At 3.7V to 0.8V	t_4			ns
-16			--	8	
-20			--	8	
-25			--	7	
386CLK2 Rise Time[1]	At 0.8V to 3.7V	t_5			ns
-16			--	8	
-20			--	8	
-25			--	7	
386 CLK2/387CLK2 Ratio		--	10/16	14/10	--
$\overline{\text{READYO}}$ Out Delay	C_L = 50 pF	t_7			ns
-16			4	34	
-20			3	31	
-25			3	24	
PEREQ, $\overline{\text{ERROR}}$ Out Delay	C_L = 50 pF	t_7			ns
-16			5	34	
-20			5	34	
-25			4	33	
$\overline{\text{BUSY}}$ Out Delay	C_L = 50 pF	t_7			ns
-16			5	34	
-20			5	29	
-25			4	29	

TABLE 8. 80387DX TIMING REQUIREMENTS OF THE BUS INTERFACE UNIT (OUTPUT TRIP LEVEL = 1.5V)

(V_{CC} = 4.75V TO 5.25V; T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
D31 - D0 Out Delay	C_L = 50 pF	t_8			ns
-16			1	54	
-20			1	54	
-25			0	50	
D31 - D0 Setup Time		t_{10}	11		ns
D31 - D0 Hold Delay		t_{11}	11		ns
D31 - D0 Float Time	C_L = 50 pF[2]	t_{12}			ns
-16			6	33	
-20			6	27	
-25			5	24	
$\overline{\text{PEREQ}}$, $\overline{\text{BUSY}}$, $\overline{\text{ERROR}}$, $\overline{\text{READYO}}$ Float Time[1]	C_L = 50 pF[1]	t_{13}			ns
-16			1	60	
-20			1	50	
-25			1	40	
$\overline{\text{ADS}}$, $\overline{\text{W/R}}$ Setup Time		t_{14}			ns
-16			26	--	
-20			21	--	
-25			16	--	
$\overline{\text{ADS}}$, $\overline{\text{W/R}}$ Hold Time		t_{15}			ns
-16			5	--	
-20			5	--	
-25			4	--	
$\overline{\text{READY}}$ SetupTime		t_{16}			ns
-16			21	--	
-20			12	--	
-25			9	--	
$\overline{\text{READY}}$ Hold Time		t_{17}			ns
-16			4	--	
-20			4	--	
-25			4	--	
$\overline{\text{CMDO}}$ SetupTime		t_{16}			ns
-16			21	--	
-20			19	--	
-25			16	--	
$\overline{\text{CMDO}}$ HoldTime		t_{17}			ns
-16			2	--	
-20			4	--	
-25			4	--	
$\overline{\text{NPS1}}$, NPS2 Setup Time		t_{16}			ns
-16			21	--	
-20			19	--	
-25			16	--	

TABLE 8. 80387DX TIMING REQUIREMENTS OF THE BUS INTERFACE UNIT (OUTPUT TRIP LEVEL = 1.5V)

(V_{CC} = 4.75V TO 5.25V; T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
$\overline{\text{NPS1}}$, NPS2 Hold Time		t_{17}			ns
-16			2	--	
-20			2	--	
-25			4	--	
STEN Setup Time		t_{16}			ns
-16			21	--	
-20			21	--	
-25			15	--	
STEN Hold Time		t_{17}			ns
-16			2	--	
-20			2	--	
-25			4	--	
RESETIN Setup Time		t_{18}			ns
-16			13	--	
-20			12	--	
-25			10	--	
RESETIN Hold Time		t_{19}			ns
-16			4	--	
-20			4	--	
-25			3	--	

1. Guaranteed By Design

2. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float Delay is not tested.

TABLE 9. 80387DX TIMING REQUIREMENT OF OTHER PARAMETER

PARAMETER	SYMBOL	MIN	MAX	UNIT
RESETIN Duration	t_{30}	40		(387 CLK2)
RESETIN Inactive to First Opcode Write	t_{31}	50		(387 CLK2)
$\overline{\text{BUSY}}$ Duration	t_{32}	6		(386 CLK2)
$\overline{\text{ERROR}}$ Inactive to $\overline{\text{BUSY}}$ Inactive	t_{33}	6		(386 CLK2)
PEREQ Inactive to $\overline{\text{ERROR}}$ Active	t_{34}	6		(386 CLK2)
$\overline{\text{READY}}$ Active to Busy Active	t_{35}	4	4	(386 CLK2)
$\overline{\text{READY}}$ Minimum Time from Opcode Write to Opcode to Opcode/ Operand Write	t_{36}	6		(386 CLK2)
$\overline{\text{READY}}$ Minimum Time from Operand Write to Operand Write	t_{37}	8		(386 CLK2)

FIGURE 1. TIMING DIAGRAMS - FAST TRANSITIONS TO AND FROM PIPELINED CYCLES

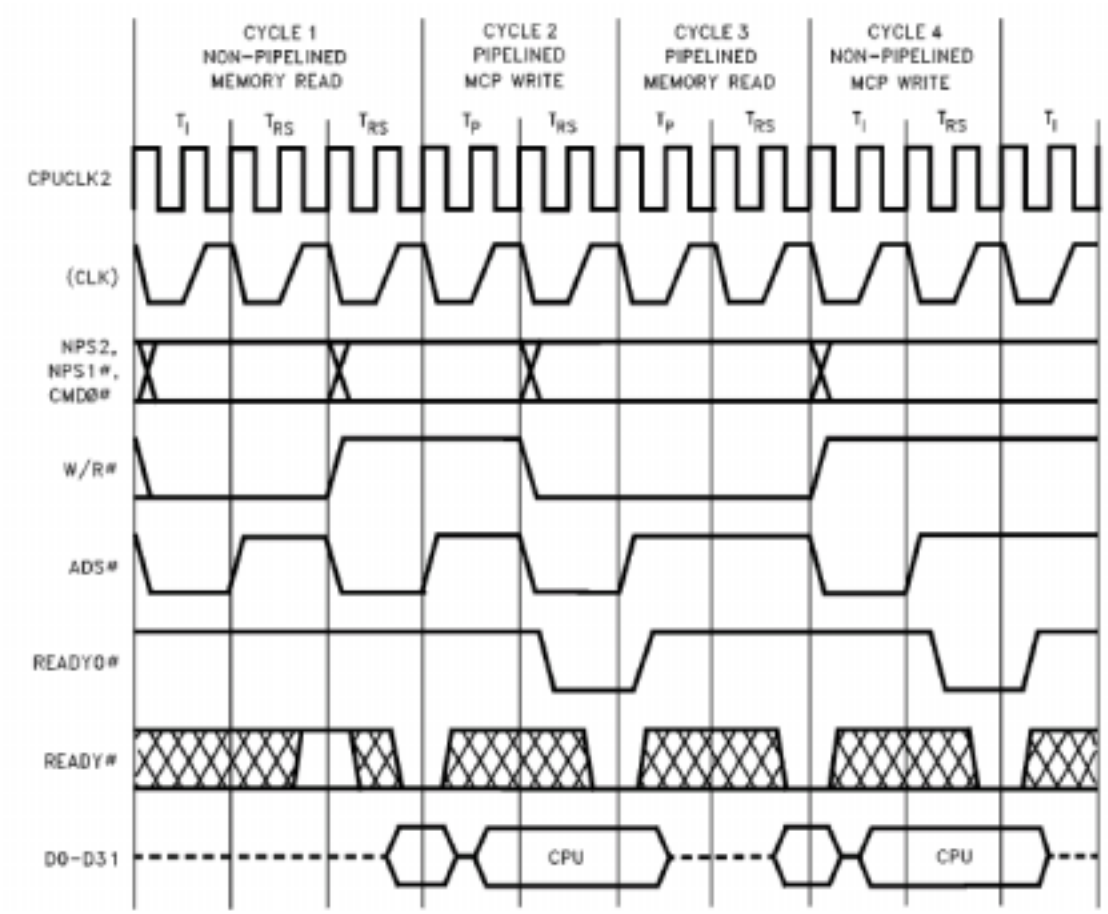
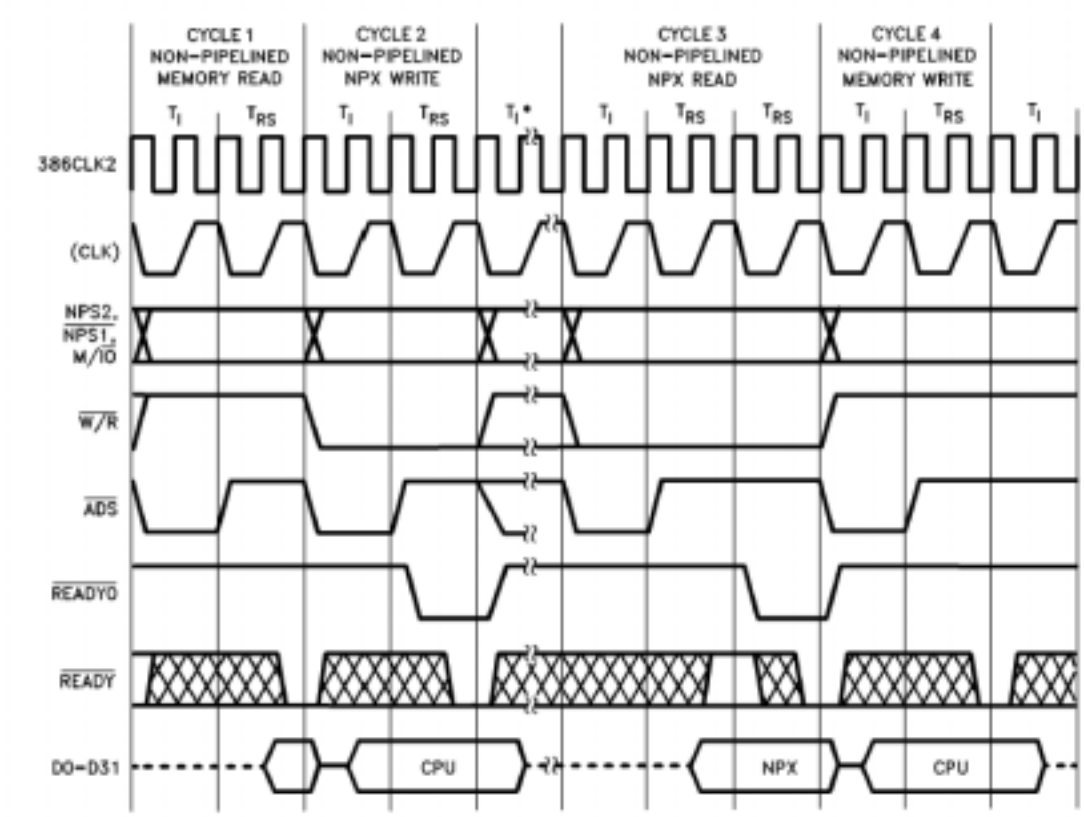
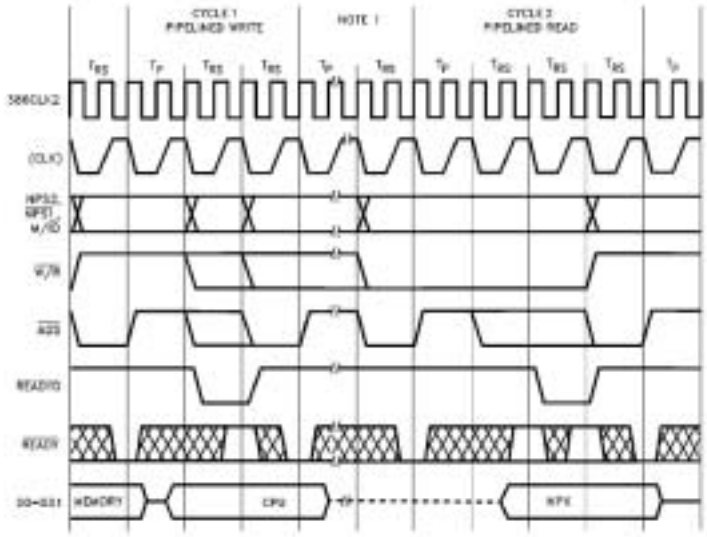


FIGURE 2. TIMING DIAGRAM – NON-PIPELINED READ AND WRITE CYCLES



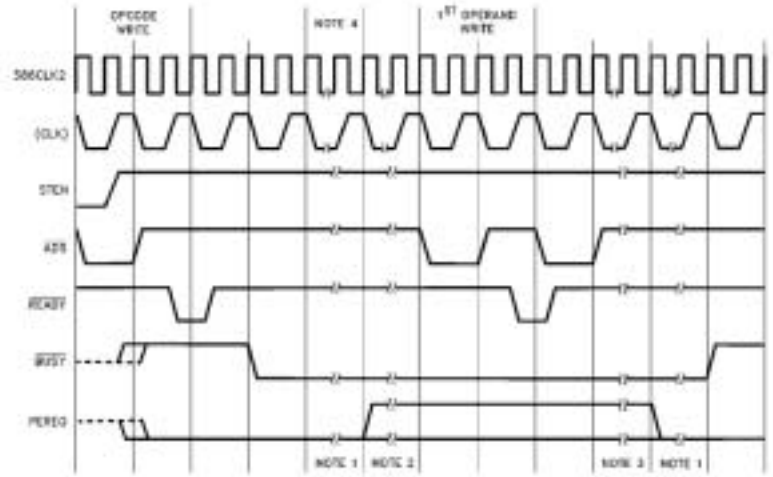
Cycles 1 & 2 represent part of the operand transfer cycle for instructions involving either 4-byte or 8-byte operand loads.
Cycles 3 & 4 represent part of the operand transfer cycle for a store operation.
*Cycles 1 & 2 could repeat here or T_I states for various non-operand transfer cycles and overhead.

FIGURE 3. TIMING DIAGRAM – PIPLINED CYCLES WITH WAIT STATES



NOTE:
1. Cycles between operand write to the NPX and storing result.

FIGURE 4. TIMING DIAGRAM – STEN, BUSY, AND PEREQ TIMING RELATIONSHIP



NOTES:
1. Instruction dependent.
2. PEREQ is an asynchronous input to the 386 processor; it may not be asserted (instruction dependent).
3. More operand transfers.
4. Memory read (operand) cycle is not shown.

FIGURE 5. TIMING DIAGRAM – 386CLK2/387CLK2 WAVEFORM AND MEASUREMENT POINTS FOR INPUT/ OUTPUT AC SPECIFICATIONS

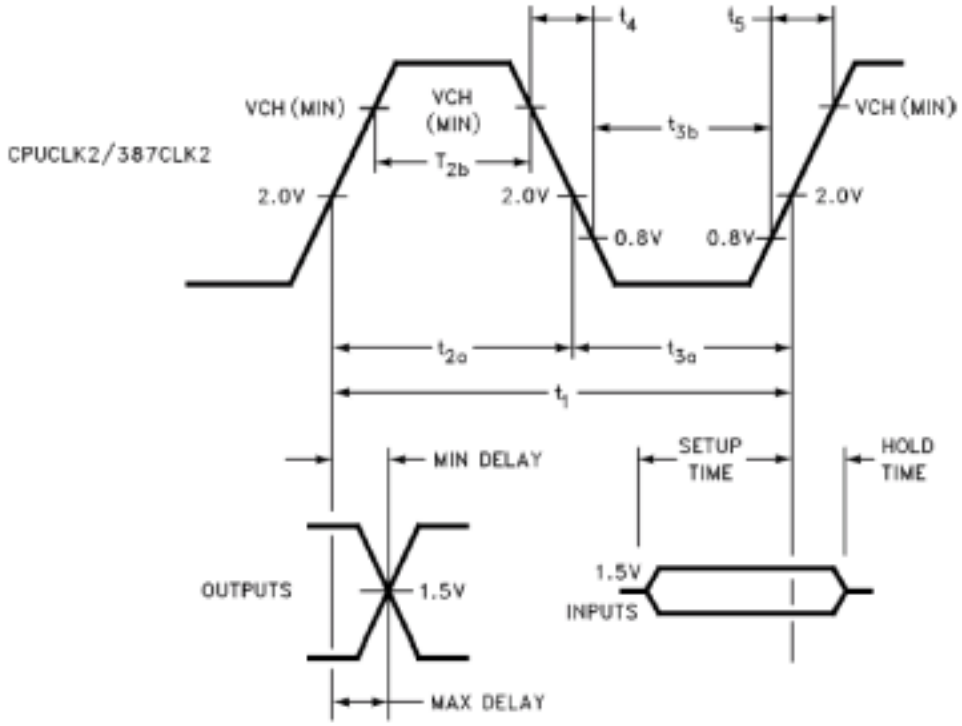


FIGURE 6. TIMING DIAGRAM – TEST CIRCUIT

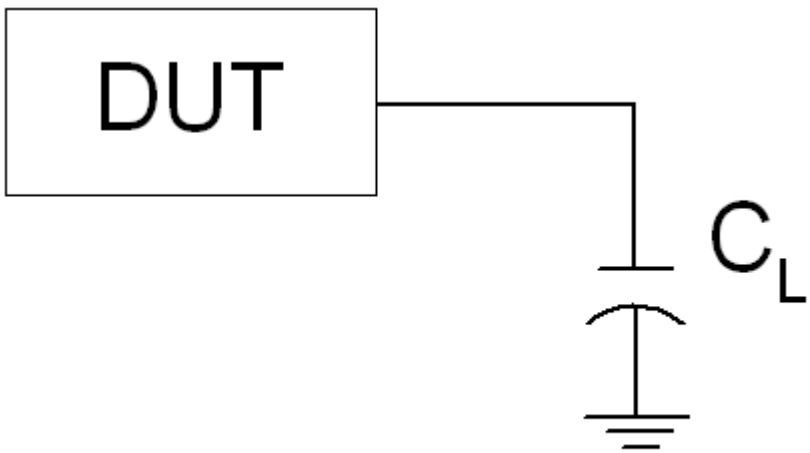
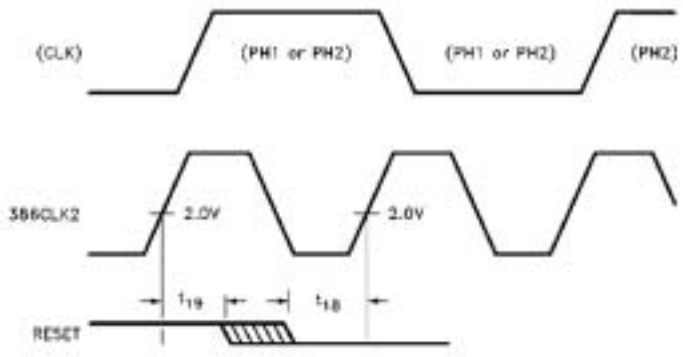


FIGURE 7. TIMING DIAGRAM – RESET



NOTE: The second internal processor phase following RESET high to low transition is PH2.

FIGURE 8. TIMING DIAGRAM – OUTPUT

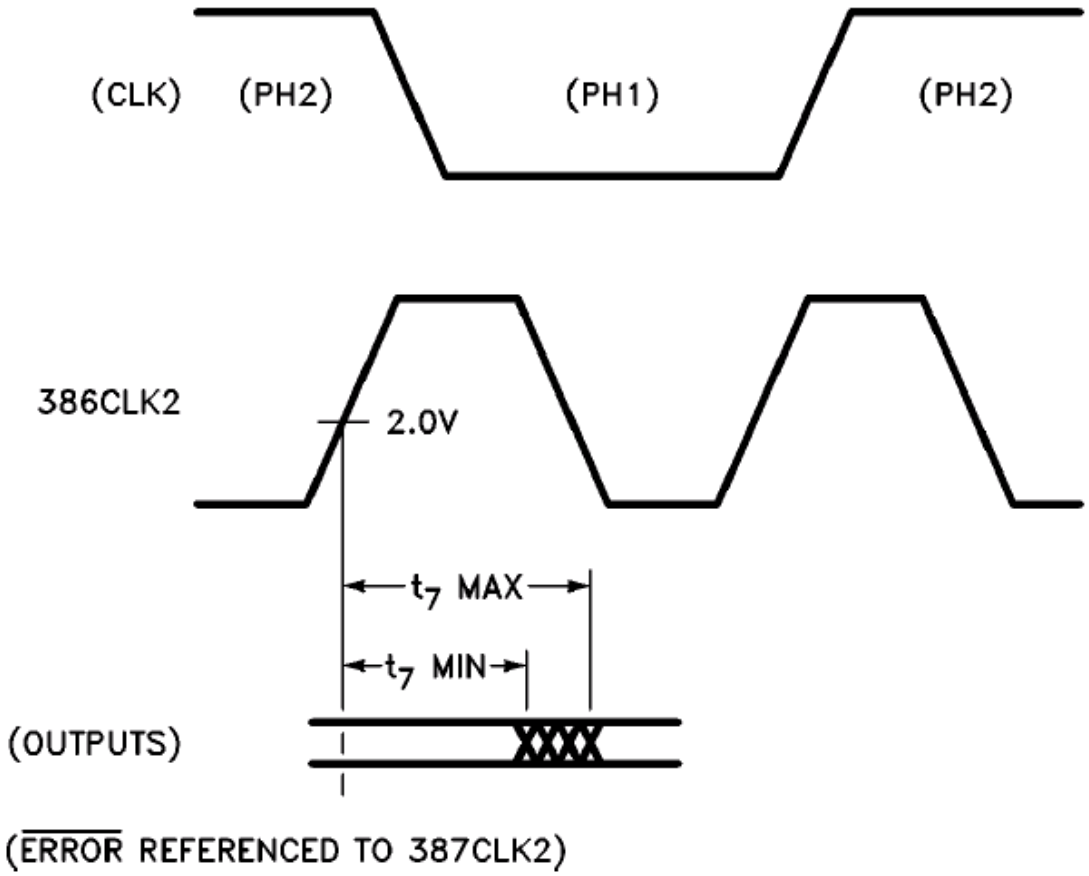


FIGURE 9. TIMING DIAGRAM – INPUT AND I/O SIGNALS

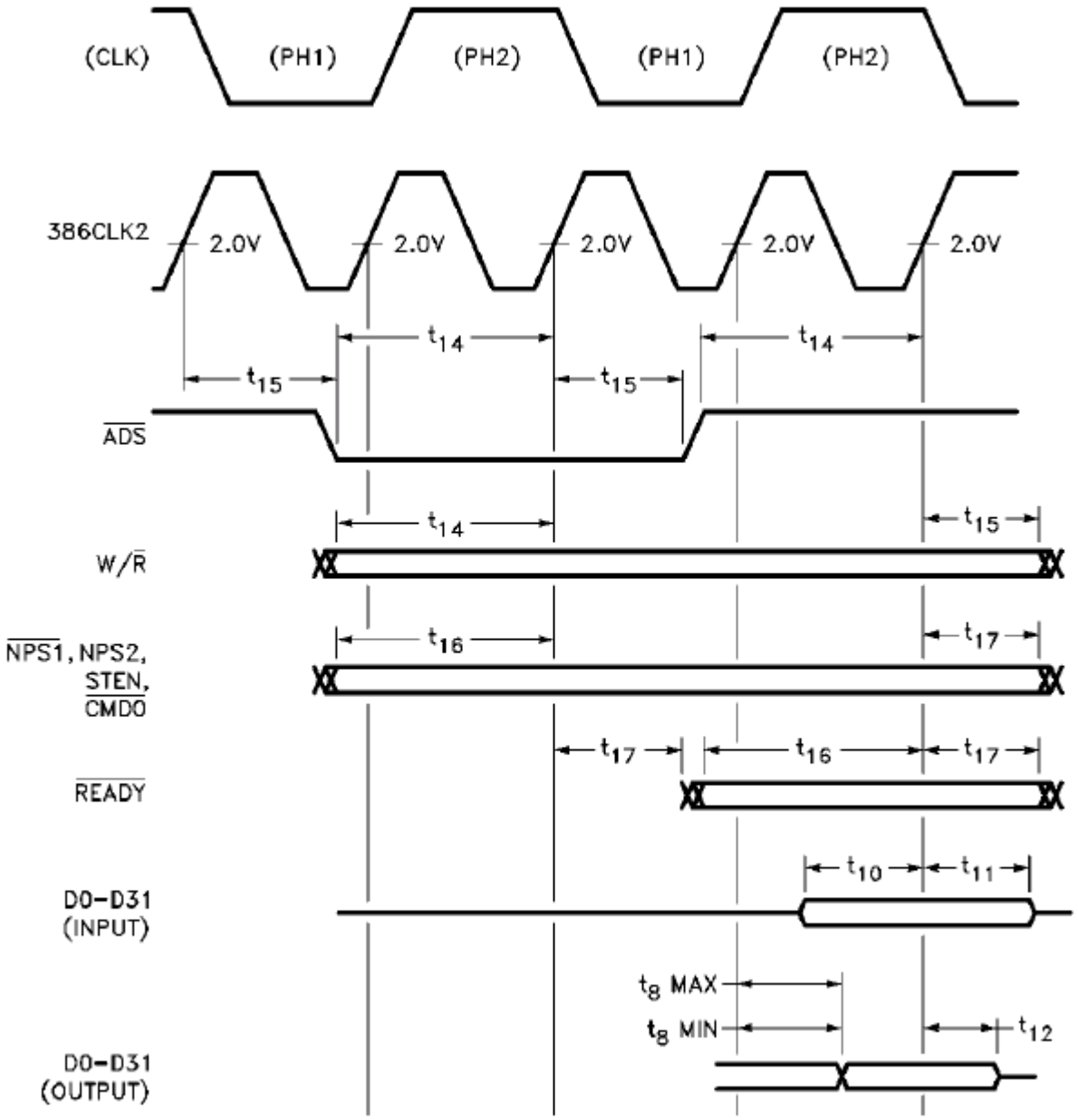


FIGURE 10. TIMING DIAGRAM – FLOAT FROM STEN

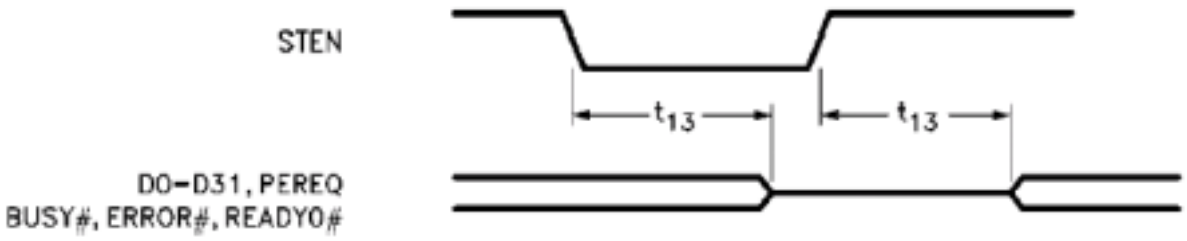
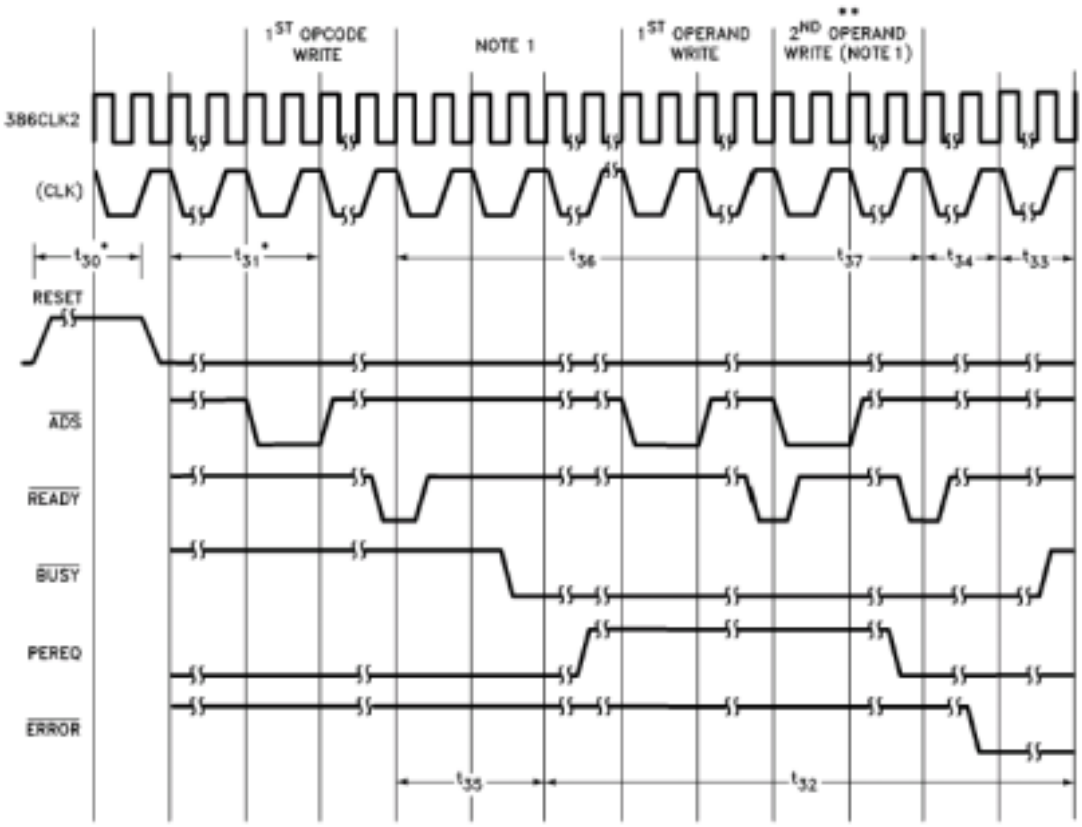
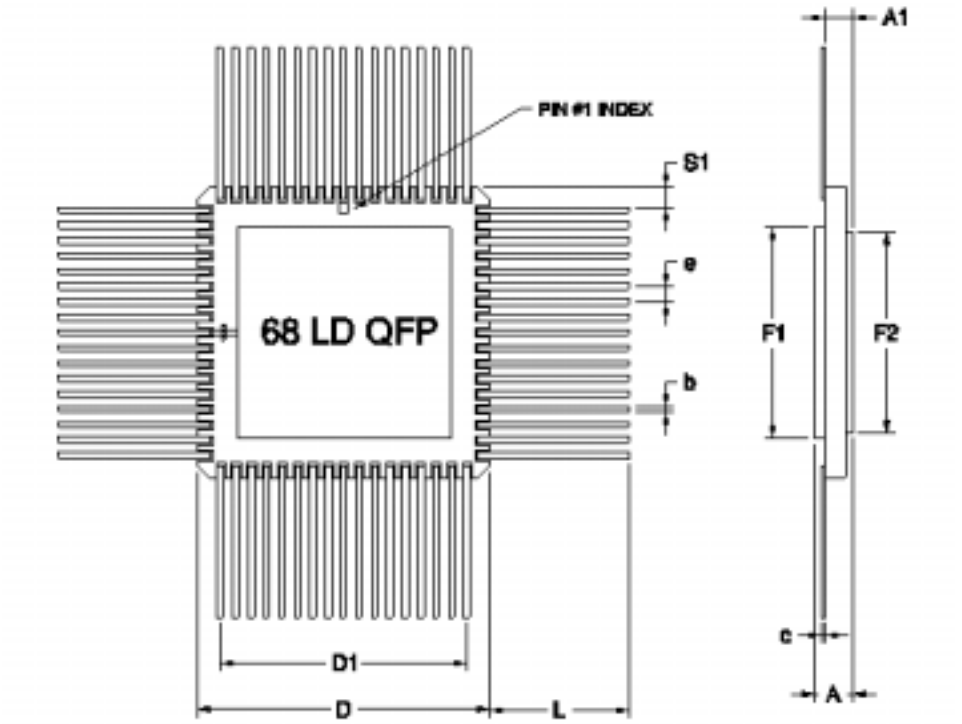


FIGURE 11. TIMING DIAGRAM – OTHER PARAMETERS



* In 387CLK2's
** or last operand

NOTE:
1. Memory read (operand) cycle is not shown.



14 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.121	0.135	0.145
b	0.016	0.018	0.020
c	0.008	0.010	0.012
D	0.940	0.950	0.960
D1		0.800 BSC	
e		0.050 BSC	
S1	0.013	0.066	--
F1	0.645	0.650	0.655
F2	0.645	0.650	0.655
L	0.477	0.487	0.497
A1	0.080	0.090	0.100
N		68	

Note: All dimensions in inches.
Q68-01

Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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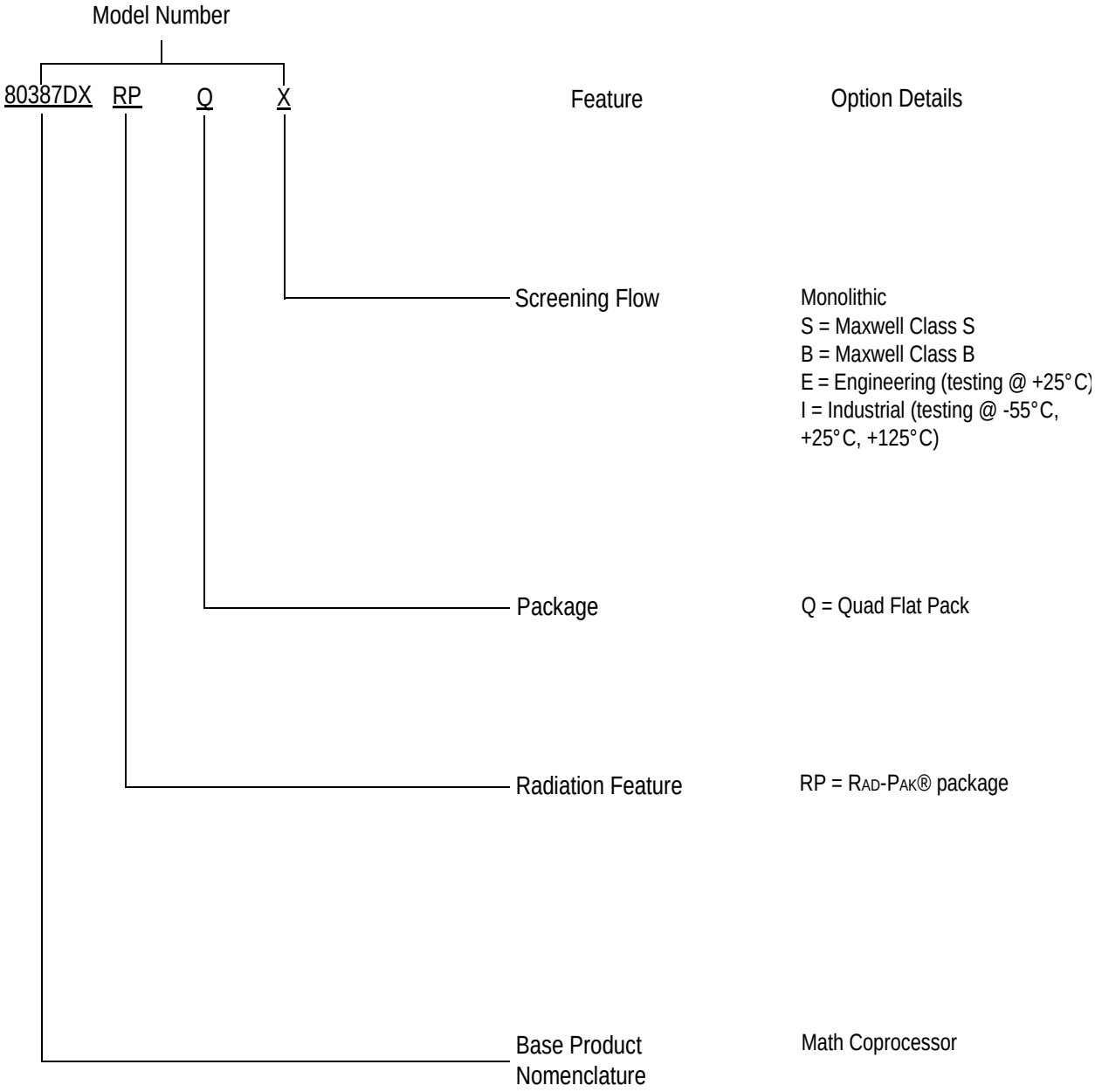

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- *Подбор аналогов.*
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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru