

74ALVC02

Quad 2-input NOR gate

Rev. 3 — 7 September 2017

Product data sheet

1 General description

The 74ALVC02 is a quad 2-input NOR gate.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

2 Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF; R = 0 Ω)
- Specified from -40 °C to +85 °C

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC02D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC02PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC02BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm	SOT762-1

nexperia

4 Functional diagram

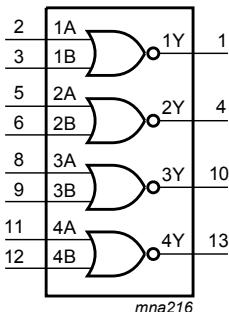


Figure 1. Logic symbol

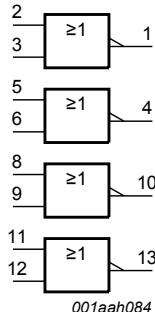


Figure 2. IEC logic symbol

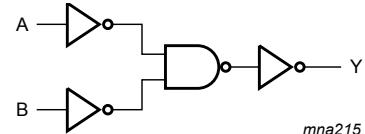


Figure 3. Logic diagram (one gate)

5 Pinning information

5.1 Pinning

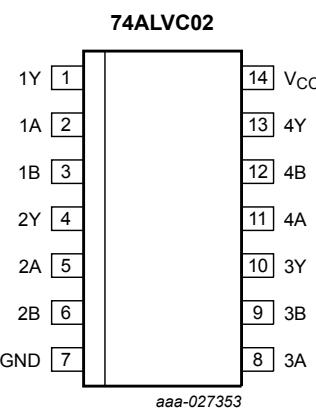


Figure 4. Pin configuration SO14

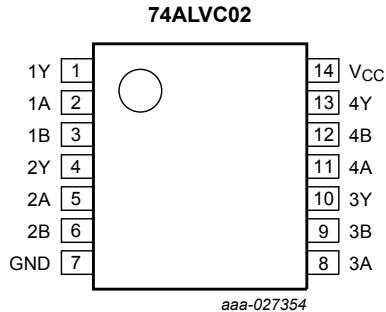
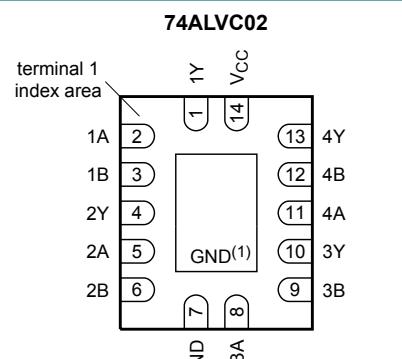


Figure 5. Pin configuration TSSOP14



Transparent top view

(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

Figure 6. Pin configuration
DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 10, 13	data output
1A, 2A, 3A, 4A	2, 5, 8, 11	data input
1B, 2B, 3B, 4B	3, 6, 9, 12	data input
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6 Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		[1] -0.5	+4.6	V
V _O	output voltage	output HIGH or LOW state	[1] [2] -0.5	V _{CC} + 0.5	V
		power-down mode, V _{CC} = 0 V	[2] -0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	[3] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (power-down mode), the output voltage can be 3.6 V in normal operation.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.65	3.6	V
V _I	input voltage		0	3.6	V
V _O	output voltage	V _{CC} = 1.65 to 3.6 V	0	V _{CC}	V
		power-down mode; V _{CC} = 0 V	0	4.6	V
T _{amb}	ambient temperature		-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
			Min	Typ ^[1]	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V}$ to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V}$ to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\text{ }\mu\text{A}$; $V_{CC} = 1.65\text{ V}$ to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6\text{ mA}$; $V_{CC} = 1.65\text{ V}$	1.25	1.51	-	V
		$I_O = -12\text{ mA}$; $V_{CC} = 2.3\text{ V}$	1.8	2.10	-	V
		$I_O = -18\text{ mA}$; $V_{CC} = 2.3\text{ V}$	1.7	2.01	-	V
		$I_O = -12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	2.2	2.53	-	V
		$I_O = -18\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.4	2.76	-	V
		$I_O = -24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.2	2.68	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\text{ }\mu\text{A}$; $V_{CC} = 1.65\text{ V}$ to 3.6 V	-	-	0.2	V
		$I_O = 6\text{ mA}$; $V_{CC} = 1.65\text{ V}$	-	0.11	0.3	V
		$I_O = 12\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	0.17	0.4	V
		$I_O = 18\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	0.25	0.6	V
		$I_O = 12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	-	0.16	0.4	V
		$I_O = 18\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	0.23	0.4	V
		$I_O = 24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	0.30	0.55	V
I_I	input leakage current	$V_{CC} = 3.6\text{ V}$; $V_I = 3.6\text{ V}$ or GND	-	± 0.1	± 5	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 3.6 V	-	± 0.1	± 10	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	0.2	20	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0\text{ V}$ to 3.6 V ; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$	-	5	750	μA
C_I	input capacitance		-	3.5	-	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ (unless stated otherwise) and $T_{amb} = 25^{\circ}\text{C}$.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
			Min	Typ [1]	Max	
t_{pd}	propagation delay	nA, nB to nY; see Figure 7	[2]			
		$V_{CC} = 1.65\text{ V}$ to 1.95 V		1.0	2.8	4.7 ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V		1.0	2.0	3.1 ns
		$V_{CC} = 2.7\text{ V}$		1.0	2.5	2.9 ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V		1.0	2.2	2.8 ns
C_{PD}	power dissipation capacitance	per gate; $V_I = \text{GND}$ to V_{CC} ; $V_{CC} = 3.3\text{ V}$	[3]	-	32	- pF

[1] Typical values are measured at $T_{amb} = 25^{\circ}\text{C}$.

Typical values for $V_{CC} = 1.65\text{ V}$ to 1.95 V are measured at $V_{CC} = 1.8\text{ V}$.

Typical values for $V_{CC} = 2.3\text{ V}$ to 2.7 V are measured at $V_{CC} = 2.5\text{ V}$.

Typical values for $V_{CC} = 3.0\text{ V}$ to 3.6 V are measured at $V_{CC} = 3.3\text{ V}$.

[2] t_{pd} is the same as t_{PHL} and t_{PLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz

f_o = output frequency in MHz

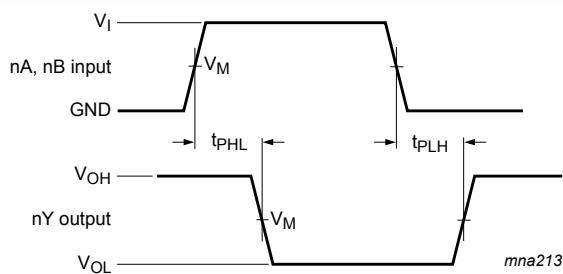
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

10.1 Waveforms and test circuit



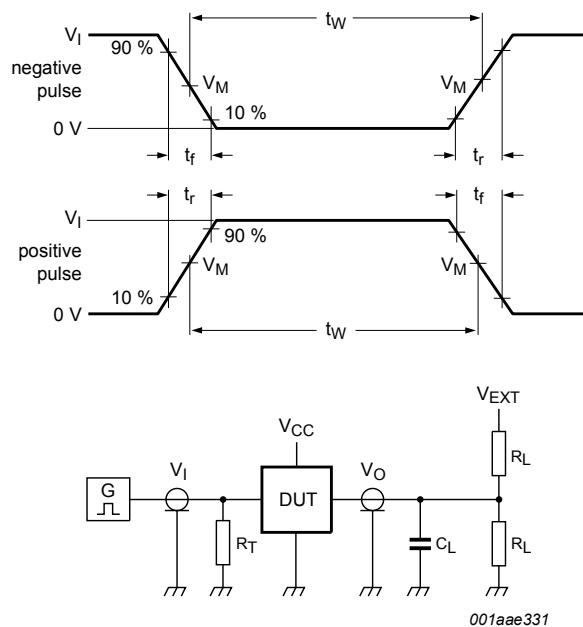
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 7. Input (nA, nB) to output (nY) propagation delays

Table 8. Measurement points

Supply voltage V_{CC}	Input V_I	V_M
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$
2.7 V	2.7 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = Test voltage for switching times.

Figure 8. Test circuit for measuring switching times

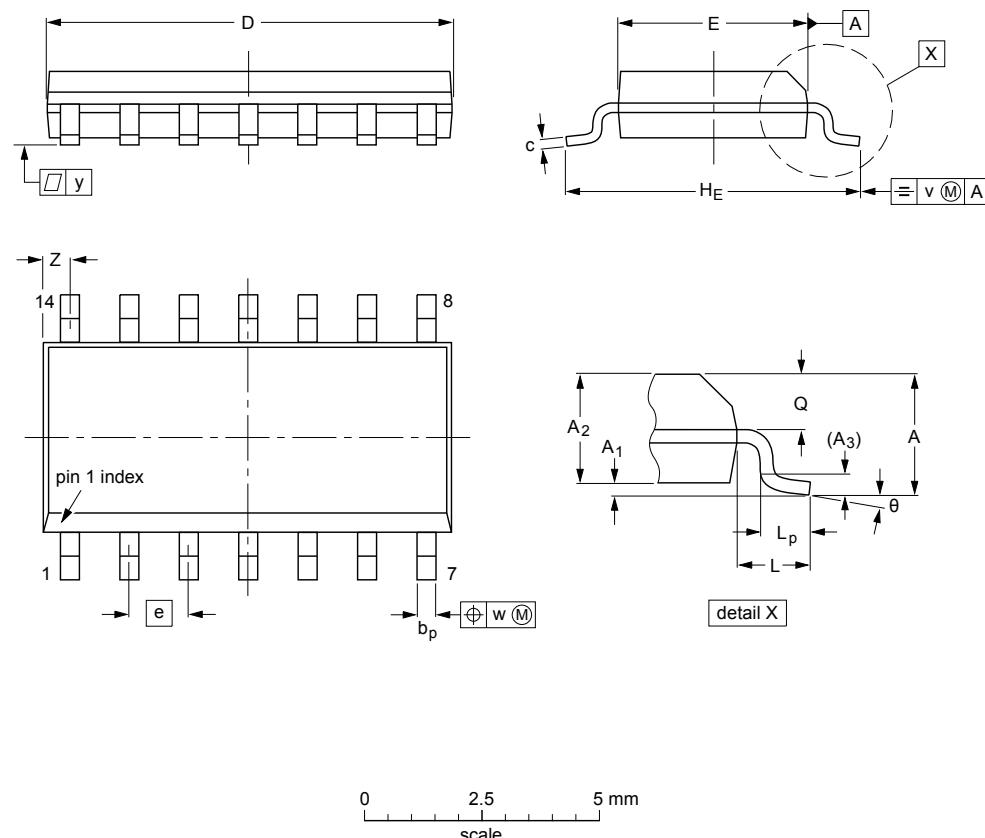
Table 9. Test data

Supply voltage V_{CC}	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

11 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75 0.10	0.25 0.36	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

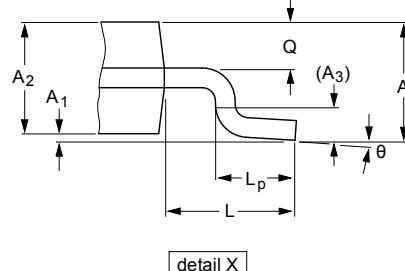
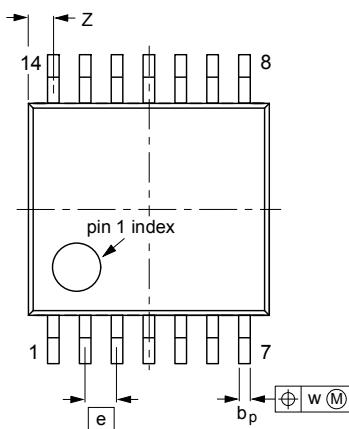
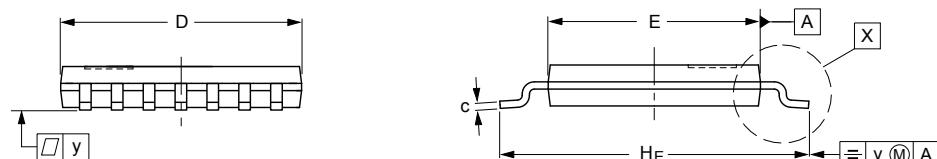
- Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Figure 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1 0.05	0.15 0.80	0.95	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

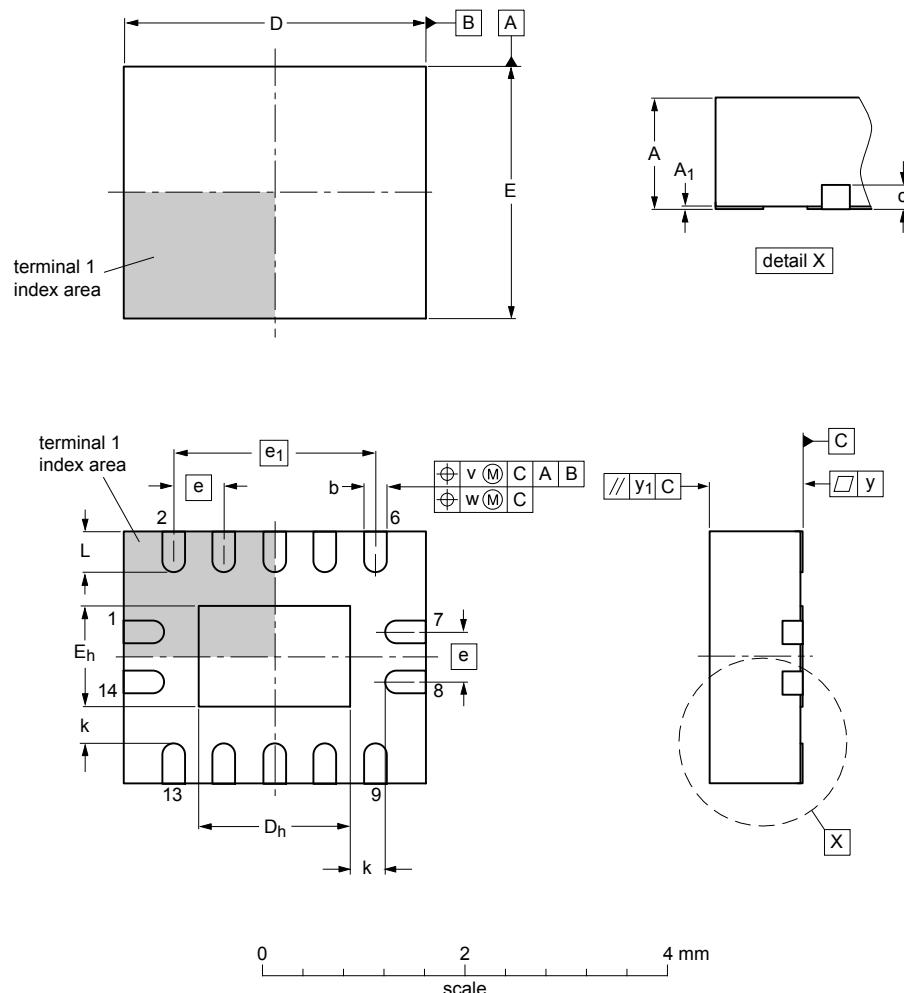
- Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT402-1		MO-153			-99-12-27-03-02-18

Figure 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit	A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	k	L	v	w	y	y ₁
mm	max	1	0.05	0.30		3.1	1.65	2.6	1.15			0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2	0.4	0.1	0.05	0.05	0.1
mm	min		0.00	0.18		2.9	1.35	2.4	0.85		0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT762-1	MO-241				15-04-10 15-05-05

Figure 11. Package outline SOT762-1 (DHVQFN14)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC02 v.3	20170907	Product data sheet	-	74ALVC02 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74ALVC02 v.2	20030714	Product specification	-	74ALVC02 v.1
74ALVC02 v.1	20030205	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

ООО "ЛайфЭлектроникс"

"LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибуторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибуторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помочь разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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