© ABLIC Inc., 2014-2015



The S-1011 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage is fixed internally, and the accuracy of the S-1011 Series A / C / E / G type is ±1.5%. It operates with current consumption of 600 nA typ.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared in the SENSE detection product, so the output is stable even if the SENSE pin falls to 0 V.
The detection signal and release signal can be delayed by setting a capacitor externally, and the detection delay time accuracy is ±20% ($C_N$ = 3.3 nF, Ta = +25°C), the release delay time accuracy is ±20% ($C_P$ = 3.3 nF, Ta = +25°C).
Output form is Nch open-drain output.

## ■ Features

- Detection voltage: 3.0 V to 10.0 V (0.05 V step) (SENSE detection product)
  3.6 V to 10.0 V (0.05 V step) (VDD detection product)
- Detection voltage accuracy: ±1.5% (A / C / E / G type)
- Detection delay time accuracy: ±20% ($C_N$ = 3.3 nF)
- Release delay time accuracy: ±20% ($C_P$ = 3.3 nF)
- Current consumption: 600 nA typ.
- Operation voltage range: 1.8 V to 36.0 V
- Hysteresis width: "Available" (5.0% typ.) / "unavailable" is selectable.
- Output form: Nch open-drain output
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

## ■ Applications

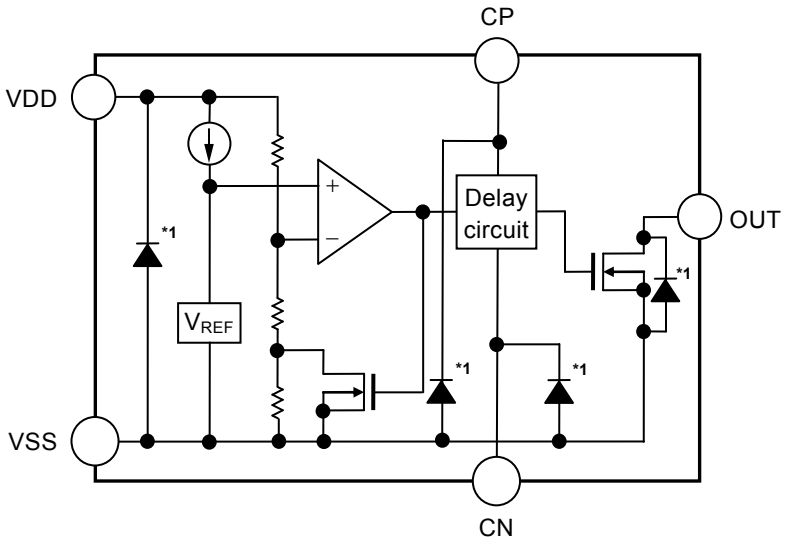
- Power supply monitor for microcomputer and reset for CPU
- Constant voltage power supply monitor for TV and home appliance etc.
- Power supply monitor for Blu-ray recorder, notebook PC and digital still camera
- Industrial equipment, housing equipment

## ■ Package

- SOT-23-6

## ■ Block Diagrams

### 1. S-1011 Series A / J type (VDD detection product)

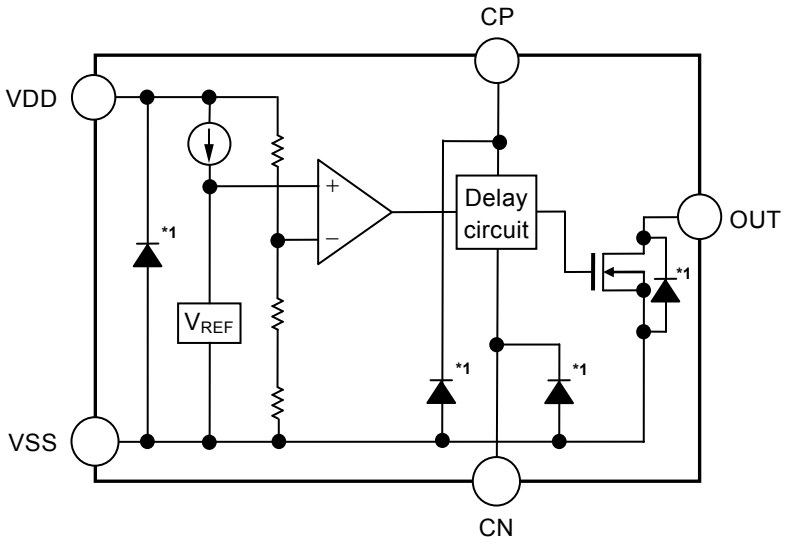



| Function | Status |
|---|---|
| Voltage detection | VDD detection |
| Hysteresis width | Available (5.0% typ.) |

***1.** Parasitic diode

**Figure 1**

### 2. S-1011 Series C / L type (VDD detection product)

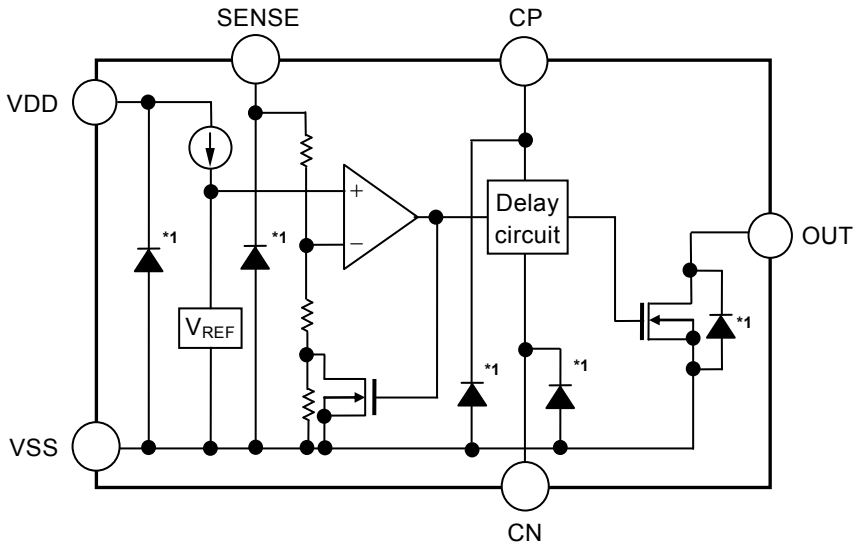



| Function | Status |
|---|---|
| Voltage detection | VDD detection |
| Hysteresis width | Unavailable |

***1.** Parasitic diode

**Figure 2**

### 3. S-1011 Series E / N type (SENSE detection product)

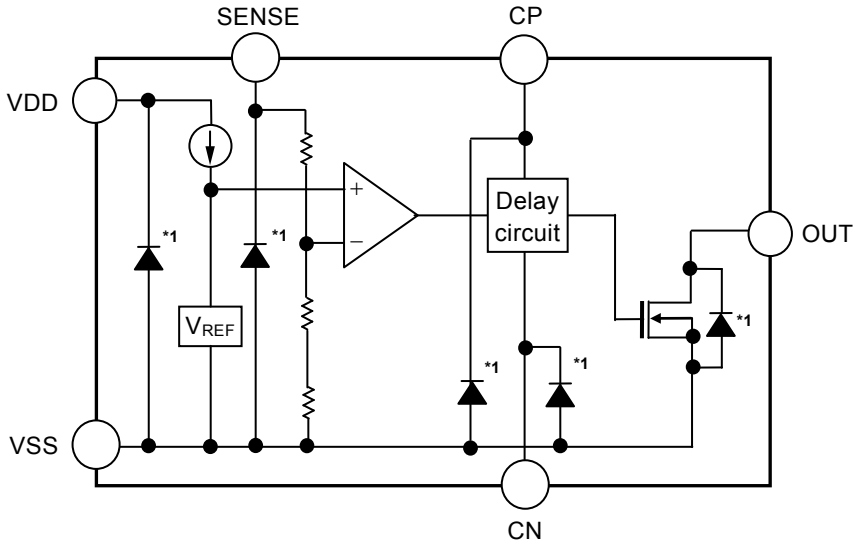



| Function | Status |
|---|---|
| Voltage detection | SENSE detection |
| Hysteresis width | Available (5.0% typ.) |

***1.** Parasitic diode

**Figure 3**

### 4. S-1011 Series G / Q type (SENSE detection product)




| Function | Status |
|---|---|
| Voltage detection | SENSE detection |
| Hysteresis width | Unavailable |

***1.** Parasitic diode

**Figure 4**

## ■ Product Name Structure

Users can select the product type and detection voltage value for the S-1011 Series.
Refer to "**1. Product name**" regarding the contents of product name, "**2. Function list of product types**" regarding the product types, "**3. Package**" regarding the package drawings and "**4. Product name lists**" regarding details of the product name.

### 1. Product name

**S-1011 x xx - M6T1 U 4**

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - M6T1: SOT-23-6, Tape
- Detection voltage value
  - 30 to A0
  - (e.g., when the output voltage is 3.0 V, it is expressed as 30.
    when the output voltage is 10.0 V, it is expressed as A0.)
- Product type*2
  - A, C, E, G, J, L, N, Q

***1.** Refer to the tape drawing.
***2.** Refer to "**2. Function list of product types**".

**Remark** Although the detection voltage in the S-1011 Series is 10.0 V max., the detection voltage exceeding 10.0 V with an external resistor can be set.
Refer to "**2. SENSE pin**" in "**■ Operation**" for details.

### 2. Function list of product types

**Table 1**

| Product Type | Voltage Detection | Output Logic | Hysteresis Width | Detection Voltage |
|---|---|---|---|---|
| A | VDD detection | Active "L" | Available (5.0% typ.) | 5.0 V to 10.0 V |
| C | VDD detection | Active "L" | Unavailable | 5.0 V to 10.0 V |
| E | SENSE detection | Active "L" | Available (5.0% typ.) | 5.0 V to 10.0 V |
| G | SENSE detection | Active "L" | Unavailable | 5.0 V to 10.0 V |
| J | VDD detection | Active "L" | Available (5.0% typ.) | 3.6 V to 4.95 V |
| L | VDD detection | Active "L" | Unavailable | 3.6 V to 4.95 V |
| N | SENSE detection | Active "L" | Available (5.0% typ.) | 3.0 V to 4.95 V |
| Q | SENSE detection | Active "L" | Unavailable | 3.0 V to 4.95 V |

### 3. Package

**Table 2 Package Drawing Codes**

| Package Name | Dimension | Tape | Reel |
|---|---|---|---|
| SOT-23-6 | MP006-A-P-SD | MP006-A-C-SD | MP006-A-R-SD |

## 4. Product name lists

### 4. 1 S-1011 Series A type

Voltage detection: VDD detection
Hysteresis width: Available (5.0% typ.)
Output logic: Active "L"
Detection voltage: 5.0 V to 10.0 V

**Table 3**

| Detection Voltage | SOT-23-6 |
|---|---|
| 5.0 V ± 1.5% | S-1011A50-M6T1U4 |
| 6.0 V ± 1.5% | S-1011A60-M6T1U4 |
| 7.0 V ± 1.5% | S-1011A70-M6T1U4 |
| 8.0 V ± 1.5% | S-1011A80-M6T1U4 |
| 9.0 V ± 1.5% | S-1011A90-M6T1U4 |
| 10.0 V ± 1.5% | S-1011AA0-M6T1U4 |

**Remark** Please contact our sales office for products with specifications other than the above.

### 4. 2 S-1011 Series C type

Voltage detection: VDD detection
Hysteresis width: Unavailable
Output logic: Active "L"
Detection voltage: 5.0 V to 10.0 V

**Table 4**

| Detection Voltage | SOT-23-6 |
|---|---|
| 5.0 V ± 1.5% | S-1011C50-M6T1U4 |
| 6.0 V ± 1.5% | S-1011C60-M6T1U4 |
| 7.0 V ± 1.5% | S-1011C70-M6T1U4 |
| 8.0 V ± 1.5% | S-1011C80-M6T1U4 |
| 9.0 V ± 1.5% | S-1011C90-M6T1U4 |
| 10.0 V ± 1.5% | S-1011CA0-M6T1U4 |

**Remark** Please contact our sales office for products with specifications other than the above.

### 4. 3 S-1011 Series E type

Voltage detection: SENSE detection
Hysteresis width: Available (5.0% typ.)
Output logic: Active "L"
Detection voltage: 5.0 V to 10.0 V

**Table 5**

| Detection Voltage | SOT-23-6 |
|---|---|
| 5.0 V ± 1.5% | S-1011E50-M6T1U4 |
| 6.0 V ± 1.5% | S-1011E60-M6T1U4 |
| 7.0 V ± 1.5% | S-1011E70-M6T1U4 |
| 8.0 V ± 1.5% | S-1011E80-M6T1U4 |
| 9.0 V ± 1.5% | S-1011E90-M6T1U4 |
| 10.0 V ± 1.5% | S-1011EA0-M6T1U4 |

**Remark** Please contact our sales office for products with specifications other than the above.

### 4. 4 S-1011 Series G type

Voltage detection: SENSE detection
Hysteresis width: Unavailable
Output logic: Active "L"
Detection voltage: 5.0 V to 10.0 V

**Table 6**

| Detection Voltage | SOT-23-6 |
|---|---|
| 5.0 V ± 1.5% | S-1011G50-M6T1U4 |
| 6.0 V ± 1.5% | S-1011G60-M6T1U4 |
| 7.0 V ± 1.5% | S-1011G70-M6T1U4 |
| 8.0 V ± 1.5% | S-1011G80-M6T1U4 |
| 9.0 V ± 1.5% | S-1011G90-M6T1U4 |
| 10.0 V ± 1.5% | S-1011GA0-M6T1U4 |

**Remark** Please contact our sales office for products with specifications other than the above.

### 4. 5 S-1011 Series J type

Voltage detection: VDD detection
Hysteresis width: Available (5.0% typ.)
Output logic: Active "L"
Detection voltage: 3.6 V to 4.95 V

**Table 7**

| Detection Voltage | SOT-23-6 |
|---|---|
| 3.6 V ± 3.0% | S-1011J36-M6T1U4 |
| 4.2 V ± 2.5% | S-1011J42-M6T1U4 |

**Remark** Please contact our sales office for products with specifications other than the above.

### 4. 6 S-1011 Series L type

Voltage detection: VDD detection
Hysteresis width: Unavailable
Output logic: Active "L"
Detection voltage: 3.6 V to 4.95 V

**Table 8**

| Detection Voltage | SOT-23-6 |
|---|---|
| 3.6 V ± 3.0% | S-1011L36-M6T1U4 |
| 4.2 V ± 2.5% | S-1011L42-M6T1U4 |

**Remark** Please contact our sales office for products with specifications other than the above.

### 4. 7 S-1011 Series N type

Voltage detection: SENSE detection
Hysteresis width: Available (5.0% typ.)
Output logic: Active "L"
Detection voltage: 3.0 V to 4.95 V

**Table 9**

| Detection Voltage | SOT-23-6 |
|---|---|
| 3.0 V ± 3.0% | S-1011N30-M6T1U4 |
| 3.3 V ± 3.0% | S-1011N33-M6T1U4 |
| 3.6 V ± 3.0% | S-1011N36-M6T1U4 |
| 4.2 V ± 2.5% | S-1011N42-M6T1U4 |

**Remark** Please contact our sales office for products with specifications other than the above.

### 4. 8 S-1011 Series Q type

Voltage detection: SENSE detection
Hysteresis width: Unavailable
Output logic: Active "L"
Detection voltage: 3.0 V to 4.95 V

**Table 10**

| Detection Voltage | SOT-23-6 |
|---|---|
| 3.0 V ± 3.0% | S-1011Q30-M6T1U4 |
| 3.3 V ± 3.0% | S-1011Q33-M6T1U4 |
| 3.6 V ± 3.0% | S-1011Q36-M6T1U4 |
| 4.2 V ± 2.5% | S-1011Q42-M6T1U4 |

**Remark** Please contact our sales office for products with specifications other than the above.

## ■ Pin Configurations

### 1. S-1011 Series A / C / J / L type (VDD detection product)

#### 1. 1 SOT-23-6

Top view

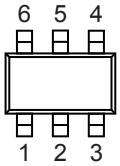



**Figure 5**

**Table 11**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VDD | Voltage input pin |
| 2 | NC*1 | No connection |
| 3 | OUT | Voltage detection output pin |
| 4 | CP*2 | Connection pin for release delay capacitor |
| 5 | VSS | GND pin |
| 6 | CN*3 | Connection pin for detection delay capacitor |

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

***2.** Connect a capacitor between the CP pin and the VSS pin.
The release delay time can be adjusted according to the capacitance.
Moreover, the CP pin is available even when it is open.

***3.** Connect a capacitor between the CN pin and the VSS pin.
The detection delay time can be adjusted according to the capacitance.
Moreover, the CN pin is available even when it is open.

### 2. S-1011 Series E / G / N / Q type (SENSE detection product)

#### 2. 1 SOT-23-6

Top view

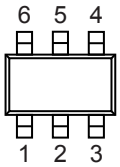



**Figure 6**

**Table 12**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VDD | Voltage input pin |
| 2 | SENSE | Detection voltage input pin |
| 3 | OUT | Voltage detection output pin |
| 4 | CP*1 | Connection pin for release delay capacitor |
| 5 | VSS | GND pin |
| 6 | CN*2 | Connection pin for detection delay capacitor |

***1.** Connect a capacitor between the CP pin and the VSS pin.
The release delay time can be adjusted according to the capacitance.
Moreover, the CP pin is available even when it is open.

***2.** Connect a capacitor between the CN pin and the VSS pin.
The detection delay time can be adjusted according to the capacitance.
Moreover, the CN pin is available even when it is open.

## ■ Absolute Maximum Ratings

**Table 13**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD} - V_{SS}$ | $V_{SS} - 0.3$ to $V_{SS} + 45$ | V |
| SENSE pin input voltage | $V_{SENSE}$ | $V_{SS} - 0.3$ to $V_{SS} + 45$ | V |
| CP pin input voltage | $V_{CP}$ | $V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 7.0$ | V |
| CN pin input voltage | $V_{CN}$ | $V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 7.0$ | V |
| Output voltage | $V_{OUT}$ | $V_{SS} - 0.3$ to $V_{SS} + 45$ | V |
| Output current | $I_{OUT}$ | 25 | mA |
| Operation ambient temperature | $T_{opr}$ | −40 to +85 | °C |
| Storage temperature | $T_{stg}$ | −40 to +125 | °C |

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

## ■ Thermal Resistance Value

**Table 14**

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Junction-to-ambient thermal resistance*1 | $\theta_{ja}$ | SOT-23-6 | Board 1 | – | 159 | – | °C/W |
| | | | Board 2 | – | 124 | – | °C/W |

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "**■ Thermal Characteristics**" for details of power dissipation and test board.

## ■ Electrical Characteristics

### 1. VDD detection product

#### 1. 1 S-1011 Series J / L type

**Table 15**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage[*1] | $-V_{DET}$ | 3.6 V ≤ $-V_{DET(S)}$ ≤ 4.15 V | | $-V_{DET(S)} \times 0.970$ | $-V_{DET(S)}$ | $-V_{DET(S)} \times 1.030$ | V | 1 |
| | | 4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V | | $-V_{DET(S)} \times 0.975$ | $-V_{DET(S)}$ | $-V_{DET(S)} \times 1.025$ | V | 1 |
| Hysteresis width | $V_{HYS}$ | J type | 3.6 V ≤ $-V_{DET(S)}$ ≤ 4.15 V | $-V_{DET} \times 0.010$ | $-V_{DET} \times 0.050$ | $-V_{DET} \times 0.100$ | V | 1 |
| | | | 4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V | $-V_{DET} \times 0.020$ | $-V_{DET} \times 0.050$ | $-V_{DET} \times 0.090$ | V | 1 |
| | | L type[*2] | 3.6 V ≤ $-V_{DET(S)}$ ≤ 4.95 V | – | 0 | – | V | 1 |
| Current consumption | $I_{SS}$ | $V_{DD}$ = $-V_{DET}$ – 0.1 V, 3.6 V ≤ $-V_{DET}$ ≤ 4.95 V | | – | 0.60 | 1.60 | μA | 2 |
| Operation voltage | $V_{DD}$ | – | | 1.8 | – | 36.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch $V_{DS}$[*3] = 0.05 V | $V_{DD}$ = 2.9 V | 0.33 | – | – | mA | 3 |
| Leakage current | $I_{LEAK}$ | Output transistor Nch | $V_{DD}$ = 30.0 V, $V_{OUT}$ = 30.0 V | – | – | 2.0 | μA | 3 |
| Detection delay time[*4] | $t_{RESET}$ | $C_N$ = 3.3 nF | | 8.0 | 10.0 | 12.0 | ms | 4 |
| Release delay time[*5] | $t_{DELAY}$ | $C_P$ = 3.3 nF | | 8.0 | 10.0 | 12.0 | ms | 4 |
| CP pin discharge ON resistance | $R_{CP}$ | $V_{DD}$ = 6.9 V, $V_{CP}$ = 0.5 V | | 0.52 | – | 2.2 | kΩ | – |
| CN pin discharge ON resistance | $R_{CN}$ | $V_{DD}$ = 2.9 V, $V_{CN}$ = 0.5 V | | 1.0 | – | 5.0 | kΩ | – |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value

***2.** Hysteresis width is "unavailable", so release voltage = detection voltage.

***3.** $V_{DS}$: Drain-to-source voltage of the output transistor

***4.** The time period from when the pulse voltage of $-V_{DET(S)}$ + 0.5 V → $-V_{DET(S)}$ – 0.5 V is applied to the VDD pin to when $V_{OUT}$ reaches $V_{DD}$ / 2, after the power supply voltage ($V_{DD}$) reaches the release voltage once.

***5.** The time period from when the pulse voltage of $-V_{DET(S)}$ – 0.5 V → $-V_{DET(S)}$ + 0.5 V is applied to the VDD pin to when $V_{OUT}$ reaches $V_{DD}$ / 2.

### 1. 2 S-1011 Series A / C type

**Table 16**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage[*1] | $-V_{DET}$ | 5.0 V ≤ $-V_{DET(S)}$ ≤ 10.0 V | | $-V_{DET(S)}$ × 0.985 | $-V_{DET(S)}$ | $-V_{DET(S)}$ × 1.015 | V | 1 |
| Hysteresis width | $V_{HYS}$ | A type | | $-V_{DET}$ × 0.030 | $-V_{DET}$ × 0.050 | $-V_{DET}$ × 0.080 | V | 1 |
| | | C type[*2] | | – | 0 | – | V | 1 |
| Current consumption | $I_{SS}$ | $V_{DD}$ = $-V_{DET}$ – 0.1 V, 5.0 V ≤ $-V_{DET}$ ≤ 10.0 V | | – | 0.60 | 1.60 | μA | 2 |
| Operation voltage | $V_{DD}$ | – | | 1.8 | – | 36.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch $V_{DS}$[*3] = 0.05 V | $V_{DD}$ = 4.5 V | 0.5 | – | – | mA | 3 |
| Leakage current | $I_{LEAK}$ | Output transistor Nch | $V_{DD}$ = 30.0 V, $V_{OUT}$ = 30.0 V | – | – | 2.0 | μA | 3 |
| Detection delay time[*4] | $t_{RESET}$ | $C_N$ = 3.3 nF | | 8.0 | 10.0 | 12.0 | ms | 4 |
| Release delay time[*5] | $t_{DELAY}$ | $C_P$ = 3.3 nF | | 8.0 | 10.0 | 12.0 | ms | 4 |
| CP pin discharge ON resistance | $R_{CP}$ | $V_{DD}$ = 14.0 V, $V_{CP}$ = 0.5 V | | 0.30 | – | 2.60 | kΩ | – |
| CN pin discharge ON resistance | $R_{CN}$ | $V_{DD}$ = 4.5 V, $V_{CN}$ = 0.5 V | | 0.63 | – | 2.60 | kΩ | – |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value

***2.** Hysteresis width is "unavailable", so release voltage = detection voltage.

***3.** $V_{DS}$: Drain-to-source voltage of the output transistor

***4.** The time period from when the pulse voltage of $-V_{DET(S)}$ + 1.0 V → $-V_{DET(S)}$ – 1.0 V is applied to the VDD pin to when $V_{OUT}$ reaches $V_{DD}$ / 2, after the power supply voltage ($V_{DD}$) reaches the release voltage once.

***5.** The time period from when the pulse voltage of $-V_{DET(S)}$ – 1.0 V → $-V_{DET(S)}$ + 1.0 V is applied to the VDD pin to when $V_{OUT}$ reaches $V_{DD}$ / 2.

## 2. SENSE detection product

### 2. 1 S-1011 Series N / Q type

**Table 17**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|---|
| Detection voltage[*1] | $-V_{DET}$ | $V_{DD}$ = 16.0 V | 3.0 V ≤ $-V_{DET(S)}$ ≤ 4.15 V | | $-V_{DET(S)} \times 0.970$ | $-V_{DET(S)}$ | $-V_{DET(S)} \times 1.030$ | V | 1 |
| | | | 4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V | | $-V_{DET(S)} \times 0.975$ | $-V_{DET(S)}$ | $-V_{DET(S)} \times 1.025$ | V | 1 |
| Hysteresis width | $V_{HYS}$ | $V_{DD}$ = 16.0 V | N type | 3.0 V ≤ $-V_{DET(S)}$ ≤ 4.15 V | $-V_{DET} \times 0.010$ | $-V_{DET} \times 0.050$ | $-V_{DET} \times 0.100$ | V | 1 |
| | | | | 4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V | $-V_{DET} \times 0.020$ | $-V_{DET} \times 0.050$ | $-V_{DET} \times 0.090$ | V | 1 |
| | | | Q type[*2] | 3.0 V ≤ $-V_{DET(S)}$ ≤ 4.95 V | – | 0 | – | V | 1 |
| Current consumption[*3] | $I_{SS}$ | $V_{DD}$ = 16.0 V, $V_{SENSE}$ = $-V_{DET}$ – 0.1 V, 3.0 V ≤ $-V_{DET}$ ≤ 4.95 V | | | – | 0.55 | 1.55 | μA | 2 |
| Operation voltage | $V_{DD}$ | – | | | 3.0 | – | 36.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch $V_{DS}$[*4] = 0.05 V | $V_{DD}$ = 5.0 V, $V_{SENSE}$ = 2.9 V | | 0.5 | – | – | mA | 3 |
| Leakage current | $I_{LEAK}$ | Output transistor Nch | $V_{DD}$ = 30.0 V, $V_{OUT}$ = 30.0 V, $V_{SENSE}$ = 30.0 V | | – | – | 2.0 | μA | 3 |
| Detection delay time[*5] | $t_{RESET}$ | $C_N$ = 3.3 nF | | | 8.0 | 10.0 | 12.0 | ms | 4 |
| Release delay time[*6] | $t_{DELAY}$ | $C_P$ = 3.3 nF | | | 8.0 | 10.0 | 12.0 | ms | 4 |
| SENSE pin resistance | $R_{SENSE}$ | – | | | 6.8 | – | 275 | MΩ | 2 |
| CP pin discharge ON resistance | $R_{CP}$ | $V_{DD}$ = 3.0 V, $V_{SENSE}$ = 6.9 V, $V_{CP}$ = 0.5 V | | | 0.72 | – | 4.29 | kΩ | – |
| CN pin discharge ON resistance | $R_{CN}$ | $V_{DD}$ = 3.0 V, $V_{SENSE}$ = 2.9 V, $V_{CN}$ = 0.5 V | | | 0.72 | – | 4.29 | kΩ | – |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value

***2.** Hysteresis width is "unavailable", so release voltage = detection voltage.

***3.** The current flowing through the SENSE pin resistance is not included.

***4.** $V_{DS}$: Drain-to-source voltage of the output transistor

***5.** The time period from when the pulse voltage of $-V_{DET(S)}$ + 0.5 V → $-V_{DET(S)}$ – 0.5 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2, after voltage of 16.0 V is applied to the VDD pin and the SENSE pin input voltage ($V_{SENSE}$) reaches the release voltage once.

***6.** The time period from when voltage of 16.0 V is applied to the VDD pin and the pulse voltage of $-V_{DET(S)}$ – 0.5 V → $-V_{DET(S)}$ + 0.5 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2.

### 2. 2 S-1011 Series E / G type

**Table 18**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage*1 | $-V_{DET}$ | $V_{DD}$ = 16.0 V, 5.0 V ≤ $-V_{DET(S)}$ ≤ 10.0 V | | $-V_{DET(S)} \times 0.985$ | $-V_{DET(S)}$ | $-V_{DET(S)} \times 1.015$ | V | 1 |
| Hysteresis width | $V_{HYS}$ | $V_{DD}$ = 16.0 V | E type | $-V_{DET} \times 0.030$ | $-V_{DET} \times 0.050$ | $-V_{DET} \times 0.080$ | V | 1 |
| | | | G type*2 | – | 0 | – | V | 1 |
| Current consumption*3 | $I_{SS}$ | $V_{DD}$ = 16.0 V, $V_{SENSE}$ = $-V_{DET}$ – 0.1 V, 5.0 V ≤ $-V_{DET}$ ≤ 10.0 V | | – | 0.55 | 1.55 | μA | 2 |
| Operation voltage | $V_{DD}$ | – | | 3.0 | – | 36.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch $V_{DS}$*4 = 0.05 V | $V_{DD}$ = 5.0 V, $V_{SENSE}$ = 4.5 V | 0.5 | – | – | mA | 3 |
| Leakage current | $I_{LEAK}$ | Output transistor Nch | $V_{DD}$ = 30.0 V, $V_{OUT}$ = 30.0 V, $V_{SENSE}$ = 30.0 V | – | – | 2.0 | μA | 3 |
| Detection delay time*5 | $t_{RESET}$ | $C_N$ = 3.3 nF | | 8.0 | 10.0 | 12.0 | ms | 4 |
| Release delay time*6 | $t_{DELAY}$ | $C_P$ = 3.3 nF | | 8.0 | 10.0 | 12.0 | ms | 4 |
| SENSE pin resistance | $R_{SENSE}$ | – | | 26.0 | – | 400 | MΩ | 2 |
| CP pin discharge ON resistance | $R_{CP}$ | $V_{DD}$ = 4.5 V, $V_{SENSE}$ = 14.0 V, $V_{CP}$ = 0.5 V | | 0.30 | – | 2.60 | kΩ | – |
| CN pin discharge ON resistance | $R_{CN}$ | $V_{DD}$ = 4.5 V, $V_{SENSE}$ = 4.5 V, $V_{CN}$ = 0.5 V | | 0.63 | – | 2.60 | kΩ | – |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value

***2.** Hysteresis width is "unavailable", so release voltage = detection voltage.

***3.** The current flowing through the SENSE pin resistance is not included.

***4.** $V_{DS}$: Drain-to-source voltage of the output transistor

***5.** The time period from when the pulse voltage of $-V_{DET(S)}$ + 1.0 V → $-V_{DET(S)}$ – 1.0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2, after voltage of 16.0 V is applied to the VDD pin and the SENSE pin input voltage ($V_{SENSE}$) reaches the release voltage once.

***6.** The time period from when voltage of 16.0 V is applied to the VDD pin and the pulse voltage of $-V_{DET(S)}$ – 1.0 V → $-V_{DET(S)}$ + 1.0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2.

## ■ Test Circuits

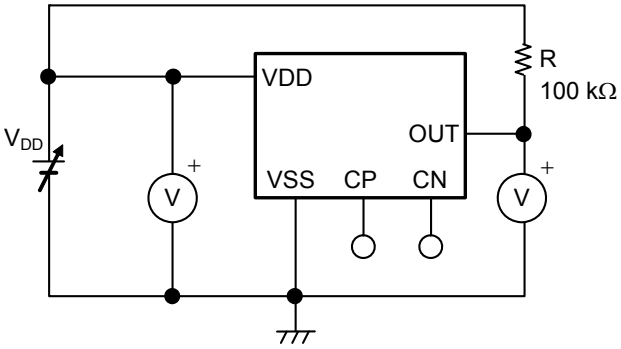



**Figure 7 Test Circuit 1 (VDD detection product)**

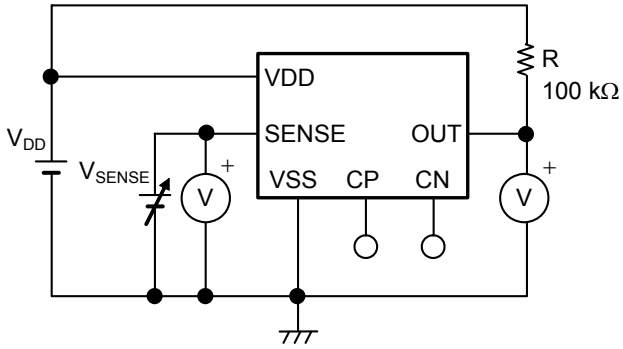



**Figure 8 Test Circuit 1 (SENSE detection product)**

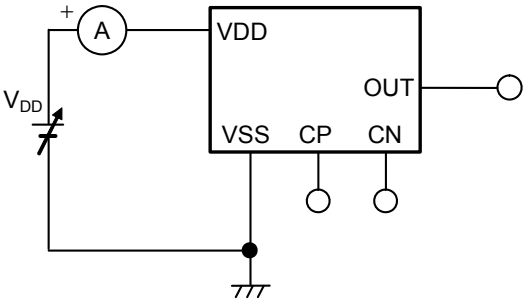



**Figure 9 Test Circuit 2 (VDD detection product)**

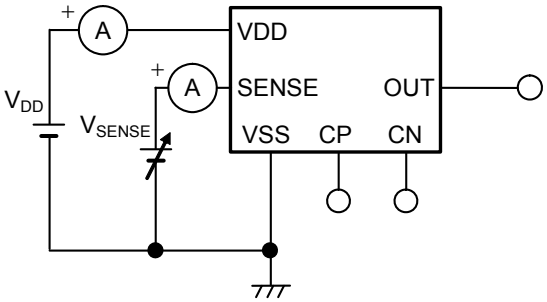



**Figure 10 Test Circuit 2 (SENSE detection product)**

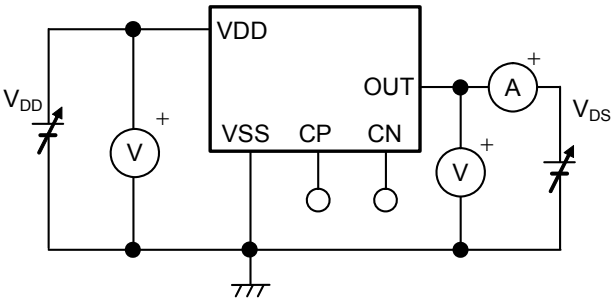



**Figure 11 Test Circuit 3 (VDD detection product)**

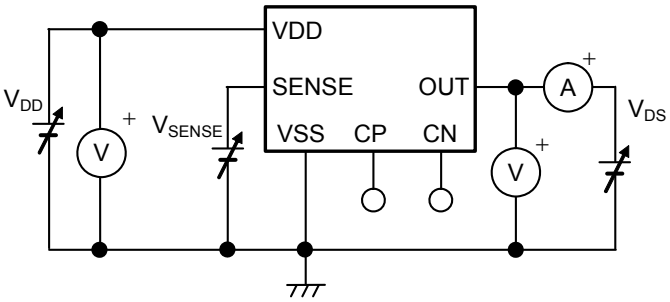



**Figure 12 Test Circuit 3 (SENSE detection product)**

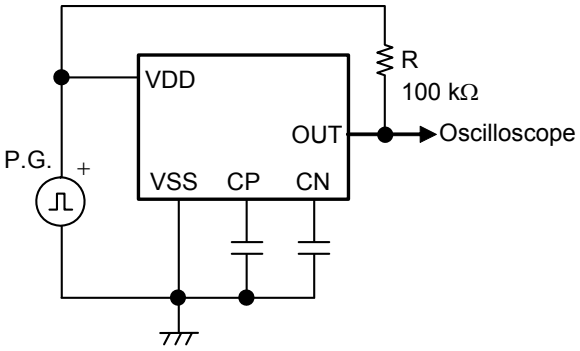



**Figure 13 Test Circuit 4 (VDD detection product)**

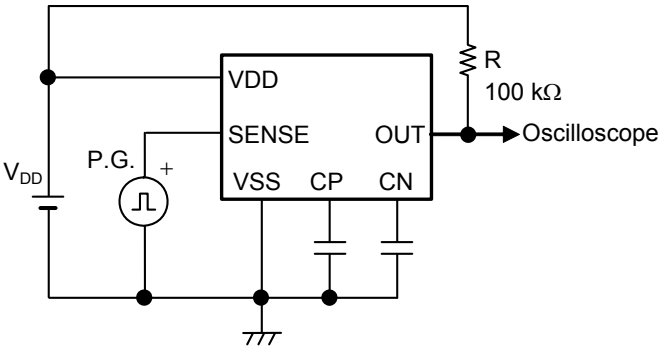
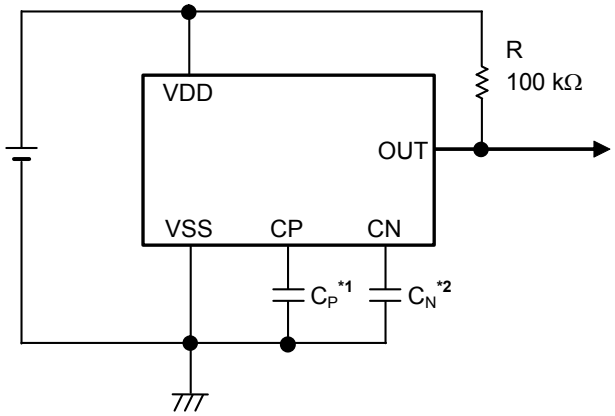



**Figure 14 Test Circuit 4 (SENSE detection product)**

## ■ Standard Circuits

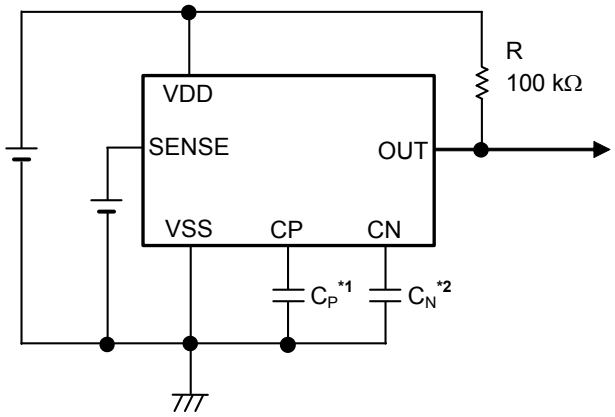
### 1. VDD detection product




***1.** The delay capacitor ($C_P$) should be connected directly to the CP pin and the VSS pin.
***2.** The delay capacitor ($C_N$) should be connected directly to the CN pin and the VSS pin.

**Figure 15**

### 2. SENSE detection product




***1.** The delay capacitor ($C_P$) should be connected directly to the CP pin and the VSS pin.
***2.** The delay capacitor ($C_N$) should be connected directly to the CN pin and the VSS pin.

**Figure 16**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Explanation of Terms

### 1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 21** or **Figure 22** turns to "L" (VDD detection product: $V_{DD}$, SENSE detection product: $V_{SENSE}$). The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 17**, **Figure 19**).

Example: In $-V_{DET}$ = 5.0 V product, the detection voltage is either one in the range of 4.925 V ≤ $-V_{DET}$ ≤ 5.075 V.
This means that some $-V_{DET}$ = 5.0 V product have $-V_{DET}$ = 4.925 V and some have $-V_{DET}$ = 5.075 V.

### 2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 21** or **Figure 22** turns to "H" (VDD detection product: $V_{DD}$, SENSE detection product: $V_{SENSE}$).
The difference of detection voltage and release voltage is 5.0% typ.
The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 18**, **Figure 20**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product.
In the S-1011 Series C / G / L / Q type, the release voltage ($+V_{DET}$) is the same value as the actual detection voltage ($-V_{DET}$) of a product.

Example: In $-V_{DET}$ = 6.0 V product, the release voltage is either one in the range of 6.0873 V ≤ $+V_{DET}$ ≤ 6.5772 V.
This means that some $-V_{DET}$ = 6.0 V product have $+V_{DET}$ = 6.0873 V and some have $+V_{DET}$ = 6.5772 V.

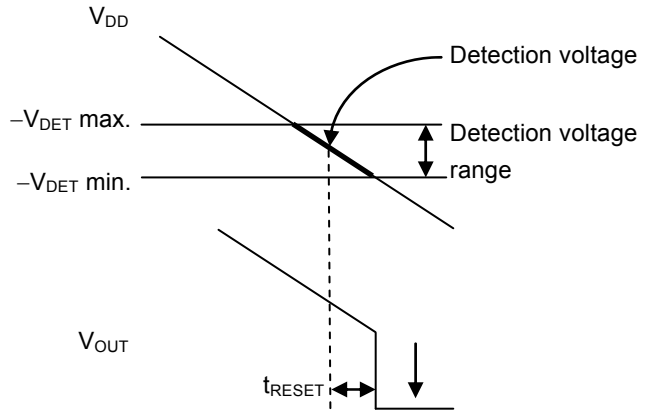



**Figure 17 Detection Voltage (VDD detection product)**

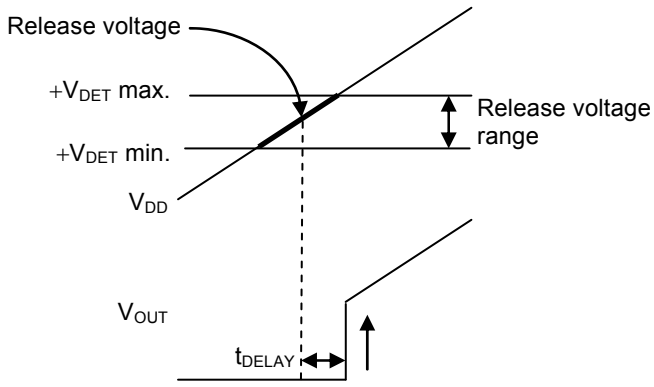



**Figure 18 Release Voltage (VDD detection product)**

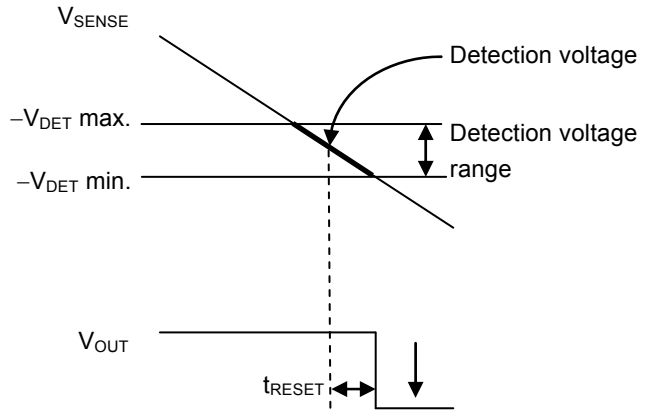



**Figure 19 Detection Voltage (SENSE detection product)**

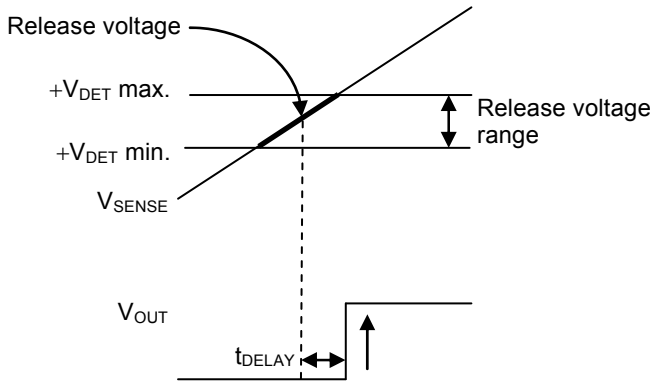



**Figure 20 Release Voltage (SENSE detection product)**

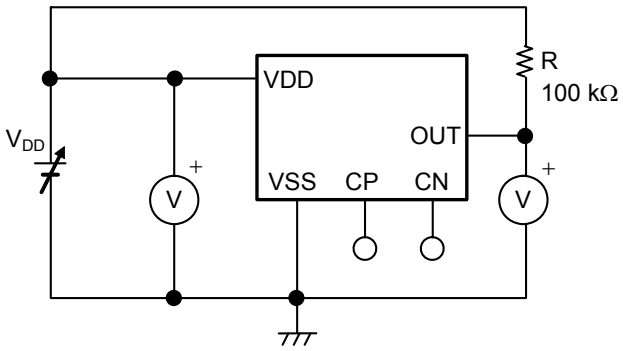



**Figure 21 Test Circuit of Detection Voltage and Release Voltage (VDD detection product)**

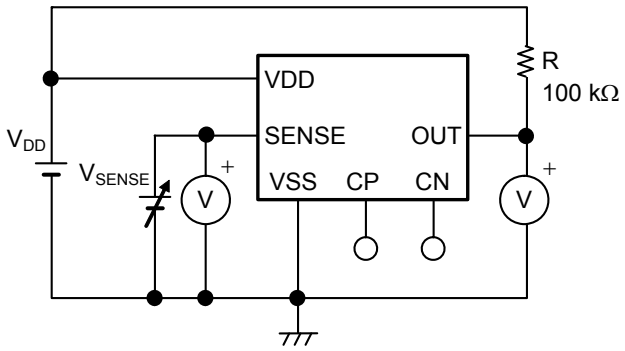



**Figure 22 Test Circuit of Detection Voltage and Release Voltage (SENSE detection product)**

### 3. Hysteresis width ($V_{HYS}$)

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B − the voltage at point A = $V_{HYS}$ in **Figure 24** and **Figure 28**). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

### 4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.

## ■ Operation

### 1. Basic operation

#### 1. 1 S-1011 Series A / J type

(1) When the power supply voltage ($V_{DD}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output $V_{DD}$ ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

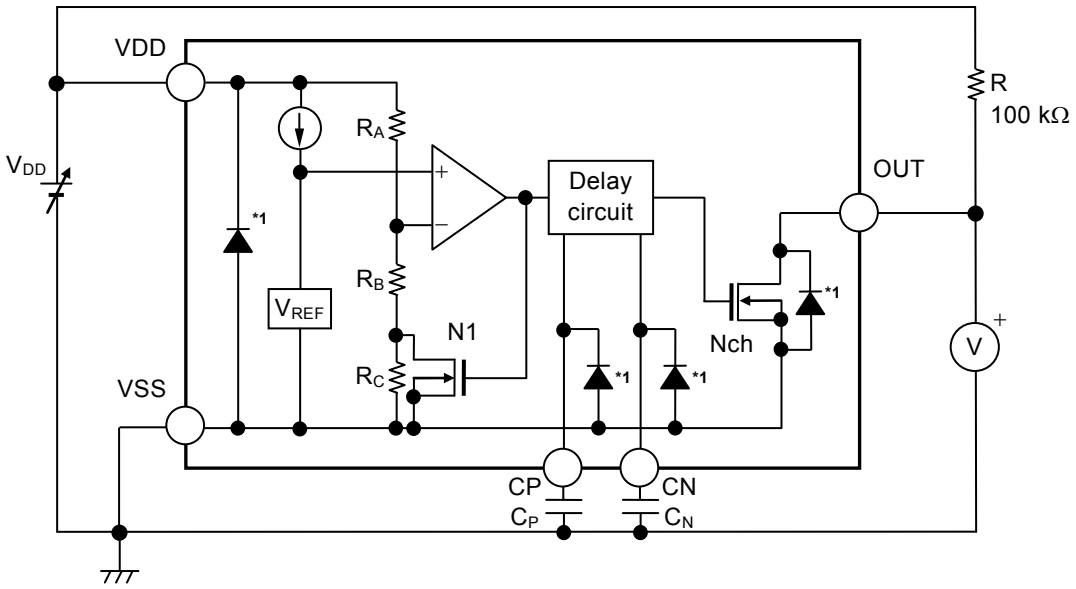
(2) Even if $V_{DD}$ decreases to $+V_{DET}$ or lower, $V_{DD}$ is output when $V_{DD}$ is higher than the detection voltage ($-V_{DET}$). When $V_{DD}$ decreases to $-V_{DET}$ or lower (point A in **Figure 24**), the Nch transistor is turned on. And then $V_{SS}$ ("L") is output from the OUT pin after the elapse of the detection delay time ($t_{RESET}$).

At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) The output is unstable when $V_{DD}$ decreases to the IC's minimum operation voltage or lower. $V_{DD}$ is output when the output is pulled up.

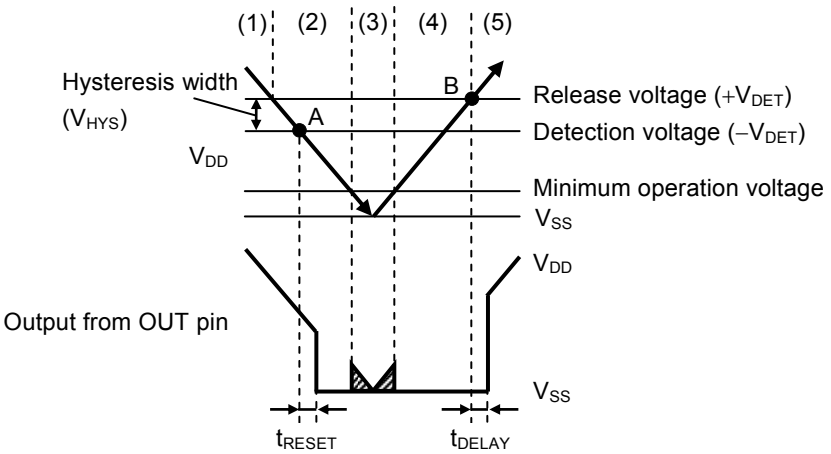
(4) $V_{SS}$ is output by increasing $V_{DD}$ to the minimum operation voltage or higher. Even if $V_{DD}$ exceeds $-V_{DET}$, $V_{SS}$ is output when $V_{DD}$ is lower than $+V_{DET}$.

(5) When $V_{DD}$ increases to $+V_{DET}$ or higher (point B in **Figure 24**), the Nch transistor is turned off. And then $V_{DD}$ is output from the OUT pin after the elapse of the release delay time ($t_{DELAY}$) when the output is pulled up.




***1.** Parasitic diode

**Figure 23 Operation of S-1011 Series A / J Type**




**Remark** When $V_{DD}$ is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

**Figure 24 Timing Chart of S-1011 Series A / J Type**

### 1. 2 S-1011 Series C / L type

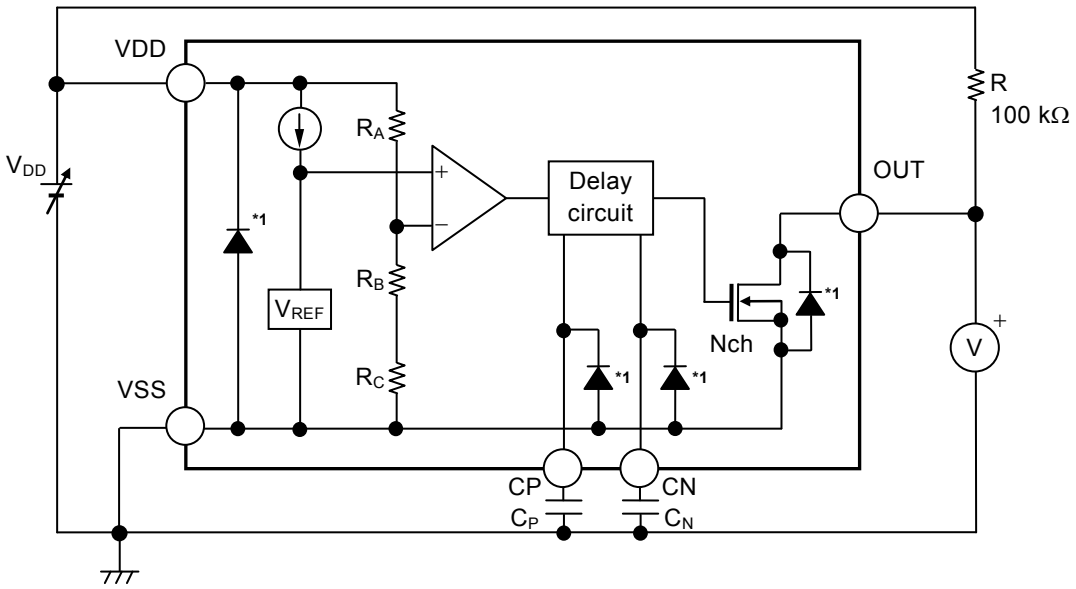
(1) When the power supply voltage ($V_{DD}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output $V_{DD}$ ("H") when the output is pulled up.
At this time, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) When $V_{DD}$ decreases to the detection voltage ($-V_{DET}$) or lower (point A in **Figure 26**), the Nch transistor is turned on. And then $V_{SS}$ ("L") is output from the OUT pin after the elapse of the detection delay time ($t_{RESET}$).

(3) The output is unstable when $V_{DD}$ decreases to the IC's minimum operation voltage or lower. $V_{DD}$ is output when the output is pulled up.

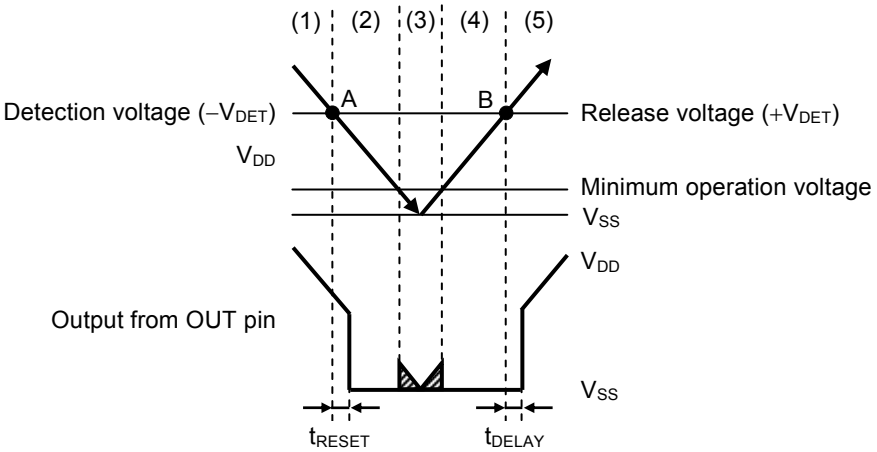
(4) $V_{SS}$ is output by increasing $V_{DD}$ to the minimum operation voltage or higher.

(5) When $V_{DD}$ increases to $+V_{DET}$ or higher (point B in **Figure 26**), the Nch transistor is turned off. And then $V_{DD}$ is output from the OUT pin after the elapse of the release delay time ($t_{DELAY}$) when the output is pulled up.




***1.** Parasitic diode

**Figure 25 Operation of S-1011 Series C / L Type**




**Remark 1.** When $V_{DD}$ is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

**2.** The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

**Figure 26 Timing Chart of S-1011 Series C / L Type**

### 1. 3 S-1011 Series E / N type

(1) When the power supply voltage ($V_{DD}$) is the minimum operation voltage or higher, and the SENSE pin voltage ($V_{SENSE}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output $V_{DD}$ ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if $V_{SENSE}$ decreases to $+V_{DET}$ or lower, $V_{DD}$ is output when $V_{SENSE}$ is higher than the detection voltage ($-V_{DET}$).

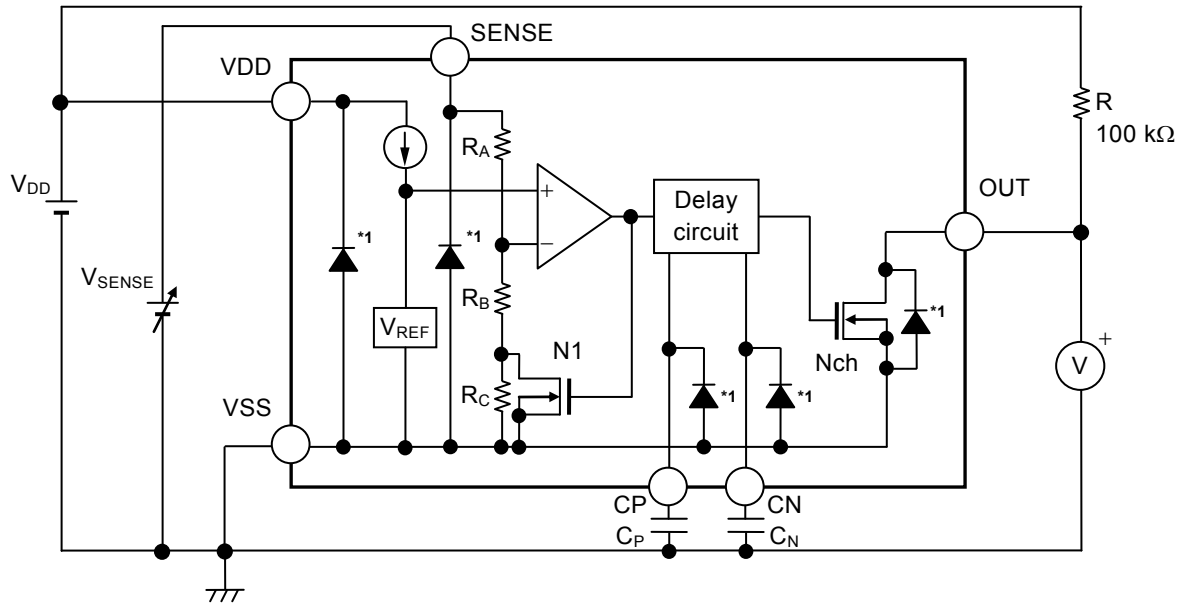
When $V_{SENSE}$ decreases to $-V_{DET}$ or lower (point A in **Figure 28**), the Nch transistor is turned on. And then $V_{SS}$ ("L") is output from the OUT pin after the elapse of the detection delay time ($t_{RESET}$).

At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if $V_{SENSE}$ further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when $V_{DD}$ is minimum operation voltage or higher.

(4) Even if $V_{SENSE}$ exceeds $-V_{DET}$, $V_{SS}$ is output when $V_{SENSE}$ is lower than $+V_{DET}$.

(5) When $V_{SENSE}$ increases to $+V_{DET}$ or higher (point B in **Figure 28**), the Nch transistor is turned off. And then $V_{DD}$ is output from the OUT pin after the elapse of the release delay time ($t_{DELAY}$) when the output is pulled up.




***1.** Parasitic diode

**Figure 27 Operation of S-1011 Series E / N Type**

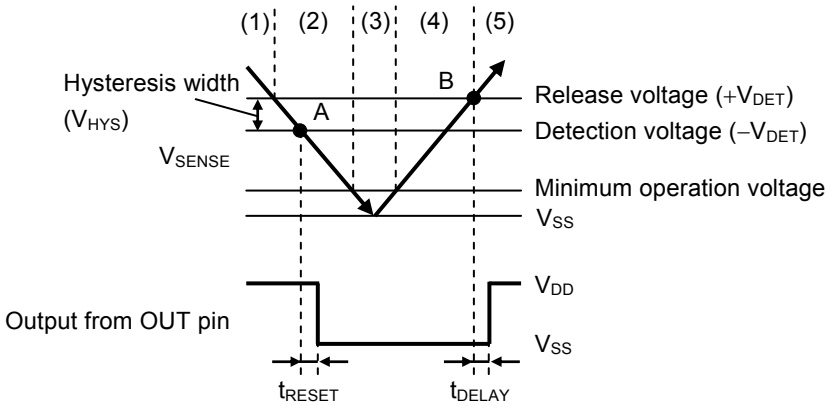



**Figure 28 Timing Chart of S-1011 Series E / N Type**

### 1. 4 S-1011 Series G / Q type

(1) When the power supply voltage ($V_{DD}$) is the minimum operation voltage or higher, and the SENSE pin voltage ($V_{SENSE}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output $V_{DD}$ ("H") when the output is pulled up.

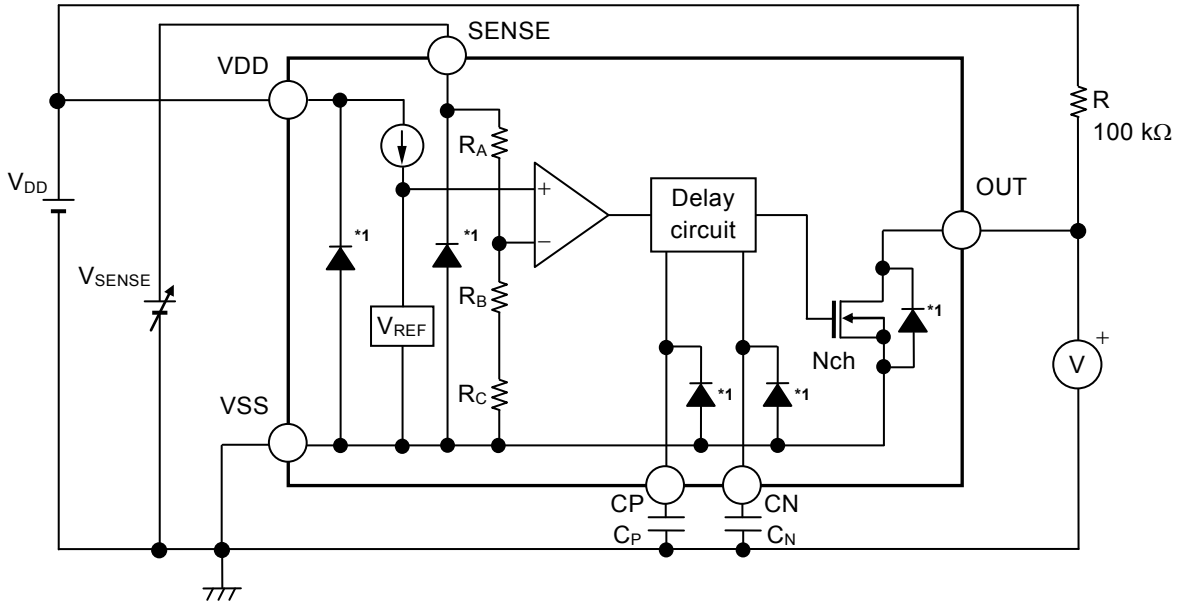
At this time, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) When $V_{SENSE}$ decreases to the detection voltage ($-V_{DET}$) or lower (point A in **Figure 30**), the Nch transistor is turned on. And then $V_{SS}$ ("L") is output from the OUT pin after the elapse of the detection delay time ($t_{RESET}$).

(3) Even if $V_{SENSE}$ further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when $V_{DD}$ is minimum operation voltage or higher.

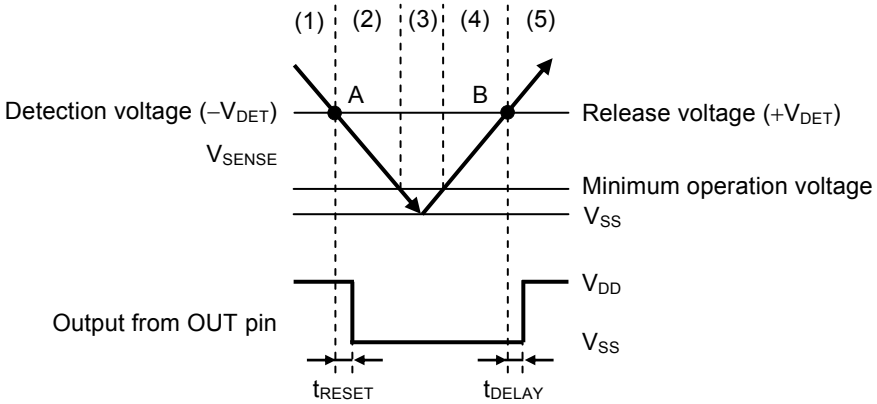
(4) Even if $V_{SENSE}$ increases, $V_{SS}$ is output when $V_{SENSE}$ is lower than $+V_{DET}$.

(5) When $V_{SENSE}$ increases to $+V_{DET}$ or higher (point B in **Figure 30**), the Nch transistor is turned off. And then $V_{DD}$ is output from the OUT pin after the elapse of the release delay time ($t_{DELAY}$) when the output is pulled up.




***1.*** Parasitic diode

**Figure 29 Operation of S-1011 Series G / Q Type**




**Remark** The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

**Figure 30 Timing Chart of S-1011 Series G / Q Type**

## 2. SENSE pin

### 2. 1 Error when detection voltage is set externally

The detection voltage for the S-1011 Series is 10.0 V max., however, in the SENSE detection product with $-V_{DET}$ = 10.0 V, the detection voltage can be set externally by connecting a node that was resistance-divided by the resistor ($R_A$) and the resistor ($R_B$) to the SENSE pin as shown in **Figure 31**.
For conventional products without the SENSE pin, external resistor cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if external resistor is large, problems such as oscillation or larger error in the hysteresis width may occur.
In the S-1011 Series, $R_A$ and $R_B$ in **Figure 31** are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance ($R_{SENSE}$) that will occur.
Although $R_{SENSE}$ in the S-1011 Series is large (the S-1011 Series E / G type: 26 MΩ min., the S-1011 Series N / Q type: 6.8 MΩ min.) to make the error small, $R_A$ and $R_B$ should be selected such that the error is within the allowable limits.

### 2. 2 Selection of $R_A$ and $R_B$

In **Figure 31**, the relation between the external setting detection voltage ($V_{DX}$) and the actual detection voltage ($-V_{DET}$) is ideally calculated by the equation below.

$$V_{DX} = -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) \quad \cdots (1)$$

However, in reality there is an error in the current flowing through $R_{SENSE}$.
When considering this error, the relation between $V_{DX}$ and $-V_{DET}$ is calculated as follows.

$$\begin{aligned} V_{DX} &= -V_{DET} \times \left(1 + \frac{R_A}{R_B \parallel R_{SENSE}}\right) \\ &= -V_{DET} \times \left(1 + \frac{R_A}{\frac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\ &= -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times -V_{DET} \quad \cdots (2) \end{aligned}$$

By using equations (1) and (2), the error is calculated as $-V_{DET} \times \frac{R_A}{R_{SENSE}}$.

The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100\ [\%] = \frac{R_A \parallel R_B}{R_{SENSE}} \times 100\ [\%] \quad \cdots (3)$$

As seen in equation (3), the smaller the resistance values of $R_A$ and $R_B$ compared to $R_{SENSE}$, the smaller the error rate becomes.

Also, the relation between the external setting hysteresis width ($V_{HX}$) and the hysteresis width ($V_{HYS}$) is calculated by equation below. Error due to $R_{SENSE}$ also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right) \quad \cdots (4)$$

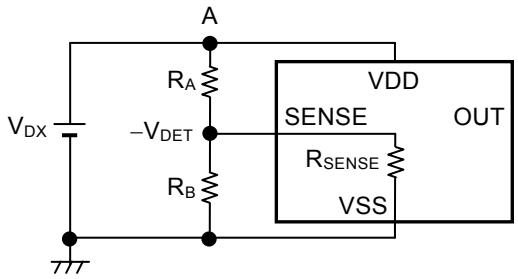



**Figure 31 Detection Voltage External Setting Circuit**

**Caution 1. When externally setting the detection voltage, perform the operation with $-V_{DET}$ = 10.0 V product. Contact our sales office for details.**

**2. If the current flowing through $R_B$ is set to 1 μA or less, the error may become larger.**

**3. If the parasitic resistance and parasitic inductance between $V_{DX}$ – point A and point A – VDD pin are larger, oscillation may occur. Perform thorough evaluation using the actual application.**

**4. If $R_A$ and $R_B$ are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.**

### 3. Delay circuit

The delay circuit has a function that adjusts the detection delay time ($t_{RESET}$) from when the power supply voltage ($V_{DD}$) or SENSE pin voltage ($V_{SENSE}$) reaches the detection voltage ($-V_{DET}$) or lower to when the output from OUT pin inverts.
It also has a function that adjusts the release delay time ($t_{DELAY}$) from when the power supply voltage ($V_{DD}$) or SENSE pin voltage ($V_{SENSE}$) reaches the release voltage ($+V_{DET}$) to when the output from OUT pin inverts.
$t_{RESET}$ is determined by the delay coefficient, the delay capacitor ($C_N$) and the detection delay time when the CN pin is open ($t_{RESET0}$), and the $t_{DELAY}$ is determined by the delay coefficient, the delay capacitor ($C_P$) and the release delay time when the CP pin is open ($t_{DELAY0}$). They are calculated by the equation below.

$t_{RESET}$ [ms] = Delay coefficient $\times$ $C_N$ [nF] + $t_{RESET0}$ [ms]
$t_{DELAY}$ [ms] = Delay coefficient $\times$ $C_P$ [nF] + $t_{DELAY0}$ [ms]

**Table 19**

| Operation Temperature | Delay Coefficient | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| Ta = +85°C | 2.41 | 2.85 | 3.32 |
| Ta = +25°C | 2.41 | 2.86 | 3.30 |
| Ta = −40°C | 2.40 | 2.83 | 3.25 |

**Table 20**

| Operation Temperature | Detection Delay Time when CN Pin is Open ($t_{RESET0}$) | Release Delay Time when CP Pin is Open ($t_{DELAY0}$) |
|---|---|---|
| | Typ. | Typ. |
| Ta = −40°C to +85°C | 0.35 ms | 0.35 ms |

**Caution 1. Mounted board layout should be made in such a way that no current flows into or flows from the CN pin or CP pin since the impedance of the CN pin and CP pin are high, otherwise correct delay time cannot be provided.**

**2. There is no limit for the capacitance of $C_N$ and $C_P$ as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 300 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.**

**3. The above equation will not guarantee successful operation. Determine the capacitance of $C_N$ and $C_P$ through thorough evaluation including temperature characteristics in the actual usage conditions.**
**When using an X8R equivalent capacitor, refer to the "2. Detection delay time ($t_{RESET}$) vs. Temperature (Ta)", "3. Detection delay time ($t_{RESET}$) vs. Power supply voltage ($V_{DD}$)", "5. Release delay time ($t_{DELAY}$) vs. Temperature (Ta)" and "6. Release delay time ($t_{DELAY}$) vs. Power supply voltage ($V_{DD}$)" in "■ Reference Data" for details.**

## ■ Usage Precautions

### 1. Feed-through current during detection and release

In the S-1011 Series, the feed-through current flows at the time of detection and release. For this reason, if the input impedance is high, oscillation may occur due to voltage drop caused by the feed-through current.
When using the S-1011 Series in configurations like those shown in **Figure 32** and **Figure 33**, it is recommended that input impedance be set to 1 kΩ or less.
Determine the impedance through thorough evaluation including temperature characteristics.

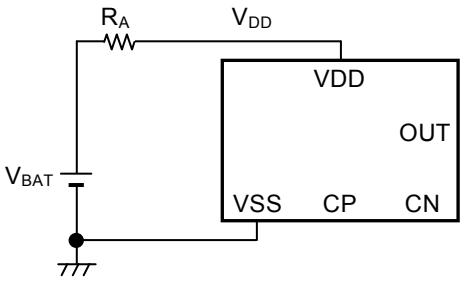



**Figure 32 VDD Detection Product**

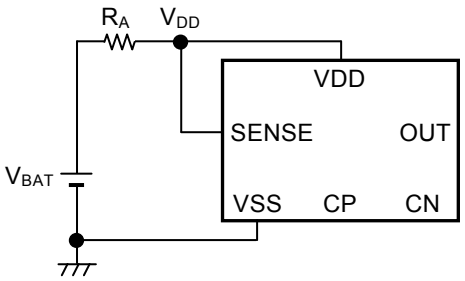



**Figure 33 SENSE Detection Product**

## 2. Power on and shut down sequence

SENSE detection products monitor SENSE pin voltage ($V_{SENSE}$) while power is being supplied to the VDD pin.
Apply power in the order, the VDD pin then the SENSE pin.
In addition, when shutting down VDD pin, shut down the SENSE pin first, and shut down the VDD pin after the detection delay time ($t_{RESET}$) has elapsed.

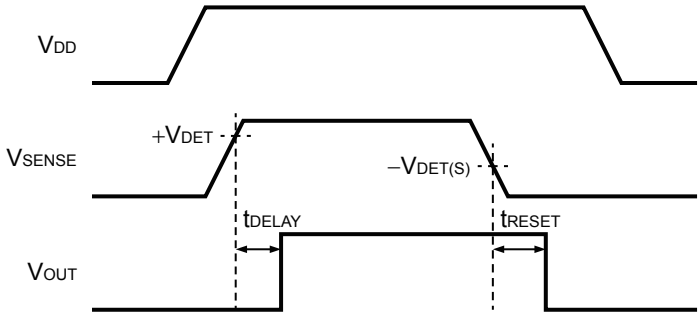



**Figure 34**

## 3. Falling power (reference)

**Figure 35** shows the relation between $V_{DD}$ amplitude ($V_{P-P}$) and input voltage falling time ($t_F$) where the release status can be maintained when the VDD pin (VDD detection product) sharply drops to a voltage equal to or higher than the detection voltage ($-V_{DET}$) during release status.

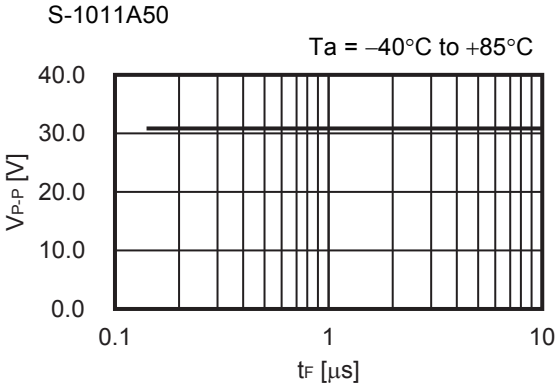
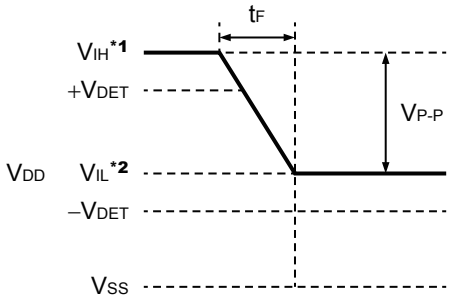



**Figure 35**




***1.** $V_{IH}$ = 36.0 V
***2.** $V_{IL} = -V_{DET(S)} + 1.0$ V

**Figure 36 VDD Pin Input Voltage Waveform**

**Caution Figure 35 shows the input voltage conditions which can maintain the release status. If the voltage whose $V_{P-P}$ and $t_F$ are larger than these conditions is input to the VDD pin (VDD detection product), the OUT pin may change to a detection status.**

### 4. Detection delay time accuracy (reference)

**Figure 37** and **Figure 38** show the relation between $V_{DD}$ amplitude ($V_{P-P}$) and input voltage falling time ($t_F$) where the arbitrarily set detection delay time accuracy can be maintained when the VDD pin (VDD detection product) sharply drops.

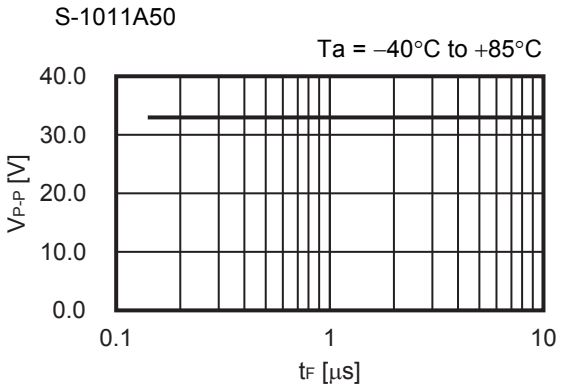



**Figure 37 $C_N$ = 3.3 nF**

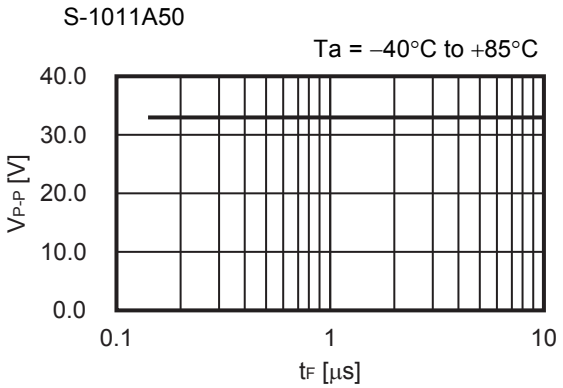
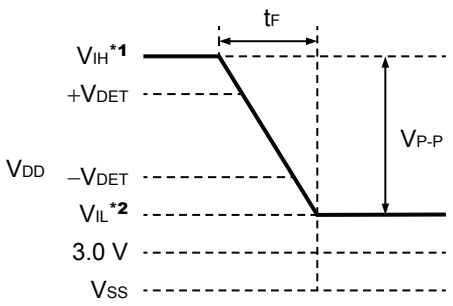



**Figure 38 $C_N$ = 100 nF**




***1.** $V_{IH}$ = 36.0 V
***2.** $V_{IL} = -V_{DET(S)} - 1.0$ V (3.0 V min.)

**Figure 39 VDD Pin Input Voltage Waveform**

**Caution Figure 37 and Figure 38 show the input voltage conditions which can maintain the detection delay time accuracy. If the voltage whose $V_{P-P}$ and $t_F$ are larger than these conditions is input to the VDD pin (VDD detection product), the desired detection delay time may not be achieved.**

### 5. $V_{DD}$ drop during release delay time (reference)

**Figure 40** and **Figure 41** show the relation between pulse width ($t_{PW}$) and $V_{DD}$ lower limit ($V_{DROP}$) where a release signal can be output after the normal release delay time has elapsed when the VDD pin (VDD detection product) instantaneously drops to the detection voltage ($-V_{DET}$) or lower and then increases to the release voltage ($+V_{DET}$) or higher during release delay time.

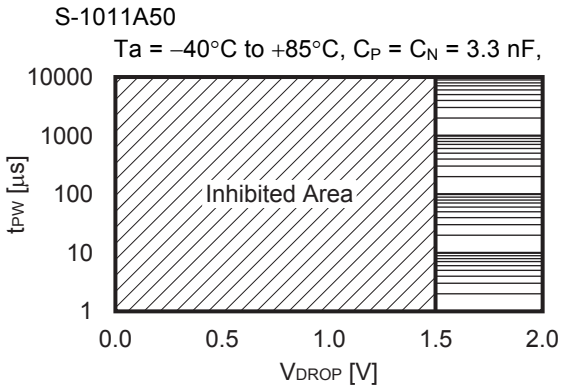



**Figure 40**

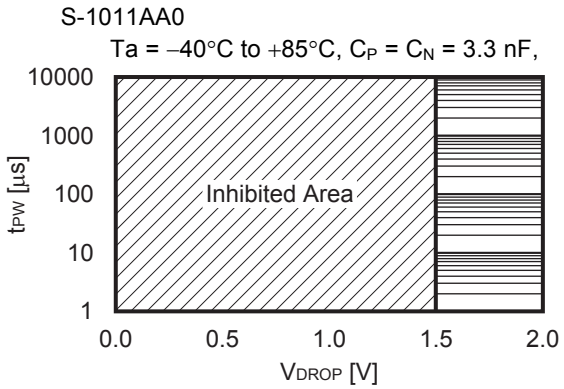
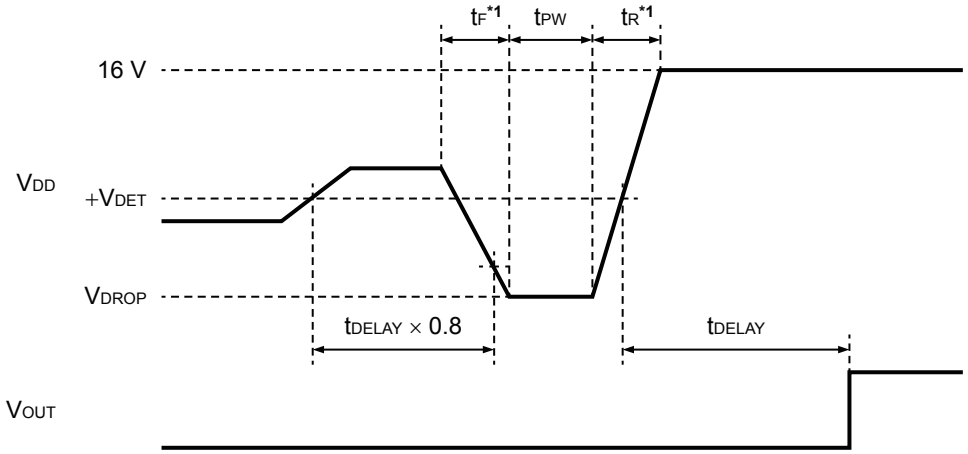



**Figure 41**




***1.** $t_R = t_F = 10\ \mu s$

**Figure 42 VDD Pin Input Voltage Waveform**

**Caution 1. Figure 40 and Figure 41 show the input voltage conditions when a release signal is output after the normal release delay time has elapsed. When this is within the inhibited area, release may erroneously be executed before the delay time completes.**

**2. When the VDD pin voltage is within the inhibited areas shown in Figure 40 and Figure 41 during release delay time, input 0 V to the VDD pin then restart the S-1011 Series.**

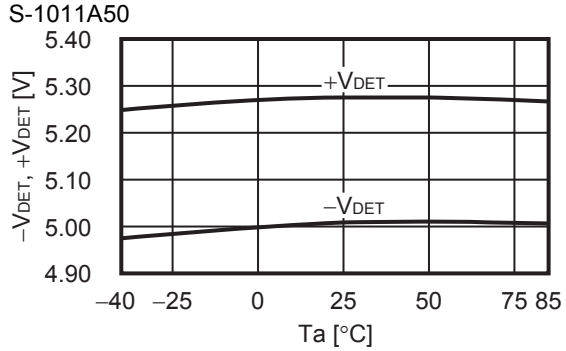
## ■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Because the SENSE pin has a high impedance, malfunctions may occur due to noise.
  Be careful of wiring adjoining SENSE pin wiring in actual applications.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

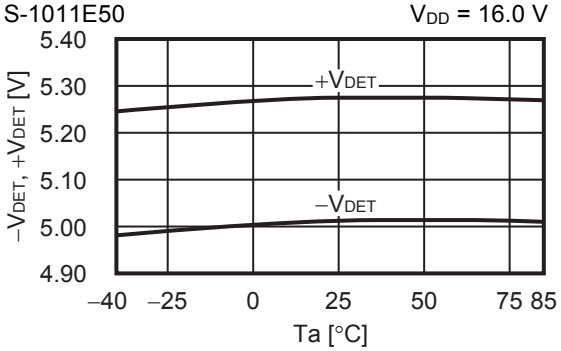
## ■ Characteristics (Typical Data)

### 1. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Temperature (Ta)

#### 1. 1 VDD detection product

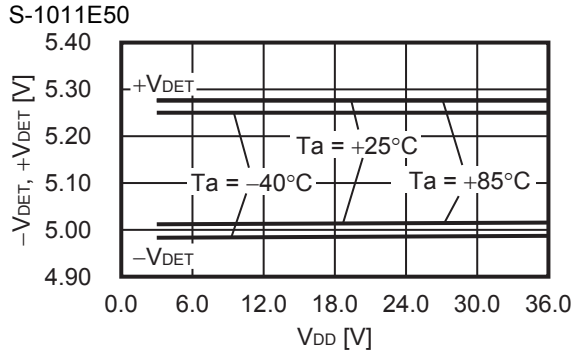



#### 1. 2 SENSE detection product



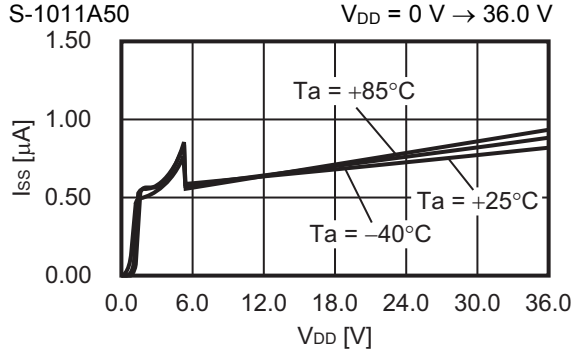

### 2. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Power supply voltage ($V_{DD}$)

#### 2. 1 SENSE detection product

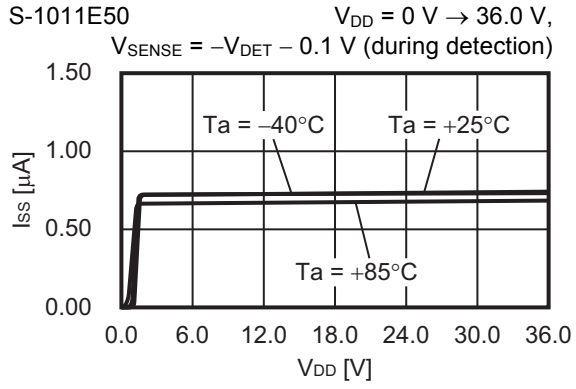


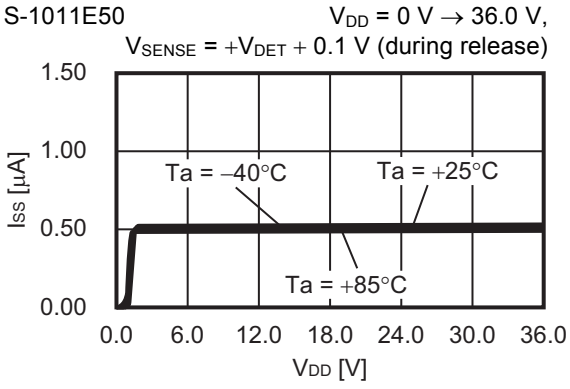

### 3. Current consumption ($I_{SS}$) vs. Power supply voltage ($V_{DD}$)

#### 3. 1 VDD detection product




#### 3. 2 SENSE detection product



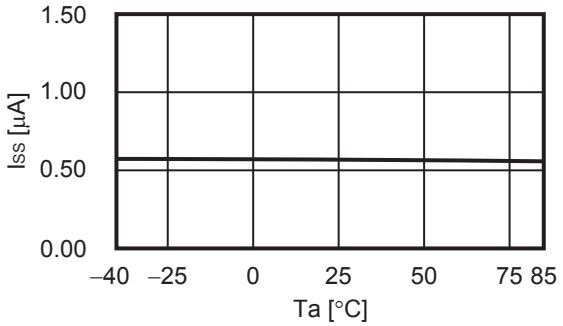



## 4. Current consumption ($I_{SS}$) vs. Temperature (Ta)

### 4. 1 VDD detection product

S-1011A50

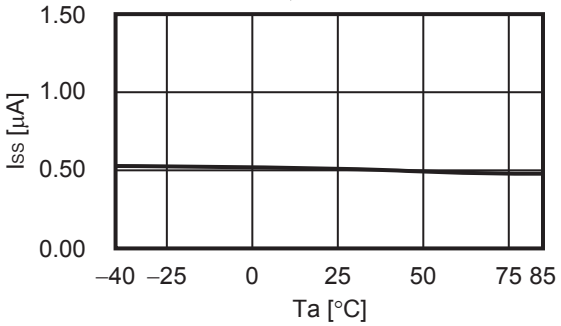
$V_{DD}$ = $+V_{DET}$ + 0.1 V




### 4. 2 SENSE detection product

S-1011E50

$V_{DD}$ = 16.0 V, $V_{SENSE}$ = $+V_{DET}$ + 0.1 V

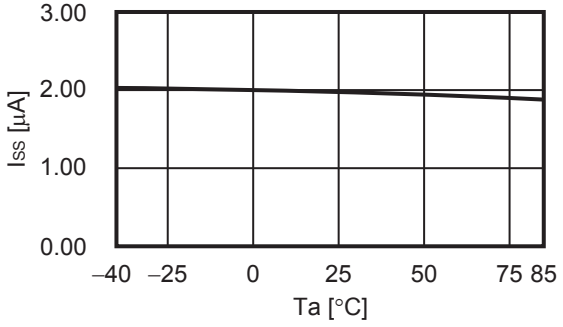



## 5. Current consumption during detection delay ($I_{SS}$) vs. Temperature (Ta)

### 5. 1 VDD detection product

S-1011A50

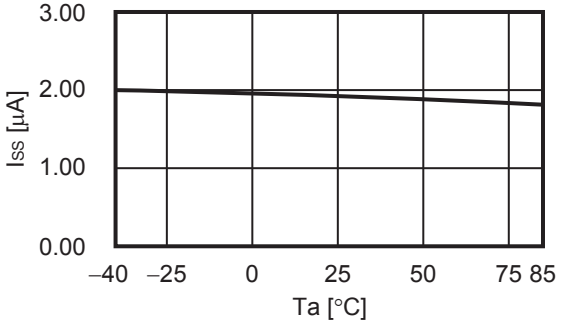
$V_{CN}$ = 0.2 V




### 5. 2 SENSE detection product

S-1011E50

$V_{DD}$ = 16.0 V, $V_{CN}$ = 0.2 V

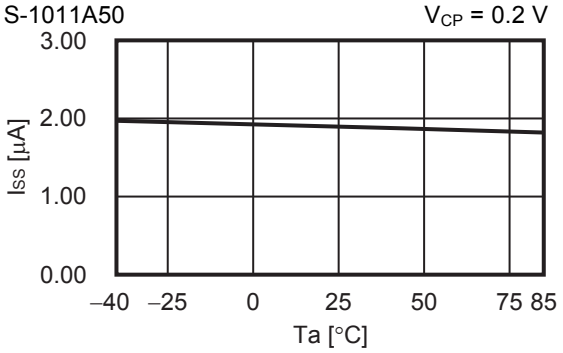



## 6. Current consumption during release delay ($I_{SS}$) vs. Temperature (Ta)

### 6. 1 VDD detection product

S-1011A50

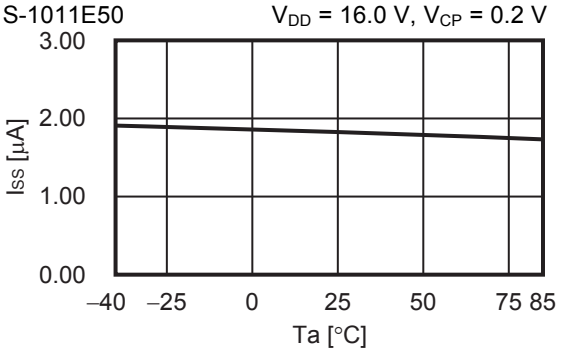
$V_{CP}$ = 0.2 V




### 6. 2 SENSE detection product

S-1011E50

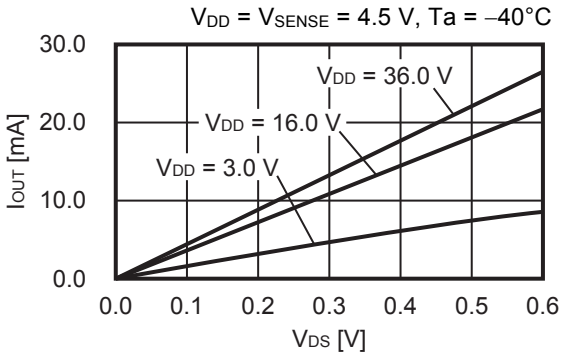
$V_{DD}$ = 16.0 V, $V_{CP}$ = 0.2 V



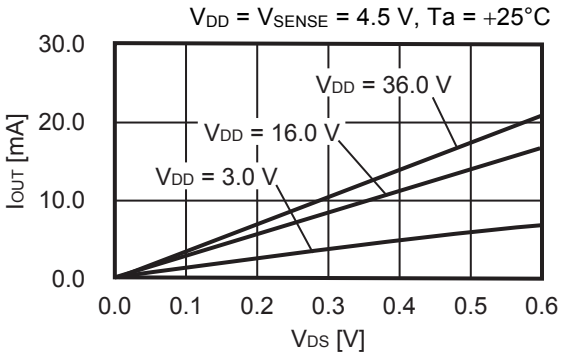
## 7. Nch transistor output current ($I_{OUT}$) vs. $V_{DS}$

### 7. 1 SENSE detection product

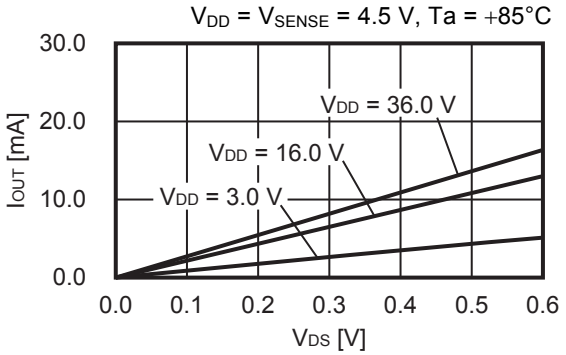
S-1011E50




S-1011E50



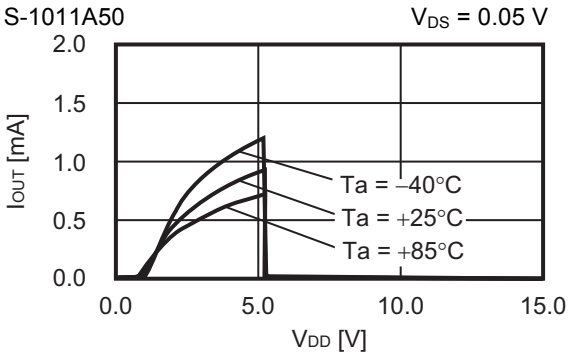

S-1011E50




## 8. Nch transistor output current ($I_{OUT}$) vs. Power supply voltage ($V_{DD}$)

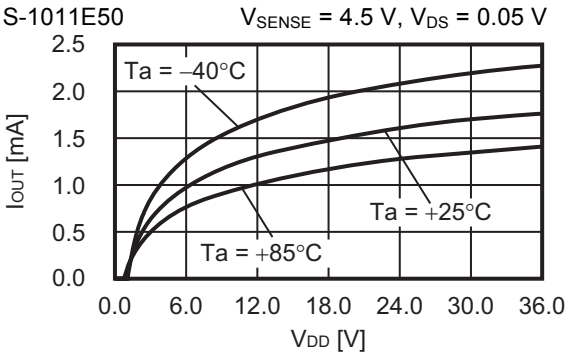
### 8. 1 VDD detection product

S-1011A50




### 8. 2 SENSE detection product

S-1011E50



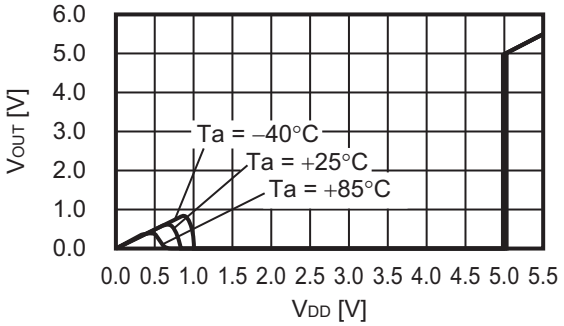

**Remark** $V_{DS}$: Drain-to-source voltage of the output transistor

## 9. Minimum operation voltage ($V_{OUT}$) vs. Power supply voltage ($V_{DD}$)

### 9. 1 VDD detection product

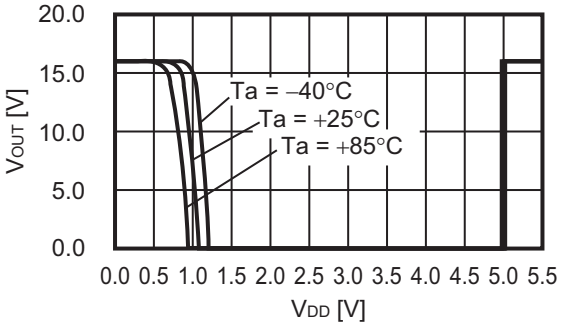
S-1011A50

Pull-up to $V_{DD}$, Pull-up resistance: 100 kΩ




S-1011A50

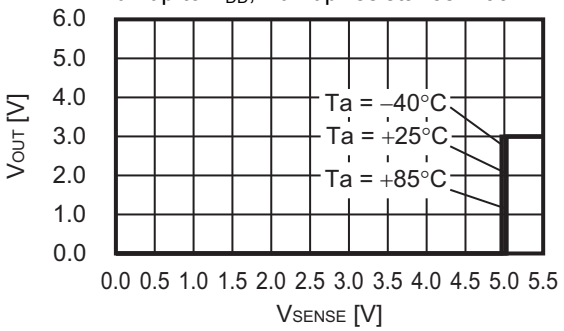
Pull-up to 16.0 V, Pull-up resistance: 100 kΩ




### 9. 2 SENSE detection product

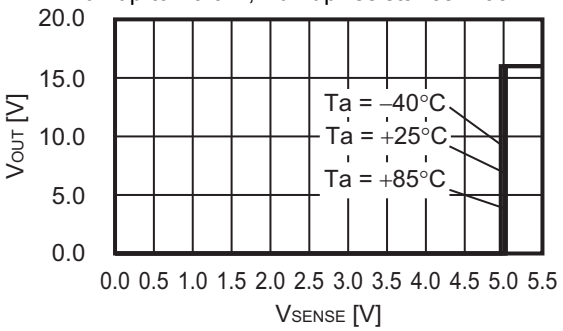
S-1011E50 $V_{DD}$ = 3.0 V,

Pull-up to $V_{DD}$, Pull-up resistance: 100 kΩ



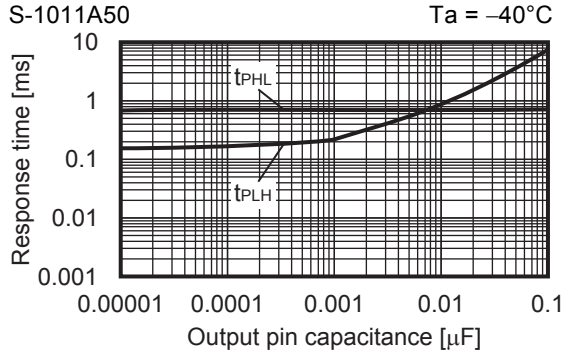

S-1011E50 $V_{DD}$ = 3.0 V,

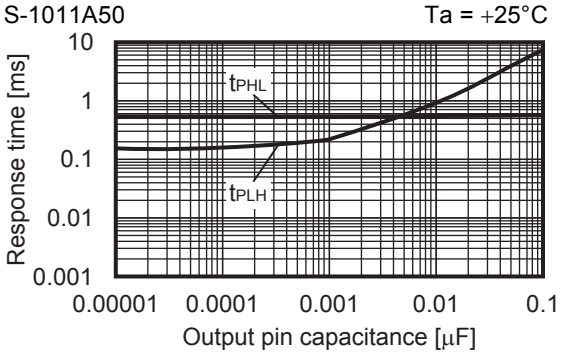
Pull-up to 16.0 V, Pull-up resistance: 100 kΩ

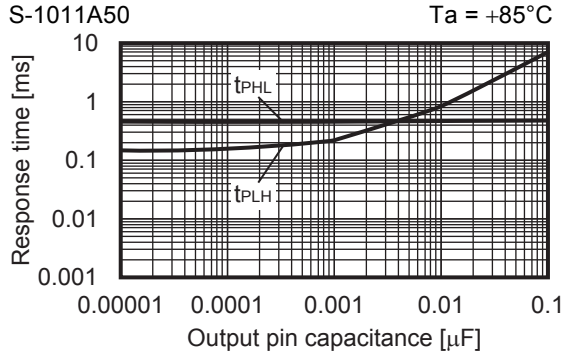


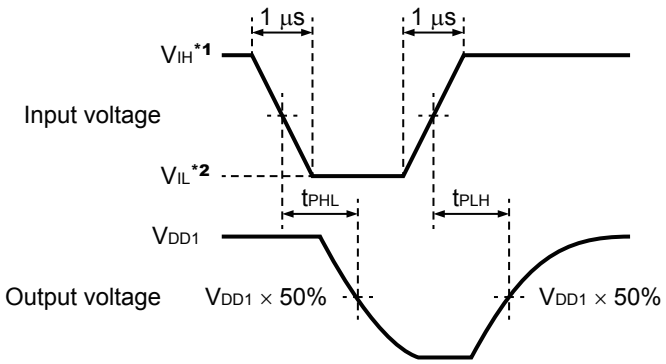
## 10. Dynamic response vs. Output pin capacitance ($C_{OUT}$) (CP pin, CN pin; open)

### 10. 1 VDD detection product




*1. $V_{IH}$ = 36.0 V
*2. $V_{IL}$ = 3.0 V

**Figure 43 Test Condition of Response Time**

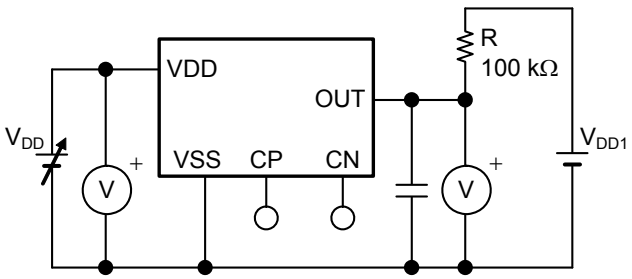



**Figure 44 Test Circuit of Response Time**

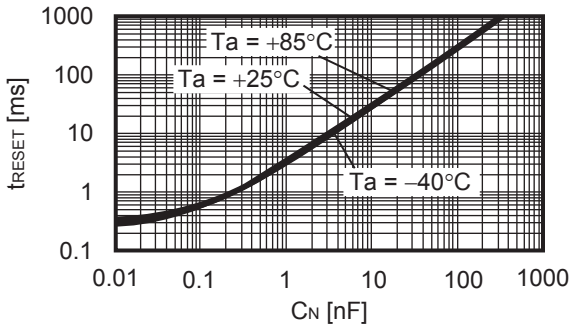
**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Reference Data

### 1. Detection delay time ($t_{RESET}$) vs. CN pin capacitance ($C_N$) (Without output pin capacitance)

#### 1. 1 VDD detection product

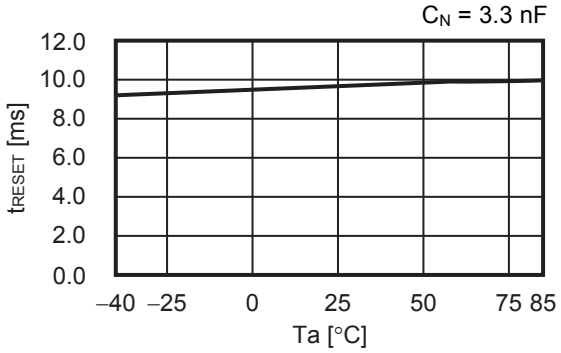
S-1011A50

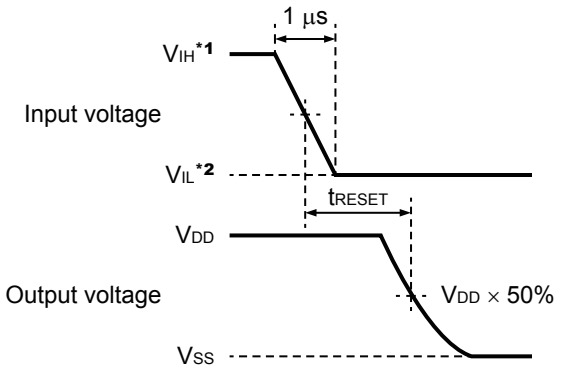


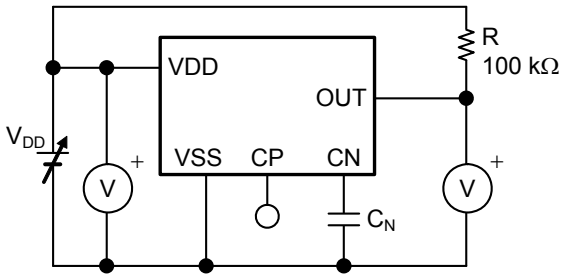

### 2. Detection delay time ($t_{RESET}$) vs. Temperature (Ta)

#### 2. 1 VDD detection product

S-1011A50




***1.** $V_{IH} = -V_{DET(S)} + 1.0$ V
***2.** $V_{IL} = -V_{DET(S)} - 1.0$ V

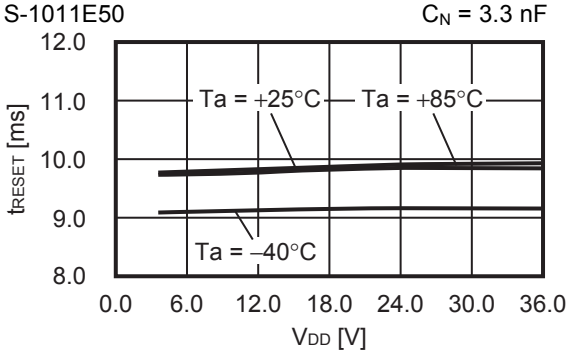
**Figure 45 Test Condition of Detection Delay Time**

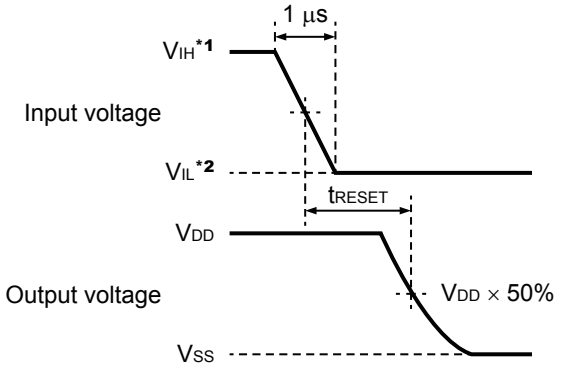
**Figure 46 Test Circuit of Detection Delay Time**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## 3. Detection delay time ($t_{RESET}$) vs. Power supply voltage ($V_{DD}$)

### 3. 1 SENSE detection product




***1.** $V_{IH} = -V_{DET(S)} + 1.0$ V
***2.** $V_{IL} = -V_{DET(S)} - 1.0$ V

**Figure 47 Test Condition of Detection Delay Time**

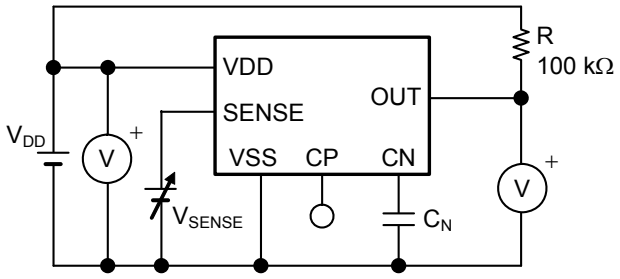


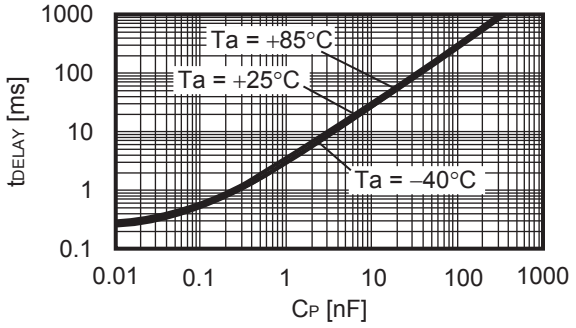

**Figure 48 Test Circuit of Detection Delay Time**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## 4. Release delay time ($t_{DELAY}$) vs. CP pin capacitance ($C_P$) (Without output pin capacitance)

### 4. 1 VDD detection product

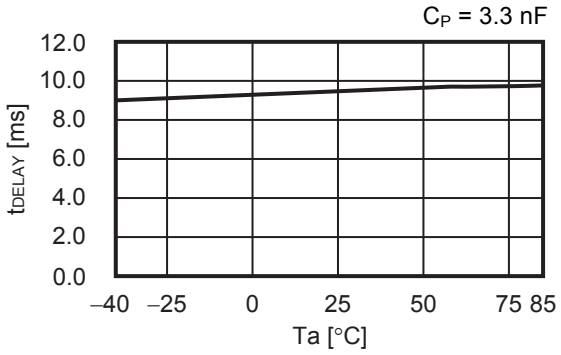
S-1011A50

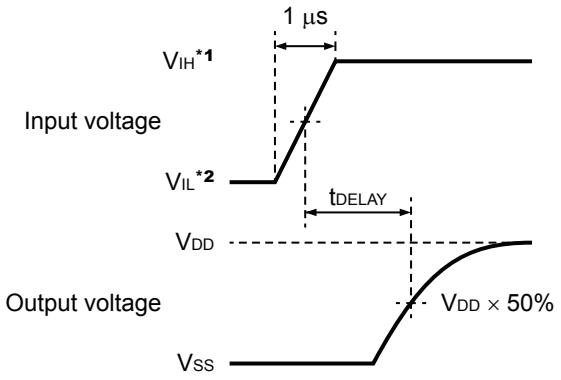


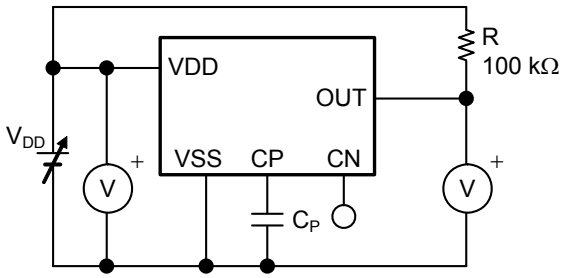

## 5. Release delay time ($t_{DELAY}$) vs. Temperature (Ta)

### 5. 1 VDD detection product

S-1011A50




***1.** $V_{IH} = +V_{DET} + 1.0$ V
***2.** $V_{IL} = +V_{DET} - 1.0$ V

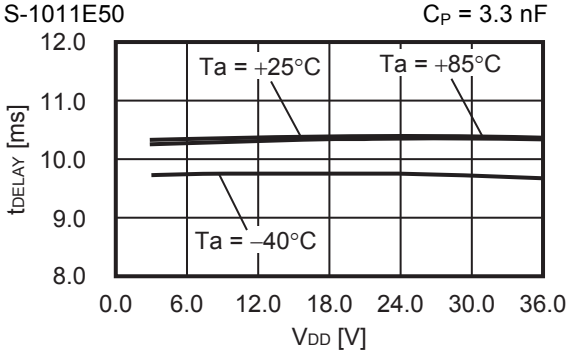
**Figure 49 Test Condition of Release Delay Time**

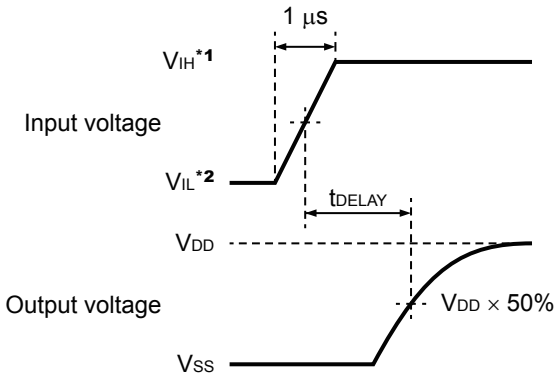
**Figure 50 Test Circuit of Release Delay Time**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## 6. Release delay time ($t_{DELAY}$) vs. Power supply voltage ($V_{DD}$)

### 6. 1 SENSE detection product




***1.** $V_{IH} = +V_{DET} + 1.0$ V
***2.** $V_{IL} = +V_{DET} - 1.0$ V

**Figure 51 Test Condition of Release Delay Time**

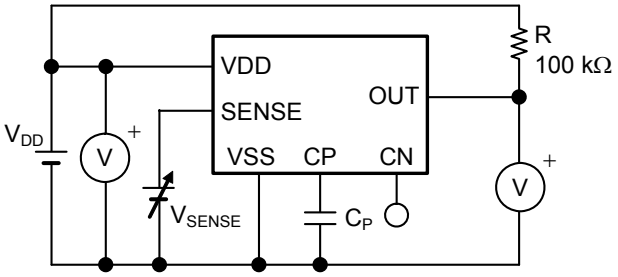



**Figure 52 Test Circuit of Release Delay Time**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Application Circuit Examples

### 1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.
Using the S-1011 Series which has the low minimum operation voltage, the high-accuracy detection voltage and the hysteresis width, reset circuits can be easily constructed as seen in **Figure 53** and **Figure 54**.

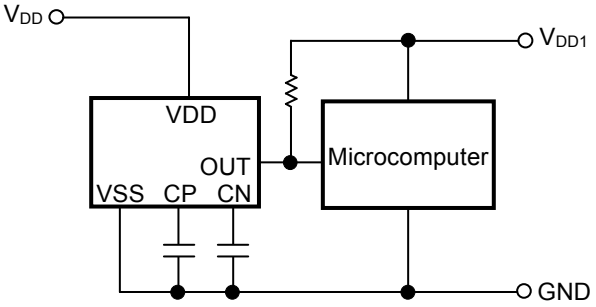



**Figure 53 Example of Reset Circuit (VDD detection product)**

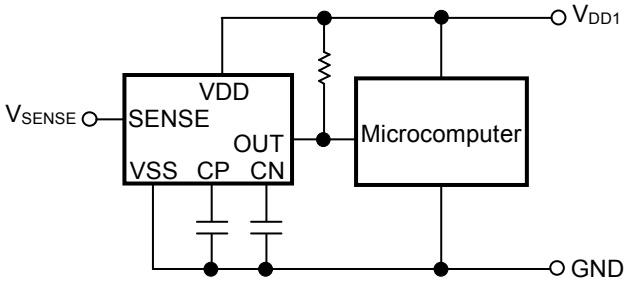



**Figure 54 Example of Reset Circuit (SENSE detection product)**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Thermal Characteristics

### 1. SOT-23-6

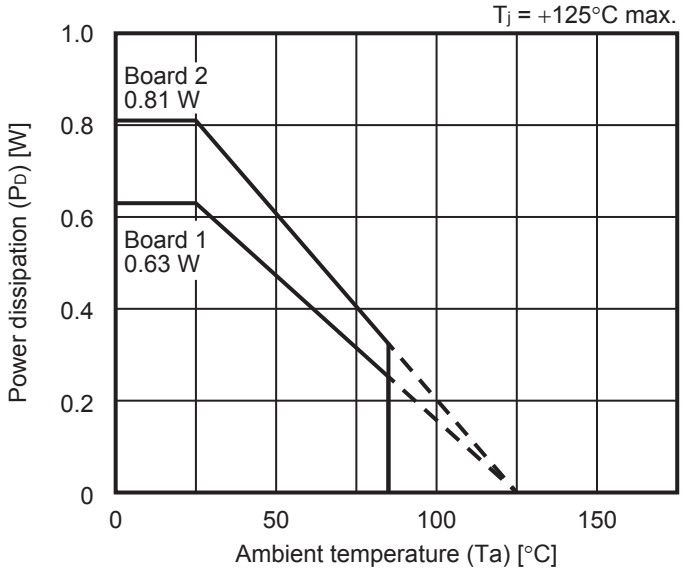



**Figure 55 Power Dissipation of Package (When Mounted on Board)**

#### 1. 1 Board 1*1

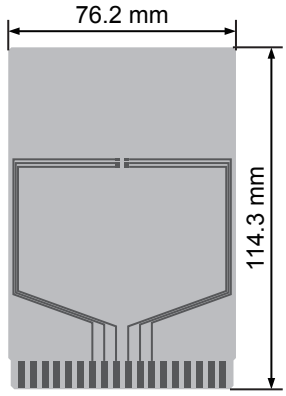



**Figure 56**

**Table 21**

| Item | | Specification |
|---|---|---|
| Thermal resistance value ($\theta_{ja}$) | | 159°C/W |
| Size | | 114.3 mm × 76.2 mm × t1.6 mm |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer | 1 | Land pattern and wiring for testing: t0.070 mm |
| | 2 | – |
| | 3 | – |
| | 4 | 74.2 mm × 74.2 mm × t0.070 mm |
| Thermal via | | – |

#### 1. 2 Board 2*1

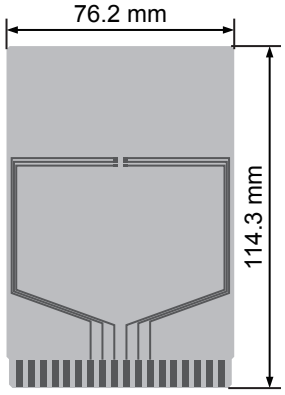
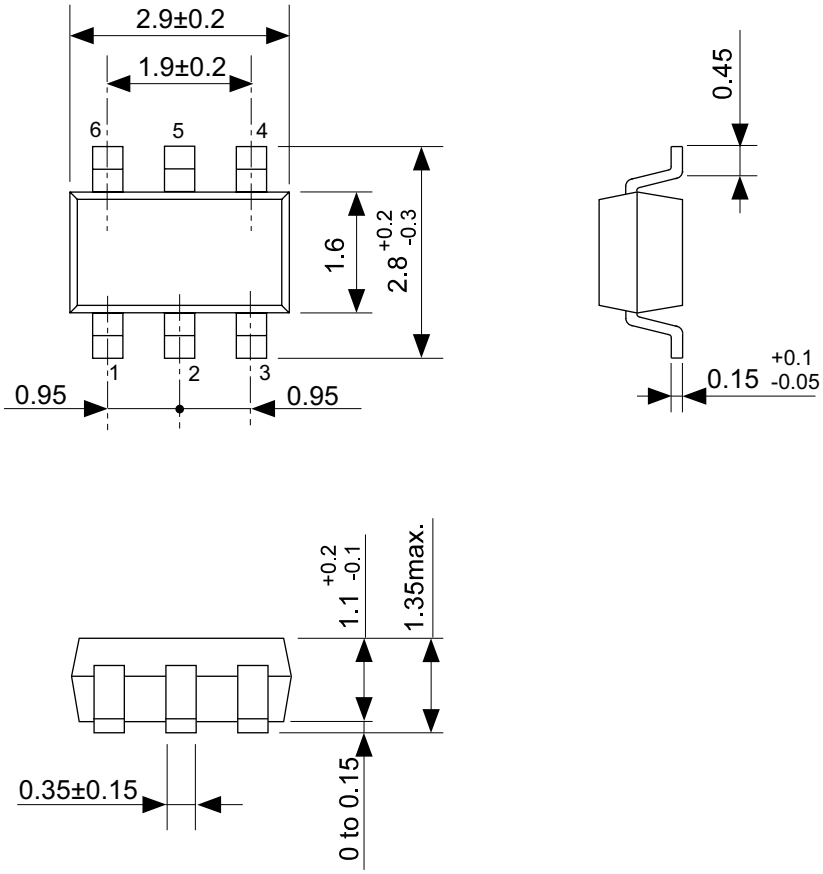



**Figure 57**

**Table 22**

| Item | | Specification |
|---|---|---|
| Thermal resistance value ($\theta_{ja}$) | | 124°C/W |
| Size | | 114.3 mm × 76.2 mm × t1.6 mm |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer | 1 | Land pattern and wiring for testing: t0.070 mm |
| | 2 | 74.2 mm × 74.2 mm × t0.035 mm |
| | 3 | 74.2 mm × 74.2 mm × t0.035 mm |
| | 4 | 74.2 mm × 74.2 mm × t0.070 mm |
| Thermal via | | – |

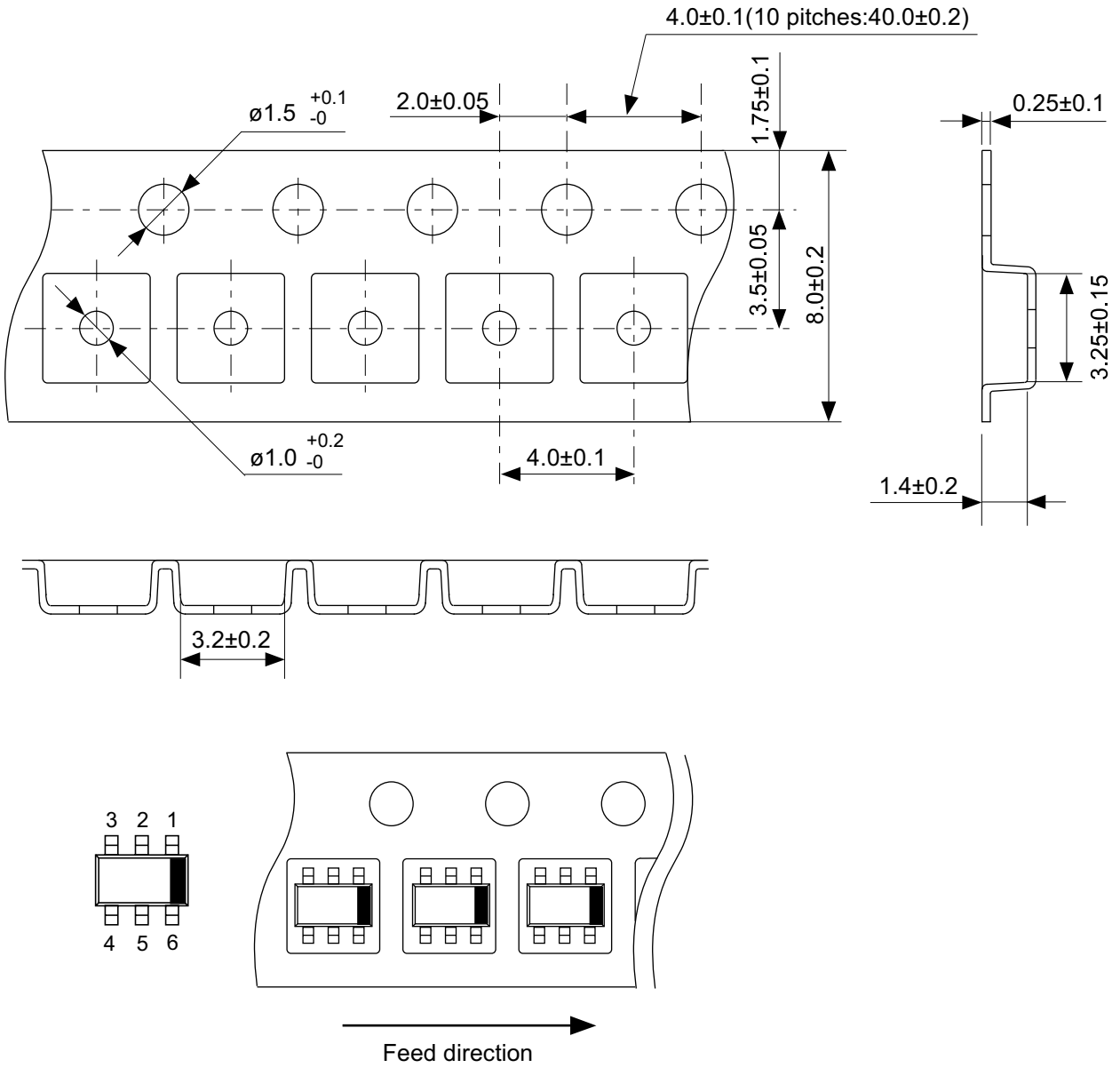
***1.** The board is same in SOT-23-3, SOT-23-5 and SOT-23-6.




No. MP006-A-P-SD-2.1

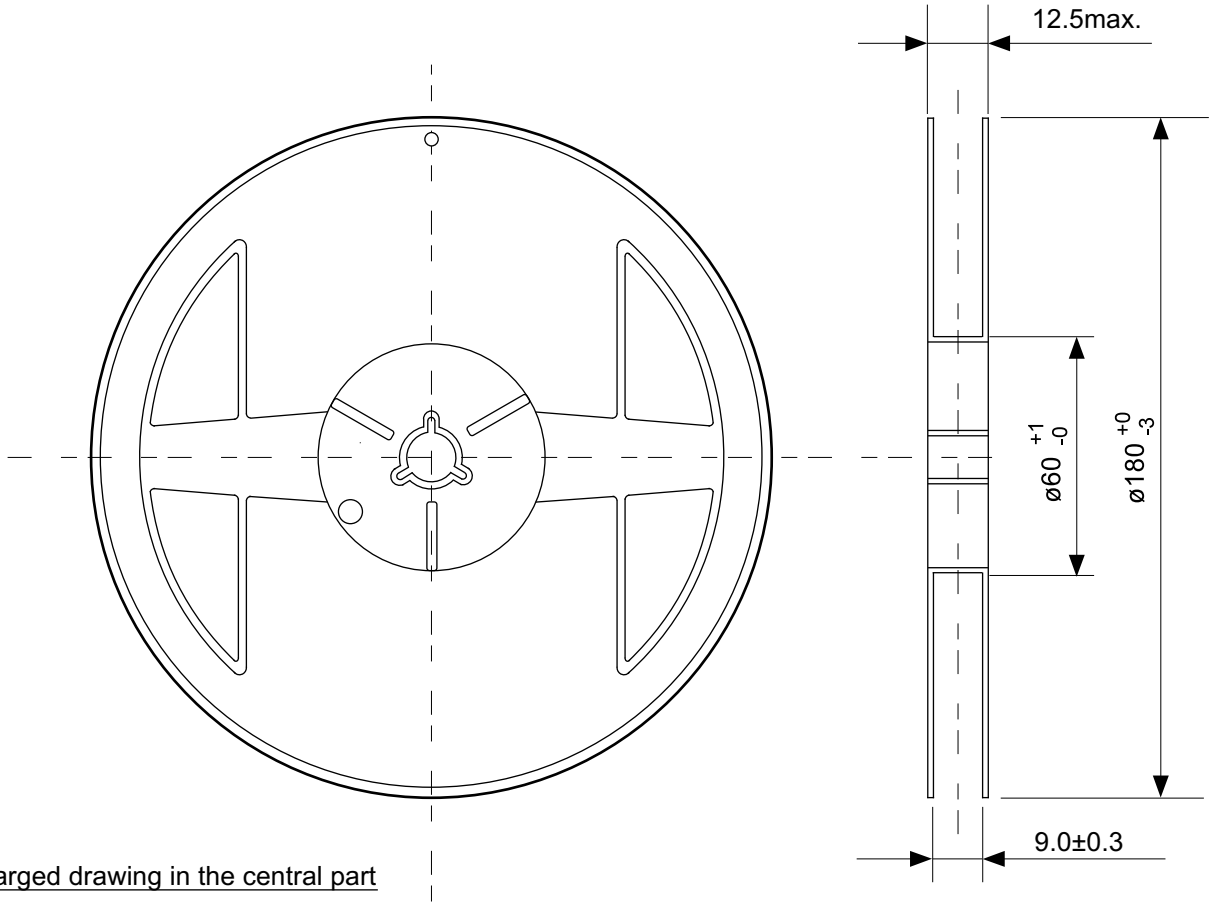
| | |
|---|---|
| TITLE | SOT236-A-PKG Dimensions |
| No. | MP006-A-P-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**

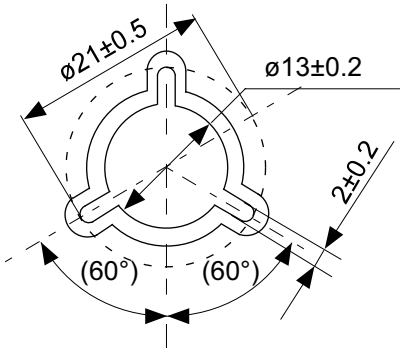



No. MP006-A-C-SD-3.1

| | |
|---|---|
| TITLE | SOT236-A-Carrier Tape |
| No. | MP006-A-C-SD-3.1 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |




Enlarged drawing in the central part




No. MP006-A-R-SD-2.1

| | | | |
|---|---|---|---|
| TITLE | SOT236-A-Reel | | |
| No. | MP006-A-R-SD-2.1 | | |
| ANGLE | | QTY | 3,000 |
| UNIT | mm | | |
| | | | |
| **ABLIC Inc.** | | | |

## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ABLIC:

S-1011C5H-M6T1U4 S-1011L36-M6T1U4 S-1011M36-M6T1U4 S-1011A90-M6T1U4 S-1011A50-M6T1U4 S-1011EAD-M6T1U4 S-1011E60-M6T1U4 S-1011C70-M6T1U4 S-1011C90-M6T1U4 S-1011C50-M6T1U4 S-1011Q30-M6T1U4 S-1011G50-M6T1U4 S-1011E80-M6T1U4 S-1011EA0-M6T1U4 S-1011B76-M6T1U4 S-1011AAB-M6T1U4 S-1011A70-M6T1U4 S-1011G70-M6T1U4 S-1011J36-M6T1U4 S-1011A5H-M6T1U4 S-1011C5B-M6T1U4 S-1011G90-M6T1U4 S-1011A60-M6T1U4 S-1011A80-M6T1U4 S-1011C60-M6T1U4 S-1011CA0-M6T1U4 S-1011E50-M6T1U4 S-1011E90-M6T1U4 S-1011GA0-M6T1U4 S-1011N33-M6T1U4 S-1011A52-M6T1U4 S-1011C80-M6T1U4 S-1011EAC-M6T1U4 S-1011E70-M6T1U4 S-1011L42-M6T1U4 S-1011J4B-M6T1U4 S-1011F76-M6T1U4 S-1011AA0-M6T1U4 S-1011B80-M6T1U4 S-1011C5E-M6T1U4 S-1011G60-M6T1U4 S-1011G80-M6T1U4 S-1011AAC-M6T1U4 S-1011J47-M6T1U4

LifeElectronics
Живое партнерство

**ООО «ЛайфЭлектроникс»** **“LifeElectronics” LLC**

*ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703*

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

*Мы предлагаем:*

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

*В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.*

*Конструкторский отдел помогает осуществить:*

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

*Тел: +7 (812) 336 43 04 (многоканальный)*
*Email: org@lifeelectronics.ru*

***www.lifeelectronics.ru***