# 512K x36 and 1024K x18 18Mb, PIPELINE 'NO WAIT' STATE BUS SYNCHRONOUS SRAM

**MAY 2015**

## FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- /CKE pin to enable clock and suspend operation
- JEDEC 100-pin QFP, 165-ball BGA and 119-ball BGA packages
- Power supply:
  NLP: $V_{DD}$ 3.3V (± 5%), $V_{DDQ}$ 3.3V/2.5V (± 5%)
  NVP: $V_{DD}$ 2.5V (± 5%), $V_{DDQ}$ 2.5V (± 5%)
  NVVP: $V_{DD}$ 1.8V (± 5%), $V_{DDQ}$ 1.8V (± 5%)
- JTAG Boundary Scan for BGA packages
- Commercial, Industrial and Automotive (x36) temperature support
- Lead-free available
- For leaded option, please contact ISSI.

## DESCRIPTION

The 18Meg product family features high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 512K words by 36 bits and 1024K words by 18 bits, fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, /CKE is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when /WE is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

## FAST ACCESS TIME

| Symbol | Parameter | -250 | -200 | Units |
|---|---|---|---|---|
| tKQ | Clock Access Time | 2.6 | 3.0 | ns |
| tKC | Cycle time | 4 | 5 | ns |
| | Frequency | 250 | 200 | MHz |

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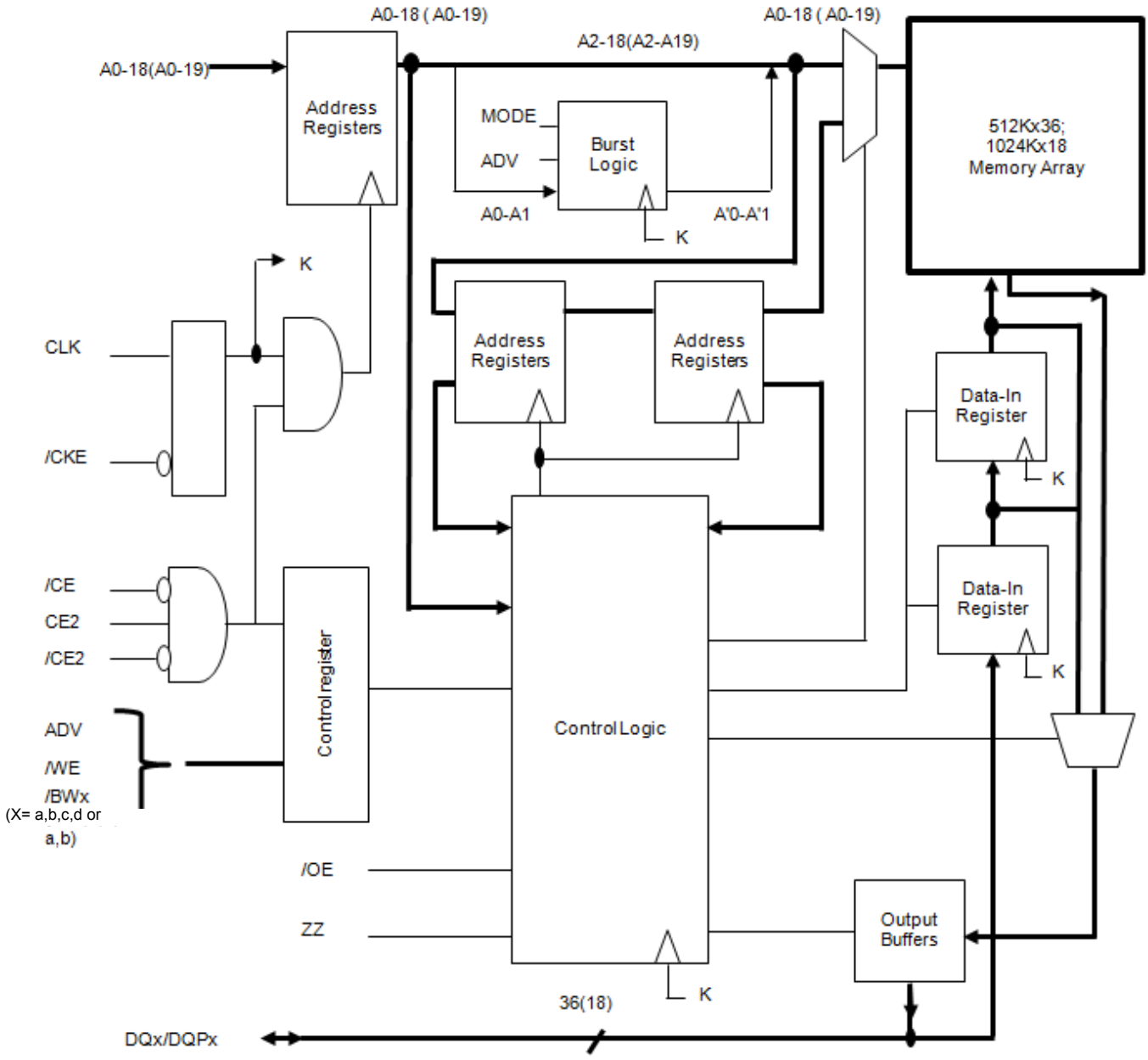
a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

## BLOCK DIAGRAM

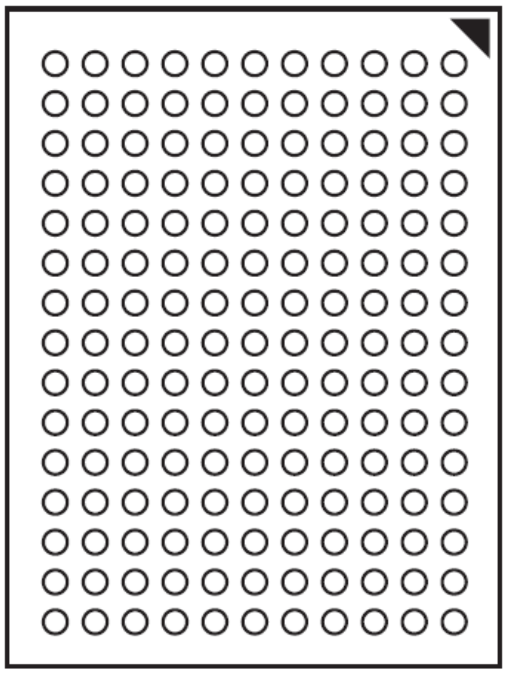


## PIN CONFIGURATION

### 512K x 36, 165-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | A | /CE | /BWc | /BWb | /CE2 | /CKE | ADV | A | A | NC |
| B | NC | A | CE2 | /BWd | /BWa | CLK | /WE | /OE | A | A | NC |
| C | DQPc | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | DQPb |
| D | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| E | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| F | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| G | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| H | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| J | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| K | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| L | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| M | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| N | DQPd | NC | $V_{DDQ}$ | $V_{SS}$ | NC | NC | NC | $V_{SS}$ | $V_{DDQ}$ | NC | DQPa |
| P | NC | NC | A | A | TDI | A1* | TDO | A | A | A | NC |
| R | MODE | NC | A | A | TMS | A0* | TCK | A | A | A | A |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA

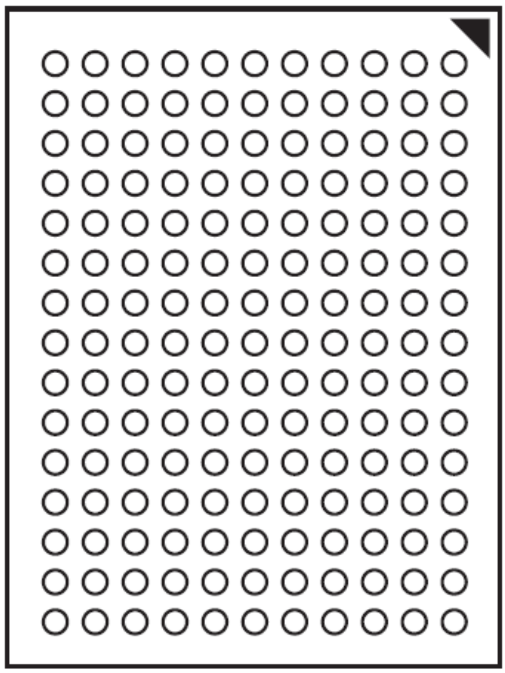
### PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| CLK | Synchronous Clock |
| /CKE | Clock Enable |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| ADV | Synchronous Burst Address Advance/Load |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /WE | Synchronous Read/Write Control Input |
| /BWx (x=a-d) | Synchronous Byte Write Inputs |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| DQPx | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| $V_{SS}$ | Ground |

### 512K x 32, 165-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | A | /CE | /BWc | /BWb | /CE2 | /CKE | ADV | A | A | NC |
| B | NC | A | CE2 | /BWd | /BWa | CLK | /WE | /OE | A | A | NC |
| C | NC | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC |
| D | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| E | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| F | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| G | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| H | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| J | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| K | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| L | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| M | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| N | NC | NC | $V_{DDQ}$ | $V_{SS}$ | NC | NC | NC | $V_{SS}$ | $V_{DDQ}$ | NC | NC |
| P | NC | NC | A | A | TDI | A1* | TDO | A | A | A | NC |
| R | MODE | NC | A | A | TMS | A0* | TCK | A | A | A | A |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA

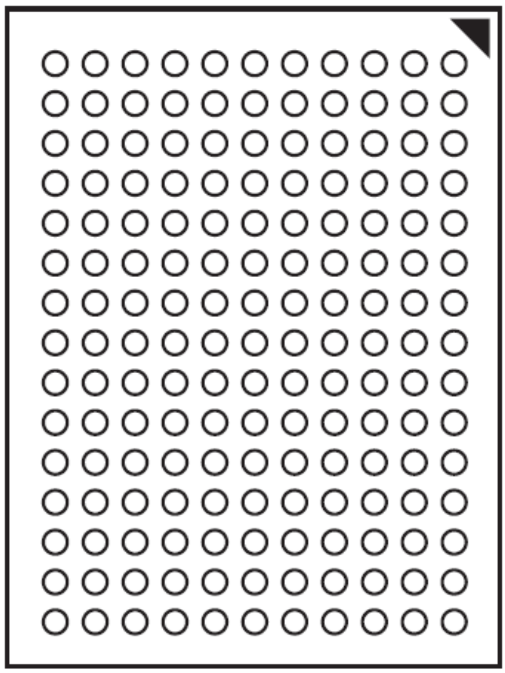
### PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| CLK | Synchronous Clock |
| /CKE | Clock Enable |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| ADV | Synchronous Burst Address Advance/Load |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /WE | Synchronous Read/Write Control Input |
| /BWx (x=a-d) | Synchronous Byte Write Inputs |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| $V_{SS}$ | Ground |

### 1024K x 18, 165-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | A | /CE | /BWb | NC | /CE2 | /CKE | ADV | A | A | A |
| B | NC | A | CE2 | NC | /BWa | CLK | /WE | /OE | A | A | NC |
| C | NC | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | DQPa |
| D | NC | DQb | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQa |
| E | NC | DQb | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQa |
| F | NC | DQb | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQa |
| G | NC | DQb | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQa |
| H | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| J | DQb | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | NC |
| K | DQb | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | NC |
| L | DQb | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | NC |
| M | DQb | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | NC |
| N | DQPb | NC | $V_{DDQ}$ | $V_{SS}$ | NC | NC | NC | $V_{SS}$ | $V_{DDQ}$ | NC | NC |
| P | NC | NC | A | A | TDI | A1* | TDO | A | A | A | NC |
| R | MODE | NC | A | A | TMS | A0* | TCK | A | A | A | A |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA

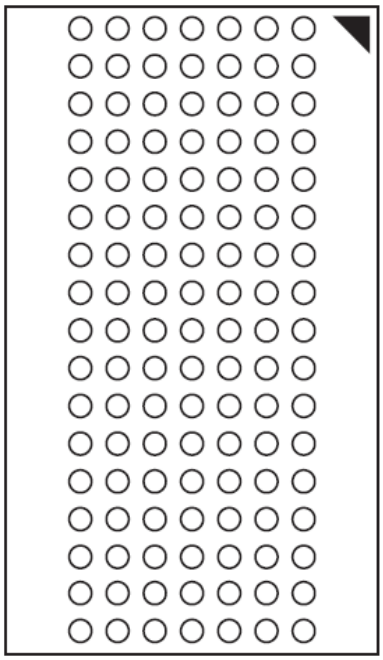
### PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| CLK | Synchronous Clock |
| /CKE | Clock Enable |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| ADV | Synchronous Burst Address Advance/Load |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /WE | Synchronous Read/Write Control Input |
| /BWx (x=a-b) | Synchronous Byte Write Inputs |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| DQPx | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| $V_{SS}$ | Ground |

### 512K x 36, 119-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | A | A | A | A | A | $V_{DDQ}$ |
| B | NC | CE2 | A | ADV | A | /CE2 | NC |
| C | NC | A | A | $V_{DD}$ | A | A | NC |
| D | DQc | DQPc | $V_{SS}$ | NC | $V_{SS}$ | DQPb | DQb |
| E | DQc | DQc | $V_{SS}$ | /CE | $V_{SS}$ | DQb | DQb |
| F | $V_{DDQ}$ | DQc | $V_{SS}$ | /OE | $V_{SS}$ | DQb | $V_{DDQ}$ |
| G | DQc | DQc | /BWc | A | /BWb | DQb | DQb |
| H | DQc | DQc | $V_{SS}$ | /WE | $V_{SS}$ | DQb | DQb |
| J | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| K | DQd | DQd | $V_{SS}$ | CLK | $V_{SS}$ | DQa | DQa |
| L | DQd | DQd | /BWd | NC | /BWa | DQa | DQa |
| M | $V_{DDQ}$ | DQd | $V_{SS}$ | /CKE | $V_{SS}$ | DQa | $V_{DDQ}$ |
| N | DQd | DQd | $V_{SS}$ | A1* | $V_{SS}$ | DQa | DQa |
| P | DQd | DQPd | $V_{SS}$ | A0* | $V_{SS}$ | DQPa | DQa |
| R | NC | A | MODE | $V_{DD}$ | NC | A | NC |
| T | NC | NC | A | A | A | NC | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA

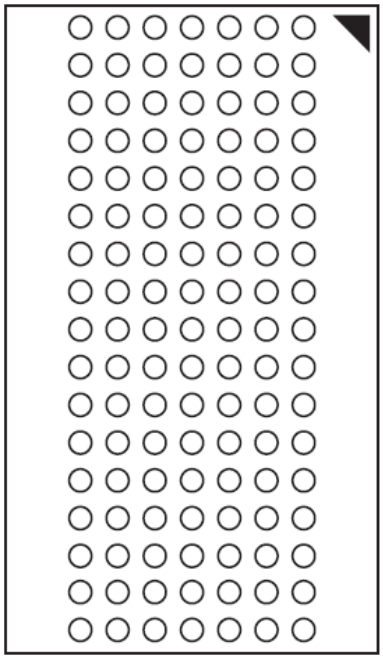
### PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| CLK | Synchronous Clock |
| /CKE | Clock Enable |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| ADV | Synchronous Burst Address Advance/Load |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /WE | Synchronous Read/Write Control Input |
| /BWx (x=a-d) | Synchronous Byte Write Inputs |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| DQPx | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| $V_{SS}$ | Ground |

### 512K x 32, 119-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | A | A | A | A | A | $V_{DDQ}$ |
| B | NC | CE2 | A | ADV | A | /CE2 | NC |
| C | NC | A | A | $V_{DD}$ | A | A | NC |
| D | DQc | NC | $V_{SS}$ | NC | $V_{SS}$ | NC | DQb |
| E | DQc | DQc | $V_{SS}$ | /CE | $V_{SS}$ | DQb | DQb |
| F | $V_{DDQ}$ | DQc | $V_{SS}$ | /OE | $V_{SS}$ | DQb | $V_{DDQ}$ |
| G | DQc | DQc | /BWc | A | /BWb | DQb | DQb |
| H | DQc | DQc | $V_{SS}$ | /WE | $V_{SS}$ | DQb | DQb |
| J | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| K | DQd | DQd | $V_{SS}$ | CLK | $V_{SS}$ | DQa | DQa |
| L | DQd | DQd | /BWd | NC | /BWa | DQa | DQa |
| M | $V_{DDQ}$ | DQd | $V_{SS}$ | /CKE | $V_{SS}$ | DQa | $V_{DDQ}$ |
| N | DQd | DQd | $V_{SS}$ | A1* | $V_{SS}$ | DQa | DQa |
| P | DQd | NC | $V_{SS}$ | A0* | $V_{SS}$ | NC | DQa |
| R | NC | A | MODE | $V_{DD}$ | NC | A | NC |
| T | NC | NC | A | A | A | NC | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA

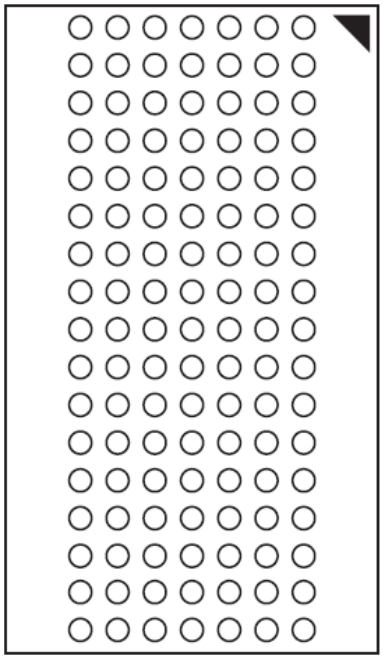
### PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| CLK | Synchronous Clock |
| /CKE | Clock Enable |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| ADV | Synchronous Burst Address Advance/Load |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /WE | Synchronous Read/Write Control Input |
| /BWx (x=a-d) | Synchronous Byte Write Inputs |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| $V_{SS}$ | Ground |

### 1024K x 18, 119-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | A | A | A | A | A | $V_{DDQ}$ |
| B | NC | CE2 | A | ADV | A | /CE2 | NC |
| C | NC | A | A | $V_{DD}$ | A | A | NC |
| D | DQb | NC | $V_{SS}$ | NC | $V_{SS}$ | DQPa | NC |
| E | NC | DQb | $V_{SS}$ | /CE | $V_{SS}$ | NC | DQa |
| F | $V_{DDQ}$ | NC | $V_{SS}$ | /OE | $V_{SS}$ | DQa | $V_{DDQ}$ |
| G | NC | DQb | /BWb | A | NC | NC | DQa |
| H | DQb | NC | VSS | /WE | $V_{SS}$ | DQa | NC |
| J | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| K | NC | DQb | VSS | CLK | $V_{SS}$ | NC | DQa |
| L | DQb | NC | NC | NC | /BWa | DQa | NC |
| M | $V_{DDQ}$ | DQb | $V_{SS}$ | /CKE | $V_{SS}$ | NC | $V_{DDQ}$ |
| N | DQb | NC | $V_{SS}$ | A1* | $V_{SS}$ | DQa | NC |
| P | NC | DQPb | $V_{SS}$ | A0* | $V_{SS}$ | NC | DQa |
| R | NC | A | MODE | $V_{DD}$ | NC | A | NC |
| T | NC | A | A | NC | A | A | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

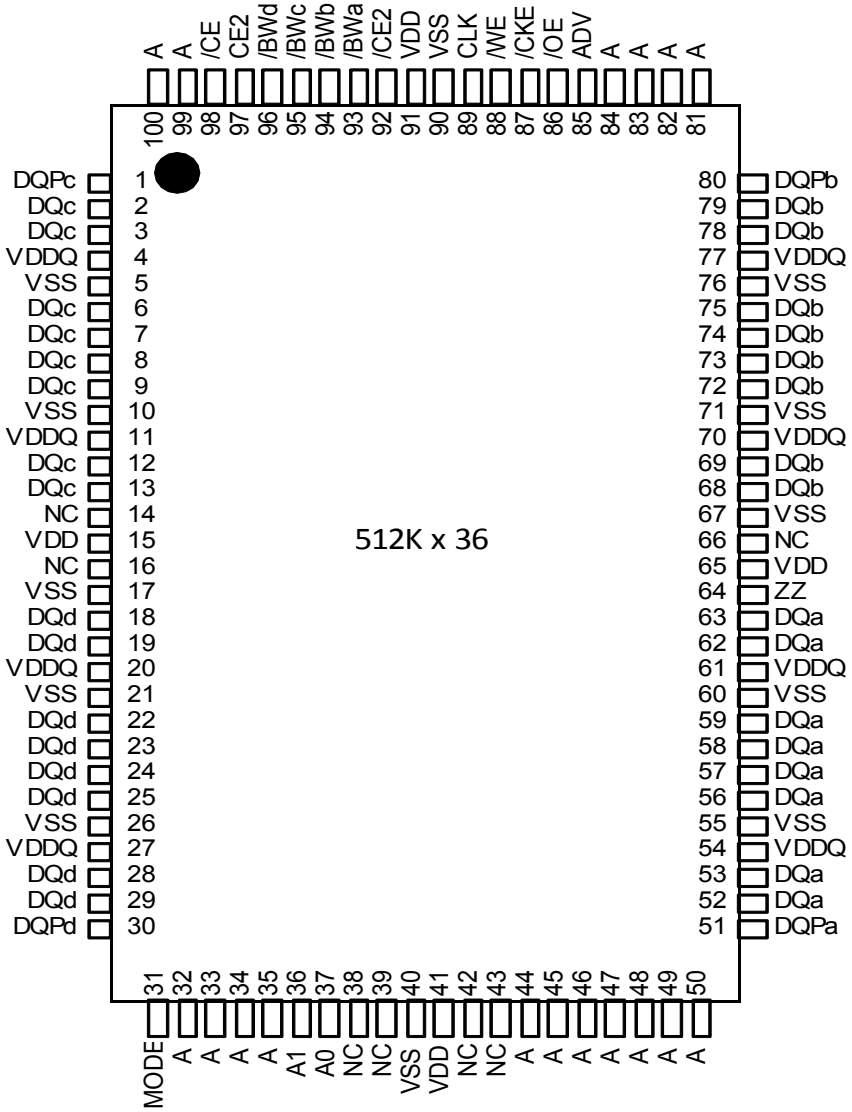


Bottom View
119-Ball, 14 mm x 22 mm BGA

### PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| CLK | Synchronous Clock |
| /CKE | Clock Enable |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| ADV | Synchronous Burst Address Advance/Load |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /WE | Synchronous Read/Write Control Input |
| /BWx (x=a-b) | Synchronous Byte Write Inputs |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| DQPx | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| $V_{SS}$ | Ground |

**512K x 36, 100PIN QFP (Top View)**

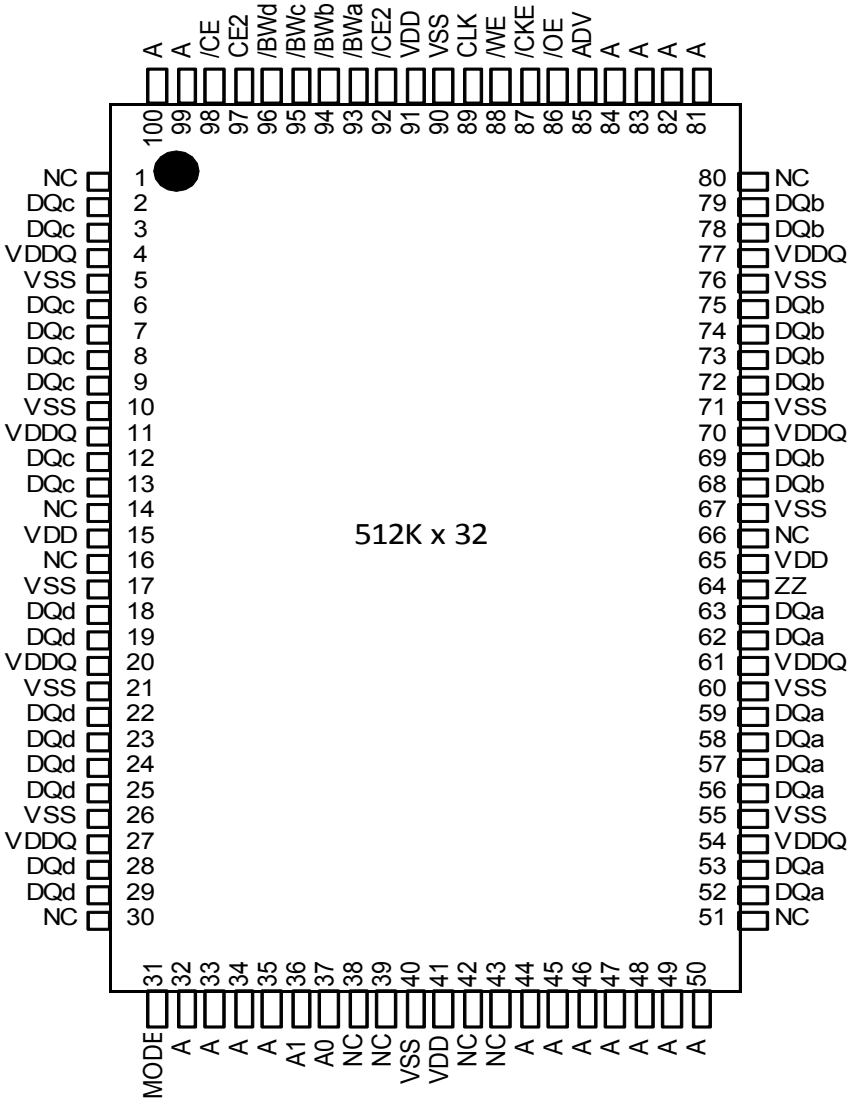



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

## PIN DESCRIPTIONS

| Symbol | Pin Name | Symbol | Pin Name |
|---|---|---|---|
| A | Address Inputs | ZZ | Power Sleep Mode |
| A0,A1 | Synchronous Burst Address Inputs | MODE | Burst Sequence Selection |
| ADV | Synchronous Burst Address Advance/Load | $V_{DD}$ | Power Supply |
| /WE | Synchronous Read/Write Control Input | NC | No Connect |
| CLK | Synchronous Clock | DQx | Data Inputs/Outputs |
| /CKE | Clock Enable | DQPx | Parity Data I/O; NC for x32 option |
| /CE,CE2,/CE2 | Synchronous Chip Enable | $V_{DDQ}$ | I/O Power Supply |
| /BWx (x=a-d) | Synchronous Byte Write Inputs | $V_{SS}$ | Ground |
| /OE | Output Enable | | |

**512K x 32, 100PIN QFP (Top View)**

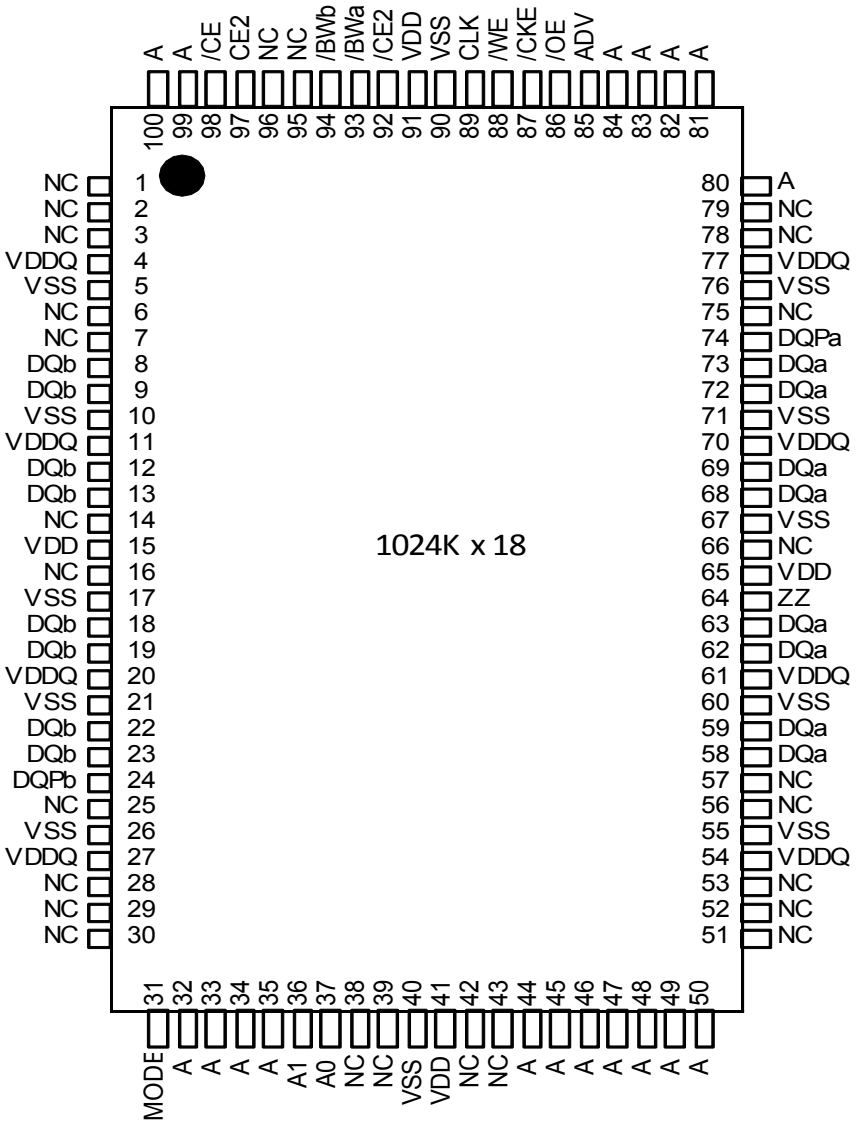



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

## PIN DESCRIPTIONS

| Symbol | Pin Name | Symbol | Pin Name |
|---|---|---|---|
| A | Address Inputs | ZZ | Power Sleep Mode |
| A0,A1 | Synchronous Burst Address Inputs | MODE | Burst Sequence Selection |
| ADV | Synchronous Burst Address Advance/Load | $V_{DD}$ | Power Supply |
| /WE | Synchronous Read/Write Control Input | NC | No Connect |
| CLK | Synchronous Clock | DQx | Data Inputs/Outputs |
| /CKE | Clock Enable | DQPx | Parity Data I/O; NC for x32 option |
| /CE,CE2,/CE2 | Synchronous Chip Enable | $V_{DDQ}$ | I/O Power Supply |
| /BWx (x=a-d) | Synchronous Byte Write Inputs | $V_{SS}$ | Ground |
| /OE | Output Enable | | |

**1024K x 18, 100PIN QFP (Top View)**

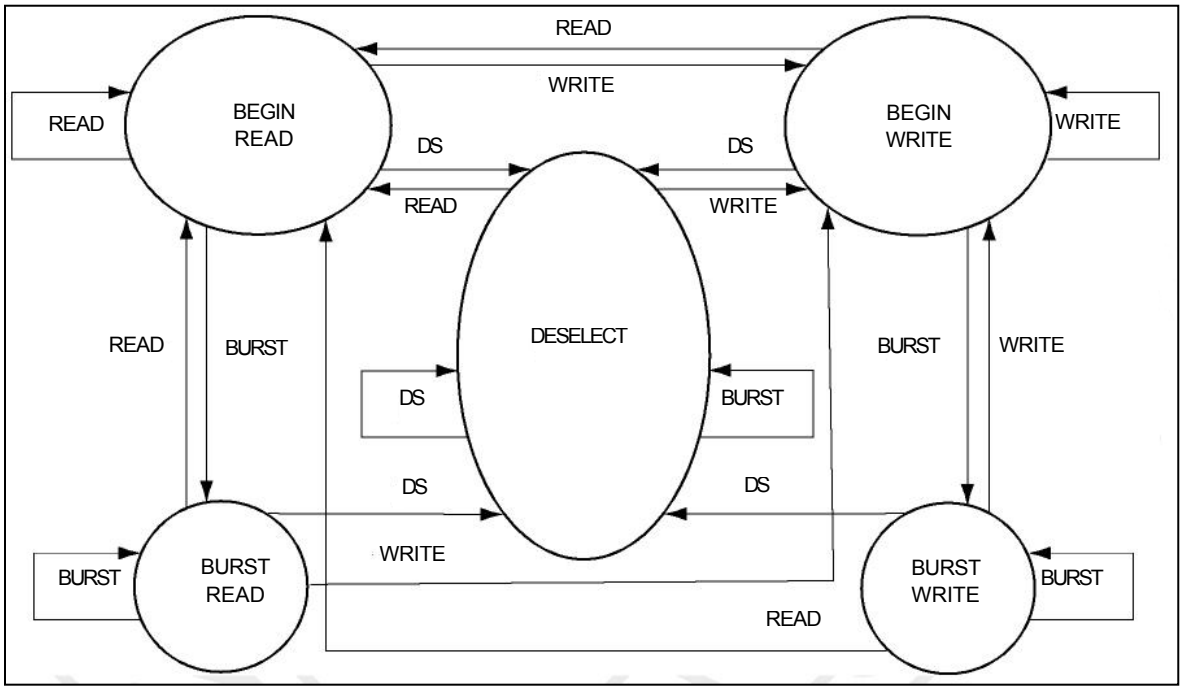



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

## PIN DESCRIPTIONS

| Symbol | Pin Name | Symbol | Pin Name |
|---|---|---|---|
| A | Address Inputs | ZZ | Power Sleep Mode |
| A0,A1 | Synchronous Burst Address Inputs | MODE | Burst Sequence Selection |
| ADV | Synchronous Burst Address Advance/Load | $V_{DD}$ | Power Supply |
| /WE | Synchronous Read/Write Control Input | NC | No Connect |
| CLK | Synchronous Clock | DQx | Data Inputs/Outputs |
| /CKE | Clock Enable | DQPx | Parity Data I/O |
| /CE,CE2,/CE2 | Synchronous Chip Enable | $V_{DDQ}$ | I/O Power Supply |
| /BWx (x=a-b) | Synchronous Byte Write Inputs | $V_{SS}$ | Ground |
| /OE | Output Enable | | |

## STATE DIAGRAM




## TRUTH TABLE

### SYNCHRONOUS TRUTH TABLE

| Operation | Address Used | /CE | CE2 | /CE2 | ADV | /WE | /BWx | /OE | /CKE | CLK |
|---|---|---|---|---|---|---|---|---|---|---|
| Not Selected | N/A | H | X | X | L | X | X | X | L | ↑ |
| Not Selected | N/A | X | L | X | L | X | X | X | L | ↑ |
| Not Selected | N/A | X | X | H | L | X | X | X | L | ↑ |
| Not Selected Continue | N/A | X | X | X | H | X | X | X | L | ↑ |
| Begin Burst Read | External Address | L | H | L | L | H | X | L | L | ↑ |
| Continue Burst Read | Next Address | X | X | X | H | X | X | L | L | ↑ |
| NOP/Dummy Read | External Address | L | H | L | L | H | X | H | L | ↑ |
| Dummy Read | Next Address | X | X | X | H | X | X | H | L | ↑ |
| Begin Burst Write | External Address | L | H | L | L | L | L | X | L | ↑ |
| Continue Burst Write | Next Address | X | X | X | H | X | L | X | L | ↑ |
| NOP/Write Abort | N/A | L | H | L | L | L | H | X | L | ↑ |
| Write Abort | Next Address | X | X | X | H | X | H | X | L | ↑ |
| Ignore Clock | Current Address | X | X | X | X | X | X | X | H | ↑ |

Notes:
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. /WE = L means Write operation in Write Truth Table.
5. /WE = H means Read operation in Write Truth Table.
6. Operation finally depends on status of asynchronous pins (ZZ and /OE).

## ASYNCHRONOUS TRUTH TABLE

| Operation | ZZ | /OE | I/O STATUS |
|---|---|---|---|
| Sleep Mode | H | X | High-Z |
| Read | L | L | DQ |
| | L | H | High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

Notes:
1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with /OE, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

## WRITE TRUTH TABLE (x18)

| Operation | /WE | /BWa | /BWb |
|---|---|---|---|
| READ | H | X | X |
| WRITE BYTE a | L | L | H |
| WRITE BYTE b | L | H | L |
| WRITE ALL BYTEs | L | L | L |
| WRITE ABORT/NOP | L | H | H |

Notes:
1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

## WRITE TRUTH TABLE (x36)

| Operation | /WE | /BWa | /BWb | /BWc | /BWd |
|---|---|---|---|---|---|
| READ | H | X | X | X | X |
| WRITE BYTE a | L | L | H | H | H |
| WRITE BYTE b | L | H | L | H | H |
| WRITE BYTE c | L | H | H | L | H |
| WRITE BYTE d | L | H | H | H | L |
| WRITE ALL BYTEs | L | L | L | L | L |
| WRITE ABORT/NOP | L | H | H | H | H |

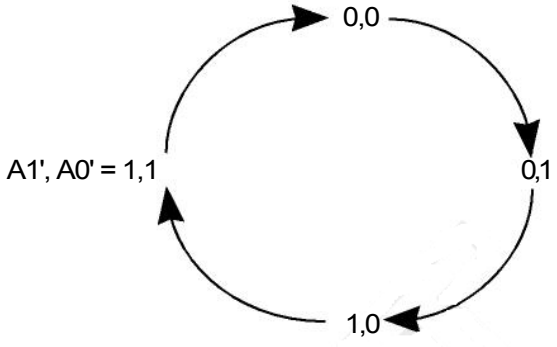
Notes:
1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

## ADDRESS SEQUENCE IN BURST MODE

### INTERLEAVED BURST ADDRESS TABLE (MODE = $V_{DD}$ or NC)

| External Address | 1st Burst Address | 2nd Burst Address | 3rd Burst Address |
|---|---|---|---|
| A1 A0 | A1 A0 | A1 A0 | A1 A0 |
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

### LINEAR BURST ADDRESS TABLE (MODE = $V_{SS}$)




## Power Up Sequence

$V_{DDQ} \rightarrow V_{DDQ}$[1] $\rightarrow$ I/O Pins[2]

Notes:
1. $V_{DD}$ can be applied at the same time as $V_{DDQ}$
2. Applying I/O inputs is recommended after $V_{DDQ}$ is stable. The inputs of the I/O pins can be applied at the same time as $V_{DDQ}$ as long as Vih (level of I/O pins) is lower than $V_{DDQ}$.

# ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | NLP Value | NVP/NVVP Value | Unit |
|---|---|---|---|---|
| Tstg | Storage Temperature | –65 to +150 | –65 to +150 | °C |
| Pd | Power Dissipation | 1.6 | 1.6 | W |
| Iout | Output Current (per I/O) | 20 | 20 | mA |
| Vin, Vout | Voltage Relative to Vss for I/O Pins | –0.5 to $V_{DDQ}$ +0.3 | –0.5 to $V_{DDQ}$ + 0.3 | V |
| Vin | Voltage Relative to Vss for Address and Control Inputs | –0.3 to $V_{DD}$ +0.5 | –0.3 to $V_{DD}$ + 0.3 | V |

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

## OPERATING RANGE (IS61NLPx)

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Automotive | -40°C to +125°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |

## OPERATING RANGE (IS61NVPx)

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 2.5V ± 5% | 2.5V ± 5% |
| Industrial | -40°C to +85°C | 2.5V ± 5% | 2.5V ± 5% |
| Automotive | *Please contact ISSI | | |

## OPERATING RANGE (IS61NVVPx)

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 1.8V ± 5% | 1.8V ± 5% |
| Industrial | -40°C to +85°C | 1.8V ± 5% | 1.8V ± 5% |
| Automotive | *Please contact ISSI | | |

# CHARACTERISTICS

## DC ELECTRICAL CHARACTERISTICS (Over operating temperature range)

| Symbol | Parameter | Test Conditions | 3.3V | | 2.5V | | 1.8V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Voh | Output HIGH Voltage | Ioh=-4.0 mA(3.3V)<br>Ioh=–1.0 mA(2.5V,1.8V) | 2.4 | — | 2.0 | — | $V_{DDQ}$ -0.4 | — | V |
| Vol | Output LOW Voltage | Iol=8.0 mA(3.3V)<br>Iol=1.0 mA(2.5V,1.8V) | — | 0.4 | — | 0.4 | — | 0.4 | V |
| Vih | Input HIGH Voltage | | 2.0 | $V_{DD}$ +0.3 | 1.7 | $V_{DD}$ +0.3 | 0.7* $V_{DD}$ | $V_{DD}$ +0.3 | V |
| Vil | Input LOW Voltage | | –0.3 | 0.8 | –0.3 | 0.7 | –0.3 | 0.3* $V_{DD}$ | V |
| Ili | Input Leakage Current | Vss≤Vin≤ $V_{DD}$ | –1 | 1 | –1 | 1 | –1 | 1 | µA |
| Ilo | Output Leakage Current | Vss≤Vout≤ $V_{DDQ}$,/OE=Vih | –1 | 1 | –1 | 1 | –1 | 1 | µA |

Notes:
1. All voltages referenced to ground.
2. Overshoot:
   3.3V and 2.5V: Vih (AC) ≤ $V_{DD}$ + 1.5V (Pulse width less than tkc /2)
   1.8V: Vih (AC) ≤ $V_{DD}$ + 0.5V (Pulse width less than tkc /2)
3. Undershoot:
   3.3V and 2.5V: Vil (AC) ≥ -1.5V (Pulse width less than tkc /2)
   1.8V: Vil (AC) ≥ -0.5V (Pulse width less than tkc /2)
4. MODE pin has an internal pull-up and should be tied to $V_{DD}$ or Vss . It exhibits ±100µA maximum leakage current when tied to ≤Vss+0.2V or ≥ $V_{DD}$–0.2V.
5. ZZ pin has an internal pull-down and should be tied to $V_{DD}$ or Vss . It exhibits ±100µA maximum leakage current when tied to ≤Vss+0.2V or ≥ $V_{DD}$–0.2V.

## POWER SUPPLY CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Temp. range | -250 | | -200 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Max | | Max | | |
| | | | | x18 | x36 | x18 | x36 | |
| Icc | AC Operating, Supply Current | Device Selected, OE = Vih, ZZ ≤ Vil,All Inputs ≤ 0.2V or ≥ $V_{DD}$ – 0.2V,Cycle Time ≥ tkc min. | Com. | 270 | 270 | 220 | 220 | mA |
| | | | Ind. | 290 | 290 | 240 | 240 | |
| Isb | Standby Current TTL Input | Device Deselected, $V_{DD}$ = Max.,All Inputs ≤ Vil or ≥ Vih,ZZ ≤ Vil, f = Max. | Com. | 80 | 80 | 70 | 70 | mA |
| | | | Ind. | 90 | 90 | 80 | 80 | |
| Isb1 | Standby Current CMOS Input | Device Deselected, $V_{DD}$ = Max.,Vin ≤ Vss + 0.2V or ≥ $V_{DD}$ – 0.2V,f = 0 | Com. | 60 | 60 | 60 | 60 | mA |
| | | | Ind. | 70 | 70 | 70 | 70 | |

Note:
1. Power-up assumes a linear ramp from 0V to $V_{DD}$ (min) within 200ms. During this time Vih < $V_{DD}$ and $V_{DDQ}$ < $V_{DD}$

## CAPACITANCE

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| Cin | Input Capacitance | Vin = 0V | 6 | pF |
| Cout | Input/Output Capacitance | Vout = 0V | 8 | pF |

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: Ta = 25°C, f = 1 MHz, $V_{DD}$ = 3.3V.

## READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | -250 | | -200 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| fmax | Clock Frequency | — | 250 | — | 200 | MHz |
| tkc | Cycle Time | 4 | — | 5 | — | ns |
| tkh | Clock High Time | 1.7 | — | 2 | — | ns |
| tkl | Clock Low Time | 1.7 | — | 2 | — | ns |
| tkq | Clock Access Time | — | 2.6 | — | 3.0 | ns |
| tkqx(2) | Clock High to Output Invalid | 0.8 | — | 1.5 | — | ns |
| tkqlz(2,3) | Clock High to Output Low-Z | 0.8 | — | 1 | — | ns |
| tkqhz(2,3) | Clock High to Output High-Z | — | 2.6 | — | 3.0 | ns |
| toeq | Output Enable to Output Valid | — | 2.6 | — | 3.0 | ns |
| toelz(2,3) | Output Enable to Output Low-Z | 0 | — | 0 | — | ns |
| toehz(2,3) | Output Disable to Output High-Z | — | 2.6 | — | 3.0 | ns |
| tas | Address Setup Time | 1.2 | — | 1.4 | — | ns |
| tws | Read/Write Setup Time | 1.2 | — | 1.4 | — | ns |
| tces | Chip Enable Setup Time | 1.2 | — | 1.4 | — | ns |
| tse | Clock Enable Setup Time | 1.2 | — | 1.4 | — | ns |
| tadvs | Address Advance Setup Time | 1.2 | — | 1.4 | — | ns |
| tds | Data Setup Time | 1.2 | — | 1.4 | — | ns |
| tah | Address Hold Time | 0.3 | — | 0.4 | — | ns |
| the | Clock Enable Hold Time | 0.3 | — | 0.4 | — | ns |
| twh | Write Hold Time | 0.3 | — | 0.4 | — | ns |
| tceh | Chip Enable Hold Time | 0.3 | — | 0.4 | — | ns |
| tadvh | Address Advance Hold Time | 0.3 | — | 0.4 | — | ns |
| tdh | Data Hold Time | 0.3 | — | 0.4 | — | ns |

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

### 3.3V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| $V_{TT}$ | 1.5V |
| $V_{LOAD}$ | 3.3V |
| R1, R2 | 317Ω, 351Ω |
| Output Load | See Figures 1 and 2 |

### 2.5V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 2.5V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.25V |
| $V_{TT}$ | 1.25V |
| $V_{LOAD}$ | 2.5V |
| R1, R2 | 1667Ω, 1538Ω |
| Output Load | See Figures 1 and 2 |

### 1.8V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 1.8V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 0.9V |
| $V_{TT}$ | 0.9V |
| $V_{LOAD}$ | 1.8V |
| R1, R2 | 1KΩ, 1KΩ |
| Output Load | See Figures 1 and 2 |

### I/O OUTPUT LOAD EQUIVALENT

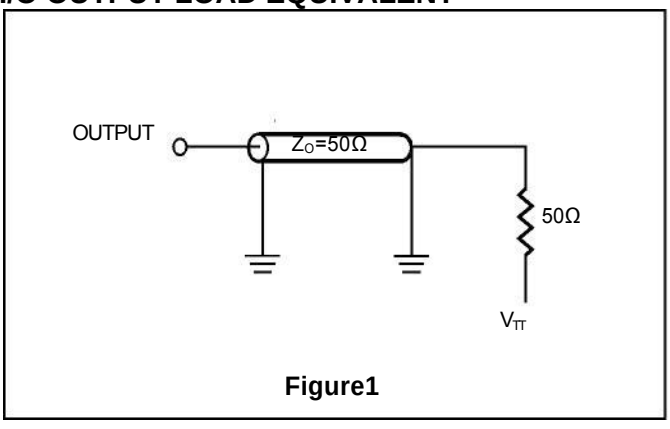



**Figure1**

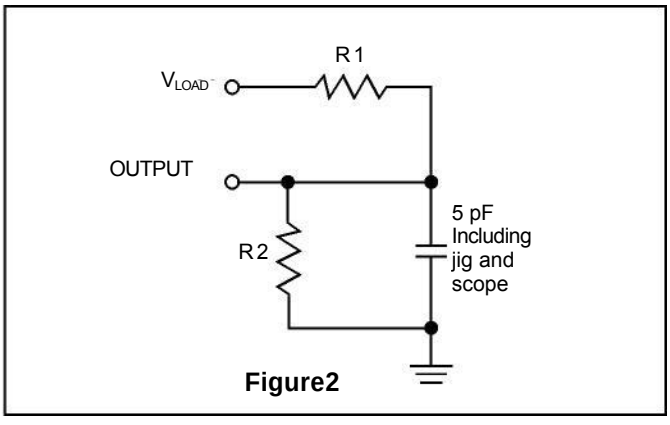
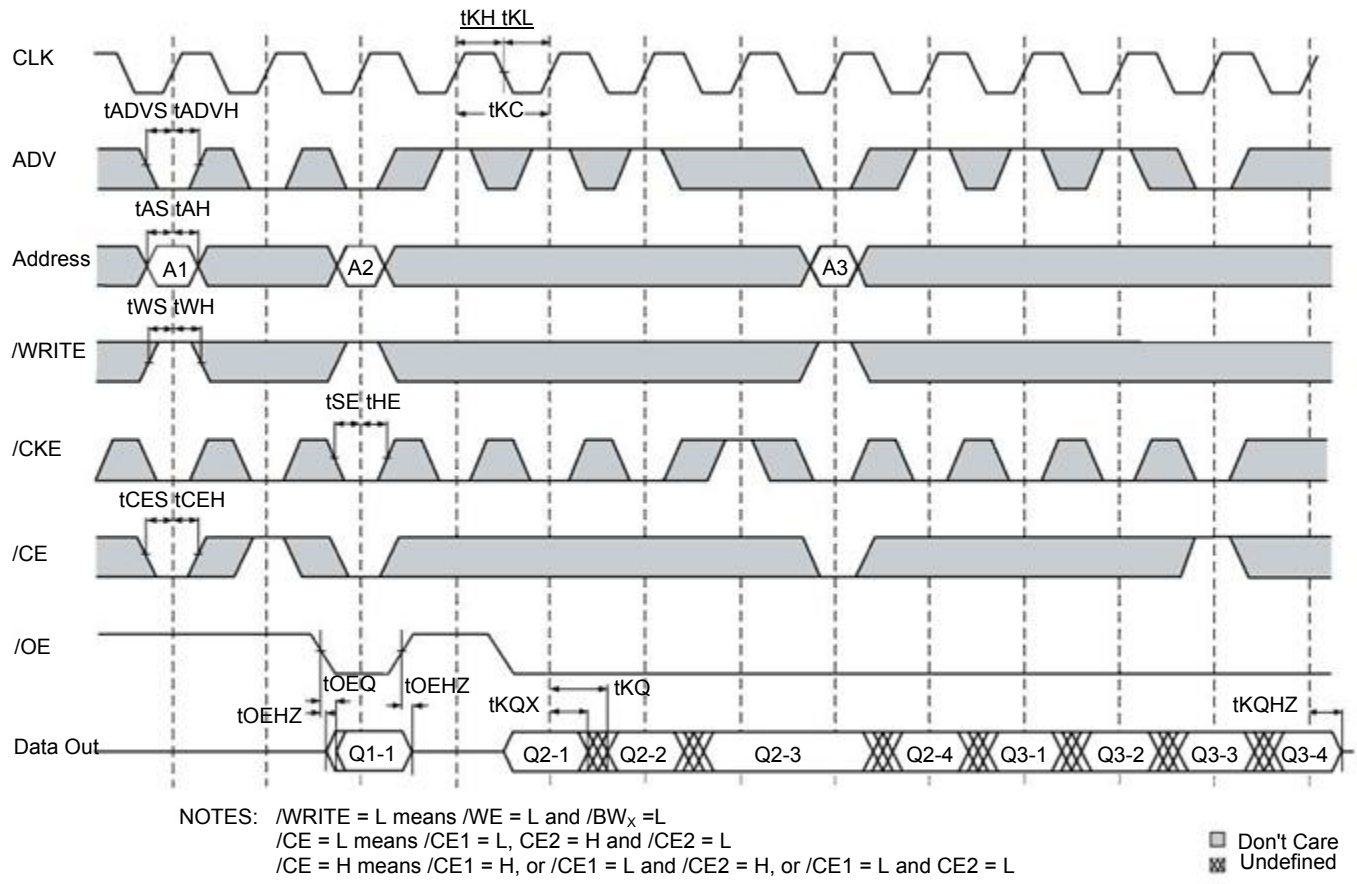
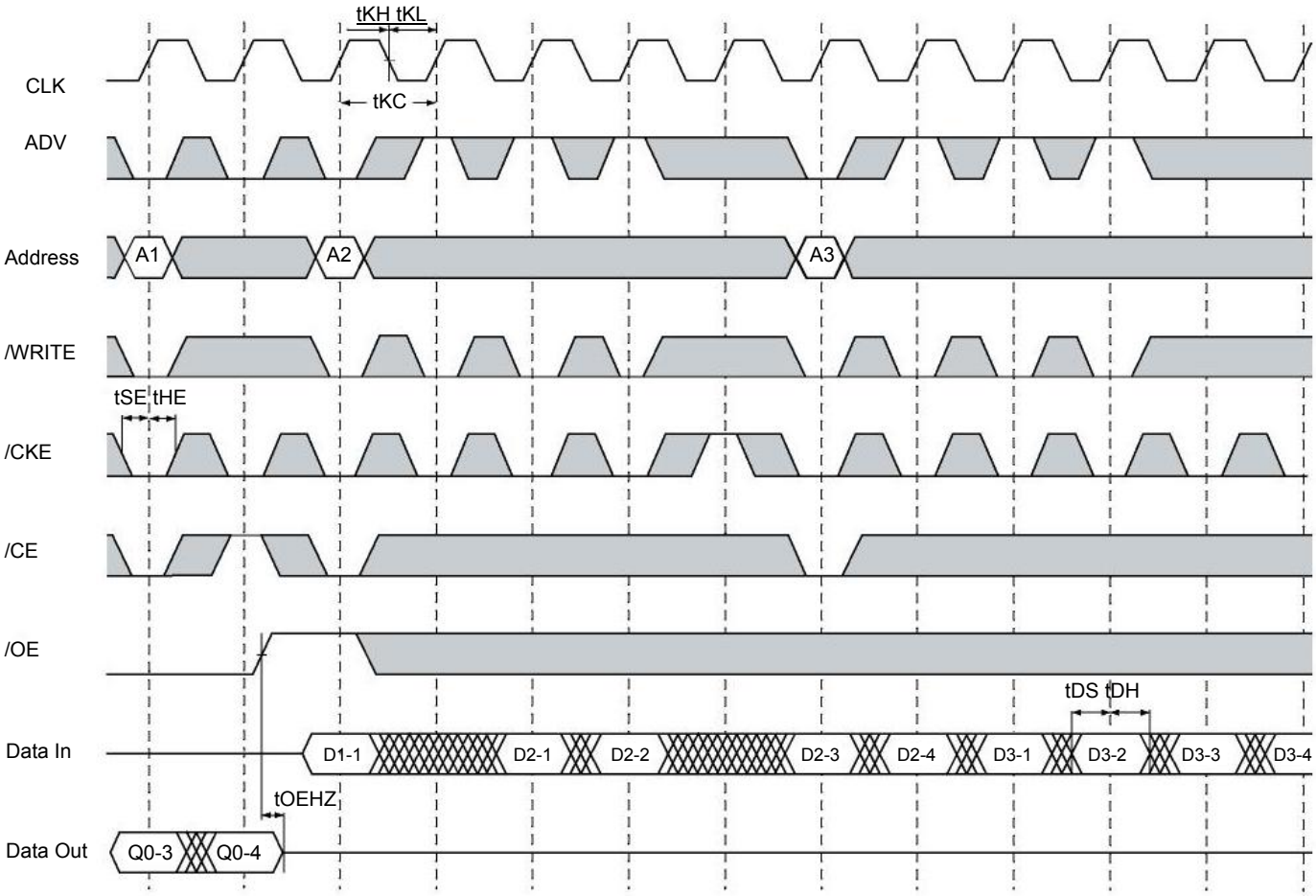



**Figure2**

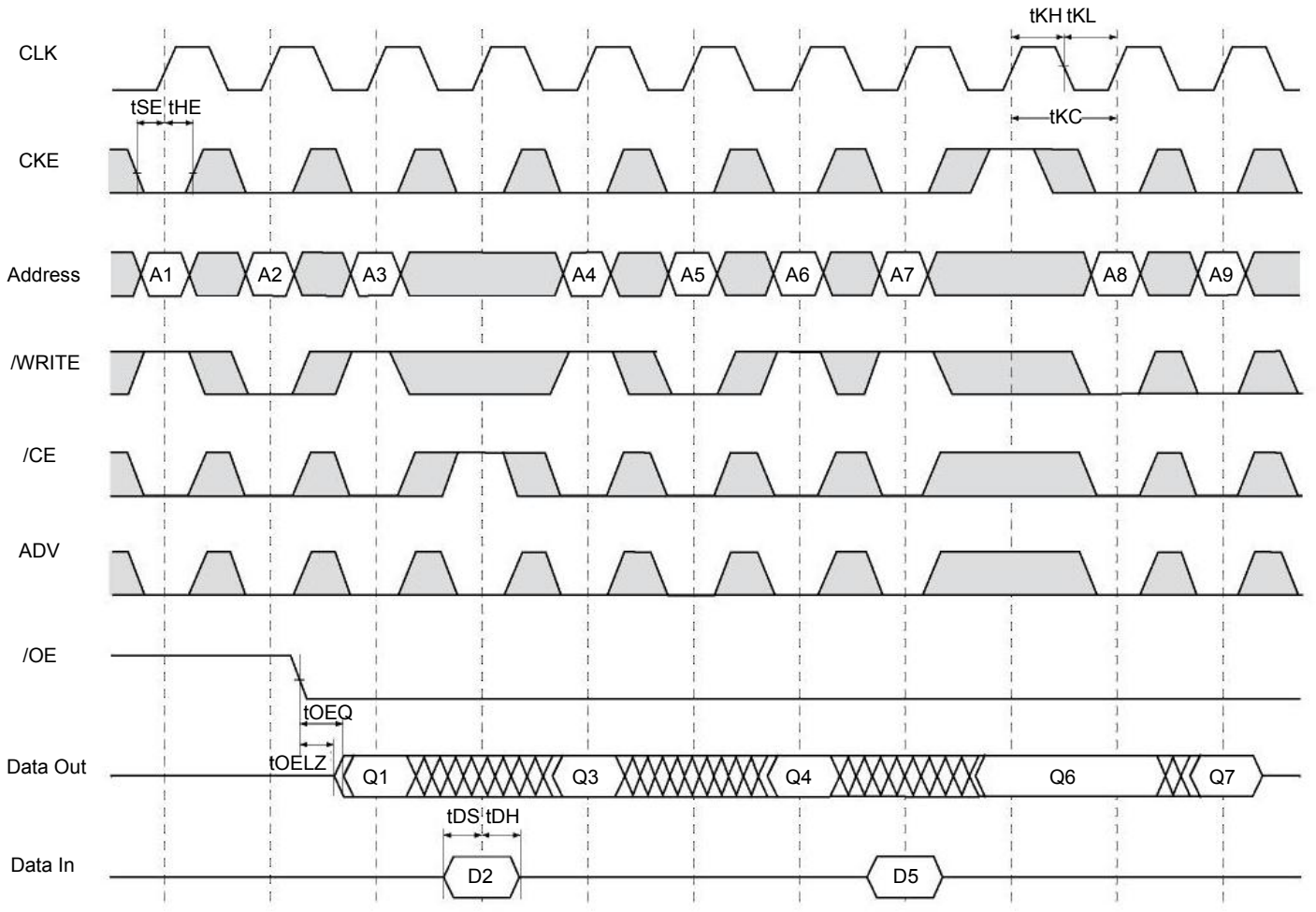
## READ CYCLE TIMING



## WRITE CYCLE TIMING

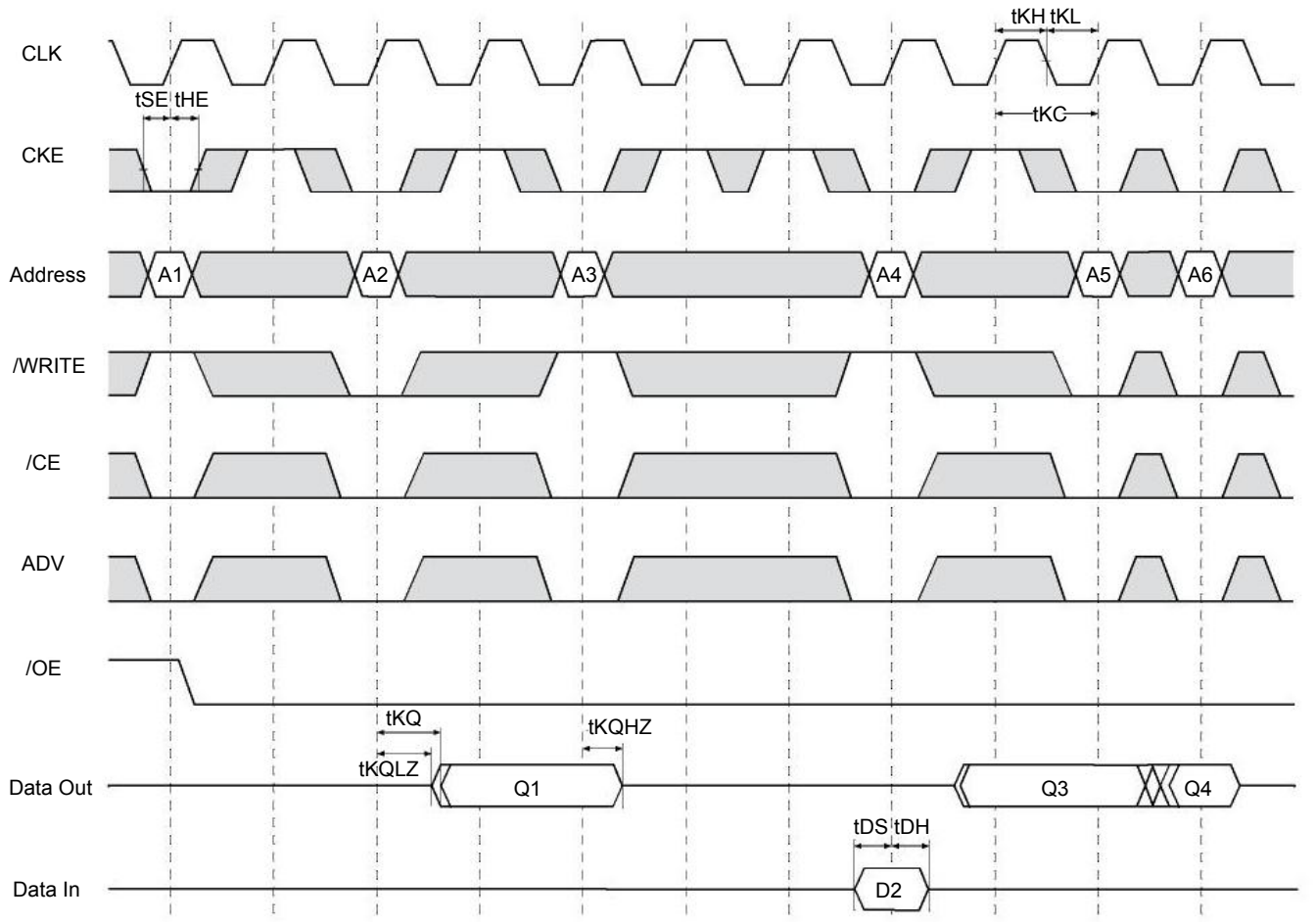


## SINGLE READ/WRITE CYCLE TIMING



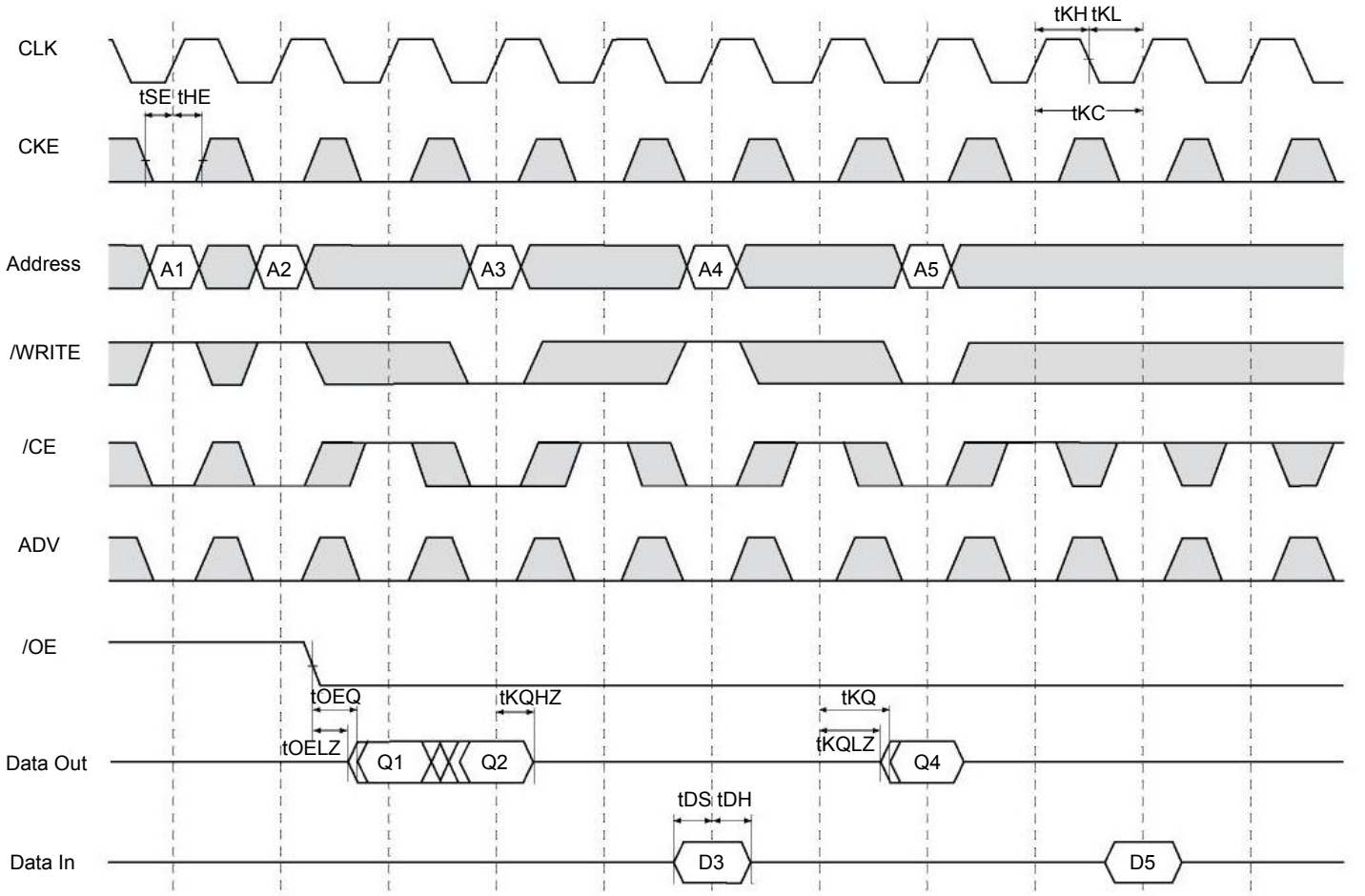

NOTES: /WRITE = L means /WE = L and /$BW_X$ = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

## /CKE OPERATION TIMING




NOTES: /WRITE = L means /WE = L and /$BW_X$ = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

## /CE OPERATION TIMING

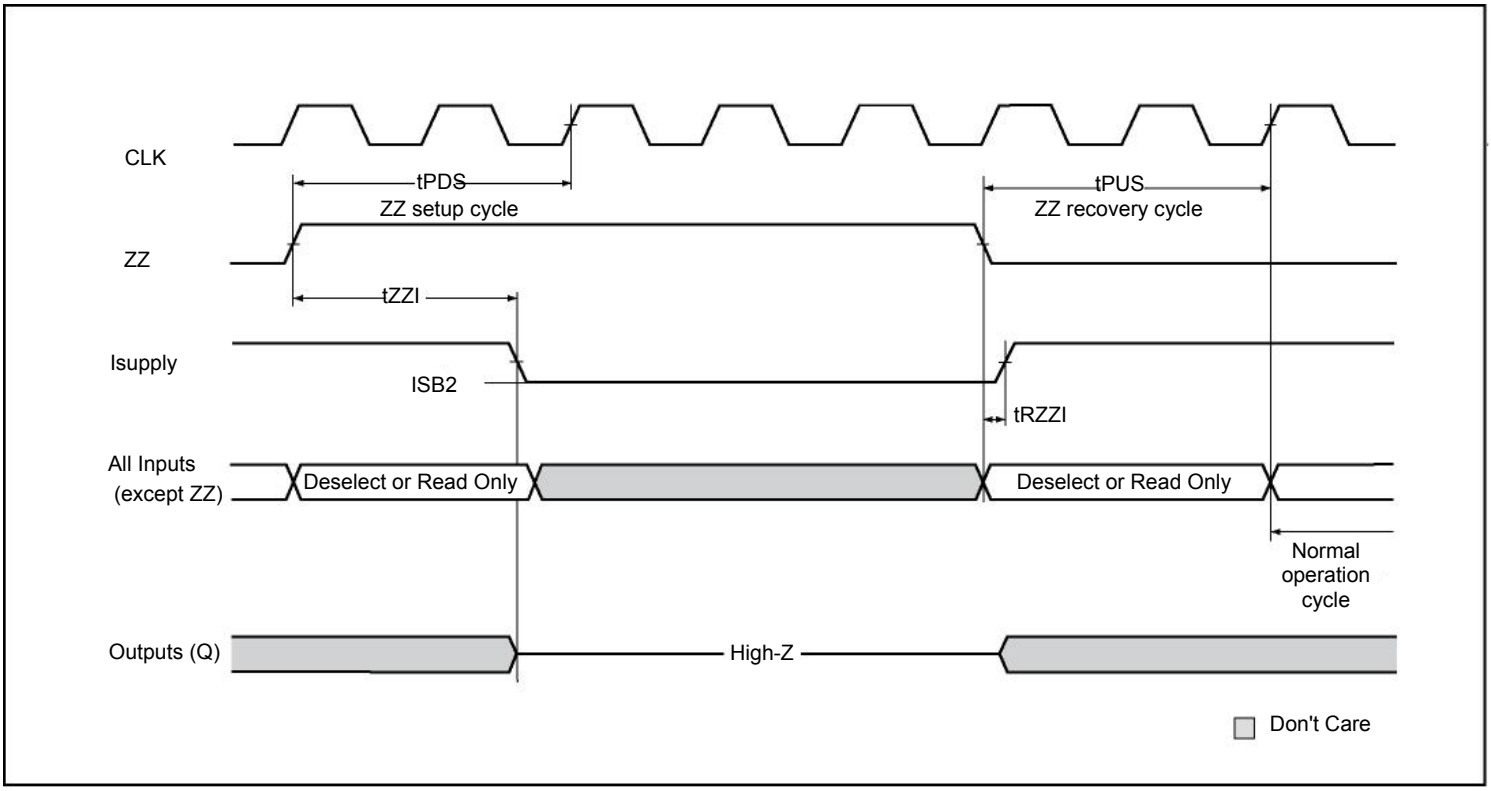



NOTES: /WRITE = L means /WE = L and /$BW_X$ = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

## SNOOZE MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Temperature Range | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| ISB2 | Current during SNOOZE MODE | ZZ ≥ Vih | Com. | — | 40 | mA |
| | | | Ind. | — | 50 | |
| | | | Auto. | — | TBD | |
| tPDS | ZZ active to input ignored | | — | — | 2 | cycle |
| tPUS | ZZ inactive to input sampled | | — | 2 | — | cycle |
| tZZI | ZZ active to SNOOZE current | | — | — | 2 | cycle |
| tRZZI | ZZ inactive to exit SNOOZE current | | — | 0 | — | ns |

## SLEEP MODE TIMING



## IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required

### Disabling the JTAG feature

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be left disconnected. They may alternately be connected to $V_{DD}$ through a pull-up resistor. TDO should be left disconnected. On power-up, the device will come up in a reset state, which will not interfere with device operation.

### Test Access Port Signal List:

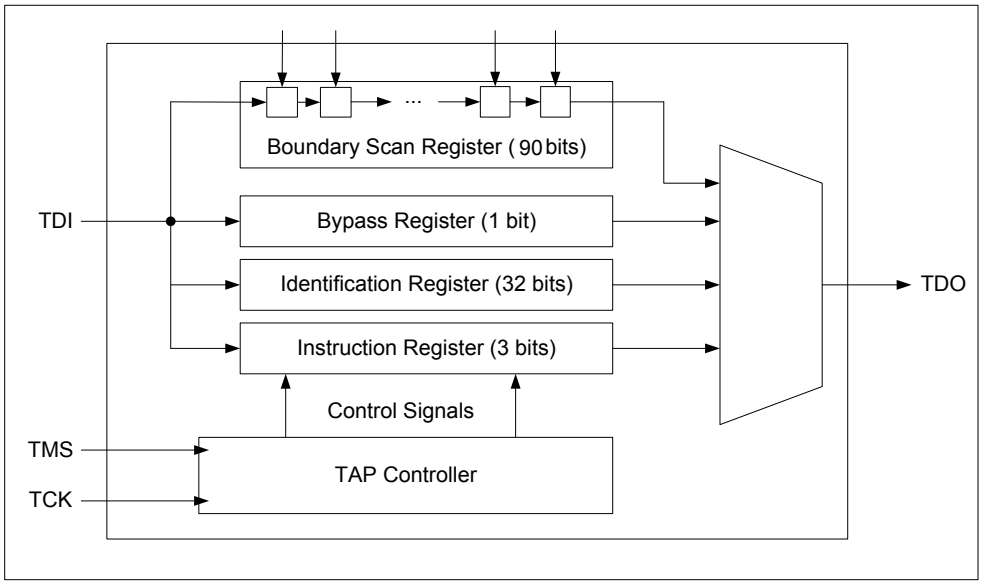
1. Test Clock (TCK)
This signal uses $V_{DD}$ as a power supply. The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

2. Test Mode Select (TMS)
This signal uses $V_{DD}$ as a power supply. The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK.

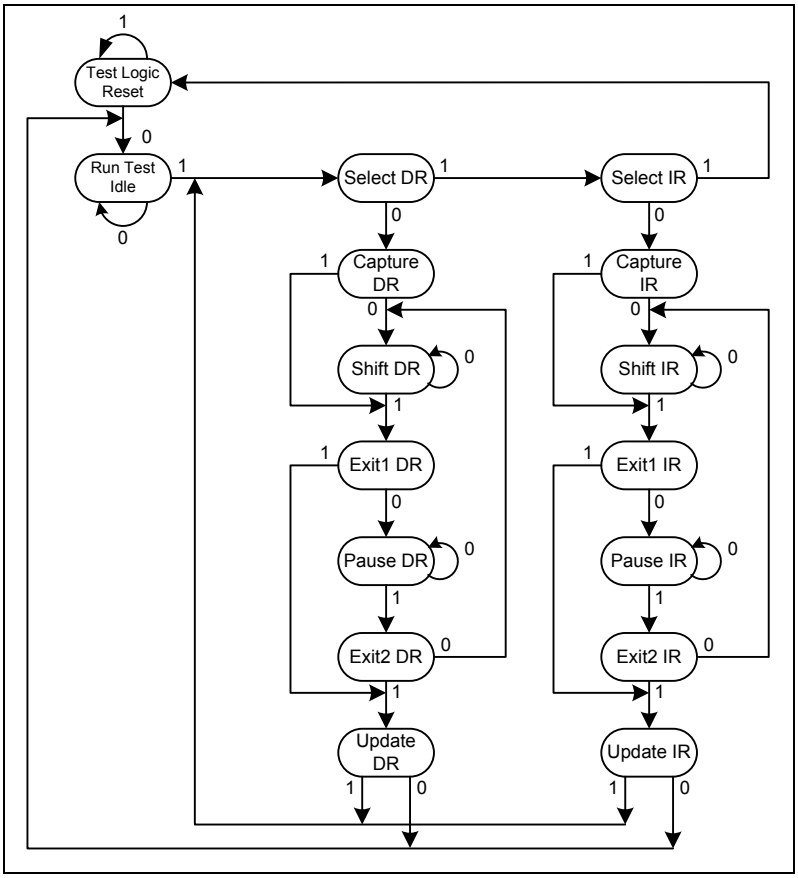
3. Test Data-In (TDI)
This signal uses $V_{DD}$ as a power supply. The TDI input is used to serially input test instructions and information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register. For more information regarding instruction register loading, please see the TAP Controller State Diagram.

4. Test Data-Out (TDO)
This signal uses $V_{DD}$ as a power supply. The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. For more information, please see the TAP Controller State Diagram.

## TAP Controller State and Block Diagram




## TAP Controller State Machine



### Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

### TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

#### 1. Instruction Register

This register is loaded during the update-IR state of the TAP controller. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

#### 2. Bypass Register

The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

#### 3. Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several balls are also included in the scan register to reserved balls. The boundary scan register is loaded with the contents of the SRAM Input and Output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

#### 4. Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the shift-DR state.

### Scan Register Sizes

| Register Name | Bit Size |
|---|---|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 90 |

### TAP Instruction Set

Many instructions are possible with an eight-bit instruction register and all valid combinations are listed in the TAP Instruction Code Table. All other instruction codes that are not listed on this table are reserved and should not be used. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the

TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

**1. EXTEST**
The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

**2. IDCODE**
The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

**3. SAMPLE Z**
If the SAMPLE-Z instruction is loaded in the instruction register, all SRAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the SRAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

**4. SAMPLE/PRELOAD**
When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register. The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible. To ensure that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time. The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/ PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register. Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.

**6. BYPASS**
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

**7. PRIVATE**
Do not use these instructions. They are reserved for future use and engineering mode.

### JTAG DC Operating Characteristics

(Over the Operating Temperature Range, 2.5V and 3.3V Option)

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| JTAG Input High Voltage | $V_{IH1}$ | 1.7 | $V_{DD}$+0.3 | V | |
| JTAG Input Low Voltage | $V_{IL1}$ | –0.3 | 0.7 | V | |
| JTAG Output High Voltage | $V_{OH1}$ | 1.7 | - | V | $\|I_{OH1}\|$=2mA |
| JTAG Output Low Voltage | $V_{OL1}$ | - | 0.7 | V | $I_{OL1}$=2mA |
| JTAG Output High Voltage | $V_{OH2}$ | 2.1 | - | V | $\|I_{OH2}\|$=100µA |
| JTAG Output Low Voltage | $V_{OL2}$ | - | 0.2 | V | $I_{OL2}$=100µA |
| JTAG Input Leakage Current | $I_{LIJTAG}$ | -10 | +10 | µA | 0 ≤ Vin ≤ $V_{DD}$ |
| JTAG Output Leakage Current | $I_{LOJTAG}$ | -10 | +10 | µA | 0 ≤ Vout ≤ $V_{DD}$ |

Notes:
1. All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTL-compatible.

### JTAG DC Operating Characteristics

(Over the Operating Temperature Range, 1.8V Option)

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| JTAG Input High Voltage | $V_{IH1}$ | TBD | TBD | V | |
| JTAG Input Low Voltage | $V_{IL1}$ | TBD | TBD | V | |
| JTAG Output High Voltage | $V_{OH1}$ | TBD | TBD | V | |
| JTAG Output Low Voltage | $V_{OL1}$ | TBD | TBD | V | |
| JTAG Input Leakage Current | $I_{LIJTAG}$ | TBD | TBD | µA | |
| JTAG Output Leakage Current | $I_{LOJTAG}$ | TBD | TBD | µA | |

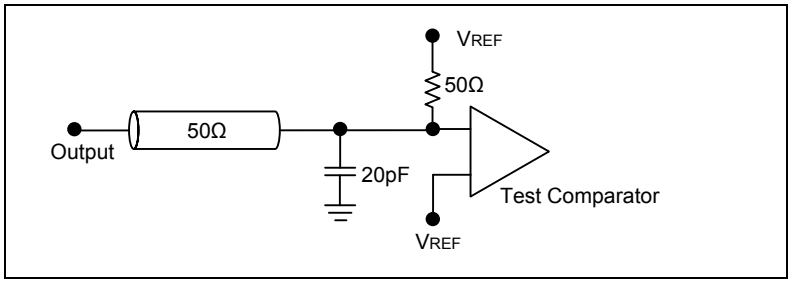
Notes:
1. All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTL-compatible.

### JTAG AC Test Conditions

(Over the Operating Temperature Range)

| Parameter | Symbol | 1.8V Option | 2.5V Option | 3.3V Option | Units |
|---|---|---|---|---|---|
| Input Pulse High Level | $V_{IH1}$ | TBD | 2.5 | 3.0 | V |
| Input Pulse Low Level | $V_{IL1}$ | TBD | 0 | 0 | V |
| Input rise and fall time | $T_{R1}$ | TBD | 1.5 | 1.5 | ns |
| Test load termination supply voltage | $V_{REF}$ | TBD | 1.25 | 1.5 | V |
| Input and Output Timing Reference Level | $V_{REF}$ | TBD | 1.25 | 1.5 | V |

TAP Output Load Equivalent

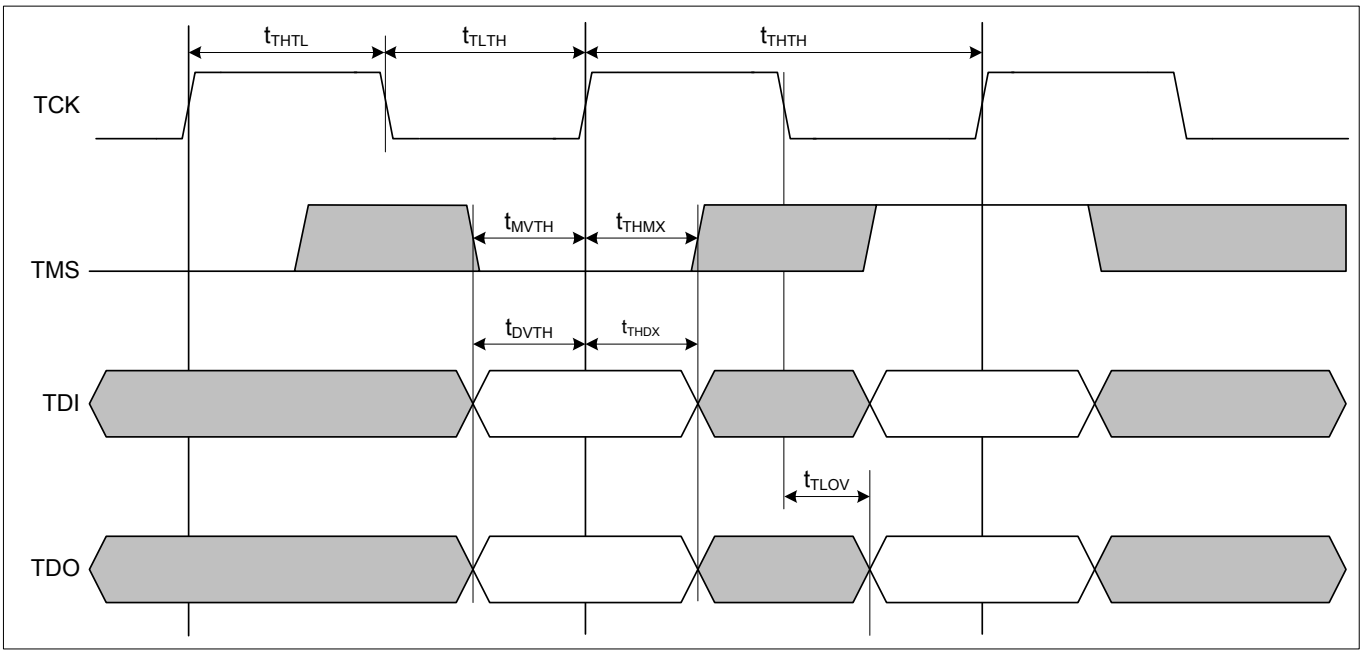


### JTAG AC Characteristics

(Over the Operating Temperature Range)

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| TCK cycle time | $t_{THTH}$ | 100 | – | ns |
| TCK high pulse width | $t_{THTL}$ | 40 | – | ns |
| TCK low pulse width | $t_{TLTH}$ | 40 | – | ns |
| TMS Setup | $t_{MVTH}$ | 10 | – | ns |
| TMS Hold | $t_{THMX}$ | 10 | – | ns |
| TDI Setup | $t_{DVTH}$ | 10 | – | ns |
| TDI Hold | $t_{THDX}$ | 10 | – | ns |
| TCK Low to Valid Data | $t_{TLOV}$ | – | 20 | ns |

### JTAG Timing Diagram



## Instruction Set

| Code | Instruction | TDO Output | Notes |
|---|---|---|---|
| 000 | EXTEST | Boundary Scan Register | 2, 6 |
| 001 | IDCODE | 32-bit Identification Register | |
| 010 | SAMPLE-Z | Boundary Scan Register | 1, 2 |
| 011 | PRIVATE | Do Not Use | 5 |
| 100 | SAMPLE(/PRELOAD) | Boundary Scan Register | 4 |
| 101 | PRIVATE | Do Not Use | 5 |
| 110 | PRIVATE | Do Not Use | 5 |
| 111 | BYPASS | Bypass Register | 3 |

Notes:
1. Places DQs in high-Z in order to sample all input data, regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to $V_{SS}$ when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the shift-DR state.
4. SAMPLE instruction does not place DQs in high-Z.
5. This instruction is reserved. Invoking this instruction will cause improper SRAM functionality.
6. By default, it places DQs in high-Z. If the internal register on the scan chain is set high, DQs will be updated with information loaded via a previous SAMPLE instruction. The actual transfer occurs during the update IR state after EXTEST is loaded. The value of the internal register can be changed during SAMPLE and EXTEST only.

## ID Register Definition

| Instruction Field | Description | 512K x 36 | 1024K x 18 |
|---|---|---|---|
| Revision Number (31:28) | Reserved for version number. | xxxx | xxxx |
| Device Depth (27:23) | Defines depth of SRAM. 512K or 1024K | 00111 | 01000 |
| Device Width (22:18) | Defines Width of the SRAM. x36 or x18 | 00100 | 00011 |
| ISSI Device ID (17:12) | Reserved for future use. | xxxxxx | xxxxxx |
| ISSI JEDEC ID (11:1) | Allows unique identification of SRAM vendor. | 00001010101 | 00001010101 |
| ID Register Presence (0) | Indicate the presence of an ID register. | 1 | 1 |

## Boundary Scan Order

*(TBA – 119 BGA)*

| 165 BGA | | | | |
|---|---|---|---|---|
| | X36 | | X18 | |
| Bit # | Bump ID | Signal | Bump ID | Signal |
| 1 | N6 | NC | N6 | NC |
| 2 | N7 | NC | N7 | NC |
| 3 | N10 | NC | N10 | NC |
| 4 | P11 | NC | P11 | NC |
| 5 | P8 | A18 | P8 | A18 |
| 6 | R8 | A17 | R8 | A17 |
| 7 | R9 | A16 | R9 | A16 |
| 8 | P9 | A15 | P9 | A15 |
| 9 | P10 | A14 | P10 | A14 |
| 10 | R10 | A13 | R10 | A13 |
| 11 | R11 | A12 | R11 | A12 |
| 12 | H11 | ZZ | H11 | ZZ |
| 13 | N11 | DQa0 | N11 | NC |
| 14 | M11 | DQa1 | M11 | NC |
| 15 | L11 | DQa2 | L11 | NC |
| 16 | M10 | DQa3 | M10 | DQa8 |
| 17 | L10 | DQa4 | L10 | DQa7 |
| 18 | K11 | DQa5 | K11 | NC |
| 19 | J11 | DQa6 | J11 | NC |
| 20 | K10 | DQa7 | K10 | DQa6 |
| 21 | J10 | DQa8 | J10 | DQa5 |
| 22 | H9 | NC | H9 | NC |
| 23 | H10 | NC | H10 | NC |
| 24 | G11 | DQb8 | G11 | DQa4 |
| 25 | F11 | DQb7 | F11 | DQa3 |
| 26 | G10 | DQb6 | G10 | NC |
| 27 | E11 | DQb5 | E11 | DQa2 |
| 28 | D11 | DQb4 | D11 | DQa1 |
| 29 | F10 | DQb3 | C11 | DQa0 |
| 30 | E10 | DQb2 | E10 | NC |
| 31 | D10 | DQb1 | D10 | NC |
| 32 | C11 | DQb0 | F10 | NC |
| 33 | A11 | NC | A11 | A19 |
| 34 | B11 | NC | B11 | NC |
| 35 | A10 | A11 | A10 | A11 |
| 36 | B10 | A10 | B10 | A10 |
| 37 | A9 | A9 | A9 | A9 |

Continued on next page

| 165 BGA | | | | |
|---|---|---|---|---|
| | X36 | | X18 | |
| Bit # | Bump ID | Signal | Bump ID | Signal |
| 38 | B9 | A8 | B9 | A8 |
| 39 | C10 | NC | C10 | NC |
| 40 | A8 | ADV | A8 | ADV |
| 41 | B8 | /OE | B8 | /OE |
| 42 | A7 | /CKE | A7 | /CKE |
| 43 | B7 | /WE | B7 | /WE |
| 44 | B6 | CLK | B6 | CLK |
| 45 | A6 | /CE2 | A6 | /CE2 |
| 46 | B5 | /Bwa | B5 | /Bwa |
| 47 | A5 | /Bwb | A5 | NC |
| 48 | A4 | /Bwc | A4 | /Bwb |
| 49 | B4 | /Bwd | B4 | NC |
| 50 | B3 | CE2 | B3 | CE2 |
| 51 | A3 | /CE1 | A3 | /CE1 |
| 52 | A2 | A7 | A2 | A7 |
| 53 | B2 | A6 | B2 | A6 |
| 54 | C2 | NC | C2 | NC |
| 55 | B1 | NC | B1 | NC |
| 56 | A1 | NC | A1 | NC |
| 57 | C1 | DQc0 | C1 | NC |
| 58 | D1 | DQc1 | D1 | NC |
| 59 | E1 | DQc2 | E1 | NC |
| 60 | D2 | DQc3 | D2 | DQb8 |
| 61 | E2 | DQc4 | E2 | DQb7 |
| 62 | F1 | DQc5 | F1 | NC |
| 63 | G1 | DQc6 | G1 | NC |
| 64 | F2 | DQc7 | F2 | DQb6 |
| 65 | G2 | DQc8 | G2 | DQb5 |
| 66 | H1 | NC | H1 | NC |
| 67 | H2 | NC | H2 | NC |
| 68 | H3 | NC | H3 | NC |
| 69 | J1 | DQd8 | J1 | DQb4 |
| 70 | K1 | DQd7 | K1 | DQb3 |
| 71 | J2 | DQd6 | J2 | NC |
| 72 | L1 | DQd5 | L1 | DQb2 |
| 73 | M1 | DQd4 | M1 | DQb1 |
| 74 | K2 | DQd3 | N1 | DQb0 |
| 75 | L2 | DQd2 | L2 | NC |
| 76 | M2 | DQd1 | M2 | NC |
| 77 | N1 | DQd0 | K2 | NC |
| 78 | N2 | NC | N2 | NC |
| 79 | P1 | NC | P1 | NC |

Continued on next page

| 165 BGA | | | | |
|---|---|---|---|---|
| | X36 | | X18 | |
| Bit # | Bump ID | Signal | Bump ID | Signal |
| 80 | R1 | MODE | R1 | MODE |
| 81 | R2 | NC | R2 | NC |
| 82 | P3 | A5 | P3 | A5 |
| 83 | R3 | A4 | R3 | A4 |
| 84 | P2 | NC | P2 | NC |
| 85 | P4 | A2 | P4 | A2 |
| 86 | R4 | A3 | R4 | A3 |
| 87 | N5 | NC | N5 | NC |
| 88 | P6 | A1 | P6 | A1 |
| 89 | R6 | A0 | R6 | A0 |
| 90 | * | Int | * | Int |

## ORDERING INFORMATION

**Commercial Range: 0°C to +70°C**

| $V_{DD}$ | Speed | X36 | X18 | Package |
|---|---|---|---|---|
| $V_{DD}$=3.3V, $V_{DDQ}$=2.5V/3.3V | 250MHz | IS61NLP51236B-250TQ | IS61NLP102418B-250TQ | 100 QFP |
| | | IS61NLP51236B-250B3 | IS61NLP102418B-250B3 | 165 BGA |
| | | IS61NLP51236B-250B2 | IS61NLP102418B-250B2 | 119 BGA |
| | | IS61NLP51236B-250TQL | IS61NLP102418B-250TQL | 100 QFP, Lead-free |
| | | IS61NLP51236B-250B3L | IS61NLP102418B-250B3L | 165 BGA, Lead-free |
| | | IS61NLP51236B-250B2L | IS61NLP102418B-250B2L | 119 BGA, Lead-free |
| | 200MHz | IS61NLP51236B-200TQ | IS61NLP102418B-200TQ | 100 QFP |
| | | IS61NLP51236B-200B3 | IS61NLP102418B-200B3 | 165 BGA |
| | | IS61NLP51236B-200B2 | IS61NLP102418B-200B2 | 119 BGA |
| | | IS61NLP51236B-200TQL | IS61NLP102418B-200TQL | 100 QFP, Lead-free |
| | | IS61NLP51236B-200B3L | IS61NLP102418B-200B3L | 165 BGA, Lead-free |
| | | IS61NLP51236B-200B2L | IS61NLP102418B-200B2L | 119 BGA, Lead-free |
| $V_{DD}$=2.5V, $V_{DDQ}$=2.5V | 250MHz | *Please contact ISSI Marketing | | |
| | 200MHz | IS61NVP51236B-200TQ | IS61NVP102418B-200TQ | 100 QFP |
| | | IS61NVP51236B-200B3 | IS61NVP102418B-200B3 | 165 BGA |
| | | IS61NVP51236B-200TQL | IS61NVP102418B-200TQL | 100 QFP, Lead-free |
| | | IS61NVP51236B-200B3L | IS61NVP102418B-200B3L | 165 BGA, Lead-free |
| $V_{DD}$=1.8V, $V_{DDQ}$=1.8V | 250MHz | *Please contact ISSI Marketing | | |
| | 200MHz | *Please contact ISSI Marketing | | |

**Industrial Range: -40°C to +85°C**

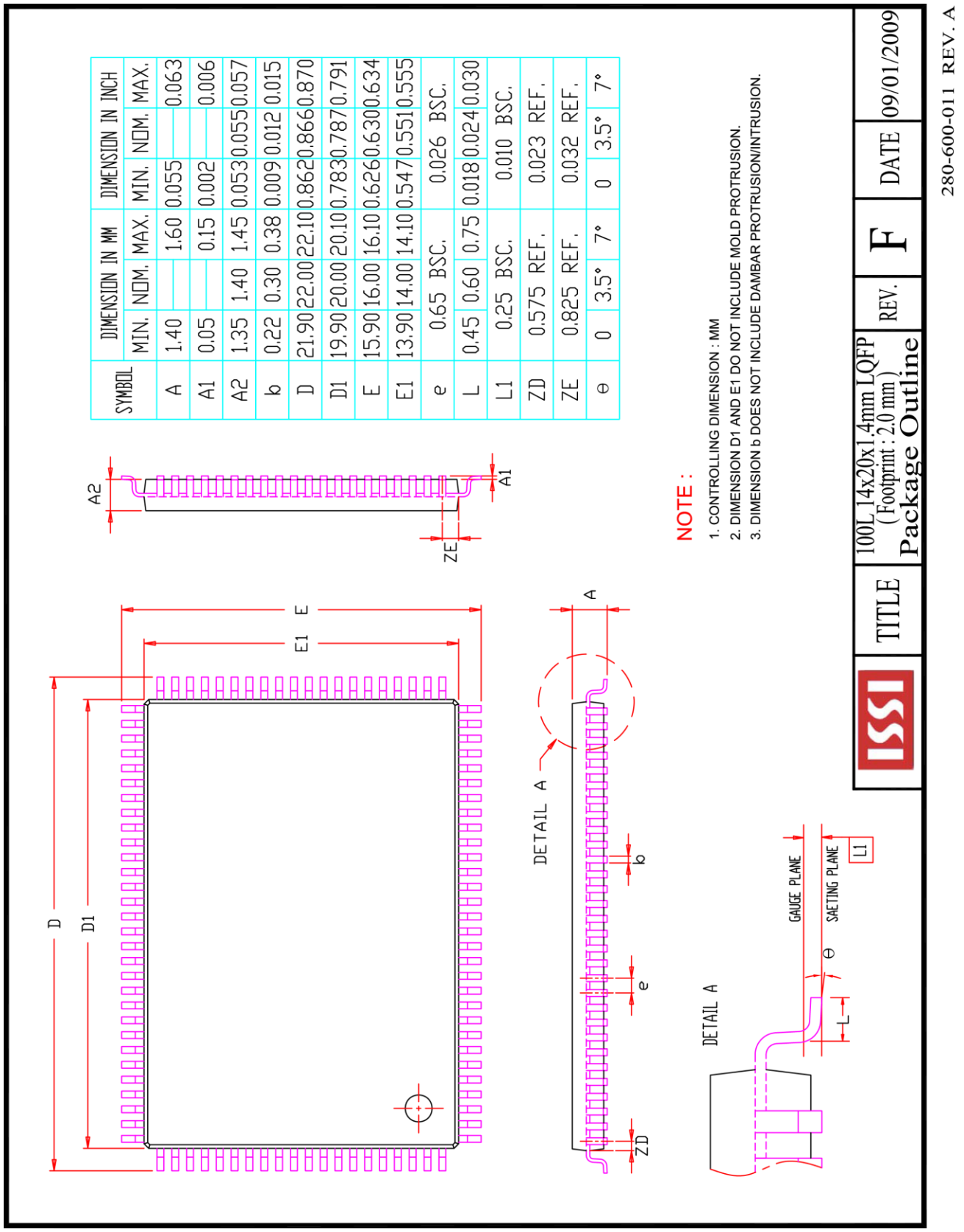
| $V_{DD}$ | Speed | X36 | X18 | Package |
|---|---|---|---|---|
| $V_{DD}$=3.3V, $V_{DDQ}$=2.5V/3.3V | 250MHz | IS61NLP51236B-250TQI | IS61NLP102418B-250TQI | 100 QFP |
| | | IS61NLP51236B-250B3I | IS61NLP102418B-250B3I | 165 BGA |
| | | IS61NLP51236B-250B2I | IS61NLP102418B-250B2I | 119 BGA |
| | | IS61NLP51236B-250TQLI | IS61NLP102418B-250TQLI | 100 QFP, Lead-free |
| | | IS61NLP51236B-250B3LI | IS61NLP102418B-250B3LI | 165 BGA, Lead-free |
| | | IS61NLP51236B-250B2LI | IS61NLP102418B-250B2LI | 119 BGA, Lead-free |
| | 200MHz | IS61NLP51236B-200TQI | IS61NLP102418B-200TQI | 100 QFP |
| | | IS61NLP51236B-200B3I | IS61NLP102418B-200B3I | 165 BGA |
| | | IS61NLP51236B-200B2I | IS61NLP102418B-200B2I | 119 BGA |
| | | IS61NLP51236B-200TQLI | IS61NLP102418B-200TQLI | 100 QFP, Lead-free |
| | | IS61NLP51236B-200B3LI | IS61NLP102418B-200B3LI | 165 BGA, Lead-free |
| | | IS61NLP51236B-200B2LI | IS61NLP102418B-200B2LI | 119 BGA, Lead-free |
| $V_{DD}$=2.5V, $V_{DDQ}$=2.5V | 250MHz | *Please contact ISSI Marketing | | |
| | 200MHz | IS61NVP51236B-200TQI | IS61NVP102418B-200TQI | 100 QFP |
| | | IS61NVP51236B-200B3I | IS61NVP102418B-200B3I | 165 BGA |
| | | IS61NVP51236B-200TQLI | IS61NVP102418B-200TQLI | 100 QFP, Lead-free |
| | | IS61NVP51236B-200B3LI | IS61NVP102418B-200B3LI | 165 BGA, Lead-free |
| $V_{DD}$=1.8V, $V_{DDQ}$=1.8V | 250MHz | *Please contact ISSI Marketing | | |
| | 200MHz | *Please contact ISSI Marketing | | |

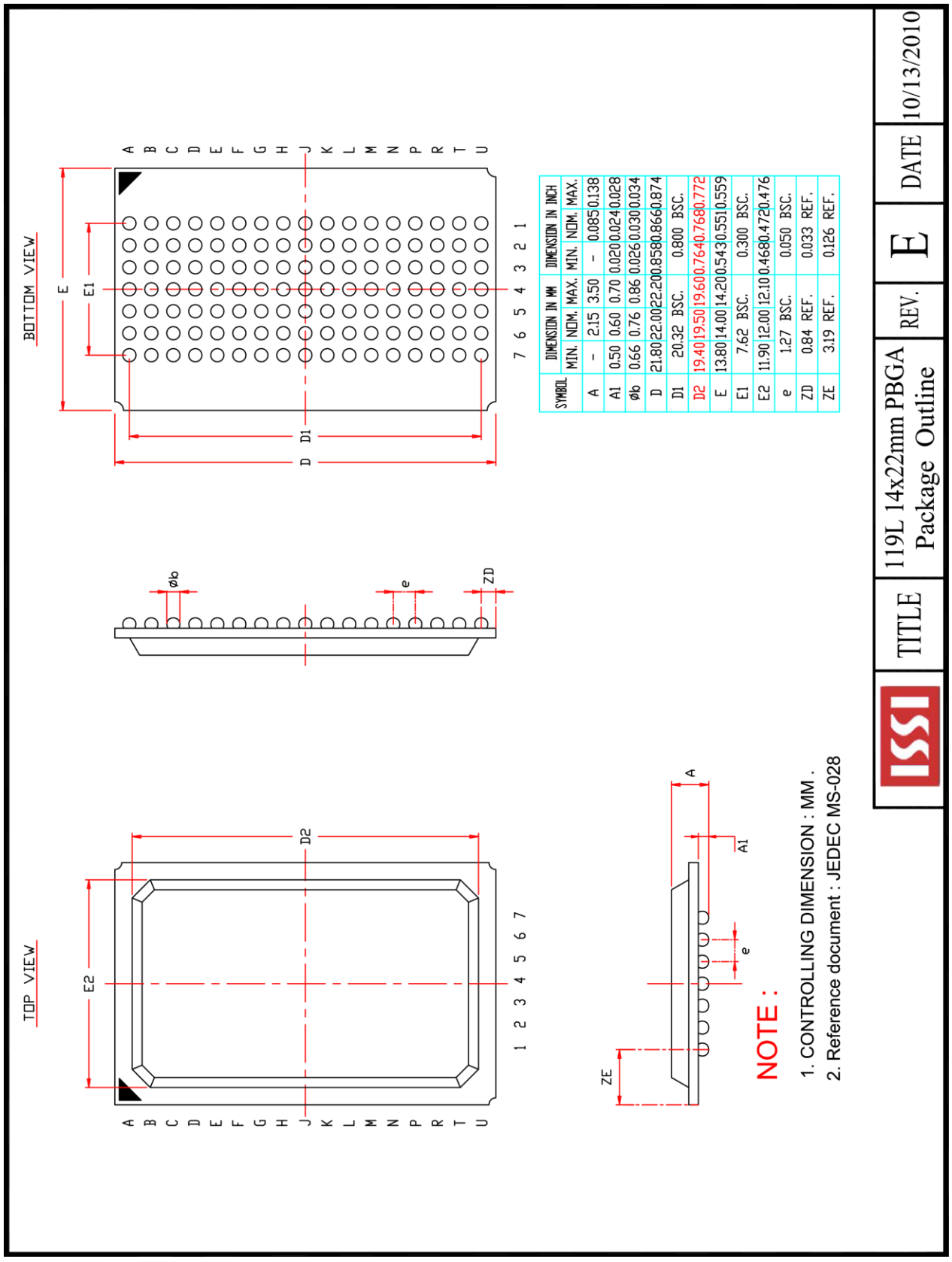
## ORDERING INFORMATION

**Automotive (A3) Range: -40°C to +125°C**

| $V_{DD}$ | Speed | X36 | Package |
|---|---|---|---|
| $V_{DD}$=3.3V, $V_{DDQ}$=2.5V/3.3V | 250MHz | IS64NLP51236B-250TQLA3 | 100 QFP, Lead-free |
| | | IS64NLP51236B-250B3LA3 | 165 BGA, Lead-free |
| | | IS64NLP51236B-250B2LA3 | 119 BGA, Lead-free |
| | 200MHz | IS64NLP51236B-200TQLA3 | 100 QFP, Lead-free |
| | | IS64NLP51236B-200B3LA3 | 165 BGA, Lead-free |
| | | IS64NLP51236B-200B2LA3 | 119 BGA, Lead-free |

**For all other voltages and options in automotive grade, please contact ISSI.*


SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A 1.40 — 1.60 0.055 — 0.063
A1 0.05 — 0.15 0.002 — 0.006
A2 1.35 1.40 1.45 0.053 0.055 0.057
b 0.22 0.30 0.38 0.009 0.012 0.015
D 21.90 22.00 22.10 0.862 0.866 0.870
D1 19.90 20.00 20.10 0.783 0.787 0.791
E 15.90 16.00 16.10 0.626 0.630 0.634
E1 13.90 14.00 14.10 0.547 0.551 0.555
e 0.65 BSC. 0.026 BSC.
L 0.45 0.60 0.75 0.018 0.024 0.030
L1 0.25 BSC. 0.010 BSC.
ZD 0.575 REF. 0.023 REF.
ZE 0.825 REF. 0.032 REF.
θ 0 3.5° 7° 0 3.5° 7°
NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
TITLE
100L 14x20x1.4mm LQFP (Footprint : 2.0 mm) Package Outline
REV. F
DATE 09/01/2009
280-600-011 REV. A
A2
A1
ZE
E
E1
D
D1
DETAIL A
A
b
e
ZD
GAUGE PLANE
SEATING PLANE
θ
L
L1

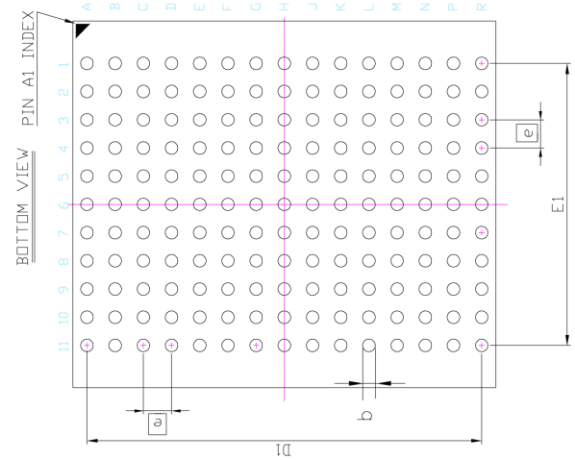


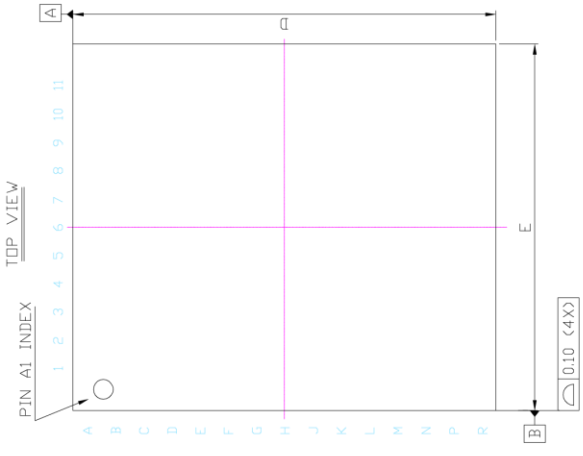

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | – | 2.15 | 3.50 | – | 0.085 | 0.138 |
| A1 | 0.50 | 0.60 | 0.70 | 0.020 | 0.024 | 0.028 |
| Øb | 0.66 | 0.76 | 0.86 | 0.026 | 0.030 | 0.034 |
| D | 21.80 | 22.00 | 22.20 | 0.858 | 0.866 | 0.874 |
| D1 | | 20.32 BSC. | | | 0.800 BSC. | |
| D2 | 19.40 | 19.50 | 19.60 | 0.764 | 0.768 | 0.772 |
| E | 13.80 | 14.00 | 14.20 | 0.543 | 0.551 | 0.559 |
| E1 | | 7.62 BSC. | | | 0.300 BSC. | |
| E2 | 11.90 | 12.00 | 12.10 | 0.468 | 0.472 | 0.476 |
| e | | 1.27 BSC. | | | 0.050 BSC. | |
| ZD | | 0.84 REF. | | | 0.033 REF. | |
| ZE | | 3.19 REF. | | | 0.126 REF. | |

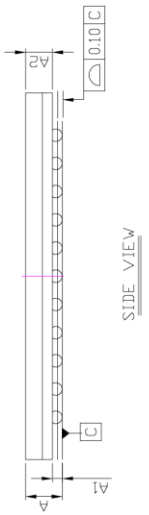
| SYM. | DIMENSION (mm) | | | DIMENSION (inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.25 | 0.35 | 0.40 | 0.010 | 0.014 | 0.016 |
| A2 | — | 0.79 | — | — | 0.031 | — |
| b | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| D | 14.90 | 15.00 | 15.10 | 0.587 | 0.591 | 0.594 |
| D1 | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 12.90 | 13.00 | 13.10 | 0.508 | 0.512 | 0.516 |
| E1 | 9.90 | 10.00 | 10.10 | 0.390 | 0.394 | 0.398 |
| e | 1.00 BSC | | | 0.039 BSC | | |

NOTE :

1. CONTROLLING DIMENSION : MM .




| ISSI | TITLE | 165L 13x15mm TF-BGA Package Outline | REV. | B | DATE | 08/28/2008 |
|---|---|---|---|---|---|---|

LifeElectronics
Живое партнерство

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*ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703*

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