KSZ9692MPB/KSZ9692XPB

Integrated Gigabit Networking and Communications Controller

Rev. 4.0

General Description

The KSZ9692MPB/KSZ9692XPB is a highly-integrated System-on-Chip (SoC) containing an ARM 922T 32-bit processor and a rich set of peripherals to address the cost-sensitive, high-performance needs of a wide variety of high-bandwidth networking and communications applications.

Features

ARM 922T High-Performance Processor Core

- 250 MHz ARM 922T RISC processor core
- 8KB I-cache and 8KB D-cache
- Configurable Memory Management Unit (MMU) for Linux and WinCE

Memory Controller

- 8/16-bit external bus interface for FLASH, ROM, SRAM, and external I/O
- NAND FLASH controller with boot option
- 200MHz 32-bit DDR controller
- Two JEDEC Specification JESD82-1-compliant differential clock drivers for a glueless DDR interface solution

Ethernet Interfaces

- Two Gb (10/100/1000 Mbps) MACs
- MII or RGMII interface
- Fully compliant with IEEE 802.3 Ethernet standards

PCI Interface

- Version PCI 2.3
- 32-bit 33/66 MHz
- Integrated PCI Arbiter supports three external masters for KSZ9692MPB and one external master for KSZ9692XPB
- Configurable as Host bridge or Guest device
- Glueless Support for mini-PCI or CardBus devices

Dual High-Speed USB 2.0 Interfaces

- Two USB2.0 ports with integrated PHY
- Can be configured as 2-port host, or host + device

SDIO/SD Host Controller (for KSZ9692MPB only)

- Meets SD Host Controller Standard Specification Version 1.0
- Meets SDIO card specification Version 1.0

DMA Controllers

- Dedicated DMA channels for PCI, USB, SDIO and Ethernet ports.

Peripherals

- Four high-speed UART ports up to 5 Mbps
- Two programmable 32-bit timers with watchdog timer capability
- Interrupt Controller
- Twenty GPIO ports
- One shared SPI/I2C interface
- One I2S port

Debugging

- ARM9 JTAG debug interface
- JTAG Boundary Scan Support

Power Management

- CPU and system clock speed step-down options
- Ethernet port Wake-on-LAN
- DDR and PCI power down

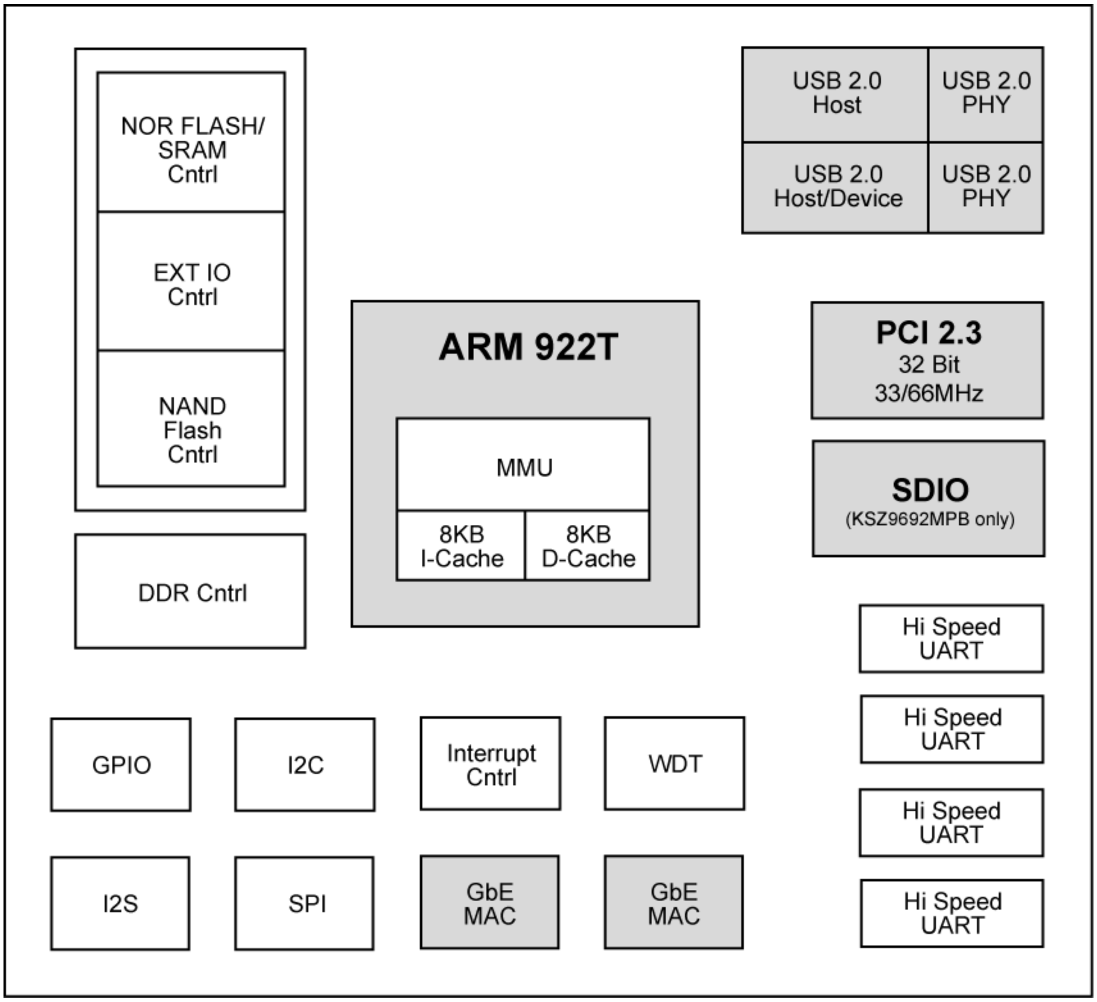
Operating Voltage

- 1.3V power for core
- 3.3V power for I/O
- 2.5V or 2.6V power for DDR memory interface

Reference Hardware and Software Evaluation Kit

- Hardware Evaluation Kit
- Software Evaluation Kit includes WinCE BSP, Open WRT BSP, Linux based SOHO Router packages

Block Diagram



Note: SDIO block for KSZ9692MPB only.

Figure 1. KSZ9692MPB/XPB Block Diagram

Applications

- Enhanced residential gateways
- High-end printer servers
- USB device servers
- IP-based multimedia systems
- Voice-over-Internet Protocol (VoIP) systems
- Set-top box
- Industrial control
- Wireless Access Points or Mesh Nodes

Ordering Information

Part Number	Temp. Range	Package	Lead Finish
KSZ9692MPB	0°C to 70°C	400-Pin PBGA	Pb-Free
KSZ9692MPBI(1)	-40°C to 85°C	400-Pin PBGA	Pb-Free
KSZ9692XPB(2)	0°C to 70°C	400-Pin PBGA	Pb-Free

Notes:

1. Industrial version of KSZ9692MPB.
2. support for one PCI Master. No SDIO.

Revision History

Revision	Date	Summary of Changes
1.0	10/14/08	Initial Release
2.0	3/10/09	Power Sequencing, Added A1 (PMEN) to pin list, 1.3V Supply for Core, Power Consumption table
3.0	8/10/09	DDR Data Width Changed to 16-bit
4.0	01/28/10	DDR Data Width Changed to 32-bit

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System Level Applications

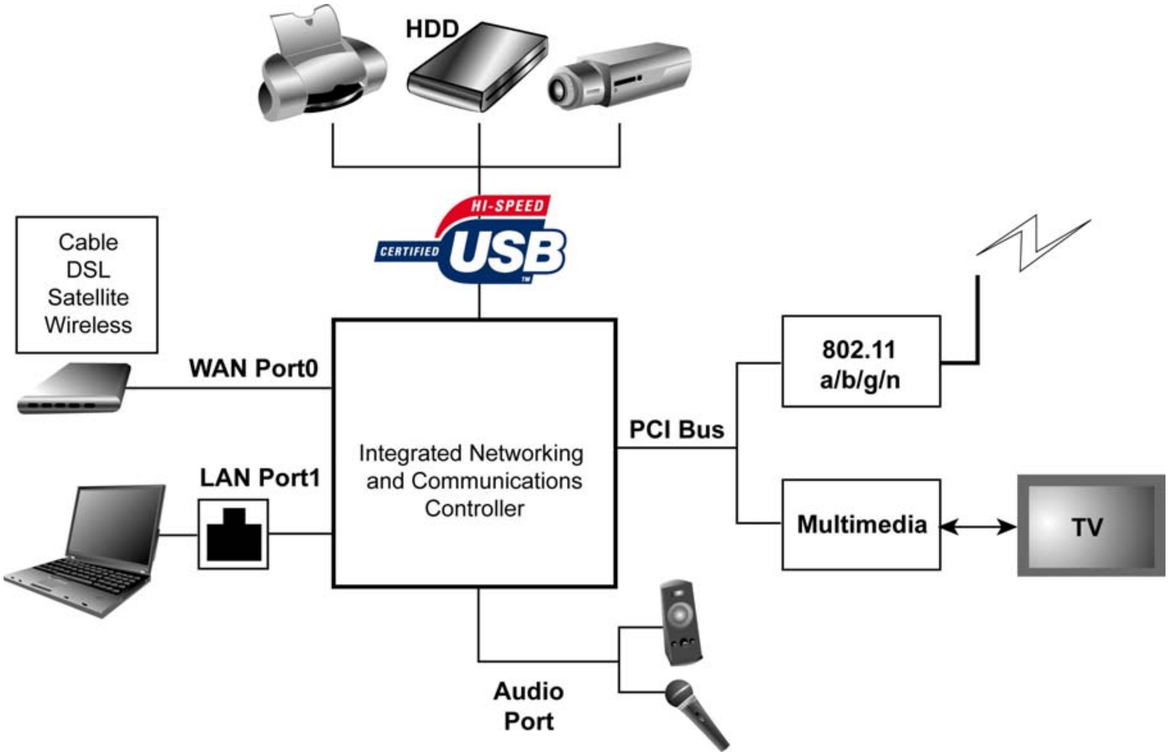

Figure 2. Peripheral Options and Examples

Functional Description

The KSZ9692MPB/KSZ9692XPB is a highly-integrated embedded application controller that is designed to provide a single-chip solution for a wide range of applications that require high-speed networking, multiple I/O controllers and interface to standard peripherals. It features a powerful 32-bit ARM RISC processor, DDR memory controller, FLASH/ROM/SRAM/External I/O interface, NAND memory controller, two Gb Ethernet MACs, two USB 2.0 ports, PCI 2.3 bus interface, SDIO interface (for KSZ9692MPB only), and a large number of standard peripherals including UARTs, I2C, I2S, SPI, MIB counters, Station Manager, timers, interrupt controller and GPIOs.

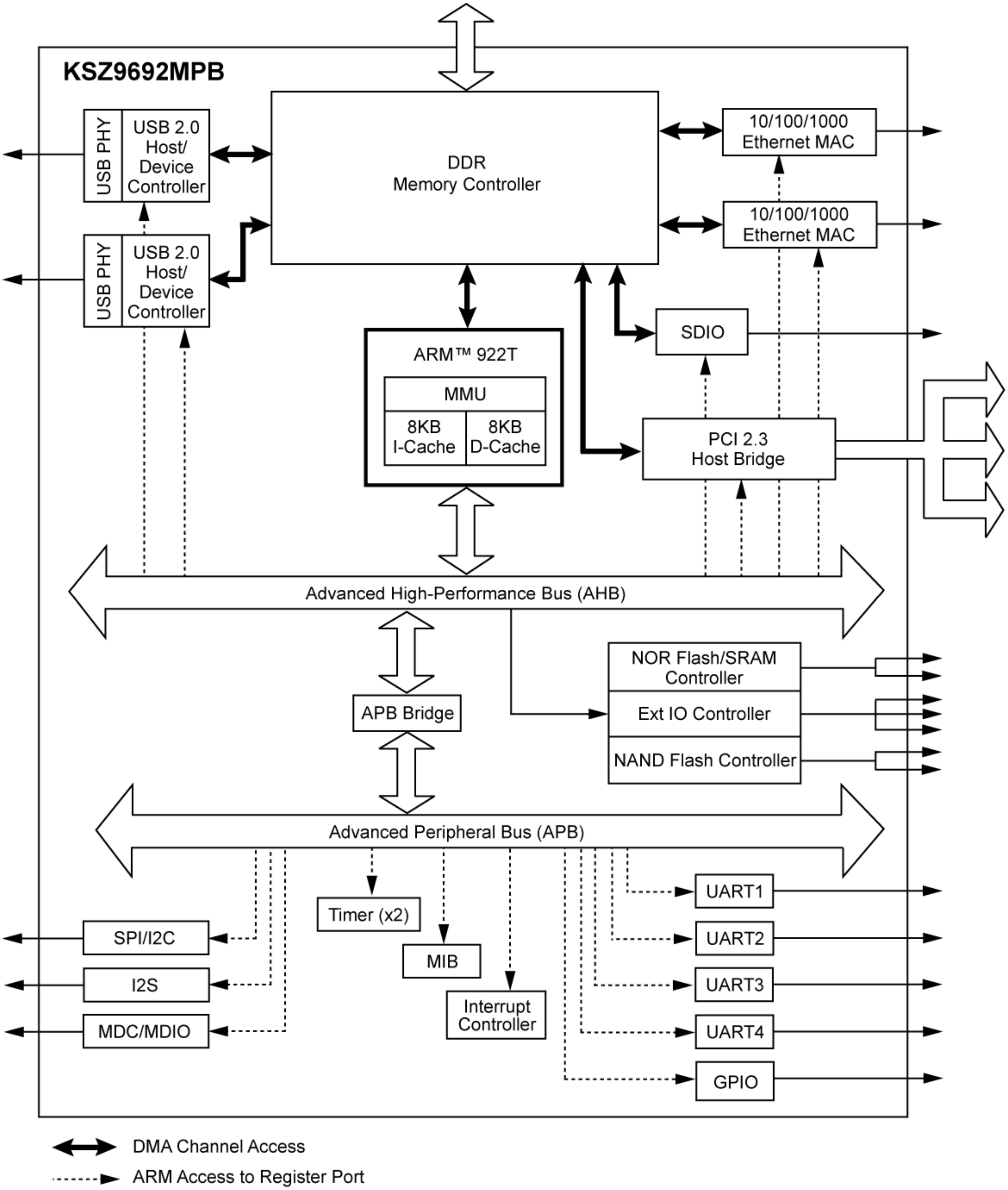

Figure 3. KSZ9692MPB Functional Block Diagram

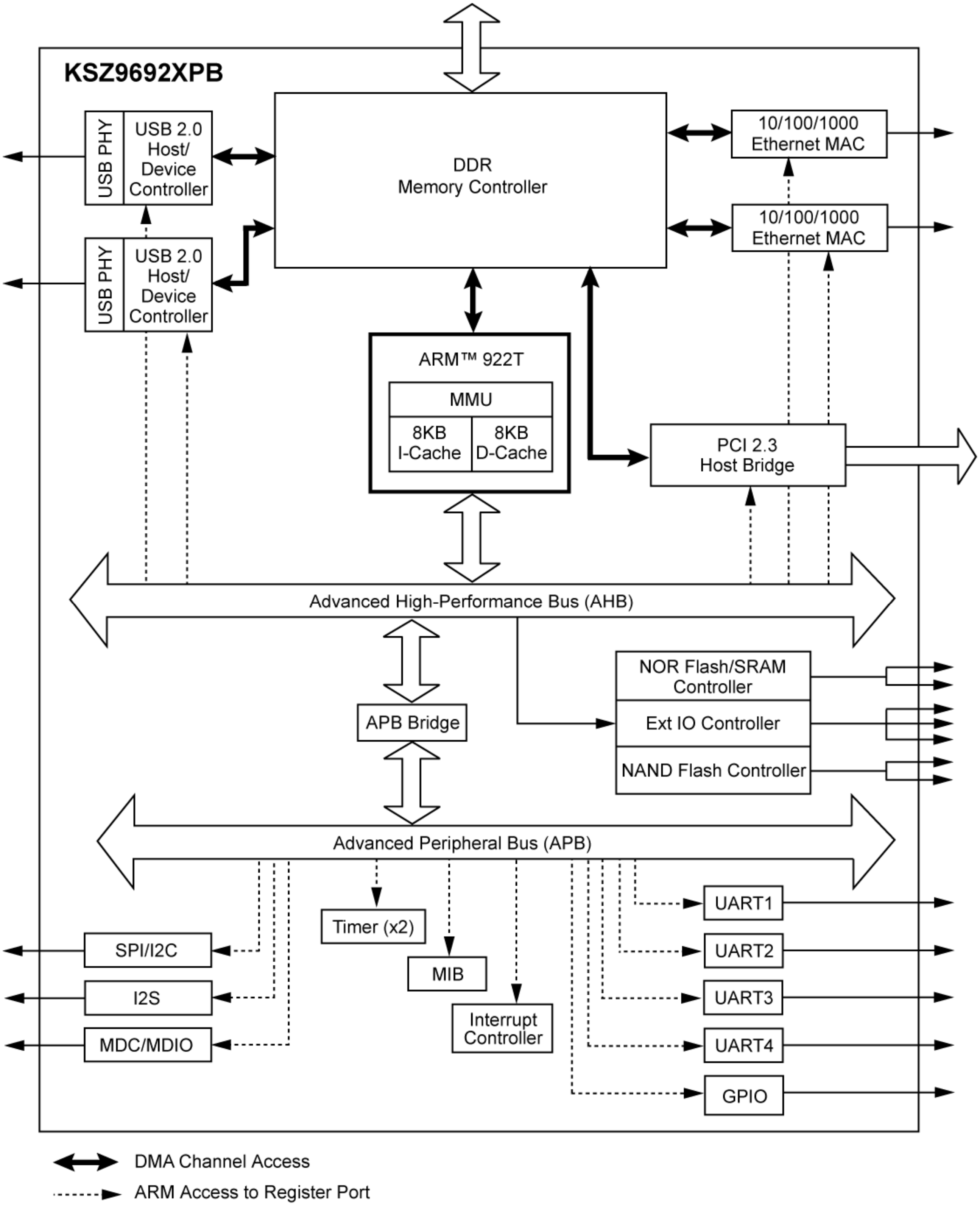

Figure 4. KSZ9692XPB Functional Block Diagram

ARM High-Performance Processor

The KSZ9692MPB/KSZ9692XPB is built around the 16/32-bit ARM922T RISC processor designed by Advanced RISC Machines. The ARM922T is a scalable, high-performance processor that was developed for highly integrated SoC applications. Its simple, elegant, and fully static design is particularly suited to cost-effective and power-sensitive embedded systems. It also offers a separate 8KB D-cache and 8KB I-cache that reduces memory access latency.16-bit thumb instruction sets are supported to minimize memory footprint. The ARM processor core can be programmed to maximum of 250 MHz for highest possible performance.

The Advanced Microprocessor Bus Architecture/Advanced High Performance Bus (AMBA AHB) is a 32-bit wide ARM system bus to which is connected the processor, the register ports of the DDR memory controller, the FLASH/ROM/SRAM/External I/O controller, the NAND memory controller, the Ethernet MACs, the PCI bridge, the USB ports and the SDIO controller (for KSZ9692MPB only). The ARM processor is the master of AHB and responsible for configuring the operational characteristics of each AHB device via their individual register port. The AHB is programmable up to 166MHz for maximum system bus performance. AHB interfaces to devices are shown in functional block diagram.

Also connected to AHB is ARM Advanced Peripheral Bus or APB bridge which is attached the standard peripherals. The APB Bridge transparently converts the AHB accesses into slower APB accesses. The ARM processor is the master of APB bridge and responsible for configuring the operational characteristics and transfer of data for each APB attached peripheral. APB interfaces to standard peripherals are shown in the functional block diagrams on page 8 and 9.

- 250MHz ARM922T RISC processor core
- 166MHz AMBA Bus 2.0
- 16-bit thumb instruction sets
- 8KB D-cache and 8KB I-cache
- Supports Little-Endian mode
- Configurable MMU
- Power saving options include clock down of both processor core and AMBA AHB

FLASH/ROM/SRAM Memory and External I/O Interface

The KSZ9692MPB/KSZ9692XPB memory controller provides glueless interface for static memory, i.e., ROM, SRAM, and NOR Flash and three banks of external I/O. NOR Flash bank0 can be configured by power-up strap option to operate as boot bank from a 8 or 16 bit device.

- Glueless connection to two banks of FLASH/ROM/SRAM memory with programmable 8 or 16 bit data width and programmable access timing
- Support for AMD/Intel like Flash
- Automatic address line mapping for 8 or 16-bit accesses on Flash, ROM, and SRAM interfaces
- Supports three external I/O banks with programmable 8 or 16 bit data width and programmable access timing
- Total 64MB address space for two banks of FLASH/ROM/SRAM and and three banks of external I/O

The memory interface for the static memory has a special automatic address mapping feature. This allows the designer to connect address bit 0 on the memory to ADDR[0] on the KSZ9692MPB/KSZ9692XPB and address bit 1 on the memory to ADDR[1] on the KSZ9692MPB/KSZ9692XPB, regardless of whether the designer is trying to achieve half word or byte addressing. The KSZ9692MPB/KSZ9692XPB memory controller performs the address mapping internally. This gives the designer the flexibilty to use 8 or 16 bit data width devices interchangeably on the same PCB (see Figure 4). For external I/O, however, the designer still needs to resolve the address mapping (see Figure 5).

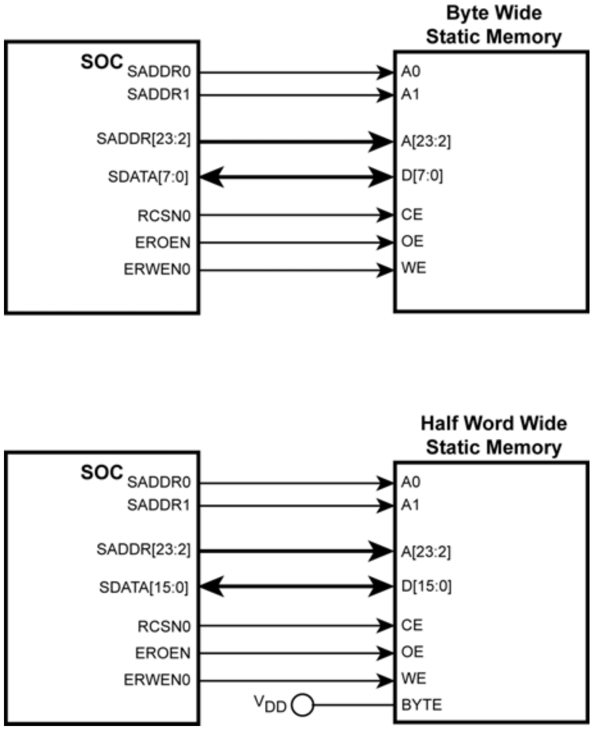

Figure 4. Static Memory Interface Examples

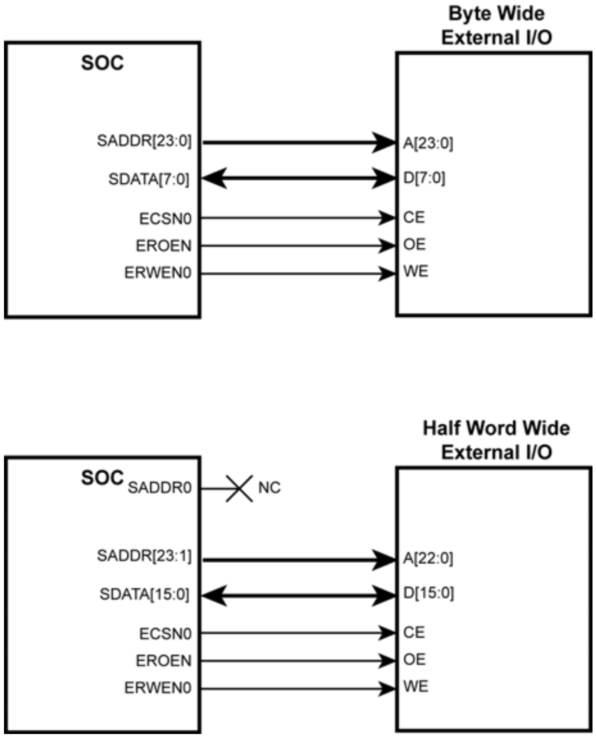

Figure 5. External I/O Interface Examples

NAND Flash Memory Interface

The KSZ9692MPB/KSZ9692XPB NAND controller provides interface to external NAND Flash memory. A total of two banks are supported. NAND Flash bank0 can be configured by power-up strap option to operate as boot bank. Both NAND Flash banks share data bus with FLASH/ROM/SRAM memory banks.

- Glueless connection to two banks with programmable 8 or 16 bit data width and programmable access timing
- Hardware ECC not supported
- Small page size 512 + 16 bytes
- Large page size 2048 + 64 bytes
- Large and small block size
- Boot option with automatic page crossing where pages are automatically opened sequentially by hardware
- Boot option with two 8-bit device in parallel to form a 16-bit bank
- Boot option with bank0 and bank1 as active banks in cascade
- Support for following device densities:
  - 64Mbit
  - 128Mbit
  - 256Mbit
  - 512Mbit
  - 1Gbit
  - 2Gbit
  - 4Gbit
  - 8Gbit

The following figures illustrate examples of NAND Flash bank configuration:

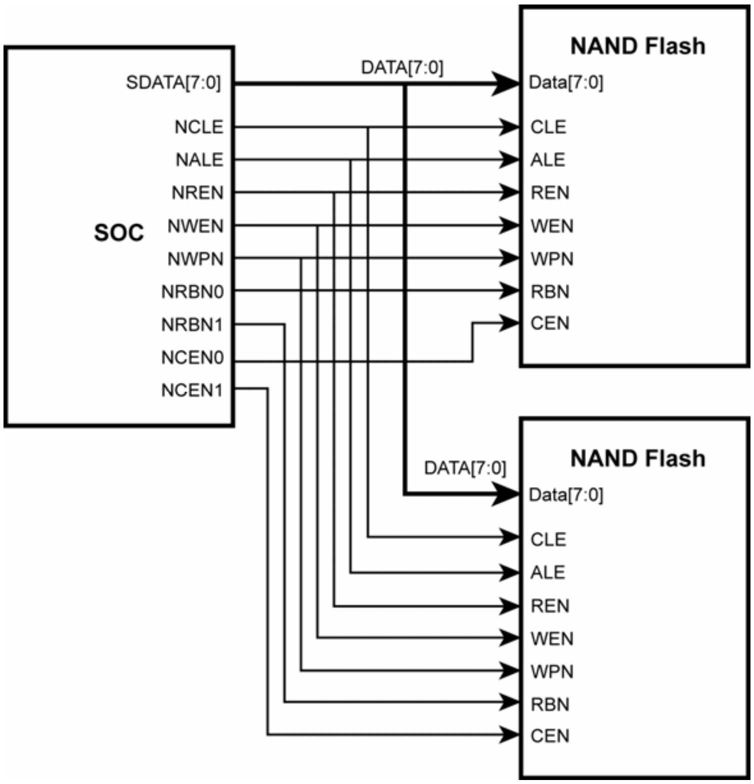

Figure 6. 8-bit NAND Interface Examples

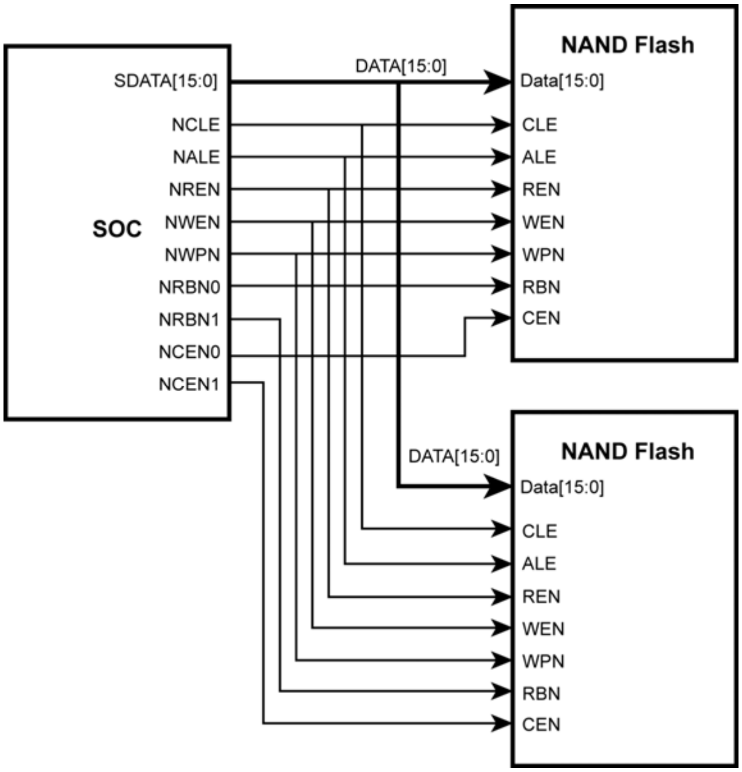

Figure 7. 16-bit NAND Interface Examples

DDR Controller

The KSZ9692MPB/KSZ9692XPB DDR memory controller provides interface for accessing external Double Data Rate Synchronous DRAM. In addition, the KSZ9692MPB/KSZ9692XPB provides two integrated DDR differential clock drivers for a complete glueless DDR interface solution.

- Up to 200 MHz clock frequency (400 MHz data rate)
- Supports one 32-bit data width bank (16-bit optional)
- Up to 128 MB of addressable space is available with 12 columns and 14 row address lines
- Supports all DDR device densities up to 1Gb
- Supports all DDR device data width x8 and x16
- Configurable DDR RAS and CAS timing parameters
- Two integrated JEDEC Specification JESD82-1 compliant differential clock drivers for a glueless DDR interface solution
- JEDEC Specification SSTL_2 I/Os

A dedicated internal PLL provides clocking to the DDR memory controller and the two differential clock drivers. This PLL is programmable up to 200 MHz and independent of AHB and ARM processor core clocks.

Figures 8 and 9 illustrate examples of bank configurations.

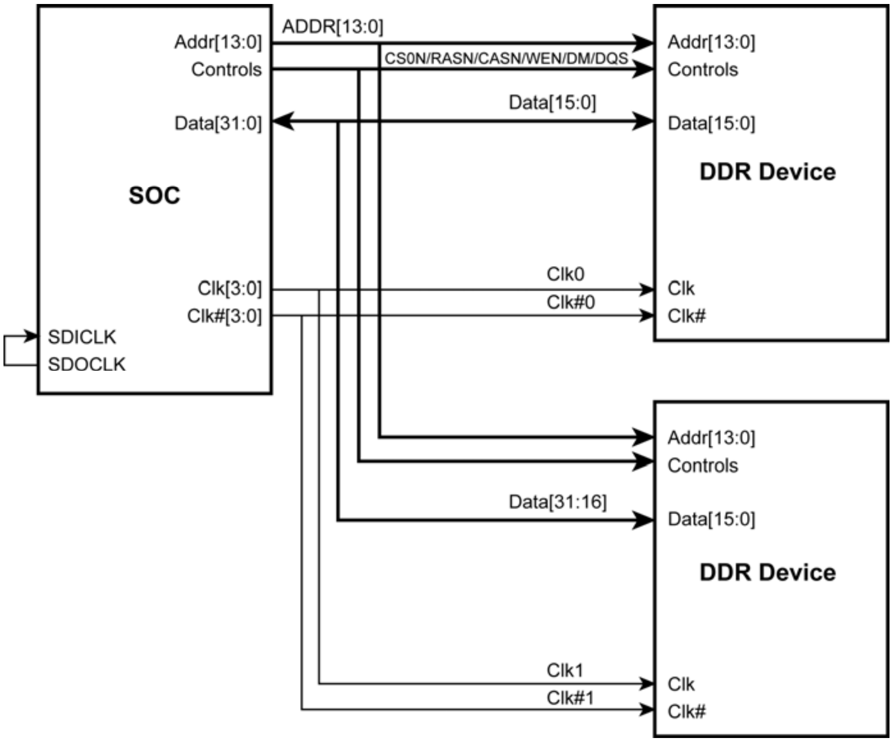

Figure 8. Two 16-bit DDR Memory Device Interface Example

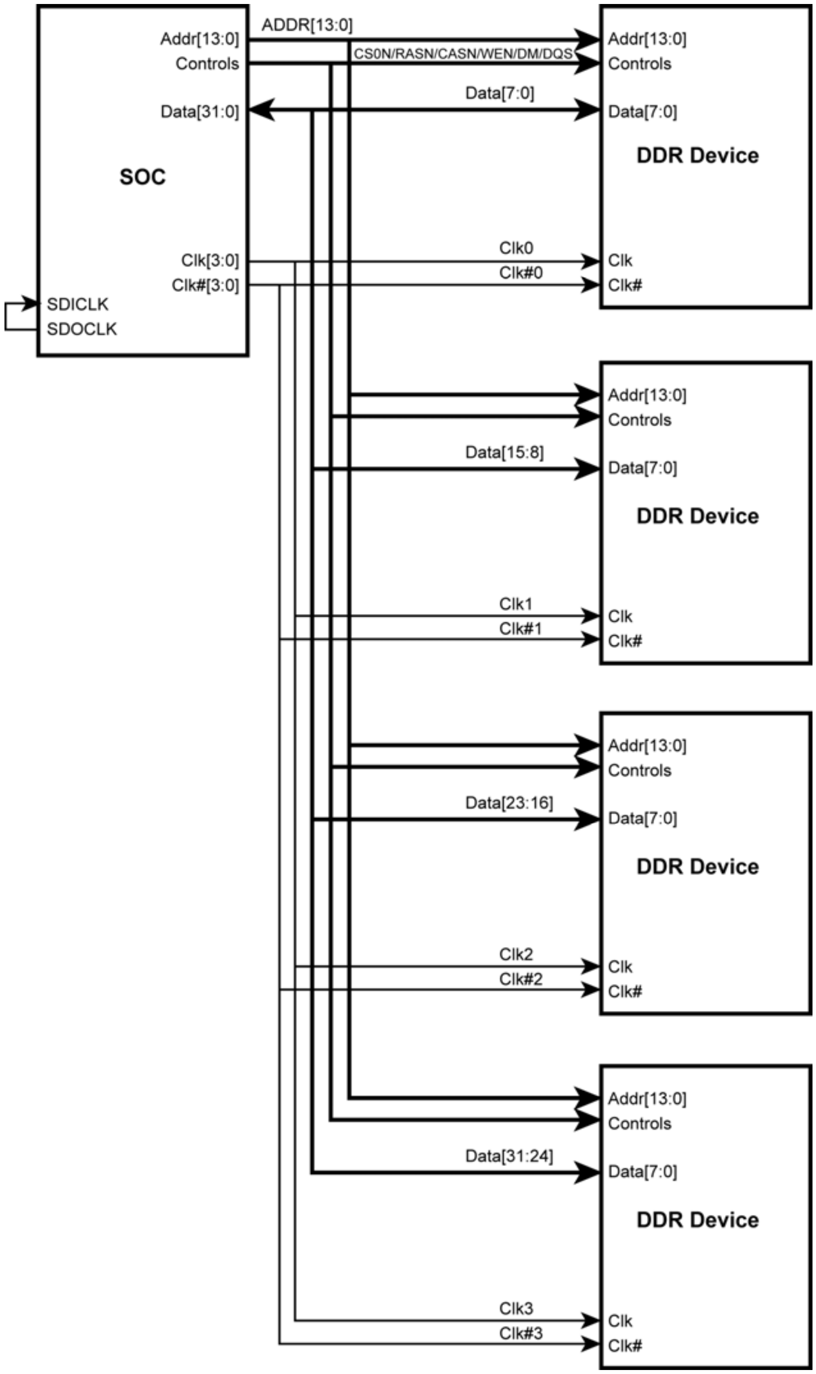

Figure 9. Four8-bit DDR Memory Devices Interface Example

DDR memory controller access to memory bank is typically of the burst type. Figures 10 and 11 are examples of burst read and write cycles.

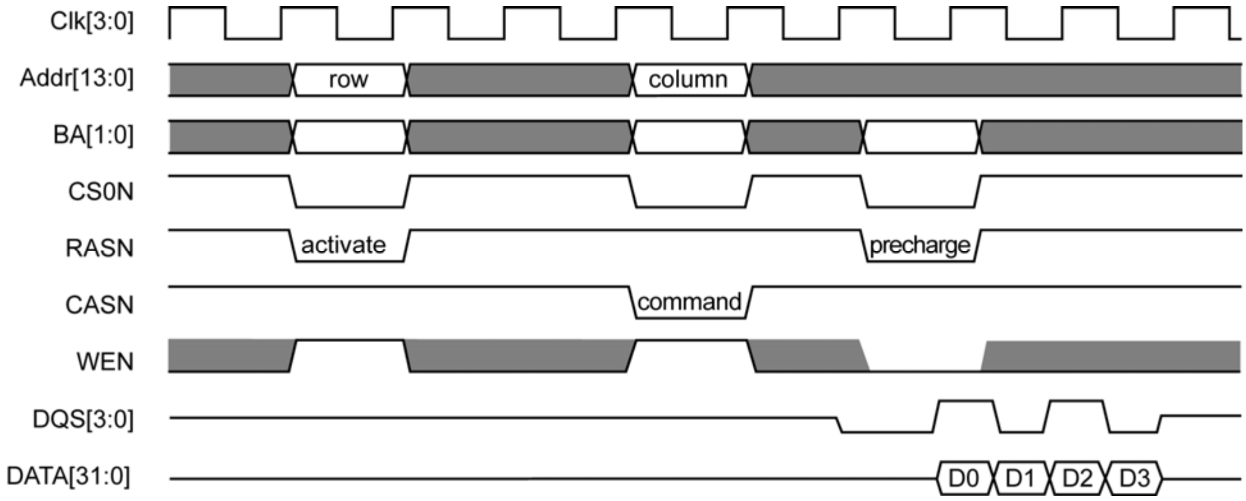

Figure 10. Burst DDR Read Timing

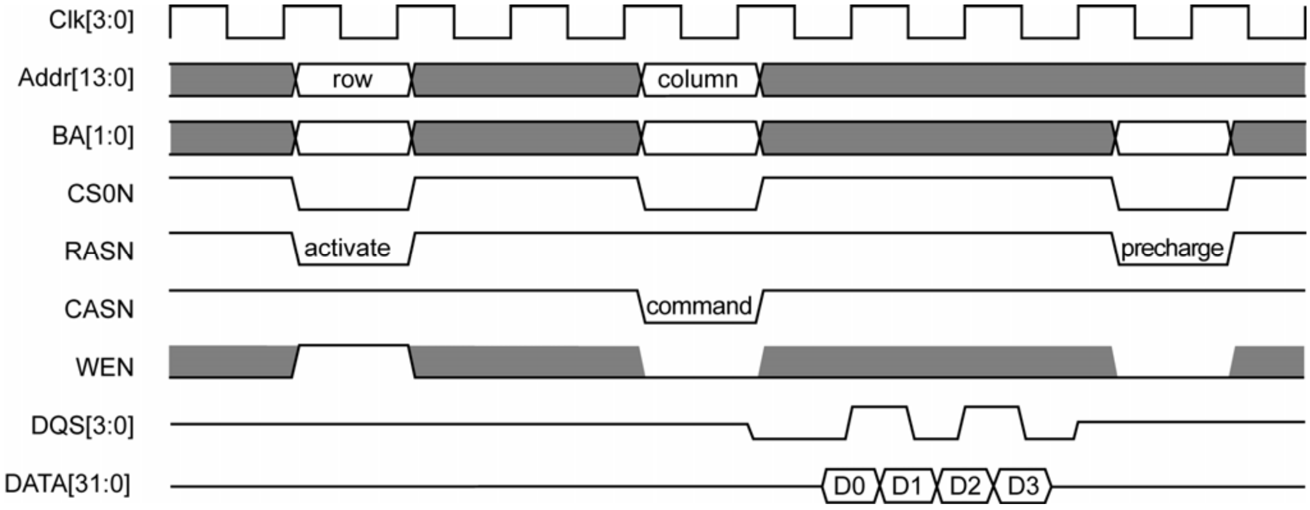

Figure 11. Burst DDR Write Timing

SDIO/SD Host Controller (for KSZ9692MPB only)

Integrated SDIO/SD host controller provides interface for removable mass storage memory card and I/O devices.

- Meets SD Host Controller Standard Specification Version 1.0
- Meets SD memory card spec 1.01. MMC spec 3.31
- Meets SDIO card specification version 1.0
- 1or 4 bit mode supported
- Card detection-insertion/removal
- Line Status LED driver
- Password protection of cards
- Supports read wait control, suspend/resume operation
- Support multi block read and write
- Up to 12.5 Mbytes per second read and write rates using 4 parallel line for full speed card.
- Dedicated DMA or programmed I/O data transfer

USB 2.0 Interface

Integrated dual USB 2.0 interface can be configured as 2-port host, or host + device. Figures 12 and 13 illustrate examples of USB 2.0 interface applications.

- Compliant with USB Specification Revision 2.0
- Compliant with Open Host Controller Interface (OHCI) Specification Rev 1.0a
- Compliant with Enhanced Host Controller Interface (EHCI) Specification Rev 1.0
- Root hub with 2 (max) downstream facing ports which are shared by OHCI and EHCI host controller cores
- All downstream facing ports can handle High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps) transaction
- OTG not supported
- Integrated 45-ohm termination, 1.5K pull-up and 15K pull-down resistors
- Support endpoint zero, and up to 6 configurable endpoints (IN/OUT, isochronous/ control/ interrupt/ bulk)
- One isochronous endpoint (IN or OUT)
- Dedicated DMA Channel for each port

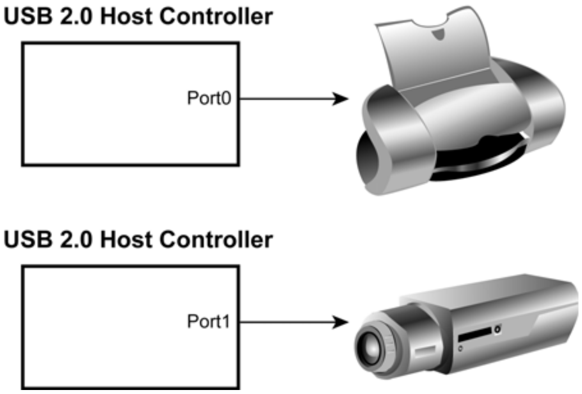

Figure 12. USB 2.0 Configuration as Two-Port Host

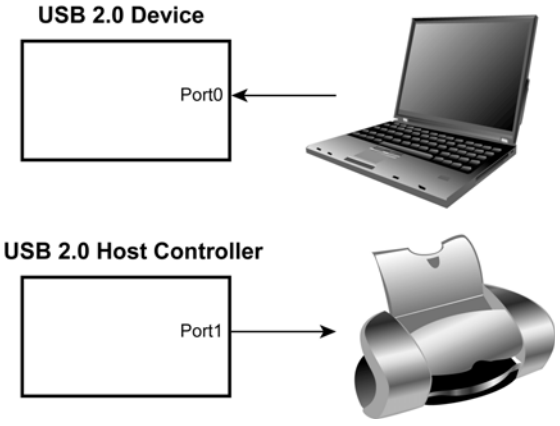

Figure 13. USB 2.0 Configuration as Host + Device

PCI Interface

The KSZ9692MPB/KSZ9692XPB integrates a PCI-to-AHB bridge solution for interfacing with 32-bit PCI, including miniPCI, and cardbus devices where it is common for 802.11x-based Wireless products. The PCI-AHB bridge supports two modes of operation in the PCI bus environment: host bridge mode and guest bridge mode. In the host bridge mode, the ARM processor acts as the host of the entire system. It configures other PCI devices and coordinates their transactions, including initiating transactions between the PCI devices and AHB bus subsystem. An on-chip PCI arbiter is included to determine the PCI bus ownership among up to three PCI master devices.

In guest bridge mode, all of the I/O registers are programmed by either the external host CPU on the PCI bus or the local ARM host processor through the AHB bus and the KSZ9692MPB/KSZ9692XPB can be configured by either the ARM or the PCI host CPU. In guest bridge mode, the on-chip PCI arbiter is disabled. In both cases, the KSZ9692MPB/KSZ9692XPB memory subsystem is accessible from either the PCI host or the ARM processor. Communications between the external host CPU and the ARM processor is accomplished through message passing or through shared memory.

- Compliant to PCI revision 2.3
- Support 33 and 66MHz, 32-bit data PCI bus
- Support 32-bit miniPCI or cardbus devices
- Supports both regular and memory-mapped I/O on the PCI interface
- AHB bus and PCI bus operate at independent clock domains
- Supports big endian and little endian on AHB
- PCI bus Round Robin arbiter for three external masters (for KSZ9692MPB only)
- PCI bus arbiter for one external master (for KSZ9692XPB only)
- Supports high speed bus request and bus parking
- Dedicated DMA channel for bulk data transfer to/from DDR memory

Ethernet MAC Ports (Port 0 = WAN, Port 1 = LAN)

The KSZ9692MPB/KSZ9692XPB integrates two Gigabit Ethernet controllers that operate at 10, 100, and 1000 Mbps. Each controller has an interface that can operate as MII or RGMII to an external 10/100 or 10/100/1000 PHY to complete Ethernet network connectivity. An integrated 25 MHz clock eliminates external crystal or oscillator requirement for PHY to reduce cost. Integrated 2-pin (MDC & MDIO) Station Manager allows ARM processor to access PHY registers and pass control and status parameters. Wake-on-LAN is supported as part of the power management mechanism. Each port has a dedicated MIB counter to accumulate statistics for received and transmitted traffic.

- IEEE 802.3 compliant MAC layer function
- Configurable as MII or RGMII interface
- RGMII interface compliant to Reduced Gigabit Media Independent Interface(RGMII) Version 1.3
- MII interface compliant to Clause 22.2.4.5 of the IEEE 802.3u Specification
- 10/100/1000 Mbps half and full-duplex operation
- Automatic CRC generation and checking
- Automatic error packet discard
- Supports IPv4 Header and IPv4/IPv6 TCP/UDP checksum generation to offload host CPU
- Supports IPv4 Header and IPv4/IPv6 TCP/UDP checksum error detection
- Supports 32 rules ACL filtering
- Maximum frame length support is 2000 Byte at WAN port and 9K-byte at LAN port
- Contains large independent receive and transmit FIFOs (8KB receive / 8KB transmit at WAN and 24KB receive / 22KB transmit at LAN) for back-to-back packet receive, and guaranteed no-under run packet transmit
- Data alignment logic and scatter gather capability
- Configurable as MAC or PHY mode
- Separate transmit and receive DMA channels for each port

Wake-on-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. In all of these instances, the network device is pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic.

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state.

A wake-up signal is caused by:

1. Detection of a change in the network link state
2. Receipt of a network wake-up frame
3. Receipt of a Magic Packet

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own way.

Link Change

Link status wake events are useful to indicate a change in the network's availability, especially when this change may impact the level at which the system should re-enter the sleeping state. For example, a change from link off to link on may trigger the system to re-enter sleep at a higher level (D2 versus D3[1]) so that wake frames can be detected. Conversely, a transition from link on to link off may trigger the system to re-enter sleep at a deeper level (D3 versus D2) since the network is not currently available.

Wake-up Packet

Wake-up packets are certain types of packets with specific CRC values that a system recognizes to as a 'wake up' frame. The KSZ9692MPB/KSZ9692XPB supports up to four user defined wake-up frameon each network control port:

Magic Packet

Magic Packet technology is used to remotely wake up a sleeping or powered off PC or device on anetwork. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC or device capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the networkcontroller, and when the networkcontroller receives a Magic Packet frame, it will alerts the system to wake up.

Magic Packet is a standard feature integrated into the KSZ9692MPB/KSZ9692XPB. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ9692MPB/KSZ9692XPB has been put into Magic Packet Enable mode, it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the networktechnology chosen, such as Source Address (SA), or Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of XoffFFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

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[1] References to D0, D1, D2, and D3 are power management states defined in a similar fashion to the way they are defined for PCI. For more information, refer to the PCI specification at www.pcisig.com/specifications/conventional/pcipm1.2.pdf.

Example:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the networkcontroller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE – MISC - .: FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - MISC - CIRC.

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination.

If the networkcontroller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ9692MPB/KSZ9692XPB controller detects the data sequence, however, it then alerts the device's power management circuitry to wake up the system.

IPv6 Support

The KSZ9692MPB/KSZ9692XPB provides the following IPv6 support in the hardware:

- Generates the checksum for IPv6 TCP/UDP packets based on register configuration (LAN MAC DMA Transmit Control Register and WAN MAC DMA Transmit Control Register) or Transmit Descriptor 1 (TDES1). The register setting is static configuration and the TDES1 setting is packet-based configuration.
- Filters IPv6 packets with TCP/UDP errors (LAN MAC DMA Receive Control Register and WAN MAC DMA Receive Control Register).
- Supports up to 8 Source IP or Destination IP based-filtering (LAN/WAN Access Control List)

Refer to the Register Description Document for more details.

DMA Controller

Integrated DMA controller connects data port of two Gb Ethernet MACs, two USB 2.0 ports, PCI 2.3 bus interface, and SDIO interface (for KSZ9692MPB only) via dedicated channels to DDR memory controller for moving large amounts of data without significant ARM processor intervention. A typical DMA channel usage is to move data from these interfaces into DDR memory. The data in the memory is processed by the ARM processor and driven back by the DMA channel to the external interface. Additionally, the ARM processor itself has a dedicated DMA channel to access the DDR memory controller. Flash/ROM/SRAM, NAND controller, and peripherals do not have dedicated DMA channel and therefore depend on the ARM processor for transfer of data to DDR memory. DMA channel interfaces are shown in functional block diagrams on page 8 and 9.

The arbitration of all requests from DMA channels are handled by the DDR memory controller and pipelined for best performance. The memory controller supports programmable bandwidth allocation for each DMA channel, thus enabling the designer to optimize I/O resource utilization of memory.

UART Interface

The KSZ9692MPB/KSZ9692XPB support four independent high-speed UARTs; UART1, UART2, UART3 and UART4. The UART ports enhance the system availability for legacy serial communication application and console port display.

UART1, UART2, UART3 and UART4 support maximum baud rate of 5 Mbps including standard rates. The higher rates allow for Bluetooth and GSM applications.

UART1 supports CTSN, DSRN, DCDN modem control pins in addition to RXD and TXD data pins. For UART2, UART3, UART4 only CTSN and RTSN control pins in addition to RXD and TXD data pins are supported.

Timers and Watchdog

Two programmable 32-bit timers with one capable of watchdog timer function. These timers can operate in a very flexible way. The host can control the timeout period as well as the pulse duration. Both timers can be enabled with interrupt capability. When the watchdog timer is programmed and the timer setting expires, the KSZ9692MPB/KSZ9692XPB resets itself and also asserts WRSTO to reset other devices in the system.

GPIO

Twenty general purpose I/O (GPIO) are individually programmable as input or output. Some GPIO ports are programmable for alternate function as listed below:

- Four GPIO programmable as inputs for external interrupts
- Two GPIO programmable as 32-bit timers output
- Six GPIO programmable as CTSN and RTSN control pins for UART2, UART3, UART4
- One GPIO programmable as SDIO Line Status LED driver (for KSZ9692MPB only)
- One GPIO programmable as ARM CPU interrupt line activity.

See Signal Description list for detailed GPIO map.

I2C

The I2C interface is a 2-pin (SCL & SDA) generic serial bus interface for both control and data. The KSZ9692MPB/KSZ9692XPB supports master mode I2C interface. To increase the firmware efficiency, KSZ9692MPB/KSZ9692XPB is equipped with hardware assisted logic to take care I2C bus sequence and protocol.

- Supports one master (KSZ9692MPB/KSZ9692XPB) in the system
- 8-bit or 10-bit addressing
- Up to 8 byte burst for read and write
- Programmable SCL clock rate for up to 400kHz

The I2C interface shares the same pins with the SPI interface.

SPI

The Serial Peripheral Interface (SPI) is a synchronous serial data link that provides communication with external devices.

- 8- to 16-bit Programmable Data Length
- Programmable Serial Clock Phase and Polarity
- Programmable Active Level of Chip Select (CS)
- Programmable Delays between Two Active CS
- Programmable Delays between Consecutive Transfers without Removing CS
- Programmable Delays between Assertion CS and 1st SPCK
- Programmable SPI clock (SPCK) rate in the range of AMBA System Clock (SYSCLK) divided by a value between 16 and 65536

The SPI interface shares the same pins with the I2C interface.

I2S

I2S provides programmable 16-, 18-, 20-, 24-bit resolution audio for two (stereo) channels playback and recording.

Interrupt Controller

Interrupt controller handles external and internal interrupt sources.

- Normal or fast interrupt mode (IRQ, FIQ) supported
- Prioritized interrupt handling

System Level Interfaces

The following figures illustrate the high-level system connections to the KSZ9692MPB/KSZ9692XPB. Note that these figures are for illustration purpose only. The system designer must refer to Evaluation Design Kit for actual circuit implementation.

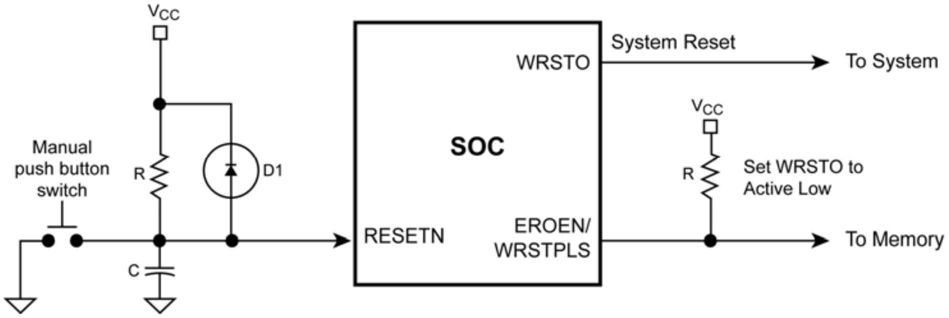


Figure 14. Reset Circuit

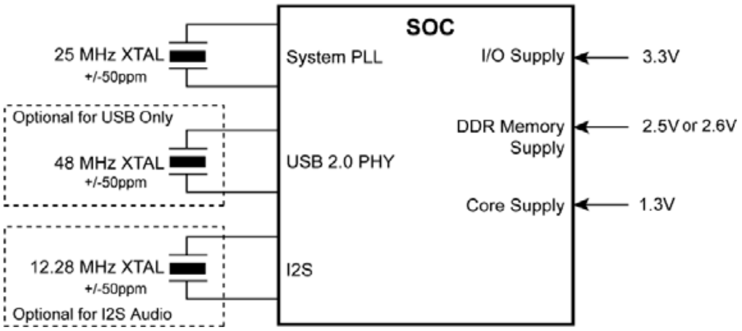


Figure 15. Power and Clocks

According to some DDR device manufacturer's electrical specification, DDR400 devices operating at 200 MHz require a 2.6V power supply. DDR333 and DDR266 devices require 2.5V power supply. Power to the SoC DDR Memory Controller must be based on DDR device power requirement specification.

Signal Descriptions by Group

Pin Number	Pin Name	Pin Type	Pin Description
System Interface			
R5	RESETN	I	Reset, asserted Low. RESETN will force the KSZ9692MPB/KSZ9692XPB to reset ARM9 CPU and all functional blocks. Once asserted, RESETN must remain asserted for a minimum duration of 256 system clock cycles. When in the reset state, all the output pins are put into Tri-state and all open drain signals are floated.
N5	WRSTO	O	Watchdog Timer Reset Output When the Watchdog Timer expires, this signal will be asserted for at least 200 msec.
W1	XCLK2	I	System Clock Input 2. External crystal or clock input 2. The clock frequency should be 25MHz ± 100ppm.
Y1	XCLK1	I	System Clock Input 1. Used with XCLK1 pin when other polarity of crystal is needed. This is unused for a normal clock input.
H19	CLK25MHz	O	25MHz output to external PHY
Y15, Y14	DDCLKO[1:0]	O	DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
W15, W14	DDCLKON[1:0]	O	The negative of differential pair of DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
U13	SDCLKEO	O	Clock Enable output for SDRAM (for Power Down Mode)
T7, U7	VREF	I	Reference Voltage for SSTL interface. Must be half of the voltage for the DDR VDD supply. See EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5V, SSTL_2)
W3	SDOCLK	O	DDR Clock Out for loopback from De-skew PLL
Y3	SDICLK	I	DDR Clock In from loopback to De-skew PLL. This pin must connect to SDOCLK with appropriate de-skew length. See Engineering Evaluation Design Kit for detailed implementation.
Y17, Y16	DDCLKO[3:2]	O	Factory Reserved
W17, W16	DDCLKON[3:2]	O	Factory Reserved
NAND/SRAM/ROM/EXIO Interface			
L2, K1, K2, J3, H5, H4, J2, H3, J1, H2, G5, H1, G3, G4, G2, F1, G1, F2, F3, F5, F4, E1, E2, E3	SADDR[23..0]	O	SRAM Address Bus. The 24-bit address bus covers 16M word memory space of ROM/SRAM/FLASH, and 16M byte external I/O banks. This address bus is shared between ROM/SRAM/FLASH/EXTIO devices.

Pin Number	Pin Name	Pin Type	Pin Description
T2, U1, L5, N4, P3, R2, T1, M4, K5, N3, P2, R1, L4, M3, P1, K4	SDATA[15..0]	Ipu/O	SRAM DATA Bus. Bidirectional Bus for 16-bit DATA In and DATA Out. The KSZ9692MPB/KSZ9692XPB also supports 8-bit data bus for ROM/SRAM/FLASH/EXTIO cycles. This data bus is shared between NAND, ROM/SRAM/FLASH/EXTIO devices.
L3	ECS2	O	External I/O Chip Select 2, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
N1	ECS1	O	External I/O Chip Select 1, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
M2	ECS0	O	External I/O Chip Select 0, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
K3	RCSN1	O	ROM/SRAM/FLASH(NOR) Chip select 1, asserted Low. The KSZ9692MPB/KSZ9692XPB can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks.
L1	RCSN0	O	ROM/SRAM/FLASH(NOR) Chip select 0, asserted Low. The KSZ9692MPB/KSZ9692XPB can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks. This bank is configurable as boot option
N2	EWAITN	I	External Wait asserted Low. This signal is asserted when an external I/O device or ROM/SRAM/FLASH(NOR) bank needs more access cycles than those defined in the corresponding control register.
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device.
J5	ERWEN1	O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[15..8] for ROM/SRAM/FLASH and EXTIO access.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[7..0 or 15..0] for ROM/SRAM/FLASH and EXTIO access.
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash.
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash.
T3	NCEN1	O	NAND Bank Chip Enable 1, asserted low NAND device bank 1 selection control.
V3	NCEN0	O	NAND Bank Chip Enable 0, asserted low NAND device bank 0 selection control. This bank is configurable as boot option

Pin Number	Pin Name	Pin Type	Pin Description
R4	NREN	Ipu/O	NAND Read Enable, asserted low.
T4	NWEN	Ipu/O	NAND Write Enable, asserted low.
U3	NWPN	Ipu/O	NAND Write Protection, asserted low.
P4, U4	NRBN[1:0]	I	NAND Ready/Busy, asserted low for busy.
DDR Interface			
T17, V18, U17, T16, W20, W19, Y20, Y19, W18, V17, U16, T15, Y18, V16	DADD[13..0]	O	DDR Address Bus.
V13, U11, V12, W13, Y13, W12, V11, U10, V10, Y11, W10, U9, Y10, V9, W9, Y9, W8, Y8, Y7, W7, V7, Y6, W6, V6, Y5, V5, W5, U5, T5, Y4, V4, W4	DDATA[31..0]	I/O	DDR Data Bus.
T13, V14	BA[1:0]	O	DDR Bank Address.
U14	CSN	O	DDR Chip Select, asserted Low. Chip select pins for DDR, the KSZ9692MPB/KSZ9692XPB supports only one DDR bank.
T14	RASN	O	DDR Row Address Strobe, asserted Low. The Row Address Strobe pin for DDR.
U15	CASN	O	DDR Column Address Strobe, asserted Low. The Column Address Strobe pin for DDR.
V15	WEN	O	DDR Write Enable, asserted Low. The write enable signal for DDR.
U8, T6	DM[1:0]	O	DDR Data Input/Output Mask Data Input/Output mask signals for DDR. DM is sampled High and is an output mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a Write cycle. DM0 corresponds to DDATA[7:0], DM1 corresponds to DDATA[15:8].
V8, U6	DQS[1:0]	I/O	DDR only Data Strobe Input with read data, output with write data. DQS0 corresponds to DDATA[7:0], DQS1 corresponds to DDATA[15:8].

Pin Number	Pin Name	Pin Type	Pin Description
Ethernet Port 0			
M16	P0_RXC	Ipd/O	MAC mode MII: input RX clock / PHY mode MII: output RX clock RGMII mode: input RX clock
P18, N17, P17, N16	P0_RXD[3:0]	I	RX data[3:0]
N18	P0_RXDV	I	MII mode: RX data valid RGMII mode: as RX_CTL. RXDV on rising edge of RXC, logic derivative of RXDV and RXER on falling edge of RXC
P19	P0_RXER	I	MII mode: RX error RGMII mode: input SEL
M17	P0_CRS	I	MAC mode MII: input carrier sense RGMII mode: not used
P20	P0_COL	I	MAC mode MII: input collision RGMII mode: not used
M18	P0_TXC	Ipd/O	MAC mode MII: input TX clock / PHY mode MII: output TX clock RGMII mode: output TX clock
L17, M19, N20, N19	P0_TXD[3:0]	O	TX data[3:0]
L16	P0_TXEN	O	MII: TX enable RGMII: as TX_CTL input. TXEN on rising edge of TXC, logic derivative of TXEN and TXER on falling edge of TXC.
Ethernet Port 1			
K19	P1_RXC	Ipd/O	MAC mode MII: input RX clock / PHY mode MII: output RX clock RGMII mode: input RX clock
L20, L19, L18, M20	P1_RXD[3:0]	I	RX data[3:0]
K16	P1_RXDV	I	MII mode: RX data valid RGMII mode: as RX_CTL. RXDV on rising edge of RXC, logic derivative of RXDV and RXER on falling edge of RXC
K17	P1_RXER	I	MII mode: RX error RGMII mode: input SEL
K18	P1_CRS	I	MAC mode MII: input carrier sense RGMII mode: not used
K20	P1_COL	I	MAC mode MII: input collision RGMII mode: not used
J17	P1_TXC	Ipd/O	MAC mode MII: input TX clock / PHY mode MII: output TX clock RGMII mode: output TX clock
H20, J19, J18, J20	P1_TXD[3:0]	O	TX data[3:0] output.
J16	P1_TXEN	O	MII: TX enable RGMII: as TX_CTL input. TXEN on rising edge of TXC, logic derivative of TXEN and TXER on falling edge of TXC.

Pin Number	Pin Name	Pin Type	Pin Description
USB Interface			
G19	U1P	I/O (analog)	USB port 1 differential + signal
G20	U1M	I/O (analog)	USB port 1 differential - signal
F19	U2P	I/O (analog)	USB port 2 differential + signal
F20	U2M	I/O (analog)	USB port 2 differential - signal
G17	USBXI	I (analog)	Crystal in for USB PLL
G18	USBXO	O (analog)	Crystal out for USB PLL
H16	USBREXT	I (analog)	Connect to an external resistor 3.4K ohm to GND
G16	USBTEST	O (Analog)	USB analog test output (factory reserved)
G15	USBCFG	I	USB port 2 configuration “1” = port 2 is host “0” = port 2 is device (port 1 is always host)
F18	USBHOVC0	I	Over current sensing input for Host Controller downstream port 1
F15	USBHOVC1	I	Over current sensing input for Host Controller downstream port 2
F17	USBHPWR0	Ipu/O (open drain)	Power switching control output for downstream port 1; open drain output
F16	USBHPWR1	Ipu/O (open drain)	Power switching control output for downstream port 2; open drain output
SDIO Interface (for KSZ9692MPB only)			
D14	KCMD	Ipd/O	SD 4-bit mode: Command line SD 1-bit mode: Command line
C18	KCLK	Ipd/O	SDIO/SD Clock
C15	KDATA3	I/O	SD 4-bit mode : data line 3 SD 1-bit mode : not used
C16	KDATA2	I/O	SD 4-bit mode : data line 2 or read wait (optional) SD 1-bit mode : read wait (optional)
E13	KDATA1	I/O	SD 4-bit mode : data line 1 or interrupt (optional) SD 1-bit mode : interrupt
C17	KDATA0	I/O	SD 4-bit mode : data line 0 SD 1-bit mode : data line
C14	KSDCDN	I	Active low used for Card Detection
D13	KSDWP	I	Active high used for Card write protection
General Purpose I/O			
B14	SLED/GPIO[19]	I/O	SDIO Line Status LED output (for KSZ9692MPB only) or General Purpose I/O Pin[19]
B15	CPUINTN/ GPIO[18]	I/O	Internal CPU interrupt request or General Purpose I/O Pin[18] As CPUINTN, any interrupt generated to ARM CPU asserts logic low on this pin. Useful for software development.
B16, B17, B18, D18, E15, D19	GPIO[17:12]	I/O	General Purpose I/O Pin[17:12]
F14	UART 4 RTSN /GPIO[11]	I/O	UART 4 RTS or general purpose I/O Pin[11]

Pin Number	Pin Name	Pin Type	Pin Description
E16	UART 4 CTSN /GPIO[10]	I/O	UART 4 CTS or general purpose I/O Pin[10]
E17	UART 3 RTSN /GPIO[9]	I/O	UART 3 RTS or general purpose I/O Pin[9]
E19	UART 3 CTSN /GPIO[8]	I/O	UART 3 CTS or general purpose I/O Pin[8]
E20	UART 2 RTSN /GPIO[7]	I/O	UART 2 RTS or general purpose I/O Pin[7]
E18	UART 2 CTSN /GPIO[6]	I/O	UART 2 CTS or general purpose I/O Pin[6]
U20, U19	TOUT[1:0]/ GPIO[5:4]	I/O	Timer 1/0 out or General Purpose I/O Pin[5:4]
V20, T18, V19, U18	EINT[3:0]/ GPIO[3:0]	I/O	External Interrupt Request or General Purpose I/O Pin[3:0]
I2S Interface			
C20	SCKIN	I	External crystal or clock input for I2S clock The maximum supported frequency is 49.2 MHz
D20	SCKOUT	O	External Crystal out for I2S clock
C19	I2S_MCLK	O	I2S master clock out This clock is of same frequency as SCKIN
B20	I2S_BCLK	O	I2S bit clock out
B19	I2S_LRCLK	O	Left/right select
A19	I2S_SDO	O	Serial data out
A20	I2S_SDI	I	Serial data in
MDIO/MDC Interface			
H18	MDC	Ipu/O	Clock for station management
H17	MDIO	Ipu/O	Serial data for station management
I2C/SPI Interface			
E14	SPCK_SCL	Ipu/O	SPI mode: master clock output I2C mode: serial clock output
D17	SPMOSI_SDA	Ipu/O	SPI mode: master data out,slave data in I2C mode: serial data
D16	SPMISO	I	SPI master data in, slave data out
D15	SPICS	Ipu/O	SPI chip select
F13	SPI_RDY	I	Micrel SPI mode ready signal
PCI Interface Signals			
C3	PRSTN	I	PCI Reset, asserted Low In Host Bridge Mode, the PCI Reset pin is an input. This pin as well as the reset pin of all the devices on the PCI bus could be driven by WRSTO. In Guest Bridge Mode, this pin is input. The system reset to drive this pin.
B2	PCLK	I	PCI Bus Clock input. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz, or 66MHz.

Pin Number	Pin Name	Pin Type	Pin Description
E4	GNT3N	O	PCI Bus Grant 3 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ3N. In Guest Bridge Mode, this is unused. (No connect for KSZ9692XPB)
D4	GNT2N	O	PCI Bus Grant 2 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ2N. In Guest Bridge Mode, this is unused. (No connect for KSZ9692XPB)
B1	GNT1N	O	PCI Bus Grant 1 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ1N. In Guest Bridge Mode, this is an output signal to indicate to the external PCI bus arbiter that KSZ9692MPB/KSZ9692XPB is requesting access to the PCI bus.
D3	REQ3N	I	PCI Bus Request 3 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this is unused. (No connect for KSZ9692XPB)
E6	REQ2N	I	PCI Bus Request 2 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this is unused. (No connect for KSZ9692XPB)
C1	REQ1N	I	PCI Bus Request 1 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this signal comes from the external arbiter to indicate that the bus is granted to KSZ9692MPB/KSZ9692XPB.
B3, E7, D6, A2, B4, A3, D7, C5, C6, B5, A4, A5, B6, E8, C7, D8, D10, B10, A11, B11, C11, A12, E11, D11, B12, A13, C12, B13, F12, C13, D12, E12	PAD[31..0]	I/O	32-bit PCI address and data lines Addresses and data bits are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the PAD bus contains the first clock cycle of a PCI transaction, the PAD bus contains the physical address. During subsequent clock cycles, these lines contain the 32-bit data to be transferred. Depending on the type of the transaction, the source of the data will be the KSZ9692MPB/KSZ9692XPB if it initiates a PCI write transaction, or the data source will be the target if it is a PCI Read transaction. The KSZ9692MPB/KSZ9692XPB bus transaction consists of an address phase followed by one or more data phases. The KSZ9692MPB/KSZ9692XPB supports both Read and Write burst transactions. In case of a Read transaction, a special data turn around cycle is needed between the address phase and the data phase.

Pin Number	Pin Name	Pin Type	Pin Description
A6, A7, E10, C10	CBEN[3..0]	I/O	PCI Commands and Byte Enable, asserted Low. The PCI command and byte enable signals are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the CBEN bus contains the command for the transaction. The PCI transaction consists of the address phases and one or more data phases. During the data phases of the transaction, the bus carries the byte enable for the current data phases.
C8	PAR	I/O	Parity PCI Bus parity is even across PAD[31:0] and CBEN[3:0]. The KSZ9692MPB/KSZ9692XPB generates PAR during the address phase and write data phases as a bus master, and during read data phases as a target. It checks for correct PAR during read data phase as a bus master, during every address phase as a bus slave, and during write data phases as a target.
D9	FRAMEN	I/O	PCI Bus Frame signal, asserted Low. FRAMEN is an indication of an active PCI bus cycle. It is asserted at the beginning of a PCI transaction, i.e. the address phase, and de-asserted before the final transfer of the data phase of the transaction.
B8	IRDYN	I/O	PCI Initiator Ready signal, asserted Low. This signal is asserted by a PCI master to indicate a valid data phase on the PAD bus during data phases of a write transaction. In a read transaction, it indicates that the master is ready to accept data from the target. A target will monitor the IRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together.
E9	TRDYN	I/O	PCI Target Ready signal, asserted Low. This signal is asserted by a PCI slave to indicate a valid data phase on the PAD bus during data phases of a read transaction. In a write transaction, it indicates that the slave is ready to accept data from the target. A PCI initiator will monitor the TRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together.
A9	DEVSELN	I/O	PCI Device Select signal, asserted Low. This signal is asserted when the KSZ9692MPB/KSZ9692XPB is selected as a target during a bus transaction. When the KSZ9692MPB/KSZ9692XPB is the initiator of the current bus access, it expects the target to assert DEVSELN within 5 PCI bus cycles, confirming the access. If the target does not assert DEVSELN within the required bus cycles, the KSZ9692MPB/KSZ9692XPB aborts the bus cycle. As a target, the KSZ9692MPB/KSZ9692XPB asserts this signal in a medium speed decode timing. (2 bus cycle)
B7	IDSEL	I	Initialization Device Select. It is used as a chip select during configuration read and write transactions.
B9	STOPN	I/O	PCI Stop signal, asserted Low. This signal is asserted by the PCI target to indicate to the bus master that it is terminating the current transaction. The KSZ9692MPB/KSZ9692XPB responds to the assertion of STOPN when it is the bus master, either to disconnect, retry, or abort.

Pin Number	Pin Name	Pin Type	Pin Description
A10	PERRN	I/O	PCI Parity Error signal, asserted Low. The KSZ9692MPB/KSZ9692XPB asserts PERRN when it checks and detects a bus parity error. When it generates the PAR output, the KSZ9692MPB/KSZ9692XPB monitors for any reported parity error on PERRN. When the KSZ9692MPB/KSZ9692XPB is the bus master and a parity error is detected, the KSZ9692MPB/KSZ9692XPB sets error bits on the control status registers. It completes the current data burst transaction, then stop the operation. After the Host clears the system error, the KSZ9692MPB/KSZ9692XPB continues its operation.
C9	SERRN	O(open drain)	PCI System Error signal, asserted Low. If an address parity error is detected, the KSZ9692MPB/KSZ9692XPB asserts the SERRN signal two clocks after the failing address.
C4	M66EN	I	PCI 66MHz Enable When asserted, this signal indicates the PCI Bus segment is operating at 66 MHz. This pin is mainly used in Guest bridge mode when the PCLK is driven by the Host bridge.
F6	PCLKOUT3	O	PCI Clock output 3 (No connect for KSZ9692XPB)
D1	PCLKOUT2	O	PCI Clock output 2 (No connect for KSZ9692XPB)
D2	PCLKOUT1	O	PCI Clock output 1
E5	PCLKOUT0	O	PCI Clock output 0. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz, or 66MHz. In Host Bridge Mode, this is an output signal for all the devices on the PCI bus to sample data and control signals. Connect this clock to drive PCLK input. In Guest Bridge Mode, this is not used.
A8	CLKRUNN	I/O	This is a CardBus only signal. The CLKRUNN signal is used by portable CardBus devices to request the system to turn on the bus clock. Output is not generated.
C2	MPCIACTN	I/O	Mini-PCI active. This signal is asserted by the PCI device to indicate that its current function requires full system performance. MPCIACTN is an open drain output signal.
D5	PBMS	I	PCI Bridge Mode Select Select the operating mode of the PCI Bridge. When PBMS is High, the Host Bridge Mode is selected and on chip PCI bus arbiter is enabled. When PBMS is Low, the Guest Bridge Mode is selected and the on-chip arbiter is disabled.
A1	PMEN	O (open drain)	PCI Power Management Enable (active low) This pin is to inform the external PCI host that KSZ9692MPB/KSZ9692XPB has detected a wake-up event.

Pin Number	Pin Name	Pin Type	Pin Description
UART Signals			
P16	U1RXD	Ipd	UART 1 Receive Data
R16	U1TXD	O (Tri-State)	UART 1Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
R19	U1CTSN	Ipd	UART 1Clear to Send
R20	U1DCDN	Ipd	UART 1 Data Carrier Detect
P15	U1DSRN	Ipd	UART 1 Data Set Ready
R15	U2RXD	Ipd	UART 2 Receive Data
R17	U2TXD	O (Tri-State)	UART 2 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
R18	U3RXD	Ipd	UART 3 Receive Data
N15	U3TXD	O (Tri-State)	UART 3 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
T19	U4RXD	Ipd	UART 4 Receive Data
T20	U4TXD	O (Tri-State)	UART 4 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
TAP Control Signals			
A18	TCK	I	JTAG Test Clock
A17	TMS	I	JTAG Test Mode Select
A16	TDI	I	JTAG Test Data In
A15	TDO	O	JTAG Test Data Out
A14	TRSTN	I	JTAG Test Reset, asserted Low
Test Signals			
P5	SCANEN	Ipd	1 = Scan Enable (Factory reserved) 0 = Normal Operation
V2	TESTEN	Ipd	1 = Test Enable (Factory reserved) 0 = Normal Operation
V1	TESTEN1	Ipd	1 = Test Enable1 (Factory reserved) 0 = Normal Operation
Y2	TEST1	O (analog)	Factory reserved
W2	TEST2	O (analog)	Factory reserved
Power and Ground (96)			
N6, M6, M7, G7, G8, G9, M14, M15, N14, P11, P12, P13, P14	VDD1.2	P	Digital power supply 1.3V (13)

Pin Number	Pin Name	Pin Type	Pin Description
G6, H6, J6, K6, F7, F8, F9, F10, F11, G10, G11, H14, J14, K14, K15, L15	VDD3.3	P	Digital power supply 3.3V (16)
R6, R7, R8, R9, R10, R11, R12, R13, R14, T8, T9, T10, T11	VDD2.5	P	DDR Pad Driver 2.5V or 2.6V Power Supply. (13)
H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, K12, L7, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, N9, N10, N11, N12, N13, P7, P8, P9, P10	GND	GROUND	Digital Ground. (37)
L6	PLLVDDA3.3	P	Band Gap Reference Analog Power. (1)
M8	PLLVSSA3.3	GROUND	Band Gap Reference Analog Ground. (1)
P6	PLLDVDD1.2	P	De-skew PLL Analog and Digital Power. (1)
M5	PLLSVDD1.2	P	System PLL Analog and Digital Power. (1)
N7, N8	PLLVSS1.2	GROUND	De-skew PLL and System PLL Ground. (2)
L8	PLLVSSISO	GROUND	Ground Isolation PLL and other circuit. (1)
G12	USB1VDDA3.3	P	Analog Power for USB Channel 1. (1)
G13	USBCVDDA3.3	P	Analog Power for Common Circuit of USB Channel 1 and 2. (1)
G14	USB2VDDA3.3	P	Analog Power for USB Channel 2. (1)
H13, J13, K13	USBVSSA3.3	GROUND	Analog Ground for both USB Channels Analog Circuit. (3)
J15	USB1VDD1.2	P	Digital Power for USB Channel 1 Controller. (1)
H15	USB2VDD1.2	P	Digital Power for USB Channel 2 Controller. (1)
J12	USBVSS1	GROUND	Digital Ground for USB Channel 1 Controller. (1)
H12	USBVSS2	GROUND	Digital Ground for USB Channel 2 Controller. (1)

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   O/I = Output in normal mode; input pin during reset.
   Ipu = Internal 55kΩ pull-up resistor.
   Ipd = Internal 55kΩ pull-down resistor.

Power-up Strapping Options

Certain pins are sampled upon power up or reset to initialize KSZ9692MPB/KSZ9692XPB system registers per system configuration requirements.

Pin Number	Pin Name	Pin Type	Pin Description
E3	SADDR[0]	Ipd/O	During reset, this pin is the input strap option for NAND Boot small page size 0 = 512 Bytes (default) 1 = 528 Bytes
E1, E2	SADDR[2:1]	Ipd/O	During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [7:6]. These pins are used to specify number of active banks (CE#) in cascade. 00 = 1 bank (default) 01 = 2 banks
F4	SADDR[3]	Ipd/O	During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [8], NAND Flash type. This pin is used to specify using large or small block NAND Flash as a boot bank as follows: “0” = small block (default) “1” = large block
F5	SADDR[4]	Ipd/O	During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [4], NAND Flash type. This pin is used to specify number of NAND Flash in parallel for combined data width as follows: “0” = 1 NAND Flash (default) “1” = 2 NAND Flash
F3	SADDR[5]	Ipu/O	During reset, this is the input strap option to enter ARM9 tic test mode 0: ARM tic test mode (factory reserved) 1: Normal mode (default)
F2	SADDR[6]	Ipd/O	During reset, this pin is the input strap option for NAND FLASH device support automatic page crossing 0: NAND FLASH device does not support automatic page crossing (default) 1: NAND FLASH device supports automatic page crossing
G1	SADDR[7]	Ipd/O	During reset, this pin is a strapping option for B0SIZE, Bank 0 Data Access Size. This is applicable to ROM/SRAM/FLASH and NAND boot bank. Bank 0 is used for boot program. This pin is used to specify the size of the bank 0 data bus width as follow: “0” = one byte (default) “1” = half word
F1	SADDR[8]	Ipd/O	During reset, this pin is a strapping option for BTSEL: “0” = Boot select from NOR flash (default) “1” = Boot select from NAND flash
G2	SADDR[9]	Ipd/O	During reset this pin is a strapping option for BYP_SYSPLL: “0” = Use systems PLL (default) “1” = Bypass systems PLL, use external clock (factory reserved)
G4	SADDR[10]	Ipd/O	During reset this pin is a strapping option for BYP_CLKSEL: “0” = Select 200MHz external clock (default) “1” = Select 250MHz external clock (factory reserved)

Pin Number	Pin Name	Pin Type	Pin Description
G3	SADDR[11]	Ipd/O	During reset, this pin is the input strap option to enable either MII or RGMII mode at port1 (LAN port) 0: MII mode (default) 1: RGMII mode
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device. During reset, this pin is used for Watchdog Timer Reset Polarity Select. This is a power strapping option pin for watchdog reset output polarity. “0” = WRSTO is selected as active high (default) “1” = WRSTO is selected as active low. This pin is shared with the EROEN pin.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, these signals control the byte write enable of the memory device for ROM/SRAM/FLASH and EXTIO access. During ARM tic test mode, this pin is TESTACK. During reset, this pin is the input strap option to enable either MII or RGMII mode at port0 (WAN port) 0: MII mode (default) 1: RGMII mode
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash. During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [2]. This bit along with configuration register bits [1:0] is used for boot program. This pin along with NALE and NWEN is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit

Pin Number	Pin Name	Pin Type	Pin Description
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash. During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [1]. This bit along with configuration register bits [2], [0] is used for boot program. This pin along with NCLE and NWEN is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit
T4	NWEN	Ipu/O	NAND Write Enable, asserted low During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [0]. This bit along with configuration register bits [2:1] is used for boot program. This pin along with NCLE and NALE is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit
U3	NWPN	Ipu/O	NAND Write Protection, asserted low During reset, this pin is the input strap option to enable test modes. This pin along with TESTEN, TESTEN1 form different test modes. {TESTEN, TESTEN1, NWPN} = 011: ARM Scan test mode 010: USB Analog Bits test mode others: refer to TESTEN and TESTEN1 pin description (factory reserved)
G15	USBCFG	I	USB port 2 configuration “1” = port 2 is host “0” = port 2 is device (port 1 is always host)

Pin Number	Pin Name	Pin Type	Pin Description
Test Pins Strapping Options			
P5	SCANEN	Ipd	1 = Scan Enable (Factory reserved) 0 = Normal Operation
V2	TESTEN	Ipd	1 = Test Enable (Factory reserved) 0 = Normal Operation
V1	TESTEN1	Ipd	1 = Test Enable1 (Factory reserved) 0 = Normal Operation

Notes:

1. P = Power supply.
   I = Input. O = Output.
   O/I = Output in normal mode; input pin during reset.
   Ipu = Internal 55kΩ pull-up resistor.
   Ipd = Internal 55kΩ pull-down resistor.

Absolute Maximum Ratings[1]

Supply Voltage	
(V_{DD}1.2, PLLDV$_{DD}$1.2, PLLSV$_{DD}$1.2, USB1V$_{DD}$1.2, USB2V$_{DD}$1.2)	–0.5V to +1.6V
V_{DD}2.5	–0.5V to +3.0V
(V_{DD}3.3, PLLV$_{DD}$A3.3, PLLDV$_{DD}$3.3, USB1V$_{DD}$A3.3, USB2V$_{DD}$A3.3, USBCV$_{DD}$A3.3)	–0.5V to +4.0V
Input Voltage (all inputs)	–0.5V to +4.0V
Output Voltage (all outputs)	–0.5V to +4.0V
Pb-Free Temperature (soldering, 10sec.)	260°C
Storage Temperature (T_s)	–55°C to +150°C

Operating Ratings[2]

Supply Voltage	
(V_{DD}1.2, PLLDV$_{DD}$1.2, PLLSV$_{DD}$1.2, USB1V$_{DD}$1.2, USB2V$_{DD}$1.2)	+1.235V to +1.365V
V_{DD}2.5	+2.3V to +2.7V
(V_{DD}3.3, PLLV$_{DD}$A3.3, PLLDV$_{DD}$3.3, USB1V$_{DD}$A3.3, USB2V$_{DD}$A3.3, USBCV$_{DD}$A3.3)	+3.0V to +3.6V
Ambient Temperature (T_A)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Junction Temperature (T_J)	150°C
Package Thermal Resistance[3]	
(θ_{JA}) No Air Flow	23.4°C/W
1m/s	21.1°C/W
2m/s	20.2°C/W
(θ_{JC}) No Air Flow	9.5°C/W

Electrical Characteristics [4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Total Supply Current with WAN and LAN ports under 1000 Mbps Data Traffic, DDR clock = 200MHz						
$I_{1.3V}$	VDD1.2, PLLDVDD1.2, PLLSVDD1.2, USB1VDD1.2, USB2VDD1.2	Single supply at 1.3V		595		mA
$I_{2.6V}$	VDD2.5	Single supply at 2.6V		160		mA
$I_{3.3v}$	VDD3.3, PLLVDDA3.3, PLLDVDD3.3, USB1VDDA3.3, USB2VDDA3.3, USBCVDDA3.3	Single supply at 3.3V		116		mA
TTL Inputs (SDIO, Static Memory, UART, SPI, I2C, I2S, MDC/MDIO, GPIO)						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current (Excluding pull-up/pull-down)	V_{IN} = GND ~ $V_{DD3.3}$	–10		10	µA
TTL Outputs (SDIO, Static Memory, UART, SPI, I2C, I2S, MDC/MDIO, GPIO)						
V_{OH}	Output High Voltage	I_{OH} = –8mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.4	V
I_{OZ}	Output Tri-state Leakage				10	µA
PCI Electrical: Compliant to PCI version 2.3 Standard **DDR Electrical: Compliant to EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5V, SSTL_2)** **USB 2.0 Electrical: Compliant to USB 2.0 Standard** **RGMII Electrical: Compliant to Reduced Gigabit Media Independent Interface(RGMII) Version 1.3 [5]** **MII Electrical: compliant to IEEE 802.3u Specification**						

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD}).
3. No heat spreader in package.
4. TA = 25°C. The specification is for the packaged product only.
5. RGMII interface is standard 3.3V CMOS VIO. However “Reduced Gigabit Media Independent Interface(RGMII) Version 1.3” specification is based on 2.5V CMOS VIO. Therefore any chosen RGMII based PHY must be evaluated based upon standard 3.3V CMOS VIO compatibility.

Timing Specifications

Figure 16 provides power sequencing requirement with respect to system reset.

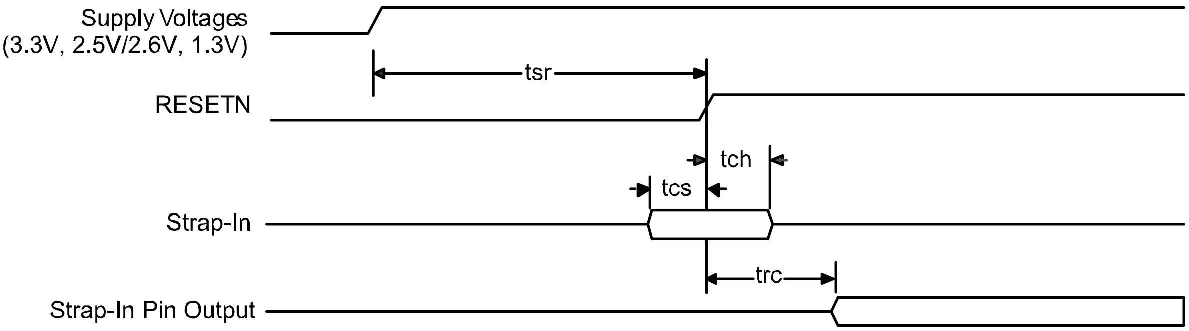


Figure 16. Reset Timing

Note: Power sequencing of supply voltages must be in order of 3.3V first, 2.5V/2.6V next and 1.3V last

Symbol	Parameter	Min	Typ	Max	Units
t_{SR}	Stable supply voltages to reset high	10			ms
t_{CS}	Configuration set-up time	50			ns
t_{CH}	Configuration hold time	50			ns
t_{RC}	Reset to strap-in pin output	50			ns

Table 1. Reset Timing Parameters

Figure 17 and Figure 18 provide NOR FLASH, ROM and SRAM interface timing.

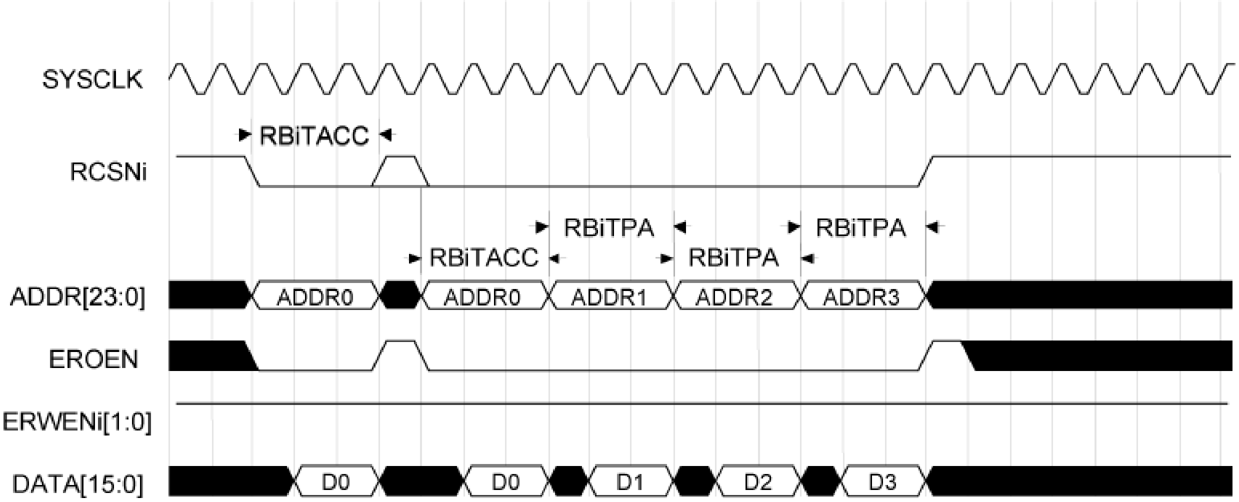


Figure 17. Static Memory Read Cycle

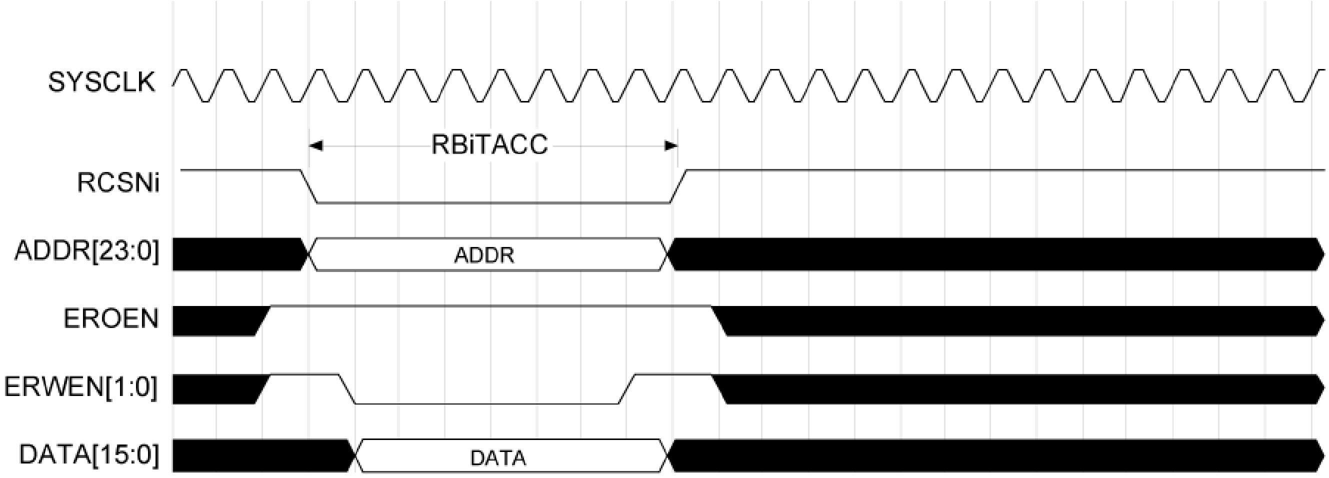


Figure 18. Static Memory Write Cycle

Symbol	Parameter[1]	Registers
RBiTACC	Programmable bank i access time	0x5010, 0x5014
RBiTPA	Programmable bank i page access time	0x5010, 0x5014

Table 2. Programmable Static Memory Timing Parameters

Note:

1. "i" Refers to chip select parameters 0 and 1.

Figure 19 provides external I/O ports interface timing.

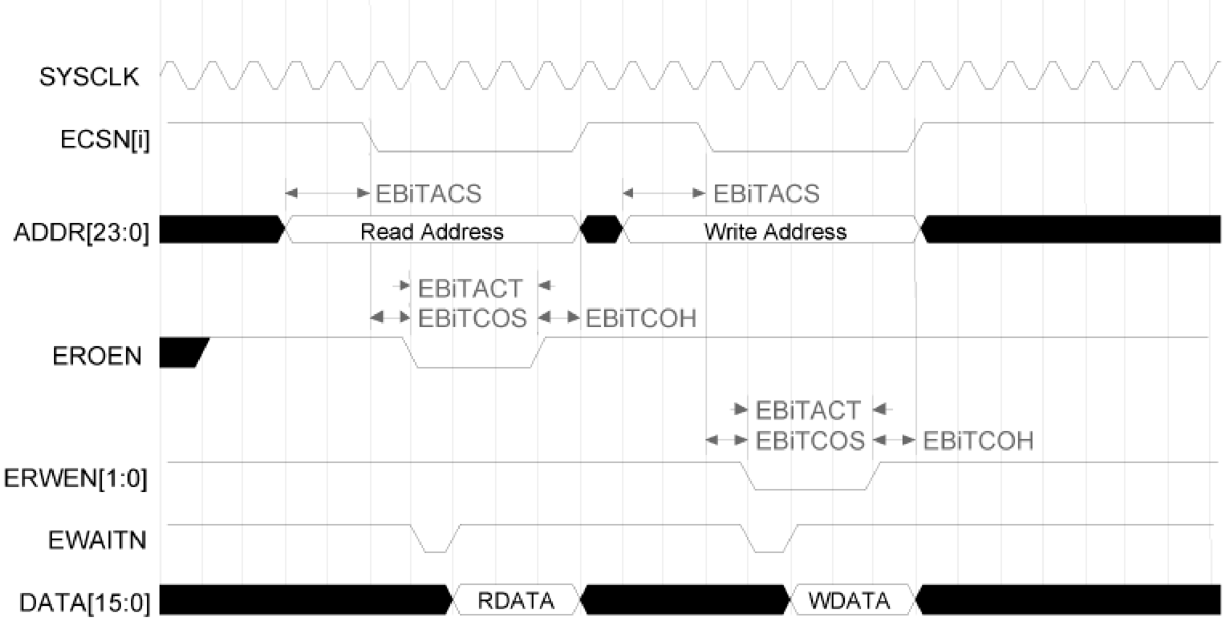


Figure 19. External I/O Read and Write Cycles

Symbol	Parameter	Min[(1)]	Typ[(1)]	Max[(1)]	Units
T_{cta}	Valid address to CS setup time	EBiTACS +0.8	EBiTACS +1.1	EBiTACS +1.3	ns
T_{cos}	OE valid to CS setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dsu}	Valid read data to OE setup time	2.0			ns
T_{cws}	WE valid to CS setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dh}	Write data to CS hold time	0			ns
T_{cah}	Address to CS hold time	EBiTCOH +1.0	EBiTCOH +1.0	EBiTCOH +1.4	ns
T_{oew}	OE/WE pulsewidth	EBiTACT		EBiTACT	ns
T_{ocs}, T_{csw}	Rising edge CS to OE/WE hold time	0			ns

Table 3. External I/O Memory Timing Parameters

Note:

1. Measurements for minimum were taken at 0°C, typical at 25°C, and maximum at 100°C.

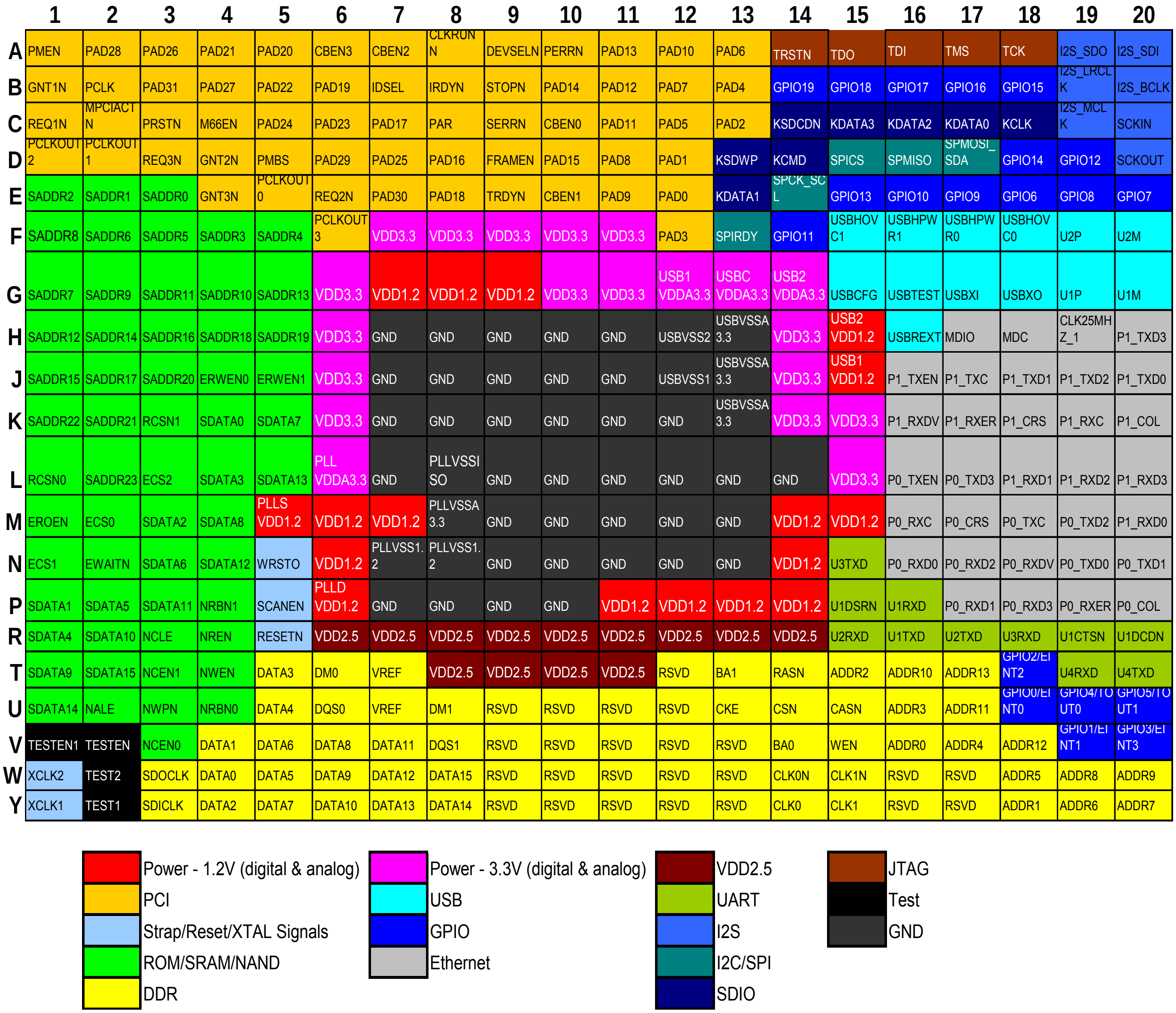
Symbol	Parameter[(1)]	Registers
EBiTACS	Programmable bank i address setup time before chip select	0x5000, 0x5004, 0x5008
EBiTACT	Programmable bank i write enable/output enable access time	0x5000, 0x5004, 0x5008
EBiTCOS	Programmable bank i chip select setup time before OEN	0x5000, 0x5004, 0x5008
EBiTCOH	Programmable bank i chip select hold time	0x5000, 0x5004, 0x5008

Table 4. Programmable External I/O Timing Parameters

Note:

1. "i" Refers to chip select parameters 0, 1, or 2.

Signal Location Information



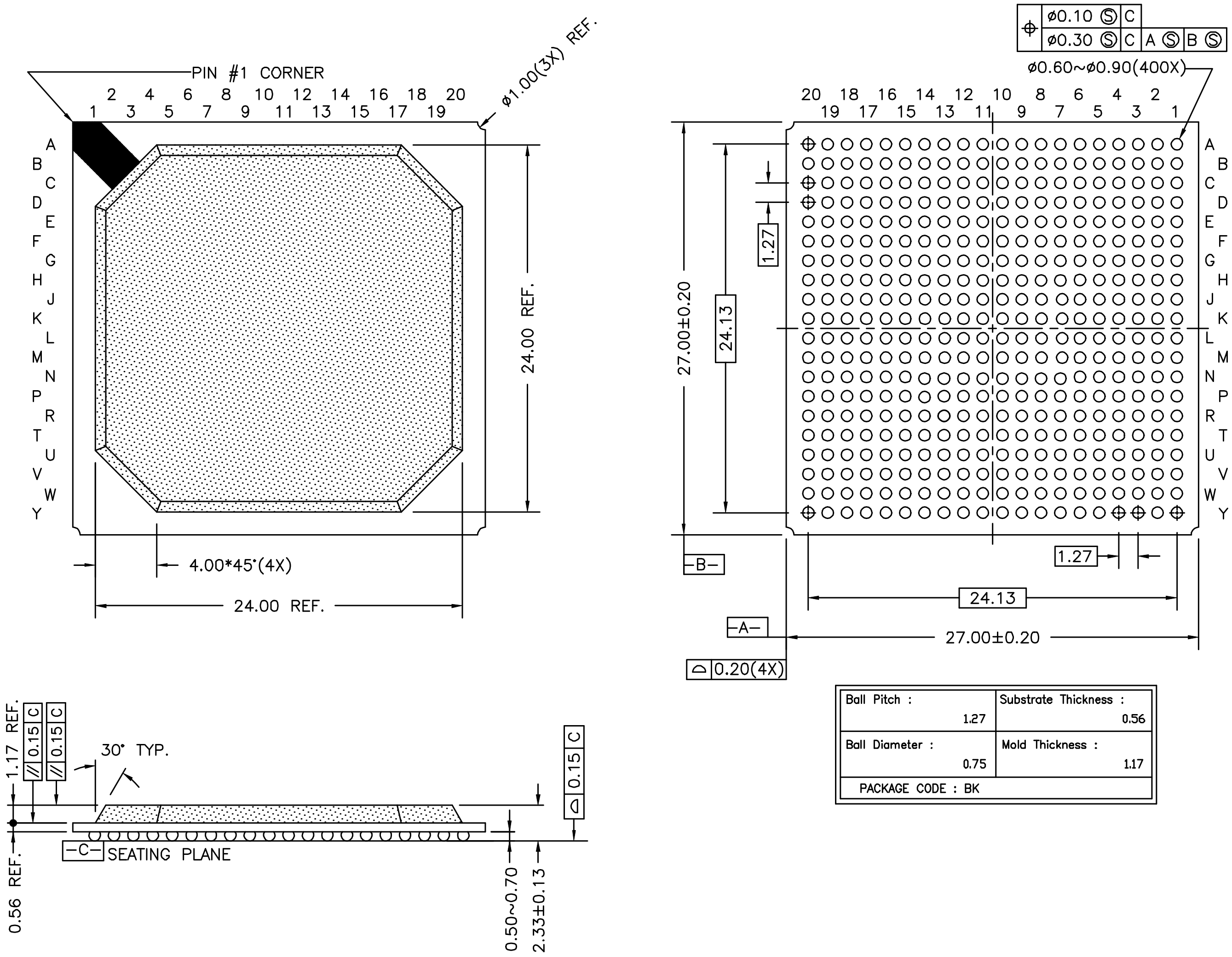
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	PMEN	PAD28	PAD26	PAD21	PAD20	CBEN3	CBEN2	CLKRUNN	DEVSELN	PERRN	PAD13	PAD10	PAD6	TRSTN	TDO	TDI	TMS	TCK	I2S_SDO	I2S_SDI
B	GNT1N	PCLK	PAD31	PAD27	PAD22	PAD19	IDSEL	IRDYN	STOPN	PAD14	PAD12	PAD7	PAD4	GPIO19	GPIO18	GPIO17	GPIO16	GPIO15	I2S_LRCLK	I2S_BCLK
C	REQ1N	MPCIACTN	PRSTN	M66EN	PAD24	PAD23	PAD17	PAR	SERRN	CBEN0	PAD11	PAD5	PAD2	KSDCDN	KDATA3	KDATA2	KDATA0	KCLK	I2S_MCLK	SCKIN
D	PCLKOUT2	PCLKOUT1	REQ3N	GNT2N	PMBS	PAD29	PAD25	PAD16	FRAMEN	PAD15	PAD8	PAD1	KSDWP	KCMD	SPICS	SPMISO	SPMOSI_SDA	GPIO14	GPIO12	SCKOUT
E	SADDR2	SADDR1	SADDR0	GNT3N	PCLKOUT0	REQ2N	PAD30	PAD18	TRDYN	CBEN1	PAD9	PAD0	KDATA1	SPCK_SCL	GPIO13	GPIO10	GPIO9	GPIO6	GPIO8	GPIO7
F	SADDR8	SADDR6	SADDR5	SADDR3	SADDR4	PCLKOUT3	VDD3.3	VDD3.3	VDD3.3	VDD3.3	VDD3.3	PAD3	SPIRDY	GPIO11	USBHOVC1	USBHPWR1	USBHPWR0	USBHOVC0	U2P	U2M
G	SADDR7	SADDR9	SADDR11	SADDR10	SADDR13	VDD3.3	VDD1.2	VDD1.2	VDD1.2	VDD3.3	VDD3.3	USB1 VDDA3.3	USBC VDDA3.3	USB2 VDDA3.3	USBCFG	USBTEST	USBXI	USBXO	U1P	U1M
H	SADDR12	SADDR14	SADDR16	SADDR18	SADDR19	VDD3.3	GND	GND	GND	GND	GND	USBVSS2	USBVSSA 3.3	VDD3.3	USB2 VDD1.2	USBREXT	MDIO	MDC	CLK25MHZ_1	P1_TXD3
J	SADDR15	SADDR17	SADDR20	ERWEN0	ERWEN1	VDD3.3	GND	GND	GND	GND	GND	USBVSS1	USBVSSA 3.3	VDD3.3	USB1 VDD1.2	P1_TXEN	P1_TXC	P1_TXD1	P1_TXD2	P1_TXD0
K	SADDR22	SADDR21	RCSN1	SDATA0	SDATA7	VDD3.3	GND	GND	GND	GND	GND	GND	USBVSSA 3.3	VDD3.3	VDD3.3	P1_RXDV	P1_RXER	P1_CRS	P1_RXC	P1_COL
L	RCSN0	SADDR23	ECS2	SDATA3	SDATA13	PLL VDDA3.3	GND	PLLVSSISO	GND	GND	GND	GND	GND	GND	VDD3.3	P0_TXEN	P0_TXD3	P1_RXD1	P1_RXD2	P1_RXD3
M	EROEN	ECS0	SDATA2	SDATA8	PLLS VDD1.2	VDD1.2	VDD1.2	PLLVSSA 3.3	GND	GND	GND	GND	GND	VDD1.2	VDD1.2	P0_RXC	P0_CRS	P0_TXC	P0_TXD2	P1_RXD0
N	ECS1	EWAITN	SDATA6	SDATA12	WRSTO	VDD1.2	PLLVSS1.2	PLLVSS1.2	GND	GND	GND	GND	GND	VDD1.2	U3TXD	P0_RXD0	P0_RXD2	P0_RXDV	P0_TXD0	P0_TXD1
P	SDATA1	SDATA5	SDATA11	NRBN1	SCANEN	PLLD VDD1.2	GND	GND	GND	GND	VDD1.2	VDD1.2	VDD1.2	VDD1.2	U1DSRN	U1RXD	P0_RXD1	P0_RXD3	P0_RXER	P0_COL
R	SDATA4	SDATA10	NCLE	NREN	RESETN	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	U2RXD	U1TXD	U2TXD	U3RXD	U1CTSN	U1DCDN
T	SDATA9	SDATA15	NCEN1	NWEN	DATA3	DM0	VREF	VDD2.5	VDD2.5	VDD2.5	VDD2.5	RSVD	BA1	RASN	ADDR2	ADDR10	ADDR13	GPIO2/EINT2	U4RXD	U4TXD
U	SDATA14	NALE	NWPN	NRBN0	DATA4	DQS0	VREF	DM1	RSVD	RSVD	RSVD	RSVD	CKE	CSN	CASN	ADDR3	ADDR11	GPIO0/EINT0	GPIO4/TOUT0	GPIO5/TOUT1
V	TESTEN1	TESTEN	NCEN0	DATA1	DATA6	DATA8	DATA11	DQS1	RSVD	RSVD	RSVD	RSVD	RSVD	BA0	WEN	ADDR0	ADDR4	ADDR12	GPIO1/EINT1	GPIO3/EINT3
W	XCLK2	TEST2	SDOCLK	DATA0	DATA5	DATA9	DATA12	DATA15	RSVD	RSVD	RSVD	RSVD	RSVD	CLK0N	CLK1N	RSVD	RSVD	ADDR5	ADDR8	ADDR9
Y	XCLK1	TEST1	SDICLK	DATA2	DATA7	DATA10	DATA13	DATA14	RSVD	RSVD	RSVD	RSVD	RSVD	CLK0	CLK1	RSVD	RSVD	ADDR1	ADDR6	ADDR7

🟥 Power - 1.2V (digital & analog)	🟪 Power - 3.3V (digital & analog)	🟫 VDD2.5	🟫 JTAG
🟧 PCI	🟦 USB	🟩 UART	⬛ Test
🟦 Strap/Reset/XTAL Signals	🟦 GPIO	🟦 I2S	⬛ GND
🟩 ROM/SRAM/NAND	⬜ Ethernet	🟦 I2C/SPI	
🟨 DDR		🟦 SDIO	

Note: for KSZ9692XPB SDIO balls (D14, C18, C15, C16, E13, C17, C14, D13) and PCI balls (E4, D4, D3, E6, F6, D1) are no connect.

Figure 20. Ball Grid Array Map

Package Information



Ball Pitch : 1.27	Substrate Thickness : 0.56
Ball Diameter : 0.75	Mold Thickness : 1.17
PACKAGE CODE : BK	

Figure 21. 400-Pin PBGA

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- *Входной контроль качества.*
- *Наличие сертификата ISO.*

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