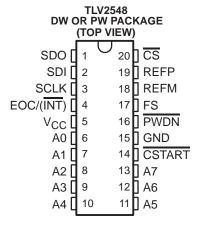
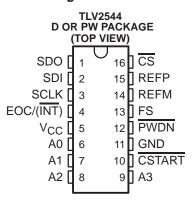
#### TLV2544, TLV2548 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN

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- Maximum Throughput 200-KSPS
- Built-In Reference, Conversion Clock and 8× FIFO
- Differential/Integral Nonlinearity Error: +1 LSB
- Signal-to-Noise and Distortion Ratio: 70 dB, f<sub>i</sub> = 12-kHz
- Spurious Free Dynamic Range: 75 dB, f<sub>i</sub> = 12- kHz
- SPI (CPOL = 0, CPHA = 0)/DSP-Compatible Serial Interfaces With SCLK up to 20-MHz

- Single Wide Range Supply 2.7 Vdc to 5.5 Vdc
- Analog Input Range 0-V to Supply Voltage With 500 kHz BW
- Hardware Controlled and Programmable Sampling Period
- Low Operating Current (1.0-mA at 3.3-V, 1.1-mA at 5.5-V With External Ref
- Power Down: Software/Hardware Power-Down Mode (1 μA Max, Ext Ref), Autopower-Down Mode (1 μA, Ext Ref)
- Programmable Auto-Channel Sweep





#### description

The TLV2548 and TLV2544 are a family of high performance, 12-bit low power, 3.86  $\mu$ s, CMOS analog-to-digital converters (ADC) which operate from a single 2.7-V to 5.5-V power supply. These devices have three digital inputs and a 3-state output [chip select ( $\overline{\text{CS}}$ ), serial input-output clock (SCLK), serial data input (SDI), and serial data output (SDO)] that provide a direct 4-wire interface to the serial port of most popular host microprocessors (SPI interface). When interfaced with a TI DSP, a frame sync (FS) signal is used to indicate the start of a serial data frame.

In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip analog multiplexer that can select any analog inputs or one of three internal self-test voltages. The sample-and-hold function is automatically started after the fourth SCLK edge (normal sampling) or can be controlled by a special pin,  $\overline{CSTART}$ , to extend the sampling period (extended sampling). The normal sampling period can also be programmed as short (12 SCLKs) or as long (24 SCLKs) to accommodate faster SCLK operation popular among high-performance signal processors. The TLV2548 and TLV2544 are designed to operate with very low power consumption. The power-saving feature is further enhanced with software/hardware/autopower-down modes and programmable conversion speeds. The conversion clock (OSC) and reference are built-in. The converter can use the external SCLK as the source of the conversion clock to achieve higher (up to 2.8 µs when a 20 MHz SCLK is used) conversion speed. Two different internal reference voltages are available. An optional external reference can also be used to achieve maximum flexibility.

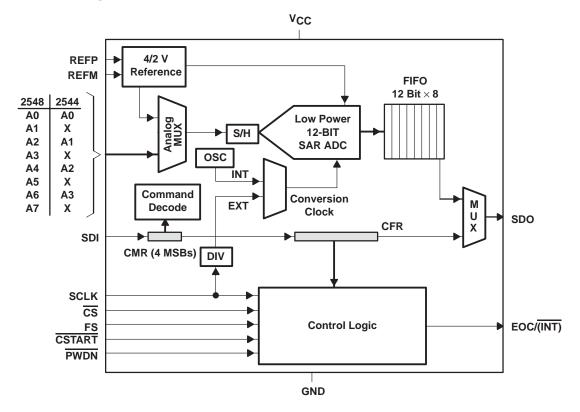
The TLV2544C and the TLV2548C are characterized for operation from 0°C to 70°C. The TLV2544I and the TLV2548I are characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### functional block diagram



#### **AVAILABLE OPTIONS**

	PACKAGED DEVICES						
TA	20-TSSOP (PW)	20-SOIC (DW)	16-SOIC (D)	16-TSSOP (PW)	20-CDIP (J)	20-LCCC (FK)	
0°C to 70°C	TLV2548CPW	TLV2548CDW	TLV2544CD	TLV2544CPW			
-40°C to 85°C	TLV2548IPW	TLV2548IDW	TLV2544ID	TLV2544IPW	_	_	



# TLV2544, TLV2548 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN SLAS198E - FEBRUARY 1999 - REVISED JUNE 2003

#### **Terminal Functions**

Т	TERMINAL					
NAME	N	NO.		DESCRIPTION		
IVAIVIL	TLV2544	TLV2548				
A0 A0 A1 A1	6 7	6 7	I	Analog signal inputs. The analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 k $\Omega$ .		
A2 A2 A3 A3 A4 A5 A6 A7	8 9	8 9 10 11 12 13		For a source impedance greater than 1 k $\Omega$ , use the asynchronous conversion start signal $\overline{\text{CSTART}}$ ( $\overline{\text{CSTART}}$ low time controls the sampling period) or program long sampling period to increase the sampling time.		
टड	16	20	I	Chip select. A high-to-low transition on the $\overline{\text{CS}}$ input resets the internal 4-bit counter, enables SDI, and removes SDO from 3-state within a maximum setup time. SDI is disabled within a setup time after the 4-bit counter counts to 16 (clock edges) or a low-to-high transition of $\overline{\text{CS}}$ whichever happens first.  NOTE: $\overline{\text{CS}}$ falling and rising edges need to happen when SCLK is low for a microprocessor interface such as SPI.		
CSTART	10	14	ı	This terminal controls the start of sampling of the analog input from a selected multiplex channel. Sampling time starts with the falling edge of CSTART and ends with the rising edge of CSTART as long as CS is held high. In mode 01, select cycle, CSTART can be issued as soon as CHANNEL is selected which means the fifth SCLK during the select cycle, but the effective sampling time is not started until CS goes to high. The rising edge of CSTART (when CS = 1) also starts the conversion. Tie this terminal to VCC if not used.		
EOC/(INT)	4	4	0	End of conversion or interrupt to host processor.  [PROGRAMMED AS EOC]: This output goes from a high-to-low logic level at the end of the sampling period and remains low until the conversion is complete and data are ready for transfer. EOC is used in conversion mode 00 only.  [PROGRAMMED AS INT]: This pin can also be programmed as an interrupt output signal to the host processor. The falling edge of INT indicates data are ready for output. The following CS↓ or FS clears INT.		
FS	13	17	I	DSP frame sync input. Indication of the start of a serial data frame in or out of the device. If FS remains low after the falling edge of $\overline{CS}$ , SDI is not enabled until an active FS is presented. A high-to-low transition on the FS input resets the internal 4-bit counter and enables SDI within a maximum setup time. SDI is disabled within a setup time after the 4-bit counter counts to 16 (clock edges) or a low-to-high transition of $\overline{CS}$ whichever happens first.  Tie this terminal to $V_{CC}$ if not used. See the date code information section, item (1).		
GND	11	15	I	Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.		
PWDN	12	16	ı	Both analog and reference circuits are powered down when this pin is at logic zero. The device can be restarted by active CS, FS or CSTART after this pin is pulled back to logic one.		
SCLK	3	3	I	Input serial clock. This terminal receives the serial SCLK from the host processor. SCLK is used to clock the input SDI to the input register. When programmed, it may also be used as the source of the conversion clock.  NOTE: This device supports CPOL (clock polarity) = 0, which is SCLK returns to zero when idling for SPI compatible interface.		
SDI	2	2	I	Serial data input. The input data is presented with the MSB (D15) first. The first 4-bit MSBs, D(15–12) are decoded as one of the 16 commands (12 only for the TLV2544). The configure write commands require an additional 12 bits of data. When FS is not used (FS =1), the first MSB (D15) is expected after the falling edge of CS and is latched in on the rising edges of SCLK (after $\overline{\text{CS}}\downarrow$ ). When FS is used (typical with an active FS from a DSP) the first MSB (D15) is expected after the falling edge of FS and is latched in on the falling edges of SCLK. SDI is disabled within a setup time after the 4-bit counter counts to 16 (clock edges) or a low-to-high transition of $\overline{\text{CS}}$ whichever happens first.		



#### **Terminal Functions (Continued)**

TERMINAL					
NAME	NAME NO.		I/O	DESCRIPTION	
TLV2544 TLV25		TLV2548			
SDO	1	1	0	The 3-state serial output for the A/D conversion result. SDO is kept in the high-impedance state when $\overline{CS}$ is high and after the $\overline{CS}$ falling edge and until the MSB is presented. The output format is MSB first.	
				When FS is not used (FS = 1 at the falling edge of $\overline{CS}$ ), the MSB is presented to the SDO pin after the $\overline{CS}$ falling edge, and successive data are available at the rising edge of SCLK and changed of the falling edge.	
				When FS is used (FS = 0 at the falling edge of $\overline{CS}$ ), the MSB is presented to SDO after the falling edge of $\overline{CS}$ and FS = 0 is detected. Successive data are available at the falling edge of SCLK and changed on the rising edge. (This is typically used with an active FS from a DSP.)	
				For conversion and FIFO read cycles, the first 12 bits are result from previous conversion (data) followed by 4 don't care bits. The first four bits from SDO for CFR read cycles should be ignored. The register content is in the last 12 bits. SDO is 3-state (float) after the 16th bit. See the date code information section, item (2).	
REFM	14	18	I	External reference input or internal reference decoupling. Tie this pin to analog ground if internal reference is used.	
REFP	15	19	I	External reference input or internal reference decoupling. (Shunt capacitors of 10 $\mu$ F and 0.1 $\mu$ F between REFP and REFM.) The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the REFM terminal when an external reference is used.	
VCC	5	5	I	Positive supply voltage	

#### detailed description

#### analog inputs and internal test voltages

The 4/8 analog inputs and three internal test inputs are selected by the analog multiplexer depending on the command entered. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

#### converter

The TLV2544/48 uses a 12-bit successive approximation ADC utilizing a charge redistribution DAC. Figure 1 shows a simplified version of the ADC.

The sampling capacitor acquires the signal on Ain during the sampling period. When the conversion process starts, the SAR control logic and charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator into a balanced condition. When the comparator is balanced, the conversion is complete and the ADC output code is generated.



## 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN

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#### detailed description (continued)

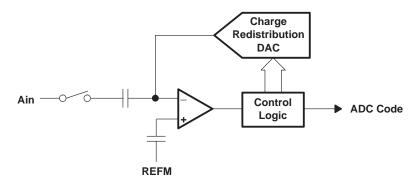


Figure 1. Simplified Model of the Successive-Approximation System

#### serial interface

INPUT DATA FORMAT					
MSB LSE					
D15-D12	D11-D0				
Command ID[15:12]	Configuration data field ID[11:0]				

Input data is binary. All trailing blanks can be filled with zeros.

OUTPUT DATA FORMAT READ CFR/FIFO READ				
MSB LSI				
D15-D12 D11-D0				
Don't care Register content or FIFO content OD[11:0]				

OUTPUT DATA FORMAT CONVERSION					
MSB LSB					
D15-D4	D3-D0				
Conversion result OD[11:0]	Don't care				

The output data format is binary (unipolar straight binary).

#### binary

Zero scale code = 000h, Vcode = VREFM Full scale code = FFFh, Vcode = VREFP - 1 LSB



#### control and timing

#### power up and initialization requirements

- Determine processor type by writing A000h to the TLV2544/48 (CS must be toggled)
- Configure the device (CS must make a high-to-low transition, then can be held low if in DSP mode; i.e., active FS.)

The first conversion after power up or resuming from power down is not valid.

#### start of the cycle:

- When FS is not used (FS = 1 at the falling edge of  $\overline{CS}$ ), the falling edge of  $\overline{CS}$  is the start of the cycle.
- When FS is used (FS is an active signal from a DSP), the falling edge of FS is the start of the cycle.

#### first 4-MSBs: the command register (CMR)

The TLV2544/TLV2548 have a 4-bit command set (see Table 1) plus a 12-bit configuration data field. Most of the commands require only the first 4 MSBs, i.e., without the 12-bit data field.

The valid commands are listed in Table 1.

Table 1. TLV2544/TLV2548 Command Set

SDI D(15-12) BINARY		TLV2548 COMMAND	TLV2544 COMMAND			
0000b	0h	Select analog input channel 0	Select analog input channel 0			
0001b	1h	Select analog input channel 1	N/A			
0010b	2h	Select analog input channel 2	Select analog input channel 1			
0011b	3h	Select analog input channel 3	N/A			
0100b	4h	Select analog input channel 4	Select analog input channel 2			
0101b	5h	Select analog input channel 5	N/A			
0110b	6h	Select analog input channel 6	Select analog input channel 3			
0111b	7h	Select analog input channel 7	N/A			
1000b	8h	SW power down (analog + reference)				
1001b	9h	Read CFR register data shown as SDO D(11-0)				
1010b	Ah plus data	Write CFR followed by 12-bit data, e.g., 0A100h means external reference, short sampling, SCLK/4, single shot, INT				
1011b	Bh	Select test, voltage = (REFP+REFM)/2				
1100b	Ch	Select test, voltage = REFM				
1101b	Dh	Select test, voltage = REFP				
1110b	Eh	FIFO read, FIFO contents shown as SDO D(15-4), D(3-0) = 0000				
1111b	1111b Fh plus data Reserved					

NOTE: The status of the CFR can be read with a read CFR command when the device is programmed for one-shot conversion mode (CFR D[6,5] = 00).



#### control and timing (continued)

#### configuration

Configuration data is stored in one 12-bit configuration register (CFR) (see Table 2 for CFR bit definitions). Once configured after first power up, the information is retained in the H/W or S/W power down state. When the device is being configured, a write CFR cycle is issued by the host processor. This is a 16-bit write. If the SCLK stops after the first 8 bits are entered, then the next eight bits can be taken after the SCLK is resumed.

Table 2. TLV2544/TLV2548 Configuration Register (CFR) Bit Definitions

BIT	DEFIN	IITION			
D11	Reference select 0: External 1: Internal (Tie REFM to analog ground if the Internal reference is selected.)				
D10	Internal reference voltage select 0: Internal ref = 4 V 1: internal ref = 2 V				
D9	Sample period select 0: Short sampling 12 SCLKs (1x sampling 1: Long sampling 24 SCLKs (2x sampling 24 SCLKs)				
D(8,7)	Conversion clock source select  00: Conversion clock = internal OSC  01: Conversion clock = SCLK  10: Conversion clock = SCLK/4  11: Conversion clock = SCLK/2				
D(6,5)	Conversion mode select 00: Single shot mode [FIFO not used, D(1,0) has no effect.] 01: Repeat mode 10: Sweep mode 11: Repeat sweep mode				
D(4,3)†	TLV2548	TLV2544			
	Sweep auto sequence select       Sweep auto sequence select         00: 0-1-2-3-4-5-6-7       00: N/A         01: 0-2-4-6-0-2-4-6       01: 0-1-2-3-0-1-2-3         10: 0-0-2-2-4-4-6-6       10: 0-0-1-1-2-3-3         11: 0-2-0-2-0-2       11: 0-1-0-1-0-1				
D2	EOC/INT – pin function select 0: Pin used as INT 1: Pin used as EOC				
D(1,0)	1: Pin used as EOC  FIFO trigger level (sweep sequence length) 00: Full (INT generated after FIFO level 7 filled) 01: 3/4 (INT generated after FIFO level 5 filled) 10: 1/2 (INT generated after FIFO level 3 filled) 11: 1/4 (INT generated after FIFO level 1 filled)				

<sup>&</sup>lt;sup>†</sup> These bits only take effect in conversion modes 10 and 11.

#### sampling

The sampling period starts after the first 4 input data are shifted in if they are decoded as one of the conversion commands. These are select analog input (channel 0 through 7) and select test (channel 1 through 3).



#### normal sampling

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When the converter is using normal sampling, the sampling period is programmable. It can be 12 SCLKs (short sampling) or 24 SCLKs (long sampling). Long sampling helps when SCLK is faster than 10 MHz or when input source resistance is high.

#### extended sampling

CSTART – An asynchronous (to the SCLK) signal, via dedicated hardware pin, CSTART, can be used in order to have total control of the sampling period and the start of a conversion. This extended sampling is user-defined and is totally independent of SCLK. While CS is high, the falling edge of CSTART is the start of the sampling period and is controlled by the low time of CSTART. The minimum low time for CSTART should be at least equal to the minimum  $t_{(SAMPLE)}$ . In a select cycle used in mode 01 (REPEAT MODE),  $\overline{CSTART}$  can be started as soon as the channel is selected (after the fifth SCLK). In this case the sampling period is not started until CS has become inactive. Therefore the nonoverlapped CSTART low time must meet the minimum sampling time requirement. The low-to-high transition of CSTART terminates the sampling period and starts the conversion period. The conversion clock can also be configured to use either internal OSC or external SCLK. This function is useful for an application that requires:

- The use of an extended sampling period to accommodate different input source impedance
- The use of a faster I/O clock on the serial port but not enough sampling time is available due to the fixed number of SCLKs. This could be due to a high input source impedance or due to higher MUX ON resistance at lower supply voltage.

Once the conversion is complete, the processor can initiate a read cycle by using either the read FIFO command to read the conversion result or by simply selecting the next channel number for conversion. Since the device has a valid conversion result in the output buffer, the conversion result is simply presented at the serial data output. To completely get out of the extended sampling mode, CS must be toggled twice from a high-to-low transition while CSTART is high. The read cycle mentioned above followed by another configuration cycle of the ADC qualifies this condition and successfully puts the ADC back to its normal sampling mode. This can be viewed in Figure 9.

**Table 3. Sample and Convert Conditions** 

	CONDITIONS	SAMPLE	CONVERT
CSTART	CS = 1 (see Figures 11 and 18)	No sampling clock (SCLK) required. Sampling period is totally controlled by the low time of CSTART. The high-to-low transition of CSTART (when CS=1) starts the sampling of the analog input signal. The low time of CSTART dictates the sampling period. The low-to-high transition of CSTART ends sampling period and begins the conversion cycle. (Note: this trigger only works when internal reference is selected for conversion modes 01, 10, and 11.)	
<del>cs</del>	CSTART = 1 FS = 1	SCLK is required. Sampling period is programmable under normal sampling. When programmed to sample under short sampling, 12 SCLKs are generated to complete sampling period. 24 SCLKs are generated when programmed for long sampling. A command set to configure the device requires 4 SCLKs thereby ex-	<ol> <li>If the internal clock OSC is selected a maximum conversion time of 3.86 μs can be achieved.</li> <li>If external SCLK is selected, conversion time is t<sub>CONV</sub> = 14 × DIV/f(SCLK), where DIV can be 1, 2, or 4.</li> </ol>
FS	CSTART = 1 CS = 0	tending to 16 or 28 SCLKs respectively before conversion takes place. (Note: Because the ADC only bypasses a valid channel select command, the user can use select channel 0, 0000b, as the SDI input when either $\overline{\text{CS}}$ or FS is used as trigger for conversion. The ADC responds to commands such as SW powerdown, 1000b.)	



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#### TLV2544/TLV2548 conversion modes

The TLV2544 and TLV2548 have four different conversion modes (mode 00, 01, 10, 11). The operation of each mode is slightly different, depending on how the converter performs the sampling and which host interface is used. The trigger for a conversion can be an active  $\overline{\text{CSTART}}$  (extended sampling),  $\overline{\text{CS}}$  (normal sampling, SPI interface), or FS (normal sampling, TMS320 DSP interface). When FS is used as the trigger,  $\overline{\text{CS}}$  can be held active, i.e.  $\overline{\text{CS}}$  does not need to be toggled through the trigger sequence. SDI can be one of the channel select commands, such as SELECT CHANNEL 0. Different types of triggers should not be mixed throughout the repeat and sweep operations. When  $\overline{\text{CSTART}}$  is used as the trigger, the conversion starts on the rising edge of  $\overline{\text{CSTART}}$ . The minimum low time for  $\overline{\text{CSTART}}$  is equal to  $t_{(SAMPLE)}$ . If an active  $\overline{\text{CS}}$  or FS is used as the trigger, the conversion is started after the 16th or 28th SCLK edge. Enough time (for conversion) should be allowed between consecutive triggers so that no conversion is terminated prematurely.

#### one shot mode (mode 00)

One shot mode (mode 00) does not use the FIFO, and the EOC is generated as the conversion is in progress (or  $\overline{\text{INT}}$  is generated after the conversion is done).

#### repeat mode (mode 01)

Repeat mode (mode 01) uses the FIFO. This mode setup requires configuration cycle and channel select cycle. Once the programmed FIFO threshold is reached, the FIFO must be read, or the data is lost when the sequence starts over again with the SELECT cycle and series of triggers. No configuration is required except for reselecting the channel unless the operation mode is changed. This allows the host to set up the converter and continue monitoring a fixed input and come back to get a set of samples when preferred.

Triggered by  $\overline{\text{CSTART}}$ : The first conversion can be started with a select cycle or  $\overline{\text{CSTART}}$ . To do so, the user can issue  $\overline{\text{CSTART}}$  during the select cycle, immediately after the four-bit channel select command. The first sample started as soon as the select cycle is finished (i.e.,  $\overline{\text{CS}}$  returns to 1). If there is enough time (2  $\mu$ s) left between the SELECT cycle and the following  $\overline{\text{CSTART}}$ , a conversion is carried out. In this case, you need one less trigger to fill the FIFO. Succeeding samples are triggered by  $\overline{\text{CSTART}}$ .

#### sweep mode (mode 10)

Sweep mode (mode 10) also uses the FIFO. Once it is programmed in this mode, all of the channels listed in the selected sweep sequence are visited in sequence. The results are converted and stored in the FIFO. This sweep sequence may not be completed if the FIFO threshold is reached before the list is completed. This allows the system designer to change the sweep sequence length. Once the FIFO has reached its programmed threshold, an interrupt (INT) is generated. The host must issue a read FIFO command to read and clear the FIFO before the next sweep can start.

#### repeat sweep mode (mode 11)

Repeat sweep mode (mode 11) works the same way as mode 10 except the operation has an option to continue even if the FIFO threshold is reached. Once the FIFO has reached its programmed threshold, an interrupt (INT) is generated. Then two things may happen:

- 1. The host may choose to act on it (read the FIFO) or ignore it. If the next cycle is a read FIFO cycle, all of the data stored in the FIFO is retained until it has been read in order.
- 2. If the next cycle is not a read FIFO cycle, or another CSTART is generated, all of the content stored in the FIFO is cleared before the next conversion result is stored in the FIFO, and the sweep is continued.



#### TLV2544/TLV2548 conversion modes (continued)

#### Table 4. TLV2544/TLV2548 Conversion Mode

CONVERSION MODE	CFR D(6,5)	SAMPLING TYPE	OPERATION
One shot	00	Normal	Single conversion from a selected channel  The conversion from a selected channel  Th
		Extended	Single conversion from a selected channel CS to select/read CSTART to start sampling and conversion One INT or EOC generated after each conversion Host must serve INT by selecting next channel and reading the previous output.
Repeat	01	Normal	<ul> <li>Repeated conversions from a selected channel</li> <li>CS or FS to start sampling/conversion</li> <li>One INT generated after FIFO is filled up to the threshold</li> <li>Host must serve INT by either 1) (FIFO read) reading out all of the FIFO contents up to the threshold, then repeat conversions from the same selected channel or 2) writing another command(s) to change the conversion mode. If the FIFO is not read when INT is served, it is cleared.</li> </ul>
		Extended	Same as normal sampling except CSTART starts each sampling and conversion when CS is high.
Sweep	10	Normal	One conversion per channel from a sequence of channels     CS or FS to start sampling/conversion     One INT generated after FIFO is filled up to the threshold     Host must serve INT by (FIFO read) reading out all of the FIFO contents up to the threshold, then write another command(s) to change the conversion mode.
		Extended	Same as normal sampling except CSTART starts each sampling and conversion when CS is high.
Repeat sweep	One INT generated after FIFO is filled up to the threshold     Host must serve INT by either 1) (FIFO read) reading out all of the FIFO countries threshold, then repeat conversions from the same selected channel or 2)		<ul> <li>CS or FS to start sampling/conversion</li> <li>One INT generated after FIFO is filled up to the threshold</li> <li>Host must serve INT by either 1) (FIFO read) reading out all of the FIFO contents up to the threshold, then repeat conversions from the same selected channel or 2) writing another command(s) to change the conversion mode. If the FIFO is not read when INT is served it is</li> </ul>
		Extended	Same as normal sampling except CSTART starts each sampling and conversion when CS is high.

NOTES: 1. Programming the EOC/INT pin as the EOC signal works for mode 00 only. The other three modes automatically generate an INT signal irrespective of how EOC/INT is programmed.

- 2. Extended. Sampling mode using CSTART as the trigger only works when internal reference is selected for conversion modes 01, 10, and 11.
- 3. When using CSTART to sample in extended mode, the falling edge of the next CSTART trigger should occur no more than 2.5 μs after the falling CS edge (or falling FS edge if FS is active) of the channel select cycle. This is to prevent an ongoing conversion from being canceled.



#### timing diagrams

The timing diagrams can be categorized into two major groups: nonconversion and conversion. The nonconversion cycles are read and write (configuration). None of these cycles carry a conversion. Conversion cycles are those four modes of conversion.

#### read cycle (read FIFO or read CFR)

#### read CFR cycle:

The read command is decoded in the first 4 clocks. SDO outputs the contents of the CFR after the 4th SCLK. This command works only when the device is programmed in the *single shot* mode (mode 00).

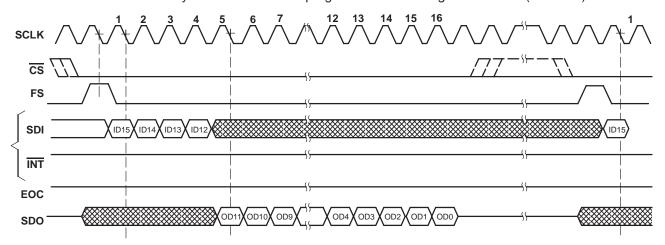


Figure 2. TLV2544/TLV2548 Read CFR Cycle (FS active)

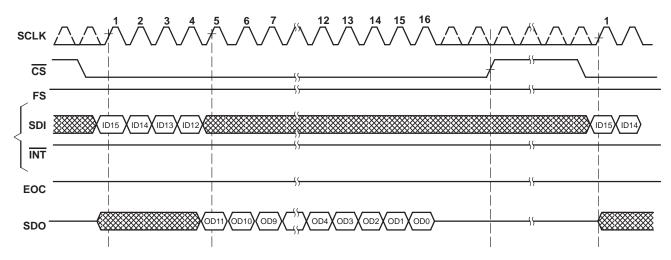
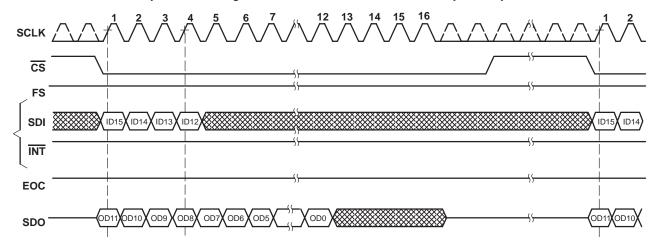


Figure 3. TLV2544/TLV2548 Read CFR Cycle (FS = 1)

#### read cycle (read FIFO or read CFR) (continued)

#### FIFO read cycle

The first command in the active cycle after INT is generated, if the FIFO is used, is assumed as the FIFO read command. The first FIFO content is output immediately before the command is decoded. If this command is not a FIFO read, then the output is terminated but the first data in the FIFO is retained until a valid FIFO read command is decoded. Use of more layers of the FIFO reduces the time taken to read multiple data. This is because the read cycle does not generate EOC or INT, nor does it carry out any conversion.



These devices can perform continuous FIFO read cycles (FS = 1) controlled by SCLK; SCLK can stop between each 16 SCLKs.

Figure 4. TLV2544/TLV2548 FIFO Read Cycle (FS = 1)



#### write cycle (write CFR)

The write cycle is used to write to the configuration register CFR (with 12-bit register content). The write cycle does not generate an EOC or  $\overline{\text{INT}}$ , nor does it carry out any conversion (see power up and initialization requirements).

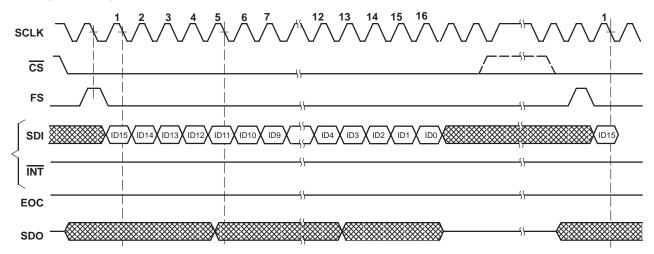


Figure 5. TLV2544/TLV2548 Write Cycle (FS Active)

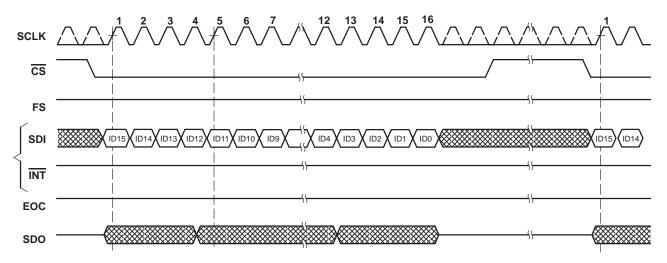


Figure 6. TLV2544/TLV2548 Write Cycle (FS = 1)

#### conversion cycles

#### **DSP/normal sampling**

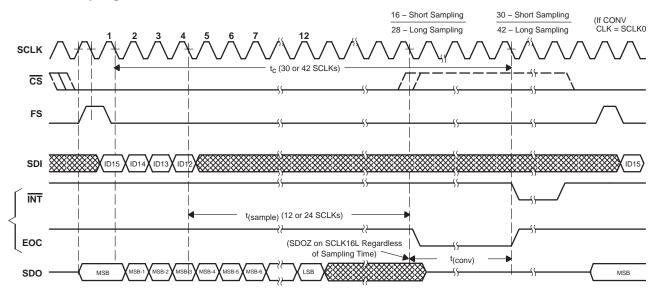


Figure 7. Mode 00 Single Shot/Normal Sampling (FS Signal Used)

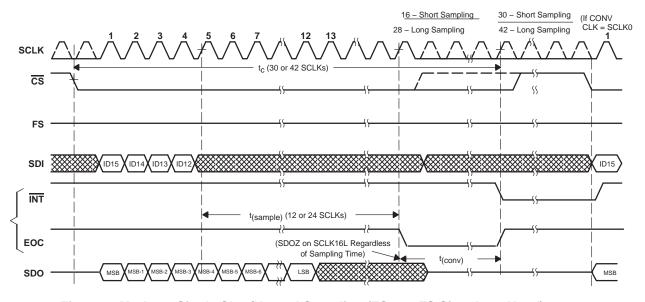
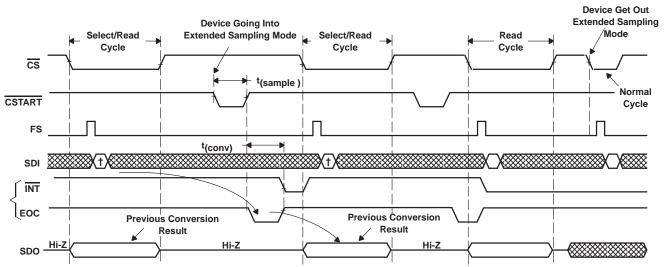


Figure 8. Mode 00 Single Shot/Normal Sampling (FS = 1, FS Signal not Used)



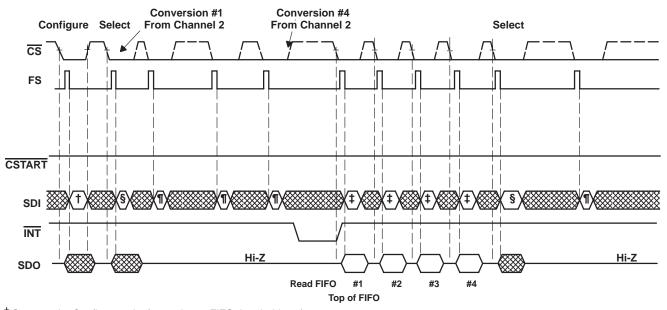
#### conversion cycles (continued)



<sup>&</sup>lt;sup>†</sup> This is one of the single shot commands. Conversion starts on next rising edge of CSTART.

Figure 9. Mode 00 Single Shot/Extended Sampling (FS Signal Used, FS Pin Connected to TMS320 DSP)

#### modes using the FIFO: modes 01, 10, 11 timing



<sup>†</sup>Command = Configure write for mode 01, FIFO threshold = 1/2

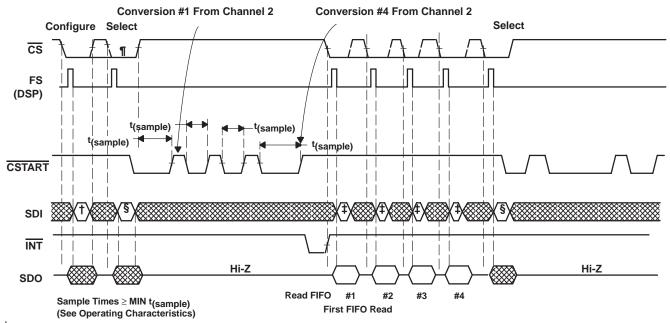
Figure 10. TLV2544/TLV2548 Mode 01 DSP Serial Interface (Conversions Triggered by FS)

<sup>‡</sup>Command = Read FIFO, first FIFO read

<sup>§</sup> Command = Select ch2.

<sup>¶</sup> Use any channel select command to trigger SDI input.

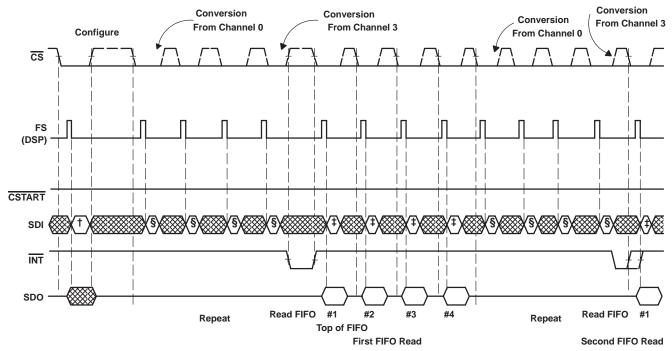
#### modes using the FIFO: modes 01, 10, 11 timing (continued)



<sup>†</sup> Command = Configure write for mode 01, FIFO threshold = 1/2

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Figure 11. TLV2544/TLV2548 Mode 01 μp/DSP Serial Interface (Conversions Triggered by CSTART)



<sup>†</sup> Command = Configure write for mode 10 or 11, FIFO threshold = 1/2, sweep seq = 0-1-2-3.

Figure 12. TLV2544/TLV2548 Mode 10/11 DSP Serial Interface (Conversions Triggered by FS)



<sup>‡</sup>Command = Read FIFO, first FIFO read

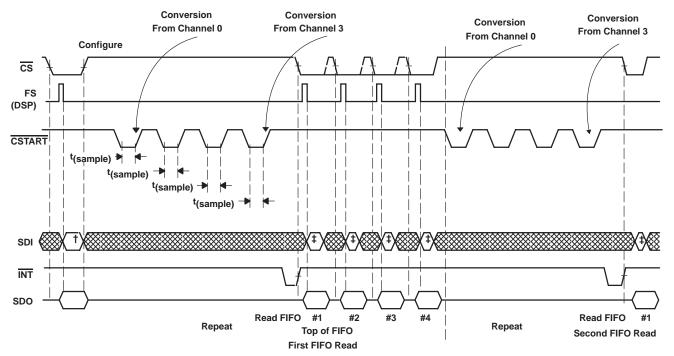
<sup>§</sup> Command = Select ch2.

Minimum  $\overline{CS}$  low time for select cycle is 6 SCLKs. The same amount of time is required between FS low to  $\overline{CSTART}$  for proper channel decoding. The low time of  $\overline{CSTART}$ , not overlapped with  $\overline{CS}$  low time, is the valid sampling time for the select cycle (see Figure 18).

<sup>‡</sup>Command = Read FIFO

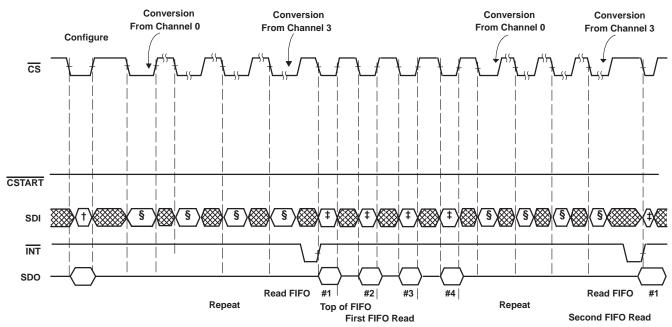
<sup>§</sup> Use any channel select command to trigger SDI input.

#### modes using the FIFO: modes 01, 10, 11 timing (continued)



<sup>†</sup> Command = Configure write for mode 10 or 11, FIFO threshold = 1/2, sweep seq = 0-1-2-3.

Figure 13. TLV2544/TLV2548 Mode 10/11 DSP Serial Interface (Conversions Triggered by CSTART)



<sup>†</sup>Command = Configure write for mode 10 or 11, FIFO threshold = 1/2, sweep seq = 0-1-2-3.

Figure 14. TLV2544/TLV2548 Mode 10/11 μp Serial Interface (Conversions Triggered by CS)

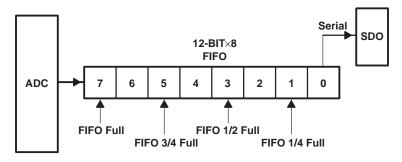


<sup>‡</sup>Command = Read FIFO

<sup>‡</sup>Command = Read FIFO

<sup>§</sup> Use any channel select command to trigger SDI input.

#### FIFO operation



**FIFO Threshold Pointer** 

Figure 15. TLV2544/TLV2548 FIFO

The device has an 8-layer FIFO that can be programmed for different thresholds. An interrupt is sent to the host after the preprogrammed threshold is reached. The FIFO can be used to store data from either a fixed channel or a series of channels based on a preprogrammed sweep sequence. For example, an application may require eight measurements from channel 3. In this case, the FIFO is filled with eight data sequentially taken from channel 3. Another application may require data from channel 0, channel 2, channel 4, and channel 6 in an orderly manner. Therefore, the threshold is set for 1/2 and the sweep sequence 0–2–4–6–0–2–4–6 is chosen. An interrupt is sent to the host as soon as all four data are in the FIFO.

In single shot mode, the FIFO automatically uses a 1/8 FIFO depth. Therefore the CFR bits (D1,0) controlling FIFO depth are *don't care*.

#### SCLK and conversion speed

There are two ways to adjust the conversion speed.

- The SCLK can be used as the source of the conversion clock to get the highest throughput of the device.
  - The minimum onboard OSC is 3.6 MHz and 14 conversion clocks are required to complete a conversion. (Corresponding 3.86  $\mu$ s conversion time) The devices can operate with an SCLK up to 20 MHz for the supply voltage range specified. When a more accurate conversion time is desired, the SCLK can be used as the source of the conversion clock. The clock divider provides speed options appropriate for an application where a high speed SCLK is used for faster I/O. The total conversion time is  $14 \times (DIV/f_{SCLK})$  where DIV is 1, 2, or 4. For example a 20 MHz SCLK with the divide by 4 option produces a  $\{14 \times (4/20 \text{ M})\} = 2.8 \text{ }\mu\text{s}$  conversion time. When an external serial clock (SCLK) is used as the source of the conversion clock, the maximum equivalent conversion clock ( $f_{SCLK}/DIV$ ) should not exceed 6 MHz.
- Autopower down can be used to slow down the device at a reduced power consumption level. This mode
  is always used by the converter. If the device is not accessed (by CS or CSTART), the converter is powered
  down to save power. The built-in reference is left on in order to quickly resume operation within one half
  SCLK period. This provides unlimited choices to trade speed with power savings.

#### reference voltage

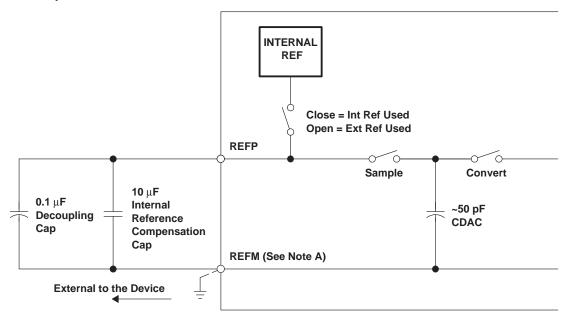
The device has a built-in reference with a programmable level of 2 V or 4 V. If the internal reference is used, REFP is set to 2 V or 4 V and REFM should be connected to the analog ground of the converter. An external reference can also be used through two reference input pins, REFP and REFM, if the reference source is programmed as external. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of REFP, REFM, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REFP and at zero when the input signal is equal to or lower than REFM.



#### 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOV

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#### reference block equivalent circuit



NOTES: A. If internal reference is used, tie REFM to analog ground and install a 10 μF (or 4.7 μF) internal reference compensation capacitor between REFP and REFM to store the charge as shown in the figure above.

- B. If external reference is used, the 10 μF (internal reference compensation) capacitor is optional. REFM can be connected to external REEM or AGND.
- C. Internal reference voltage drift, due to temperature variations, is approximately ±10 mV about the nominal 2 V (typically) from -10°C to 100°C. The nominal value also varies approximately ±50 mV across devices.
- D. Internal reference leakage during low ON time: Leakage resistance is on the order of 100 M $\Omega$  or more. This means the time constant is about 1000 s with 10 µF compensation capacitance. Since the REF voltage does not vary much, the reference comes up quickly after resuming from auto power down. At power up and power down the internal reference sees a glitch of about 500 µV when 2 V internal reference is used (1 mV when 4 V internal reference is used). This glitch settles out after about 50 µs.

#### power down

The device has three power-down modes.

#### autopower-down mode

The device enters the autopower-down state at the end of a conversion.

In autopower-down, the power consumption reduces to about 1 mA when an internal reference is selected. The built-in reference is still on to allow the device to resume quickly. The resumption is fast enough (within 0.5 SCLK) for use between cycles. An active  $\overline{CS}$ , FS, or  $\overline{CSTART}$  resumes the device from power-down state. The power current is 1 μA when an external reference is programmed and SCLK stops.

#### hardware/software power-down mode

Writing 8000h to the device puts the device into a software power down state, and the entire chip (including the built-in reference) is powered down. For a hardware power-down, the dedicated PWDN pin provides another way to power down the device asynchronously. These two power-down modes power down the entire device including the built-in reference to save power. The power down current is reduced to about 1 μA is the SCLK is stopped.

An active CS, FS, or CSTART restores the device. There is no time delay when an external reference is selected. However, if an internal reference is used, it takes about 20 ms to warm up. Deselect PWDN pin to remove the device from the hardware power-down state. This requires about 20 ms to warm up if an internal reference is also selected.

The configuration register is not affected by any of the power down modes but the sweep operation sequence has to be started over again. All FIFO contents are cleared by the power-down modes.



#### TLV2544, TLV2548 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN

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#### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, GND to V <sub>CC</sub>		
Analog input voltage range		
Reference input voltage		V <sub>CC</sub> + 0.3 V
Digital input voltage range		0.3 V to V <sub>CC</sub> + 0.3 V
Operating virtual junction temperature ran-	ge, T」	–55°C to 150°C
Operating free-air temperature range, T <sub>A</sub> :	TLV2544/48C	0°C to 70°C
	TLV2544/48I	–40°C to 85°C
Storage temperature range, T <sub>stq</sub>		
Lead temperature 1,6 mm (1/16 inch) from		

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### **DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C <sup>‡</sup>	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	1110 mW	8.9 mW/°C	710 mW	577 mW	222 mW
DW	1294 mW	10.4 mW/°C	828 mW	673 mW	259 mW
16 PW	839 mW	6.7 mW/°C	537 mW	437 mW	_
20 PW	977 mW	7.8 mW/°C	625 mW	508 mW	_

<sup>‡</sup> This is the inverse of the traditional junction-to-ambient thermal resistance (R<sub>OJA</sub>). Thermal resistance is not production tested and the values given are for informational purposes only.

#### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>		2.7	3.3	5.5	V
Analog input voltage (see Note 4)	0		Vcc	V	
High level control input voltage, VIH		2.1			V
Low-level control input voltage, V <sub>IL</sub>				0.6	V
Delay time, delay from CS falling edge to FS (See Figure 16)	0.5			SCLKs	
Delay time, delay time from 16th SCLK falling 17th rising edge (FS is active) t <sub>d</sub> (SCLK-CSH)	0.5			SCLKs	
Setup time, FS rising edge before SCLK fallin (See Figure 16)	g edge, t <sub>SU</sub> (FSH-SCLKL	20			ns
Hold time, FS hold high after SCLK falling ed	ge, th(FSH-SCLKL) (See Figure 16)	30			ns
Pulse width, CS high time, twH(CS) (See Figu	ures 16 and 19)	100			ns
Pulse width, FS high time, t <sub>WH</sub> (FS) (See Figu	0.75		1	SCLKs	
SCLK cycle time, t <sub>C</sub> (SCLK)	V <sub>CC</sub> = 2.7 V to 3.6 V	75		10000	
(See Figures 16, and 19)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{V}$	50		10000	ns

NOTE 4: When binary output format is used, analog input voltages greater than that applied to REFP convert as all ones (11111111111), while input voltages less than that applied to REFM convert as all zeros (000000000000). The device is functional with reference down to 1 V. (VREFP – VREFM – 1); however, the electrical specifications are no longer applicable.



# TLV2544, TLV2548 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN SLAS198E - FEBRUARY 1999 - REVISED JUNE 2003

#### recommended operating conditions (continued)

			MIN	NOM	MAX	UNIT
Pulse width, SCLK low time, twL(SCLK) (See Figur	0.4		0.6	SCLKs		
Pulse width, SCLK high time, twH(SCLK) (See Figure 1)	ures 16 and 19)		0.4		0.6	SCLKs
Setup time, SDI valid before falling edge of SCLK (SCLK (FS=1), $t_{SU(DI-SCLK}$ (See Figures 16 and 19	25			ns		
Hold time, SDI hold valid after falling edge of SCLK of SCLK (FS=1), $t_{h(DI-SCLK)}$ (See Figure 16)	,	the rising edge	5			ns
Delay time, delay from CS falling edge to SDO valid (See Figures 16 and 19)	d, td(CSL-DOV)				25	ns
Delay time, delay from FS falling edge to SDO valid	d, td(FSL-DOV) (	See Figure 16)			25	ns
	V 45V	SDO = 5 pF	0.5 SCLK		0.5 SCLK + 9	
Delay time, delay from SCLK falling edge (FS is active) or SCLK rising edge (FS=1) to SDO valid,	V <sub>CC</sub> = 4.5 V	SDO = 25 pF	0.5 SCLK		0.5 SCLK + 10	
SCLK-DOV). (See Figures 16 and 19). r a date code later than xxx, see the date code ormation item (3).	V 0.7V	SDO = 5 pF	0.5 SCLK		0.5 SCLK + 18	ns
( )	V <sub>CC</sub> = 2.7 V	SDO = 25 pF	0.5 SCLK		0.5 SCLK + 19	
Delay time, delay from 17th SCLK rising edge (FS (FS=1) to EOC falling edge, t <sub>d</sub> (SCLK-EOCL) (See				45		ns
Delay time, delay from 16th SCLK falling edge to IN the 17th rising edge SCLK to INT falling edge (whe (See Figure 19)			Min t <sub>(conv)</sub>			μs
Delay time, delay from CS falling edge or FS rising td(CSL-INTH) or td(FSH-INTH). See Figures 16, 17	7, 18 and 19)		1		50	ns
Delay time, delay from CS rising edge to CSTART (See Figures 17 and 18)	falling edge, t <sub>d(C</sub>	SH-CSTARTL)	100			ns
Delay time, delay from CSTART rising edge to EOC (See Figures 17 and 18)	falling edge, t <sub>d(C</sub>	STARTH-EOCL)	1		50	ns
Pulse width, CSTART low time, t <sub>WL</sub> (CSTART) (See	Min t(sample)			μs		
Delay time, delay from CSTART rising edge to CST td(CSTARTH-CSTARTL) (See Figure 18)	Max t <sub>(conv)</sub>			μs		
Delay time, delay from CSTART rising edge to INT (See Figures 17 and 18)		Max t <sub>(conv)</sub>		μs		
Operating free air temperature T.	TLV2544C/TLV	/2548C	0		70	°C
Operating free-air temperature, T <sub>A</sub>	TLV2544I/TLV2	2548I	-40		85	~C

## TLV2544, TLV2548 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN SLAS198E - FEBRUARY 1999 - REVISED JUNE 2003

#### electrical characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = V<sub>REFP</sub> = 2.7 V to 5.5 V, V<sub>REFM</sub> = 0 V, SCLK frequency = 20 MHz at 5 V, 15 MHz at 3 V (unless otherwise noted)

	PARAMETER	TEST C	MIN	TYP†	MAX	UNIT	
.,		$V_{CC} = 5.5 \text{ V}, I_{OH} = -$	0.2 mA at 25 pF load	2.4			.,
$V_{OH}$	High-level output voltage	$V_{CC} = 2.7 \text{ V}, I_{OH} = -2.2 \text{ V}$	20 μA at 25 pF load	V <sub>CC</sub> -0.2			V
.,		$V_{CC} = 5.5 \text{ V}, I_{OL} = 0$	.8 mA at 25 pF load			0.4	.,
$V_{OL}$	Low-level output voltage	$V_{CC} = 2.7 \text{ V}, I_{OL} = 20$	0 μA at 25 pF load			0.1	V
I <sub>OZ</sub>	Off-state output current (high-impedance-state)	$V_O = V_{CC}$	CS = V <sub>CC</sub>		1	2.5	μΑ
l <sub>OZ</sub>	Off-state output current (high-impedance-state)	V <sub>O</sub> = 0	CS = V <sub>CC</sub>	-2.5	-1		μΑ
I <sub>IH</sub>	High-level input current	$V_I = V_{CC}$	·		0.005	2.5	μА
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0 V			-0.005	2.5	μΑ
		00 -1 0 V Frd (	V <sub>CC</sub> = 4.5 V to 5.5 V			1.1	
I <sub>CC</sub>	Operating supply current, normal	CS at 0 V, Ext ref	V <sub>CC</sub> = 2.7 V to 3.3 V			1	mA
	short sampling	CS at 0 V, Int ref	V <sub>CC</sub> = 4.5 V to 5.5 V			2.1	
		CS at 0 V, Int rer	$V_{CC} = 2.7 \text{ V to } 3.3 \text{ V}$			1.6	mA
		<del></del>	V <sub>CC</sub> = 4.5 V to 5.5 V	1.1			
	Operating supply current, extended	CS at 0 V, Ext ref	$V_{CC} = 2.7 \text{ V to } 3.3 \text{ V}$		1		mA
	sampling	CS at 0 V, Int ref	V <sub>CC</sub> = 4.5 V to 5.5 V		2.1		4
		$V_{CC} = 2.7 \text{ V to } 3.3 \text{ V}$			1.6		mA
1	Power down supply current for all digital inputs,	$V_{CC}$ = 4.5 V to 5.5 V, Ext clock			0.1	1	^
I <sub>CC(PD)</sub>	$0 \le V_1 \le 0.3 \text{ V or}$ $V_1 \ge V_{CC} - 0.3 \text{ V}, \text{ SCLK} = 0$	$V_{CC} = 2.7 \text{ V to } 3.3 \text{ V},$	Ext clock		0.1	1	μΑ
	Auto power-down current for all	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	Ext clock, Ext ref			1‡	
I <sub>CC(AUTOPWDN)</sub>	digital inputs, $0 \le V_1 \le 0.3 \text{ V}$ or $V_1 \ge V_{CC} - 0.3 \text{ V}$ , SCLK = 0	$V_{CC} = 2.7 \text{ V to } 3.3 \text{ V},$	Ext ref, Ext clock			1.0§	μΑ
	Octobrillo to the control of the con	Selected channel at '	Vcc			1	•
	Selected channel leakage current	Selected channel at	0 V			1	μΑ
	Maximum static analog reference current into REFP (use external reference)	V <sub>REFP</sub> = V <sub>CC</sub> = 5.5 V	, V <sub>REFM</sub> = GND		1		μΑ
C	Input conscitones	Analog inputs			45	50	۲,
C <sub>i</sub>	Input capacitance	Control Inputs		5	25	pF	
7	Input MLIV ON registeres	V <sub>CC</sub> = 4.5 V			500	0	
Z <sub>i</sub>	Input MUX ON resistance	V <sub>CC</sub> = 2.7 V			600	Ω	

 $<sup>\</sup>uparrow$  All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

 $<sup>\</sup>ddagger$  1.2 mA if internal reference is used, 165  $\mu$ A if internal clock is used.

 $<sup>\</sup>S\,0.8$  mA if internal reference is used, 116  $\dot{\mu}A$  if internal clock is used.

#### TLV2544, TLV2548 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN

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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = V_{REFP} = 2.7 \text{ V}$  to 5.5 V,  $V_{REFM} = 0$  V, SCLK frequency = 20 MHz at 5 V, 15 MHz at 3 V (unless otherwise noted) (continued)

#### ac specifications

	PARAMETER	TEST CO	MIN	TYP	MAX	UNIT	
SINAD	Signal-to-noise ratio +distortion	f <sub>I</sub> = 12 kHz at 200 KSPS	C and I suffix	69	70		dB
THD	Total harmonic distortion	f <sub>I</sub> = 12 kHz at 200 KSPS		-82	-76	dB	
ENOB	Effective number of bits	f <sub>I</sub> = 12 kHz at 200 KSPS		11.6		Bits	
SFDR	Spurious free dynamic range	f <sub>I</sub> = 12 kHz at 200 KSPS	f <sub>I</sub> = 12 kHz at 200 KSPS				
Analog	input						
	Full power-bandwidth, -3 dB				1		MHz
	Full-power bandwidth, -1 dB			500		kHz	

#### reference specifications† (0.1 $\mu$ F and 10 $\mu$ F between REFP and REFM pins)

PARAMETER	TE	EST CONDITIONS	MIN	TYP	MAX	UNIT
Positive reference input voltage, REFP	$V_{CC} = 2.7 \text{ V to } 5.8$	2		Vcc	V	
Negative reference input voltage, REFM	$V_{CC} = 2.7 \text{ V to } 5.8$	5 V	0		2	V
	.,	CS = 1, SCLK = 0, (off)	100			MΩ
Reference Input impedance	V <sub>CC</sub> = 5.5 V	CS = 0, SCLK = 20 MHz (on)	20	25		kΩ
	V 07V	CS = 1, SCLK = 0 (off)	100			MΩ
	$V_{CC} = 2.7 \text{ V}$	CS = 0, SCLK = 15 MHz (on)	20	25		kΩ
Reference Input voltage difference, REFP-REFM	$V_{CC} = 2.7 \text{ V to } 5.8$	5 V	2		Vcc	V
	V <sub>CC</sub> = 5.5 V	VREF SELECT = 4 V	3.85	4	4.15	V
Internal reference voltage, REFP-REFM	V <sub>CC</sub> = 5.5 V	VREF SELECT = 2 V	1.925	2	2.075	V
	$V_{CC} = 2.7 \text{ V}$	1.925	2	2.075	V	
Internal reference start-up time	V <sub>CC</sub> = 5.5 V, 2.7 V with 10 μF compensation cap			20		ms
Internal reference temperature coefficient	V <sub>CC</sub> = 2.7 V to 5.	V <sub>CC</sub> = 2.7 V to 5.5 V				PPM/°C

<sup>†</sup> Specified by design

## TLV2544, TLV2548 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN

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### operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REFP} = 2.7 \text{ V}$ to 5.5 V, $V_{REFM} = 0 \text{ V}$ , SCLK frequency = 20 MHz at 5 V, 15 MHz at 3 V (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
EL	Integral linearity error (INL)	(see Note 6)				±1	LSB
ED	Differential linearity error (I	DNL)	See Note 5			±1	LSB
EO	Offset error (see Note 7)		See Note 5			±2.5	LSB
E <sub>FS</sub>	Full scale error (see Note 7	7)	See Note 5	-1.6		+3.5	LSB
			SDI = B000h		800h (2048D)		
	Self-test output code (see Note 8)	Table 1 and	SDI = C000h		000h (0D)		
			SDI = D000h		FFFh (4095D)		
		Internal OSC		2.33	3.5	3.86	
<sup>t</sup> (conv)	Conversion time External SCLK				(14 × DIV) fSCLK		μs
t(sample)	Sampling time	•	With a maximum of $1-k\Omega$ input source impedance	600			ns

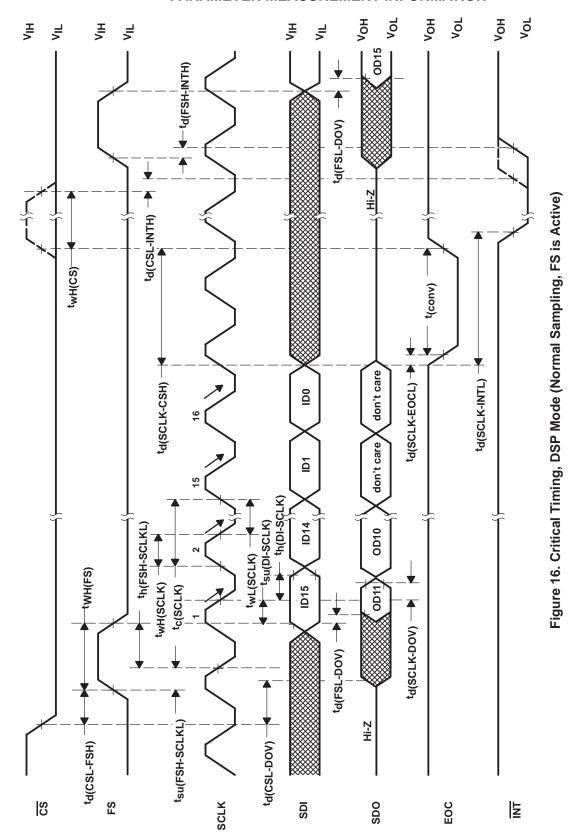
<sup>†</sup> All typical values are at  $T_A = 25$ °C.

NOTES: 5. Analog input voltages greater than that applied to REFP convert as all ones (111111111111), while input voltages less than that applied to REFM convert as all zeros (000000000000).

- 6. Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.
- 7. Zero error is the difference between 000000000000 and the converted output for zero input voltage: full-scale error is the difference between 11111111111 and the converted output for full-scale input voltage.
- 8. Both the input data and the output codes are expressed in positive logic.

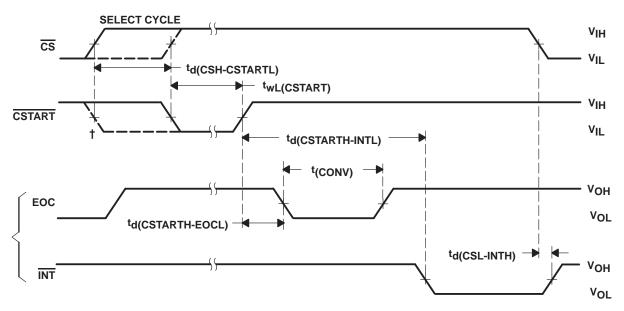


#### PARAMETER MEASUREMENT INFORMATION



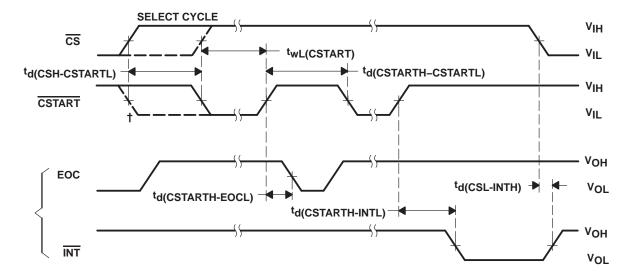


#### PARAMETER MEASUREMENT INFORMATION



<sup>†</sup>CSTART falling edge may come before the rising edge of CS but no sooner than the fifth SCLK of the SELECT CYCLE.

Figure 17. Critical Timing (Extended Sampling, Single Shot)

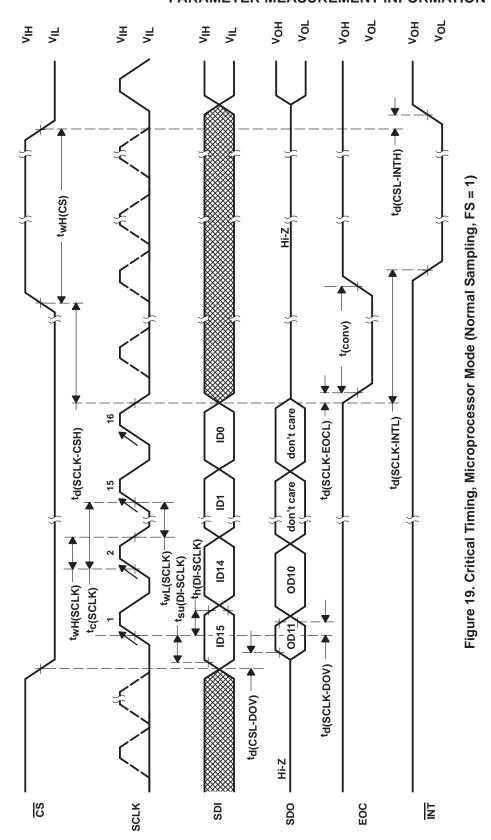


<sup>†</sup> CSTART falling edge may come before the rising edge of  $\overline{\text{CS}}$  but no sooner than the fifth SCLK of the SELECT CYCLE. In this case, the actual sampling time is measured from the rising edge  $\overline{\text{CS}}$  to the rising edge of  $\overline{\text{CSTART}}$ .

Figure 18. Critical Timing (Extended Sampling, Repeat/Sweep/Repeat Sweep)



#### PARAMETER MEASUREMENT INFORMATION





#### TYPICAL CHARACTERISTICS

#### INTEGRAL NONLINEARITY **TEMPERATURE** 0.53 0.52 INL - Integral Nonlinearity - LSB 0.51 0.5 0.49 V<sub>CC</sub> = 2.7 V, Internal Reference = 2 V, Internal Oscillator, Single Shot, Short Sample, Mode 00 µP Mode 0.48 25 41.25 57.5 73.75 90 -40 -23.75 -7.5 8.75 T<sub>A</sub> - Temperature - °C



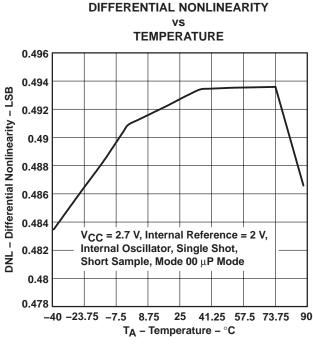


Figure 22

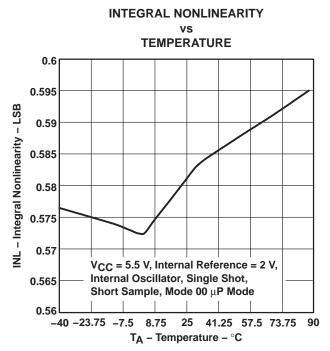


Figure 21

#### **DIFFERENTIAL NONLINEARITY**

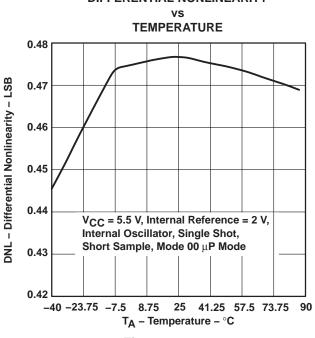


Figure 23

#### TYPICAL CHARACTERISTICS

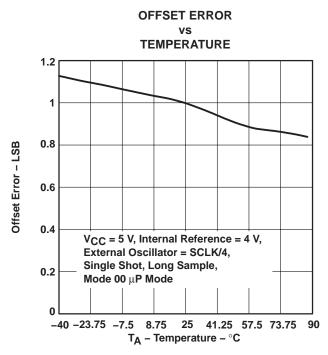


Figure 24

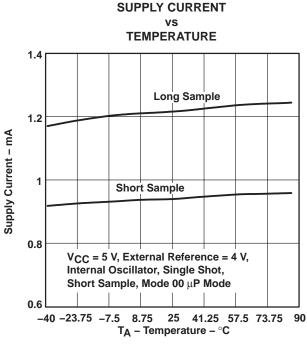


Figure 26

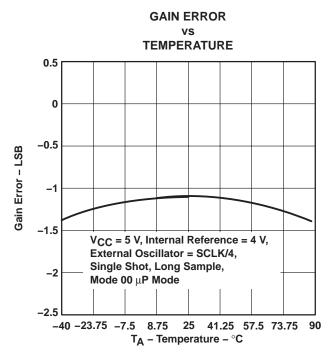


Figure 25

#### POWER DOWN CURRENT vs TEMPERATURE

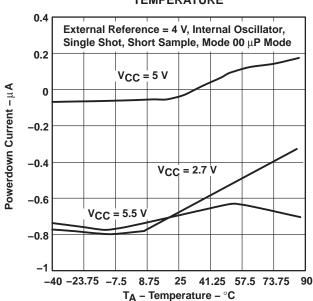


Figure 27

#### TYPICAL CHARACTERISTICS

#### INTEGRAL NONLINEARITY

٧S **SAMPLES** 

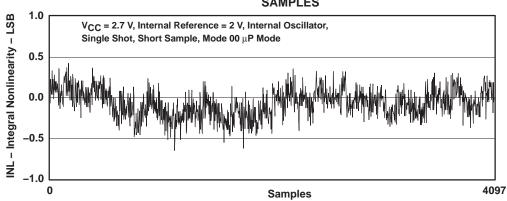


Figure 28

#### **DIFFERENTIAL NONLINEARITY**

٧S

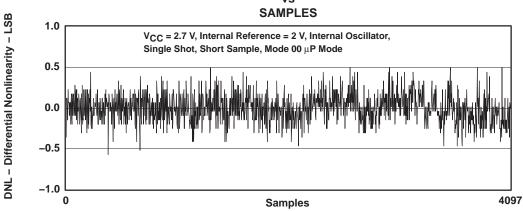


Figure 29

#### INTEGRAL NONLINEARITY

vs **SAMPLES** 

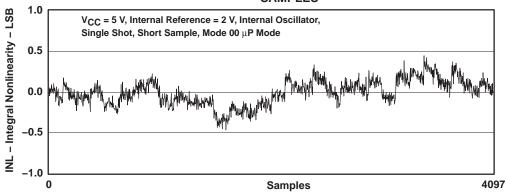


Figure 30



#### **TYPICAL CHARACTERISTICS**

### DIFFERENTIAL NONLINEARITY vs

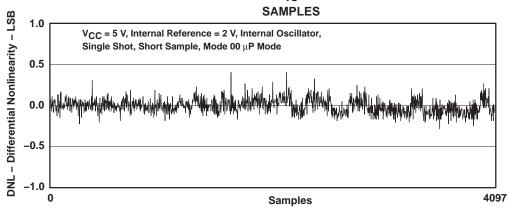


Figure 31

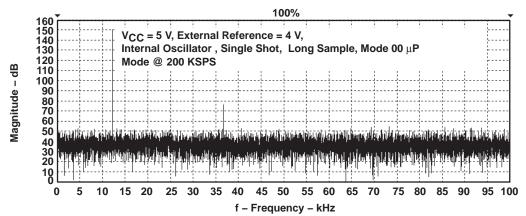
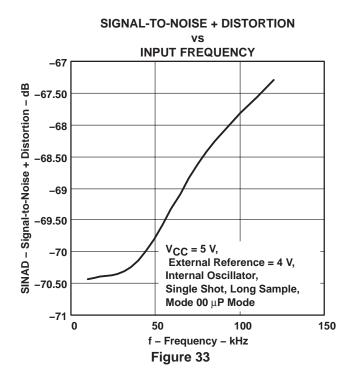
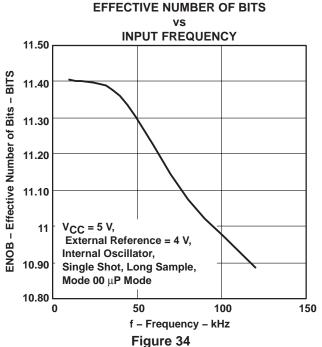


Figure 32

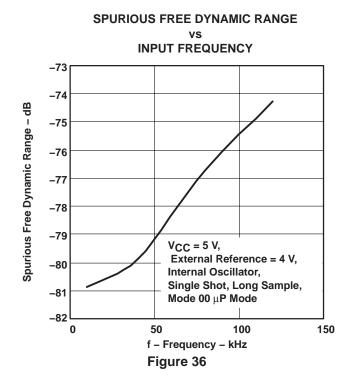


#### TYPICAL CHARACTERISTICS





#### TOTAL HARMONIC DISTORTION **INPUT FREQUENCY** -69 -70 THD - Total Harmonic Distortion - dB -71 -72 -73 -74 -75 -76 $V_{CC} = 5 V$ External Reference = 4 V, -77 Internal Oscillator, Single Shot, Long Sample, -78 Mode 00 µP Mode 0 50 100 150 f - Frequency - kHz Figure 35



#### **TYPICAL CHARACTERISTICS**

#### SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

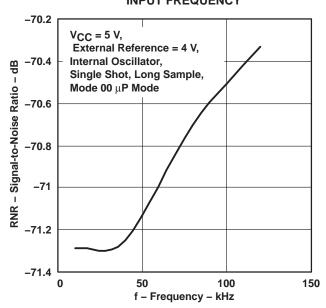


Figure 37

#### PRINCIPLES OF OPERATION

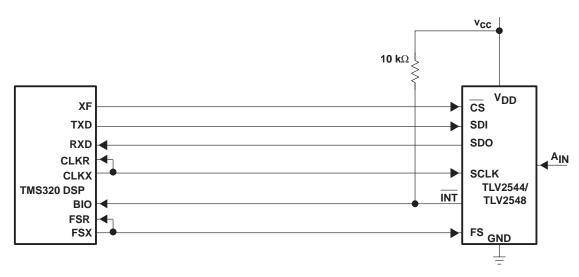


Figure 38. Typical Interface to a TMS320 DSP™



#### TLV2544, TLV2548 2.7-V TO 5.5-V, 12-BIT, 200-KSPS, 4-/8-CHANNEL, LOW-POWER SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER-DOWN

SLAS198E - FEBRUARY 1999 - REVISED JUNE 2003

#### DATA CODE INFORMATION

Parts with a date code earlier than 31xxxxx have the following discrepancies:

- 1. Earlier devices react to FS input irrespective of the state of the  $\overline{\text{CS}}$  signal
- 2. The earlier silicon was designed with SDO prereleased half clock ahead. This means in the microcontroller mode (FS=1) the SDO is changed on the rising edge of SCLK with a delay; and for DSP serial port (when FS is active) the SDO is changed on the falling edge of SCLK with a delay. This helps the setup time for processor input data, but may reduce the hold time for processor input data. It is recommended that a 100 pF capacitance be added to the SDO line of the ADC when interfacing with a slower processor that requires longer input data hold time.
- 3. For earlier silicon, the delay time is specified as:

			MIN	NOM	MAX	UNIT
	V 45V	SDO = 0 pF	16			
Delay time, delay from SCLK falling edge (FS is active) or	$V_{CC} = 4.5 \text{ V}$	SDO = 100 pF	20			
SCLK rising edge (FS=1) to next SDO valid, $t_{d(SCLK-DOV)}$	07.1/	SDO = 0 pF	24			ns
	$V_{CC} = 2.7 \text{ V}$	SDO = 100 pF	30			

This is because the SDO is changed at the rising edge in the up mode with a delay. This is the hold time required by the external digital host processor, therefore, a minimum value is specified. The newer silicon has been revised with SDO changed at the falling edge in the up mode with a delay. Since at least 0.5 SCLK exists as the hold time for the external host processor, the specified maximum value helps with the calculation of the setup time requirement of the external digital host processor.

For an explanation of the DSP mode, reverse the rising/falling edges in item (2) above.







10-Jun-2014

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2544CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2544C	Samples
TLV2544CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2544C	Samples
TLV2544CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2544	Samples
TLV2544CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2544	Samples
TLV2544ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	25441	Samples
TLV2544IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	25441	Samples
TLV2544IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	25441	Samples
TLV2544IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2544	Samples
TLV2544IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2544	Samples
TLV2544IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2544	Samples
TLV2548CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2548C	Samples
TLV2548CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2548C	Samples
TLV2548CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2548C	Samples
TLV2548CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2548C	Samples
TLV2548CPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2548	Samples
TLV2548CPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2548	Samples
TLV2548CPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2548	Samples



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#### PACKAGE OPTION ADDENDUM

10-Jun-2014

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TLV2548CPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2548	Samples
TLV2548IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2548I	Samples
TLV2548IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2548I	Samples
TLV2548IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2548I	Samples
TLV2548IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2548	Samples
TLV2548IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2548	Samples
TLV2548IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2548	Samples
TLV2548IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2548	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



### PACKAGE OPTION ADDENDUM

10-Jun-2014

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF TLV2548:

■ Enhanced Product: TLV2548-EP

Military: TLV2548M

NOTE: Qualified Version Definitions:

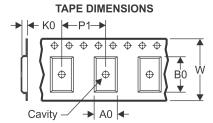
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

### PACKAGE MATERIALS INFORMATION

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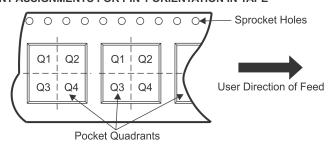
### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2544CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2544CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2544IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2544IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2548CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV2548CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV2548IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV2548IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TLV2544CDR	SOIC	D	16	2500	367.0	367.0	38.0	
TLV2544CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0	
TLV2544IDR	SOIC	D	16	2500	367.0	367.0	38.0	
TLV2544IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0	
TLV2548CDWR	SOIC	DW	20	2000	367.0	367.0	45.0	
TLV2548CPWR	TSSOP	PW	20	2000	367.0	367.0	38.0	
TLV2548IDWR	SOIC	DW	20	2000	367.0	367.0	45.0	
TLV2548IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0	

DW (R-PDSO-G20)

### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



# DW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

### PLASTIC SMALL OUTLINE

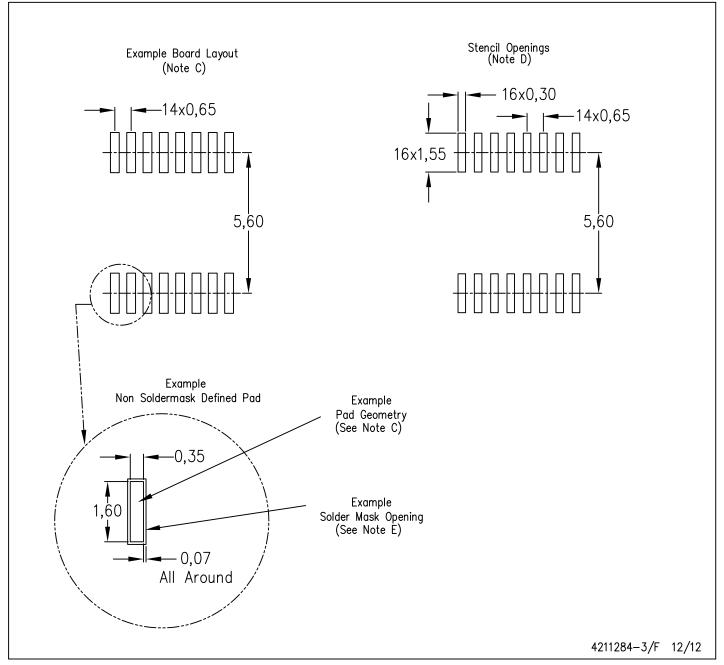


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G20)

### PLASTIC SMALL OUTLINE

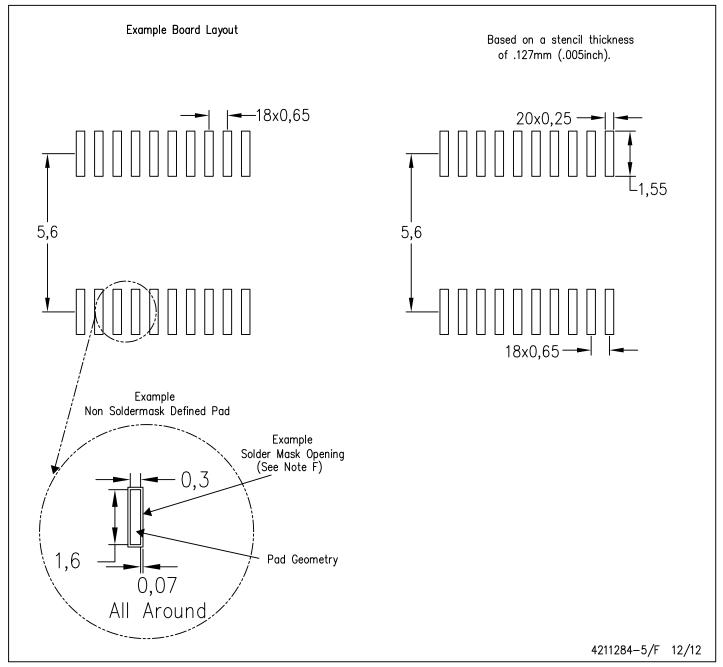


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

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- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
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- Тестирование поставляемой продукции.
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- Изготовление тестовой платы монтаж и пусконаладочные работы.



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