IS43/46R16800E, IS43/46R32400E

4Mx32, 8Mx16
128Mb DDR SDRAM

FEATURES

- VDD and VDDQ: 2.5V ± 0.2V (-5,-6)
- VDD and VDDQ: 2.5V ± 0.1V (-4)
- SSTL_2 compatible I/O
- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs and centre-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data Mask for write data. DM masks write data at both rising and falling edges of data strobe
- Burst Length: 2, 4 and 8
- Burst Type: Sequential and Interleave mode
- Programmable CAS latency: 2, 2.5, 3, and 4
- Auto Refresh and Self Refresh Modes
- Auto Precharge
- T_{RAS} Lockout supported ($t_{RAP} = t_{RCD}$)

OPTIONS

- Configuration(s): 4Mx32, 8Mx16
- Package(s):
  144 Ball BGA (x32)
  66-pin TSOP-II (x16) and 60 Ball BGA (x16)
- Lead-free package available
- Temperature Range:
  Commercial (0°C to +70°C)
  Industrial (-40°C to +85°C)
  Automotive, A1 (-40°C to +85°C)
  Automotive, A2 (-40°C to +105°C)

DEVICE OVERVIEW

ISSI's 128-Mbit DDR SDRAM achieves high speed data transfer using pipeline architecture and two data word accesses per clock cycle. The 134,217,728-bit memory array is internally organized as four banks of 32Mb to allow concurrent operations. The pipeline allows Read and Write burst accesses to be virtually continuous, with the option to concatenate or truncate the bursts. The programmable features of burst length, burst sequence and CAS latency enable further advantages. The device is available in 16-bit and 32-bit data word size Input data is registered on the I/O pins on both edges of Data Strobe signal(s), while output data is referenced to both edges of Data Strobe and both edges of CLK. Commands are registered on the positive edges of CLK.

An Auto Refresh mode is provided, along with a Self Refresh mode. All I/Os are SSTL_2 compatible.

ADDRESS TABLE

Parameter	4M x 32	8M x 16
Configuration	1M x 32 x 4 banks	2M x 16 x 4 banks
Bank Address Pins	BA0, BA1	BA0, BA1
Autoprecharge Pins	A8/AP	A10/AP
Row Address	4K(A0 – A11)	4K(A0 – A11)
Column Address	256(A0 – A7)	512(A0 – A8)
Refresh Count Com./Ind./A1 A2	4K / 64ms 4K / 16ms	4K / 64ms 4K / 16ms

KEY TIMING PARAMETERS

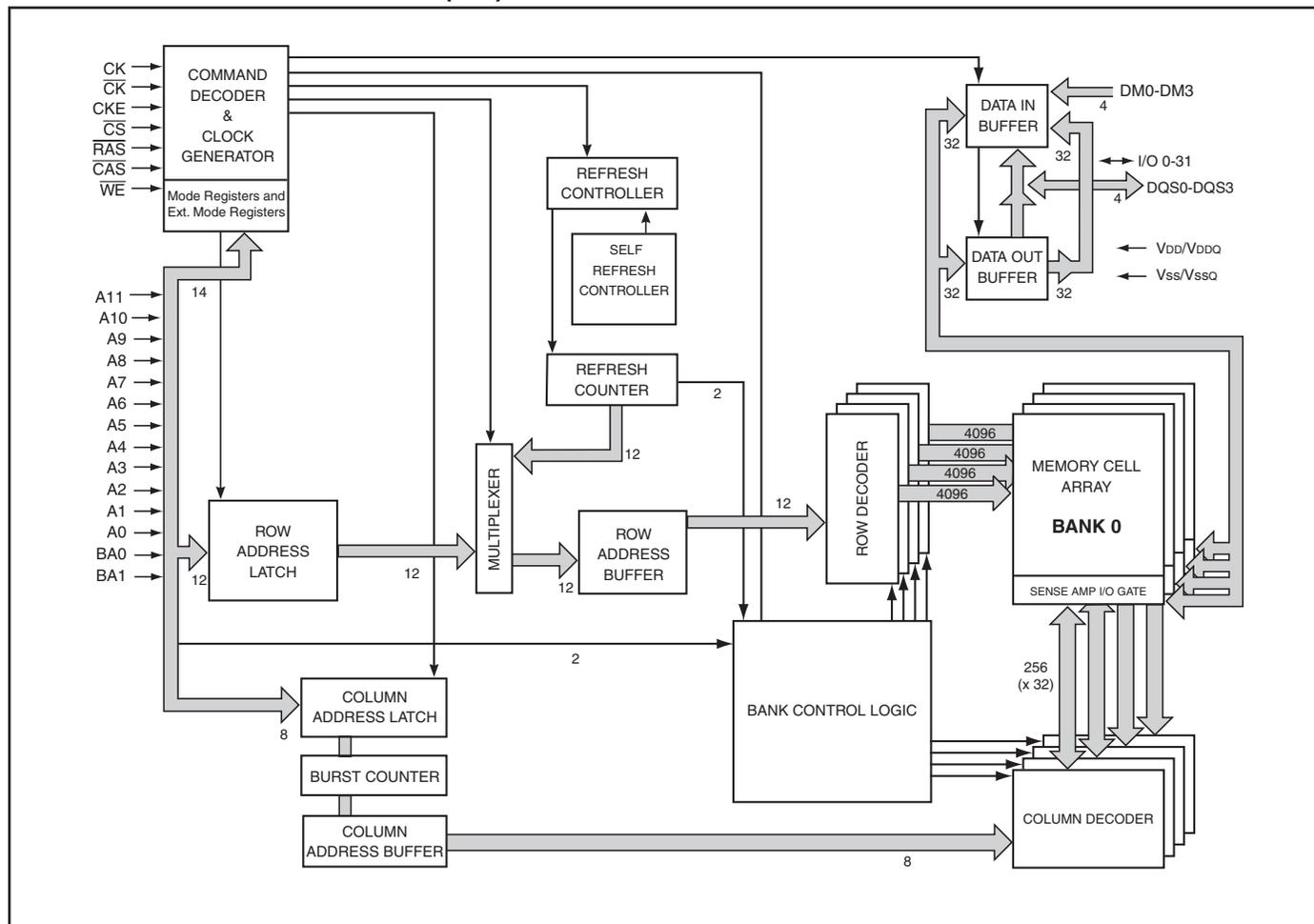| Speed Grade	-4	-5	-6	Units
F_{CK} Max CL = 4	250	—	—	MHz
F_{CK} Max CL = 3	200	200	167	MHz
F_{CK} Max CL = 2.5	—	167	167	MHz
F_{CK} Max CL = 2	—	133	133	MHz

FUNCTIONAL BLOCK DIAGRAM (x32)

FUNCTIONAL BLOCK DIAGRAM (x16)
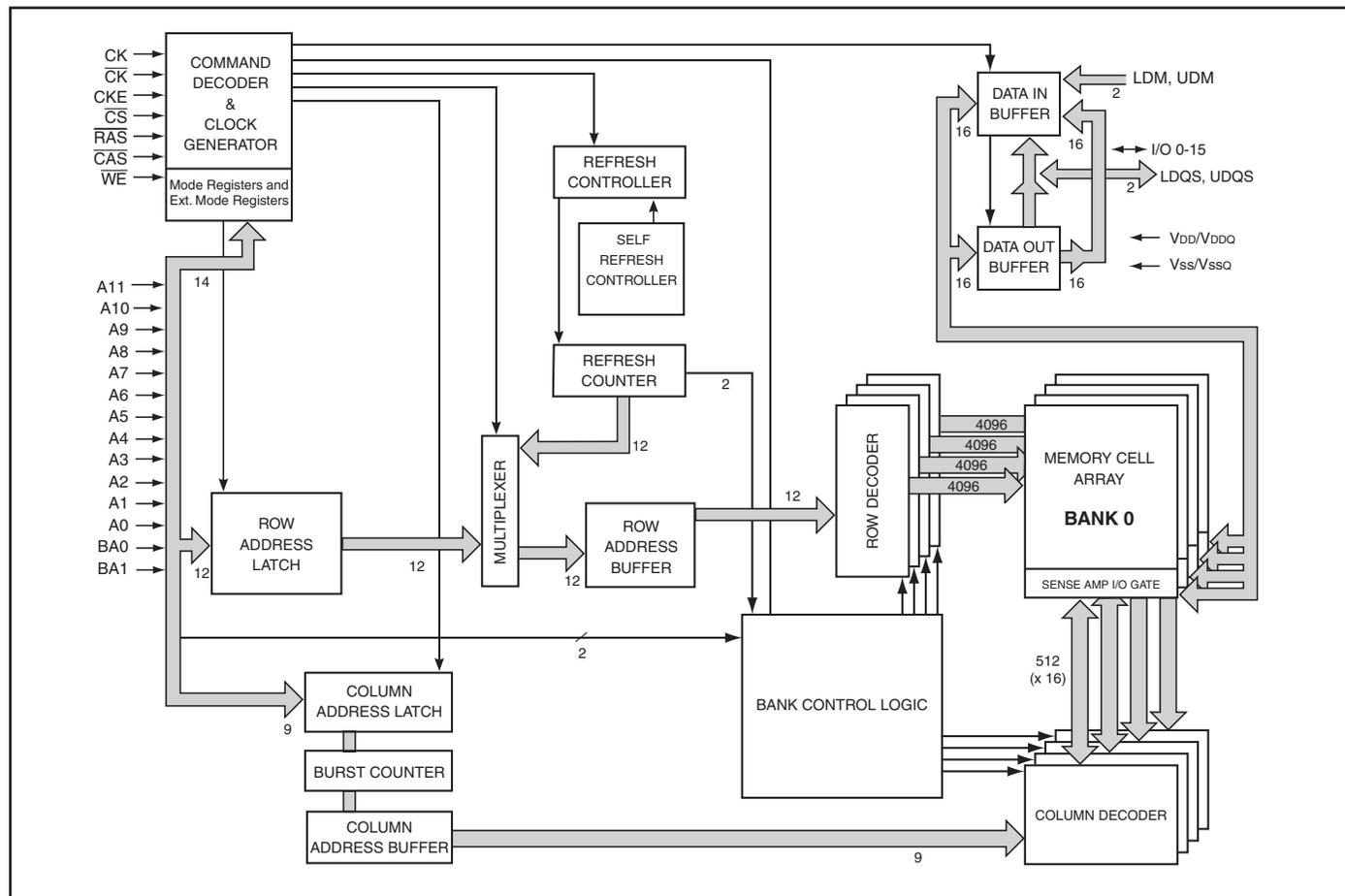
IS43/46R16800E, IS43/46R32400E

PIN CONFIGURATIONS
66 pin TSOP - Type II for x16

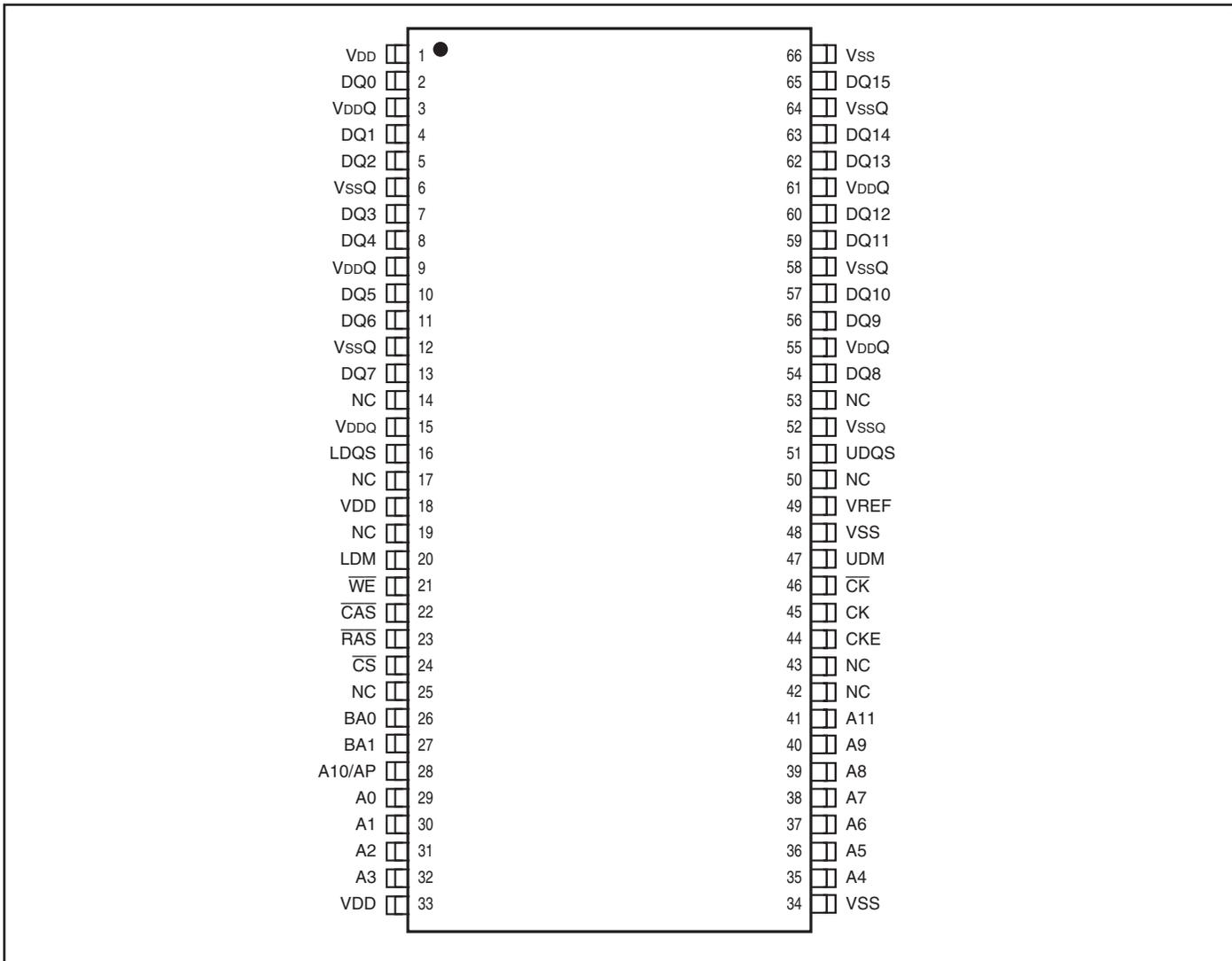| Left Pin	#		#	Right Pin
V$_{DD}$	1		66	V$_{SS}$
DQ0	2		65	DQ15
V$_{DDQ}$	3		64	V$_{SSQ}$
DQ1	4		63	DQ14
DQ2	5		62	DQ13
V$_{SSQ}$	6		61	V$_{DDQ}$
DQ3	7		60	DQ12
DQ4	8		59	DQ11
V$_{DDQ}$	9		58	V$_{SSQ}$
DQ5	10		57	DQ10
DQ6	11		56	DQ9
V$_{SSQ}$	12		55	V$_{DDQ}$
DQ7	13		54	DQ8
NC	14		53	NC
V$_{DDQ}$	15		52	V$_{SSQ}$
LDQS	16		51	UDQS
NC	17		50	NC
VDD	18		49	VREF
NC	19		48	VSS
LDM	20		47	UDM
$\overline{WE}$	21		46	$\overline{CK}$
$\overline{CAS}$	22		45	CK
$\overline{RAS}$	23		44	CKE
$\overline{CS}$	24		43	NC
NC	25		42	NC
BA0	26		41	A11
BA1	27		40	A9
A10/AP	28		39	A8
A0	29		38	A7
A1	30		37	A6
A2	31		36	A5
A3	32		35	A4
VDD	33		34	VSS

PIN DESCRIPTION: x16

A0-A11	Row Address Input
A0-A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0 – DQ15	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe Command
$\overline{RAS}$	Row Address Strobe Command
$\overline{WE}$	Write Enable

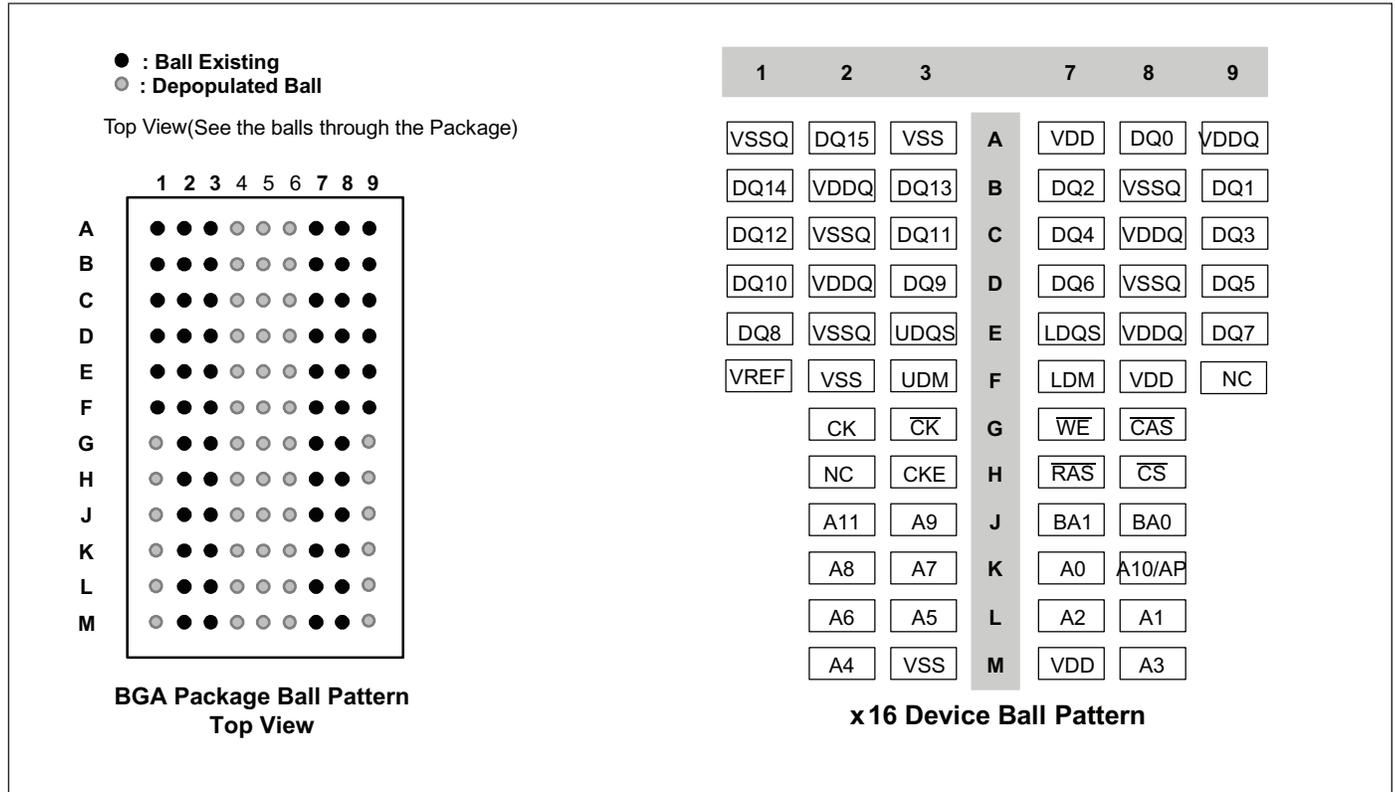|	
LDM, UDM	Data Write Mask
LDQS, UDQS	Data Strobe
VDD	Power
VDDQ	Power Supply for I/O Pins
VSS	Ground
VSSQ	Ground for I/O Pins
VREF	SSTL_2 reference voltage
NC	No Connection

PIN CONFIGURATION

Package Code B: 60-ball FBGA (top view) for x16

(8mm x 13mm Body, 0.8mm Ball Pitch)

Top View

(Balls seen through the Package)

● : Ball Existing
● : Depopulated Ball

Top View(See the balls through the Package)

**BGA Package Ball Pattern
Top View**

	1	2	3		7	8	9
A	VSSQ	DQ15	VSS		VDD	DQ0	VDDQ
B	DQ14	VDDQ	DQ13		DQ2	VSSQ	DQ1
C	DQ12	VSSQ	DQ11		DQ4	VDDQ	DQ3
D	DQ10	VDDQ	DQ9		DQ6	VSSQ	DQ5
E	DQ8	VSSQ	UDQS		LDQS	VDDQ	DQ7
F	VREF	VSS	UDM		LDM	VDD	NC
G	CK	$\overline{CK}$			$\overline{WE}$	$\overline{CAS}$	
H	NC	CKE			$\overline{RAS}$	$\overline{CS}$	
J	A11	A9			BA1	BA0	
K	A8	A7			A0	A10/AP	
L	A6	A5			A2	A1	
M	A4	VSS			VDD	A3	

x16 Device Ball Pattern

PIN DESCRIPTION: x16

A0-A11	Row Address Input
A0-A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0 – DQ15	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe Command
$\overline{RAS}$	Row Address Strobe Command
$\overline{WE}$	Write Enable
LDM, UDM	Data Write Mask

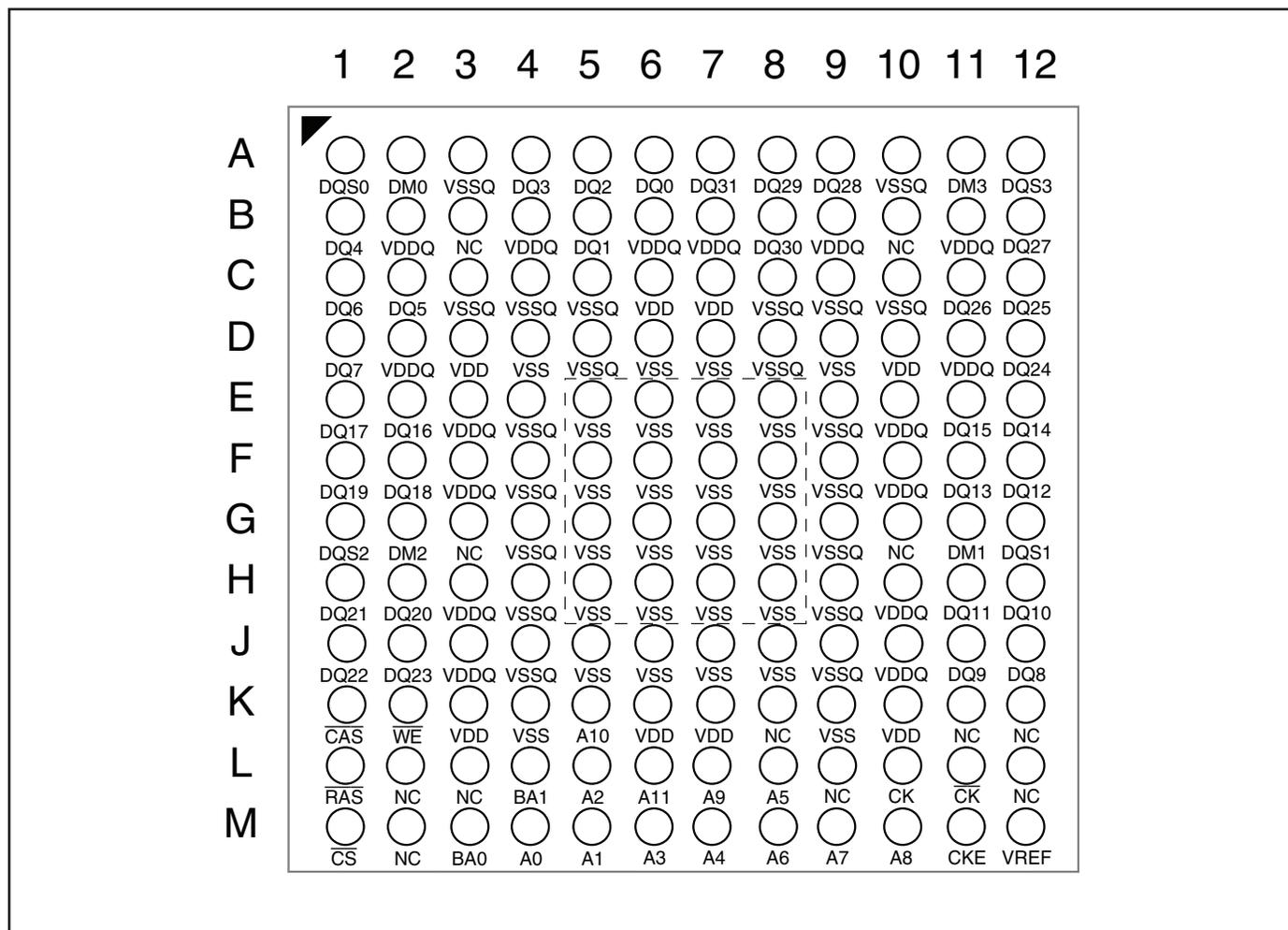|	
LDQS, UDQS	Data Strobe
VDD	Power
VDDQ	Power Supply for I/O Pins
VSS	Ground
VSSQ	Ground for I/O Pins
VREF	SSTL_2 reference voltage
NC	No Connection

PIN CONFIGURATION
Package Code B: 144-ball FBGA (top view)

(12mm x 12mm Body, 0.8mm Ball Pitch)

Top View (Balls seen through the package)

	1	2	3	4	5	6	7	8	9	10	11	12
A	DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3
B	DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27
C	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
D	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
E	DQ17	DQ16	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ15	DQ14
F	DQ19	DQ18	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ13	DQ12
G	DQS2	DM2	NC	VSSQ	VSS	VSS	VSS	VSS	VSSQ	NC	DM1	DQS1
H	DQ21	DQ20	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ11	DQ10
J	DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8
K	$\overline{CAS}$	$\overline{WE}$	VDD	VSS	A10	VDD	VDD	NC	VSS	VDD	NC	NC
L	$\overline{RAS}$	NC	NC	BA1	A2	A11	A9	A5	NC	CK	$\overline{CK}$	NC
M	$\overline{CS}$	NC	BA0	A0	A1	A3	A4	A6	A7	A8	CKE	VREF

Note: Vss balls inside the dotted box are optional for purposes of thermal dissipation.

PIN DESCRIPTION: for x32

A0-A11	Row Address Input
A0-A7	Column Address Input
BA0, BA1	Bank Select Address
DQ0 – DQ31	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe Command
$\overline{RAS}$	Row Address Strobe Command

$\overline{WE}$	Write Enable
DM0-DM3	Data Write Mask
DQS0-DQS3	Data Strobe
VDD	Power
VDDQ	Power Supply for I/O Pins
VREF	SSTL_2 reference voltage
VSS	Ground
VSSQ	Ground for I/O Pins
NC	No Connection

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PIN FUNCTIONAL DESCRIPTIONS

Symbol	Type	Description
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of crossing). Internal clock signals are derived from CK/ $\overline{CK}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWERDOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{CS}$	Input	Chip Select: CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS is registered HIGH. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM: x8; LDM, UDM: x16; DM0-DM3: x32	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15. For x32 devices, DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
BA0, BA1	Input	Input Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [11:0]	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
DQ: DQ0-DQ7: x8; DQ0-DQ15: x16 DQ0-DQ31: x32	I/O	Data Bus: Input / Output
DQS: x8; LDQS, UDQS x16: DQS0-DQS3: x32	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. For x16 device, LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15. For x32 device, DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
NC	--	No Connect: Should be left unconnected.
VREF	Supply	SSTL_2 reference voltage.
VDDQ	Supply	I/O Power Supply.
VSSQ	Supply	I/O Ground.
VDD	Supply	Power Supply.
VSS	Supply	Ground.

COMMANDS TRUTH TABLES

All commands (address and control signals) are registered on the positive edge of clock (crossing of CK going high and CK going low). Truth Table shows basic timing parameters for all commands.

TRUTH TABLE - COMMANDS

NAME (FUNCTION)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	AP	Address	Notes
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (select bank and activate row)	L	L	H	H	Valid	X	Row	
READ (select bank and column and start read burst)	L	H	L	H	Valid	L	Column	
READ with AP (read burst with Auto Precharge)	L	H	L	H	Valid	H	Column	3
WRITE (select bank and column and start write burst)	L	H	L	L	Valid	L	Column	
WRITE with AP (write burst with Auto Precharge)	L	H	L	L	Valid	H	Column	3
BURST TERMINATE	L	H	H	L	X	X	X	4
PRECHARGE (deactivate row in selected bank)	L	L	H	L	Valid	L	X	5
PRECHARGE ALL (deactivate rows in all banks)	L	L	H	L	X	H	X	5
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	6,7,8
MODE REGISTER SET	L	L	L	L	Valid	Op-code		9

Notes:
1. All states and sequences not shown are illegal or reserved.
2. DESELECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. AP High enables Auto Precharge, while AP Low disables Autoprecharge.
4. Burst Terminate applies to only Read bursts with Auto Precharge disabled. This command is undefined and should not be used for Read with Auto Precharge enabled, and for Write bursts.
5. If AP is Low, bank address determines which bank is to be precharged. If AP is High, all banks are precharged and BA0-BA1are don't care.
6. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
7. All address inputs and I/O are 'don't care' except for CKE. Internal refresh counters control bank and row addressing.
8. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
9. BA0 and BA1 value select between MRS and EMRS.
10. CKE is HIGH for all commands shown except SELF REFRESH.

TRUTH TABLE - DM Operations

FUNCTION	DM	DQ
Write Enable	L	Valid
Write Inhibit	H	X

Note: Used to mask write data, provided coincident with the corresponding data.

ADDRESSING

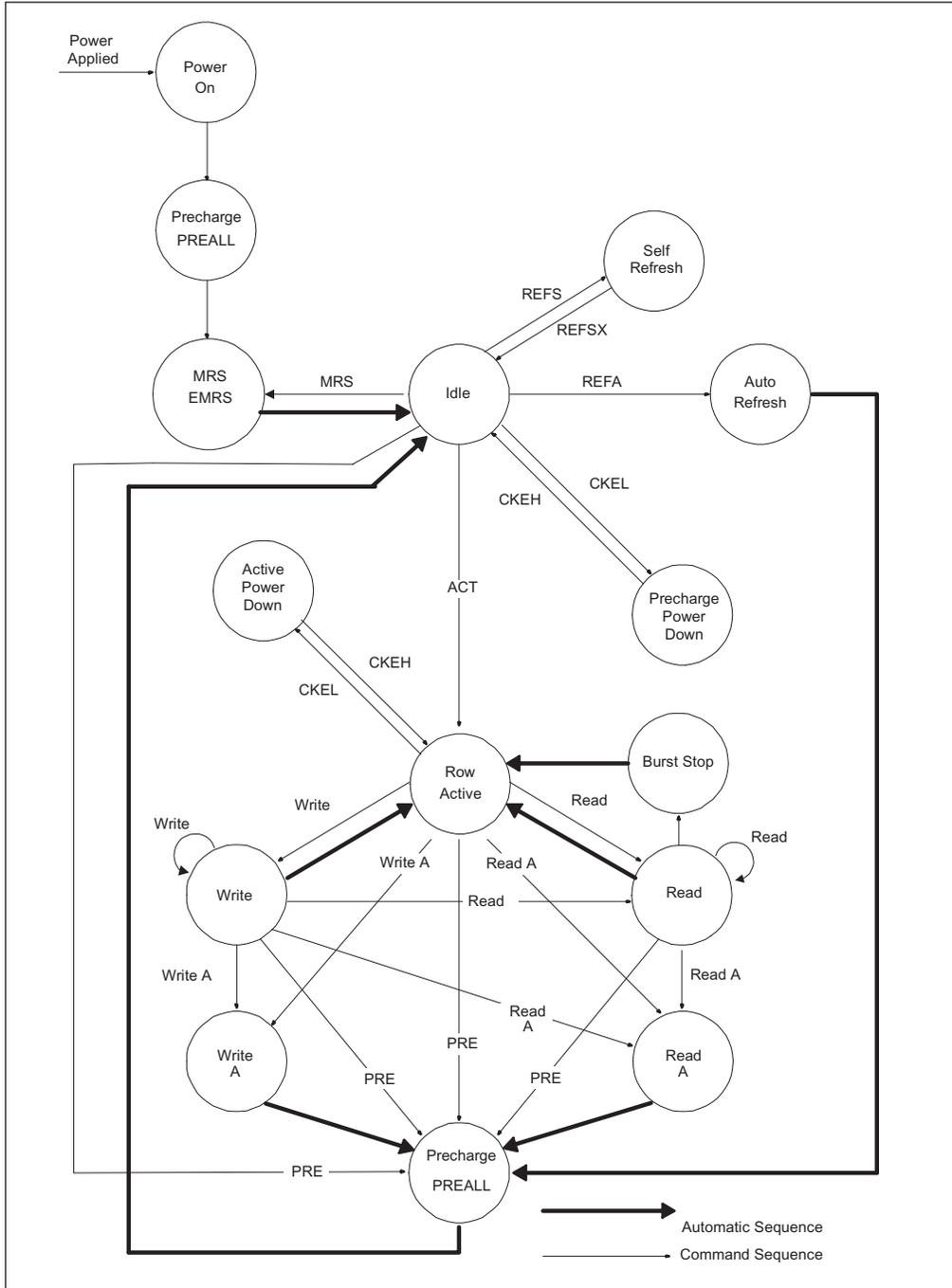|	x32	x16
Auto Precharge (AP)	A8	A10
Row Address (RA)	A0-A11	A0-A11
Column Address (CA)	A0-A7	A0-A8

TRUTH TABLE - CKE

CKE n-1	CKE n	Current State	COMMAND n	ACTION n	NOTES
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	H	Power Down	NOP or DESELECT	Exit Power Down	6
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	6, 7
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	6
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	6
H	L	All Banks Idle	AUTO REFRESH	Self Refresh entry	
H	H	See Truth Tables - Commands			

Notes:
1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of DDR immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is the result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. CKE must not go LOW during a Read or Write, and must stay HIGH until after t_{RPST} or t_{WR}, respectively.
6. DESELECT and NOP are functionally interchangeable.
7. NOPs or Deselects must be issued for at least t_{SNR} after Self-Refresh exit before any other command. After DLL Reset, at least t_{XSRD} must elapse before any Read commands occur.

Basic Timing Parameters for Commands

NOTE: Input = A0 - An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$;
An = Address bus MSB
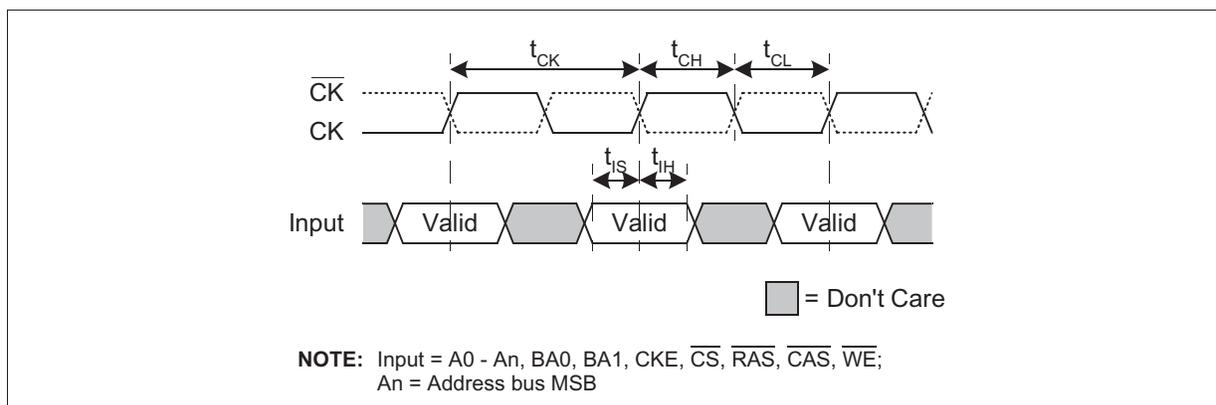
SIMPLIFIED STATE DIAGRAM

PREALL = Precharge All Banks

CKEL = Enter Power Down

MRS = Mode Register Set

CKEH = Exit Power Down

EMRS = Extended Mode Register Set

ACT = Active

REFS = Enter Self Refresh

Write A = Write with Autoprecharge

REFSX = Exit Self Refresh

Read A = Read with Autoprecharge

REFA = Auto Refresh

PRE = Precharge

FUNCTIONAL DESCRIPTION

The DDR SDRAM is a high speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. The 128Mb devices contains: 134,217,728 bits.

The DDR SDRAM uses double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below. The Initialization Flow diagram and the Initialization Flow sequence are shown in the following figures.

The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation. The clock stop feature is not available until the device has been properly initialized from Step 1 through 13.

- Step 1: Apply VDD before or at the same time as VDDQ.
- Step 2: CKE must maintain LVCMOS Low until VREF is stable. Apply VDDQ before applying VTT and VREF.
- Step 3: There must be at least 200 μs of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus and CKE should be brought HIGH.
- Step 4: Issue a PRECHARGE ALL command.
- Step 5: Provide NOPs or DESELECT commands for at least tRP time.
- Step 6: Issue EMRS command
- Step 7: Issue MRS command, load the base mode register and to reset the DLL. Set the desired operating modes.
- Step 8: Provide NOPs or DESELECT commands for at least tMRD time.
- Step 9: Issue a PRECHARGE ALL command
- Step 10: Issue 2 or more AUTO REFRESH cycles
- Step 11: Issue MRS command with the reset DLL bit deactivated to program operating parameters without resetting the DLL
- Step 12: Provide NOP or DESELECT commands for at least tMRD time.
- Step 13: The DRAM has been properly initialized and is ready for any valid command.
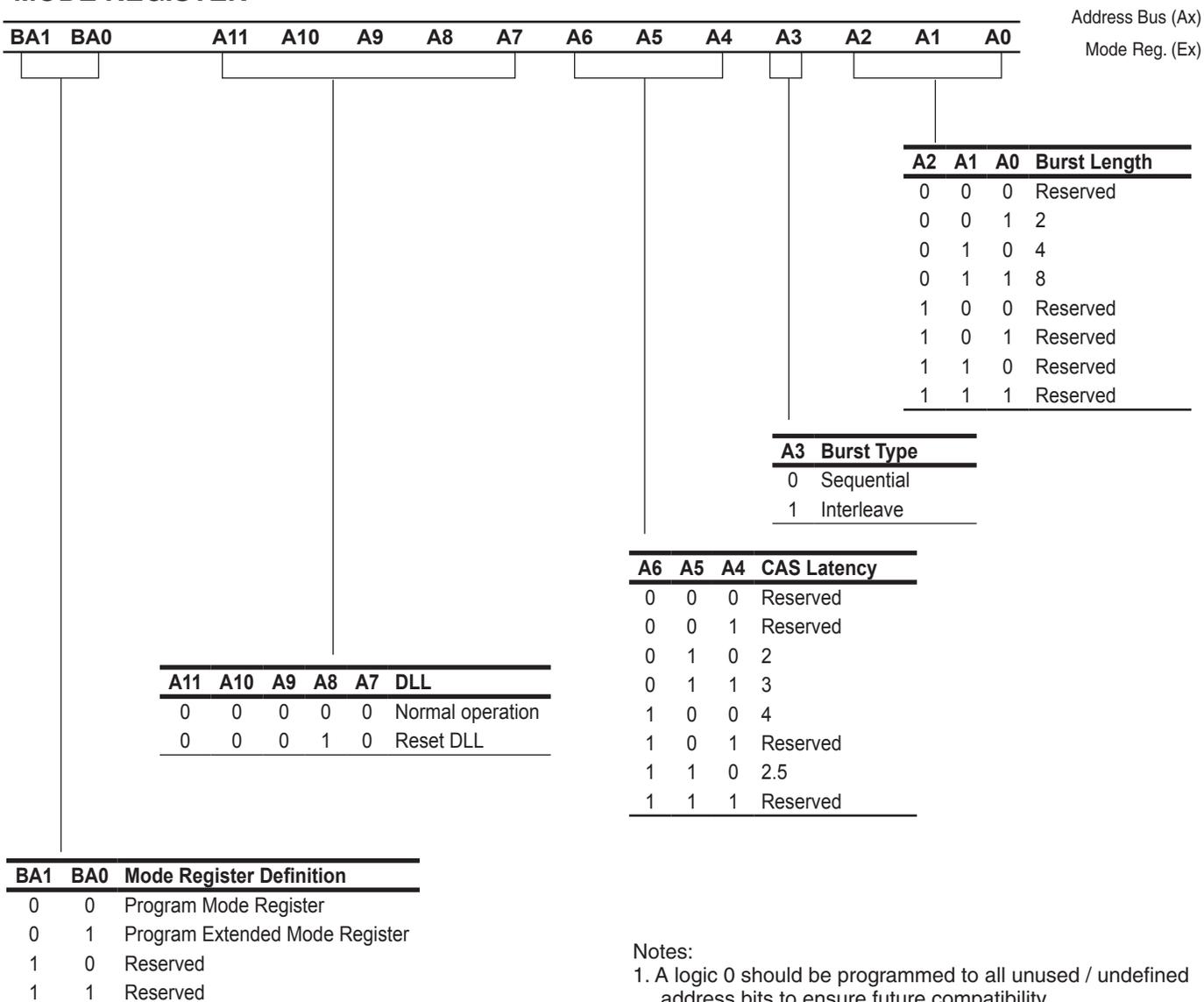
Initialization Waveform Sequence
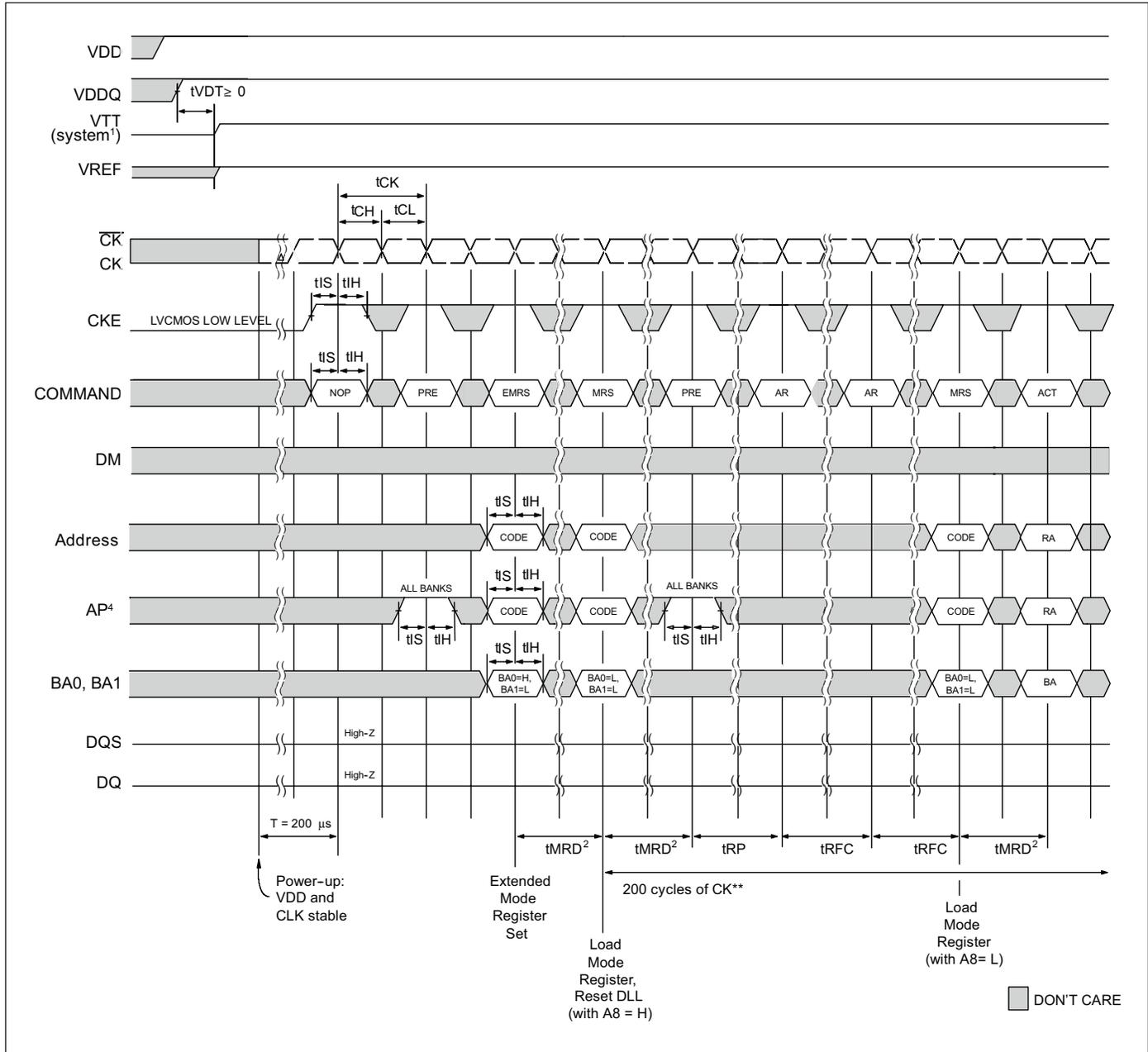
Notes:
1. VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch--up.
2. tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied
3. The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.
4. AP is A8 for x32, and A10 for x16. Address is A0 to A11 except AP.

MODE REGISTER (MR) DEFINITION

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the definition of a burst length, a burst type, and a CAS latency. The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, or the device loses power. Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential or interleave), A4-A6 the CAS latency, and A8 DLL reset. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility. The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Reserved states should not be used, as unknown operation or incompatibility with future versions may result

MODE REGISTER

BA1	BA0		A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus (Ax)
															Mode Reg. (Ex)

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A11	A10	A9	A8	A7	DLL
0	0	0	0	0	Normal operation
0	0	0	1	0	Reset DLL

BA1	BA0	Mode Register Definition
0	0	Program Mode Register
0	1	Program Extended Mode Register
1	0	Reserved
1	1	Reserved

Notes:
1. A logic 0 should be programmed to all unused / undefined address bits to ensure future compatibility.

BURST LENGTH

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being set and the burst order as in Burst Definition. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A 0		
			0	0-1	0-1
			1	1-0	1-0
4		A 1	A 0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A 2	A 1	A 0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:
1. For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.
2. For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-An selects the eight data element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to 4, by A3-An when the burst length is set to 8. An is the most significant column address bit, which depends if the device is x16 or x32. An = A8 for x16 and An = A7 for x32. The programmed burst length applies to both read and write bursts.

BURST TYPE
Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address.

READ LATENCY
The READ latency, or CAS latency, is the delay between the registration of a READ command and the availability of the first piece of output data.

If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at n + 2tCK + tAC. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at n + tCK + tAC.

OPERATING MODE
The normal operating mode is selected by issuing a Mode Register Set command with bits A7 to A11 each set to zero, and bits A0 to A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9 to A11 each set to zero, bit A8 set to one, and bits A0 to A6 set to the desired values. A Mode Register Set command issued to reset the DLL must always be followed by a Mode Register Set command to select normal operating mode (A8=0).

All other combinations of values for A7 to A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.
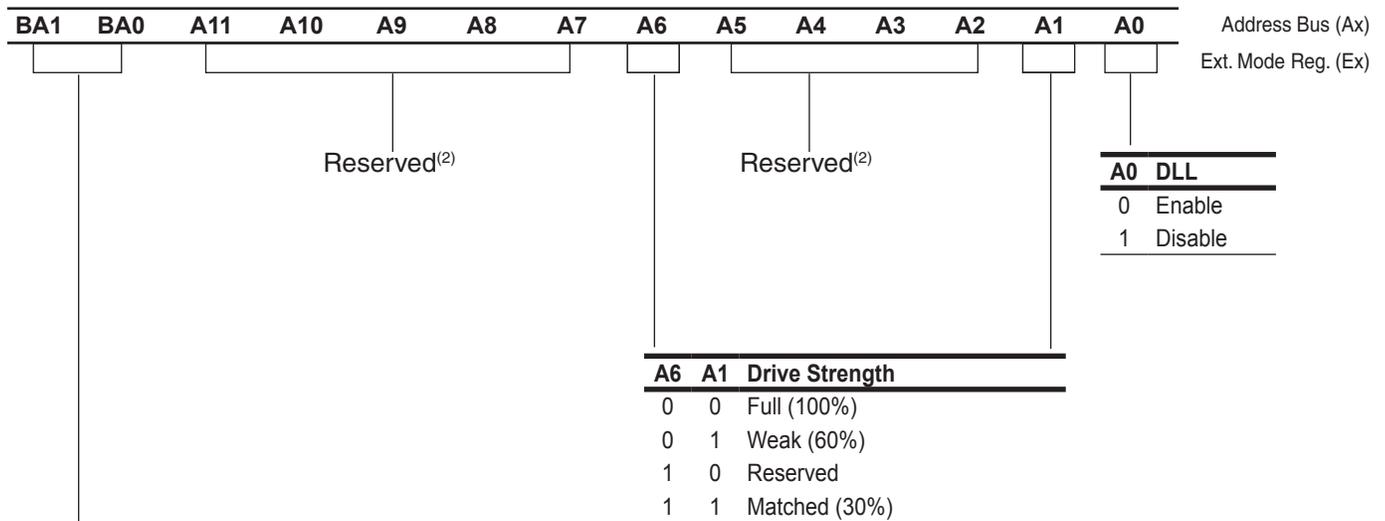
CAS LATENCIES

Burst Length = 4 in the cases shown

Shown with nominal tDQSCK

DON'T CARE
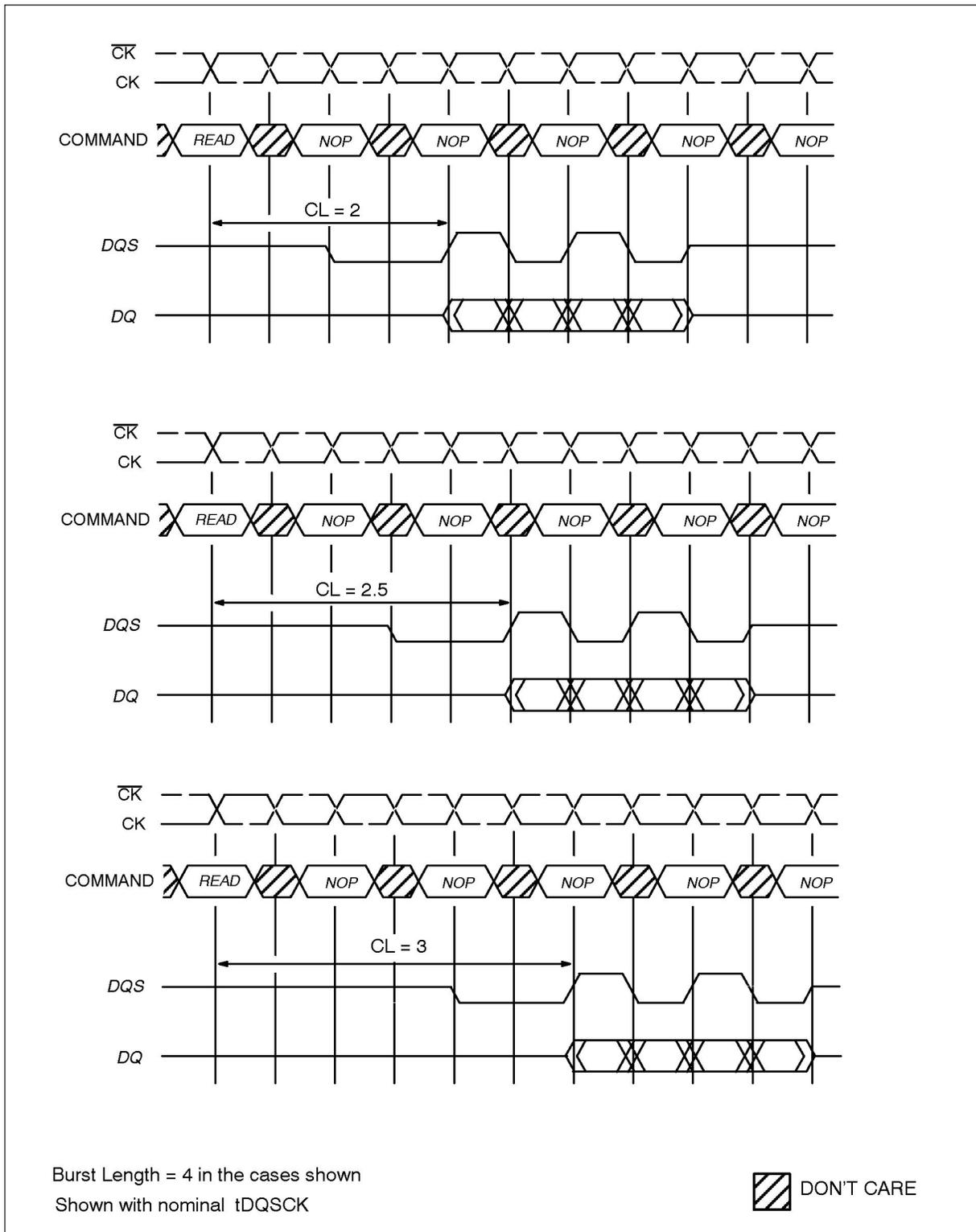
EXTENDED MODE REGISTER (EMR) DEFINITION

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, and output drive strength selection. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=0 and BA0=1) and will retain the stored information until it is reprogrammed, or the device loses power. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles must occur before any executable command can be issued.

OUTPUT DRIVE STRENGTH (DS)

The normal drive strength for all outputs is specified to be SSTL_2, Class II. This DRAM also supports a weak driver strength option, intended for lighter load and/or point-to-point environments. I--V curves for the normal drive strength are included in this datasheet.

EXTENDED MODE REGISTER DEFINITION

Extended Mode Register

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus (Ax)
														Ext. Mode Reg. (Ex)

Reserved[2]   Reserved[2]

A0	DLL
0	Enable
1	Disable

A6	A1	Drive Strength
0	0	Full (100%)
0	1	Weak (60%)
1	0	Reserved
1	1	Matched (30%)

BA1	BA0	Mode Register Definition
0	0	Program Mode Register
0	1	Program Extended Mode Register
1	0	Reserved
1	1	Reserved

NOTES:
1. MSB depends on DDR SDRAM density.
2. A logic 0 should be programmed to all unused/undefined address bits to ensure future compatibility

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_{IN}, V_{OUT}	-1.0 ~ 3.6	V
Voltage on VDD & VDDQ supply relative to VSS	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5	W
Short circuit current	I_{OS}	50	mA

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

AC/DC Electrical Characteristics and Operating Conditions

Recommended operating conditions (Voltage referenced to VSS=0V; TA=0 to 70°C for Commercial, TA = -40°C to +85°C for Industrial and A1, TA = -40°C to +105°C for A2)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage (with a nominal V_{DD} of 2.5V for -5, -6)	V_{DD}	2.3	2.7	V	
Supply voltage(with a nominal V_{DD} of 2.5V for -4)	V_{DD}	2.4	2.6	V	
I/O Supply voltage (with a nominal V_{DD} of 2.5V for -5, -6)	V_{DDQ}	2.3	2.7	V	
I/O Supply voltage(with a nominal V_{DD} of 2.5V for -4)	V_{DDQ}	2.4	2.6	V	
I/O Reference voltage	V_{REF}	0.49*V_{DDQ}	0.51*V_{DDQ}	V	1
I/O Termination voltage (system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	$V_{IH(DC)}$	V_{REF}+0.15	V_{DDQ}+0.45	V	
Input logic low voltage	$V_{IL(DC)}$	V_{DDQ}-0.45	V_{REF}-0.15	V	
Input Voltage Level, CLK and CLK inputs	$V_{IN(DC)}$	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CLK and CLK inputs	$V_{ID(DC)}$	0.36	V_{DDQ}+0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	V_I(Ratio)	0.71	1.4	–	4
Input leakage current	I_L	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current (Normal strength driver) ; V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8	–	mA	
Output Low Current (Normal strength driver) ; V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8	–	mA	
Output High Current (Half strength driver); V_{OUT} = V_{TT} + 0.45V	I_{OHR}	-9	–	mA	
Output Low Current (Half strength driver); V_{OUT} = V_{TT} - 0.45V	I_{OLR}	9	–	mA	
Ambient Operating Temperature					
Commercial	T_A	0	+70	°C	
Industrial	T_A	-40	+85	°C	
A1	T_A	-40	+85	°C	
A2	T_A	-40	+105	°C	

Note :
1. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on VREF may not exceed +/-2% of the dc value.
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CLK and the input level on CLK.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

Integrated Silicon Solution, Inc.

CAPACITANCE CHARACTERISTICS[1, 2]
(V_{DD} = V_{DDQ} = 2.5V + 0.2V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Units
			Min	Max	
CI(A)	Input Capacitance, address pin	VI=1.25v	1.3	3	pF
CI(C)	Input Capacitance, control pin	f=100MHz	1.3	3	pF
CI(K)	Input Capacitance, CLK pin	VI=25mVrms	2	4	pF
CI/O	I/O Capacitance, I/O, DQS, DM pin		2	5	pF

Notes:
1. This parameter is characterized.
2. Conditions: Frequency = 100MHz; V_{OUT}(DC) = V_{DD}/2; V_{OUT}(peak-to-peak) = 0.2V; V_{REF} = Vss.

IDD Specification Parameters and Test Conditions: x16

(VDD = VDDQ = 2.5V ± 0.2V (-5,-6); VDD = VDDQ = 2.5V ±0.1V(-4); Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/ Test Condition	-4	-5	-6	Units
IDD0	Operating current for one bank active-precharge; tRC = tRC(min); tCK = tCK(min); DQ, DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles; CS = high between valid commands.	130	125	120	mA
IDD1	Operating current for one bank operation; one bank open, BL = 4, tRC = tRC(min), tCK = tCK(min), Iout=0mA, Address and control inputs changing once per clock cycle.	140	135	130	mA
IDD2P	Precharge power-down standby current; all banks idle; power-down mode; CKE VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS and DM	30	30	30	mA
IDD2N	Precharge floating standby current; CS VIH(min); all banks idle; CKE VIH(min); tCK = tCK(min); address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS and DM	85	70	60	mA
IDD3P	Active power-down standby current; all banks active; power-down mode; CKE VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS and DM	30	30	30	mA
IDD3N	Active standby current; CS VIH(min); CKE VIH(min); all banks active; tRC = tRAS(max); tCK = tCK(min); DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	100	80	70	mA
IDD4R	Operating current for burst read; burst length = 2; reads; continuous burst; one bank active; address and control inputs changing once per clock cycle; tCK = tCK(min); 50% of data changing on every transfer; IOUT = 0mA	240	180	170	mA
IDD4W	Operating current for burst write; burst length = 2; writes; continuous burst; one bank active address and control inputs changing once per clock cycle; tCK = tCK(min); DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer	240	180	170	mA
IDD5	Auto refresh current; tRC = tRFC(min);	190	180	170	mA
IDD6	Self refresh current; CKE 0.2V;	3	3	3	mA
IDD7	Operating current for four bank operation; four bank interleaving READs (BL=4) with auto precharge; tRC = tRC(min), tCK = tCK(min); Address and control inputs change only during ACTIVE, READ, or WRITE commands	280	240	220	mA

IDD Specification Parameters and Test Conditions: x32

(V_{DD} = V_{DDQ} = 2.5V ± 0.2V (-5,-6); V_{DD} = V_{DDQ} = 2.5V ±0.1V(-4); Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/ Test Condition	-4	-5	-6	Units
IDD0	Operating current for one bank active-precharge; tRC = tRC(min); tCK = tCK(min); DQ, DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles; CS = high between valid commands.	160	150	140	mA
IDD1	Operating current for one bank operation; one bank open, BL = 4, tRC = tRC(min), tCK = tCK(min), Iout=0mA, Address and control inputs changing once per clock cycle.	180	170	160	mA
IDD2P	Precharge power-down standby current; all banks idle; power-down mode; CKE VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS and DM	30	30	30	mA
IDD2N	Precharge floating standby current; CS VIH(min); all banks idle; CKE VIH(min); tCK = tCK(min); address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS and DM	80	70	60	mA
IDD3P	Active power-down standby current; all banks active; power-down mode; CKE VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS and DM	40	30	30	mA
IDD3N	Active standby current; CS VIH(min); CKE VIH(min); all banks active; tRC = tRAS(max); tCK = tCK(min); DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	90	80	70	mA
IDD4R	Operating current for burst read; burst length = 2; reads; continuous burst; one bank active; address and control inputs changing once per clock cycle; tCK = tCK(min); 50% of data changing on every transfer; IOUT = 0mA	300	250	230	mA
IDD4W	Operating current for burst write; burst length = 2; writes; continuous burst; one bank active address and control inputs changing once per clock cycle; tCK = tCK(min); DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer	300	250	230	mA
IDD5	Auto refresh current; tRC = tRFC(min);	190	180	170	mA
IDD6	Self refresh current; CKE 0.2V;	3	3	3	mA
IDD7	Operating current for four bank operation; four bank interleaving READs (BL=4) with auto precharge; tRC = tRC(min), tCK = tCK(min); Address and control inputs change only during ACTIVE, READ, or WRITE commands	340	320	300	mA

AC TIMING REQUIREMENTS [1-4,12,13,21]
Absolute Specifications (VDD, VDDQ = +2.5 V ±0.1 V @ -4)

PARAMETER	SYMBOL	-4		UNITS	Notes
		MIN	MAX		
DQ output access time for CLK,/CLK	tAC	-0.7	0.7	ns	
DQS output access time for CLK,/CLK	tDQSCK	-0.6	0.6	ns	
CLK high-level width	tCH	0.45	0.55	tCK	
CLK low-level width	tCL	0.45	0.55	tCK	
CLK half period	tHP	min (tCL,tCH)	–	ns	20
CLK cycle time CL=4	tCK(4)	4	10	ns	
CL=3	tCK(3)	5	10	ns	
CL=2.5	tCK(2.5)	–	–	ns	
CL=2	tCK(2)	–	–	ns	
DQ and DM input hold time	tDH	0.4	–	ns	
DQ and DM input setup time	tDS	0.4	–	ns	
Control & Address input pulse width (for each input)	tIPW	2.2	–	ns	
DQ and DM input pulse width (for each input)	tDIPW	1.75	–	ns	
DQ & DQS high-impedance time from CLK,/CLK	tHZ	–	0.7	ns	14
DQ & DQS low--impedance time from CLK,/CLK	tLZ	-0.7	–	ns	14
DQS--DQ Skew, DQS to last DQ valid, per group, per access	tDQSQ	–	0.4	ns	
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	–	ns	
Data Hold Skew Factor	tQHS	–	0.5	ns	
Write command to first DQS latching transition	tDQSS	0.72	1.28	tCK	
DQS input high pulse width	tDQSH	0.35	–	tCK	
DQS input low pulse width	tDQSL	0.35	–	tCK	
DQS falling edge to CLK setup time	tDSS	0.2	–	tCK	
DQS falling edge hold time from CLK	tDSH	0.2	–	tCK	
MODE REGISTER SET command cycle time	tMRD	2	–	tCK	
Write preamble setup time	tWPRES	0	–	ns	16
Write postamble	tWPST	0.4	0.6	tCK	15
Write preamble	tWPRE	0.25	–	tCK	
Address and Control input hold time (fast slew rate)	tIHF	0.6	–	ns	
Address and Control input setup time (fast slew rate)	tISF	0.6	–	ns	
Address and Control input hold time (slow slew rate)	tIH	0.7	---	ns	19
Address and Control input setup time (slow slew rate)	tIS	0.7	–	ns	19
Read preamble	tRPRE	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	tCK	
ACTIVE to PRECHARGE command	tRAS	40	70,000	ns	

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = +2.5 V ±0.1 V @ -4)

PARAMETER		SYMBOL	-4		UNITS	Notes
			MIN	MAX		
ACTIVE to ACTIVE/Auto Refresh command period		tRC	52	–	ns	
Auto Refresh to Active/Auto		tRFC	68	–	ns	
ACTIVE to READ or WRITE delay		tRCD	16	–	ns	
PRECHARGE command period		tRP	16	–	ns	
Active to Autoprecharge Delay		tRAP	15	–	ns	
ACTIVE bank A to ACTIVE bank B command		tRRD	8	–	ns	
Write recovery time		tWR	16	–	ns	
Auto Precharge write recovery + precharge time		tDAL	tWR+tRP	–	tCK	
Internal Write to Read Command Delay		tWTR	2	–	tCK	
Exit self refresh to non-READ		tXSNR	70	–	ns	
Exit self refresh to READ command		tXSRD	200	–	tCK	
Average Periodic Refresh Interval	$T_A \leq 85°C$	tREFI	–	15.6	µs	17

AC TIMING REQUIREMENTS [1-4,12,13,21]
Absolute Specifications (VDD, VDDQ = +2.5 V ±0.2 V @ -5,-6)

| PARAMETER	SYMBOL	-5		-6		UNITS	Notes
		MIN	MAX	MIN	MAX		
DQ output access time for CLK,/CLK	tAC	-0.7	0.7	-0.7	0.7	ns	
DQS output access time for CLK,/CLK	tDQSCK	-0.6	0.6	-0.6	0.6	ns	
CLK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CLK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CLK half period	tHP	min (tCL,tCH)	–	min (tCL,tCH)	–	ns	20
CLK cycle time CL=3	tCK(3)	5	10	6	10	ns	
CL=2.5	tCK(2.5)	6	10	6	10	ns	
CL=2	tCK(2)	7.5	10	7.5	10	ns	
DQ and DM input hold time	tDH	0.4	–	0.45	–	ns	
DQ and DM input setup time	tDS	0.4	–	0.45	–	ns	
Control & Address input pulse width (for each input)	tIPW	2.2	–	2.2	–	ns	
DQ and DM input pulse width (for each input)	tDIPW	1.75	–	1.75	–	ns	
DQ & DQS high-impedance time from CLK,/CLK	tHZ	–	0.7	–	0.7	ns	14
DQ & DQS low--impedance time from CLK,/CLK	tLZ	-0.7	–	-0.7	–	ns	14
DQS--DQ Skew, DQS to last DQ valid, per group, per access	tDQSQ	–	0.4	–	0.45	ns	
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	–	tHP-tQHS	–	ns	
Data Hold Skew Factor	tQHS	–	0.5	–	0.55	ns	
Write command to first DQS latching transition	tDQSS	0.72	1.28	0.75	1.28	tCK	
DQS input high pulse width	tDQSH	0.35	–	0.35	–	tCK	
DQS input low pulse width	tDQSL	0.35	–	0.35	–	tCK	
DQS falling edge to CLK setup time	tDSS	0.2	–	0.2	–	tCK	
DQS falling edge hold time from CLK	tDSH	0.2	–	0.2	–	tCK	
MODE REGISTER SET command cycle time	tMRD	2	–	2	–	tCK	
Write preamble setup time	tWPRES	0	–	0	–	ns	16
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	15
Write preamble	tWPRE	0.25	–	0.25	–	tCK	
Address and Control input hold time (fast slew rate)	tIHF	0.6	–	0.75	–	ns	
Address and Control input setup time (fast slew rate)	tISF	0.6	–	0.75	–	ns	
Address and Control input hold time (slow slew rate)	tIH	0.7	–	0.8	-–	ns	19
Address and Control input setup time (slow slew rate)	tIS	0.7	–	0.8	–	ns	19
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
ACTIVE to PRECHARGE command	tRAS	40	70,000	42	120,000	ns	

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = +2.5 V ±0.2 V @ -5,-6)

PARAMETER		SYMBOL	-5		-6		UNITS	Notes
			MIN	MAX	MIN	MAX		
ACTIVE to ACTIVE/Auto Refresh command period		tRC	50	–	54	–	ns	
Auto Refresh to Active/Auto		tRFC	70	–	70	–	ns	
ACTIVE to READ or WRITE delay		tRCD	15	–	18	–	ns	
PRECHARGE command period		tRP	15	–	18	–	ns	
Active to Autoprecharge Delay		tRAP	15	–	18	–	ns	
ACTIVE bank A to ACTIVE bank B command		tRRD	10	–	12	–	ns	
Write recovery time		tWR	15	–	12	–	ns	
Auto Precharge write recovery + precharge time		tDAL	tWR+tRP	–	tWR+tRP	–	tCK	
Internal Write to Read Command Delay		tWTR	2	–	1	–	tCK	
Exit self refresh to non-READ		tXSNR	75	–	75	–	ns	
Exit self refresh to READ command		tXSRD	200	–	200	–	tCK	
Average Periodic Refresh Interval	TA ≤ 85 °C	tREFI	–	15.6	–	15.6	µs	17
	TA > 85 °C, A2 only	tREFI	–	3.9	–	3.9	µs	17

Output Load Condition
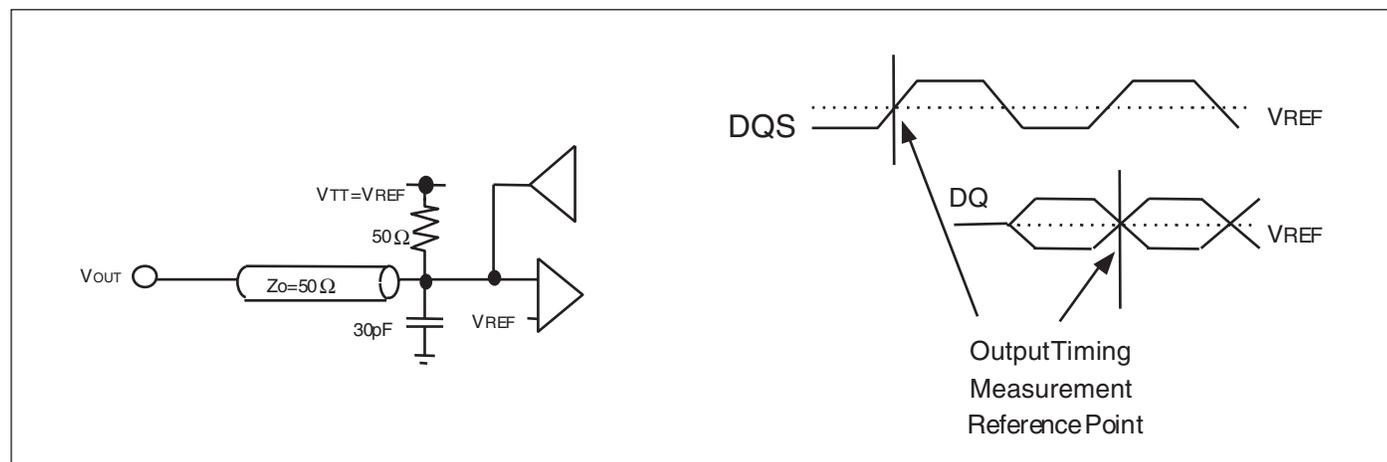
Notes

1. All voltages referenced to Vss.

2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

3. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK//CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).

4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

5. VREF is expected to be equal to 0.5*VddQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +2% of the DC value.

6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.

7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.

8. The value of VIX is expected to equal 0.5*VddQ of the transmitting device and must track variations in the DC level of the same.

9. Enables on-chip refresh and address counters.

10. IDD specifications are tested after the device is properly initialized.

11. This parameter is sampled. VddQ = Vdd = 2.5V, f = 100 MHz, Ta = 25°C, VOUT(DC) = VddQ/2, VOUT(PEAK TO PEAK) = 25mV. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).

12. The CLK//CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.

13. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE< 0.3VddQ is recognized as LOW.

14. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).

15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

16. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.

17. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.

18. tXPRD should be 200 tCLK in the condition of the unstable CLK operation during the power down mode.

19. For command/address and CK & /CK slew rate > 1.0V/ns.

20. Min (tCL,tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device.

21. CL=4 is specified only for -4 speed option.

Integrated Silicon Solution, Inc.

OUTPUT SLEW RATE CHARACTERISTICS

Slew Rate Characteristic	Typical Range (V/ns)	Min (V/ns)	Max (V/ns)
Pullup Slew Rate	1.2-2.5	0.7	5.0
Pulldown Slew Rate	1.2-2.5	0.7	5.0

AC OVERSHOOT/UNDERSHOOT SPECIFICATION FOR ADDRESS AND CONTROL PINS

Parameter	Max	Units
Peak amplitude allowed for overshoot	1.5	V
Peak amplitude allowed for undershoot	1.5	V
Area between the overshoot signal and VDD must be less than or equal to (see figure below)	4.5	V-ns
Area between the undershoot signal and GND must be less than or equal to (see figure below)	4.5	V-ns
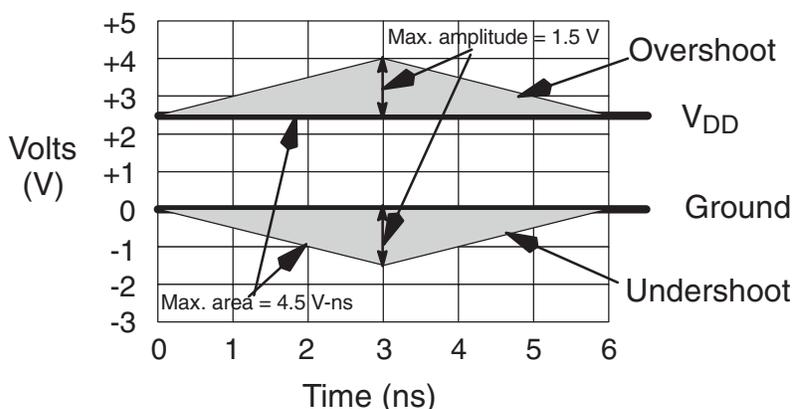
Address and Control AC Overshoot and Undershoot Definition

OVERSHOOT/UNDERSHOOT SPECIFICATION FOR DATA, STROBE, AND MASK PINS

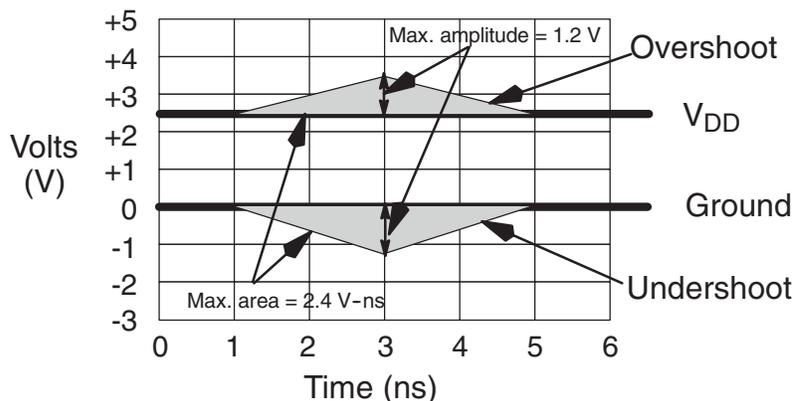| Parameter	Max	Units
Peak amplitude allowed for overshoot	1.2	V
Peak amplitude allowed for undershoot	1.2	V
Area between the overshoot signal and VDD must be less than or equal to (see figure below)	2.4	V-ns
Area between the undershoot signal and GND must be less than or equal to (see figure below)	2.4	V-ns

DQ/DM/DQS AC Overshoot and Undershoot Definition

IS43/46R16800E, IS43/46R32400E

8Mx16 ORDERING INFORMATION - VDD = 2.5V

Commercial Range: 0°C to +70°C

Frequency	Speed (ns)	Order Part No.	Package
200 MHz	5	IS43R16800E-5BL	60-ball FBGA, Lead-free
		IS43R16800E-5TL	66-pin TSOP-II, Lead-free
166 MHz	6	IS43R16800E-6BL	60-ball FBGA, Lead-free
		IS43R16800E-6TL	66-pin TSOP-II, Lead-free

Industrial Range: -40°C to +85°C

Frequency	Speed (ns)	Order Part No.	Package
200 MHz	5	IS43R16800E-5BLI	60-ball FBGA, Lead-free
		IS43R16800E-5BI	60-ball FBGA
		IS43R16800E-5TLI	66-pin TSOP-II, Lead-free
166 MHz	6	IS43R16800E-6BLI	60-ball FBGA, Lead-free
		IS43R16800E-6BI	60-ball FBGA
		IS43R16800E-6TLI	66-pin TSOP-II, Lead-free

Automotive (A1) Range: -40°C to +85°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS46R16800E-6BLA1	60-ball FBGA, Lead-free
		IS46R16800E-6TLA1	66-pin TSOP-II, Lead-free

Automotive (A2) Range: -40°C to +105°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS46R16800E-6BLA2	60-ball FBGA, Lead-free
		IS46R16800E-6TLA2	66-pin TSOP-II, Lead-free

4Mx32 ORDERING INFORMATION - VDD = 2.5V

Commercial Range: 0°C to +70°C

Frequency	Speed (ns)	Order Part No.	Package
250 MHz	4	IS43R32400E-4BL	144-ball FBGA, Lead-free
200 MHz	5	IS43R32400E-5BL	144-ball FBGA, Lead-free
166 MHz	6	IS43R32400E-6BL	144-ball FBGA, Lead-free

Industrial Range: -40°C to +85°C

Frequency	Speed (ns)	Order Part No.	Package
200 MHz	5	IS43R32400E-5BLI	144-ball FBGA, Lead-free
166 MHz	6	IS43R32400E-6BLI	144-ball FBGA, Lead-free

Automotive (A1) Range: -40°C to +85°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS46R32400E-6BLA1	144-ball FBGA, Lead-free

Note : Contact ISSI for availability of leaded options.

SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A			1.20
A1	0.05		0.20
A2	0.95	1.00	1.05
b	0.22		0.40
C	0.12		0.21
D	22.02	22.22	22.42
E	11.56	11.76	11.96
E1	10.03	10.16	10.29
e	0.65 BSC.		
L	0.40	0.50	0.60
L1	0.25 BSC.		
ZD	0.71 REF.		
θ	0		8°

NOTE :

1. Controlling dimension : mm

2. Dimension D and E1 do not include mold protrusion .

3. Dimension b does not include dambar protrusion/intrusion.

4. Formed leads shall be planar with respect to one another within 0.1mm
   at the seating plane after final test.

TITLE	**66L 400mil TSOP-2** Package Outline	**REV.**	**C**	**DATE**	10/04/2006

Mini Ball Grid Array
Package Code: B (60-Ball) 8mm x 13mm

SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A			1.20
A1	0.25		0.40
φb	0.40	0.45	0.50
D	7.90	8.00	8.10
D1		6.40 BSC.	
E	12.90	13.00	13.10
E1		11.00 BSC.	
eD		0.80 BSC.	
eE		1.00 BSC.	
y			0.10

NOTE :

1. CONTROLLING DIMENSION : MM.

BOTTOM VIEW

TOP VIEW

SEATING PLANE
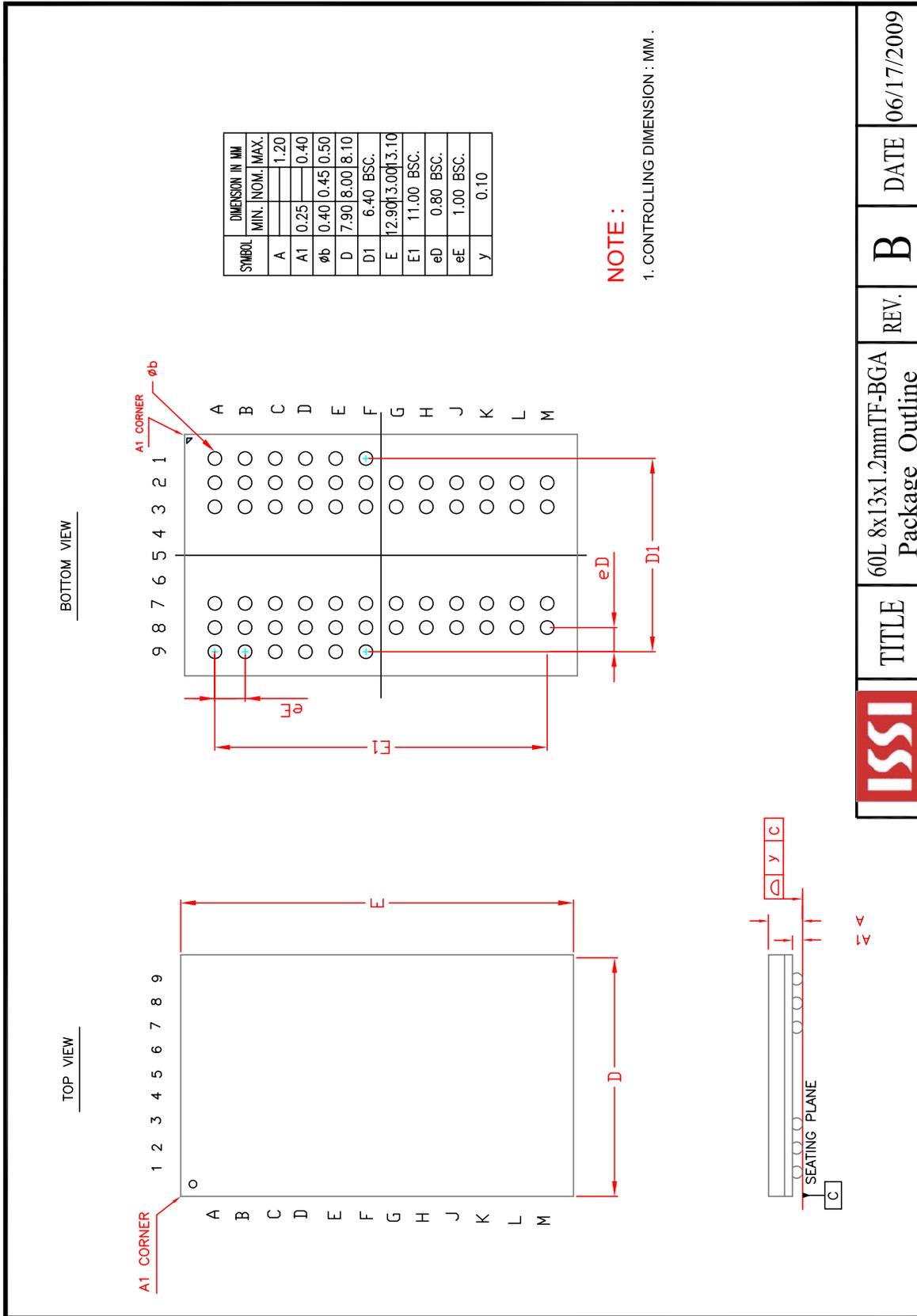
TITLE: 60L 8x13x1.2mmTF-BGA Package Outline

REV. B

DATE 06/17/2009

Integrated Silicon Solution, Inc.
Rev. C
1/16/14

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.40	—	—	0.055
A1	0.25	—	0.40	0.010	—	0.016
D	11.90	12.00	12.10	0.469	0.472	0.476
D1	—	8.80	—	—	0.346	—
E	11.90	12.00	12.10	0.469	0.472	0.476
E1	—	8.80	—	—	0.346	—
e	—	0.80	—	—	0.031	—
φb	0.40	0.45	0.50	0.016	0.018	0.020

NOTE :

1. CONTROLLING DIMENSION : MM.
2. Reference document : JEDEC MO-205
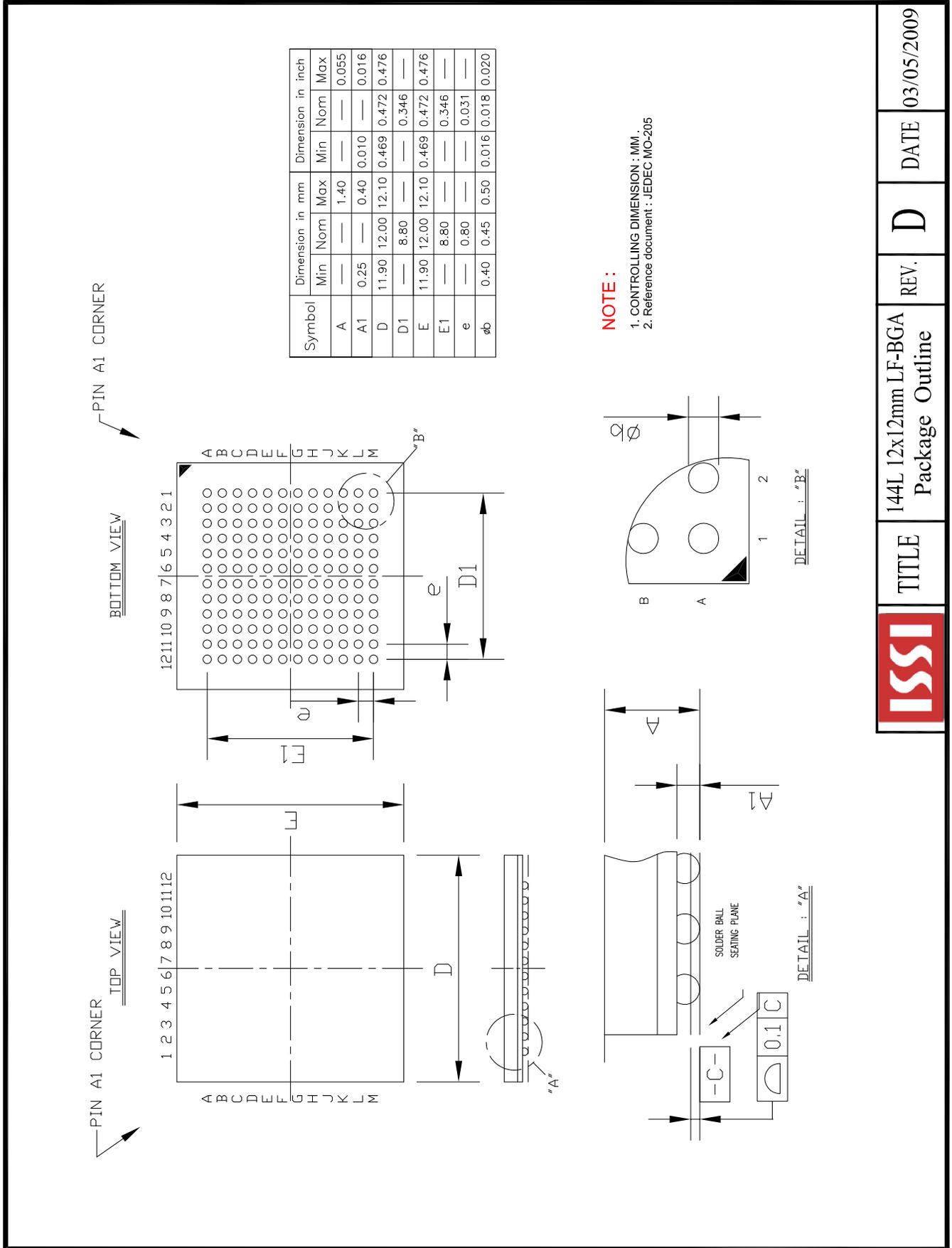
TITLE: 144L 12x12mm LF-BGA Package Outline

REV. D

DATE 03/05/2009

PIN A1 CORNER

BOTTOM VIEW

TOP VIEW

PIN A1 CORNER

DETAIL : "B"

DETAIL : "A"

SOLDER BALL SEATING PLANE

ООО "ЛайфЭлектроникс"   **"LifeElectronics" LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.

- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.

- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.

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