

FEATURES

- 2.3 A peak output current (typical)**
- 2.5 V to 6.5 V input**
- 7.5 V to 35 V output**
- Undervoltage lockout (UVLO) at 2.5 V V_{DD1} and 7.5 V V_{DD2}**
- Precise timing characteristics**
 - 53 ns maximum isolator and driver propagation delay**
- CMOS input logic levels**
- High common-mode transient immunity: >150 kV/ μ s**
- High junction temperature operation: 125°C**
- Default low output**
- Internal Miller clamp**
- Safety and regulatory approvals (pending)**
 - UL recognition per UL 1577**
 - 5 kV rms for 1-minute withstand**
 - CSA Component Acceptance Notice 5A**
 - VDE certificate of conformity (pending)**
 - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12**
 - $V_{IORM} = 849$ V peak**
- Wide-body, 8-lead SOIC**

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)**
- Military temperature range (-55°C to +125°C)**
- Controlled manufacturing baseline**
- 1 assembly/test site**
- 1 fabrication site**
- Product change notification**
- Qualification data available on request**

APPLICATIONS

- Missiles and munitions**
- Avionics**
- Unmanned systems**
- Isolated IGBT/MOSFET gate drives**

GENERAL DESCRIPTION

The ADuM4121-1-EP¹ is a 2.3 A isolated, single-channel driver that employ Analog Devices, Inc., iCoupler® technology to provide precision isolation. The ADuM4121-1-EP provides 5 kV rms isolation in the wide-body, 8-lead SOIC package. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as the combination of pulse transformers and gate drivers.

The ADuM4121-1-EP operates with an input supply ranging from 2.5 V to 6.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers that employ high voltage level translation methodologies, the ADuM4121-1-EP offers the benefit of true, galvanic isolation between the input and the output.

The ADuM4121-1-EP includes an internal Miller clamp that activates at 2 V on the falling edge of the gate drive output, supplying the driven gate with a lower impedance path to reduce the chance of Miller capacitance induced turn on.

The ADuM4121-1-EP provides reliable control over the switching characteristics of insulated gate bipolar transistor (IGBT)/metal oxide semiconductor field effect transistor (MOSFET) configurations over a wide range of switching voltages.

Additional application and technical information can be found in the [ADuM4121-1](#) data sheet.

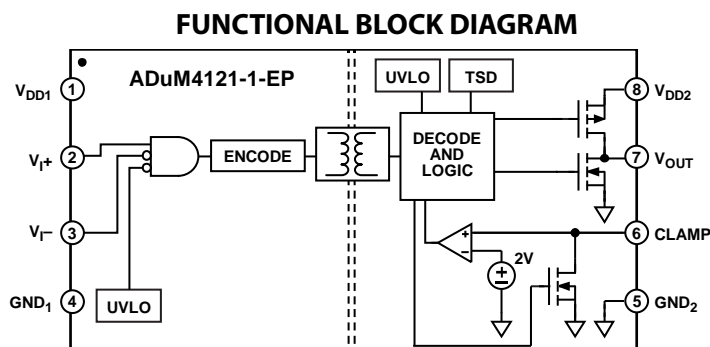


Figure 1.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329. Other patents pending.

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REVISION HISTORY

1/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Low-side voltages referenced to GND₁. High side voltages referenced to GND₂; $2.5\text{ V} \leq V_{DD1} \leq 6.5\text{ V}$; $7.5\text{ V} \leq V_{DD2} \leq 35\text{ V}$, $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_J = 25^\circ\text{C}$, $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 15\text{ V}$.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|------------------------------------|---------------------|----------------------|------|----------------------|---------------|--|
| DC SPECIFICATIONS | | | | | | |
| High Side Power Supply | | | | | | |
| V_{DD2} Input Voltage | V_{DD2} | 7.5 | | 35 | V | |
| V_{DD2} Input Current, Quiescent | $I_{DD2(Q)}$ | | 2.3 | 2.7 | mA | |
| Logic Supply | | | | | | |
| V_{DD1} Input Voltage | V_{DD1} | 2.5 | | 6.5 | V | |
| Input Current | I_{DD1} | | 3.6 | 5 | mA | $V_{I+} = \text{high}, V_{I-} = \text{low}$ |
| Logic Inputs (V_{I+}, V_{I-}) | | | | | | |
| Input Current | I_{I+}, I_{I-} | -1 | 0.01 | +1 | μA | |
| Input Voltage | | | | | | |
| Logic High | V_{IH} | $0.7 \times V_{DD1}$ | | | V | $2.5\text{ V} \leq V_{DD1} \leq 5\text{ V}$ |
| | | 3.5 | | | V | $V_{DD1} > 5\text{ V}$ |
| Logic Low | V_{IL} | | | $0.3 \times V_{DD1}$ | V | $2.5\text{ V} \leq V_{DD1} \leq 5\text{ V}$ |
| | | | | 1.5 | V | $V_{DD1} > 5\text{ V}$ |
| UVLO | | | | | | |
| V_{DD1} | | | | | | |
| Positive Going Threshold | $V_{VDD1UV+}$ | | 2.45 | 2.5 | V | |
| Negative Going Threshold | $V_{VDD1UV-}$ | 2.3 | 2.35 | | V | |
| Hysteresis | $V_{VDD1UVH}$ | | 0.1 | | V | |
| V_{DD2} | | | | | | |
| Positive Going Threshold | $V_{VDD2UV+}$ | | 7.3 | 7.5 | V | |
| Negative Going Threshold | $V_{VDD2UV-}$ | 6.9 | 7.1 | | V | |
| Hysteresis | $V_{VDD2UVH}$ | | 0.2 | | V | |
| Internal NMOS Gate Resistance | $R_{DS(on)_N}$ | | 0.6 | 1.6 | Ω | Tested at 250 mA, $V_{DD2} = 15\text{ V}$ |
| | | | 0.6 | 1.6 | Ω | Tested at 1 A, $V_{DD2} = 15\text{ V}$ |
| Internal PMOS Gate Resistance | $R_{DS(on)_P}$ | | 0.8 | 1.8 | Ω | Tested at 250 mA, $V_{DD2} = 15\text{ V}$ |
| | | | 0.8 | 1.8 | Ω | Tested at 1 A, $V_{DD2} = 15\text{ V}$ |
| Internal Miller Clamp Resistance | $R_{DS(on)_MILLER}$ | | 0.8 | 2 | Ω | Tested at 200 mA, $V_{DD2} = 15\text{ V}$ |
| Miller Clamp Voltage Threshold | V_{CLP_TH} | 1.75 | 2 | 2.25 | V | Referenced to GND ₂ , $V_{DD2} = 15\text{ V}$ |
| Peak Current | I_{PK} | | 2.3 | | A | $V_{DD2} = 12\text{ V}, 4\ \Omega$ gate resistance |
| SWITCHING SPECIFICATIONS | | | | | | |
| Pulse Width | PW | 50 | | | ns | $C_L = 2\text{ nF}, V_{DD2} = 15\text{ V}, R_{GON}^1 = R_{GOFF}^1 = 5\ \Omega$ |
| Propagation Delay | | | | | | |
| Rising Edge ² | t_{DLH} | 22 | 32 | 42 | ns | $C_L = 2\text{ nF}, V_{DD2} = 15\text{ V}, R_{GON} = R_{GOFF} = 5\ \Omega$ |
| Falling Edge ² | t_{DHL} | 30 | 38 | 53 | ns | $C_L = 2\text{ nF}, V_{DD2} = 15\text{ V}, R_{GON} = R_{GOFF} = 5\ \Omega$ |
| Skew ³ | t_{PSK} | | | 22 | ns | $C_L = 2\text{ nF}, V_{DD2} = 15\text{ V}, R_{GON} = R_{GOFF} = 5\ \Omega$ |
| Falling Edge ⁴ | t_{PSKHL} | | | 12 | ns | $C_L = 2\text{ nF}, V_{DD2} = 15\text{ V}, R_{GON} = R_{GOFF} = 5\ \Omega$ |
| Rising Edge ⁵ | t_{PSKHLH} | | | 15 | ns | $C_L = 2\text{ nF}, V_{DD2} = 15\text{ V}, R_{GON} = R_{GOFF} = 5\ \Omega$ |
| Pulse Width Distortion | t_{PWD} | | 7 | 13 | ns | $C_L = 2\text{ nF}, V_{DD2} = 15\text{ V}, R_{GON} = R_{GOFF} = 5\ \Omega$ |
| Output Rise/Fall Time (10% to 90%) | t_r/t_f | 11 | 18 | 26 | ns | $C_L = 2\text{ nF}, V_{DD2} = 15\text{ V}, R_{GON} = R_{GOFF} = 5\ \Omega$ |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---------------------------------------|--------|-----|-----|-----|-------------|--------------------------|
| Common-Mode Transient Immunity (CMTI) | CM | | | | | |
| Static CMTI ⁶ | | 150 | | | kV/ μ s | $V_{CM} = 1500\text{ V}$ |
| Dynamic CMTI ⁷ | | 150 | | | kV/ μ s | $V_{CM} = 1500\text{ V}$ |

¹ R_{GON} and $R_{G OFF}$ are the external gate resistors in the test.

² t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH} , to the output rising 10% threshold of the V_{OUT} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL} , to the output falling 90% threshold of the V_{OX} signal. See the ADuM4121-1 data sheet for waveforms of the propagation delay parameters.

³ t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See the ADuM4121-1 data sheet for waveforms of the propagation delay parameters.

⁴ t_{PSKHL} is the magnitude of the worst case difference in t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See the ADuM4121-1 data sheet for waveforms of the propagation delay parameters.

⁵ t_{PSKHL} is the magnitude of the worst case difference in t_{DLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See the ADuM4121-1 data sheet for waveforms of the propagation delay parameters.

⁶ Static common-mode transient immunity (CMTI) is defined as the largest dv/dt between GND_1 and GND_2 , with inputs held either high or low, such that the output voltage remains either above $0.8 \times V_{DD2}$ for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets.

⁷ Dynamic common-mode transient immunity (CMTI) is defined as the largest dv/dt between GND_1 and GND_2 with the switching edge coincident with the transient test pulse. Operation with transients above the recommended levels can cause momentary data upsets.

REGULATORY INFORMATION

The ADuM4121-1-EP is pending approval by the organizations listed in Table 2.

Table 2.

| UL (Pending) | CSA (Pending) | VDE (Pending) | CQC (Pending) |
|---|--|---|--|
| UL1577 Component Recognition Program Single Protection, 5000 V rms Isolation Voltage | Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 800 V rms (1131 V peak) Reinforced insulation at 400 V rms (565 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 means of patient protection (MOPP)), 500 V rms (707 V peak) Reinforced insulation (2 MOPP), 250 V rms (1414 V peak) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation at: 600 V rms mains, 800 V secondary (1089 V peak) Reinforced insulation at: 300 V rms mains, 400 V secondary (565 V peak) | DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Reinforced insulation, 849 V peak, $V_{IOSM} = 10\text{ kV peak}$ Basic insulation 849 V peak, $V_{IOSM} = 16\text{ kV peak}$ | Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 800 V rms (1131 V peak) Reinforced insulation at 400 V rms (565 V peak) |
| File E214100 | File 205078 | File 2471900-4880-0001 | File (pending) |

PACKAGE CHARACTERISTICS

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------|-----|-----------|-----|----------|
| Resistance (Input Side to High-Side Output) ¹ | R_{I-O} | | 10^{12} | | Ω |
| Capacitance (Input Side to High-Side Output) ¹ | C_{I-O} | | 2.0 | | pF |
| Input Capacitance | C_I | | 4.0 | | pF |

¹ The device is considered a two-terminal device: Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

| Parameter | Symbol | Value | Unit | Conditions |
|---|---------|----------|-------|--|
| Rated Dielectric Insulation Voltage | | 5000 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 8 min | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 8 min | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance) | L (PCB) | 8.3 min | mm | Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane |
| Minimum Internal Gap (Internal Clearance) | | 25.5 min | µm | Minimum distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 3 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

Table 5. VDE Characteristics

| Description | Test Conditions/Comments | Symbol | Characteristic | Unit |
|---|--|--------------------|------------------|--------|
| Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 600 V rms | | | I to IV | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Working Insulation Voltage | | V _{IORM} | 849 | V peak |
| Input to Output Test Voltage, Method B1 | V _{IORM} × 1.875 = V _{pd(m)} , 100% production test, t _{ini} = t _m = 1 sec, partial discharge < 5 pC | V _{pd(m)} | 1592 | V peak |
| Input to Output Test Voltage, Method A | | | | |
| After Environmental Tests Subgroup 1 | V _{IORM} × 1.5 = V _{pd(m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC | V _{pd(m)} | 1274 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | V _{IORM} × 1.2 = V _{pd(m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC | V _{pd(m)} | 1019 | V peak |
| Highest Allowable Overtoltage | | V _{IO7M} | 7000 | V peak |
| Surge Isolation Voltage Basic | VPEAK = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time | V _{IOSM} | 16,000 | V peak |
| Surge Isolation Voltage Reinforced | VPEAK = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time | V _{IOSM} | 10,000 | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 2) | | | |
| Maximum Junction Temperature | | T _s | 150 | °C |
| Safety Total Dissipated Power | | P _s | 1.2 | W |
| Insulation Resistance at T _s | V _{IO} = 500 V | R _s | >10 ⁹ | Ω |



Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Ambient Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 6.

| Parameter | Value |
|---|-----------------|
| Operating Temperature Range (T _j) | -55°C to +125°C |
| Supply Voltages | |
| V _{DD1} to GND ₁ | 2.5 V to 6.5 V |
| V _{DD2} to GND ₂ | 7.5 V to 35 V |

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 7.

| Parameter | Rating |
|--|--------------------------------------|
| Storage Temperature Range (T_{ST}) | -55°C to +150°C |
| Junction Operating Temperature Range (T_J) | -55°C to +125°C |
| Supply Voltages | |
| V_{DD1} to GND ₁ | -0.3 V to +7 V |
| V_{DD2} to GND ₂ | -0.3 V to +40 V |
| Input Voltages | |
| V_{I+} , V_{I-} ¹ | -0.3 V to +7 V |
| V_{CLAMP} ² | -0.3 V to $V_{DD2} + 0.3$ V |
| Output Voltages | |
| V_{OUT} ² | -0.3 V to $V_{DD2} + 0.3$ V |
| Common-Mode Transients ($ CM $) ³ | -200 kV/ μ s to +200 kV/ μ s |

¹ Rating assumes V_{DD1} is above 2.5 V. V_{I+} and V_{I-} are rated up to 6.5 V when V_{DD1} is unpowered.

² Referenced to GND₂, maximum of 40 V.

³ $|CM|$ refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Maximum Continuous Working Voltage¹

| Parameter | Rating | Unit | Constraint |
|-----------------------|--------|--------|---|
| AC Voltage | | | |
| Bipolar Waveform | | | |
| Basic Insulation | 849 | V peak | 50-year minimum insulation lifetime |
| Reinforced Insulation | 789 | V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Unipolar Waveform | | | |
| Basic Insulation | 1698 | V peak | 50-year minimum insulation lifetime |
| Reinforced Insulation | 849 | V peak | 50-year minimum insulation lifetime |
| DC Voltage | | | |
| Basic Insulation | 1118 | V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 558 | V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |

¹ Maximum continuous working voltage refers to continuous voltage magnitude imposed across the isolation barrier. See the ADuM4121-1 data sheet for more details.

Table 10. Truth Table

| V_{I-} | V_{I+} | V_{DD1} State | V_{DD2} State | V_{OUT} Output |
|------------|------------|-----------------|-----------------|------------------|
| Don't care | Low | Powered | Powered | Low |
| Low | High | Powered | Powered | High |
| High | Don't care | Powered | Powered | Low |
| Don't care | Don't care | Unpowered | Powered | Low |
| Don't care | Don't care | Powered | Unpowered | Low ¹ |

¹ The output is low, but not actively driven because the device is not powered.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 8. Thermal Resistance

| Package Type | θ_{JA} | Unit |
|---------------------|---------------|------|
| RI-8-1 ¹ | 104.2 | °C/W |

¹ Test Condition 1: thermal impedance simulated values are based on a 4-layer PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

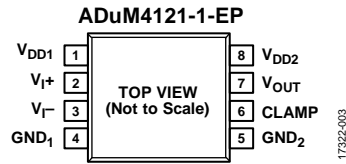


Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | V _{I+} | Noninverting Gate Drive Logic Input. |
| 3 | V _{I-} | Inverting Gate Drive Logic Input. |
| 4 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 5 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 6 | CLAMP | Miller Clamp and Gate Voltage Sense. Connect this pin directly to the gate being driven. |
| 7 | V _{OUT} | Gate Drive Output. Connect this pin to the gate being driven through an external series resistor. |
| 8 | V _{DD2} | Supply Voltage for Isolator Side 2. |

TYPICAL PERFORMANCE CHARACTERISTICS

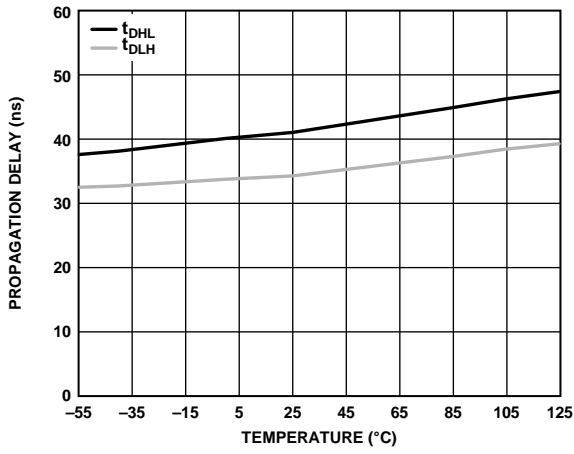


Figure 4. Propagation Delay vs. Temperature, 2 nF Load

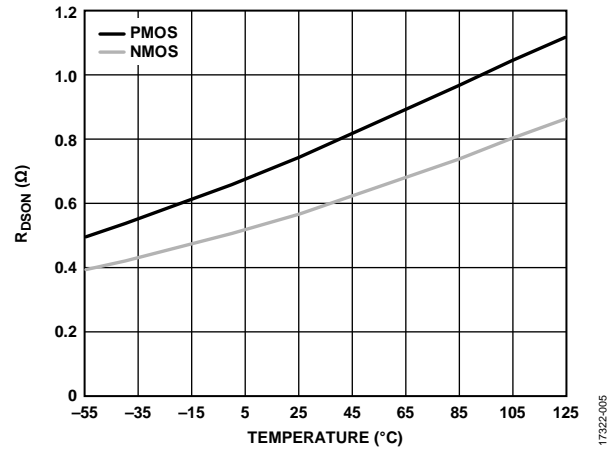
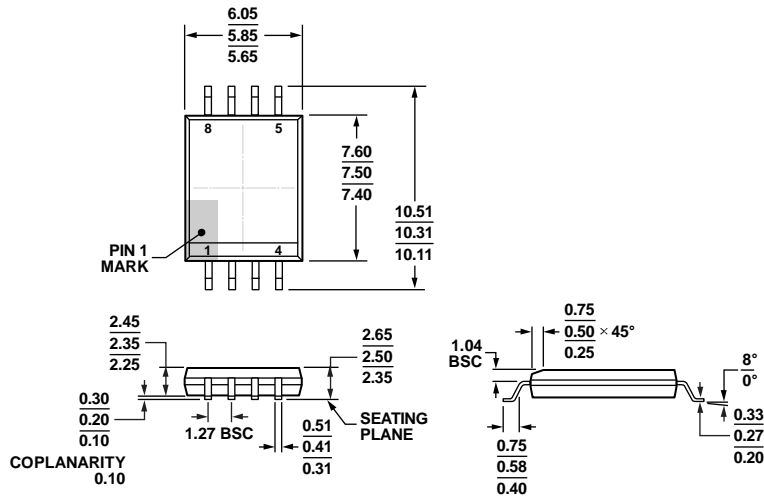


Figure 5. Output Resistance (R_{DSON}) vs. Temperature, V_{DD2} = 15 V

OUTLINE DIMENSIONS



09-17-2014-B

Figure 6. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] Wide Body (RI-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | No. of Channels | Output Peak Current (A) | Thermal Shutdown | Minimum Output Voltage (V) | Temperature Range | Package Description | Package Option |
|--------------------|-----------------|-------------------------|------------------|----------------------------|-------------------|---------------------|----------------|
| ADUM4121-1TRIZ-EP | 1 | 2 | No | 7.5 | -55°C to +125°C | 8-Lead SOIC_IC | RI-8-1 |
| ADUM4121-1TRIZ-EPR | 1 | 2 | No | 7.5 | -55°C to +125°C | 8-Lead SOIC_IC | RI-8-1 |

¹ Z = RoHS Compliant Part.

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