

Serial EEPROM Series Standard EEPROM

I²C BUS EEPROM (2-Wire)

BR24G512-3A

General Description

BR24G512-3A is a serial EEPROM of I²C BUS Interface Method

Features

- All controls available by 2 ports of serial clock (SCL) and serial data (SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 1.7V to 5.5V single power source operation most suitable for battery use
- 1.7V to 5.5V wide limit of operating voltage, possible 1MHz operation
- Page Write Mode useful for initial value write at factory shipment
- Self-timed Programming Cycle
- Low Current Consumption
- Prevention of Write Mistake
 - Write (Write Protect) Function added
 - Prevention of Write Mistake at Low Voltage
- More than 1 million write cycles
- More than 40 years data retention
- Noise filter built in SCL / SDA terminal
- Initial delivery state FFh

Packages W(Typ) x D(Typ)x H(Max)



Figure 1.

Page Write

age Wille	
Number of Pages	128 Bytes
Product number	BR24G512-3A

BR24G512-3A

12+0012-0A						
Capacity	Bit Format	Туре	Power Supply Voltage	Package		
	BR24G512-3A		DIP-T8			
E10Khit	12Kbit 64K×8	BR24G512F-3A	1.7V to 5.5V	SOP8		
STANDIL		BR24G512FJ-3A	1.7 V 10 5.5 V	SOP-J8		
	BR24G512FVT-3A		TSSOP-B8			

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	Vcc	-0.3 to +6.5	V	
		0.45 (SOP8)		Derate by 4.5mW/°C when operating above Ta=25°C
Dower Dissipation	Dd	0.45 (SOP-J8)	W	Derate by 4.5mW/°C when operating above Ta=25°C
Power Dissipation	Pd	0.33 (TSSOP-B8)	VV	Derate by 3.3mW/°C when operating above Ta=25°C
		0.80 (DIP-T8)		Derate by 8.0mW/°C when operating above Ta=25°C
Storage Temperature	Tstg	-65 to +150	°C	
Operating Temperature	Topr	-40 to +85	°C	
Input Voltage / Output Voltage	-	-0.3 to Vcc+1.0	V	The Max value of Input voltage/Output voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Input voltage/Output voltage is not lower than -1.0V.
Junction Temperature	Tjmax	150	°C	Junction temperature at the storage condition
Electrostatic discharge voltage (human body model)	V _{ESD}	-4000 to +4000	V	

Memory Cell Characteristics (Ta=25°C, Vcc=1.7V to 5.5V)

Parameter		Unit		
Farameter	Min	Тур	Max	Offic
Write Cycles (1)	1,000,000	-	-	Times
Data Retention (1)	40	-	-	Years

(1) Not 100% TESTED

Recommended Operating Ratings

Parameter	Symbol	Rating	Unit
Power Source Voltage	Vcc	1.7 to 5.5	\/
Input Voltage	Vin	0 to Vcc	V

DC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, Vcc =1.7V to 5.5V)

Donomotor	Cymah al		Limit		l lmit	Conditions
Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Input High Voltage1	V _{IH1}	0.7Vcc	-	Vcc+1.0	V	
Input Low Voltage1	V _{IL1}	-0.3 ⁽²⁾	-	+0.3Vcc	V	
Output Low Voltage1	V _{OL1}	-	-	0.4	>	I _{OL} =3.0mA, 2.5V≦Vcc≦5.5V (SDA)
Output Low Voltage2	V _{OL2}	-	-	0.2	٧	I _{OL} =0.7mA, 1.7V≦Vcc<2.5V (SDA)
Input Leakage Current	lu	-1	-	+1	μΑ	V _{IN} =0 to Vcc
Output Leakage Current	ILO	-1	-	+1	μΑ	V _{OUT} =0 to Vcc (SDA)
Supply Current (Write)	Icc ₁	-	-	4.5	mA	Vcc=5.5V,fscl=1MHz, twr=5ms, Byte write, Page write
Supply Current (Read)	Icc2	-	-	2.0	mA	Vcc=5.5V,f _{SCL} =1MHz Random read, current read, Sequential read
Standby Current	I _{SB}	-	-	3.0	μA	Vcc=5.5V, SDA · SCL=Vcc A0,A1,A2=GND,WP=GND

⁽²⁾ When the pulse width is 50ns or less, it is -1.0V.

AC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, Vcc=1.7V to 5.5V)

Parameter	Symbol		Limit			
Parameter	Symbol	Min	Тур	Max	Unit	
Clock Frequency	fscL	-	-	1000	kHz	
Data Clock "HIGH" Period	t _{HIGH}	0.30	-	-	μs	
Data Clock "LOW" Period	tLOW	0.5	-	-	μs	
SDA, SCL (INPUT) Rise Time (1)	t _R	-	-	0.12	μs	
SDA, SCL (INPUT) Fall Time (1)	t _{F1}	-	-	0.12	μs	
SDA (OUTPUT) Fall Time (1)	t _{F2}	-	-	0.12	μs	
Start Condition Hold Time	t _{HD:STA}	0.25	-	-	μs	
Start Condition Setup Time	tsu:sta	0.20	-	-	μs	
Input Data Hold Time	t _{HD:DAT}	0	-	-	ns	
Input Data Setup Time	tsu:dat	50	-	-	ns	
Output Data Delay Time	t _{PD}	0.05	-	0.45	μs	
Output Data Dold Time	t _{DH}	0.05	-	-	μs	
Stop Condition Setup Time	t su:sто	0.25	-	-	μs	
Bus Free Time	t _{BUF}	0.5	-	-	μs	
Write Cycle Time	twr	-	-	5	ms	
Noise Spike Width (SDA, SCL)	tı	-	-	0.05	μs	
WP Hold Time	t _{HD:WP}	1.0		-	μs	
WP Setup Time	tsu:wp	0.1	-	-	μs	
WP High Period	t _{HIGH:WP}	1.0	-	-	μs	

⁽¹⁾ Not 100% tested

AC Characteristics Condition

<u> </u>			
Parameter	Symbol	Conditions	Unit
Load Capacitance	CL	100	pF
SDA, SCL (INPUT) Rise Time	t _R	20	ns
SDA, SCL (INPUT) Fall Time	t _{F1}	20	ns
Input Data Level	V _{IL1} /V _{IH1}	0.2Vcc/0.8Vcc	V
Input/Output Data Timing Reference Level	-	0.3Vcc/0.7Vcc	V

Serial Input / Output Timing

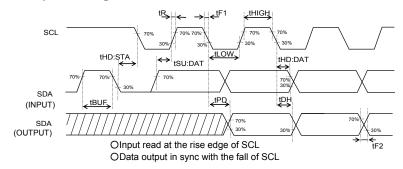


Figure 2-(a). Serial Input / Output Timing

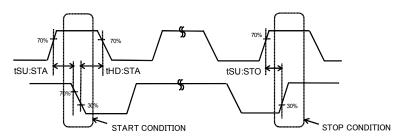
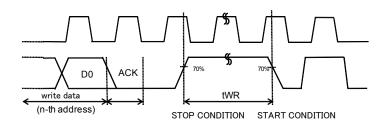


Figure 2-(b). Start-Stop Bit Timing



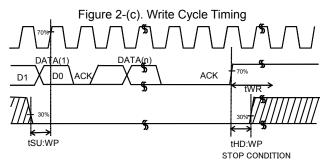


Figure 2-(d). WP Timing at Write Execution

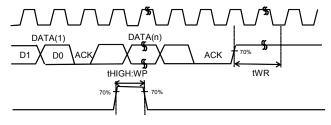


Figure 2-(e). WP Timing at Write Cancel

Block Diagram

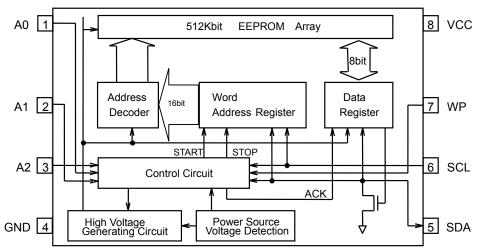
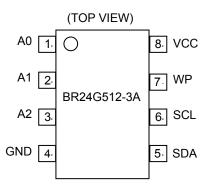


Figure 3. Block Diagram

Pin Configuration



Pin Descriptions

Terminal	Input/	Descriptions
Name	Output	Boomptions
A0	Input	Slave address setting*
A1	Input	Slave address setting*
A2	Input	Slave address setting*
GND	-	Reference voltage of all input / output, 0V
SDA	Input/ Output	Serial data input serial data output
SCL	Input	Serial clock input
WP	Input	Write protect terminal
VCC	-	Connect the power source

*A0,A1 and A2 are not allowed to use as open.

Typical Performance Curves

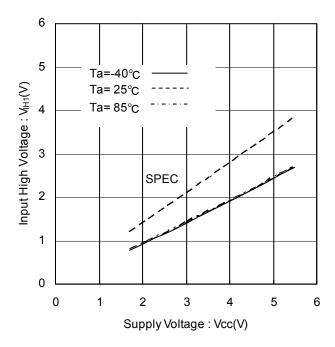


Figure 4. Input High Voltage vs Supply Voltage (A0,A1,A2,SCL,SDA,WP)

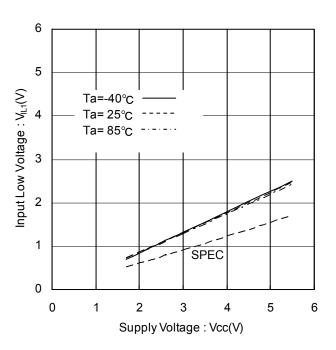


Figure 5. Input Low Voltage vs Supply Voltage (A0, A1, A2, SCL, SDA, WP)

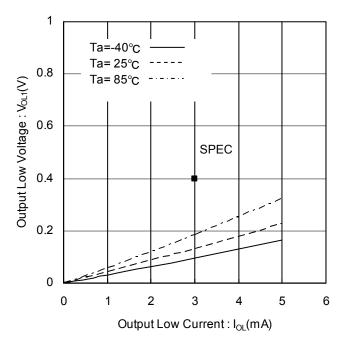


Figure 6. Output Low Voltage1 vs Output Low Current (Vcc=2.5V)

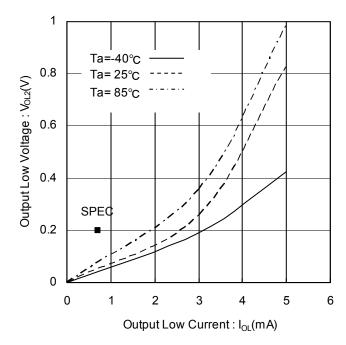


Figure 7. Output Low Voltage2 vs Output Low Current (Vcc=1.7V)

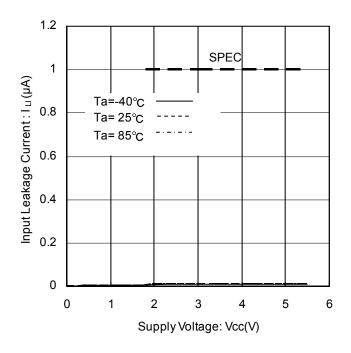


Figure 8. Input Leakage Current vs Supply Voltage (A0, A1, A2, SCL, WP)

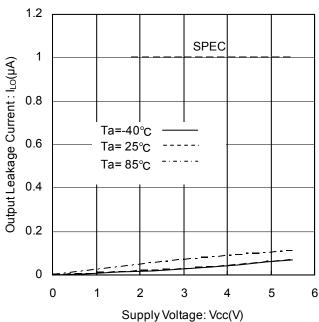


Figure 9. Output Leakage Current vs Supply Voltage (SDA)

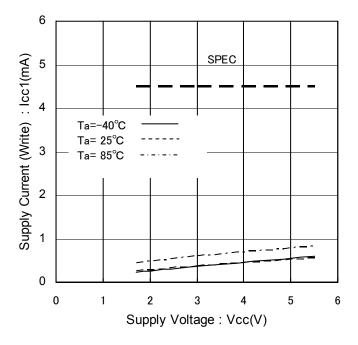


Figure 10. Supply Current (Write) vs Supply Voltage (f_{SCL}=1MHz)

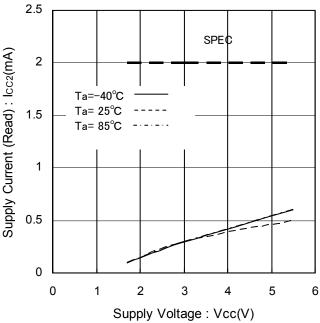


Figure 11. Supply Current (Read) vs Supply Voltage (f_{SCL}=1MHz)

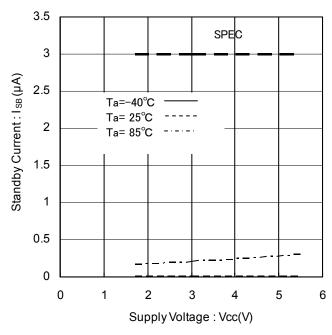


Figure 12. Standby Current vs Supply Voltage (BR24G1M-3A)

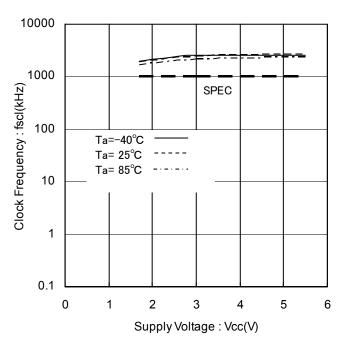


Figure 13. Clock Frequency vs Supply Voltage

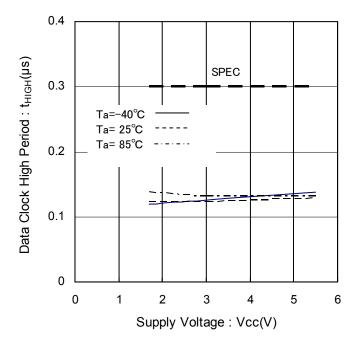


Figure 14. Data Clock High Period vs Supply Voltage

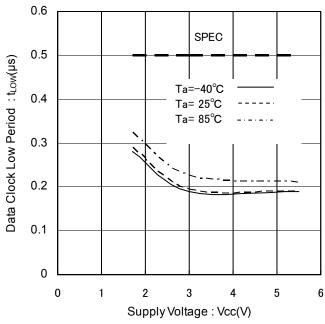


Figure 15. Data Clock Low Period vs Supply Voltage

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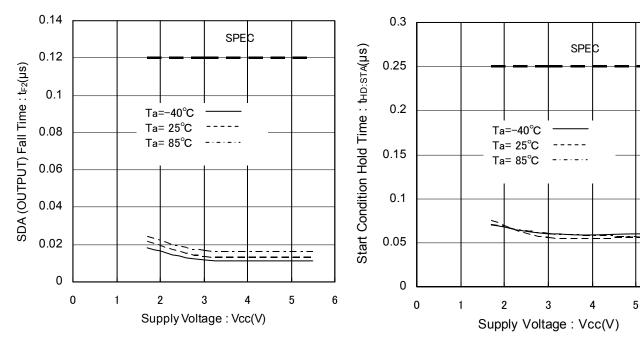


Figure 16. SDA (OUTPUT) Fall Time vs Supply Voltage

Figure 17. Start Condition Hold Time vs Supply Voltage

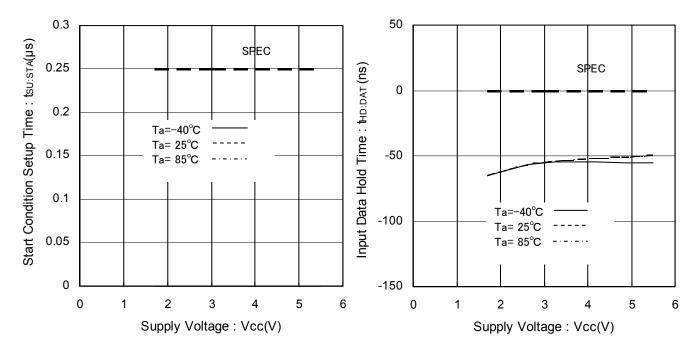


Figure 18. Start Condition Setup Time vs Supply Voltage

Figure 19. Input Data Hold Time vs Supply Voltage (HIGH)

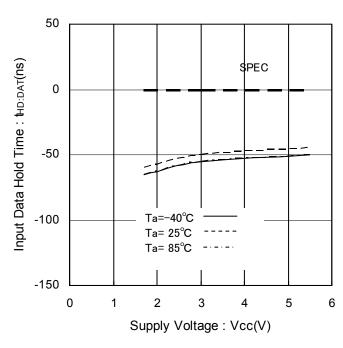


Figure 20. Input Data Hold Time vs Supply Voltage (LOW)

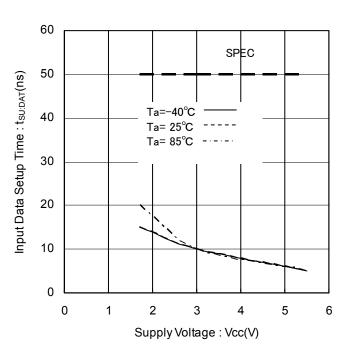


Figure 21. Input Data Setup Time vs Supply Voltage (HIGH)

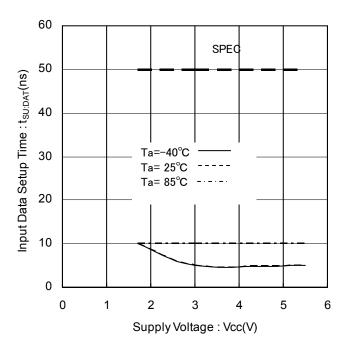


Figure 22. Input Data Setup Time vs Supply Voltage (LOW)

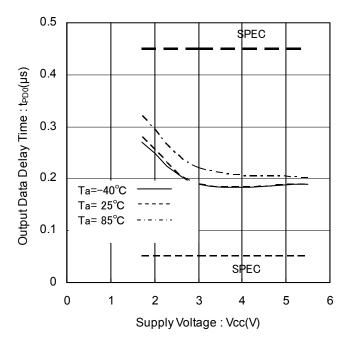


Figure 23. Output Data Delay Time vs Supply Voltage

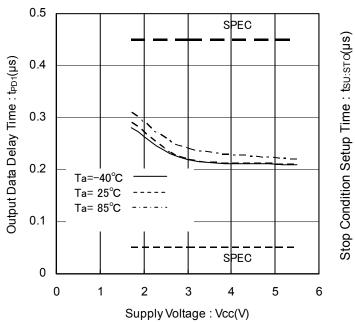


Figure 24. Output Data Delay Time vs Supply Voltage

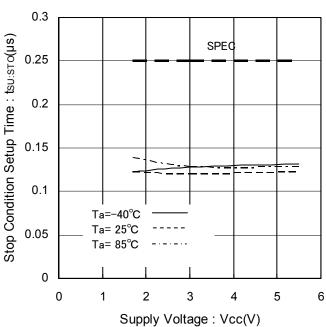


Figure 25. Stop Condition Setup Time vs Supply Voltage

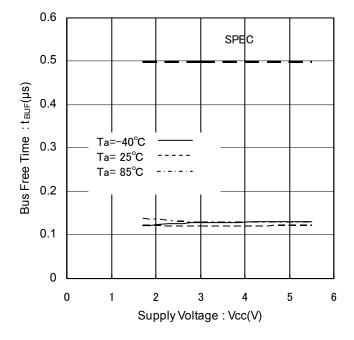


Figure 26. Bus Free Time vs Supply Voltage

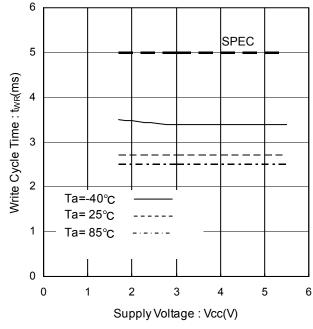


Figure 27. Write Cycle Time vs Supply Voltage

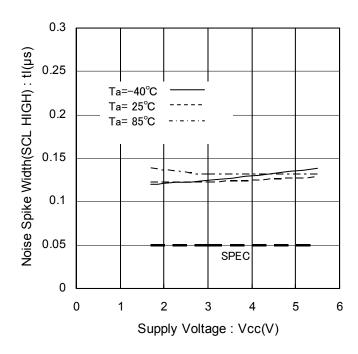


Figure 28. Noise Spike Width vs Supply Voltage (SCL HIGH)

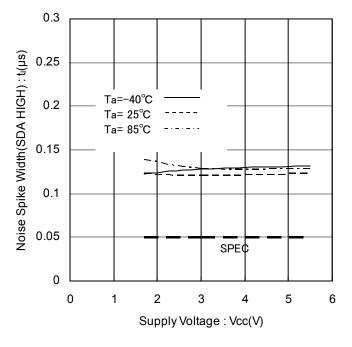


Figure 30. Noise Spike Width vs Supply Voltage (SDA HIGH)

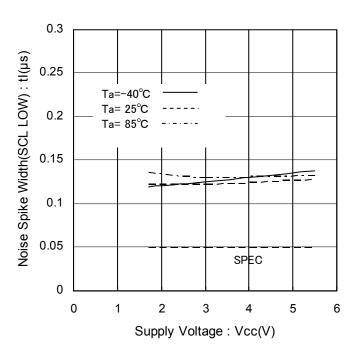


Figure 29. Noise Spike Width vs Supply Voltage (SCL LOW)

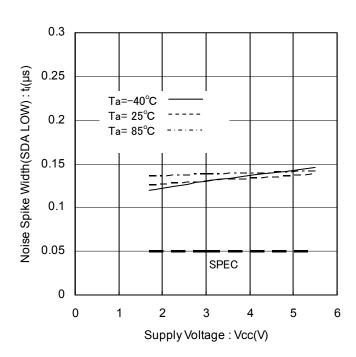


Figure 31. Noise Spike Width vs Supply Voltage (SDA LOW)

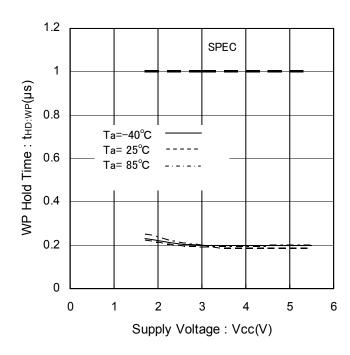


Figure 32. WP Hold Time vs Supply Voltage

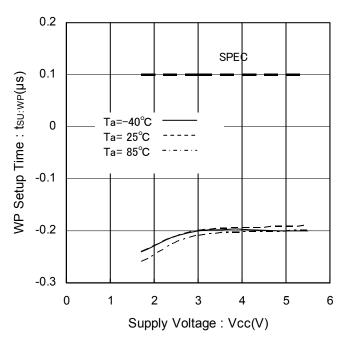


Figure 33. WP Setup Time vs Supply Voltage

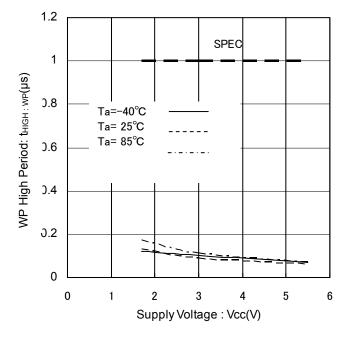


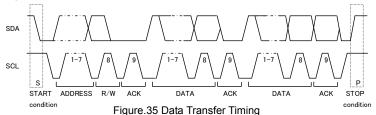
Figure 34. WP High Period vs Supply Voltage

Timing Chart

1. I2C BUS Data Communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS data communication with several devices is possible by connecting with 2 communication lines: serial data (SDA) and serial clock (SCL).

Among the devices, there should be a "master" that generates clock and control communication start and end. The rest become "slave" which are controlled by an address peculiar to each device, like this EEPROM. The device that outputs data to the bus during data communication is called "transmitter", and the device that receives data is called "receiver".



2. Start Condition (Start Bit Recognition)

- (1) Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- (2) This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command cannot be executed.

3. Stop Condition (Stop Bit Recognition)

(1) Each command can be ended by a stop condition (stop bit) where SDA goes from 'LOW' to 'HIGH' while SCL is 'HIGH'.

4. Acknowledge (ACK) Signal

- (1) This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master-slave communication, the device (Ex. μ-COM sends slave address input for write or read command to this IC) at the transmitter (sending) side releases the bus after output of 8bit data.
- (2) The device (Ex. This IC receives the slave address input for write or read command from the μ-COM) at the receiver (receiving) side sets SDA 'LOW' during 9th clock cycle, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- (3) This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- (4) After receiving 8bit data (word address and write data) during each write operation, this IC outputs acknowledge signal (ACK signal) 'LOW'.
- (5) During read operation, this IC outputs 8bit data (read data) and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ-COM) side, this IC continues to output data. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, recognizes stop condition (stop bit), and ends read operation. Then this IC becomes ready for another trasmission.

5. Device Addressing

- (1) Slave address comes after start condition from master.
- (2) The significant 4 bits of slave address are used for recognizing a device type. The device code of this IC is fixed to '1010'.
- (3) Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
- (4) The most insignificant bit (R/W --- READ / WRITE) of slave address is used for designating write or read operation, and is as shown below

Setting R / \overline{w} to 0 ------ write (setting 0 to word address setting of random read) Setting R / \overline{w} to 1 ------ read

Туре	Slave address	Maximum number of Connected buses
BR24G512-3A	1 0 1 0 A2 A1 A0 R/W	8

Write Command

1. Write Cycle

(1) Arbitrary data can be written to EEPROM. When writing only 1 byte, Byte Write is normally used, and when writing continuous data of 2 bytes or more, simultaneous write is possible by Page Write cycle. The maximum number of write bytes is specified per device of each capacity.

Up to 128 arbitrary bytes can be written.

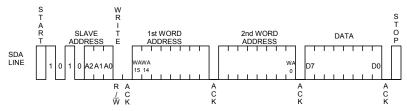


Figure.36 Byte Write Cycle

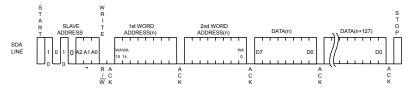


Figure 37. Page Write Cycle

- (2) During internal write execution, all input commands are ignored, therefore ACK is not returned.
- (3) Data is written to the address designated by word address (n-th address)
- (4) By issuing stop bit after 8bit data input, internal write to memory cell starts.
- (5) When internal write is started, command is not accepted for two (5ms at maximum).
- (6) Using page write cycle, the following can be written in bulk:

Up to 64Byte (BR24G128-3A, BR24G256-3A)

Up to 256Byte (BR24G1M-3A)

The bytes in excess overwrite the data already sent first.

(Refer to "Internal Address Increment")

(7) As for page write cycle of BR24G512-3A, where 2 or more bytes of data is intended to be written, after the 9 significant bits of word address are designated arbitrarily, only the value of 7 least significant bits in the address is incremented internally, so that data up to 128 bytes of memory only can be written.

2. Notes on Write Cycle Continuous Input

List of Numbers of Page Write

Number of Pages	128Byte
Product number	BR24G512-3A

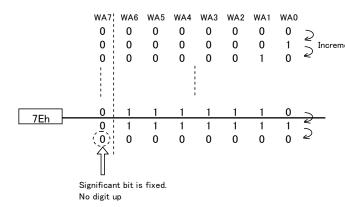
The above numbers are maximum bytes for respective types.

Any bytes below these can be written.

In the case BR24G512-3A, 1 page=128bytes, but the page write cycle time is 5ms at maximum for 128byte bulk write. It does not stand 5ms at maximum × 128byte=640ms(Max)

3. Internal Address Increment

Page Write Mode



For example, when it is started from address 3Eh, then, increment is made as below,

7Eh→7Fh→00h→01h··· please take note.

%7Eh \cdots 7E in hexadecimal, therefore, 01111110 becomes a binary number.

4. Write Protect (WP) Terminal

Write Protect (WP) Function

When WP terminal is set at Vcc(H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not leave it open.

In case of using it as ROM, it is recommended to connect it to pull up or Vcc.

At extremely low voltage at power ON/OFF, by setting the WP terminal 'H', write error can be prevented.

Read Command

1. Read Cycle

Read cycle is when data of EEPROM is read. Read cycle could be random read cycle or current read cycle. Random read cycle is a command to read data by designating a specific address, and is used generally. Current read cycle is a command to read data of internal address register without designating an address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available where the next address data can be read in succession.

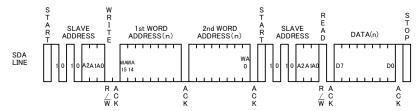


Figure.38 Random Read Cycle

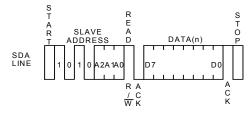


Figure.39 Current Read Cycle

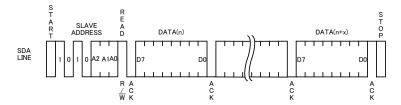


Figure.40 Sequential Read Cycle (in the case of current read cycle)

- (1) In random read cycle, data of designated word address can be read.
- (2) When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th, i.e. data of the (n+1)-th address is output.
- (3) When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ-COM) side, the next address data can be read in succession.
- (4) Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal goes from 'L' to 'H' while at SCL signal is 'H'.
- (5) When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output. Therefore, read command cycle cannot be ended. To end read command cycle, be sure to input 'H' to ACK signal after D0, and the stop condition where SDA goes from 'L' to 'H' while SCL signal is 'H'.
- (6) Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is asserted from 'L' to 'H' while SCL signal is 'H'.

Software Reset

Software reset is executed to avoid malfunction after power ON, and during command input. Software reset has several kinds and 3 kinds of them are shown in the figure below. (Refer to Figure 41-(a), Figure 41-(b), Figure 41-(c)) Within the dummy clock input area, the SDA bus is released ('H' by pull up) and ACK output and read data '0' (both 'L' level) may be output from EEPROM. Therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

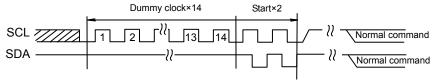


Figure 41-(a). The Case of Dummy Clock × 14 +START+START+ Command Input

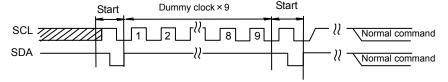
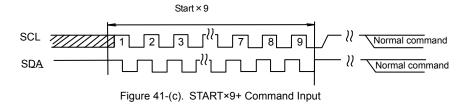


Figure 41-(b). The Case of START + Dummy Clock × 9 +START+ Command Input



XStart command from START input.

Acknowledge Polling

During internal write execution, all input commands are ignored, therefore ACK is not returned. During internal automatic write execution after write cycle input, next command (slave address) is sent. If the first ACK signal sends back 'L', then it means end of write operation, else 'H' is returned, which means writing is still in progress. By the use of acknowledge polling, next command can be executed without waiting for twe = 5ms.

To write continuously, $R/\overline{W} = 0$, then to carry out current read cycle after write, slave address with $R/\overline{W} = 1$ is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

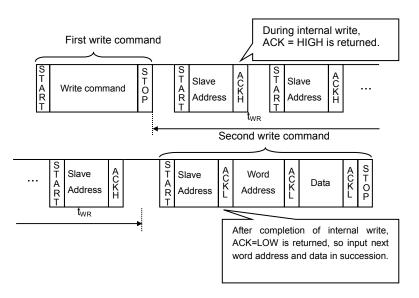


Figure 42. Case to Continuous Write by Acknowledge Polling

WP Valid Timing (Write Cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so on, pay attention to the following WP valid timing. During write cycle execution, inside cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to take in D0 of data(in page write cycle, the first byte data) is the cancel invalid area.

WP input in this area becomes 'Don't care'. The area from the rise of SCL to take in D0 to the stop condition input is the cancel valid area. Furthermore, after the execution of forced end by WP, the IC enters standby status..

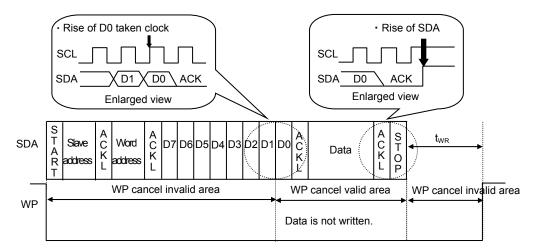


Figure 43. WP Valid Timing

Command Cancel by Start Condition and Stop Condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Figure 44.) However, within ACK output area and during data read, SDA bus may output 'L'. In this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. When command is cancelled by start-stop condition during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined. Therefore, it is not possible to carry out current read cycle in succession. To carry out read cycle in succession, carry out random read cycle.

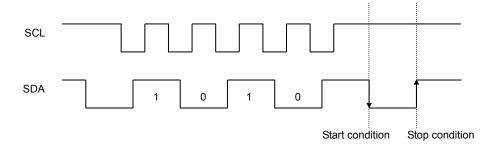


Figure 44. Case of Cancel by Start, Stop Condition during Slave Address Input

I/O Peripheral Circuit

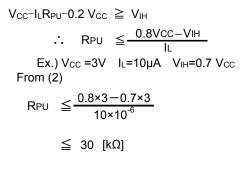
1. Pull-up Resistance of SDA Terminal

SDA is NMOS open drain, so it requires a pull up resistor. As for this resistor value (R_{PU}), select an appropriate value from microcontroller V_{IL} , I_L , and V_{OL} - I_{OL} characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU} , the larger is the supply current (Read).

2. Maximum Value of RPU

The maximum value of RPU is determined by the following factors.

- (1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line and R_{PU} of SDA should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.
- (2) The bus electric potential 🐧 to be determined by input current leak total (I_L) of the device connected to the bus with output of 'H' to SDA line and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin of 0.2Vcc.



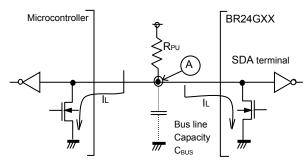


Figure.45 I/O Circuit Diagram

3. Minimum Value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1) When IC outputs LOW, it should be satisfied that V_{OLMAX} =0.4V and I_{OLMAX} =3mA.

$$\frac{\text{Vcc-Vol}}{\text{RPU}} \le \text{IoL}$$

$$\therefore$$
 RPU $\geq \frac{Vcc-Vol}{lol}$

(2) V_{OLMAX}=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin 0.1V_{CC}.

Ex.) V_{CC} =3V, V_{OL}=0.4V, I_{OL}=3mA, microcontroller, EEPROM V_{IL}=0.3Vcc

From (1)
$$R_{PU} \ge \frac{3-0.4}{3\times10^{-3}}$$
 $\ge 867 \ [\Omega]$ And $V_{OL}=0.4 \ [V]$ $V_{IL}=0.3\times3$ $=0.9 \ [V]$

Therefore, the condition (2) is satisfied.

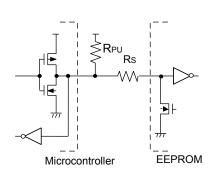
4. Pull-up Resistance of SCL Terminal

When SCL control is made at the CMOS output port, there is no need for a pull up resistor. But when there is a time where SCL becomes 'Hi-Z', add a pull up resistor. As for the pull up resistor value, one of several $k\Omega$ to several ten $k\Omega$ is recommended in consideration of drive performance of output port of microcontroller.

Cautions on Microcontroller Connection

1. Rs

In I 2 C BUS, it is recommended that SDA port is of open drain input/output. However, when using CMOS input / output of tri state to SDA port, insert a series resistance R $_8$ between the pull up resistor R $_{PU}$ and the SDA terminal of EEPROM. This is to control over current that may occur when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. R $_8$ also plays the role of protecting the SDA terminal against surge. Therefore, even when SDA port is open drain input/output, R $_8$ can be used.



SCL

SDA

'H' output of microcontroller

Over current flows to SDA line by 'H' output of microcontroller and 'L' output of EEPROM.

Figure 46. I/O Circuit Diagram

Figure 47. Input / Output Collision Timing

2. Maximum Value of Rs

The maximum value of Rs is determined by the following relations.

- (1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line and R_{PU} of SDA should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.
- (2) The bus electric potential ♠ to be determined by R_{PU} and R_S the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin of 0.1Vcc.

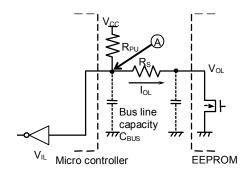


Figure 48. I/O Circuit Diagram

$$\frac{(\text{Vcc-Vol}) \times \text{Rs}}{\text{RPU+Rs}} + \text{Vol+0.1Vcc} \leq \text{Vil}$$

$$\therefore \text{Rs} \leq \frac{\text{Vil-Vol-0.1Vcc}}{1.1 \text{Vcc-Vil}} \times \text{RPU}$$

Ex.)Vcc=3V VIL=0.3Vcc VoL=0.4V Rpu=20k
$$\Omega$$

Rs
$$\leq \frac{0.3 \times 3 - 0.4 - 0.1 \times 3}{1.1 \times 3 - 0.3 \times 3} \times 20 \times 10^{3}$$

 $\leq 1.67 [k\Omega]$

3. Minimum Value of Rs

The minimum value of R_S is determined by over current at bus collision. When over current flows, noises in power source line and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of the impedance of power source line in set and so forth. Set the over current to EEPROM at 10mA or lower.

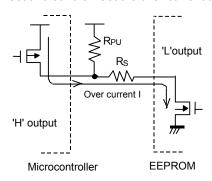
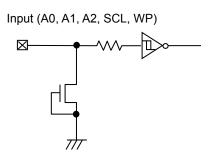


Figure 49. I/O Circuit Diagram

I/O Equivalence Circuit





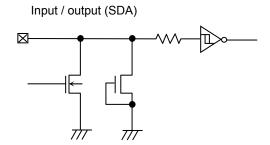


Figure 51. Input / Output Pin Circuit Diagram

Power-Up / Down Conditions

At power on, the IC's internal circuits may go through unstable low voltage area as the Vcc rises, making the IC's internal logic circuit not completely reset, hence, malfunction may occur. To prevent this, the IC is equipped with POR circuit and LVCC circuit. To assure the operation, observe the following conditions at power ON.

- 1. Set SDA = 'H' and SCL ='L' or 'H'
- 2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and V_{bot} for operating POR circuit.

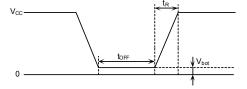
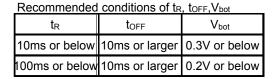


Figure 52. Rise Waveform Diagram



3. Set SDA and SCL so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

- (1) In the case when the above condition 1 cannot be observed such that SDA becomes 'L' at power ON.
 - →Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

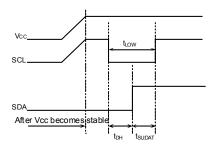


Figure 53. When SCL= 'H' and SDA= 'L'

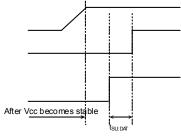


Figure 54. When SCL='L' and SDA='L'

- (2) In the case when the above condition 2 cannot be observed.
 - →After power source becomes stable, execute software reset(Page18).
- (3) In the case when the above conditions 1 and 2 cannot be observed.
 - →Carry out (1), and then carry out (2).

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power, and prevents write error. At LVCC voltage (Typ =1.2V) or below, data rewrite is prevented.

Noise Countermeasures

1. Bypass Capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, it is recommended to attach a bypass capacitor $(0.1\mu\text{F})$ between the IC's V_{CC} and GND pins. Attach it as close to the IC as possible. In addition, it is also recommended to attach a bypass capacitor between board's V_{CC} and GND.

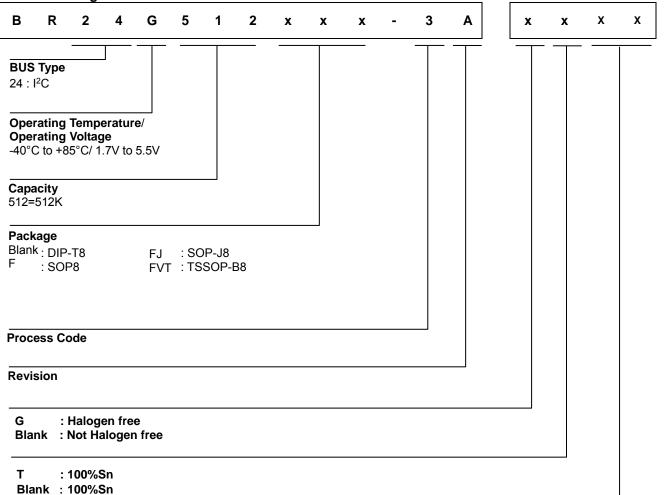
Operational Notes

- 1. Described numeric values and data are design representative values, and the values are not guaranteed.
- 2. We believe that the application circuit examples in this document are recommendable. However, in actual use, confirm characteristics further sufficiently. If changing the fixed number of external parts is desired, make your decision with sufficient margin in consideration of static characteristics, transient characteristics, and fluctuations of external parts and our LSI.
- 3. Absolute Maximum Ratings

If the absolute maximum ratings such as supply voltage, operating temperature range, and so on are exceeded, LSI may be destroyed. Do not supply voltage or subject the IC to temperatures exceeding the absolute maximum ratings. In the case of fear of exceeding the absolute maximum ratings, take physical safety countermeasures such as adding fuses, and see to it that conditions exceeding the absolute maximum ratings should not be supplied to the LSI.

- 4. GND Electric Potential
 - Set the voltage of GND terminal lowest at any operating condition. Make sure that each terminal voltage is not lower than that of GND terminal.
- 5. Thermal design
 - Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.
- 6. Short between Pins and Mounting Errors
 - Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.
- 7. Operating the IC in the presence of strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

Part Numbering



Packaging and Forming Specification

E2 : Embossed tape and reel

(SOP8,SOP-J8, TSSOP-B8)

None : Tube

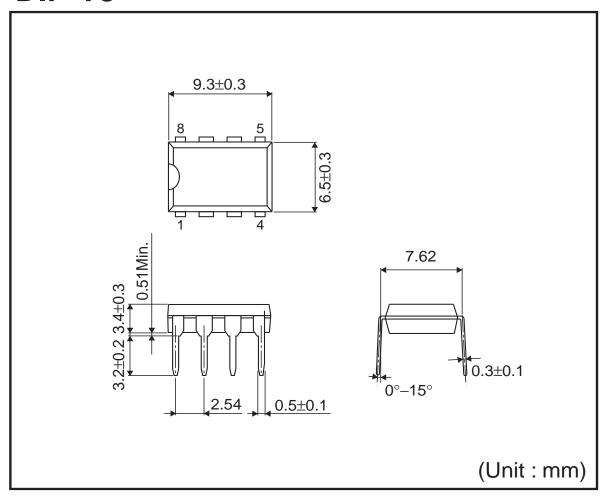
(DIP-T8)

●Lineup

Canacity	Packa	Package		lumbor	Remark	
Capacity	Туре	Quantity	Orderable Part Number			
	DIP-T8	Tube of 2000	BR24G512	-3A	Not Halogen free	100% Sn
512K	SOP8	Reel of 2500	BR24G512F	-3AGTE2	Halogen free	100% Sn
312K	SOP-J8	Reel 01 2500	BR24G512FJ	-3AGTE2	Halogen free	100% Sn
	TSSOP-B8	Reel of 3000	BR24G512FVT	-3AGE2	Halogen free	100% Sn

Physical Dimensions Tape and Reel Information

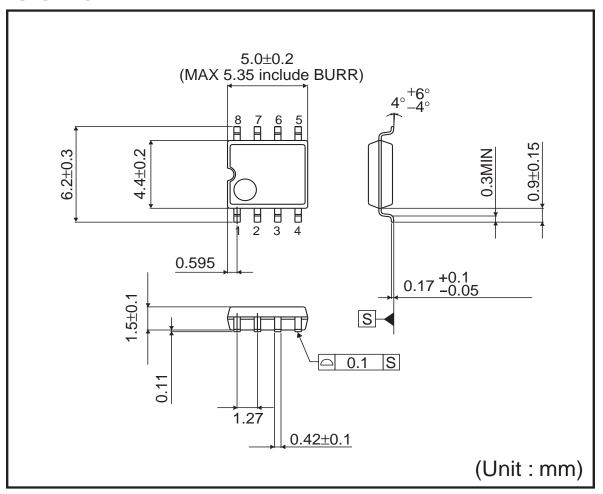
DIP-T8

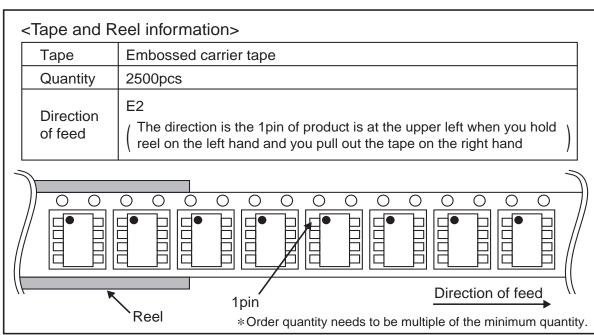


<tape and="" information="" reel=""></tape>						
Container	Tube					
Quantity	2000pcs					
Direction of feed	Direction of products is fixed in a container tube					
	*Order quantity needs to be multiple of the minimum quantity.					

Physical Dimensions Tape and Reel Information - comtinued

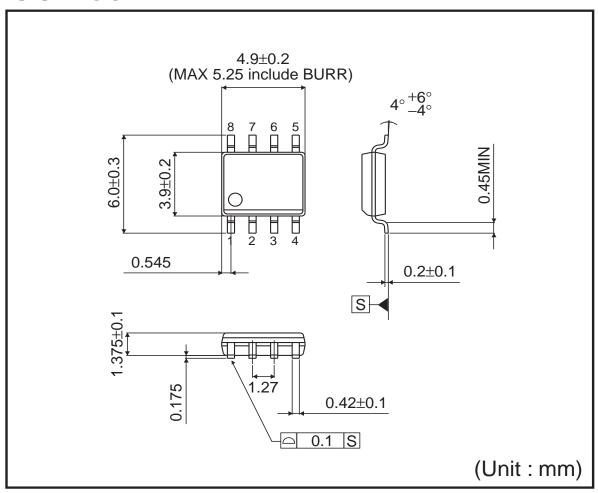
SOP8

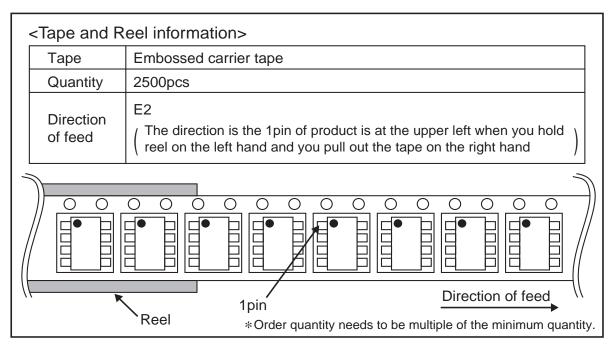




Physical Dimensions Tape and Reel Information - comtinued

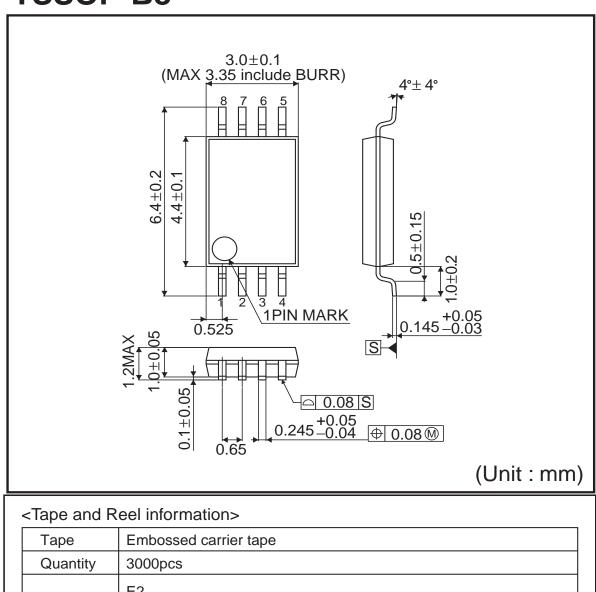
SOP-J8



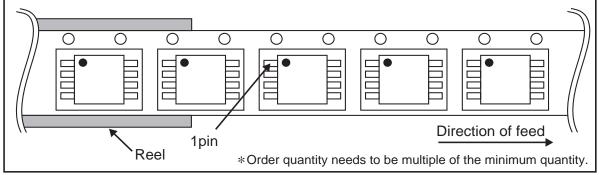


Physical Dimensions Tape and Reel Information - comtinued

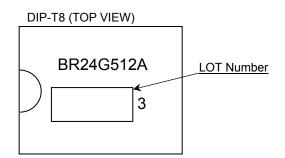
TSSOP-B8

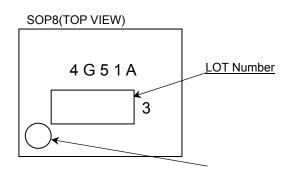


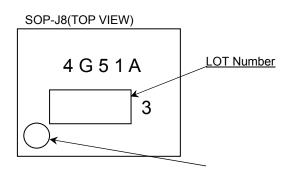
	Tape	Embossed carrier tape
	Quantity	3000pcs
•	Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand

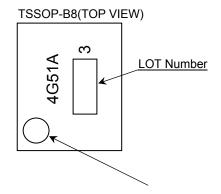


Marking Diagrams









Revision History

Date	Revision	Changes	
30.Aug.2012	001	New Release	
25.Feb.2013	002	Update some English words, sentences' descriptions, grammar and formatting. Delete SSOP-B8, TSSOP-B8J from Packaging and Forming Specification.	
08.May.2013	003	P1 Change format of package line-up table. Update wrong description of bit format. P5 Add directions in Pin Descriptions	
24.May.2014	004	P2 Add VESD in Absolute Maximum Ratings P2 Change Unit mW to W in Power Dissipation P3 Change Start Condition Setup Time from 0.25us to 0.20us. P24. Update Part Numbering. Add Lineup table.	

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(Note1) Medical Equipment Classification of the Specific Applications

JÁPAN	USA	EU	CHINA
CLASSII	CLASSIII	CLASSIIb	OL ACOM
CLASSIV		CLASSⅢ	CLASSⅢ

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 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
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- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
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- 7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
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For details, please refer to ROHM Mounting specification

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Rev.001



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- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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