

# PTN3460I

eDP to LVDS bridge for industrial and embedded applications

Rev. 2.1 — 16 August 2016

Product data sheet

## 1. General description

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PTN3460I is an (embedded) DisplayPort to LVDS bridge device that enables connectivity between an (embedded) DisplayPort (eDP) source and LVDS display panel. It processes the incoming DisplayPort (DP) stream, performs DP to LVDS protocol conversion and transmits processed stream in LVDS format.

PTN3460I has two high-speed ports: Receive port facing DP Source (for example, CPU/GPU/chip set), Transmit port facing the LVDS receiver (for example, LVDS display panel controller). The PTN3460I can receive DP stream at link rate 1.62 Gbit/s or 2.7 Gbit/s and it can support 1-lane or 2-lane DP operation. It interacts with DP source via DP Auxiliary (AUX) channel transactions for DP link training and setup.

It supports single bus or dual bus LVDS signaling with color depths of 18 bits per pixel or 24 bits per pixel and pixel clock frequency up to 112 MHz. The LVDS data packing can be done either in VESA or JEIDA format. Also, the DP AUX interface transports I<sup>2</sup>C-over-AUX commands and support EDID-DDC communication with LVDS panel. To support panels without EDID ROM, the PTN3460I can emulate EDID ROM behavior avoiding specific changes in system video BIOS.

PTN3460I is suitable for industrial design due to its wide temperature range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

PTN3460I provides high flexibility to optimally fit under different platform environments. It supports three configuration options: multi-level configuration pins, DP AUX interface, and I<sup>2</sup>C-bus interface.

PTN3460I can be powered by either 3.3 V supply only or dual supplies (3.3 V/1.8 V) and is available in the HVQFN56 7 mm × 7 mm package with 0.4 mm pitch.

## 2. Features and benefits

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### 2.1 Device features

- Embedded microcontroller and on-chip Non-Volatile Memory (NVM) allow for flexibility in firmware updates
- LVDS panel power-up (/down) sequencing control
- Firmware controlled panel power-up (/down) sequence timing parameters
- No external timing reference needed
- EDID ROM emulation to support panels with no EDID ROM. Emulation ON/OFF is set via configuration pin CFG4 (see [Table 14](#) for more details)
  - ◆ Supports EDID structure v1.3
  - ◆ On-chip EDID emulation up to seven different EDID data structures



- eDP complying PWM signal generation or PWM signal pass through from eDP source

## 2.2 DisplayPort receiver features

- Compliant to DP v1.2a and v1.1a
- Compliant to eDP v1.2 and v1.1
- Supports Main Link operation with one or two lanes (select through configuration pin CFG3, see [Table 4](#) for more details)
- Supports Main Link rate: Reduced Bit Rate (1.62 Gbit/s) and High Bit Rate (2.7 Gbit/s)
- Supports 1 Mbit/s AUX channel
  - ◆ Supports Native AUX and I<sup>2</sup>C-over-AUX transactions
- Supports down spreading to minimize EMI
- Integrated 50 Ω termination resistors provide impedance matching on both Main Link lanes and AUX channel
- High performance Auto Receive Equalization enabling optimal channel compensation, device placement flexibility and power saving at CPU/GPU
- Supports eDP authentication options: Alternate Scrambler Seed Reset (ASSR) and Alternate Framing
- Supports Full Link training
- Supports DisplayPort symbol error rate measurements
- Supports PCB routing flexibility by programming for:
  - ◆ AUX P/N swapping
  - ◆ DP Main Link P/N swapping

## 2.3 LVDS transmitter features

- Compatible with ANSI/TIA/EIA-644-A-2001 standard
- Supports RGB data packing as per JEIDA and VESA data formats
- Supports pixel clock frequency from 6 MHz to 112 MHz
- Supports single LVDS bus operation up to 112 mega pixels per second
- Supports dual LVDS bus operation up to 224 mega pixels per second
- Supports color depth options: 18 bpp, 24 bpp
- Programmable center spreading of pixel clock frequency to minimize EMI
- Supports 1920 × 1200 at 60 Hz resolution in dual LVDS bus mode
- Programmable LVDS signal swing to pre-compensate for channel attenuation or allow for power saving
- Supports PCB routing flexibility by programming for:
  - ◆ LVDS bus swapping
  - ◆ Channel swapping
  - ◆ Differential signal pair swapping
- Supports Data Enable polarity programming
- DDC control for EDID ROM access; I<sup>2</sup>C-bus interface up to 400 kbit/s

## 2.4 Control and system features

- Device programmability
  - ◆ Multi-level configuration pins enabling wider choice

- ◆ I<sup>2</sup>C-bus slave interface supporting Standard-mode (100 kbit/s) and Fast-mode (400 kbit/s)
- Power management
  - ◆ Low-power state: DP AUX command-based Low-power mode (SET POWER)
  - ◆ Deep power-saving state via a dedicated pin

**2.5 General**

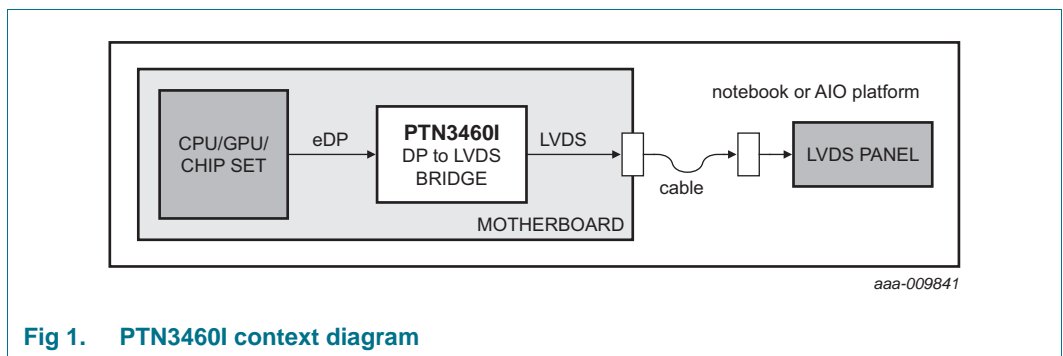
- Power supply: with on-chip regulator
  - ◆ 3.3 V ± 10 % (integrated regulator switched on)
  - ◆ 3.3 V ± 10 %, 1.8 V ± 5 % (integrated regulator switched off)
- ESD: 8 kV HBM, 1 kV CDM
- Operating temperature range: -40 °C to +85 °C
- HVQFN56 package 7 mm × 7 mm, 0.4 mm pitch; exposed center pad for thermal relief and electrical ground

**3. Applications**

- Industrial PC design
- Printer display
- Automotive dashboard display
- AIO platforms
- Notebook platforms
- Netbooks/net tops

**4. System context diagram**

Figure 1 illustrates the PTN3460I usage.



## 5. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PTN3460IBS/Fx <sup>[1][2]</sup>	PTN3460IBS <sup>[3]</sup>	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 7 × 7 × 0.85 mm <sup>[4]</sup> ; 0.4 mm pitch	SOT949-2

- [1] PTN3460IBS/Fx is firmware -specific, where the 'x' indicates the firmware version.
- [2] Notes on firmware and marking:
- Firmware versions are not necessarily backwards compatible.
  - Box/reel labels will indicate the firmware version via the orderable part number (e.g., labeling will indicate PTN3460IBS/F1 for firmware version 1).
- [3] Topside marking is limited to PTN3460IBS and will not indicate the firmware version.
- [4] Maximum package height is 1 mm.

### 5.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN3460IBS/Fx <sup>[1]</sup>	PTN3460IBS/FxMP	HVQFN56	Reel 13" Q2/T3 *standard mark SMD dry pack	2000	T <sub>amb</sub> = -40 °C to +85 °C

- [1] PTN3460IBS/Fx uses specific firmware version ('x' = 1, 2, 3, etc., and changes according to firmware version).

6. Block diagram

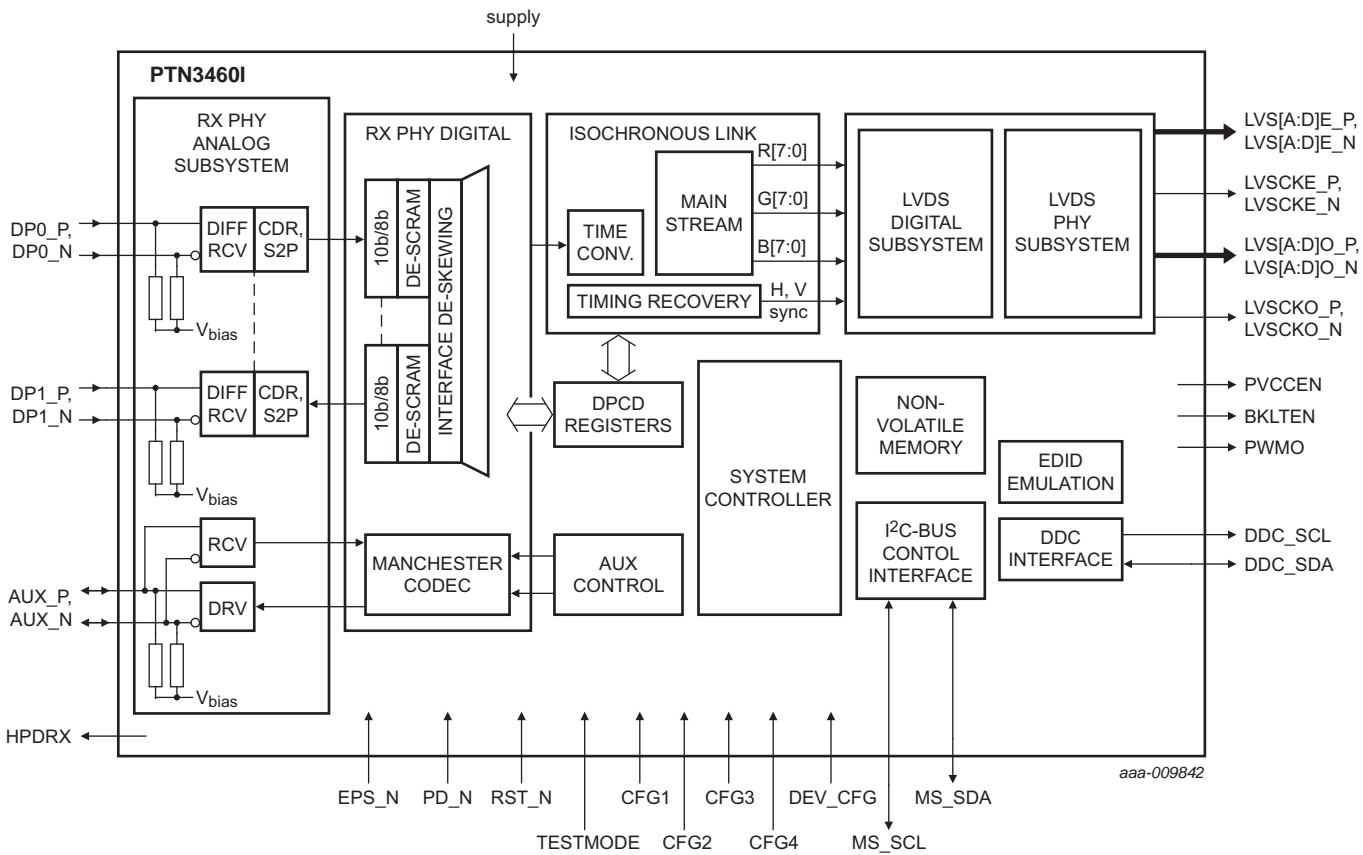


Fig 2. Block diagram of PTN34601

## 7. Pinning information

### 7.1 Pinning



Refer to [Section 13 “Package outline”](#) for package and pin dimensions.

## 7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
<b>DisplayPort interface signals</b>			
DP0_P	4	self-biasing differential input	Differential signal from DP source. DP0_P makes a differential pair with DP0_N. The input to this pin must be AC-coupled externally.
DP0_N	5	self-biasing differential input	Differential signal from DP source. DP0_N makes a differential pair with DP0_P. The input to this pin must be AC-coupled externally.
DP1_P	7	self-biasing differential input	Differential signal from DP source. DP1_P makes a differential pair with DP1_N. The input to this pin must be AC-coupled externally.
DP1_N	8	self-biasing differential input	Differential signal from DP source. DP1_N makes a differential pair with DP1_P. The input to this pin must be AC-coupled externally.
AUX_P	2	self-biasing differential I/O	Differential signal towards DP source. AUX_P makes a differential pair with AUX_N. The pin must be AC-coupled externally.
AUX_N	1	self-biasing differential I/O	Differential signal towards DP source. AUX_N makes a differential pair with AUX_P. The pin must be AC-coupled externally.
HPDRX	11	single-ended 3.3 V CMOS output	Hot Plug Detect signal to DP source.
<b>LVDS interface signals</b>			
LVSAE_P	41	LVDS output	Even bus, Channel A differential signal to LVDS receiver. LVSAE_P makes a differential pair with LVSAE_N.
LVSAE_N	42	LVDS output	Even bus, Channel A differential signal to LVDS receiver. LVSAE_N makes a differential pair with LVSAE_P.
LVSBE_P	39	LVDS output	Even bus, Channel B differential signal to LVDS receiver. LVSBE_P makes a differential pair with LVSBE_N.
LVSBE_N	40	LVDS output	Even bus, Channel B differential signal to LVDS receiver. LVSBE_N makes a differential pair with LVSBE_P.
LVSCE_P	36	LVDS output	Even bus, Channel C differential signal to LVDS receiver. LVSCE_P makes a differential pair with LVSCE_N.
LVSCE_N	37	LVDS output	Even bus, Channel C differential signal to LVDS receiver. LVSCE_N makes a differential pair with LVSCE_P.
LVSCKE_P	34	LVDS clock output	Even bus, clock differential signal to LVDS receiver. LVSCKE_P makes a differential pair with LVSCKE_N.
LVSCKE_N	35	LVDS clock output	Even bus, clock differential signal to LVDS receiver. LVSCKE_N makes a differential pair with LVSCKE_P.
LVSDE_P	31	LVDS output	Even bus, Channel D differential signal to LVDS receiver. LVSDE_P makes a differential pair with LVSDE_N.
LVSDE_N	32	LVDS output	Even bus, Channel D differential signal to LVDS receiver. LVSDE_N makes a differential pair with LVSDE_P.
LVSAO_P	53	LVDS output	Odd bus, Channel A differential signal to LVDS receiver. LVSAO_P makes a differential pair with LVSAO_N.
LVSAO_N	54	LVDS output	Odd bus, Channel A differential signal to LVDS receiver. LVSAO_N makes a differential pair with LVSAO_P.
LVSBO_P	51	LVDS output	Odd bus, Channel B differential signal to LVDS receiver. LVSBO_P makes a differential pair with LVSBO_N.
LVSBO_N	52	LVDS output	Odd bus, Channel B differential signal to LVDS receiver. LVSBO_N makes a differential pair with LVSBO_P.

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
LVSCO_P	48	LVDS output	Odd bus, Channel C differential signal to LVDS receiver. LVSCO_P makes a differential pair with LVSCO_N.
LVSCO_N	49	LVDS output	Odd bus, Channel C differential signal to LVDS receiver. LVSCO_N makes a differential pair with LVSCO_P.
LVSCKO_P	46	LVDS clock output	Odd bus, clock differential signal to LVDS receiver. LVSCKO_P makes a differential pair with LVSCKO_N.
LVSCKO_N	47	LVDS clock output	Odd bus, clock differential signal to LVDS receiver. LVSCKO_N makes a differential pair with LVSCKO_P.
LVSDO_P	43	LVDS output	Odd bus, Channel D differential signal to LVDS receiver. LVSDO_P makes a differential pair with LVSDO_N.
LVSDO_N	44	LVDS output	Odd bus, Channel D differential signal to LVDS receiver. LVSDO_N makes a differential pair with LVSDO_P.
DDC_SDA	30	open-drain DDC data I/O	DDC data signal connection to display panel. Pulled-up by external termination resistor (5 V tolerant).
DDC_SCL	29	open-drain DDC clock I/O	DDC clock signal connection to display panel. Pulled-up by external termination resistor (5 V tolerant).
<b>Panel and backlight interface signals</b>			
PVCCEN	33	CMOS output	Panel power ( $V_{CC}$ ) enable output.
PWMO	28	CMOS output	PWM output signal to display panel.
BKLTEN	26	CMOS output	Backlight enable output.
<b>Control interface signals</b>			
PD_N	10	CMOS input	Chip power-down input (active LOW). If PD_N is LOW, then the device is in Deep power-down completely, even if supply rail is ON; for the device to be able to operate, the PD_N pin must be HIGH.
RST_N	9	CMOS input	Chip reset pin (active LOW); internally pulled-up. The pin is meant to reset the device and all its internal states/logic; all internal registers are taken to default value after RST_N is applied and made HIGH. If RST_N is LOW, the device stays in reset condition and for the device to be able to operate, RST_N must be HIGH.
DEV_CFG	12	CMOS I/O	I <sup>2</sup> C-bus address/mode selection pin.
TESTMODE	20	CMOS input	If TESTMODE is left open or pulled HIGH, CFG[4:1] operate as JTAG pins. If TESTMODE is pulled LOW, these pins serve as configuration pins.
CFG1	21	input	Behavior defined by TESTMODE pin. If TESTMODE is left open or pulled HIGH, this pin functions as JTAG TEST CLOCK input. If TESTMODE is pulled LOW, this pin acts as configuration input.
CFG2	22	input	Behavior defined by TESTMODE pin. If TESTMODE is left open or pulled HIGH, this pin functions as JTAG MODE SELECT input. If TESTMODE is pulled LOW, this pin acts as configuration input.
CFG3	23	input	Behavior defined by TESTMODE pin. If TESTMODE is left open or pulled HIGH, this pin functions as JTAG TEST DATA INPUT. If TESTMODE is pulled LOW, this pin acts as configuration input.
CFG4	27	I/O	Behavior defined by TESTMODE pin value. If TESTMODE is left open or pulled HIGH, this pin functions as JTAG TEST DATA OUTPUT. If TESTMODE is pulled LOW, this pin acts as configuration input.



Table 3. Pin description ...continued

Symbol	Pin	Type	Description
MS_SDA	24	open-drain (I <sup>2</sup> C) data input/output	I <sup>2</sup> C-bus data signal connection to I <sup>2</sup> C-bus master or slave. Pulled up by external resistor.
MS_SCL	25	open-drain (I <sup>2</sup> C) clock input/output	I <sup>2</sup> C-bus clock signal connection to I <sup>2</sup> C-bus master or slave. Pulled up by external resistor.
n.c.	55	-	not connected; reserved.
EPS_N	56	input	Can be left open or pulled HIGH for 3.3 V supply only option relying on internal regulator for 1.8 V generation. Should be pulled down to GND for dual supply (3.3 V/1.8 V) option.
<b>Supply, ground and decoupling</b>			
V <sub>DD(3V3)</sub>	13, 14, 38, 50	power	3.3 V supply input.
V <sub>DD(1V8)</sub>	6, 45	power	1.8 V supply input.
V <sub>DD(1V8)</sub>	19	power	1.8 V regulator supply output.
n.c.	15, 16	power	Not connected.
GND	3	power	Ground.
GNDREG	17, 18	power	Ground for regulator.
GND	center pad	power	The center pad must be connected to motherboard GND plane for both electrical ground and thermal relief.

## 8. Functional description

PTN3460I is an (Embedded) DisplayPort to LVDS bridge IC that processes the incoming DisplayPort (DP) stream, performs DP to LVDS protocol conversion and transmits processed stream in LVDS format. Refer to [Figure 2 “Block diagram of PTN3460I”](#).

The PTN3460I consists of:

- DisplayPort receiver
- LVDS transmitter
- System control and operation

The following sections describe individual sub-systems and their capabilities in more detail.

### 8.1 DisplayPort receiver

PTN3460I implements a DisplayPort receiver consisting of up to 2-lane Main Link and AUX channel.

PTN3460I implements a high-performance Auto Receive Equalizer and Clock Data Recovery (CDR) algorithm, with which it identifies and selects an optimal operational setting for given channel environment. Given that the device is targeted primarily for embedded Display connectivity, both Display Authentication and Copy Protection Method 3a (Alternate Scrambler Seed Reset) and Method 3b (Enhanced Framing) are supported, as per *eDP 1.2*.

The PTN3460I DPCD registers can be accessed by DP source through AUX channel. It supports both Native AUX transactions and I<sup>2</sup>C-over-AUX transactions.

Native AUX transactions are used to access PTN3460I DisplayPort Configuration Data (DPCD) registers (for example, to facilitate Link training, check error conditions) and I<sup>2</sup>C-over-AUX transactions are used to perform any required access to DDC bus (for example, EDID reads).

Given that the HPDRX pin is internally connected to GND through an integrated pull-down resistor (> 100 kΩ), the DP source will see HPDRX pin as LOW indicating that the DisplayPort receiver is not ready when the device is not powered. This helps avoid raising false events to the source. After power-up, PTN3460I continues to drive HPDRX pin LOW until completion of internal initialization. After this, PTN3460I generates HPD signal to notify DP source and take corrective action(s).

**8.1.1 DP Link**

PTN3460I is capable of operating either in DP 2-lane or 1-lane mode.

DP 1-lane or 2-lane mode is selected through configuration pin CFG3. See [Table 4](#) for more details.

**Table 4. CFG3 configuration options**

Configuration input setting	DP lane selection
LOW	2-lane DP configuration
HIGH	1-lane DP configuration

**8.1.2 DPCD registers**

DPCD registers are described in VESA DisplayPort v1.1a/1.2a specifications in detail and PTN3460I supports DPCD version 1.2.

PTN3460I configuration registers can be accessed through DP AUX channel from the GPU/CPU, if required. They are defined under vendor-specific region starting at base address 0x00510h. So any configuration register can be accessed at DPCD address obtained by adding the register offset and base address.

PTN3460I supports down spreading on DP link and this is reflected in DPCD register MAX\_DOWNSPREAD at address 0003h. Further, the DP source could control down spreading and inform PTN3460I via DOWNSPREAD\_CTRL register at DPCD register 00107h.

The key aspect is that the system designer must take care that the Input video payload fits well within both DP link bandwidth and LVDS bandwidth (for a given pixel frequency, SSC depths) when clock spreading is enabled. Also, another aspect for the system designer is to ensure LVDS (panel) TCONs are capable of handling SSC modulated LVDS signaling.

## 8.2 LVDS transmitter

The LVDS interface can operate either in Single or Dual LVDS Bus mode at pixel clock frequencies over the range of 6 MHz to 112 MHz and color depths of 18 bpp or 24 bpp. Each LVDS bus consists of 3/4 differential data pairs and one clock pair. PTN3460I can packetize RGB video data, HSYNC, VSYNC, DE either in VESA or JEIDA format. To enable system EMI reduction, the device can be programmed for center spreading of LVDS channel clock outputs.

The LVDS interface can be flexibly configured using multi-level configuration pins (CFG1, CFG2) or via register interface. The configuration pins and the corresponding definitions are described in [Table 5](#) and [Table 6](#). Nevertheless, as the configuration pins are designed for general purpose, their definitions can be modified and they can be used for any other purposes. However, this can be achieved through firmware upgrade only.

**Table 5. CFG1 configuration options**

Configuration input setting	Number of LVDS links
LOW	single LVDS bus
HIGH	dual LVDS bus

**Table 6. CFG2 configuration options**

3-level configuration input setting	Data format	Number of bits per pixel (bpp)
LOW	VESA	24 bpp
OPEN	JEIDA	24 bpp
HIGH	JEIDA or VESA	18 bpp

The VESA and JEIDA data format definitions are described in [Table 7](#) to [Table 13](#).

**Table 7. LVDS single bus, 18 bpp, VESA or JEIDA data packing**

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2

**Table 8. LVDS single bus, 24 bpp, VESA data packing**

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

**Table 9. LVDS dual bus, 18 bpp, VESA data packing**

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2

**Table 10. LVDS dual bus, 24 bpp, VESA data packing**

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

**Table 11. LVDS single bus, 24 bpp, JEIDA data packing**

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel B	bit 3	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 7	bit 6	bit 5	bit 4
LVDS odd differential channel D	don't care	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0

**Table 12. LVDS dual bus, 18 bpp, JEIDA data packing**

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2

**Table 13. LVDS dual bus, 24 bpp, JEIDA data packing**

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel B	bit 3	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 7	bit 6	bit 5	bit 4
LVDS odd differential channel D	don't care	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0
LVDS even differential channel A	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel B	bit 3	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 7	bit 6	bit 5	bit 4
LVDS even differential channel D	don't care	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0

PTN3460I delivers great flexibility by supporting more programmable options via I<sup>2</sup>C-bus or AUX interface. Please refer to [Section 8.3.11](#) for more details.

### 8.3 System control and operation

With its combination of embedded microcontroller, non-volatile memory, DPCD AUX and I<sup>2</sup>C-bus interfaces, PTN3460I delivers significant value for customer applications by providing higher degree of control and programmability.

By default, all user controllable registers can be accessed through DPCD AUX interface. This interface is always enabled. This AUX interface delivers seamless access of PTN3460I registers to system/platform (GPU) firmware driver. Nevertheless, use of I<sup>2</sup>C-bus interface for configuring PTN3460I is left to the choice of system integrator.

DEV\_CFG (pin 12) sets up I<sup>2</sup>C-bus configuration mode:

- Pull-down resistor to GND — PTN3460I operates as I<sup>2</sup>C-bus slave, low address (0x40h)
- Open — PTN3460I operates as I<sup>2</sup>C-bus slave, high address (0xC0h)
- Pull-up resistor to V<sub>DD(3V3)</sub> — PTN3460I operates as I<sup>2</sup>C-bus master capable of reading from external EEPROM

**Remark:** PTN3460I I2C pins are not failsafe and cannot be connected to the SMBus if the SMBus has active communications during VDD33 supply switch ON. In the application there MUST be no MS\_I2C traffic during supply rise-up.

#### 8.3.1 Reset and power-on initialization

The device has a built-in reset circuitry that generates internal reset signal after power-on. All the internal registers and state machines are initialized and the registers take default values. In addition, PTN3460I has a dedicated control pin RST\_N. This serves the same purpose as power-on reset, but without power cycling of the device/platform.

PTN3460I starts up in a default condition after power-on or after RST\_N is toggled from LOW to HIGH. The configuration pins are sampled at power-on, or external reset, or when returning from Deep Sleep.

PTN3460I has a built-in reset circuitry that generates internal reset signal after power-on. All the internal registers and state machines are synchronously initialized and the registers take default values. Though PTN3460I is designed NOT to need the RST\_N pin, RST\_N is still provided. This serves the same purpose as power-on reset, but without power cycling of the device/platform.

It is good practice to provide for RST\_N control if EPS\_N is LOW (external 1.8 V supply is used). In case RST\_N is used, it must be released after all supplies are within operating conditions.

PTN3460I starts up in a default condition after power-on or after RST\_N is toggled from LOW to HIGH. The configuration pins are sampled at power-on and when there is change of state (for example, from Power saving state to Active state).

Device start-up time from power-on and RST\_N = HIGH is 90 ms max.

**Remark:** Driving RST\_N HIGH is not possible and forbidden during power-up, because the ESD diodes will clamp the signal to the VDDIO+0.6 V. RST\_N pin should be left at Tri-state level during power-up.



Fig 4. Start-up behavior with RST\_N and PD\_N unconnected

### 8.3.2 Power-down for Ultra Power Save

PTN3460I goes into Deep power-saving when both PD\_N and RST\_N are LOW. This will trigger a power-down sequence.

PD\_N and RST\_N can be controlled by GPIO pins of system microcontroller. To leave Deep power-saving state, the system needs to drive PD\_N back to HIGH, then issue a RST\_N pulse for at least 10  $\mu s$ . If PD\_N pin is open, the device will not enter Deep power-saving state. Once the device is in Deep power-saving condition, the HPDRX pin will go LOW automatically and this can be used by the system to remove the 3.3 V supply, if required.

PTN3460I will not respect the Panel power-down sequence if PD\_N is asserted LOW while video is being streamed to the display; the system is not supposed to toggle PD\_N and RST\_N pins asynchronously while the LVDS output is streaming video to the display panel, but instead follow the panel powering sequence as described in [Section 8.3.5](#).

The time between PD\_N going HIGH and HPD raised HIGH by PTN3460I is also 90 ms max.



Fig 5. Start-up behavior with RST\_N and PD\_N sequence when used

### 8.3.3 Use GPIOs to control PD\_N and RST\_N from system side

One example to control PD\_N and RST\_N pulses from system side is shown below:

- Assert PD\_N (make it LOW)
- Assert RST\_N (make it LOW)
- De-assert PD\_N (make it HIGH)
- De-assert RST\_N (make it HIGH)



### 8.3.4 LVDS panel control

PTN3460I implements eDPv1.2 specific DPCD registers that concern panel power, backlight and PWM controls and the DP source can issue AUX commands to initiate panel power-up/down sequence as required. Also, PTN3460I supports LVDS panel control pins — backlight enable, panel power enable and PWM — that can be set via AUX commands.

- **PVCCEN pin** — the signal output is set based on SET\_POWER DPCD register 00600h and SET\_POWER\_CAPABLE bit of EDP\_GENERAL\_CAPABILITY\_REGISTER\_1 DPCD register 00701h and detection and handling of video data stream by PTN3460I
- **BKLTEN pin** — the signal output is set based on BACKLIGHT\_PIN\_ENABLE\_CAPABLE bit of EDP\_GENERAL\_CAPABILITY\_REGISTER\_1 DPCD register 00701h and BACKLIGHT\_ENABLE bit of EDP\_DISPLAY\_CONTROL\_REGISTER DPCD register 00720h
- **PWMO pin** — the PWM signal generated by PTN3460I based on controls set in DPCD registers. In addition, PTN3460I can pass through PWM signal from eDP source as well.

All the panel control enable and signal outputs from PTN3460I are aligned with panel power-on sequence timing including LVDS video output generation. It is important to note that the Panel power must be delivered by the system platform and it should be gated by PVCCEN signal.

8.3.5 Panel power sequencing

Figure 6 illustrates an example of panel power-up/power-down sequence for PTN3460I.

Depending on the source behavior and PTN3460I firmware version, the powering sequence/timing could have some slight differences.



Fig 6. Panel power-up/power-down sequence example

When working with eDP capable DP sources, PTN3460I supports the following (for specific sequence, refer to Figure 6):

- After power-on/startup, HPDRX is asserted HIGH, DP source will start AUX communication for initialization, perform Link Training and starts the video data stream. Once presence of video data is detected, PTN3460I will assert PVCCEN to HIGH, synchronize to video stream, output LVDS data and assert rise the Sink\_status lock as indicated in DPCD register (0x00205h). PTN3460I will wait for Backlight enabling delay (T3) to avoid visual artifacts and program the BKLTEN HIGH.
- While transitioning out of Active state by receiving DPCD 0x600 to set PTN3460I in D3 mode, PTN3460I will disable BKLTEN prior to cutting off Video streaming to avoid visible artifacts following specific panel specifications. PTN3460I will assert PVCCEN to LOW after T5 delay as long as either if the video stream is stopped or video synchronization is lost. This is to avoid driving the LVDS panel with illegal stream for long periods of time. It is good practice for sources to keep video data or at least DP-idle stream active during T4 + T5.
- When PTN3460I is in Low-power state (DisplayPort D3 power state), the LVDS differential I/Os are weakly pulled down to 0 V. In this state, PVCCEN and BKLTEN are pulled LOW.
- When PD\_N is LOW, which sets PTN3460I in Deep power-saving state, the BKLTEN pin is set to LOW. LVDS differential I/Os are pulled LOW via the weak pull-downs.

**8.3.6 Termination resistors**

The device provides integrated and calibrated 50 Ω termination resistors on both DisplayPort Main Link lanes and AUX channel.

**8.3.7 Reference clock input**

PTN3460I does not require an external clock. It relies fully on the clock derived internally from incoming DP stream or on-chip clock generator.

**8.3.8 Power supply**

PTN3460I can be flexibly supplied with either 3.3 V supply only or dual supplies (3.3 V/1.8 V). When supplied with 3.3 V supply only, the integrated regulator is used to generate 1.8 V for internal circuit operation. In this case, the EPS\_N pin must be pulled HIGH or left open. For optimal power consumption, dual supply option (3.3 V and 1.8 V) is recommended.



**Fig 7. Internal regulator start-up**

- EPS\_N pin not connected
- V<sub>DD(1V8)</sub> total decoupling C<sub>decap</sub> < 8 μF total

The 8 μF is 4.7 μF + 100 nF on pin 19 + 100 nF on pin 45 + 2.2 μF + 100 nF on pin 6 + 10 %

**8.3.9 Power-on reset**

Figure 8 shows a possible curve of the regulated VDD(1V8) voltage with dips at t2 to t3 and t4 to t5. The on-chip reset\_n (active LOW) starts active at t0. At t1, the voltage gets higher than the V<sub>trip(H)</sub> level and if this condition is maintained for a period longer than T<sub>high</sub>, a delay element will add another T<sub>porp</sub> before the on-chip reset\_n is de-asserted. If the voltage drops below V<sub>trip(L)</sub> for a period longer than T<sub>low</sub>, the reset\_n is re-asserted. If the supply dip is shorter (eg. t4 to t5) the internal reset is not asserted. This means that voltage drops less than T<sub>low</sub> must be avoided in the system.



Fig 8. Timing diagram of on-chip power-on reset generator

### 8.3.10 Power management

In tune with the system application needs, PTN3460I implements aggressive techniques to support system power management and conservation. The device can exist in one of the three different states as described below:

- **Active state** when the device is fully operational.
- **Low-power state** when DP source issues AUX SET\_POWER command on DPCD register 00600h. In this state, AUX and HPD circuits are operational but the main DP Link and LVDS Bus are put to high-impedance condition. The device will transition back to Active state when the DP source sets the corresponding DPCD register bits to 'DisplayPort D0/Normal Operation mode'. The I<sup>2</sup>C-bus interface will not be operational in this state.
- **Deep power-saving state:** In this state PTN3460I is put to ultra low-power condition. This is effected when PD\_N is LOW. To get back to Active state, PD\_N must be made HIGH. The external interfaces (like I<sup>2</sup>C, AUX, DP, LVDS, configuration pins) will not be operational.

### 8.3.11 Register interface — control and programmability

PTN3460I has a register interface that can be accessed by CPU/GPU or System Controller to choose settings suitably for the System application needs. The registers can be read/written either via DP AUX or I<sup>2</sup>C-bus interface. It is left to system integrator choice to use an interface to configure PTN3460I.

PTN3460I provides greater level of configurability of certain parameters (e.g., LVDS output swing, spreading depth, etc.) via registers beyond what is available through pins. The register settings override the pin values. All registers must be configured during power-on initialization after HPDRX is HIGH. The registers and bit definitions are described in *"I<sup>2</sup>C-bus utility and programming guide for firmware and EDID update"*

**8.3.12 EDID handling**

The DP source issues EDID reads using I<sup>2</sup>C-over-AUX transactions and PTN3460I, in turn, reads from the panel EDID ROM and passes back to the source. To support seamless functioning of panels without EDID ROM, the PTN3460I can be programmed to emulate EDID ROM and delivers internally stored EDID information to the source. Given that EDID is specific to panels, PTN3460I enables system integrator to program EDID information into embedded memory through DP AUX and I<sup>2</sup>C-bus interfaces. The supported EDID ROM emulation size is 896 bytes (seven EDID data structures, each of 128 bytes).

EDID ROM emulation bit is programmed in the configuration table inside the flash memory. It can also be configured through pin setting. FW will read in the pin settings and overwrite the configuration table settings. CFG4 pin is used to turn EDID emulation bit ON/OFF.

**Table 14. CFG4 configuration options**

Configuration input setting	Emulation bit on/off selection
pull-down resistor <sup>[1]</sup> to GND	Emulation ON, EDID is read from internal flash
pull-up resistor <sup>[1]</sup> to V <sub>DD(3V3)</sub>	Emulation OFF, EDID is read from DDC bus

[1] Pull-up/down resistor value in the range of 1 kΩ to 10 kΩ.

**9. Application design-in information**

[Figure 9](#) illustrates PTN3460I usage in a system context. The eDP inputs are connected to DP source port on CPU/GPU and the LVDS outputs are connected to LVDS panel TCON.

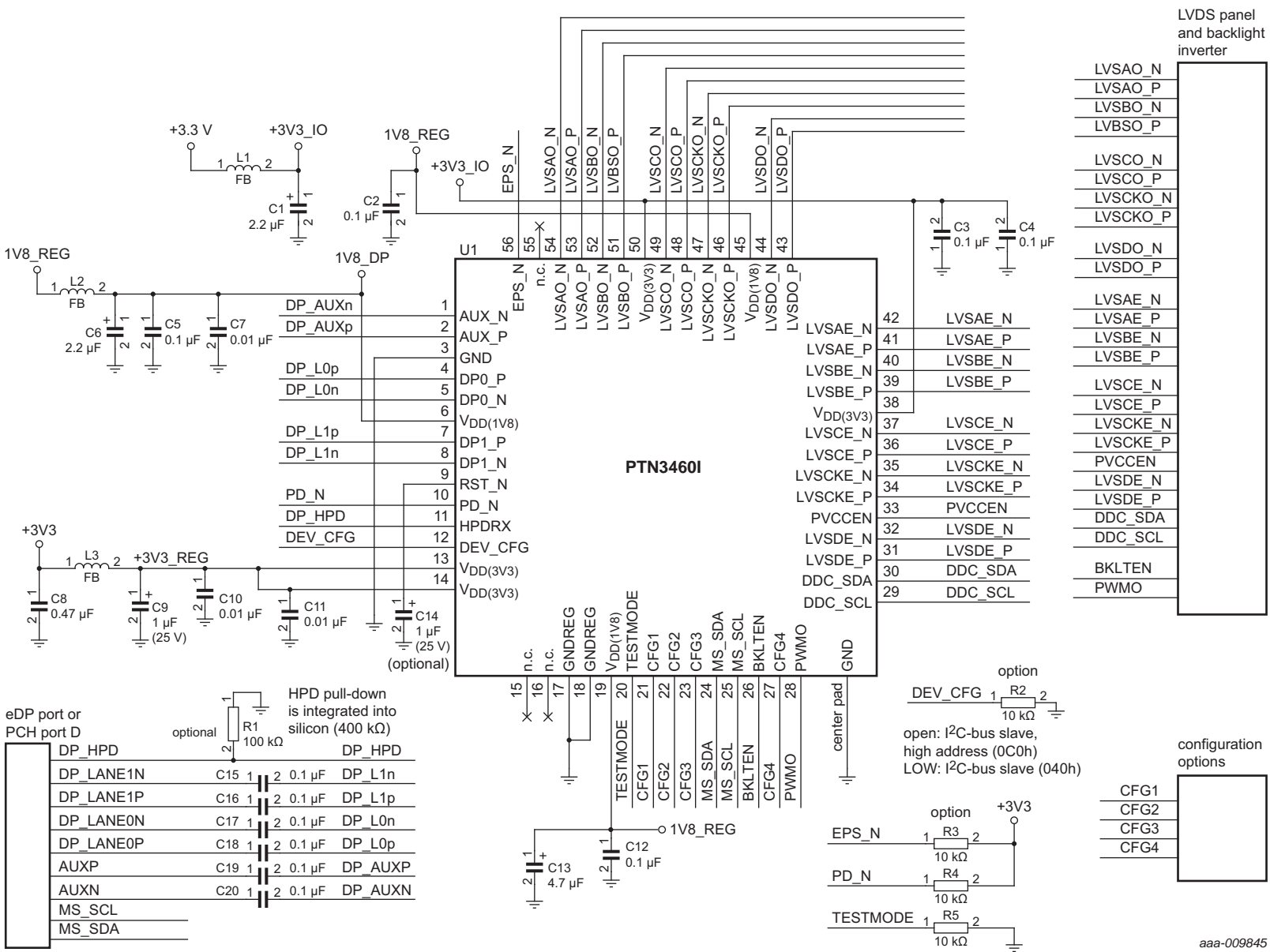


Fig 9. Application diagram

aaa-009845

## 10. Limiting values

**Table 15. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		[1] -0.3	+4.6	V
V <sub>I</sub>	input voltage	3.3 V CMOS inputs	[1] -0.3	V <sub>DD</sub> + 0.5	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[2] -	8000	V
		CDM	[3] -	1000	V

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged-Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged-Device Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.

## 11. Recommended operating conditions

**Table 16. Operating conditions**

*Over operating free-air temperature range, unless otherwise noted.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD(3V3)</sub>	supply voltage (3.3 V)		3.0	3.3	3.6	V
V <sub>DD(1V8)</sub>	supply voltage (1.8 V)		1.7	1.8	1.9	V
V <sub>I</sub>	input voltage	3.3 V CMOS inputs	0	3.3	3.6	V
		open-drain I/O with respect to ground (e.g., DDC_SCL, DDC_SDA, MS_SDA, MS_SCL)	0	5	5.5	V
T <sub>amb</sub>	ambient temperature	operating in free air	-40	-	+85	°C

## 12. Characteristics

### 12.1 Device characteristics

**Table 17. Device characteristics**

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>startup</sub>	start-up time	device start-up time from power-on and RST_N = HIGH; supply voltage within operating range to specified operating characteristics	-	-	90	ms
t <sub>w(rst)</sub>	reset pulse width	device is supplied with valid supply voltage	10	-	-	μs
t <sub>d(rst)</sub>	reset delay time <sup>[1]</sup>	device is supplied with valid supply voltage	-	-	90	ms
t <sub>d(pwrsave-act)</sub>	delay time from power-save to active	time between PD_N going HIGH and HPD raised HIGH by PTN3460I; RST_N is HIGH. Device is supplied with valid supply voltage.	-	-	90	ms

[1] Time for device to be ready after rising edge of RST\_N.

### 12.2 Power consumption

**Table 18. Power consumption**

At operating free-air temperature of 25 °C and under nominal supply value (unless otherwise noted).

Symbol	Parameter	Conditions	Single supply mode EPS_N = HIGH or open			Dual supply mode EPS_N = LOW			Unit	
			Min	Typ	Max	Min	Typ	Max		
P <sub>cons</sub>	power consumption	Active mode; 1440 × 900 at 60 Hz; 24 bits per pixel; dual LVDS bus	[1]	-	430	-	-	290	-	mW
		Active mode; 1600 × 900 at 60 Hz; 24 bits per pixel; dual LVDS bus	[1]	-	448	-	-	305	-	mW
		Active mode; 1920 × 1200 at 60 Hz; 24-bits per pixel; dual LVDS bus	[1]	-	570	-	-	380	-	mW
		D3 mode/Power-saving mode; when PTN3460I is set to Power-saving mode via 'SET_POWER' AUX command by eDP source; AUX and HPDRX circuitry are only kept active		-	27	-	-	15	-	mW
		Deep power-saving/Shutdown mode; when PD_N is LOW and the device is supplied with valid supply voltage		-	5	-	-	2	-	mW

[1] For Active mode power consumption, LVDS output swing of 300 mV is considered.

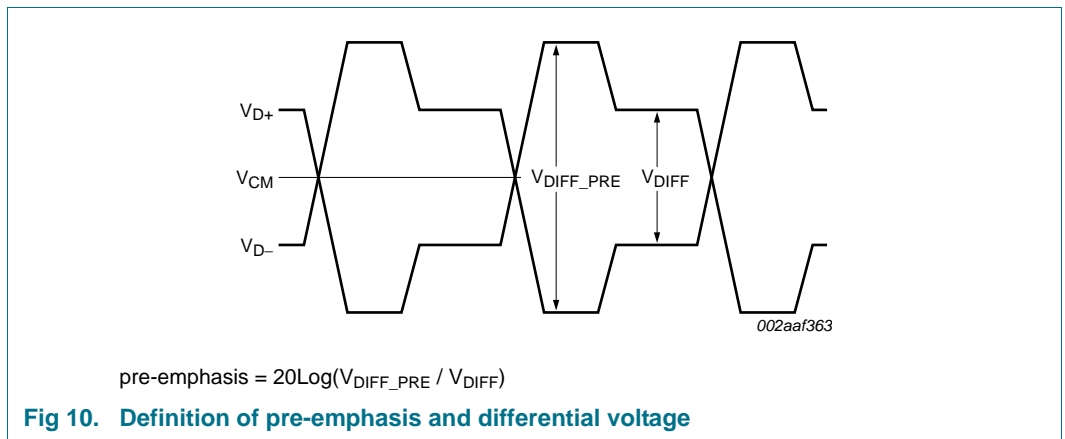


### 12.3 DisplayPort receiver characteristics

**Table 19. DisplayPort receiver main channel characteristics**  
*Over operating free-air temperature range (unless otherwise noted).*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UI	unit interval	high bit rate (2.7 Gbit/s per lane)	[1]	-	370	-	ps
		reduced bit rate (1.62 Gbit/s per lane)	[1]	-	617	-	ps
$\Delta f_{\text{DOWN\_SPREAD}}$	link clock down spreading		[2]	0	-	0.5	%
$C_{\text{RX}}$	AC coupling capacitor			75	-	200	nF
$V_{\text{RX\_DIFFp-p}}$	differential input peak-to-peak voltage	at receiver package pins					
		high bit rate (2.7 Gbit/s per lane)	[3]	120	-	-	mV
		reduced bit rate (1.62 Gbit/s per lane)	[3]	40	-	-	mV
$V_{\text{RX\_DC\_CM}}$	RX DC common mode voltage		[4]	0	-	2.0	V
$I_{\text{RX\_SHORT}}$	RX short-circuit current limit		[5]	-	-	50	mA
$f_{\text{RX\_TRACKING\_BW}}$	jitter tracking bandwidth		[6]	20	-	-	MHz
$G_{\text{eq(max)}}$	maximum equalization gain	at 1.35 GHz		-	15	-	dB

- [1] Range is nominal  $\pm 350$  ppm. DisplayPort channel RX does not require local crystal for channel clock generation.
- [2] Up to 0.5 % down spreading is supported. Modulation frequency range of 30 kHz to 33 kHz is supported.
- [3] Informative; refer to [Figure 10](#) for definition of differential voltage.
- [4] Common-mode voltage is equal to  $V_{\text{bias\_RX}}$  voltage.
- [5] Total drive current of the input bias circuit when it is shorted to its ground.
- [6] Minimum CDR tracking bandwidth at the receiver when the input is repetition of D10.2 symbols without scrambling.



## 12.4 DisplayPort AUX characteristics

Table 20. DisplayPort AUX characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UI	unit interval		[1]	0.4	0.5	0.6	μs
t <sub>jit(cc)</sub>	cycle-to-cycle jitter time	transmitting device	[2]	-	-	0.04	UI
		receiving device	[3]	-	-	0.05	UI
V <sub>AUX_DIFFp-p</sub>	AUX differential peak-to-peak voltage	transmitting device	[4]	0.39	-	1.38	V
		receiving device	[4]	0.32	-	1.36	V
R <sub>AUX_TERM(DC)</sub>	AUX CH termination DC resistance	informative		-	100	-	Ω
V <sub>AUX_DC_CM</sub>	AUX DC common-mode voltage		[5]	0	-	2.0	V
V <sub>AUX_TURN_CM</sub>	AUX turnaround common-mode voltage		[6]	-	-	0.3	V
I <sub>AUX_SHORT</sub>	AUX short-circuit current limit		[7]	-	-	90	mA
C <sub>AUX</sub>	AUX AC coupling capacitor		[8]	75	-	200	nF

- [1] Results in the bit rate of 1 Mbit/s including the overhead of Manchester II coding.
- [2] Maximum allowable UI variation within a single transaction at connector pins of a transmitting device. Equal to 24 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.
- [3] Maximum allowable UI variation within a single transaction at connector pins of a receiving device. Equal to 30 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.
- [4]  $V_{AUX\_DIFFp-p} = 2 \times |V_{AUX\_P} - V_{AUX\_N}|$ .
- [5] Common-mode voltage is equal to V<sub>bias\_TX</sub> (or V<sub>bias\_RX</sub>) voltage.
- [6] Steady-state common-mode voltage shift between transmit and receive modes of operation.
- [7] Total drive current of the transmitter when it is shorted to its ground.
- [8] The AUX channel AC-coupling capacitor placed both on the DisplayPort source and sink devices.

## 12.5 LVDS interface characteristics

Table 21. LVDS interface characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	$R_L = 100 \Omega$ ; CFG4 pin is open and LVDS interface control 2 register in default value	250	300	350	mV
$\Delta V_{o(dif)}$	differential output voltage variation	$R_L = 100 \Omega$ ; change in differential output voltage between complementary output states	-	-	50	mV
$V_{cm}$	common-mode voltage	$R_L = 100 \Omega$	1.125	1.2	1.375	V
$I_{OS}$	output short-circuit current	$R_L = 100 \Omega$	-	-	24	mA
$I_{OZ}$	OFF-state output current	output 3-state circuit current; $R_L = 100 \Omega$ ; LVDS outputs are 3-stated; receiver biasing at 1.2 V	-	-	20	$\mu$ A
$t_r$	rise time	$R_L = 100 \Omega$ ; from 20 % to 80 %	-	-	390	ps
$t_f$	fall time	$R_L = 100 \Omega$ ; from 80 % to 20 %	-	-	390	ps
$t_{sk}$	skew time	intra-pair skew between differential pairs	-	-	50	ps
		inter-pair skew between 2 adjacent LVDS channels	-	-	200	ps
m	modulation index	for center spreading				
		minimum modulation depth	-	0	-	%
		maximum modulation depth	-	2.5	-	%
$f_{mod}$	modulation frequency	center spreading	30	-	100	kHz

## 12.6 Control inputs and outputs

Table 22. Control input and output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Signal output pins — PVCCEN, BKLTEN, HPDRX, PWMO</b>						
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -2 \text{ mA}$	2.4	-	-	V
$V_{OL}$	LOW-level output voltage	$I_{OL} = 2 \text{ mA}$	-	-	0.4	V
<b>Control input pins — PD_N, TESTMODE, DEV_CFG, CFG[4:1]</b>						
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD(3V3)}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD(3V3)}$	V
<b>Control input pin — EPS_N</b>						
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD(3V3)}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.2V_{DD(3V3)}$	V
<b>DDC_SDA, DDC_SCL, MS_SDA, MS_SCL<sup>[1]</sup></b>						
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD(3V3)}$	-	5.25	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD(3V3)}$	V
$I_{OL}$	LOW-level output current	static output; $V_{OL} = 0.4 \text{ V}$	3.0	-	-	mA

[1] For DDC\_SCL, DDC\_SDA, MS\_SCL, MS\_SDA characteristics, please refer to UM10204, "I<sup>2</sup>C-bus specification and user manual" (Ref. 6).

## 12.7 RST\_N

**Table 23. RST\_N characteristics**

Over operating free-air temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input characteristics</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.7 × V <sub>DD(3V3)</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3 × V <sub>DD(3V3)</sub>	V
I <sub>pu(RST_N)</sub>	pull-up current on pin RST_N	V <sub>I</sub> = 0 V	25	55	90	μA

## 12.8 On-chip power-on reset

**Table 24. On-chip power-on reset characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
T <sub>high</sub>	time V <sub>DD(1V8)</sub> has to be above V <sub>trip(H)</sub> before reset_n will be '1'	-	-	2	μs
T <sub>low</sub>	time V <sub>DD(1V8)</sub> has to be below V <sub>trip(L)</sub> before reset_n will be '0'	-	-	11	μs
T <sub>porp</sub>	minimal time reset_n will be '1' after V <sub>DD(1V8)</sub> > V <sub>trip(H)</sub>	0.2	0.32	0.5	μs
V <sub>trip(H)</sub>	HIGH trip level	1.0	1.2	1.6	V
V <sub>trip(L)</sub>	LOW trip level	0.95	1.1	1.4	V
T <sub>d(rstn_i2chz)</sub>	delay time for I2C pins (SCL or SDA) to get into Hi impedance state from the rising edge of RST_N or internal reset_n	-	-	20 <sup>[1]</sup>	μs
T <sub>startup</sub>	time delay from RST_N or internal reset_n signal and rising edge of HPD	-	-	90 <sup>[2]</sup>	ms
T <sub>pwrsave</sub>	time delay from falling edge of PD_N and actual HPD falling edge while entering power saving mode	-	-	90 <sup>[3]</sup>	μs
T <sub>w(rst)</sub>	minimum requirement for external RST_N reset pulse width	10	-	-	μs
T <sub>startup(vdd1v8)</sub>	internal 1.8 V regulator delay from V <sub>DD(3V3)</sub> within specification to V <sub>DD(1V8)</sub> within specification	-	-	30 <sup>[4]</sup>	μs

- [1] This is based on simulations. In all cases seen in measurement this delay is actually much shorter.
- [2] This is a firmware deadline and the typical value can change with a FW update. The max timing has to be respected and checked at any FW update.
- [3] This delay is also defined by firmware. The FW polls for DP\_N pin state at periods close to 50 ms and this makes the response fluctuate.
- [4] Based on worst-case measurements starting the regulator after V<sub>DD(3V3)</sub> is 3.0 V. In practical case the regulator starts at much lower supply level and this value can be considered 0 if input supply has rise time > 1 ms.

### 13. Package outline

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads;  
56 terminals; body 7 x 7 x 0.85 mm

SOT949-2



Fig 11. Package outline SOT949-2 (HVQFN56)

## 14. Packing information

### 14.1 SOT949-2 (HVQFN56); Reel dry pack, SMD, 13"; Q2/T3 turned product orientation; Orderable part number ending ,528 or MP; Ordering code (12NC) ending 528

#### 14.1.1 Packing method

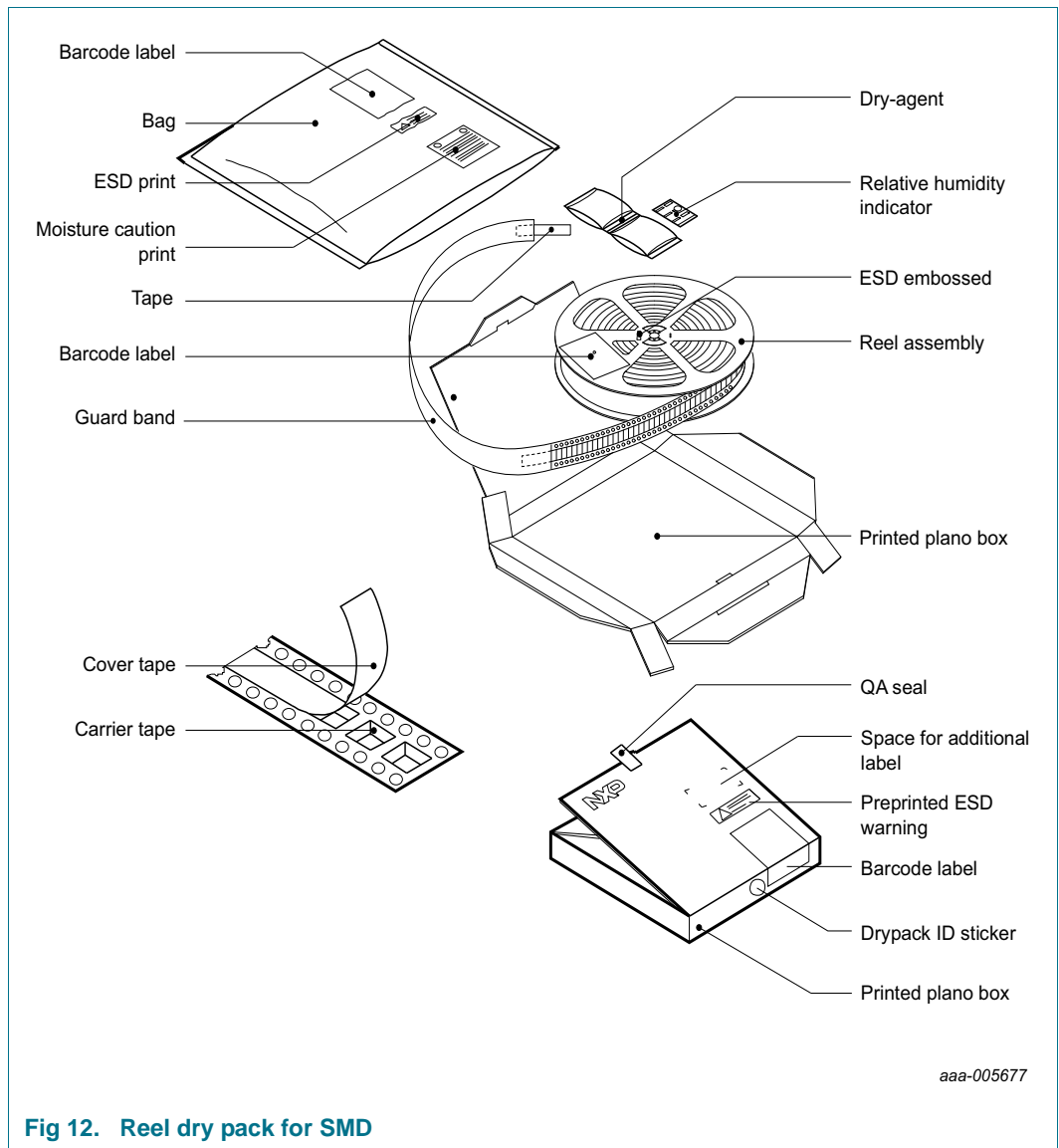


Fig 12. Reel dry pack for SMD

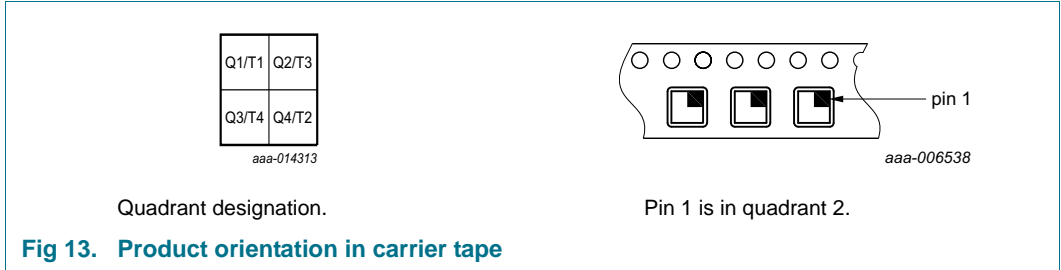
Table 25. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
330 × 16	4000	1	339 × 335 × 43
	2000		

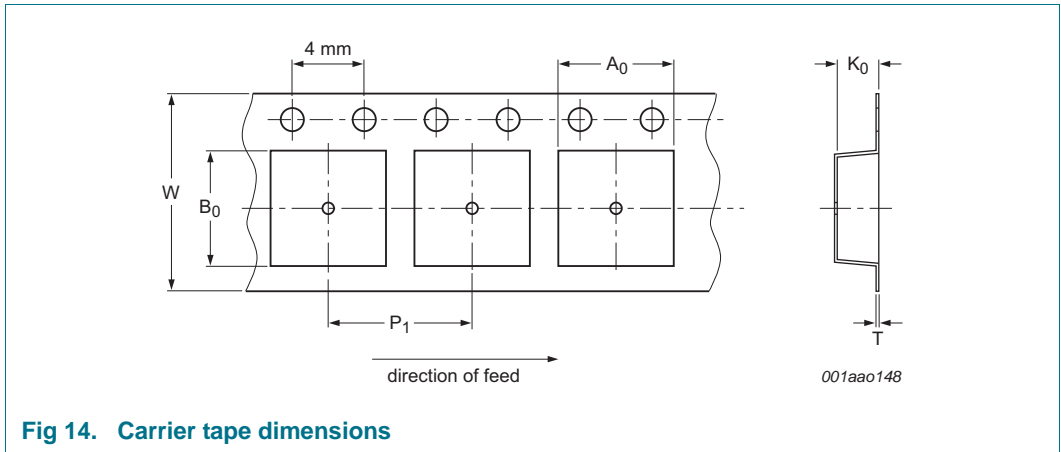
[1] d = reel diameter; w = tape width.

- [2] Packing quantity dependent on specific product type.  
View ordering and availability details at [NXP order portal](#), or contact your local NXP representative.

14.1.2 Product orientation



14.1.3 Carrier tape dimensions



**Table 26. Carrier tape dimensions**  
In accordance with IEC 60286-3.

A <sub>0</sub> (mm)	B <sub>0</sub> (mm)	K <sub>0</sub> (mm)	T (mm)	P <sub>1</sub> (mm)	W (mm)
7.3 ± 0.1	7.3 ± 0.1	1.10 ± 0.1	0.30 ± 0.05	12 ± 0.1	16 ± 0.3

14.1.4 Reel dimensions

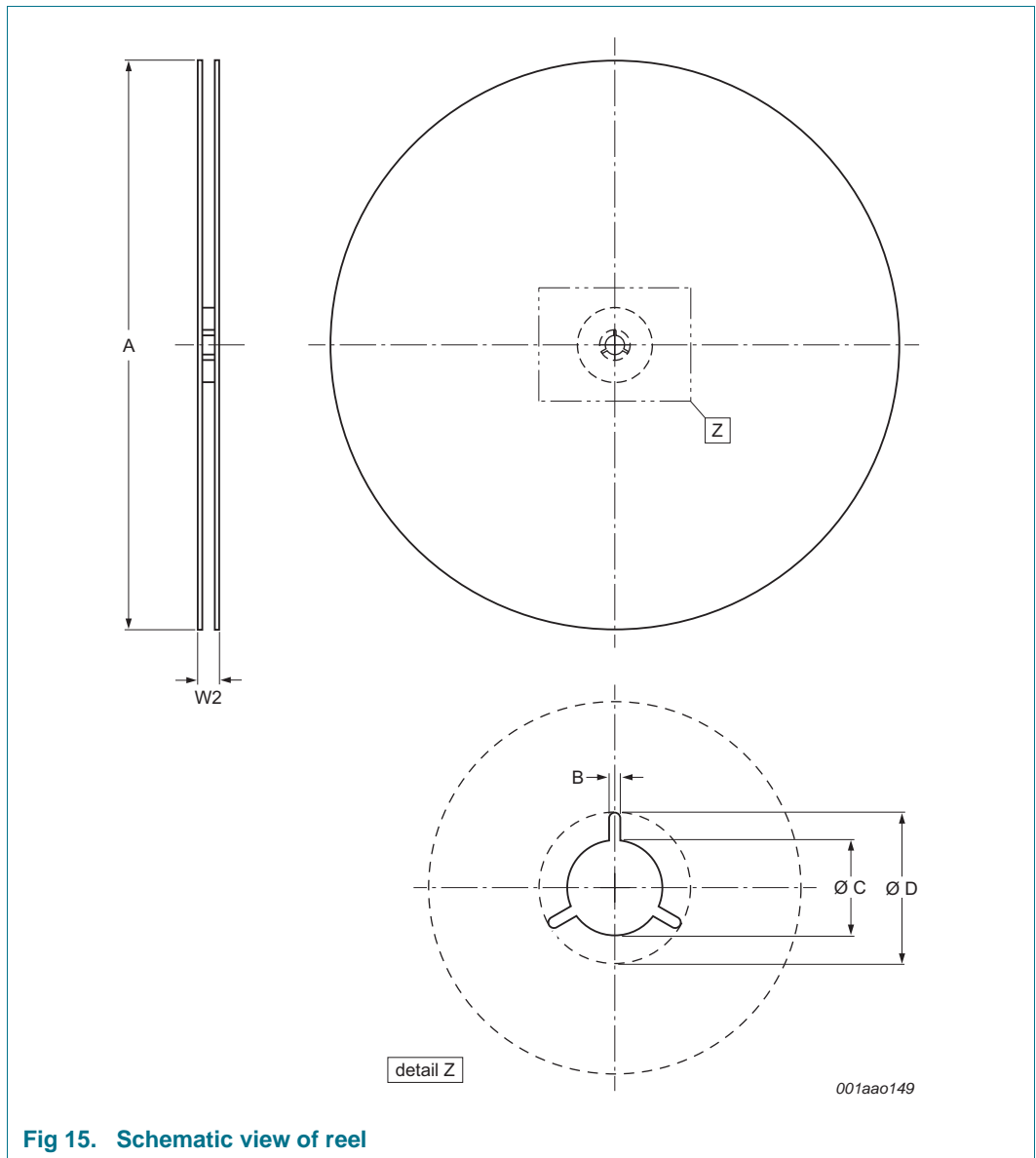


Fig 15. Schematic view of reel

Table 27. Reel dimensions  
In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
330	22.4	1.5	12.8	20.2



14.1.5 Barcode label

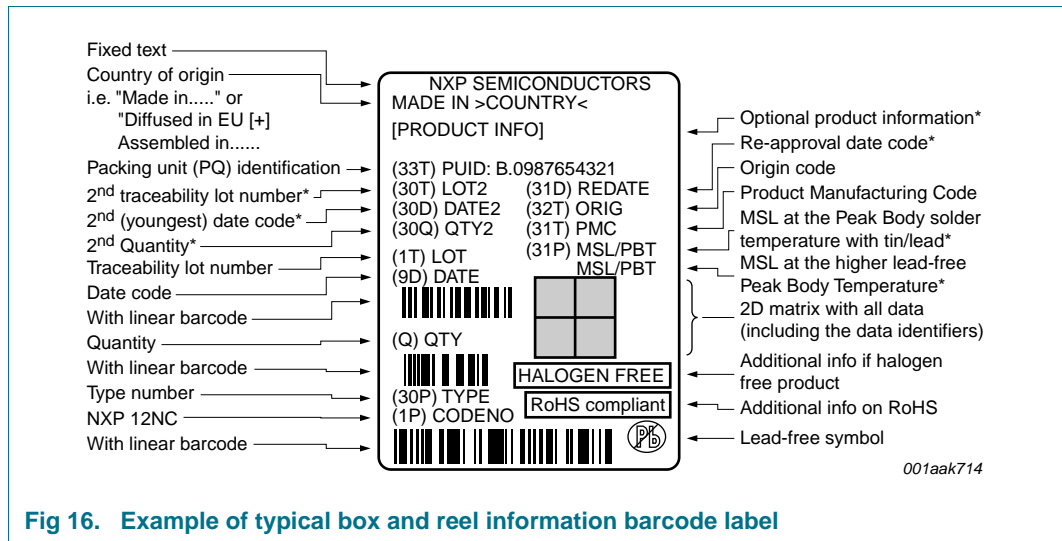


Fig 16. Example of typical box and reel information barcode label

Table 28. Barcode label dimensions

Box barcode label l × w (mm)	Reel barcode label l × w (mm)
100 × 75	100 × 75

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 17](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 29](#) and [30](#)

**Table 29. SnPb eutectic process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 30. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 17](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

### 16. Soldering: PCB footprint

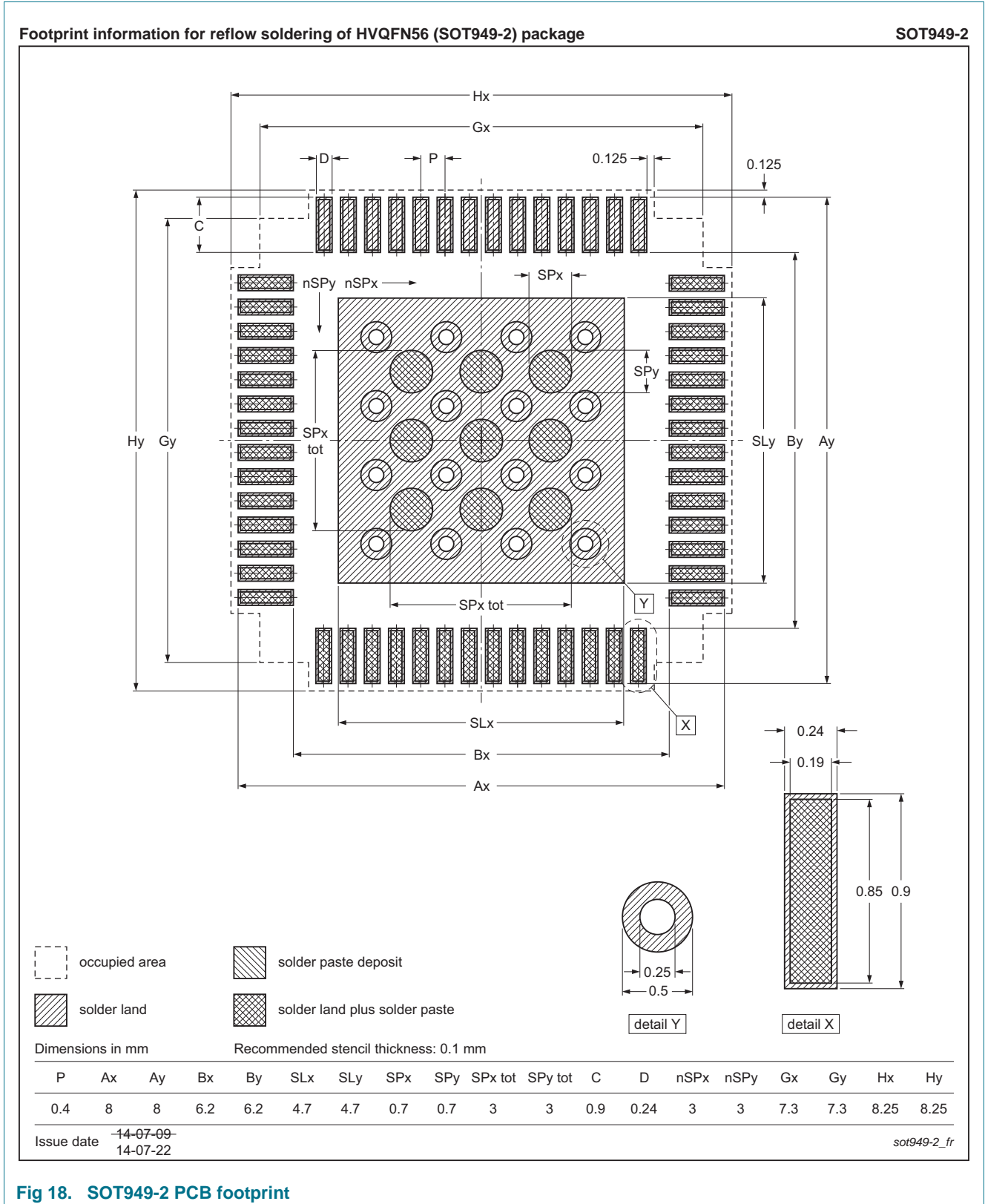


Fig 18. SOT949-2 PCB footprint

## 17. Abbreviations

Table 31. Abbreviations

Acronym	Description
AIO	All In One
AUX	Auxiliary channel
BIOS	Basic Input/Output System
bpp	bits per pixel
CDM	Charged-Device Model
CDR	Clock Data Recovery
CPU	Central Processing Unit
DDC	Data Display Channel
DP	DisplayPort
DPCD	DisplayPort Configuration Data
EDID	Extended Display Identification Data
eDP	embedded DisplayPort
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
GPU	Graphics Processor Unit
HBM	Human Body Model
HBR	High Bit Rate (2.7 Gbit/s) of DisplayPort specification
HPD	Hot Plug Detect signal of DisplayPort or LVDS interface
I/O	Input/Output
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
LVDS	Low-Voltage Differential Signaling
NVM	Non-Volatile Memory
PCB	Printed-Circuit Board
POR	Power-On Reset
PWM	Pulse Width Modulation (or Modulator)
RBR	Reduced Bit Rate (1.62 Gbit/s) of DisplayPort specification
RGB	Red/Green/Blue
ROM	Read-Only Memory
Rx	Receive
SSC	Spread Spectrum Clock
TCON	Timing CONTroller
Tx	Transmit
UI	Unit Interval
VESA	Video Electronics Standards Association

## 18. References

- [1] **VESA DisplayPort standard** — version 1, revision 1a; January 11, 2008
- [2] **VESA DisplayPort standard** — version 1, revision 2a; March 2012
- [3] **VESA embedded DisplayPort standard** — version 1.2; May 5, 2010
- [4] **VESA embedded DisplayPort standard** — version 1.1, October 23, 2009
- [5] **ANSI/TIA/EIA-644-A-2001, Electrical characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits** — approved: January 30, 2001
- [6] **UM10204, I<sup>2</sup>C-bus specification and user manual** — NXP Semiconductors

## 19. Revision history

Table 32. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN3460I v.2.1	20160816	Product data sheet	-	PTN3460IBS v.2
Modifications:	<ul style="list-style-type: none"> <li>• Removed 500 piece MOQ</li> <li>• Added <a href="#">Section 14 “Packing information”</a></li> </ul>			
PTN3460I v.2	20141219	Product data sheet	-	PTN3460IBS v.1
Modifications:	<ul style="list-style-type: none"> <li>• Changed document name from “PTN3460IBS” to “PTN3460I”.</li> <li>• <a href="#">Table 24 “On-chip power-on reset characteristics”</a>: Updated typ and max values for <math>T_{porp}</math>.</li> <li>• Updated <a href="#">Figure 4 “Start-up behavior with RST_N and PD_N unconnected”</a> and <a href="#">Figure 5 “Start-up behavior with RST_N and PD_N sequence when used”</a></li> </ul>			
PTN3460IBS v.1	20140910	Product data sheet	-	-

## 20. Legal information

### 20.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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