Automotive Sensor Signal Conditioner for Thermocouples with SENT Output

ZSSC4175D-01
Datasheet

Description

The ZSSC4175D-01 is a member of IDT's family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of two signals from thermocouple elements.

Digital compensation of offset, sensitivity, temperature drift, and nonlinearity is accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the ZSSC4175D-01 nonvolatile memory (NVM), which is reliable in automotive applications.

Measured values are provided via a digital SENT interface. The SENT interface enables transmission of conditioned thermocouple data via its Fast Channel as well as transmission of supplementary data via its Serial Data Message (SDM) Channel (also referred to as the "slow" channel) using only one output pin. End-of-line calibration is also supported through this output pin via a One-Wire Interface (OWI). The ZSSC4175D-01 and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4175D-01 is optimized for automotive environments by over-voltage and reverse-polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Exhaust Systems

Available Support

- Evaluation Kit
- Application Notes
- Calculation Tools

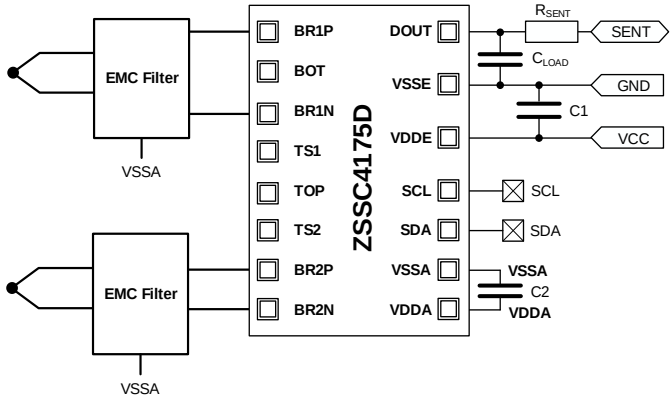
Features

- Two differential thermocouple element inputs and an on-chip temperature sensor, available for cold-junction compensation and temperature output
- Operating temperature range: -40°C to 150°C
- Accuracy: up to 5K at 1000°C hot junction
- Supports N-type thermocouples
- NVM memory for configuration, calibration data, and configurable measurement and conditioning functionality
- SENT output compliant to SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4) standard (refer to section 7.6 for details)
- Supports output of one or more thermocouple signals and product identification via a single SENT interface connection
- End-of-line calibration process minimizes production costs
- No external trimming or components required
- Qualified according to AEC-Q100 Grade 0
- Enhanced diagnostic features for sensor module

Physical Characteristics

- Supply voltage: 4.5V to 5.5V
- Over-voltage and reverse-polarity protection up to ±18V
- Input span: -5mV to 80mV thermocouple voltage range
- ADC resolution: 14-bit
- Output resolution: 12-bit via SENT interface
- Package: 24-QFN (4 × 4 mm; wettable flanks)

ZSSC4175D-01 Basic Circuit



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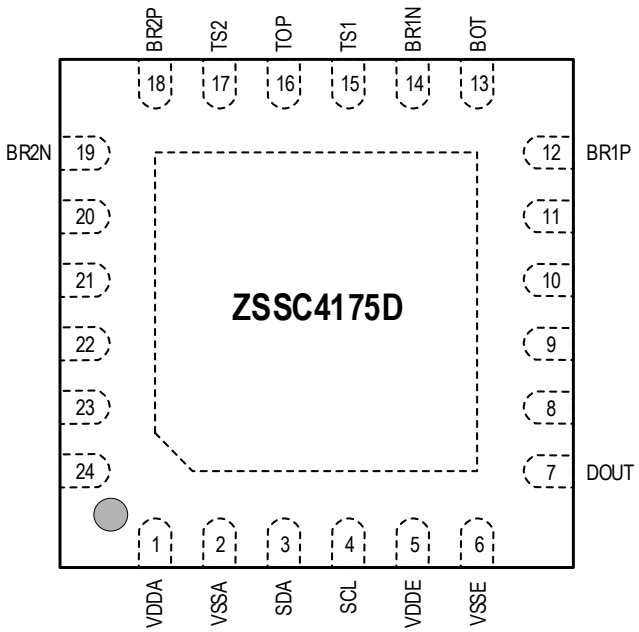
1. Pin Assignments

The ZSSC4175D-01 is available in a 24-QFN (4 × 4 mm; wettable flanks) RoHS-conformant package.

Note: The backside of the 24-QFN package (exposed pad; see section 13) is electrically connected to VSSA.

Recommendation: On the printed circuit board (PCB), the land pattern of the exposed pad should be shorted to the solder pad of the VSSA pin. The exposed pad of the 24-QFN package should be soldered to reduce thermal resistance.

Figure 1. Pin Assignments for 4 × 4 mm 24-QFN Package – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

24-QFN Pin	Pin Name	Type	Description
1	VDDA	Supply	Internal supply
2	VSSA	Supply	Internal ground
3	SDA [a], [b]	I/O	I2C data input/output with internal pull-up (optional for production purposes only)
4	SCL [a], [b]	Input	I2C clock, with internal pull-up (optional for production purposes only)
5	VDDE	Supply	External supply
6	VSSE	Supply	External ground
7	DOUT	I/O	SENT output and One-Wire Interface (OWI) input/output
8 to 11	n.c.	–	No connection – unused
12	BR1P	Input	Positive thermocouple input
13	BOT	Supply	High ohmic – unused
14	BR1N	Input	Negative thermocouple input
15	TS1	Input	High ohmic – unused

24-QFN Pin	Pin Name	Type	Description
16	TOP	Supply	High ohmic – unused
17	TS2	Input	High ohmic – unused
18	BR2P	Input	Positive thermocouple input 2
19	BR2N	Input	Negative thermocouple input 2
20 to 24	n.c.	–	No connection – unused
25	EPAD [c]	Supply	Exposed pad – internally connected to VSSA

[a] Internal pull-up.

[b] No connection required.

[c] Ground – should be shorted externally to VSSA (pin 2).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZSSC4175D-01 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 4 might affect device reliability.

See section 7.8 for information about over-voltage protection, reverse-polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

No.	Symbol	Parameter	Conditions	Min	Max	Unit
DS_001	V_{DDE_ABS}	Supply voltage		-18	18	V
DS_002	V_{DOUT_ABS}	Voltage at the DOUT pin		-18	18	V
DS_003	V_{PIN_ABS}	Pin voltage difference	Voltage between any two of these pins: VDDE, OUT and VSSE	-18	18	V
DS_004	V_{DDA_ABS}	Analog supply voltage	On-chip controlled voltage; do not supply externally	-0.3	6	V
DS_006	V_{PIN_ABS}	Voltage at all other pins	Maximum voltage is V_{DDA} + 0.3V	-0.3	6	V
DS_007	T_{J_ABS}	Junction temperature	Note: See section 7.8 regarding over-voltage protection	-40	160 [a]	°C
DS_008	T_{STOR_ABS}	Storage temperature		-55	155	°C

[a] Required for DS_016 and DS_012.

4. Operating Conditions

The operating conditions below specify the conditions that the application circuit must provide to the device during operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in sections 5.

Table 3. Recommended Operating Conditions

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DP_001	V_{DDE}	Supply voltage	VDDE to VSSE	4.5	5	5.5	V
DS_011	V_{DDE_OP}[a]	Extended operation supply voltage [a]	VDDE to VSSE; derated accuracy and derated SENT pulse shaping outside of normal supply range V_{DDE} Note for a supply greater than 5.5V: Above the ZSSC4175D-01 over-voltage limitation threshold, the output potential is clipped at this threshold	4		6	V
DS_012	T_{AMB} [b], [c]	Ambient temperature [b]	Temperature range	-40		150	°C
Informal [d]	$R_{th\_JA\_QFN24}$ [a]	Thermal resistance 24-QFN	According to JESD 51		32		K/W

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Temperature stress over lifetime is restricted to the Temperature Profile described in section 12 or to similar stress caused by equivalent temperature profiles. Contact IDT for a calculation sheet *Temperature Profile Calculation Sheet* for temperature stress calculation. See the last page for contact information.

[c] Assuming application conditions according to Test Board Design as per JESD51-7 and natural convection Test Conditions as per JESD51-2.

[d] Package-related parameter.

5. Electrical Characteristics

All parameter values are valid under the operating conditions specified in section 4 (unless otherwise stated). All parameters are valid for the ambient temperature range T_{AMB} and for the supply voltage range V_{DDE} = 4.5 to 5.5 V. Unless otherwise defined, the parameters are related to the ZSSC4175D-01 itself. All voltages are referenced to VSSA pin.

Table 4. Electrical Parameters

Note: See important table notes at the end of this table.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.1 Supply Current and System Operating Conditions							
DP_002	I_S	Supply current	Excluding output current at DOUT pin; oscillator adjusted to f_{OSC} = 8MHz.		8	11	mA
DS_016	P_{OV}	Over-voltage power consumption[a]	5.5V < V_{DDE} < 18V; excluding output load.			300	mW
DS_018	$V_{OV\_OFF\_TH}$ [a]	Over-voltage switch-off threshold	The ZSSC4175D-01 is set to the reset state with limited current consumption if V_{DDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.	7		12	V
DS_019	$t_{OV\_OFF\_DLY}$ [a]	Over-voltage switch-off delay	The ZSSC4175D-01 is set to the reset state with limited current consumption if V_{DDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.		10	25	ms
DS_020	$I_{S\_OV\_OFF}$ [a]	Supply current limitation in the event of over-voltage switch-off	Over-voltage switch-off is activated if the supply voltage exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$. V_{DDE} < 18V; excluding thermocouple and output load.			10	mA
DS_184	V_{DDA}	Analog supply voltage		0.95		1.0	V_{DDE}
DP_002	V_{SENS}	Thermocouple supply voltage	V_{SENS} is the common mode voltage of thermocouple generated by AFE.		0.5		V_{DDA}
DS_022	V_{POR_OFF}	Power-on reset off-threshold	V_{DDA} measured referenced to VSSA; POR is active until V_{DDA} exceeds this threshold.	3.3		3.8	V
DS_023	V_{POR_ON}	Power-on reset on-threshold	V_{DDA} measured referenced to VSSA; POR is activated if V_{DDA} falls below this threshold.	3.0		3.6	V
DS_024	V_{POR_HYST}[a]	Power-on reset hysteresis	V_{POR_ON} – V_{POR_OFF}		0.4		V
DS_025	f_{OSC}	Oscillator frequency	Calibrated oscillator frequency.	7.6	8	8.6	MHz

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.2 Analog Front-End Characteristics							
DP_003	V_{IN_SPAN}	Differential input span		-5		60	mV
Informal		Bandgap voltage			1.129		V
5.3 Internal Temperature Measurement							
DP_004	F_{ALL_PTAT}	Internal temperature PTAT accuracy	Calibration performed with PTAT raw data delivered by IDT in NVM.			2.0	K
5.4 Thermocouple Measurement							
DP_044	TC_{RNG} [a]	Thermocouple temperature range	For N-type thermocouple.	-45		1250	°C
DP_007	R_{TC_RNG} [a]	Thermocouple resistance measurement range		1		18	Ω
DP_009	R_{isoL_RNG} [a]	Thermocouple leakage measurement range	Thermocouple isolation resistance to VSSA.	20		10000	kΩ
DP_047	R_{isoH_RNG} [a]	Thermocouple leakage measurement range	Thermocouple isolation resistance to VDDA.	50		10000	kΩ
DP_016	F_{abs}	Thermocouple measurement accuracy	N-type thermocouple with standard characteristic.[d]			±0.3 %±2.0	K
5.5 SENT Output Refer to *SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4)* for detailed specifications for the SENT Physical and Software Layer.							
DS_048	t_{TICK}	Tick time	Adjustment step = 1µs for tick times ≥ 3µs.	2.4		90	µs
DS_049	t_{TICK_JITTER}[a], [c]	Tick time jitter	Valid for tick time ≤ 10µs, 6-sigma value.			300	ns
DS_050	n_{SDM}	Number of SDMs	Absolute count of different messages.	0		32	
Informal	n_{SDM_CYC}	Number of SDM in SDM cycle	Message count in SDM cycle, including repeated SDMs.	0		64	
DS_052	n_{SDM_PRIO}	SDM transmission priority levels		1		3	
DS_053	t_{PAUSE}	Pause length	Fixed frame length.	12		768	t_{TICK}
DS_054	t_{FRAME}	Frame length	Pause pulse disabled, 6 data nibble, and variable frame length.	154		270	t_{TICK}
			Pause pulse enabled, 6 data nibble, and fixed frame length.	282		922	t_{TICK}

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.6 System Response							
DP_010	$t_{STARTUP}$[a]	Startup time	Time to first valid output after power-on; V_{DDE} slew rate > 0.1V/µs.	5		20	ms
DP_011	OUR [a]	Output update rate	ZSSC4175D-01 internal output update, asynchronous to SENT transmission.		2	3	ms
DP_012	ORT [a]	Output response time	100% input step, t_{TICK} = 3µs, SENT pause = on, minimum.	2		10	ms
DP_013	DTI [a]	Diagnostic testing interval			16	20	ms
DP_014	FRT [a]	Failure reaction time	Time between failure detection and reaction inside the IC.			25	ms
DP_015	FMT [a]	Failure messaging time	Time between occurrence of an failure event and reporting on SENT output (with one failure confirmation and 3µs tick time).	15		70	ms

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] The temperature sensor range is the calibration target for the SENT output of the SDM temperature channels. This target can be adjusted.

[c] Compliant to SENT – SAEJ2716 APR2016 (Rev. 4). Sent – SAEJ2716 JAN2010 (Rev. 3) specifies maximum jitter of 50ns at tick time = 3µs and maximum jitter of 250ns at tick time = 10µs without any sigma limitation.

[d] Refer National Institute of Standards and Technology (NIST) for calibration table for n-type thermocouples as an example.

[e] R_{ISO} is measured indirectly by current and has a limited SENT output update rate.

6. Interface Characteristics and Nonvolatile Memory

Table 5. Interface Characteristics and Nonvolatile Memory

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
6.1 I2C Interface – Only for production purposes							
DS_171	V_{I2C_HIGH} [a]	I2C input voltage level HIGH	Master to slave	3.0			V
DS_172	V_{I2C_LOW}[a]	I2C input voltage level LOW	Master to slave			0.5	V
DS_173	$V_{I2C\_LOW\_OUT}$[a]	Slave output level LOW	Open drain, I_{OL} < 4mA			0.5	V
DS_174	C_{I2C_SDA} [a]	SDA load capacitance				400	pF
DS_175	f_{I2C} [a]	SCL clock frequency				400	kHz
DS_176	R_{I2C_PULLUP} [a]	Internal pull-up resistor		25		100	kΩ
6.2 ZACwire™ One-Wire Interface One-wire communication at the DOUT pin.							
DS_060	t_{PWRUP}[a]	Power-on time	Time to ready for communication after power-on; V_{DDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz			3.0	ms
DS_061	$t_{OWI\_STARTWIN}$ [a]	Start window	OWI enabled latest 5ms after power-on; V_{DDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz		250		ms
DS_062	$V_{OWI\_IN\_H}$[a]	OWI input voltage level HIGH	Master to slave	0.80			V_{DDE}
DS_063	$V_{OWI\_IN\_L}$[a]	OWI input voltage level LOW	Master to slave			0.20	V_{DDE}
DS_064	$V_{OWI\_OUT\_L}$	Slave output level LOW	Open drain, I_{OL} < 4mA			0.1	V_{DDE}
6.3 Nonvolatile Memory (NVM)							
DS_065	T_{AMB_NVM} [b]	Ambient temperature for NVM programming		-40		150	°C
DS_066	N_{NVM_MTP} [a]	Re-write cycles	Multiple-time programmable approach is supported	2			
DS_067	t_{NVM_RET}[a]	Data retention	Temperature profile [c]	15			years
DS_068	t_{NVM_WRI} [a]	Programming time	Per written word		1		ms

[a] No measurement in volume production; parameter is guaranteed by design and/or quality observation.

[b] Take into consideration additional package and temperature range restrictions.

[c] Over lifetime and valid for the dice. Note that the package can cause additional restrictions.

7. Circuit Description

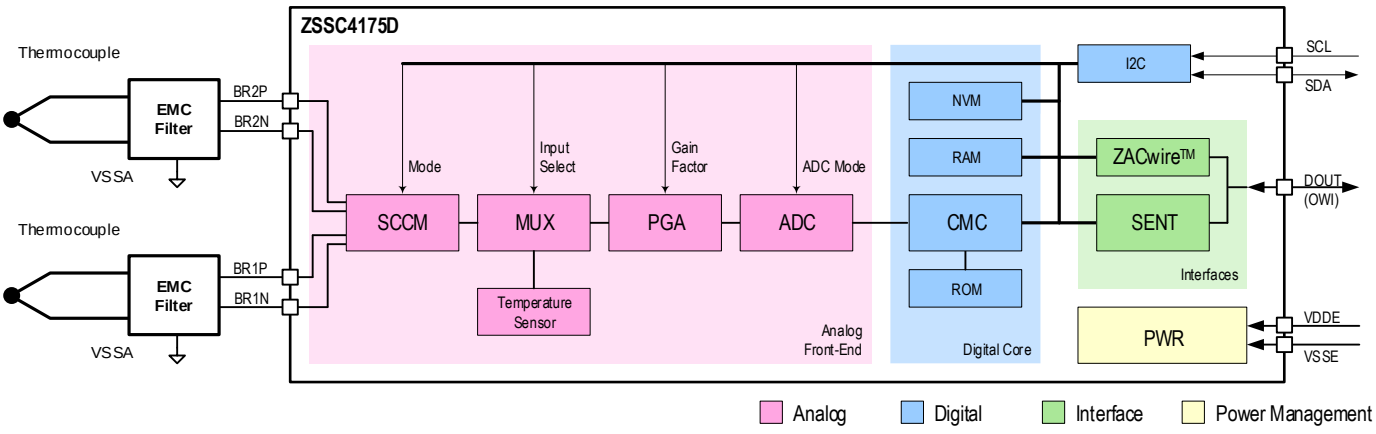
7.1 General Operation Description

The ZSSC4175D-01 is a sensor signal conditioner for readout of thermocouple elements. The thermocouple signal is pre-amplified and converted to a digital signal by the analog-to-digital-converter (ADC). Then the digital conversion result is compensated in terms of thermocouple nonlinearity and internal temperature measurement. Then the calculated conditioning result is output using the SENT protocol.

Signal conditioning processes the following tasks:

- Measurement of the voltage signal from the connected thermocouple element
- Measurement of internal temperature for cold junction compensation
- Diagnostic monitors for chip functionality
- Diagnostic monitors for thermocouple elements
- Conditioning calculation for the thermocouple signal
- SENT output of the conditioning result

Figure 2. Block Diagram



SCCM	Sensor Check and Common Mode Adjustment Unit
MUX	Multiplexer
PGA	Programmable Gain Amplifier
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
ROM	Read-Only Memory for Correction Formula and Algorithm
NVM	Nonvolatile Memory for Configuration and Conditioning Coefficients
RAM	Volatile Memory for Configuration and Conditioning Coefficients
SENT	SENT Controller and SENT Physical Layer Output Stage
ZACwire™	Digital One-Wire Interface
I2C	I2C Digital Interface
PWR	Power Management and Protection Unit

7.2 Signal Path

The ZSSC4175D-01 signal path consists of the analog front-end (AFE), the digital signal processing unit, the SENT Controller, and the SENT physical interface (SENT PHY). In addition, the SENT PHY supports a serial digital one-wire interface (ZACwire™).

Each thermocouple signal is input via the BR1P and BR1N pins, or the BR2P and BR2N pins, and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (analog ground; equal to $V_{DDA}/2$) so that it is possible to process positive and negative differential input signals. These differential signals are pre-amplified by the programmable gain amplifier (PGA) and are converted to digital values by the A/D converter (ADC).

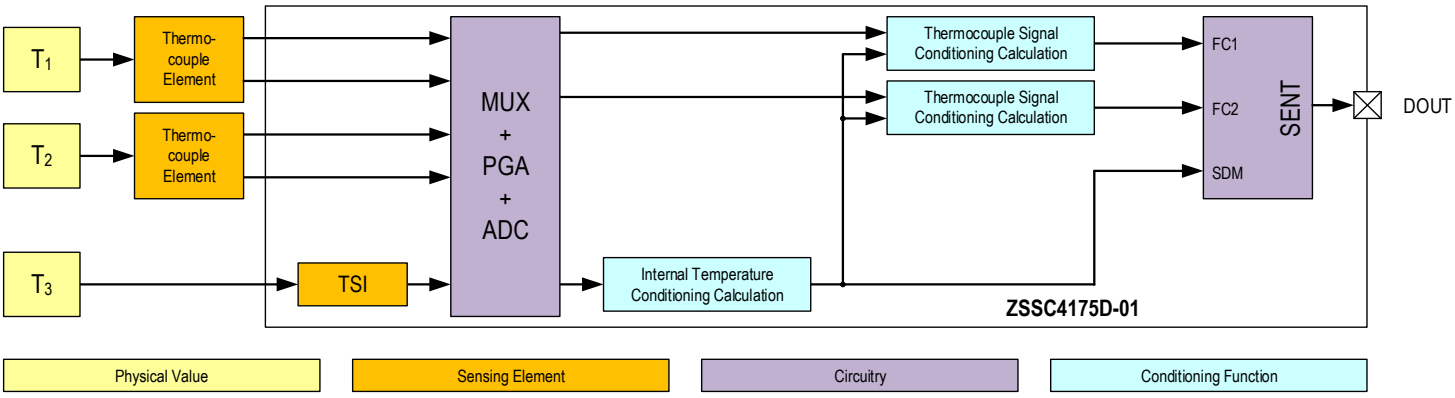
A multiplexer (MUX) selects and transmits the signals from either the thermocouple element or the internal temperature sensor to the analog-to-digital converter (ADC) in a defined sequence.

The digital signal correction is processed in the calibration microcontroller (CMC) using thermocouple element-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the manufacturing process by digital one-wire communication via the DOUT pins depending on the final application use case.

During the manufacturing process, raw measurement values provided by the IDT test center can be requested for calculation and fine-tuning of the overall system performance parameters via the digital interfaces.

The ZSSC4175D-01 provides SENT transmission according to the *SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4)*. Depending on the programmed configuration, there are several SENT output modes. These modes include assignment of the various sensor signals to the SENT Fast and Serial Data Message (SDM) communication channels as well as the configuration of the SENT frame itself.

Figure 3. Main Signal Path of the ZSSC4175D-01 Application



7.3 Signal Conditioning

7.3.1 Thermocouple Sensor Signal Conditioning

The ZSSC4175D-01 uses a spline interpolation for compensation of thermocouple nonlinearity. The spline formula uses thermocouple element-specific coefficients stored in the NVM. Signal conditioning will map thermocouple input data to a standardized SENT output format. The formula and coefficient handling are described in the *Configuration Description Report* (CDR) included with the product delivery. Thermocouple conditioning is processed every time that a new thermocouple input value is available. Therefore, the repetition time of the thermocouple measurement will define the internal output update rate (OUR).

7.3.2 Internal Temperature Sensor Signal Conditioning

The internal temperature sensor signal conditioning is processed every time that a new internal temperature measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset and gain, and of the nonlinearity.

7.4 Analog Front-End

7.4.1 Overview

The analog front-end (AFE) consists of the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC). The internal offset of the analog front-end is eliminated by an auto-zero compensation.

7.4.2 SCCM

The sensor connection check module (SCCM) provides the thermocouple supply voltage and the connection check functionality. It can measure the required driving current and can inject a current into the bridge pins.

7.4.3 Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path utilizing a single ADC. It allows a very flexible signal routing between the thermocouple elements and the ZSSC4175D-01.

7.4.4 Programmable Gain Amplifier

Thermocouple input voltage will be preamplified before it is passed to ADC. The gain is configured to a fixed value. The adjustment for the SENT output can be done with coefficients in the NVM.

7.4.5 Analog-to-Digital Converter

The analog-to-digital converter is implemented using the full-differential switched-capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC provides adjustability of the A/D conversion input voltage range.

7.5 Signal Measurement

7.5.1 Thermocouple Element Measurement

The ZSSC4175D-01 measures two differential signals (BR1P to BR1N and BR2P to BR2N). The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to internal bandgap voltage.

7.5.2 Internal Temperature Measurement

The ZSSC4175D-01 supports an internal proportional-to-absolute-temperature (PTAT) measurement. This temperature will be used for cold junction compensation and SENT output if selected. The temperature offset between the cold junction temperature and the IC temperature after self-heating can be adjusted with coefficients in the NVM.

7.5.3 Isolation Conductance Measurement (Giso)

The ZSSC4175D-01 measures the required supply current to bias the BR1P and BR2P pins. This is used to calculate an equivalent resistance value connected to the supply. This is used to detect a short to the supply or ground if the resistance is lower than the limit.

7.5.4 Thermocouple Resistor Measurement (Ropen)

The ZSSC4175D-01 injects current into the BR1N and BR2N pins to measure the thermocouple resistance. This is used to detect an open connection of the thermocouple if the resistance is above the limit.

7.5.5 Measurement Cycle

The measurement cycle is the sequence of measurements processed during the Normal Operation Mode (NOM). It delivers the raw measurement results from all connected thermocouples and from the supervision functions. The measurements are processed sequentially, all using the ADC to convert the analog input voltages to a digital value.

All measurement tasks will create the measurement cycle that is processed in a loop during NOM continuously. All measurements are executed at least once in this measurement cycle. Measurement tasks that are related to thermocouple measurements are measured most frequently in the main measurement slots while all other measurements are inserted alternatively as auxiliary measurements.

The sequence of measurements is retained even if any fault check connected to a measurement is disabled. The sensor signal conditioning is synchronized to the main measurement tasks to ensure a regular internal output update rate.

The list of available measurements and the complete measurement cycle are explained in the *Configuration Description Report* (CDR).

7.6 SENT Output

7.6.1 Overview

The ZSSC4175D-01 provides three different digital interfaces for the output of data and status messages:

- The SENT controller and physical layer for SENT transmission complies with the *SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4)* and enables readout of the conditioned thermocouple signal data.
  - SAE 27J16 JAN2010 (SENT Rev. 3) specifies up to 32 SDM messages in one SDM cycle.
  - SAE 27J16 APR2016 (SENT Rev. 4) specifies up to 64 SDM messages in one SDM cycle. This is supported in regards to the absolute number of SDMs in one cycle, but the amount of different SDMs is limited to 32
- The ZACwire™ interface for one-wire communication supports the sensor configuration and manufacturing process.
- The I2C interface supports the sensor configuration and manufacturing process.

The SENT interface is the main application output interface. The configuration of the SENT frame format and the assignment of thermocouple signals and fault messages to the SENT output channels are configurable.

In addition to other protocols, the SENT interface supports the application-specific SENT protocols* *High Temperature Sensor (T or T/t), Single High Temperature Secure Sensor (T/S or T/S/t)* and *High Temperature / High Temperature Sensor (T1/T2 or T1/T2/t).*

* According to SAE J2716 APR2016 (SENT Rev. 4) because JAN2010 does not provide a detailed SENT sensor class for high temperature sensors.

In the SENT protocols, the following abbreviations are used:

T = Temperature information used in Fast Channel

S = Secure counter used in Fast Channel (only available in H.5 and H.4 *)

t = Cold junction temperature

Table 6. Requirements – SENT Output Protocol

No.	Parameter
DP_017	SENT Protocol High Temperature Sensor T and T/t
DP_018	SENT Protocol High Temperature Secure Sensor T/S and T/S/t
DP_019	SENT Protocol High Temperature / High Temperature Sensor T1/T1 and T1/T2/t

7.6.2 SENT Fast Channel Modes and Frame Format

The ZSSC4175D-01 SENT interface supports various frame configurations:

- SENT Fast Channel Mode: one or two Fast data channels.
- SENT Transmission Mode: fixed SENT frame length and adjustable pause pulse, or SENT transmission without pause pulse.

The ZSSC4175D-01 provides the following different Fast data channel modes:

- 12-bit FC1 (3 nibbles) (H.2 *)
- 12-bit FC1 and 12-bit FC2 (6 nibbles) (H.1 *)
- 12-bit FC1, 8-bit rolling counter and 4-bit zero (6 nibbles) (H.5 *)
- 12-bit FC1, 8-bit rolling counter and 4-bit MSN of FC1 inverted (6 nibbles) (H.4 *)

The SENT frame transmission is not synchronized to the ZSSC4175D-01 internal output data update. The internal output data update is determined by the fixed ADC resolution for the thermocouple element signal measurements and supervision function measurements. The output update rate and the SENT frame length are generally different. Depending on the SENT frame length used, it is possible that individual data is either sent twice or it is skipped and not sent at all.

After power-on, the initial output values of the SENT Fast data channels are defined by the selected SENT output mode as described in section 7.6.4.

Table 7. Requirements – SENT Fast Channel Modes and Frame Format

No.	Parameter	Value	Unit
DP_020	Fast channel modes	4	–
DP_021	Fast channel 1 data: conditioned thermocouple element signal of thermocouple 1	n.a.	–
DP_022	Fast channel 2 data: source assignment configurable ▪ Inverted conditioned thermocouple element signal of thermocouple 1 ▪ Secure counter information ▪ Conditioned thermocouple element sensor of thermocouple 2	n.a.	–

7.6.3 SENT SDM Channel Modes

The ZSSC4175D-01 SENT interface supports up to 32 different serial data messages (SDM) transmitted in the SDM data channels. The SDM format, the number of SDMs, and the transmission priority are configurable as illustrated in the examples given in Table 8 and Figure 4. Refer to the CDR for programming instructions and descriptions of the fields used in configuration.

- Enhanced SDM format with up to 32 SDMs
- Mode with no SDM available (SDM bits in the status nibble are set to “0”)
- Configurable SDM IDs
- Three priority levels; configurable sequence of SDMs per priority level

Also see section 8.2 regarding fault messaging using the SDM Channel.

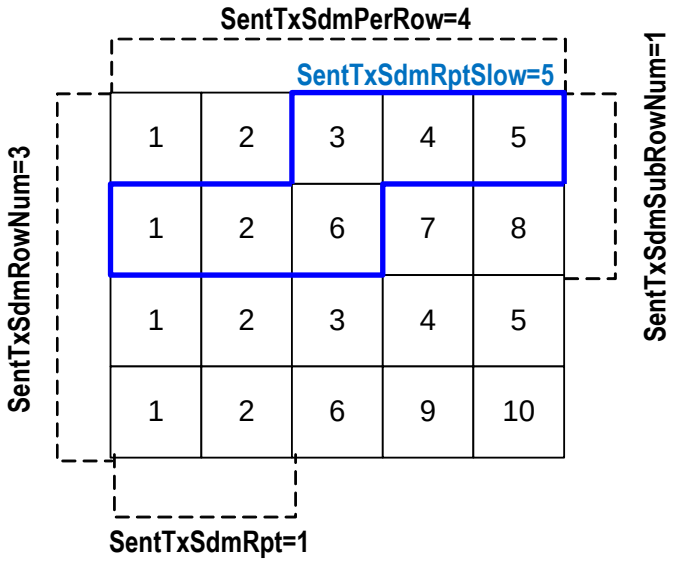
Table 8. Example of SDM ID Priority Level and Sequence Configuration

Priority Level	SDM ID			
1	*1*	*2*		
2	*3*	*4*	*5*	*6*
3	*7*	*8*	*9*	*10*

Configuration via Field	Value
SentTxSdmRpt	*1*
SentTxSdmRowNum	*3*
SentTxSdmPerRow	*4*
SentTxSdmRptSlow	*5*
SentTxSdmSubRowNum	*1*

Figure 4. SDM Cycle Example

Note: The **blue** line indicates the number of second-priority SDMs that are repeated in a cycle (adjusted by SentTxSdmRptSlow).



7.6.4 SENT Output Operation Modes

The ZSSC4175D-01 provides SENT output of the conditioned thermocouple element measurement results at the DOUT pin. This pin is also connected to the ZACwire™ interface for "End of Line" communication using a one-wire communication protocol (OWI).

There are four different modes for starting the OWI communication in combination with the SENT output:

After Initialization:

- SENT transmission starts immediately after the initialization phase.
- During the initialization, the DOUT pin is set to the output idle state.
- SENT data channels are set to their initial value (usually "0") until the first valid thermocouple element values are available.
- OWI Rx is enabled in parallel with the SENT output for a time window.
- OWI communication can be started by transmitting the command for starting the Command Mode (CM) during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

After First Measurement:

- SENT transmission starts after the first measurement and conditioning cycle and thus with the first valid thermocouple element values.
- During the initialization and the first cycle, the DOUT pin is set to the output idle state.
- SENT data channels start transmission with valid values.
- This mode allows the fastest possible transmission of the first thermocouple data after power on.
- OWI Rx is enabled in parallel to the SENT output for a time window.
- OWI communication can be started by transmitting the command for starting CM during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

After 250ms:

- SENT transmission starts only after a time window (approximately 250ms). The DOUT pin is set to the output idle state.
- DOUT is weakly pulled to VDDA (pull-up current: ~2.5µA). OWI Rx is enabled for a specified time window.
- OWI communication can be started by transmitting the command for starting CM during this time window.

Disable SENT:

- SENT transmission is disabled. OWI Rx/Tx is enabled without time limitation. OWI communication can be started by transmitting the command for starting CM.

The output idle state of the ZSSC4175D-01 is defined as follows:

- The DOUT pin is switched to high impedance; DOUT is weakly pulled to VDDA (pull-up current: ~2.5µA).
- The final resulting potential at the output is defined by the (pull-up) load resistor at the SENT communication line.

Table 9. Requirements – SENT Output Operation Modes and Initialization Behavior

No.	Parameter	Value	Unit
DS_079	Number of SENT output operation modes	4	–

7.6.5 SENT Pulse Shaping

The ZSSC4175D-01 has several fixed adjustment options optimized for rise and fall times depending on the SENT tick time. This helps obtain optimal EMC performance regarding electromagnetic emission.

7.7 NVM OEM Data Memory

The ZSSC4175D-01 provides a NVM memory area for the storage of OEM data, which is physically part of the NVM memory module (OTP; i.e., one-time programmable) but is delimited from the configuration and calibration data by dedicated commands for read and write access. Data protection and multiple-time programming data management must be implemented by the OEM.

Table 10. NVM OEM Data Memory

No.	Parameter	Value	Unit
DS_081	NVM OEM data memory (OTP)	64	16-bit words
DS_082	NVM OEM data memory (OTP) with dedicated command set	64	16-bit words

7.8 Over-Voltage and Short-Circuit Protection

The ZSSC4175D-01 is designed for a 5V supply provided by an electronic control unit (ECU).

The ZSSC4175D-01 and the connected thermocouples are protected from over-voltage and reverse-polarity damage by an internal supply voltage limiter. The SENT output pin DOUT is protected regarding short circuits, over-voltage conditions, and reverse polarity. These functions are described in Table 11 and are valid for operation of the ZSSC4175D-01 in the application circuit shown in section 10 within the specifications of absolute maximum ratings given in section 3.

Note: The specified junction temperature range T_{J_ABS} (Table 2) is in force not only for operation but also for all the protection cases listed in Table 11. In the event of an over-voltage, the device might have increased power dissipation. Depending on the thermocouple temperature, which results in a different R_{ISO} value, and depending on the output load, this might lead to a violation of the maximum junction temperature.

Table 11. Over-Voltage, Reverse-Polarity, and Short-Circuit Protection

Note: See important notes at the end of the table.

Requirement	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Over-Voltage and Reverse-Polarity Protection							
DS_085	V_{DDE_OV1}	Maximum voltage at VDDE to VSSE	DOUT is connected to VSSE or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_086	V_{DDE_OV2}	Maximum voltage at VDDE to DOUT	VSSE is connected to DOUT or VDDE [a] (connection resistance value = 0 to ∞)	0		18	V
DS_087	V_{DOUT_OV1}	Maximum voltage at DOUT to VSSE	VDDE is connected to DOUT or VSSE (connection resistance value = 0 to ∞)	0		18	V
DS_088	V_{DOUT_OV2}	Maximum voltage at DOUT to VDDE	VSSE is connected to DOUT [a] or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_089	V_{SSE_OV1}	Maximum voltage at VSSE to VDDE [a]	DOUT is connected to VSSE or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_090	V_{SSE_OV2}	Maximum voltage at VSSE to DOUT [a]	VDDE is connected to DOUT or VSSE (connection resistance value = 0 to ∞)	0		18	V

Requirement	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Short Circuit Protection							
DS_091	$I_{VDDA\_SHRT\_VSSA}$	Current limitation in the event of a VDDA to VSSA short circuit				60	mA
DS_092	$I_{DOUT\_SHRT\_VSSE}$	Current limitation in the event of a DOUT to VSSE short circuit		-15		-5	mA
DS_093	$I_{DOUT\_SHRT\_VDDE}$	Current limitation in the event of a DOUT to VDDE short circuit		5		15	mA

[a] Reverse-polarity condition.

8. Fault-Safe Operation

8.1 Fault-Safe Operation Modes

Fault checks verify the operation of the ZSSC4175D-01 and of the connected thermocouple element at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is provided via one of the two methods described below depending on the diagnostic mode.

The ZSSC4175D-01 differentiates between two DMs with different behavior:

Static Diagnostic Mode

- Measurement and conditioning cycle are interrupted.
- SENT transmission is stopped, and the output pin DOUT is either driven to a HIGH output level or is switched to high impedance.
- The ZACwire™ interface for one-wire communication (OWI) is enabled; both RAM output pages are readable. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing.
- If enabled, the watchdog will trigger reset, i.e. the ZSSC4175D-01 is restarted including a reset of all status registers.
- The ZSSC4175D-01 can be restarted by a power-off/power-on sequence.

Temporary Diagnostic Mode

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault confirmation (see below).
- SENT transmission is continued. At least one of the following fault messaging options is activated:
  - The fault code is transmitted in the SENT Fast Channel.
  - Fault bit(s) are set in the SENT status nibble.
  - The fault code is transmitted in the SDM Channel (SENT fault messaging and fault codes are configurable).
- The ZACwire™ interface for one-wire communication (OWI) is enabled. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing (SENT output must be overwritten by the OWI master).
- The ZSSC4175D-01 returns to Normal Operation Mode including SENT transmission of valid thermocouple signals if fault checks do not detect continuation of fault conditions.

The fault confirmation of the ZSSC4175D-01 is defined as follows:

- Fault confirmation is only processed for fault checks assigned to the Temporary DM.
- Fault confirmation is a low-pass filter that delays the activation and deactivation of the Temporary DM.
- In the event of a fault detection, faults are re-checked before entering Temporary DM.
- In the case of Temporary DM, detected fault conditions that no longer exist are re-checked before returning from Temporary DM to NOM.
- Fault confirmation is an up-and-down event counter that allows confirmation of a failure event.

8.2 Fault Messaging

8.2.1 Overview

The SENT offers three options for fault messaging:

- Fault codes in the data channels (the Fast Channels as well as the SDM Channels; e.g., the channel used for temperature)
- Two status bits in the SENT status nibble
- SDM Channel status word

8.2.2 SENT Fast Channel Fault Codes

For the 12-bit SENT Fast Channel, the output value interval [4089, 4095] is reserved for fault codes. This is according to the SENT standard. In addition, the value 0 is used for signal initialization (no valid data available).

In the ZSSC4175D-01, the SENT Fast Channel fault codes are selectable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the fault code of the highest prioritized fault is transmitted.

8.2.3 SENT Status Bits

According to the SENT standard, the SENT status nibble contains two bits for status information. The assignment of the status bits to the individual detectable faults is configurable.

8.2.4 SENT SDM Channel Status Codes

The SENT standard defines a SMD Channel status word assigned to the SDM identifier #01.

In the ZSSC4175D-01, the SENT SMD Channel status codes are freely programmable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the status code of the highest prioritized fault is transmitted. See section 7.6.3 for details.

8.2.5 Timing Definitions

The timing for the update of the SENT output and for the fault messaging is defined in Figure 5 and Figure 6. The relevant timing parameters are listed in Table 12.

Table 12. Timing Parameter

Symbol	Parameter	Description
OUR	Output update rate	Internal update rate of the main signal data
ORT	Output response time	Latency from the main signal event to the completion of the SENT transmission of this signal event
DTI	Diagnostic testing interval	Rate of fault check processing
FMT	Fault messaging time	Latency from the fault event to the completion of the SENT transmission of the fault message

Figure 5. Output Update Timing Diagram

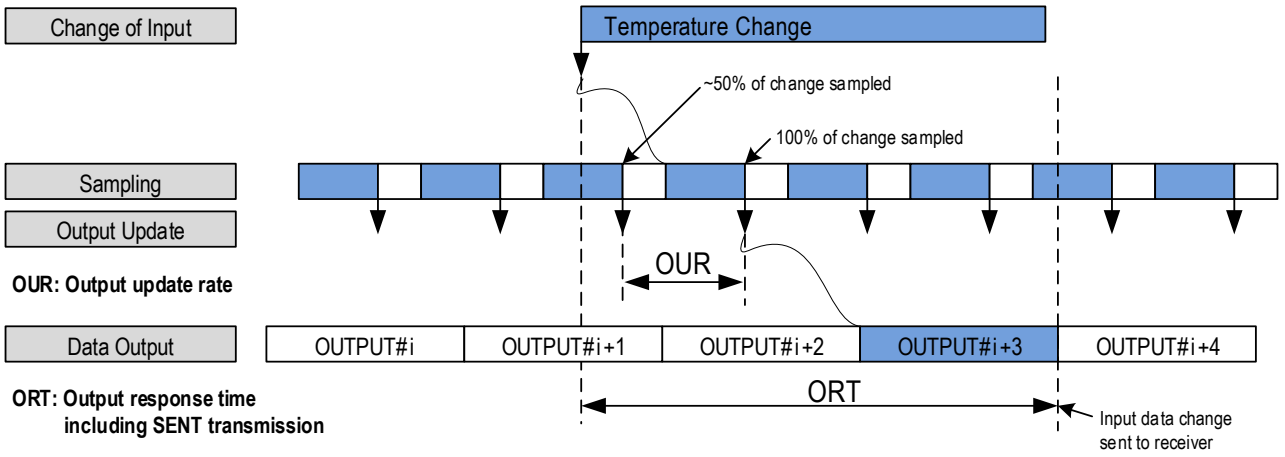
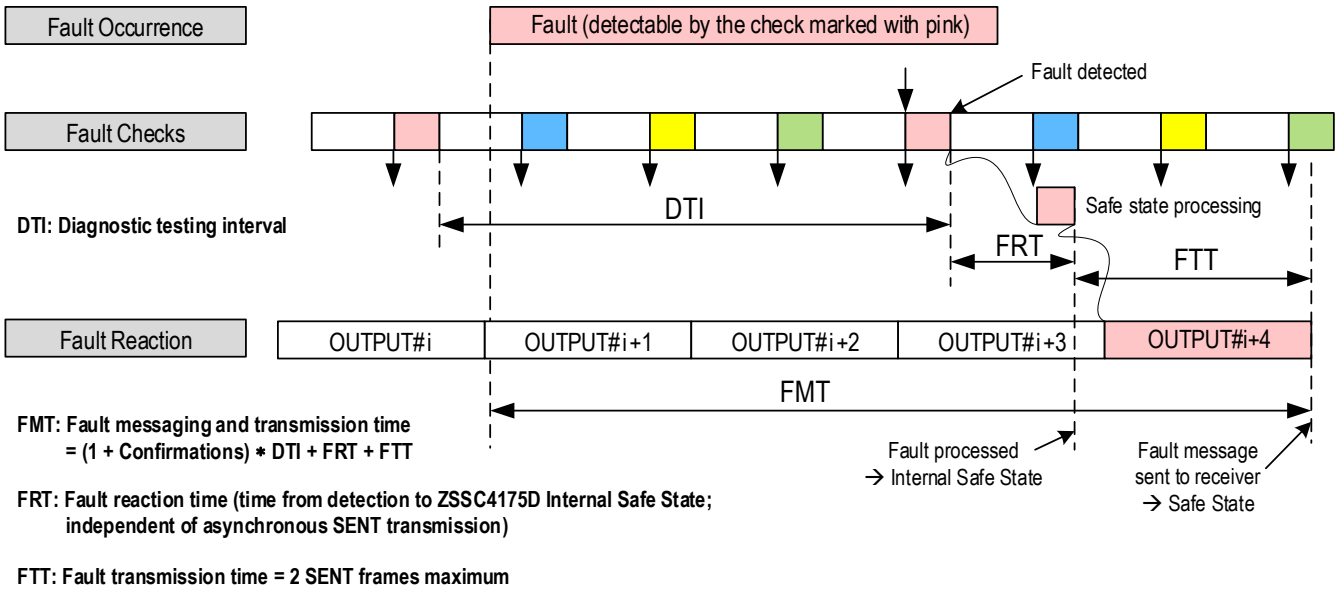


Figure 6. Fault Messaging Timing Diagram

Note: In this figure, the different colors indicate the different fault checks processed in the cycle.



9. Fault Checks

9.1 Overview

The ZSSC4175D-01 supports several fault checks that can be evaluated on the application system level to enable fault tolerant operation. These fault checks are supported by three types of monitors:

- Firmware Monitors: implemented in the hardware and firmware of the ZSSC4175D-01.
- Application Monitors: defined by the 4175_0500_01 configuration. These monitors primarily check values for a certain range.
- Transmission Monitors: not implemented by the ZSSC4175D-01 but by the receiver of the conditioned signal data (ECU).

The tables below list the monitors for the supported fault checks.

9.2 Hardware Fault Checks

Table 13. Firmware Monitors

No.	Fault Check	Messaging Time	Active	DM Type
DS_094	V_{DDA} under-voltage check (VDDAPOR); power-on reset	< 200µs	Always on	Static
DS_095	Digital supply under-voltage check (VDDDBOD); brownout detection	< 200µs	Always on	Static
DS_096	Oscillator fail check (OSCFAIL)	< 200µs	Always on	Static
DS_097	ROM CRC check (ROMCRC)	< FMT	Always on	Static
DS_098	NVM CRC check (NVMCRC)	Power-on	Always on	Static
DS_099	RAM CRC check (RAMCRC)	< FMT	Always on	Static
DS_100	RAM parity check (RAMPRTY)	< FMT	Always on	Static
DS_101	Windowed watchdog (WWDG)	< FMT	Always on	Static
DS_102	Initialization phase check (INITCRC)	Power-on	Always on [a]	Static
DS_103	Measurement cycle check (MCYCCRC) including ▪ AFE input multiplexer check (AFEMUX) ▪ Register data check (REGCRC)	< FMT	Always on [a]	Static
DS_104	Conditioning cycle check (CCYCCRC)	< FMT	Always on [a]	Static
DS_107	Broken Chip Check (CHIPP)	< FMT	Always on	Static

[a] Must be ensured in customer production line by sending command RunCycCrcCalc to the IC.

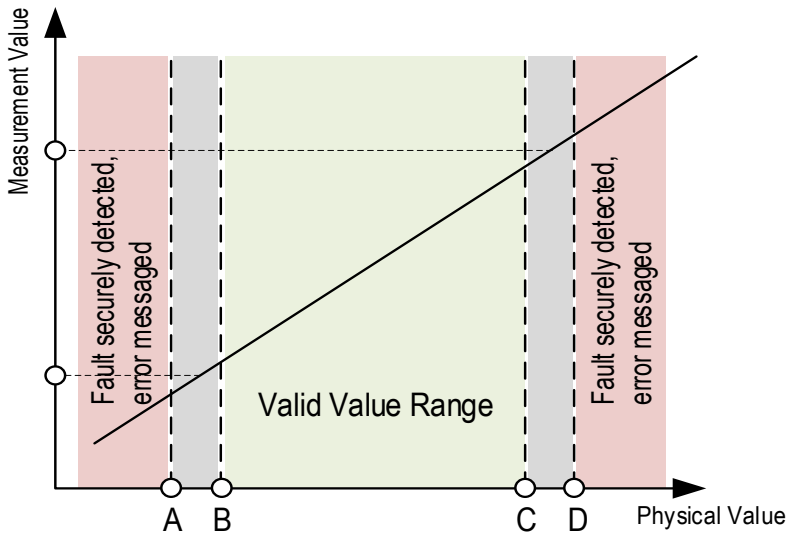
9.3 Application Monitors

The ZSSC4175D-01 provides several fault checks mainly based on the monitoring of a physical value. A fault is detected if the measurement value exceeds or falls below a given threshold. For every measurement, there is a certain transfer characteristic from the monitored physical value to the measurement value. The reverse function maps a threshold to a specific physical value. Because of the part-dependent measurement tolerance, a defined threshold spreads out over a certain range determined by a lower value and an upper value. The range limits are defined using A, B, C, and D references in Table 14 and Figure 7. A fault is securely detected if the physical value falls below the lower value (A) coming from the lower threshold, or if it exceeds the upper value (D) coming from the upper threshold. Otherwise it is ensured that no fault is messaged if the physical value is in the range between the upper value (B) coming from the lower threshold and the lower value (C) coming from the upper threshold.

Table 14. Fault Check Threshold Definition

Threshold	Description
A	If the physical value is below this measured value, the fault is securely detected and messaged.
B	If the physical value is above this measured value, a non-fault state is securely detected.
C	If the physical value is below this measured value, a non-fault state is securely detected.
D	If the physical value is above this measured value, the fault is securely detected and messaged.

Figure 7. Fault Check Thresholds



Note that there are multiple application monitors as defined in Table 15. Some have thresholds predefined by IDT. Others can have custom thresholds. All monitors require a correctly programmed and calibrated configuration to ensure the correct fault check operation.

Table 15. Application Monitors

No.	Group	Block [a]	Monitor [a]	Thresholds	Unit
DP_023	1	TC1 Meas	ADCOFFSRNG	n/a	
DP_043	1	TC2 Meas	ADCOFFSRNG	n/a	
DS_106	1	Hardware Check	ICSM	n/a	
DP_024	1	Afe Gain Check	AFEGAIN	n/a	
DP_034	2	Supply Check	VSUPOV	5.7 ± 0.2	V
DP_033	3	Supply Check	VSUPUV	4.3 ± 0.2	V
DP_029	4	ChipTempMeas	TSI	n/a	
DP_030	4	CJ Norm	ORNG	Custom [a]	°C
DP_031	4	CJ Norm	URNG	Custom [a]	°C
DP_026	6	TC1 Check	TCISOLOW	25 to 100	kΩ
DP_025	7	TC1 Check	TCISOHIGH	50 to 200	kΩ
DP_036	9	TC2 Check	TCISOLOW	25 to 100	kΩ
DP_037	10	TC2 Check	TCISOHIGH	50 to 200	kΩ
DP_038	11	TC1 CSAT	CSAT	n/a	
DP_028	11	TC1 Meas	TCRAW	n/a	
DP_027	11	TC1 Check	TCC	15 ± 2	Ω
DP_039	12	TC2 CSAT	CSAT	n/a	
DP_040	12	TC2 Meas	TCRAW	n/a	
DP_041	12	TC2 Check	TCC	15 ± 2	Ω
DP_032	13	TC1 Lin	OUTRNG	Custom [a]	°C
DP_042	14	TC2 Lin	OUTRNG	Custom [a]	°C
DP_035	15	Computational Saturation	CSAT	n/a	

[a] See the *Configuration Description Report* (CDR) for more information.

9.4 Transmission Fault Checks

Transmission fault checks must be implemented on the receiver side of the conditioned output signals of the ZSSC4175D-01 (typically the ECU).

Table 16. SENT Transmission Monitors

Fault Check	Messaging Time	Adjustable	Notes
SENT CRC (SENTCRC)	t_{FRAME}	n.a.	SENT receiver
SENT timeout (SENTIMEOUT)	t_{FRAME}	n.a.	SENT receiver
SENT sync time (SENTSYNC)	t_{FRAME}	n.a.	SENT receiver
SENT supply monitor (SENTPWR)	t_{FRAME}	n.a.	SENT receiver
SENT idle state (SENTIDLE)	t_{FRAME}	n.a.	SENT receiver

10. Application Circuit and External Components

Figure 8. Application Circuit Example of a Temperature Sensor with SENT Output

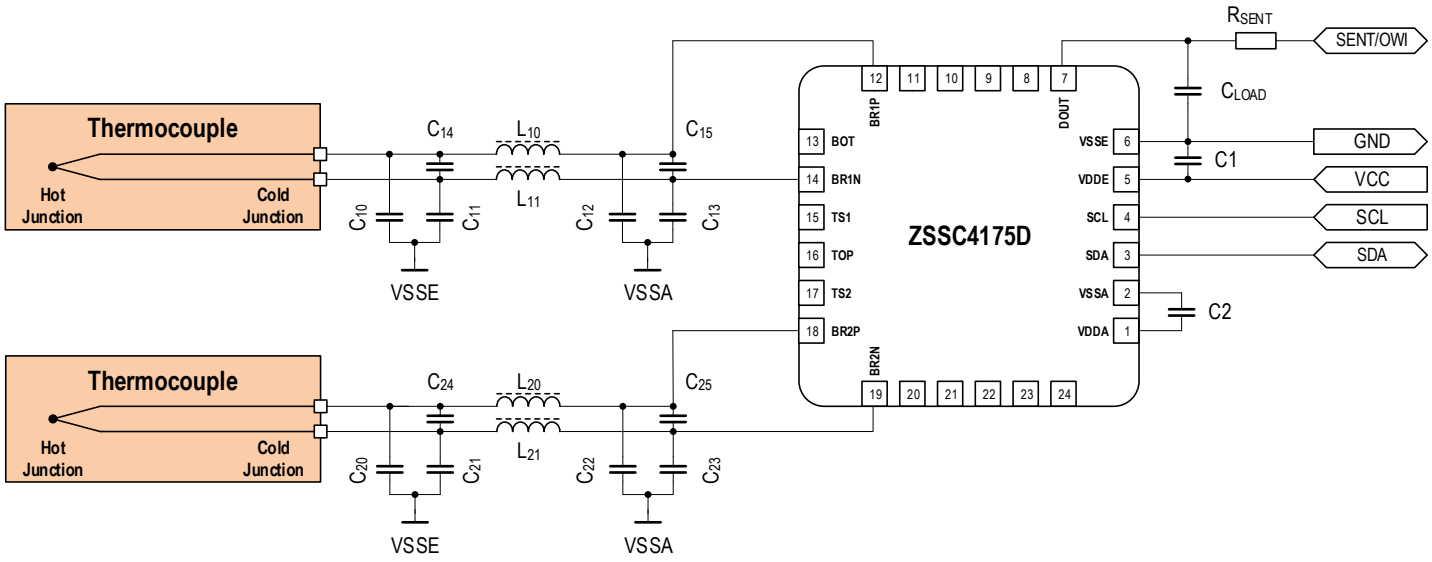


Table 17. Dimensioning of External Components for the Application Example

Component	Symbol	Conditions	Min	Typical	Max	Unit
Capacitor	C1 [a]	V_{MAX} ≥ 32V		100 ± 20%		nF
Capacitor	C2 [a]	V_{MAX} ≥ 10V		100 ± 20%	470 + 20%	nF
Capacitor	C_{LOAD}	V_{MAX} ≥ 32V		2.2 ± 20%		nF
Resistor	R_{SENT}				47 + 5%	Ω
Capacitor	C_{10} to C_{15}	Sum of all capacitances at one node V_{MAX} ≥ 10V			15	nF
Capacitor	C_{20} to C_{25}	Sum of all capacitances at one node V_{MAX} ≥ 10V			15	nF
Ferrite Bead (e.g. BLM18HK102)	L_{10} to L_{21}	DC resistance < 2.5Ω Suitable for noise suppression within a wide frequency range	0	333		Z[Ω] at 0Hz

[a] Device is mandatory for meeting specifications described in section 5.

Note: The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

- Physical cold-junction connection should be placed as close as possible to cold-junction temperature measurement (IC).
- Symmetric PCB design is recommended.
- Capacitive coupling from thermocouples to external supply ground is recommended (C_{10}, C_{11}, C_{20}, C_{21}).

11. ESD Protection and EMC Specification

11.1 ESD Protection

All pins have an ESD protection of ≥2000V according to the Human Body Model (HBM with 1.5kOhm/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE, and DOUT pins have an additional ESD protection of ≥ 4000V (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7).

The levels of ESD protection are tested with devices in a 4 × 4 mm 24-QFN package during the product qualification.

11.2 Electromagnetic Emission

The wired emission of the externally connected pins of the ZSSC4175D-01 is measured according to the following standard: *IEC 61967_4:2002 + A1:2006.*

Measurements must be performed with the application circuit described in Figure 8; SENT transmission uses a tick time of 9µs.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN*. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN.*

11.3 Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard:

Measurements must be performed with the application circuit described in Figure 8; the thermocouples are replaced by 5Ω resistors connected between the bridge pins BR1P, BR1N, and BR2P, BR2N; SENT transmission uses a tick time of 9µs.

Table 18 gives the specifications for the DPI tests. RES refers to the coupling impedance. CAP refers to the injection capacitance.

Table 18. Conducted Susceptibility (DPI) Tests

No.	Test	Frequency Range	Power	Load Pins	Protocol	Error Band [a]	Comment
DS_169	DPI, direct coupled	1MHz to 10MHz	20dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP= 4.7nF
DS_170	DPI, direct coupled	>10MHz	30dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP = 4.7nF

[a] Error band regarding main signal (SENT FC1).

12. Reliability and RoHS Conformity

The ZSSC4175D-01 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate < 5 FIT (junction temperature = 55°C, confidence level = 60%, activation energy = 0.7eV) is estimated.

The reliability calculation is based on an average operating junction temperature of 90.5°C over an operating lifetime of 15000 hours in normal operating conditions and according to the ambient temperature profile listed in Table 19.

Table 19. Ambient Temperature Profile (Example)

Operating Ambient Temperature [°C]	Relative Time [%] Based on a 15000h Operating Lifetime	Absolute Time [h]
-40	2	300
-20	8	1200
0	15	2250
25	25	3750
55	25	3750
85	17	2550
125	6	900
150	2	300

Examples of self-heating (typical thermal resistor in a 24-QFN package is $R_{th\_JA\_QFN24}$ = 32K/W):

- Normal Operation:

  Maximum supply current = 11mA (at 5.5V); minimum SENT load resistance = 10kΩ; maximum voltage = 5.5V.

  Maximum power dissipation P_{max} = 5.5V · 11mA + 5.5V · 5.5V / 10kΩ ≈ 61mW.

  Temperature difference: $T_J - T_{AMB}$ = 32K/W · 61mW < 2K.

  → With the conditions above, the typical junction temperature T_J is < 4K greater than the ambient temperature T_{AMB}.

- Over-Voltage Conditions (18V):

  Maximum power dissipation $P_{max,OV}$ = 300mW; output is switched off.

  Temperature difference: $T_J - T_{AMB}$ = 32K/W · 300mW = 9.6K

  → With these conditions, the typical junction temperature T_J is ~10K greater than the ambient temperature T_{AMB}.

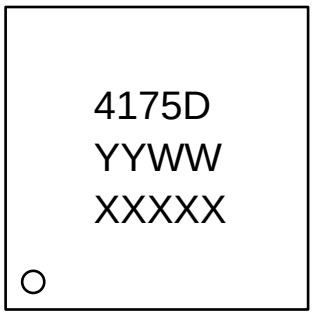
The ZSSC4175D-01 complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration and other declarations regarding environmental compliance including a material declaration sheet are available on request.

13. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.idt.com/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-085-mm-body-050mm-pitch-epad-250-x-250-mm-wettable-flank

14. Marking Diagram



1. “4175D” is the truncated part number.
2. “YYWW” is the last digits of the year and week that the part was assembled.
3. “XXXXX” is the last digits of the lot number.

15. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
CDR	Configuration Description Report
CM	Command Mode
CMC	Calibration Microcontroller; optimized microcontroller architecture for IDT signal conditioners
DM	Diagnostic Mode
DNL	Differential Nonlinearity
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FC	Fast Channel; transmitted in SENT frame
FMT	Fault Messaging Time
FS	Full Scale
HBM	Human Body Model
I/O	Input/Output
I2C	Inter-integrated Circuit; serial two-wire data bus
INL	Integral Nonlinearity
LSB	Least Significant Bit
LSN	Least Significant Nibble
MSB	Most Significant Bit
MSN	Most Significant Nibble
MUX	Multiplexer
MTP	Multiple-Time Programmable
n.a.	Not Applicable
NOM	Normal Operation Mode
NVM	Nonvolatile memory
OTP	One-Time Programmable
OWI	One-Wire Interface
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
POR	Power-On Reset
PTAT	Proportional-to-Absolute Temperature

Term	Description
PWR	Power Management and Protection Unit
QFN	Quad-Flat No-Leads – ZSSC4175D-01 package
RAM	Volatile Memory for Configuration and Conditioning Coefficients
RISC	Reduced Instruction Set Computing
ROM	Read-Only Memory
SCCM	Sensor Check and Common Mode Adjustment Unit
SDM	Serial Data Message; transmitted in the slow channel of SENT protocol
SENT	Single Edge Nibble Transmission; communication protocol for automotive applications defined by SAE International.
TSI	Internal Temperature Sensor
ZACwire™	IDT-specific one-wire interface

16. Ordering Information

Part Number	Description and Package	MSL Rating	Shipping Packaging	Temperature
ZSSC4175DE4R	Dual Thermocouple input, SENT output, internal temperature measurement, 4 × 4 mm 24-QFN, wettable flanks	MSL1	13” Reel	-40°C to 150°C
ZSSC4175DE4W	Dual Thermocouple input, SENT output, internal temperature measurement, 4 × 4 mm 24-QFN, wettable flanks	MSL1	7” Reel	-40°C to 150°C
ZSSC4175KIT	ZSSC4175 SSC Evaluation Kit: Communication Board, ZSSC415x/6x/7x Evaluation Board, USB Cable, ZSSC4175D Test PCB, Tweezer, 5 Samples.			

Contact IDT for additional options.

17. Revision History

Revision Date	Description of Change
June 7, 2019	▪ DS_105 (SENTDATA monitor) removed. ▪ Thresholds for supply voltage monitor (DP_033, DP_034) changed.
April 16, 2019	Revision of part codes and product references. Product is now referred to as the ZSSC4175D-01
February 26, 2019	▪ DP_015: Fault message time is now unique because failure confirmation is fixed as “one.” ▪ DP_017, DP_018, DP_019: Irrelevant columns “value” and “Unit” removed. ▪ DS_020, DS_066, DS_081, DS_082: Corrected. ▪ DP_027, DP_041: Threshold increased. ▪ Figure 6: Reference of C_{10}, C_{11}, C_{20}, C_{21} changed to VSSE. ▪ Table 16: Maximum values and units fixed for C_{LOAD} and L_{10} to L_{15}. ▪ Chapter 17: Ordering numbers fixed. ▪ SAE 27J16 APR2016 (SENT Rev. 4) compliance documented. ▪ OPR_{TS} informational parameter removed from section 5.1. ▪ Minor edits.
August 30, 2018	Initial datasheet release.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

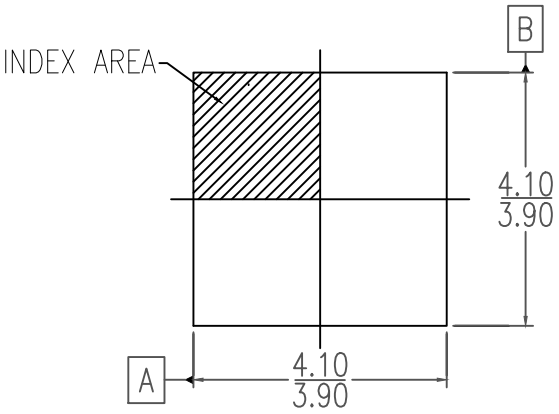
Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

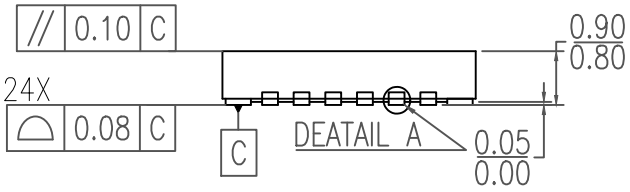
24-VFQFPN, Package Outline Drawing

4.0 x 4.0 x 0.85 mm Body,0.50mm Pitch,Epad 2.50 x 2.50 mm Wettable Flank (Step Cut)

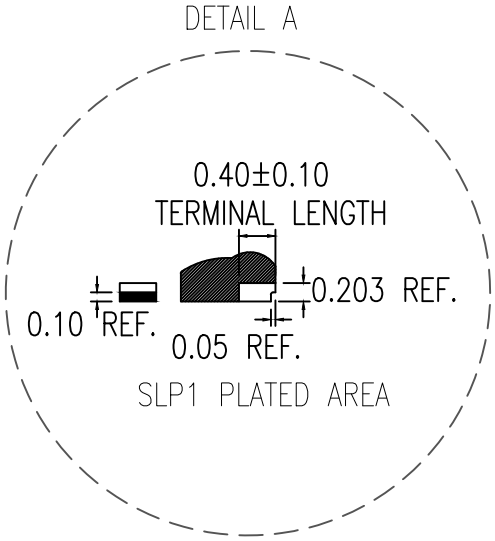
NLG24S2, PSC-4192-05, Rev 02, Page 1

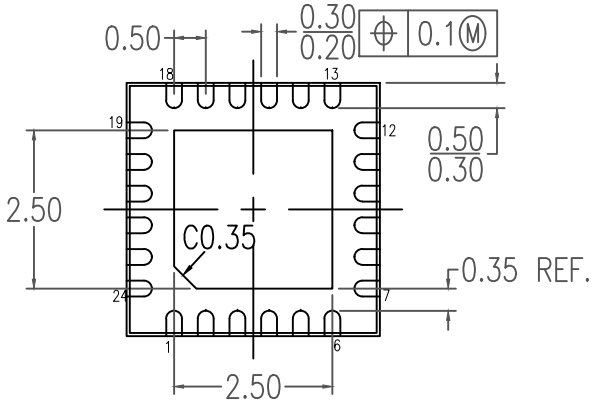


TOP VIEW



SIDE VIEW

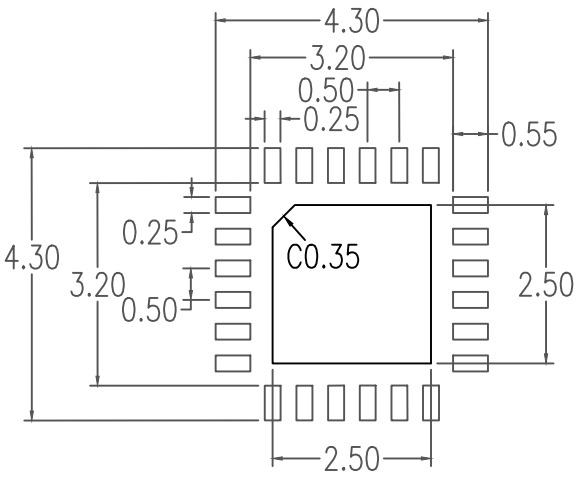




BOTTOM VIEW

NOTE:

1. DIMENSIONS IN MM, ANGLES IN DEGREES.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Nov 5, 2018	Rev 02	New Format, Change EPC Code
Jul 5, 2017	Rev 01	Update Title

LifeElectronics
Живое партнерство

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru