

Compact Flash III series
AP-CFxxxxE3NR-XXXXXXQ

RoHS Compliant

Compact Flash Series III

Industrial CF Specifications

September 10th, 2014

Version 1.5



Apacer Technology Inc.

1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C

Tel: +886-2-2267-8000 Fax: +886-2-2267-2261

www.apacer.com

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

Features:

- **Compact Flash Association Specification Revision 3.0 Standard Interface**
 - ATA command set compatible
 - ATA mode support for up to:
 - PIO Mode-6
 - Multiword DMA Mode-4
 - Ultra DMA Mode-4
- **Connector Type**
 - 50 pins female
- **Power consumption (typical)***
 - Supply voltage: 3.3V & 5V
 - Active mode: 80 mA/95 mA (3.3V/5.0V)
 - Sleep mode: 700 μ A/900 μ A (3.3V/5.0V)
- **Performance***
 - Sustained read: up to 29 MB/sec
 - Sustained write: up to 15 MB/sec
- **Capacity**
 - 128, 256, 512 MB
 - 1, 2, 4, 8, 16 GB
- **NAND Flash Type: SLC**
- **Shock & Vibration****
 - Shock: 1,500 G
 - Vibration: 15 G
- **Temperature ranges**
 - Operating:
 - Standard: 0°C to 70°C
 - Extended: -40°C to 85°C
 - Storage: -40°C to 100°C
- **Flash management**
 - Advanced wear-leveling algorithms
 - S.M.A.R.T. technology
 - Built-in hardware ECC
 - Flash block management
 - Power failure management
- **Endurance (TBW: Terabytes Written)**
 - 128 MB: 3.3 TBW
 - 256 MB: 6.7 TBW
 - 512 MB: 12.9 TBW
 - 1 GB: 25.6 TBW
 - 2 GB: 38.4 TBW
 - 4 GB: 51.9 TBW
 - 8 GB: 69.8 TBW
 - 16 GB: 115.0 TBW
- **Physical Dimensions**
 - 36.4mm x 42.8mm x 3.3mm
- **RoHS compliant**

*Varies from capacities. The values addressed for Performance and Power consumptions are typical and may vary depending on settings and platforms.

**Non-operating

Compact Flash III series

AP-CFxxxxE3NR-XXXXXQ

Table of Contents

| | |
|--|-----------|
| 1. GENERAL DESCRIPTION | 3 |
| 2. FUNCTIONAL BLOCK | 3 |
| 3. PIN ASSIGNMENTS | 4 |
| 4. PRODUCT SPECIFICATIONS..... | 6 |
| 4.1 CAPACITY..... | 6 |
| 4.2 PERFORMANCE SPECIFICATION..... | 6 |
| 4.3 ENVIRONMENTAL SPECIFICATIONS..... | 7 |
| 4.5 ENDURANCE | 7 |
| 5. FLASH MANAGEMENT | 8 |
| 5.1. ADVANCED WEAR-LEVELING ALGORITHMS | 8 |
| 5.2 S.M.A.R.T. TECHNOLOGY | 8 |
| 5.3 BUILT-IN HARDWARE ECC | 8 |
| 5.4 FLASH BLOCK MANAGEMENT | 8 |
| 5.5 POWER FAILURE MANAGEMENT..... | 8 |
| 6. SOFTWARE INTERFACE | 9 |
| 6.1 COMMAND SET..... | 9 |
| 7. ELECTRICAL SPECIFICATION | 11 |
| 7.1 DC CHARACTERISTICS | 12 |
| 7.2 AC CHARACTERISTICS | 13 |
| 7.2.1 Attribute Memory Read Timing Specification..... | 14 |
| 7.2.2 Configuration Register (Attribute Memory) Write Specification..... | 15 |
| 7.2.3 Common Memory Read Timing Specification | 16 |
| 7.2.4 Common Memory Write Timing Specification..... | 17 |
| 7.2.5 I/O Input (Read) Timing Specification..... | 18 |
| 7.2.6 I/O Output (Write) Timing Specification | 19 |
| 7.2.7 True IDE I/O Read Timing | 20 |
| 7.2.8 True IDE I/O Write Timing | 21 |
| 7.2.9 Ultra DMA Mode Data Transfer Input/Output (Read/Write) Timing..... | 22 |
| 7.3.0 Media Side Interface I/O Timing Specifications..... | 34 |
| 8. PHYSICAL CHARACTERISTICS..... | 37 |
| 8.1 DIMENSION..... | 37 |
| 9. PRODUCT ORDERING INFORMATION..... | 38 |
| 9.1 PRODUCT CODE DESIGNATIONS | 38 |
| 9.2 VALID COMBINATIONS | 39 |

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

1. General Description

Apacer's value-added Industrial CompactFlash Card offers high performance, high reliability and power-efficient storage. Regarding standard compliance, this CompactFlash Card complies with CompactFlash specification revision 3.0, supporting transfer modes up to Programmed Input Output (PIO) Mode 6, Multi-word Direct Memory Access (DMA) Mode 4, and Ultra DMA Mode 4.

Apacer's value-added CFC provides complete PCMCIA – ATA functionality and compatibility. Apacer's CompactFlash technology is designed for applications in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications.

2. Functional Block

The Compact Flash Card (CFC) includes a controller and flash media, as well as the Compact Flash standard interface. Figure 2-1 shows the functional block diagram.

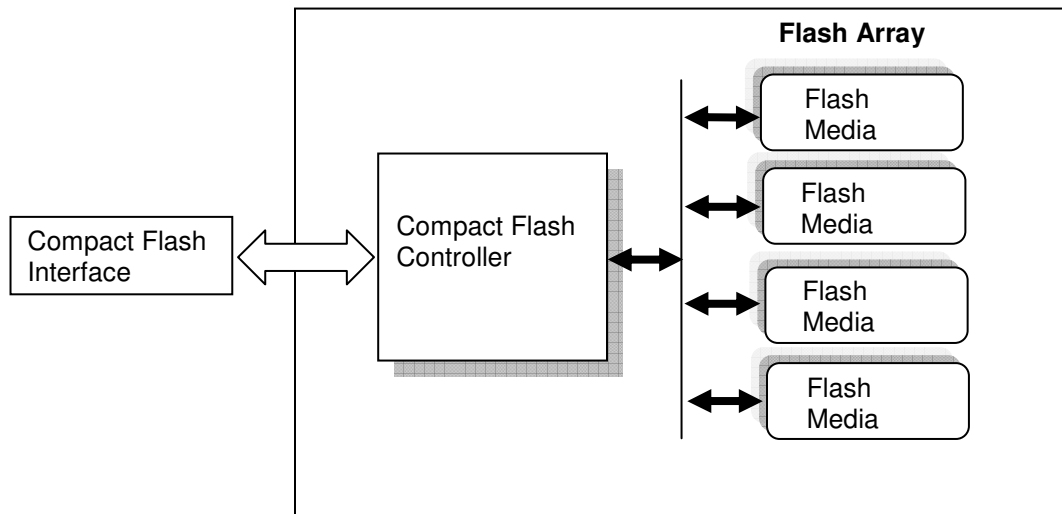


Figure 2-1: Functional block diagram

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A “#” suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1: Pin assignments (1 of 2)

| Pin No. | Memory card mode | | I/O card mode | | True IDE mode | |
|---------|--------------------|--------------|--------------------|--------------|---|--------------|
| | Signal name | Pin I/O type | Signal name | Pin I/O type | Signal name | Pin I/O type |
| 1 | GND | - | GND | - | GND | - |
| 2 | D3 | I/O | D3 | I/O | D3 | I/O |
| 3 | D4 | I/O | D4 | I/O | D4 | I/O |
| 4 | D5 | I/O | D5 | I/O | D5 | I/O |
| 5 | D6 | I/O | D6 | I/O | D6 | I/O |
| 6 | D7 | I/O | D7 | I/O | D7 | I/O |
| 7 | -CE1 | I | -CE1 | I | -CS0 | I |
| 8 | A10 | I | A10 | I | A10 ² | I |
| 9 | -OE | I | -OE | I | -ATA SEL | I |
| 10 | A9 | I | A9 | I | A9 ² | I |
| 11 | A8 | I | A8 | I | A8 ² | I |
| 12 | A7 | I | A7 | I | A7 ² | I |
| 13 | VCC | - | VCC | - | VCC | - |
| 14 | A6 | I | A6 | I | A6 ² | I |
| 15 | A5 | I | A5 | I | A5 ² | I |
| 16 | A4 | I | A4 | I | A4 ² | I |
| 17 | A3 | I | A3 | I | A3 ² | I |
| 18 | A2 | I | A2 | I | A2 | I |
| 19 | A1 | I | A1 | I | A1 | I |
| 20 | A0 | I | A0 | I | A0 | I |
| 21 | D0 | I/O | D0 | I/O | D0 | I/O |
| 22 | D1 | I/O | D1 | I/O | D1 | I/O |
| 23 | D2 | I/O | D2 | I/O | D2 | I/O |
| 24 | WP | O | -IOCS16 | O | -IOCS16 | O |
| 25 | -CD2 | O | -CD2 | O | -CD2 | O |
| 26 | -CD1 | O | -CD1 | O | -CD1 | O |
| 27 | D11 ¹ | I/O | D11 ¹ | I/O | D11 ¹ | I/O |
| 28 | D12 ¹ | I/O | D12 ¹ | I/O | D12 ¹ | I/O |
| 29 | D13 ¹ | I/O | D13 ¹ | I/O | D13 ¹ | I/O |
| 30 | D14 ¹ | I/O | D14 ¹ | I/O | D14 ¹ | I/O |
| 31 | D15 ¹ | I/O | D15 ¹ | I/O | D15 ¹ | I/O |
| 32 | -CE2 ¹ | I | -CE2 ¹ | I | -CS1 ¹ | I |
| 33 | -VS1 | O | -VS1 | O | -VS1 | O |
| 34 | -IORD | I | -IORD | I | -IORD ⁷ HSTROBE ⁸ -HDMARDY ⁹ | I |
| 35 | -IOWR | I | -IOWR | I | -IOWR ⁷ STOP ^{8,9} | I |
| 36 | -WE | I | -WE | I | -WE ³ | I |
| 37 | READY | O | -IREQ | O | INTRQ | O |
| 38 | VCC | - | VCC | - | VCC | - |
| 39 | -CSEL ⁵ | I | -CSEL ⁵ | I | -CSEL | I |
| 40 | -VS2 | O | -VS2 | O | -VS2 | O |
| 41 | RESET | I | RESET | I | -RESET | I |

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

Table 3-1: Pin assignments (2 of 2)

| Pin No. | Memory card mode | | I/O card mode | | True IDE mode | |
|---------|------------------|--------------|------------------|--------------|---|--------------|
| | Signal name | Pin I/O type | Signal name | Pin I/O type | Signal name | Pin I/O type |
| 42 | -WAIT | O | -WAIT | O | IORDY ⁷ -DDMARDY ⁸ DSTROBE ⁹ | O |
| 43 | -INPACK | O | -INPACK | O | DMARQ | O |
| 44 | -REG | I | -REG | I | -DMACK ⁶ | I |
| 45 | BVD2 | O | -SPKR | O | -DASP | I/O |
| 46 | BVD1 | O | -STSCHG | O | -PDIAG | I/O |
| 47 | D8 ¹ | I/O | D8 ¹ | I/O | D8 ¹ | I/O |
| 48 | D9 ¹ | I/O | D9 ¹ | I/O | D9 ¹ | I/O |
| 49 | D10 ¹ | I/O | D10 ¹ | I/O | D10 ¹ | I/O |
| 50 | GND | - | GND | - | GND | - |

Notes:

1. These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. The signals should be grounded by the host.
3. The signal should be tied to VCC by the host.
4. The mode is optional for CF+ cards, but required for CompactFlash storage cards
5. The -CSEL signal is ignored by the card in PC card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC card modes. In these modes, the pin should be connected by the host to PC card A25 or grounded by the host.
6. If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition.
7. Signal usage in True IDE mode except when Ultra DMA mode protocol is active
8. Signal usage in True IDE mode when Ultra DMA mode protocol DMA write is active
9. Signal usage in True IDE mode when Ultra DMA mode protocol DMA read is active.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

4. Product Specifications

4.1 Capacity

Capacity specification of the Compact Flash Card series (CFC) is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1: Capacity specifications

| Capacity | Total bytes ^{1,2} | Cylinders | Heads | Sectors | Max LBA |
|----------|----------------------------|---------------------|-------|---------|------------|
| 128 MB | 128,450,560 | 980 | 8 | 32 | 250,880 |
| 256 MB | 256,901,120 | 980 | 16 | 32 | 501,760 |
| 512 MB | 512,483,328 | 993 | 16 | 63 | 1,000,944 |
| 1GB | 1,024,966,656 | 1,986 | 16 | 63 | 2,001,888 |
| 2GB | 2,048,901,120 | 3,970 | 16 | 63 | 4,001,760 |
| 4GB | 4,110,188,544 | 7,964 | 16 | 63 | 8,027,712 |
| 8GB | 8,195,604,480 | 15,880 | 16 | 63 | 16,007,040 |
| 16GB | 16,391,208,960 | 16,383 ³ | 16 | 63 | 32,014,080 |

Notes:

Display of total bytes varies from operating systems.

Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance Specification

Performances of the CF cards are listed in Table 4-2

Table 4-2: Performance specifications

| Capacity \ Performance | 128 MB | 256 MB | 512 MB | 1 GB | 2 GB | 4 GB | 8 GB | 16 GB |
|------------------------|--------|--------|--------|------|------|------|------|-------|
| Sustained read (MB/s) | 17 | 29 | 19 | 21 | 20 | 21 | 21 | 20 |
| Sustained write (MB/s) | 4 | 8 | 7 | 12 | 11 | 11 | 13 | 15 |

Notes: performance may vary depending on flash configurations or host system settings.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

4.3 Environmental Specifications

Environmental specification of the Compact Flash Card series (CFC) follows the MIL-STD-810F standards as shown in Table 4-3.

Table 4-3: Environmental specifications

| Environment | | Specification |
|---------------------------|-----------|---|
| Temperature | Operation | 0°C to 70°C; -40°C to 85°C (Extended Temperature) |
| | Storage | -40°C to 100°C |
| Humidity | | 5% to 95% RH (Non-condensing) |
| Vibration (Non-Operation) | | Sine wave : 10~2000Hz, 15G (X, Y, Z axes) |
| Shock (Non-Operation) | | Half sine wave 1,500G (X, Y, Z ; All 6 axes) |

4.4 Certification & Compliance

The CompactFlash card complies with the following global standards:

- CE
- FCC
- RoHS

4.5 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

| Capacity | TeraBytes Written |
|----------|-------------------|
| 128 MB | 3.3 |
| 256 MB | 6.7 |
| 512 MB | 12.9 |
| 1 GB | 25.6 |
| 2 GB | 38.4 |
| 4 GB | 51.9 |
| 8 GB | 69.8 |
| 16 GB | 115.0 |

Notes:

- The measurement assumes the data written to the SSD for test is under a typical and constant rate.
- The measurement follows the standard metric: 1 TB (Terabyte) = 1000 GB.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

5. Flash Management

5.1. Advanced wear-leveling algorithms

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Wear leveling is an important mechanism that level out the wearing of blocks so that the wearing-down of blocks can be almost evenly distributed. This will increase the lifespan of SSDs. Commonly used wear leveling types are Static and Dynamic.

5.2 S.M.A.R.T. technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

5.3 Built-in hardware ECC

The ATA-Disk Module uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data. High performance is fulfilled through hardware-based error detection and correction.

5.4 Flash block management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.5 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

6. Software Interface

6.1 Command Set

Table 6-1 summarizes the command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 6-1: Command set

| Command | Code | FR ¹ | SC ² | SN ³ | CY ⁴ | DH ⁵ | LBA ⁶ |
|------------------------------|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| Check-Power-Mode | E5h or 98h | - | - | - | - | D ⁸ | - |
| Execute-Drive-Diagnostic | 90h | - | - | - | - | D | - |
| Erase Sector(s) | C0h | - | Y | Y | Y | Y | Y |
| Flush-Cache | E7h | - | - | - | - | D | - |
| Format Track | 50h | - | Y ⁷ | - | Y | Y ⁸ | Y |
| Identify-Drive | ECh | - | - | - | - | D | - |
| Idle | E3h or 97h | - | Y | - | - | D | - |
| Idle-Immediate | E1h or 95h | - | - | - | - | D | - |
| Initialize-Drive-Parameters | 91h | - | Y | - | - | Y | - |
| NOP | 00h | - | - | - | - | D | - |
| Read-Buffer | E4h | - | - | - | - | D | - |
| Read-DMA | C8h or C9h | - | Y | Y | Y | Y | Y |
| Read-Multiple | C4h | - | Y | Y | Y | Y | Y |
| Read-Sector(s) | 20h or 21h | - | Y | Y | Y | Y | Y |
| Read-Verify-Sector(s) | 40h or 41h | - | Y | Y | Y | Y | Y |
| Recalibrate | 1Xh | - | - | - | - | D | - |
| Request-Sense | 03h | - | - | - | - | D | - |
| Seek | 7Xh | - | - | Y | Y | Y | Y |
| Set-Features | EFh | Y ⁷ | - | - | - | D | - |
| SMART | B0h | Y | Y | Y | Y | D | - |
| Set-Multiple-Mode | C6h | - | Y | - | - | D | - |
| Set-Sleep-Mode | E6h or 99h | - | - | - | - | D | - |
| Standby | E2h or 96h | - | - | - | - | D | - |
| Standby-Immediate | E0h or 94h | - | - | - | - | D | - |
| Translate-Sector | 87h | - | Y | Y | Y | Y | Y |
| Write-Buffer | E8h | - | - | - | - | D | - |
| Write-DMA | CAh or CBh | - | Y | Y | Y | Y | Y |
| Write-Multiple | C5h | - | Y | Y | Y | Y | Y |
| Write-Multiple-Without-Erase | CDh | - | Y | Y | Y | Y | Y |

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

| | | | | | | | |
|----------------------------|------------|---|---|---|---|---|---|
| Write-Sector(s) | 30h or 31h | - | Y | Y | Y | Y | Y |
| Write-Sector-Without-Erase | 38h | - | Y | Y | Y | Y | Y |
| Write-Verify | 3Ch | - | Y | Y | Y | Y | Y |

1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder registers
5. DH - Drive/Head register
6. LBA - Logical Block Address mode supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command
8. For the Drive/Head register:
 - Y means both the CFC and Head parameters are used
 - D means only the CFC parameter is valid and not the Head parameter

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7. Electrical Specification

Caution: Absolute Maximum Stress Ratings – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 7-1: Operating range

| | |
|---------------------------------------|--------------------------|
| Standard Operating Temperature | 0 °C to +70 °C |
| Extended Operating Temperature | -40 °C to +85 °C |
| Supply voltage | 5V ± 5% (4.75-5.25V) |
| | 3.3V ± 5% (3.135-3.465V) |

Table 7-2: Absolute maximum power pin stress ratings

| Parameter | Symbol | Conditions |
|---|-----------------|---|
| Input Power | V _{DD} | -0.3V min. to 6.5V max. |
| Voltage on any pin except V _{DD} with respect to GND | V | -0.5V min. to V _{DD} + 0.5V max. |

Table 7-3: Recommended system power-up timing

| Symbol | Parameter | Typical | Maximum | Units |
|------------------------------------|-----------------------------|---------|---------|-------|
| T _{PU-READY} ¹ | Power-up to Ready Operation | 200 | 1000 | ms |
| T _{PU-WRITE} ¹ | Power-up to Write Operation | 200 | 1000 | ms |

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.1 DC Characteristics

Table 7-4: DC Characteristics

| Symbol | Type | Parameter | Min | Max | Units | Conditions |
|------------------------|------------------------------|---|------|------|-----------------------------------|--|
| V_{IH1} V_{IL1} | I1 | Input Voltage | 2.0V | 0.8V | V | $V_{DDQ}=V_{DDQ} \text{ Max}$ $V_{DDQ}=V_{DDQ} \text{ Min}$ |
| I_{IL1} | I1Z | Input Leakage Current | -10 | 10 | μA | $V_{IN}=\text{GND to } V_{DDQ}$ $V_{DDQ}=V_{DDQ} \text{ Max}$ |
| I_{U1} | I1U | Input Pull-Up Current | -110 | -1 | μA | $V_{OUT}=\text{GND,}$ $V_{DDQ}=V_{DDQ} \text{ Max}$ |
| V_{T+2} V_{T-2} | I2 | Input Voltage Schmitt Trigger | 0.8 | 2.0 | V | $V_{DDQ}=V_{DDQ} \text{ Max}$ $V_{DDQ}=V_{DDQ} \text{ Min}$ |
| I_{IL2} | I2Z | Input Leakage Current | -10 | 10 | μA | $V_{IN}=\text{GND to } V_{DDQ}$ $V_{DDQ}=V_{DDQ} \text{ Max}$ |
| I_{U2} | I2U | Input Pull-Up Current | -110 | -1 | μA | $V_{OUT}=\text{GND,}$ $V_{DDQ}=V_{DDQ} \text{ Max}$ |
| V_{OH1} V_{OL1} | O1 | Output Voltage | 2.4 | 0.4 | V | $I_{OH1}=I_{OH1} \text{ Min}$ $I_{OL1}=I_{OL1} \text{ Max}$ |
| I_{OH1} | | Output Current | -4 | | mA | $V_{DDQ}=V_{DDQ} \text{ Min}$ |
| I_{OL1} | | Output Current | | 4 | mA | $V_{DDQ}=V_{DDQ} \text{ Min}$ |
| V_{OH2} V_{OL2} | O2 | Output Voltage | 2.4 | 0.4 | V | $I_{OH2}=I_{OH2} \text{ Min}$ $I_{OL2}=I_{OL2} \text{ Max}$ |
| I_{OH2} | | Output Current | -6 | | mA | $V_{DDQ}=3.135\text{V}-3.465\text{V}$ |
| I_{OL2} | | Output Current | | 6 | mA | $V_{DDQ}=3.135\text{V}-3.465\text{V}$ |
| I_{OH2} | | Output Current | -8 | | mA | $V_{DDQ}=4.5\text{V}-5.5\text{V}$ |
| I_{OL2} | Output Current | | 8 | mA | $V_{DDQ}=4.5\text{V}-5.5\text{V}$ | |
| V_{OH6} V_{OL6} | O6 | Output Voltage for DASP# pin | 2.4 | 0.4 | V | $I_{OH6}=I_{OH6} \text{ Min}$ $I_{OL6}=I_{OL6} \text{ Max}$ |
| I_{OH6} | | Output Current for DASP# pin | -3 | | mA | $V_{DDQ}=3.135\text{V}-3.465\text{V}$ |
| I_{OL6} | | Output Current for DASP# pin | | 8 | mA | $V_{DDQ}=3.135\text{V}-3.465\text{V}$ |
| I_{OH6} | | Output Current for DASP# pin | -3 | | mA | $V_{DDQ}=4.5\text{V}-5.5\text{V}$ |
| I_{OL6} | Output Current for DASP# pin | | 12 | mA | $V_{DDQ}=4.5\text{V}-5.5\text{V}$ | |
| $I_{DD}^{1,2}$ | PWR | Power supply current ($T_a = 0^\circ\text{C to } +70^\circ\text{C}$) | | 50 | mA | $V_{DD}=V_{DD} \text{ Max}$ $V_{DDQ}=V_{DDQ} \text{ Max}$ |
| $I_{DD}^{1,2}$ | PWR | Power supply current ($T_a = -40^\circ\text{C to } +85^\circ\text{C}$) | | 100 | mA | $V_{DD}=V_{DD} \text{ Max}$ $V_{DDQ}=V_{DDQ} \text{ Max}$ |
| I_{SP} | PWR | Sleep/Standby/Idle current ($T_a = 0^\circ\text{C to } +70^\circ\text{C}$) | | 100 | μA | $V_{DD}=V_{DD} \text{ Max}$ $V_{DDQ}=V_{DDQ} \text{ Max}$ |
| I_{SP} | PWR | Sleep/Standby/Idle current ($T_a = -40^\circ\text{C to } +85^\circ\text{C}$) | | 200 | μA | $V_{DD}=V_{DD} \text{ Max}$ $V_{DDQ}=V_{DDQ} \text{ Max}$ |

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.2 AC Characteristics

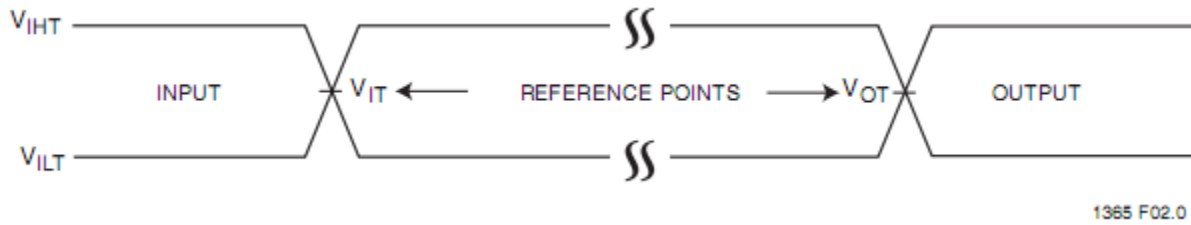


Figure 7-1: AC Input/Output Reference Waveforms

AC test inputs are driven at V_{IHT} (0.9 VDD) for a logic "1" and V_{ILT} (0.1 VDD) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 VDD) and V_{OT} (0.5 VDD). Input rise and fall times (10% \leftrightarrow 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
 V_{OT} - V_{OUTPUT} Test
 V_{IHT} - $V_{INPUT HIGH}$ Test
 V_{ILT} - $V_{INPUT LOW}$ Test

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

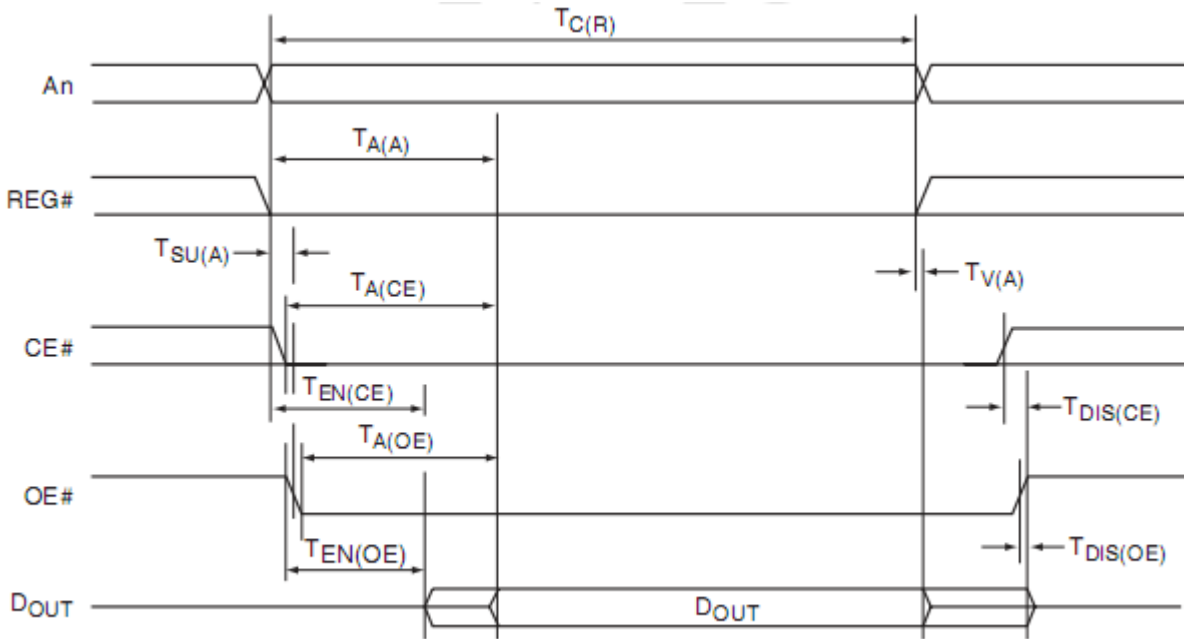
7.2.1 Attribute Memory Read Timing Specification

The Attribute Memory access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

Table 7-5 Attribute Memory Read Timing Specification

| Speed Version | Item | Symbol | IEEE Symbol | 100 ns | | |
|---------------|--------------------------------|---------------|-------------|------------------|------------------|-------|
| | | | | Min ¹ | Min ¹ | Units |
| | Read Cycle Time | $T_{C(R)}$ | tAVAV | 100 | | ns |
| | Address Access Time | $T_{A(A)}$ | tAVQV | | 100 | ns |
| | Card Enable Access Time | $T_{A(CE)}$ | tELQV | | 100 | ns |
| | Output Enable Access Time | $T_{A(OE)}$ | tGLQV | | 50 | ns |
| | Output Disable Time from CE# | $T_{DIS(CE)}$ | tEHQZ | | 50 | ns |
| | Output Disable Time from OE# | $T_{DIS(OE)}$ | tGHQZ | | 50 | ns |
| | Address Setup Time | $T_{SU(A)}$ | tAVGL | 10 | | ns |
| | Output Enable Time from CE# | $T_{EN(CE)}$ | tELQNZ | 5 | | ns |
| | Output Enable Time from OE# | $T_{EN(OE)}$ | tGLQNZ | 5 | | ns |
| | Data Valid from Address Change | $T_{V(A)}$ | tAXQZ | 0 | | ns |

1. D_{OUT} signifies data provided by the Compact Flash card to the system. The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations. All AC specifications are guaranteed by design.



1365 F03.0

Figure 7-2: Attribute Memory Read Timing Diagram

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.2.2 Configuration Register (Attribute Memory) Write Specification

The card configuration write access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

Table 7-6 Configuration Register (Attribute Memory) Write Timing

| Speed Version | 100 ns | | | | |
|------------------------|------------------|-------------|------------------|------------------|-------|
| Item | Symbol | IEEE Symbol | Min ¹ | Min ¹ | Units |
| Write Cycle Time | $T_{C(W)}$ | tAVAV | 100 | | ns |
| Write Pulse Width | $T_{W(WE)}$ | tWLWH | 60 | | ns |
| Address Setup Time | $T_{SU(A)}$ | tAVWL | 10 | | ns |
| Write Recover Time | $T_{REC(WE)}$ | tWMAX | 15 | | ns |
| Data Setup Time for WE | $T_{SU(DWE\#H)}$ | tDVWH | 40 | | ns |
| Data Hold Time | $T_{H(D)}$ | tWMDX | 15 | | ns |

1. D_{IN} signifies data provided by the system to the Compact Flash card. All AC specifications are guaranteed by design.

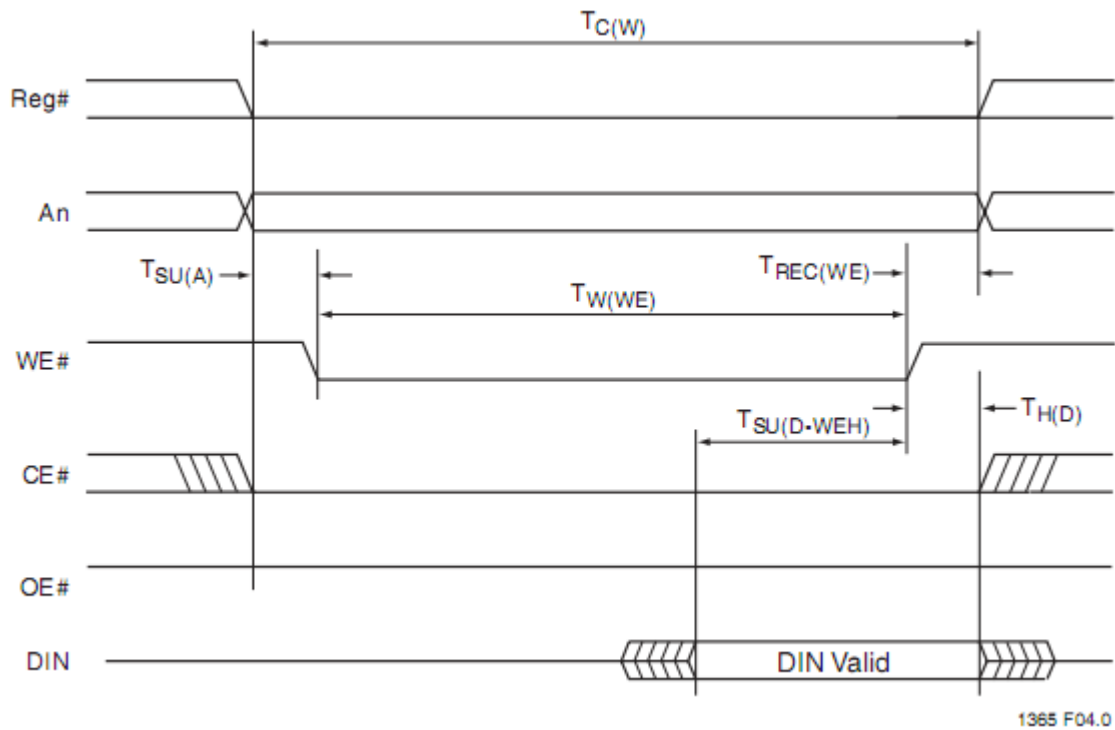


Figure 7-3: Configuration Register (Attribute Memory) Write Timing Diagram

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.2.3 Common Memory Read Timing Specification

Table 7-7 Common Memory Read Timing

| Item | Symbol | IEEE Symbol | Min ¹ | Min ¹ | Units |
|-----------------------------|---------------|-------------|------------------|------------------|-------|
| Output Enable Access Time | $T_{A(OE)}$ | tGLQV | | 50 | ns |
| Output Disable Time from OE | $T_{DIS(OE)}$ | tGHQZ | | 50 | ns |
| Address Setup Time | $T_{SU(A)}$ | tAVGL | 10 | | ns |
| Address Hold Time | $T_{REC(WE)}$ | tGHAX | 15 | | ns |
| CE Setup before OE | $T_{SU(CE)}$ | tELGL | 0 | | ns |
| CE Hold following OE | $T_{H(CE)}$ | tGHEH | 15 | | ns |

1. All AC specifications are guaranteed by design.

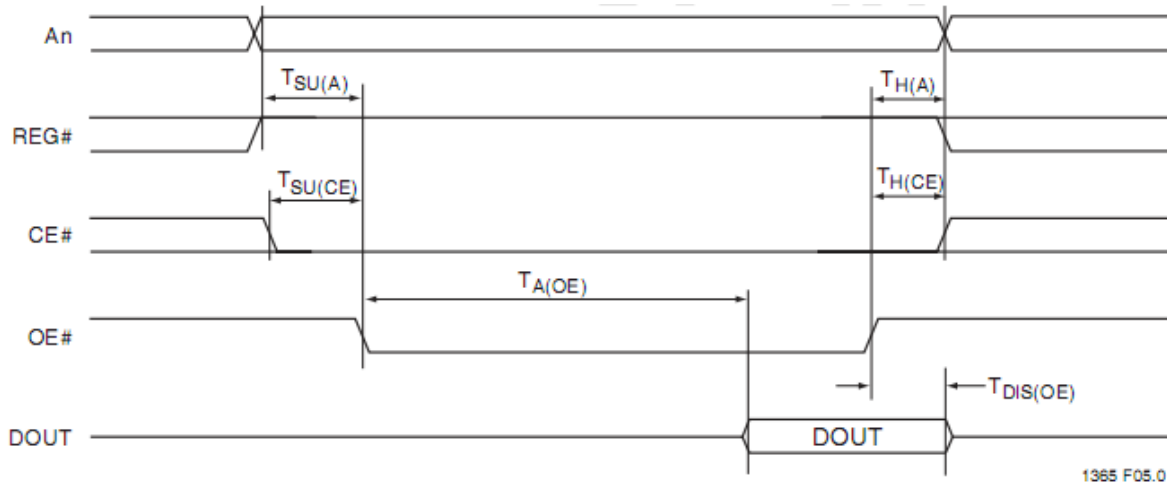


Figure 7-4: Common Memory Read Timing Diagram

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.2.4 Common Memory Write Timing Specification

Table 7-8 Common Memory Write Timing

| Item | Symbol | IEEE Symbol | Min ¹ | Min ¹ | Units |
|------------------------|------------------|-------------|------------------|------------------|-------|
| Data Setup before WE | $T_{SU(DWE\#H)}$ | tDVWH | 40 | | ns |
| Data Hold following WE | $T_{H(D)}$ | tWMDX | 15 | | ns |
| WE Pulse Width | $T_{W(WE)}$ | tWLWH | 60 | | ns |
| Address Setup Time | $T_{SU(A)}$ | tAVWL | 10 | | ns |
| CE Setup before WE | $T_{SU(CE)}$ | tELWL | 0 | | ns |
| Write Recovery Time | $T_{REC(WE)}$ | tWMAX | 15 | | ns |
| Address Hold Time | $T_{H(A)}$ | tGHAX | 15 | | ns |
| CE Hold following WE | $T_{H(CE)}$ | tGHEH | 15 | | ns |

1. All AC specifications are guaranteed by design.

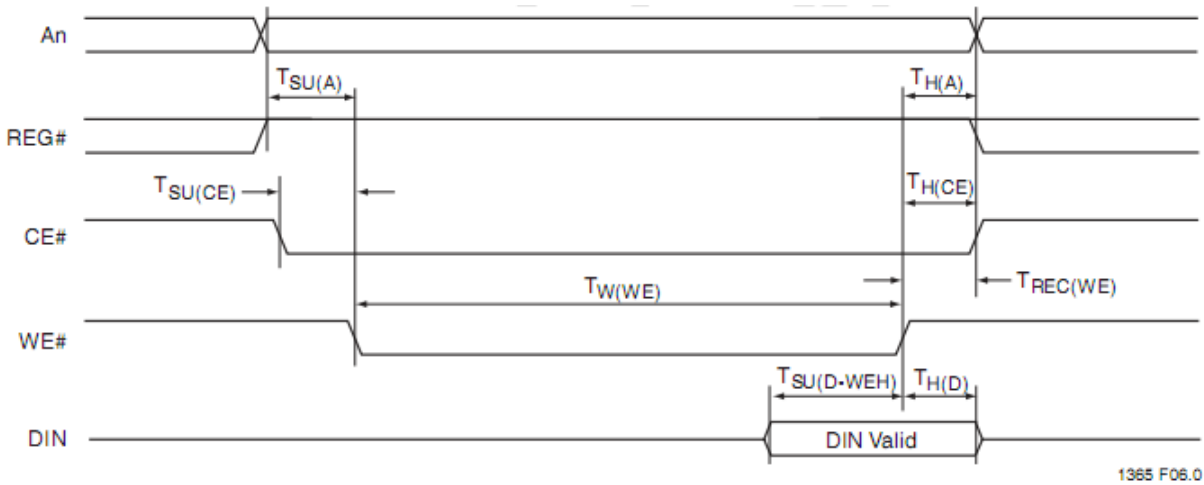


Figure 7-5: Common Memory Write Timing Diagram

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.2.5 I/O Input (Read) Timing Specification

Table 7-9 I/O Read Timing

| Item | Symbol | IEEE Symbol | Min ¹ | Min ¹ | Units |
|-----------------------------------|----------------------|-------------|------------------|------------------|-------|
| Data Delay after IORD | $T_{D(IORD)}$ | tIGLQV | | 100 | ns |
| Data Hold following IORD | $T_{H(IORD)}$ | tIGHQX | 0 | | ns |
| IORD Width Time | $T_{W(IORD)}$ | tIGLIGH | 165 | | ns |
| Address Setup before IORD | $T_{SUA(IORD)}$ | tAVIGL | 70 | | ns |
| Address Hold following IORD | $T_{HA(IORD)}$ | tIGHAX | 20 | | ns |
| CE Setup before IORD | $T_{SUCE(IORD)}$ | tELIGL | 5 | | ns |
| CE Hold following IORD | $T_{HCE(IORD)}$ | tIGHEH | 20 | | ns |
| REG Setup before IORD | $T_{SUREG(IORD)}$ | tRGLIGL | 5 | | ns |
| REG Hold following IORD | $T_{HREG(IORD)}$ | tIGHRGH | 0 | | ns |
| INPACK Delay Falling from IORD | $T_{DFINPACK(IORD)}$ | tIGLIAL | 0 | 45 | ns |
| INPACK Delay Rising from IORD | $T_{DRINPACK(IORD)}$ | tIGHIAH | | 45 | ns |
| IOIS16 Delay Falling from Address | $T_{DFIOIS16(ADR)}$ | tAVISL | | 35 | ns |
| IOIS16 Delay Rising from Address | $T_{DRIOIS16(ADR)}$ | tAVISH | | 35 | ns |

1. All AC specifications are guaranteed by design.

Note: The maximum load on -INPACK and IOIS16# is 1 LSTTL with 50pF total load.

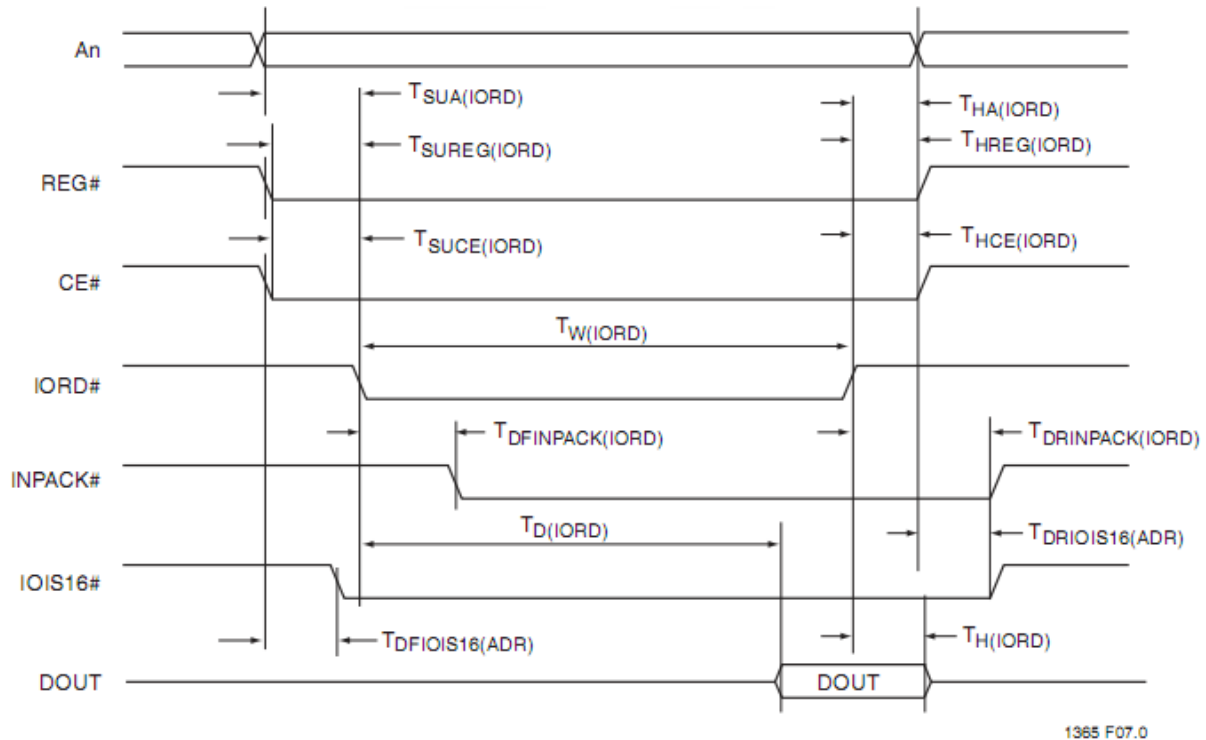


Figure 7-6: I/O Read Timing Diagram

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.2.6 I/O Output (Write) Timing Specification

Table 7-10 I/O Write Timing

| Item | Symbol | IEEE Symbol | Min ¹ | Min ¹ | Units |
|-----------------------------------|---------------------|-------------|------------------|------------------|-------|
| Data Setup before IOWR | $T_{SU(IOWR)}$ | tDVIWH | 60 | | ns |
| Data Hold following IOWR | $T_{H(IOWR)}$ | tIWHDX | 30 | | ns |
| IOWR Width Time | $T_{W(IOWR)}$ | tWLIWH | 165 | | ns |
| Address Setup before IOWR | $T_{SUA(IOWR)}$ | tAVIWL | 70 | | ns |
| Address Hold following IOWR | $T_{HA(IOWR)}$ | tIWHAX | 20 | | ns |
| CE Setup before IOWR | $T_{SUCE(IOWR)}$ | tELIWL | 5 | | ns |
| CE Hold following IOWR | $T_{HCE(IOWR)}$ | tIWHEH | 20 | | ns |
| REG Setup before IOWR | $T_{SUREG(IOWR)}$ | tRGLIWL | 5 | | ns |
| REG Hold following IOWR | $T_{HREG(IOWR)}$ | tIWHRGH | 0 | | ns |
| IOIS16 Delay Falling from Address | $T_{DFIOIS16(ARD)}$ | tAVISL | | 35 | ns |
| IOIS16 Delay Rising from Address | $T_{DRIOIS16(ADR)}$ | tAVISH | | 35 | ns |

1. All AC specifications are guaranteed by design.

Note: The maximum load on $-\text{INPACK}$ and IOIS16# is 1 LSTTL with 50pF total load.

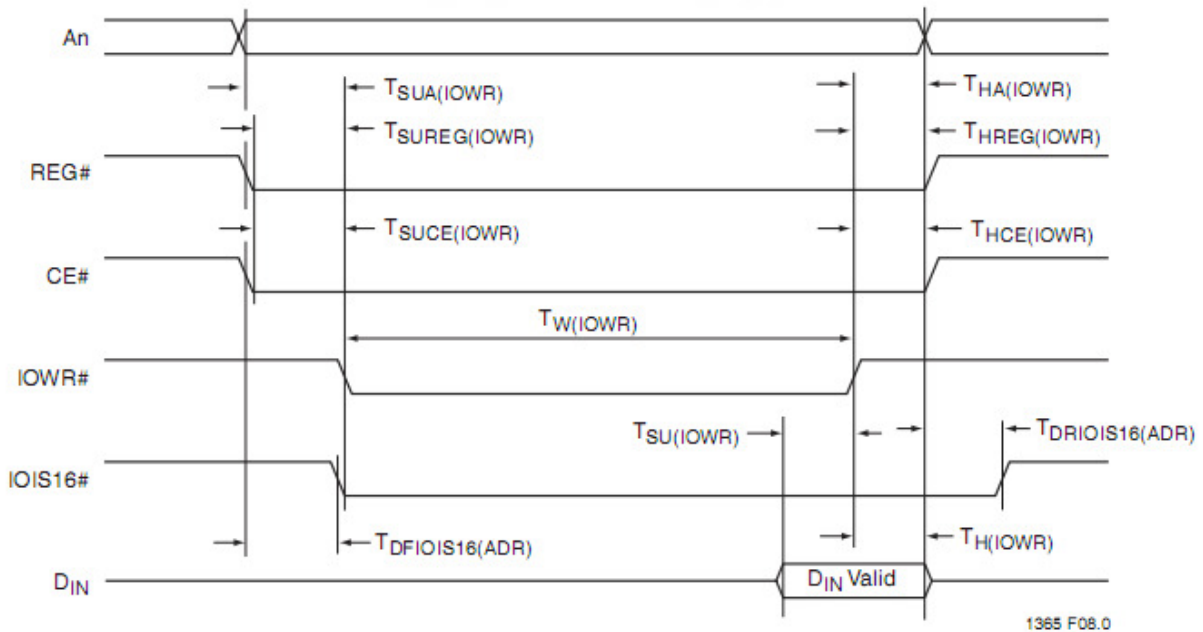


Figure 7-7: I/O Write Timing Diagram

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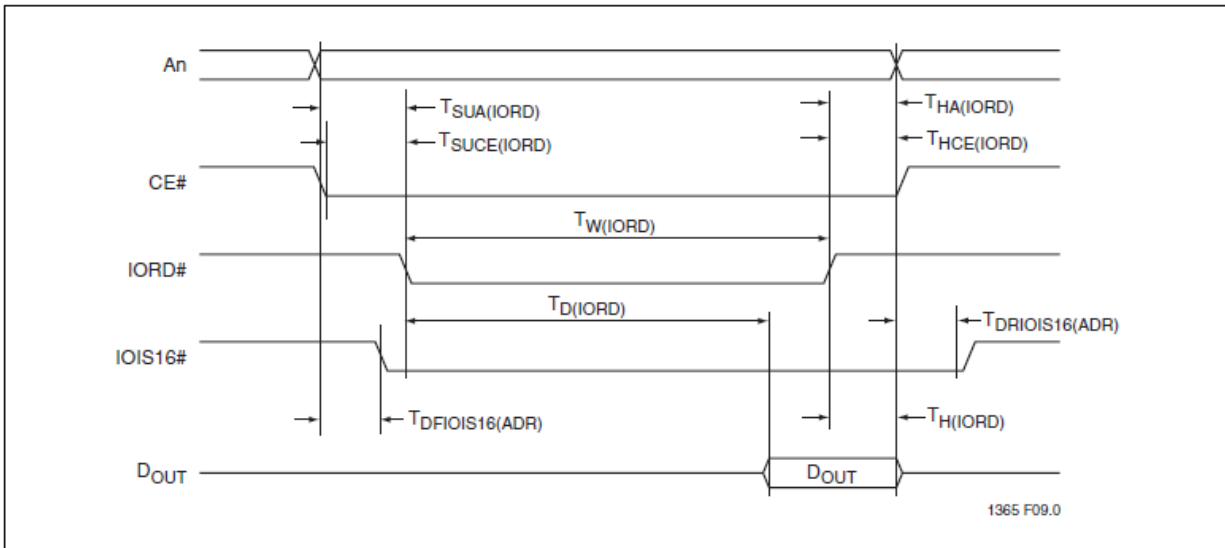
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7.2.7 True IDE I/O Read Timing

| Item | Symbol | IEEE Symbol | Min | Max | Units |
|-----------------------------------|---------------------|-------------|-----|-----|-------|
| Data Delay after IORD | $T_{D(IORD)}$ | tIGLQV | | 50 | ns |
| Data Hold following IORD | $T_{H(IORD)}$ | tIGHQX | 5 | | ns |
| IORD Width Time | $T_{W(IORD)}$ | tIGLIGH | 70 | | ns |
| Address Setup before IORD | $T_{SUA(IORD)}$ | tAVIGL | 25 | | ns |
| Address Hold following IORD | $T_{HA(IORD)}$ | tIGHAX | 10 | | ns |
| CE Setup before IORD | $T_{SUCE(IORD)}$ | tELIGL | 10 | | ns |
| CE Hold following IORD | $T_{HCE(IORD)}$ | tIGHEH | 5 | | ns |
| IOIS16 Delay Falling from Address | $T_{DFIOIS16(ADR)}$ | tAVISL | | 20 | ns |
| IOIS16 Delay Rising from Address | $T_{DRIOIS16(ADR)}$ | tAVISH | | 20 | ns |

Note: The maximum load on IOIS16# is 1 LSTTL with 50pF total load.

All AC specifications are guaranteed by design.



Compact Flash III series

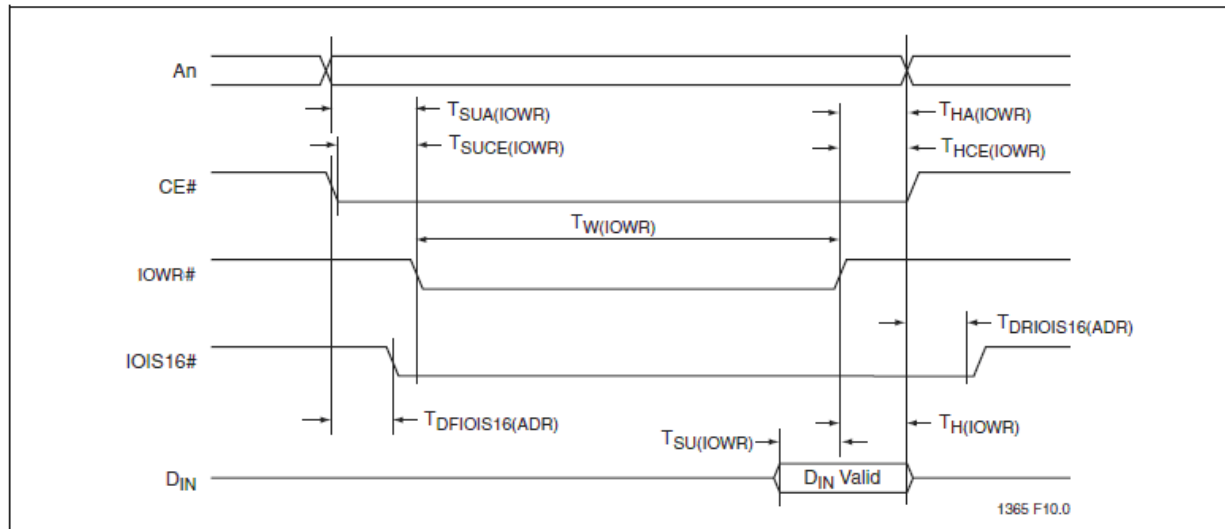
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7.2.8 True IDE I/O Write Timing

| Item | Symbol | IEEE Symbol | Min | Max | Units |
|-----------------------------------|---------------------|-------------|-----|-----|-------|
| Data Setup before IOWR | $T_{SU(IOWR)}$ | tDVIWH | 20 | | ns |
| Data Hold following IOWR | $T_{H(IOWR)}$ | tIWHDX | 10 | | ns |
| IOWR Width Time | $T_{W(IOWR)}$ | tIWLWH | 70 | | ns |
| Address Setup before IOWR | $T_{SUA(IOWR)}$ | tAVIWL | 25 | | ns |
| Address Hold following IOWR | $T_{HA(IOWR)}$ | tIWHAX | 10 | | ns |
| CE Setup before IOWR | $T_{SUCE(IOWR)}$ | tELIWL | 10 | | ns |
| CE Hold following IOWR | $T_{HCE(IOWR)}$ | tIWHHEH | 5 | | ns |
| IOIS16 Delay Falling from Address | $T_{DFIOIS16(ADR)}$ | tAVISL | | 20 | ns |
| IOIS16 Delay Rising from Address | $T_{DRIOIS16(ADR)}$ | tAVISH | | 20 | ns |

Note: The maximum load on IOIS16# is 1 LSTTL with 50pF total load.

All AC specifications are guaranteed by design.



Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.2.9 Ultra DMA Mode Data Transfer Input/Output (Read/Write) Timing

Table 7-11 Ultra DMA Data Burst Timing Specifications¹

| Name | Descriptions | Mode 4 | | Unit | Measurement Location ² |
|----------------------|--|--------|-----|------|-----------------------------------|
| | | Min | Max | | |
| T _{2CYCTYP} | Typical sustained average two cycle time | 60 | | ns | Sender |
| T _{CYC} | Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge) | 25 | | ns | Note ³ |
| T _{2CYC} | Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE) | 57 | | ns | Sender |
| T _{DS} | Data setup time at recipient (from data valid until STROBE edge) ^{4,5} | 5.0 | | ns | Recipient |
| T _{DH} | Data hold time at Recipient (from STROBE edge until data becomes invalid) ^{1,2} | 5.0 | | ns | Recipient |
| T _{DVS} | Data valid setup time for Sender (from data valid until STROBE edge) ⁶ | 6.0 | | ns | Sender |
| T _{DVH} | Data valid hold time at Sender (from STROBE edge until data becomes invalid) ³ | 6.0 | | ns | Sender |
| T _{CS} | CRC word setup time at device ¹ | 5.0 | | ns | Device |
| T _{CH} | CRC word hold time at device ¹ | 5.0 | | ns | Device |
| T _{CVS} | CRC word valid setup time at host (from CRC valid until DMACK negation) ³ | 6.7 | | ns | Host |
| T _{CVH} | CRC word valid hold time at Sender (from DMACK negation until CRC becomes invalid) ³ | 6.2 | | ns | Host |
| T _{ZFS} | Time from STROBE output released-to-driving until the first transition of critical timing | 0 | | ns | Device |
| T _{DZFS} | Time from data output released-to-driving until the first transition of critical timing | 6.7 | | ns | Sender |
| T _{FS} | First STROBE time (for device to first negate DSTROBE from STOP during a data in burst) | | 120 | ns | Device |
| T _{LJ} | Limited interlock time ⁷ | 0 | 100 | ns | Note ⁸ |
| T _{MLI} | Interlock time with minimum ⁴ | 20 | | ns | Host |
| T _{UI} | Unlimited interlock time ⁴ | 0 | | ns | Host |
| T _{AZ} | Maximum time allowed for output drivers to release (from asserted to negated) | | 10 | ns | Note ⁹ |
| T _{ZAH} | Minimum delay time required for output | 20 | | ns | Host |
| T _{ZAD} | Drivers to assert or negate (from released) | 0 | | ns | Device |
| T _{ENV} | Envelope time (from DMACK# to STOP and HDMARDY# during data in burst initiation and from DMACK to STOP during data our burst initiation) | 20 | 55 | ns | Host |
| T _{RFS} | Ready-to-final STROBE time (no STROBE edge are sent this long after negation of DMARDY) | | 60 | ns | Sender |
| T _{RP} | Ready-to-pause time (Recipient waits to pause until after negating DMARDY) | 100 | | ns | Recipient |
| T _{IORDYZ} | Maximum time before releasing IORDY | | 20 | ns | Device |
| T _{ZIORDY} | Minimum time before driving IORDY ¹⁰ | 0 | | ns | Device |
| T _{ACK} | | 20 | | ns | Host |
| T _{SS} | | 50 | | ns | Sender |

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

1. All timing measurement switching points (low-to-high and high-to-low) are taken at 1.5V.
2. All signal transitions for a timing parameter are measured at the connector specified in the measurement location column. For example, in the case of TRFS, both STROBE and DMARDY Transitions are measured at the Sender connector.
3. The parameter TCYC is measured at the recipient's connector farthest from the Sender.
4. 80-Conductor cabling is required in order to meet setup (TDS, TCS) and hold (TDH, TCH) times in modes greater than two.
5. The parameters TDS and TDH for Mode 5 are defined for a Recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for TDS and TDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.
6. Timing for TDVS, TDVH, TCVS, and TCVH are met for lumped capacitive loads of 15 and 50 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
7. The parameters TUI, TMLI, and TLI indicate Sender-to-Recipient or Recipient-to-Recipient interlocks. For example, one agent (either Sender or Recipient) is waiting for the other agent to respond with a signal before proceeding; TUI is an unlimited interlock that has no maximum time value, TMLI is a limited time-out that has a defined minimum, and TLI is a limited time-out that has a defined maximum.
8. The parameter TLI is measured at the connector of the Sender or Recipient that is responding to an incoming transition from the Recipient or Sender respectively. Both the incoming signal and the outgoing response are measured at the same connector.
9. The parameter TAZ is measured at the connector of the Sender or Recipient that is driving the bus but must release the bus that allow for a bus turnaround.
10. For all modes the parameter TZIORDY may be greater than TENV because the host has a pull-on IORDY giving it a known state when released.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

Table 7-12 Ultra DMA Sender and Recipient IC Timing Specifications¹

| Name | Descriptions | Mode 4 | | Unit |
|-------------|--|--------|-----|------|
| | | Min | Max | |
| T_{DSIC} | Recipient IC data setup time (from data valid until STROBE edge) ² | 4.8 | | ns |
| T_{DHIC} | Recipient IC data hold time (from STROBE edge until data becomes invalid) ¹ | 4.8 | | ns |
| T_{DVSIC} | Sender IC data valid setup time (from data valid until STROBE edge) ³ | 9.5 | | ns |
| T_{DVHIC} | | 9.0 | | ns |

1. All timing measurement switching point (low-to-high and high-to-low)
2. The correct data value is captured by the Recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at T_{DSIC} and T_{DHIC} timing (as measured through 1.5 V).
3. The parameters T_{DVSIC} and T_{DVHIC} are met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

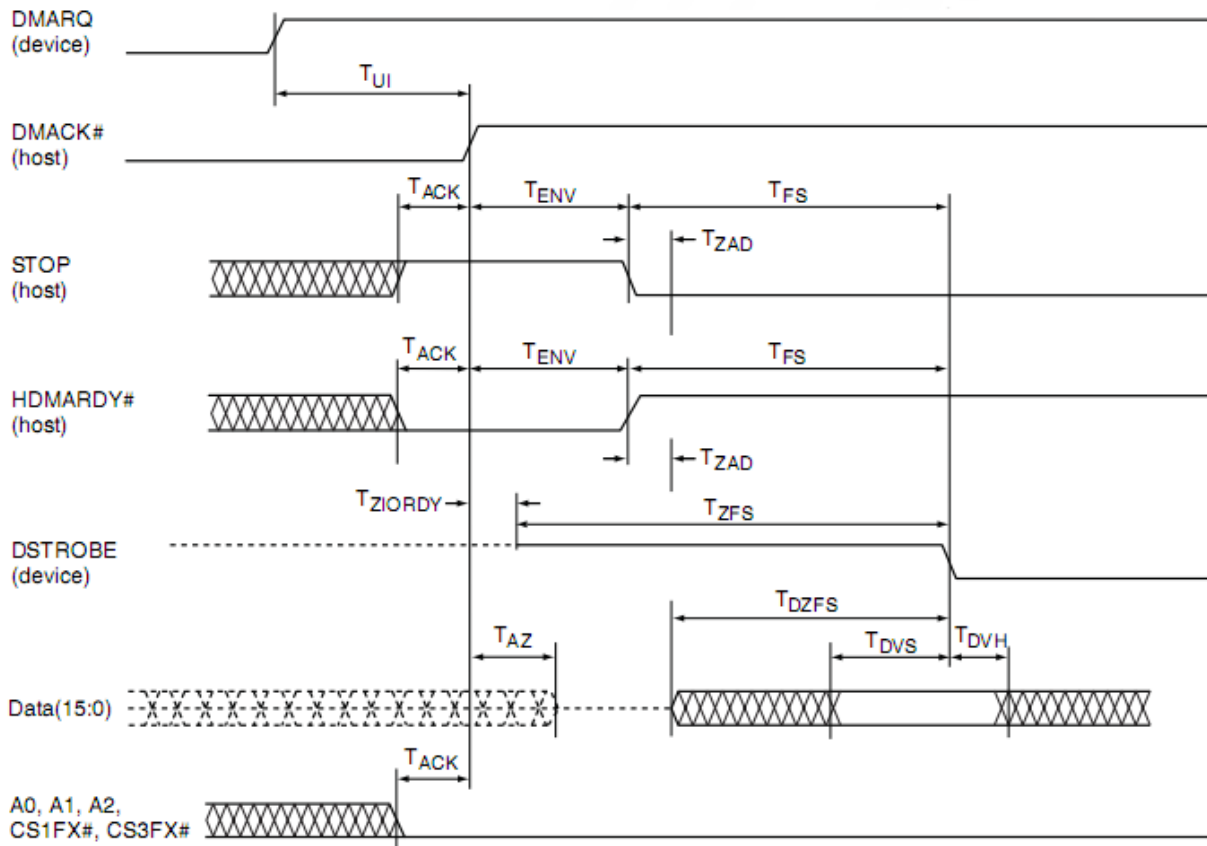


Figure 7-8: Initiating an Ultra DMA Data-In Burst

Notes:

1. The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDRARDY-: DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

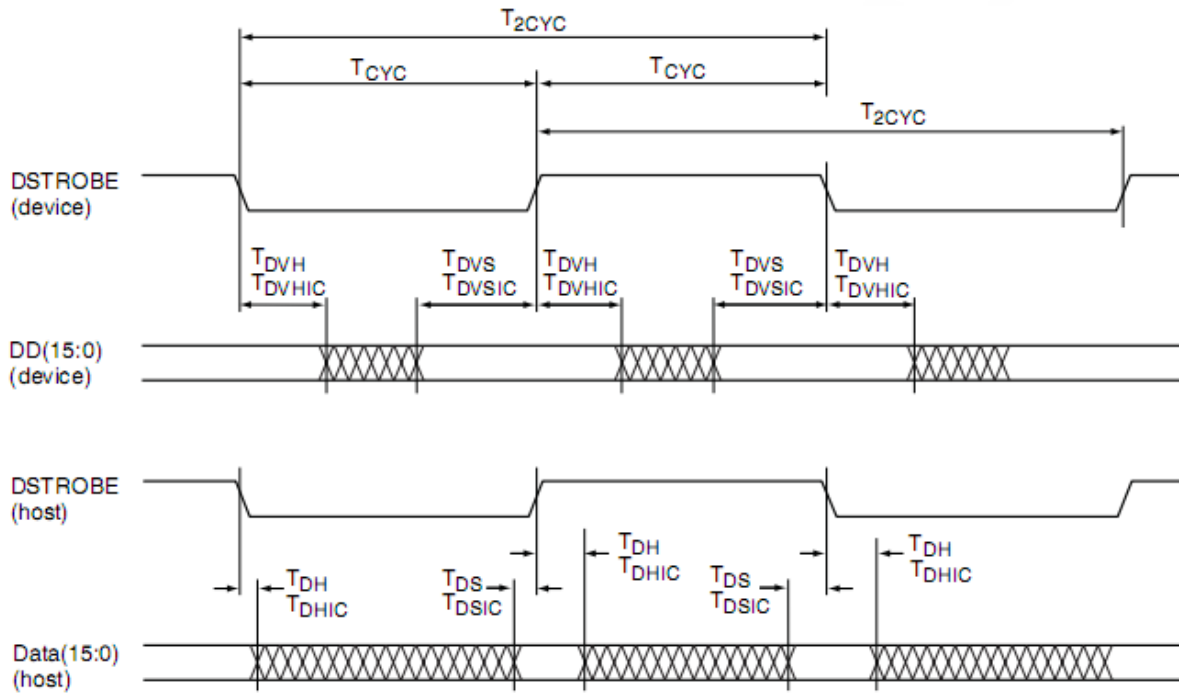


Figure 7-9: Sustained Ultra DMA Data-In Burst

Notes:

1. DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay will not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

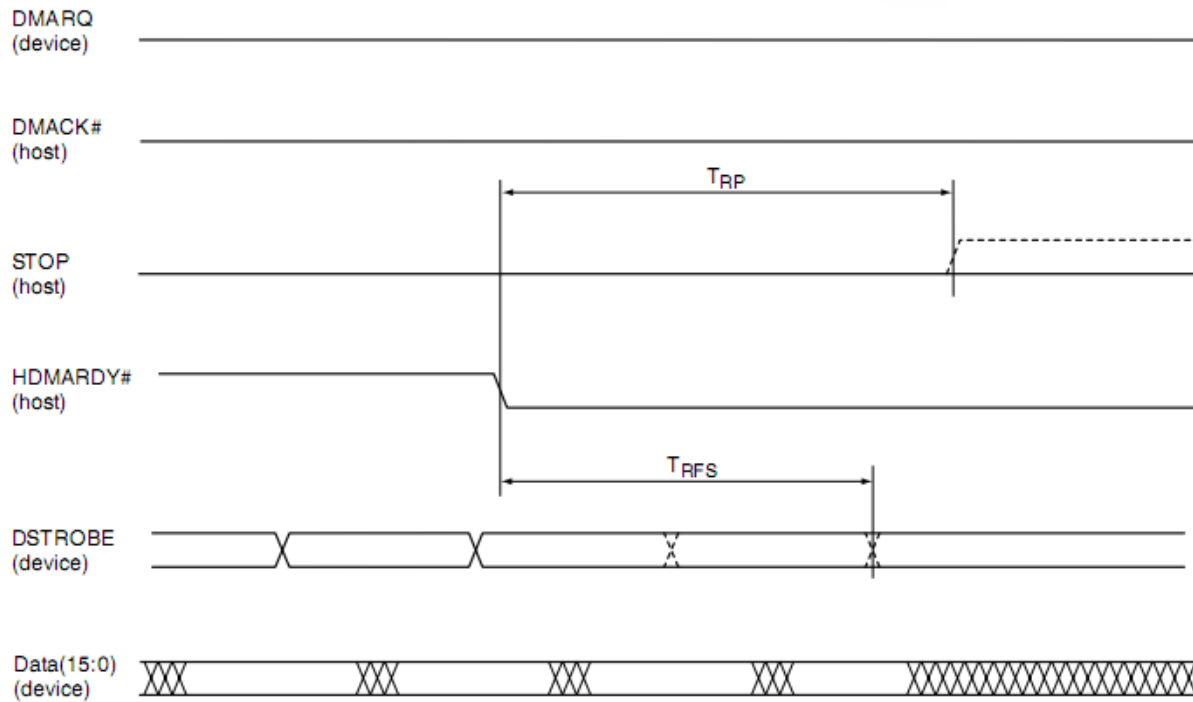


Figure 7-10: Sustained Ultra DMA Data-In Burst

Notes:

1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than T_{RP} after HDMARDY# is negated.
2. After negating HDMARDY#, the host may receive zero, one, two, or three more data words from the device.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

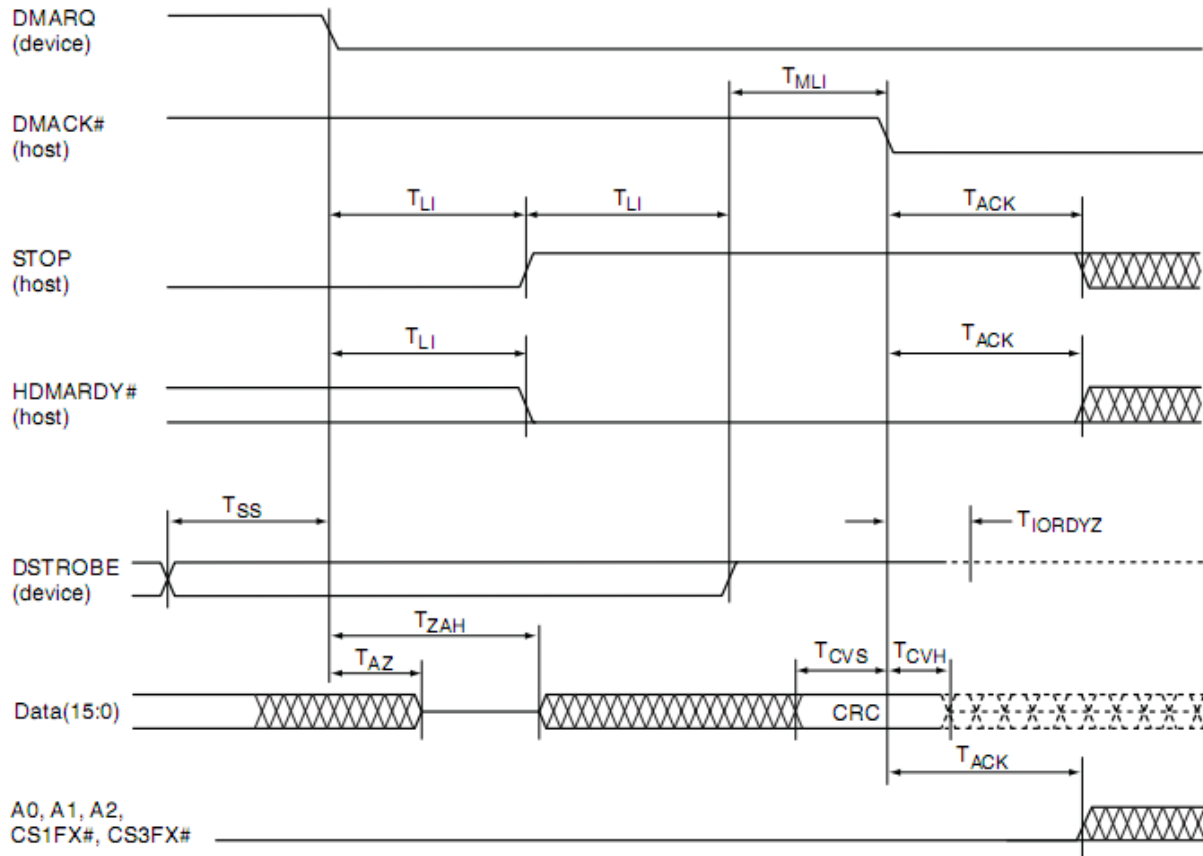


Figure 7-11: Device Terminating and Ultra DMA Data-In Burst

Notes:

1. The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

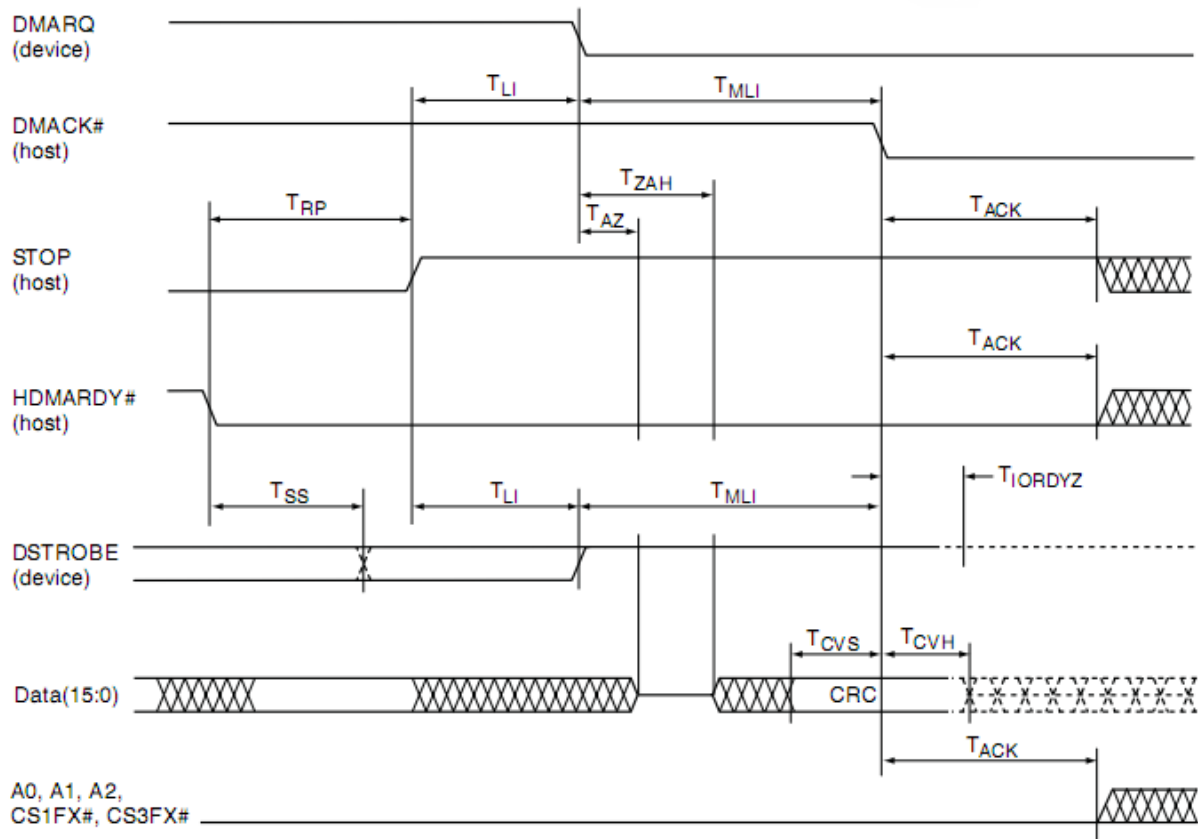


Figure 7-12: Host Terminating and Ultra DMA Data-In Burst

Notes:

1. The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

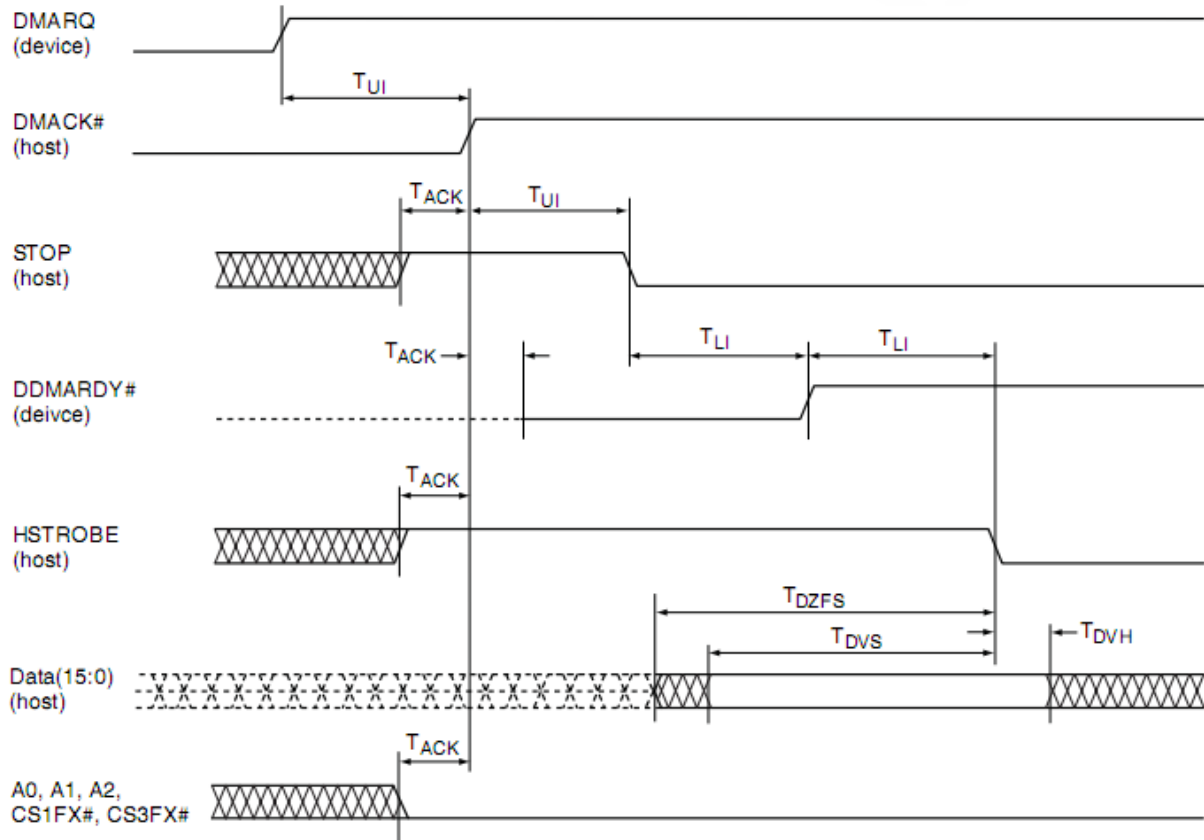


Figure 7-13: Initiating an Ultra DMA Data-Out Burst

Notes:

1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

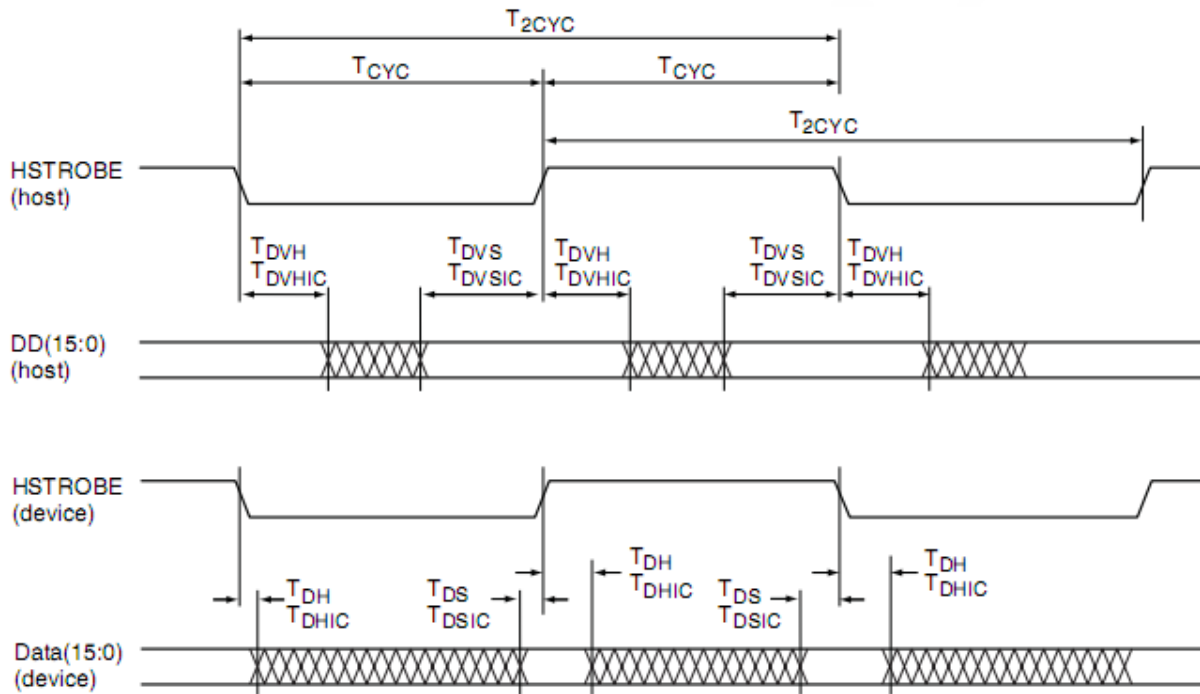


Figure 7-14: Sustained Ultra DMA Data-Out Burst

Notes:

1. DD(15:0) and HSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay will not allow the data signals to be considered stable at the host until some time after they are driven by the host.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

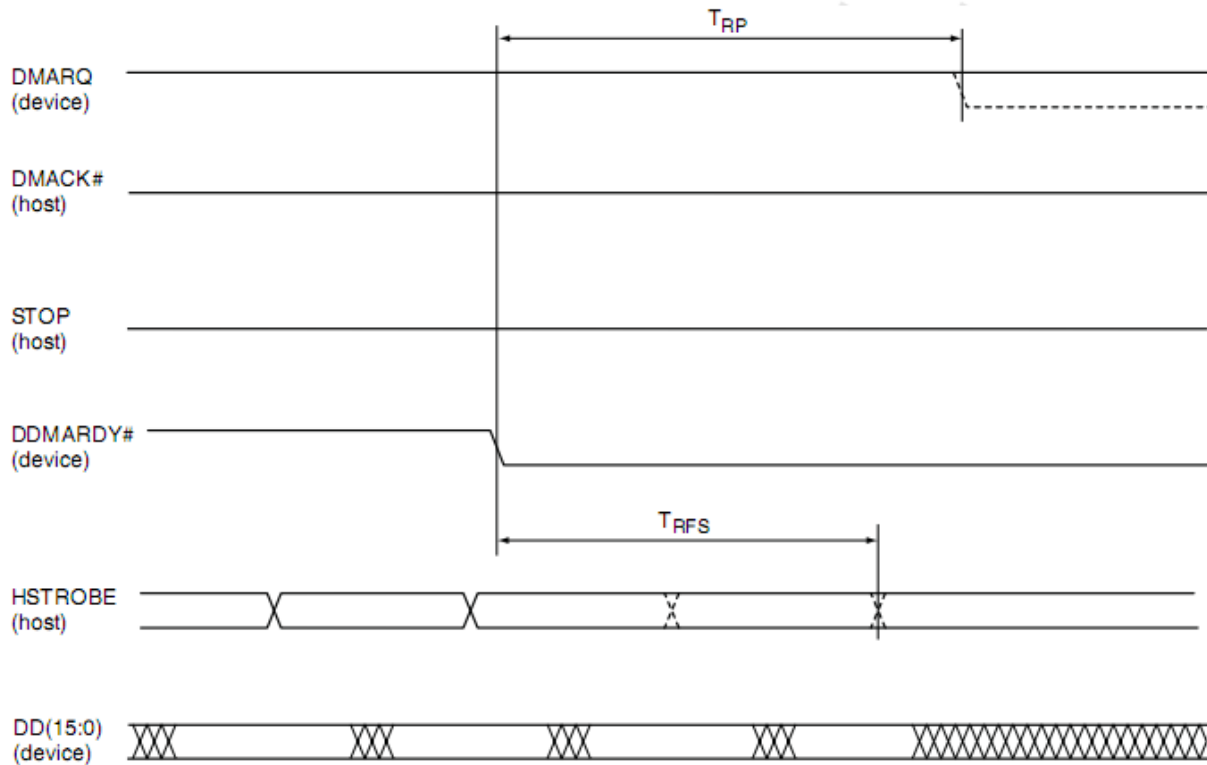


Figure 7-15: Device Pausing and Ultra DMA Data-Out Burst

Notes:

1. The host may negate DMARQ to request termination of the Ultra DMA burst no sooner than T_{RP} after DDMARDY# is negated.
2. After negating DDMARDY#, the host may receive zero, one, two, or three more data words from the host.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

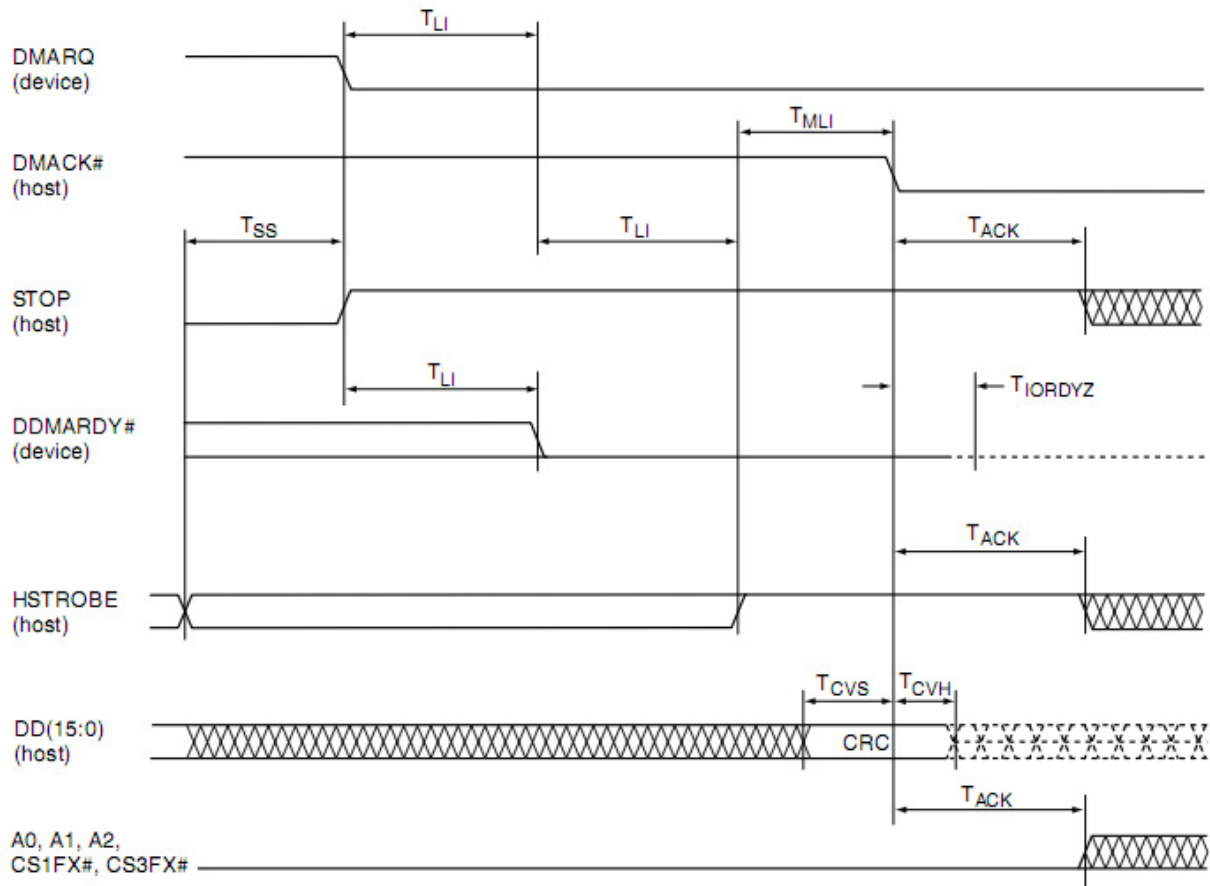


Figure 7-16: Host Terminating and Ultra DMA Data-Out Burst

Notes:

1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

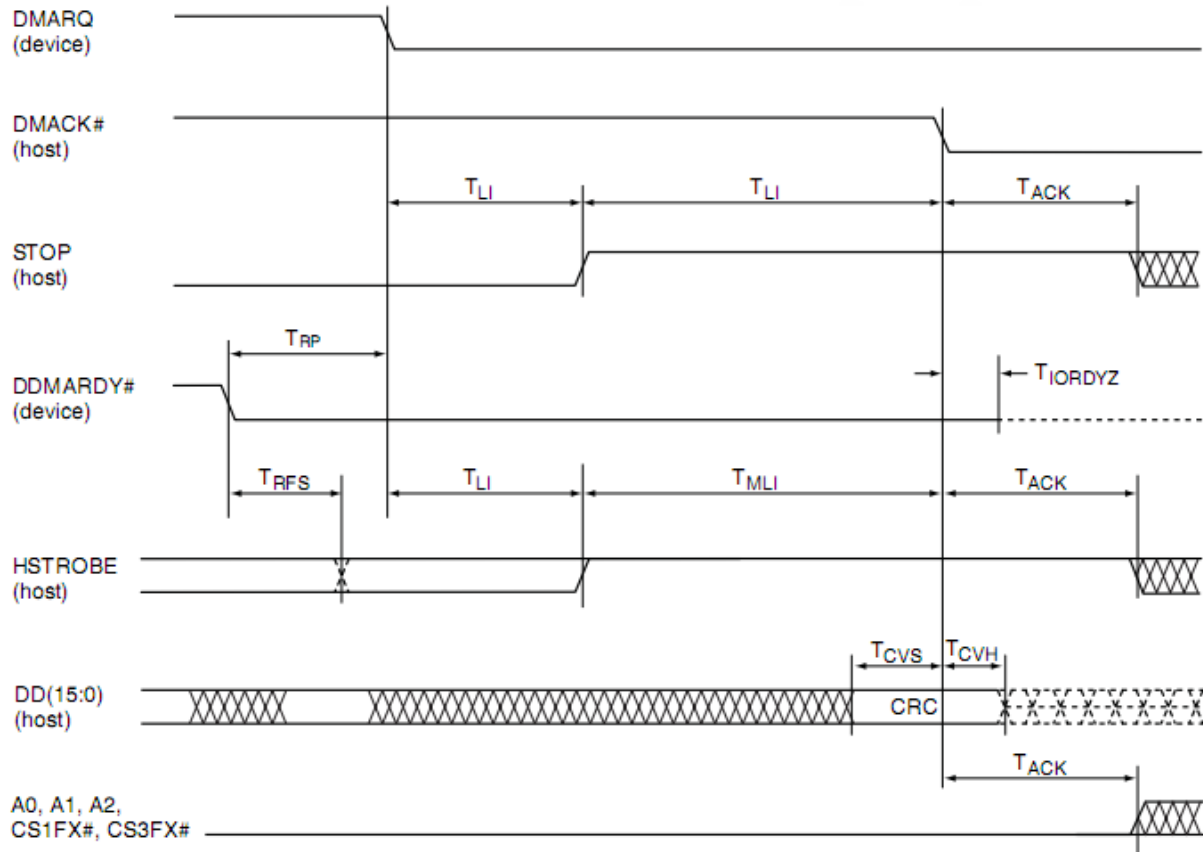


Figure 7-17: Device Terminating and Ultra DMA Data-Out Burst

Notes:

1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

7.3.0 Media Side Interface I/O Timing Specifications

Table 7-13: Timing Parameter

| Symbol | Parameter | Min | Max | Units |
|------------------|---|-----|-----|-------|
| T _{CLS} | FCLE Setup Time | 20 | - | ns |
| T _{CLH} | FCLE Hold Time | 40 | - | ns |
| T _{CS} | FCE# Setup Time | 40 | - | ns |
| T _{CH} | FCE# Hold Time for Command/Data Write Cycle | 40 | - | ns |
| T _{CHR} | FCE# Hold Time for Sequential Read Last Cycle | - | 40 | ns |
| T _{WP} | FWE# Pulse Width | 20 | - | ns |
| T _{WH} | FWE# High Hold Time | 20 | - | ns |
| T _{WC} | Write Cycle Time | 40 | - | ns |
| T _{ALS} | FALE Setup Time | 20 | - | ns |
| T _{ALH} | FALE Hold Time | 40 | - | ns |
| T _{DS} | FAD[15:0] Setup Time | 20 | - | ns |
| T _{DH} | FAD[15:0] Hold Time | 20 | - | ns |
| T _{RP} | FRE# Pulse Width | 20 | - | ns |
| T _{RR} | Ready to FRE# Low | 40 | - | ns |
| T _{RES} | FRE# Data Setup Access Time | 20 | - | ns |
| T _{RC} | Read Cycle Time | 40 | - | ns |
| T _{REH} | FRE# High Hold Time | 20 | - | ns |
| T _{RHZ} | FRE# High to Data Hi-Z | 5 | - | ns |

Note: All AC specifications are guaranteed by design.

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

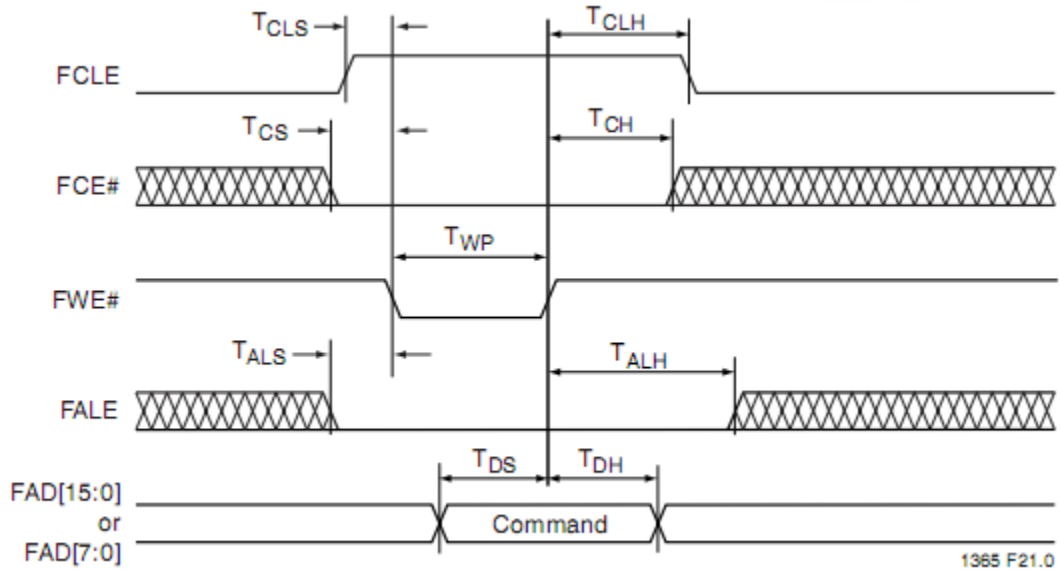


Figure 7-18: Media Command Latch Cycle

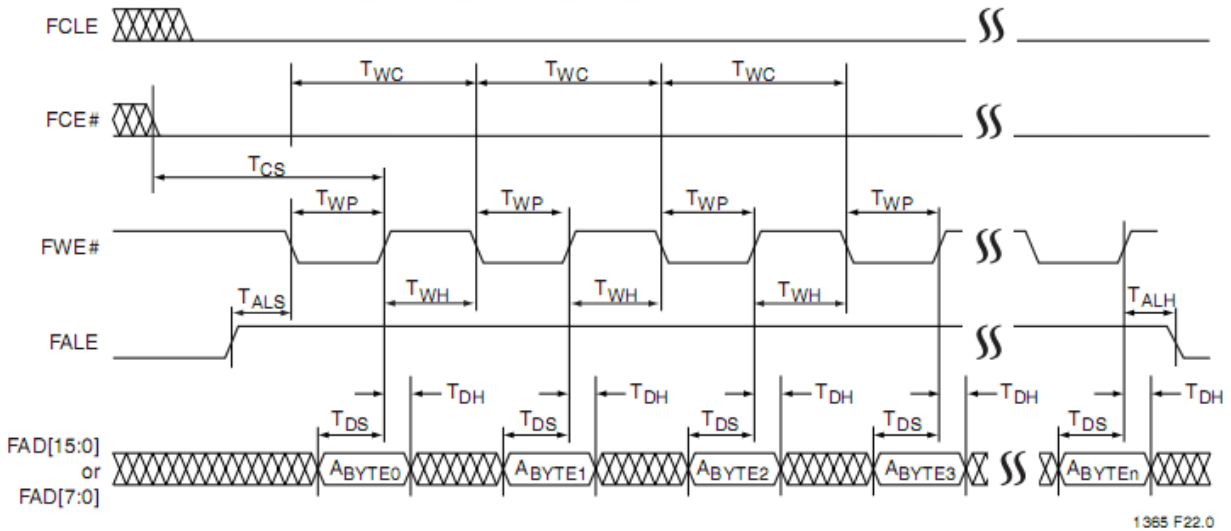


Figure 7-19: Media Access Latch Cycle

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

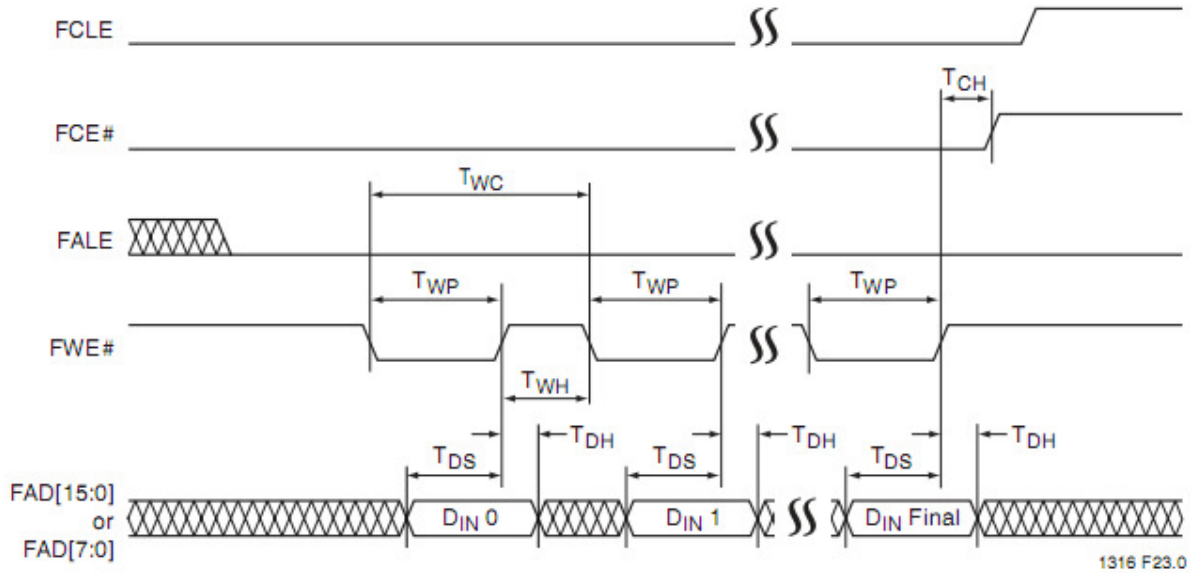


Figure 7-20: Media Data Loading Latch Cycle

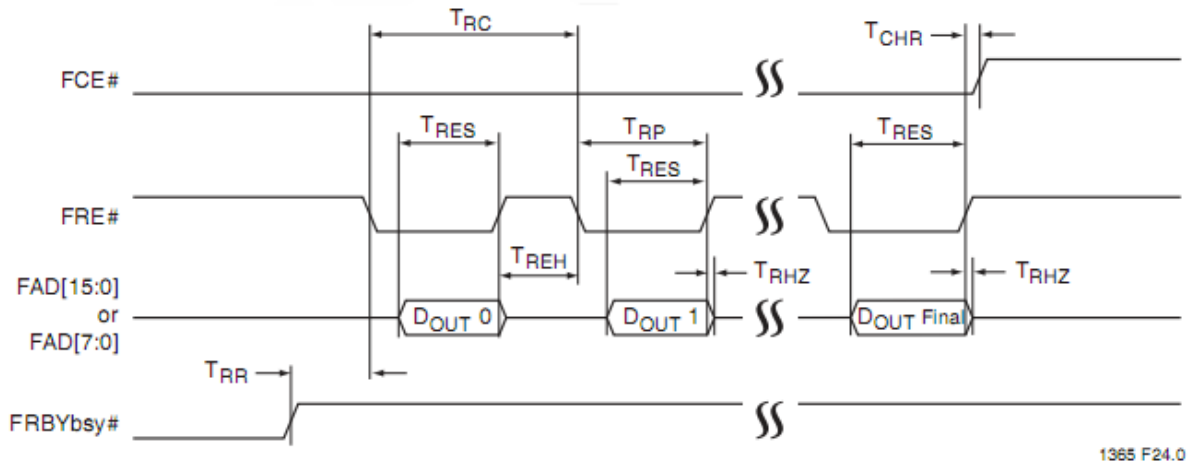


Figure 7-21: Media Data Read Cycle

Compact Flash III series AP-CFxxxxE3NR-XXXXXXQ

8. Physical Characteristics

8.1 Dimension

TABLE 8-1: Type I CFC physical specification

| | |
|--|--------------------------------------|
| Length: | 36.40 +/- 0.15mm (1.433+/- 0.06 in.) |
| Width: | 42.80 +/- 0.10mm (1.685+/- 0.04 in.) |
| Thickness (Including Label Area): | 3.3mm+/-0.10mm (0.130+/-0.04in.) |

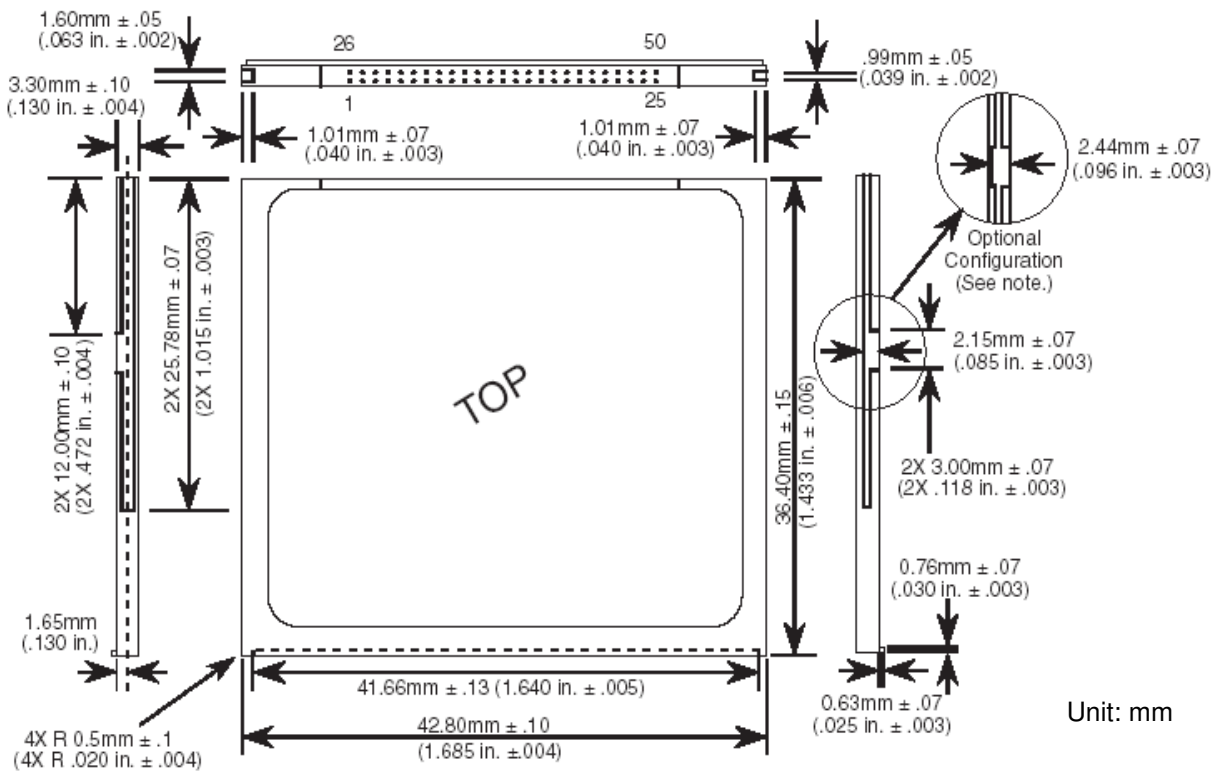


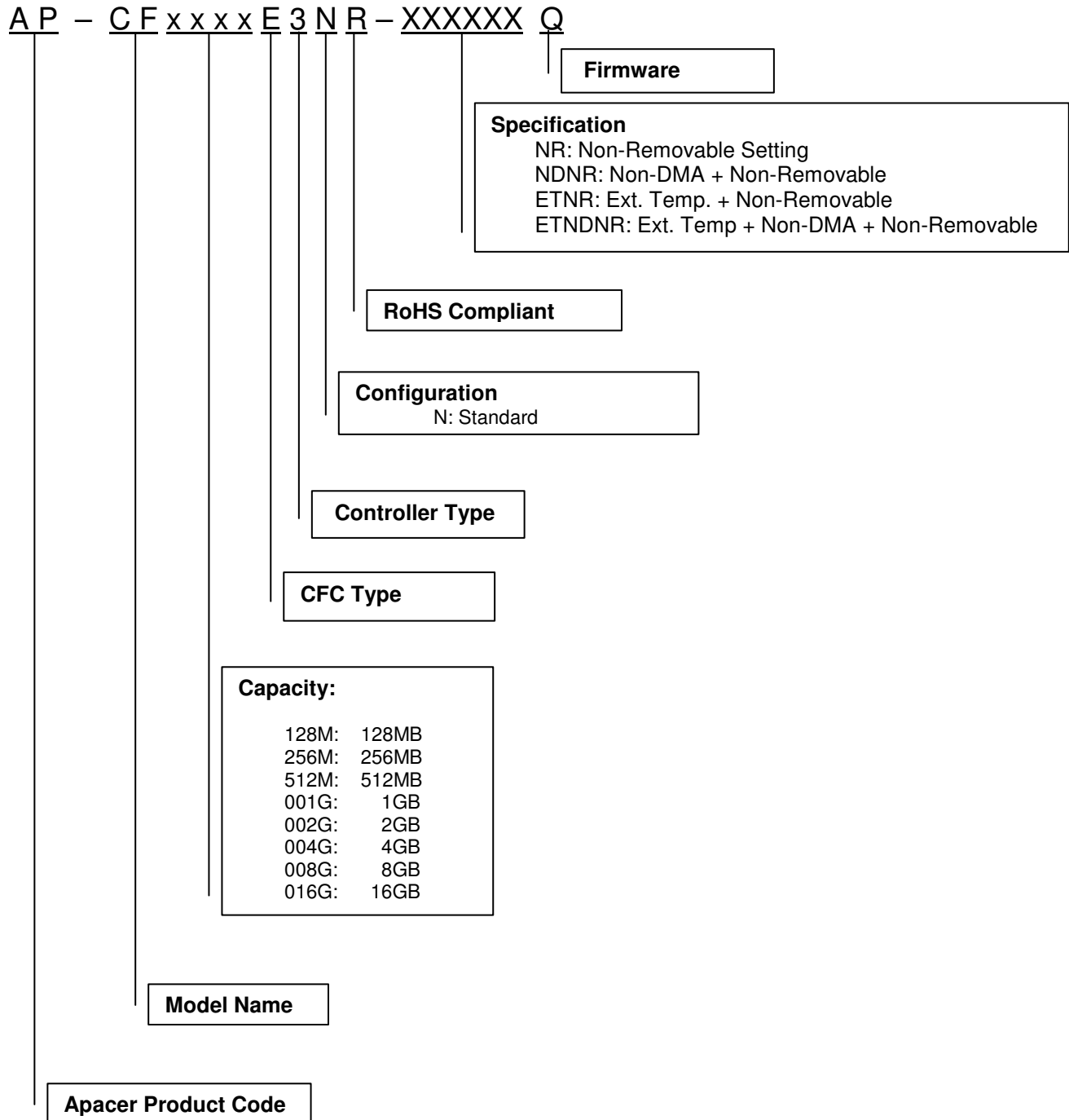
FIGURE 8-1: Physical dimension

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

9. Product Ordering Information

9.1 Product Code Designations



Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

9.2 Valid Combinations

Standard Temperature

Non-Removable

| Capacity | Model Number |
|----------|-------------------|
| 128MB | AP-CF128ME3NR-NRQ |
| 256MB | AP-CF256ME3NR-NRQ |
| 512MB | AP-CF512ME3NR-NRQ |
| 1GB | AP-CF001GE3NR-NRQ |
| 2GB | AP-CF002GE3NR-NRQ |
| 4GB | AP-CF004GE3NR-NRQ |
| 8GB | AP-CF008GE3NR-NRQ |
| 16GB | AP-CF016GE3NR-NRQ |

Non-DMA & Non-Removable

| Capacity | Model Number |
|----------|---------------------|
| 128MB | AP-CF128ME3NR-NDNRQ |
| 256MB | AP-CF256ME3NR-NDNRQ |
| 512MB | AP-CF512ME3NR-NDNRQ |
| 1GB | AP-CF001GE3NR-NDNRQ |
| 2GB | AP-CF002GE3NR-NDNRQ |
| 4GB | AP-CF004GE3NR-NDNRQ |
| 8GB | AP-CF008GE3NR-NDNRQ |
| 16GB | AP-CF016GE3NR-NDNRQ |

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

Extended Temperature

Non-Removable

| Capacity | Model Number |
|----------|---------------------|
| 128MB | AP-CF128ME3NR-ETNRQ |
| 256MB | AP-CF256ME3NR-ETNRQ |
| 512MB | AP-CF512ME3NR-ETNRQ |
| 1GB | AP-CF001GE3NR-ETNRQ |
| 2GB | AP-CF002GE3NR-ETNRQ |
| 4GB | AP-CF004GE3NR-ETNRQ |
| 8GB | AP-CF008GE3NR-ETNRQ |
| 16GB | AP-CF016GE3NR-ETNRQ |

Non-DMA & Non-Removable

| Capacity | Model Number |
|----------|-----------------------|
| 128MB | AP-CF128ME3NR-ETNDNRQ |
| 256MB | AP-CF256ME3NR-ETNDNRQ |
| 512MB | AP-CF512ME3NR-ETNDNRQ |
| 1GB | AP-CF001GE3NR-ETNDNRQ |
| 2GB | AP-CF002GE3NR-ETNDNRQ |
| 4GB | AP-CF004GE3NR-ETNDNRQ |
| 8GB | AP-CF008GE3NR-ETNDNRQ |
| 16GB | AP-CF016GE3NR-ETNDNRQ |

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

Revision History

| Revision | Date | Description | Remark |
|----------|------------|--|--------|
| 1.0 | 05/19/2011 | Official release | |
| 1.1 | 08/11/2013 | Updated performance and product ordering information due to change in NAND flash use Updated the address of Taiwan headquarter Added endurance TBW section to replace MTBF | |
| 1.2 | 11/08/2013 | Added AC/DC characteristics Revised True IDE mode pin assignments | |
| 1.3 | 01/15/2014 | Revised DC characteristic table | |
| 1.4 | 03/27/2014 | Updated command set table | |
| 1.5 | 09/10/2014 | Updated pin assignments | |

Compact Flash III series

AP-CFxxxxE3NR-XXXXXXQ

Global Presence

| | |
|------------------------------|---|
| Taiwan (Headquarters) | Apacer Technology Inc. Apacer Technology Inc. 1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan R.O.C. Tel: 886-2-2267-8000 Fax: 886-2-2267-2261 amtsales@apacer.com |
| U.S.A. | Apacer Memory America, Inc. 386 Fairview Way, Suite102, Milpitas, CA 95035 Tel: 1-408-518-8699 Fax: 1-408-935-9611 sa@apacerus.com |
| Japan | Apacer Technology Corp. 5F, Matsura Bldg., Shiba, Minato-Ku Tokyo, 105-0014, Japan Tel: 81-3-5419-2668 Fax: 81-3-5419-0018 jpservices@apacer.com |
| Europe | Apacer Technology B.V. Science Park Eindhoven 5051 5692 EB Son, The Netherlands Tel: 31-40-267-0000 Fax: 31-40-267-0000#6199 sales@apacer.nl |
| China | Apacer Electronic (Shanghai) Co., Ltd 1301, No.251, Xiaomuqiao Road, Shanghai, 200032, China Tel: 86-21-5529-0222 Fax: 86-21-5206-6939 sales@apacer.com.cn |
| India | Apacer Technologies Pvt. Ltd. # 535, 1st Floor, 8th cross, JP Nagar 3rd Phase, Bangalore – 560078, India Tel: 91-80-4152-9061 sales_india@apacer.com |

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
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- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru