

Description

The 9DBV0941 is a member of IDT's Full-Featured PCIe family. The device has 9 output enables for clock management, and 3 selectable SMBus addresses. It has integrated terminations for direct connection to 100Ω transmission lines.

Recommended Application

PCIe Gen1–3 clock distribution in Storage, Networking, Compute, Consumer

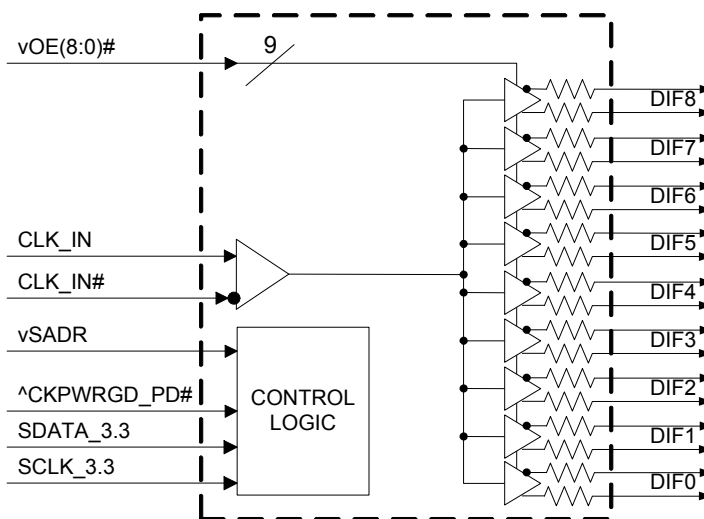
Output Features

- 9 1–200MHz Low-Power (LP) HCSL DIF pairs with $Z_o = 100\Omega$
- Easy AC-coupling to other logic families, see IDT application note [AN-891](#)

Key Specifications

- *Additive* cycle-to-cycle jitter < 5ps
- Output-to-output skew < 60ps
- *Additive* phase jitter is < 100fs rms for PCIe Gen3
- *Additive* phase jitter < 300fs rms (12kHz-20MHz at 125MHz)

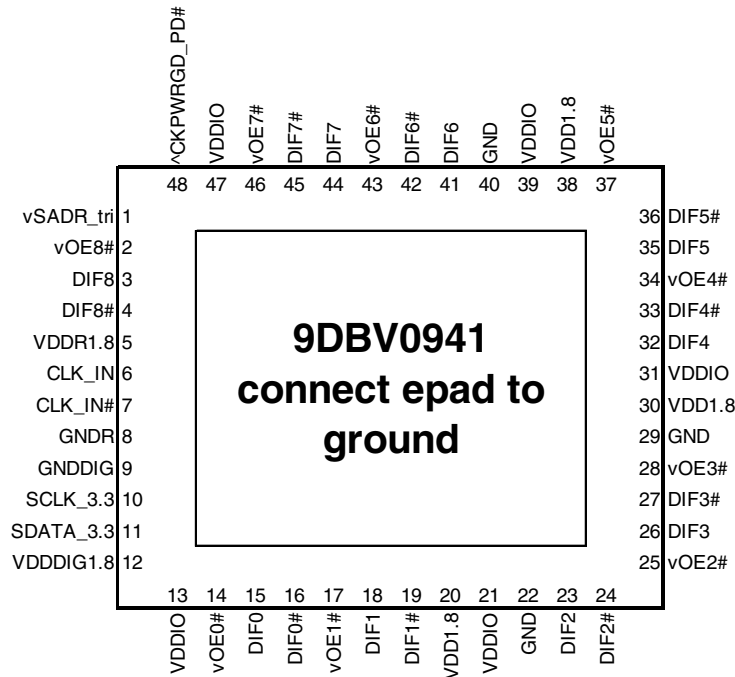
Block Diagram



Features/Benefits

- 100Ω direct connect; saves 36 resistors and 62mm^2 compared to standard HCSL
- 53mW typical power consumption; eliminates thermal concerns
- Outputs can optionally be supplied from any voltage between 1.05V and 1.8V; maximum power savings
- OE# pins; support DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- SMBus-selectable features allow optimization to customer requirements
 - Slew rate for each output; allows tuning for various line lengths
 - Differential output amplitude; allows tuning for various application environments
- 1MHz to 200MHz operating frequency
- 3.3V tolerant SMBus interface works with legacy controllers
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Device contains default configuration; SMBus interface not required for device operation
- 6 x 6 mm 48-VFQFPN; minimal board space

Pin Configuration



48-pin VFQFPN, 6x6 mm, 0.4mm pitch

- ^v prefix indicates internal 120KOhm pull up *AND* pull down resistor (biased to VDD/2)
- v prefix indicates internal 120KOhm pull down resistor
- ^ prefix indicates internal 120KOhm pull up resistor

SMBus Address Selection Table

| | SADR | Address | + Read/Write bit |
|---|------|---------|------------------|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101011 | x |
| | M | 1101100 | x |
| | 1 | 1101101 | x |

Power Management Table

| CKPWRGD_PD# | CLK_IN | SMBus OEx bit | OEx# Pin | DIFx | |
|-------------|---------|---------------|----------|----------|-----------|
| | | | | True O/P | Comp. O/P |
| 0 | X | X | X | Low | Low |
| 1 | Running | 0 | X | Low | Low |
| 1 | Running | 1 | 0 | Running | Running |
| 1 | Running | 1 | 1 | Low | Low |

Power Connections

| Pin Number | | | Description |
|-------------|----------------|----------|-----------------------|
| VDD | VDDIO | GND | |
| 5 | | 8 | Input receiver analog |
| 12 | | 9 | Digital power |
| 20,30,31,38 | 13,21,31,39,47 | 22,29,40 | DIF outputs |

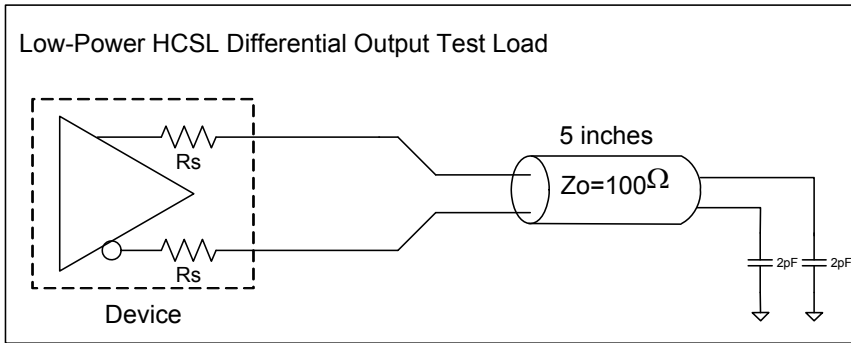
Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------|---------------|--|
| 1 | vSADR_tri | LATCHED IN | Tri-level latch to select SMBus Address. It has an internal 120kohm pull down resistor. See SMBus Address Selection Table. |
| 2 | vOE8# | IN | Active low input for enabling output 8. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 3 | DIF8 | OUT | Differential true clock output. |
| 4 | DIF8# | OUT | Differential complementary clock output. |
| 5 | VDDR1.8 | PWR | Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 1.8V. |
| 6 | CLK_IN | IN | True input for differential reference clock. |
| 7 | CLK_IN# | IN | Complementary input for differential reference clock. |
| 8 | GNDR | GND | Analog ground pin for the differential input (receiver). |
| 9 | GNDDIG | GND | Ground pin for digital circuitry. |
| 10 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 11 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 12 | VDDDIG1.8 | PWR | 1.8V digital power (dirty power). |
| 13 | VDDIO | PWR | Power supply for differential outputs. |
| 14 | vOE0# | IN | Active low input for enabling output 0. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 15 | DIF0 | OUT | Differential true clock output. |
| 16 | DIF0# | OUT | Differential complementary clock output. |
| 17 | vOE1# | IN | Active low input for enabling output 1. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 18 | DIF1 | OUT | Differential true clock output. |
| 19 | DIF1# | OUT | Differential complementary clock output. |
| 20 | VDD1.8 | PWR | Power supply, nominally 1.8V. |
| 21 | VDDIO | PWR | Power supply for differential outputs. |
| 22 | GND | GND | Ground pin. |
| 23 | DIF2 | OUT | Differential true clock output. |
| 24 | DIF2# | OUT | Differential complementary clock output. |
| 25 | vOE2# | IN | Active low input for enabling output 2. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 26 | DIF3 | OUT | Differential true clock output. |
| 27 | DIF3# | OUT | Differential complementary clock output. |
| 28 | vOE3# | IN | Active low input for enabling output 3. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 29 | GND | GND | Ground pin. |
| 30 | VDD1.8 | PWR | Power supply, nominally 1.8V. |
| 31 | VDDIO | PWR | Power supply for differential outputs. |
| 32 | DIF4 | OUT | Differential true clock output. |
| 33 | DIF4# | OUT | Differential complementary clock output. |
| 34 | vOE4# | IN | Active low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 35 | DIF5 | OUT | Differential true clock output. |

Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------|------|---|
| 36 | DIF5# | OUT | Differential complementary clock output. |
| 37 | vOE5# | IN | Active low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 38 | VDD1.8 | PWR | Power supply, nominally 1.8V. |
| 39 | VDDIO | PWR | Power supply for differential outputs. |
| 40 | GND | GND | Ground pin. |
| 41 | DIF6 | OUT | Differential true clock output. |
| 42 | DIF6# | OUT | Differential complementary clock output. |
| 43 | vOE6# | IN | Active low input for enabling output 6. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 44 | DIF7 | OUT | Differential true clock output. |
| 45 | DIF7# | OUT | Differential complementary clock output. |
| 46 | vOE7# | IN | Active low input for enabling output 7. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. |
| 47 | VDDIO | PWR | Power supply for differential outputs. |
| 48 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kohm pull-up resistor. |
| 49 | EPAD | GND | Connect epad to ground. |

Test Loads



Alternate Terminations

The 9DBV0941 can easily drive LVPECL, LVDS, and CML logic. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with IDT’s “Universal” Low-Power HCSL Outputs”](#) for details.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBV0941. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|--------------------------------|------|-----|----------------------|-------|-------|
| Supply Voltage | VDDx | Applies to VDD, VDDA and VDDIO | -0.5 | | 2.5 | V | 1,2 |
| Input Voltage | V _{IN} | | -0.5 | | V _{DD} +0.5 | V | 1,3 |
| Input High Voltage, SMBus | V _{IHSMB} | SMBus clock and data pins | | | 3.6 | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD Protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 2.5V.

Electrical Characteristics—Clock Input Parameters

T_A = T_{COM} or T_{IND}; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|--------------------|---|-----|-----|-----|-------|-------|
| Input Crossover Voltage - DIF_IN | V _{CROSS} | Cross over voltage | 150 | | 900 | mV | 1 |
| Input Swing - DIF_IN | V _{SWING} | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | μA | |
| Input Duty Cycle | d _{tin} | Measurement from differential waveform | 40 | | 60 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFIN} | Differential measurement | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T_{COM} or T_{IND}; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--|------------------------|---|----------------------|----------|-----------------------|--------|-------|
| Supply Voltage | VDDx | Supply voltage for core and analog | 1.7 | 1.8 | 1.9 | V | |
| Output Supply Voltage | VDDIO | Low Voltage Supply LP-HCSL Outputs | 0.9975 | 1.05-1.8 | 1.9 | V | |
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | 25 | 70 | °C | 1 |
| | T _{IND} | Industrial range | -40 | 25 | 85 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus | 0.75 V _{DD} | | V _{DD} + 0.3 | V | |
| Input Mid Voltage | V _{IM} | Single-ended tri-level inputs ('_tri' suffix) | 0.4 V _{DD} | | 0.6 V _{DD} | V | |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus | -0.3 | | 0.25 V _{DD} | V | |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | µA | |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | µA | |
| Input Frequency | F _{in} | | 1 | | 200 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,6 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} power-up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | f _{MODINPCIe} | Allowable frequency for PCIe applications (Triangular modulation) | 30 | | 33 | kHz | |
| Input SS Modulation Frequency non-PCIe | f _{MODIN} | Allowable frequency for non-PCIe applications (Triangular modulation) | 0 | | 66 | kHz | |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | µs | 1,3 |
| Tfall | t _F | Fall time of single-ended control inputs | | | 5 | ns | 2 |
| Trise | t _R | Rise time of single-ended control inputs | | | 5 | ns | 2 |
| SMBus Input Low Voltage | V _{ILSMB} | V _{DDSMB} = 3.3V, see note 4 for V _{DDSMB} < 3.3V | | | 0.8 | V | 4 |
| SMBus Input High Voltage | V _{IHSMB} | V _{DDSMB} = 3.3V, see note 5 for V _{DDSMB} < 3.3V | 2.1 | | 3.3 | V | 5 |
| SMBus Output Low Voltage | V _{OLSMB} | at I _{PULLUP} | | | 0.4 | V | |
| SMBus Sink Current | I _{PULLUP} | at V _{OL} | 4 | | | mA | |
| Nominal Bus Voltage | V _{DDSMB} | Bus voltage | 1.7 | | 3.6 | V | |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max VIL - 0.15V) to (Min VIH + 0.15V) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min VIH + 0.15V) to (Max VIL - 0.15V) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 400 | kHz | 7 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200 mV.

⁴ For V_{DDSMB} < 3.3V, V_{ILSMB} <= 0.35V_{DDSMB}.

⁵ For V_{DDSMB} < 3.3V, V_{IHSMB} >= 0.65V_{DDSMB}.

⁶ DIF_IN input.

⁷ The differential input clock must be running for the SMBus to be active.

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T_{COM} or T_{IND}; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| Parameter | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------|---|------|------|------|-------|-------|
| Slew Rate | Trf | Scope averaging on, fast slew rate setting | 1.6 | 2.6 | 4.3 | V/ns | 1,2,3 |
| | | Scope averaging on, slow slew rate setting | 1.2 | 2.0 | 3.2 | V/ns | 1,2,3 |
| Slew Rate Matching | ΔTrf | Slew rate matching, scope averaging on | | 6 | 20 | % | 1,2,4 |
| Voltage High | V _{HIGH} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 758 | 850 | mV | 7 |
| Voltage Low | V _{LOW} | | -150 | 43 | 150 | | 7 |
| Max Voltage | V _{max} | Measurement on single ended signal using absolute value. (Scope averaging off) | | 775 | 1150 | mV | 7 |
| Min Voltage | V _{min} | | -300 | 12 | | | 7 |
| Vswing | Vswing | Scope averaging off | 300 | 1428 | | mV | 1,2 |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off | 250 | 391 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ-V _{cross} | Scope averaging off | | 14 | 140 | mV | 1,6 |

¹Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF with R_S = 33Ω for Z_O = 50Ω (100Ω differential trace)

² Measured from differential waveform.

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting Δ-V_{cross} to be smaller than V_{cross} absolute.

⁷ 660mV V_{high} is the minimum when VDDIO is >= 1.05V +/-5%. If VDDIO is < 1.05V +/-5%, the minimum V_{high} will be VDDIO_{min} - 250mV. For example, for VDDIO = 0.9V +/-5%, V_{HIGHmin} will be 860mV - 250mV = 610mV.

Electrical Characteristics–Current Consumption

TA = T_{COM} or T_{IND}; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|----------------------|--|-----|-------|-----|-------|-------|
| Operating Supply Current | I _{DDR} | VDDR at 100MHz | | 3 | 5 | mA | 1 |
| | I _{DDDIG} | VDDIG, all outputs at 100MHz | | 6 | 10 | mA | 1 |
| | I _{DDO} | VDDO1.8 + VDDIO, all outputs at 100MHz | | 35 | 40 | mA | 1 |
| Powerdown Current | I _{DRPD} | VDDR, CKPWRGD_PD# = 0 | | 0.4 | 1 | mA | 1,2 |
| | I _{DDDIGPD} | VDDDIG, CKPWRGD_PD# = 0 | | 0.6 | 1 | mA | 1, 2 |
| | I _{DDOPD} | VDDO1.8 + VDDIO, CKPWRGD_PD# = 0 | | 0.002 | 0.1 | mA | 1, 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{COM} or T_{IND}; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|-----------------------------------|------|------|------|-------|-------|
| Duty Cycle Distortion | t _{DCD} | Measured differentially at 100MHz | -1 | -0.1 | 1 | % | 1,3 |
| Skew, Input to Output | t _{pdBYP} | V _T = 50% | 1800 | 2342 | 3000 | ps | 1 |
| Skew, Output to Output | t _{sk3} | V _T = 50% | | 37 | 60 | ps | 1,4 |
| Jitter, Cycle to Cycle | t _{jcc-cyc} | Additive Jitter | | 0.1 | 5 | ps | 1,2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Duty cycle distortion is the difference in duty cycle between the output and the input clock.

⁴ All outputs at default slew rate.

Electrical Characteristics–Phase Jitter Parameters

TA = T_{COM} or T_{IND}; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|-----------------------|-------------------------|---|-----|------|-----|----------------|----------|---------|
| Additive Phase Jitter | t _{jphPCleG1} | PCIe Gen 1 | | 0.1 | 5 | N/A | ps (p-p) | 1,2,3 |
| | t _{jphPCleG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.1 | 0.4 | N/A | ps (rms) | 1,2,5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.01 | 0.4 | N/A | ps (rms) | 1,2,5 |
| | t _{jphPCleG3} | PCIe Gen 3 (2-4MHz or 2-5MHz, CDR = 10MHz) | | 0.00 | 0.1 | N/A | ps (rms) | 1,2,4,5 |
| | t _{jphSGMIIM0} | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 165 | 200 | N/A | fs (rms) | 1,6 |
| | t _{jphSGMIIM1} | 125MHz, 12kHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 251 | 300 | N/A | fs (rms) | 1,6 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs.

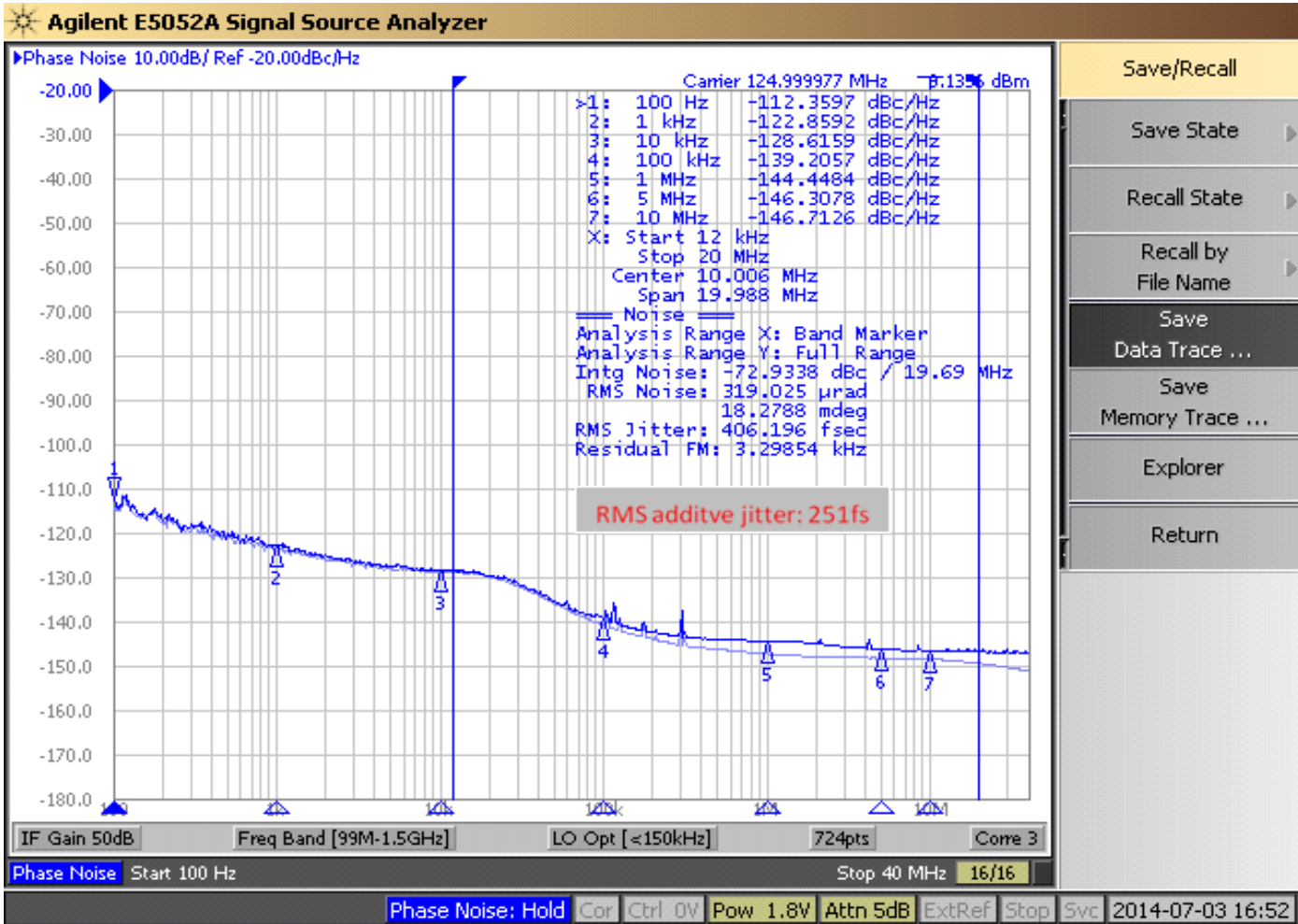
³ Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1-12.

⁴ For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)² - (input jitter)²].

⁵ Driven by 9FGV0831 or equivalent.

⁶ Driven by Rohde & Schwarz SMA100.

Additive Phase Jitter Plot: 125M (12kHz to 20MHz)



General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation | | | |
|-----------------------------|-----------|--------|----------------------|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | O |
| O | | | O |
| O | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

Note: SMBus Address is Latched on SADR pin.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|----------------------------|-----------------|--------|----------------------|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | Data Byte Count=X |
| ACK | | X Byte | |
| ACK | | | Beginning Byte N |
| | | | O |
| | | | O |
| | | | O |
| ACK | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

SMBus Table: Output Enable Register ¹

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|--------|---------|------------------|------|---------|-----------------|---------|
| Bit 7 | DIF OE7 | Output Enable | RW | Low/Low | OE# pin control | 1 |
| Bit 6 | DIF OE6 | Output Enable | RW | Low/Low | OE# pin control | 1 |
| Bit 5 | DIF OE5 | Output Enable | RW | Low/Low | OE# pin control | 1 |
| Bit 4 | DIF OE4 | Output Enable | RW | Low/Low | OE# pin control | 1 |
| Bit 3 | DIF OE3 | Output Enable | RW | Low/Low | OE# pin control | 1 |
| Bit 2 | DIF OE2 | Output Enable | RW | Low/Low | OE# pin control | 1 |
| Bit 1 | DIF OE1 | Output Enable | RW | Low/Low | OE# pin control | 1 |
| Bit 0 | DIF OE0 | Output Enable | RW | Low/Low | OE# pin control | 1 |

1. A low on these bits will override the OE# pin and force the differential output Low/Low

SMBus Table: Output Enable and Output Amplitude Control Register

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------|---------------------------|------|-----------|-----------------|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | DIF OE8 | Output Enable | RW | Low/Low | OE# pin control | 1 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 1 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.6V | 01 = 0.7V | 1 |
| Bit 0 | AMPLITUDE 0 | | RW | 10 = 0.8V | 11 = 0.9V | 0 |

1. A low on the DIF OE bit will override the OE# pin and force the differential output Low/Low

SMBus Table: DIF Slew Rate Control Register

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|--------------------------|------|--------------|--------------|---------|
| Bit 7 | SLEWRATESEL DIF7 | Adjust Slew Rate of DIF7 | RW | Slow setting | Fast setting | 1 |
| Bit 6 | SLEWRATESEL DIF6 | Adjust Slew Rate of DIF6 | RW | Slow setting | Fast setting | 1 |
| Bit 5 | SLEWRATESEL DIF5 | Adjust Slew Rate of DIF5 | RW | Slow setting | Fast setting | 1 |
| Bit 4 | SLEWRATESEL DIF4 | Adjust Slew Rate of DIF4 | RW | Slow setting | Fast setting | 1 |
| Bit 3 | SLEWRATESEL DIF3 | Adjust Slew Rate of DIF3 | RW | Slow setting | Fast setting | 1 |
| Bit 2 | SLEWRATESEL DIF2 | Adjust Slew Rate of DIF2 | RW | Slow setting | Fast setting | 1 |
| Bit 1 | SLEWRATESEL DIF1 | Adjust Slew Rate of DIF1 | RW | Slow setting | Fast setting | 1 |
| Bit 0 | SLEWRATESEL DIF0 | Adjust Slew Rate of DIF0 | RW | Slow setting | Fast setting | 1 |

SMBus Table: DIF Slew Rate Control Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|--------------------------|------|--------------|--------------|---------|
| Bit 7 | Reserved | | | | | 1 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | Reserved | | | | | 1 |
| Bit 0 | SLEWRATESEL DIF8 | Adjust Slew Rate of DIF8 | RW | Slow setting | Fast setting | 1 |

Byte 4 is Reserved and reads back 'hFF'

SMBus Table: Revision and Vendor ID Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|--------------|---|---------|
| Bit 7 | RID3 | Revision ID | R | A rev = 0000 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 0 |
| Bit 3 | VID3 | VENDOR ID | R | 0001 = IDT | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

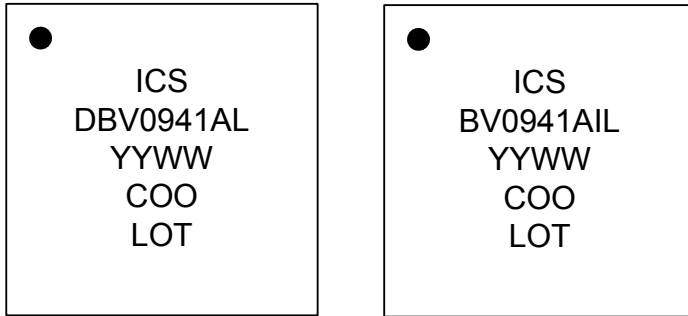
SMBus Table: Device Type/Device ID

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|--------|--------------|------------------|------|---|---|---------|
| Bit 7 | Device Type1 | Device Type | R | 00 = FG, 01 = DB 10 = DM, 11= DB fanout only | | 1 |
| Bit 6 | Device Type0 | | R | | | 1 |
| Bit 5 | Device ID5 | Device ID | R | 001001binary or 09 hex | | 0 |
| Bit 4 | Device ID4 | | R | | | 0 |
| Bit 3 | Device ID3 | | R | | | 1 |
| Bit 2 | Device ID2 | | R | | | 0 |
| Bit 1 | Device ID1 | | R | | | 0 |
| Bit 0 | Device ID0 | | R | | | 1 |

SMBus Table: Byte Count Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------------|------|---|---|---------|
| Bit 7 | | | | | | 0 |
| Bit 6 | | | | | | 0 |
| Bit 5 | | | | | | 0 |
| Bit 4 | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

Marking Diagrams



Notes:

1. "LOT" is the lot sequence number.
2. "COO" denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. "L" denotes RoHS compliant package.
6. "I" denotes industrial temperature range device.

Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|-----------|-------|-------|
| Thermal Resistance | θ_{JC} | Junction to Case | NDG48 | 33 | °C/W | 1 |
| | θ_{Jb} | Junction to Base | | 2.1 | °C/W | 1 |
| | θ_{JA0} | Junction to Air, still air | | 37 | °C/W | 1 |
| | θ_{JA1} | Junction to Air, 1 m/s air flow | | 30 | °C/W | 1 |
| | θ_{JA3} | Junction to Air, 3 m/s air flow | | 27 | °C/W | 1 |
| | θ_{JA5} | Junction to Air, 5 m/s air flow | | 26 | °C/W | 1 |

¹ePad soldered to board

Package Outline and Dimensions (NDG48)

| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 5/18/16 | JH |

| SYMBOL | DIMENSION | | |
|------------------------------|------------------|------|------|
| | MIN | NOM | MAX |
| D2 | 3.95 | 4.10 | 4.20 |
| E2 | 3.95 | 4.10 | 4.20 |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.55 REF | | |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| e | 0.40 BSC | | |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | --- 0.20 REF --- | | |
| N | 48 | | |
| ND | 12 | | |
| NE | 12 | | |
| b | 0.15 | 0.20 | 0.25 |
| TOLERANCE of FORM & POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.07 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

TOLERANCES UNLESS SPECIFIED

DECIMAL ±1%

ANGULAR ±1°

X±

XX±

XXX±

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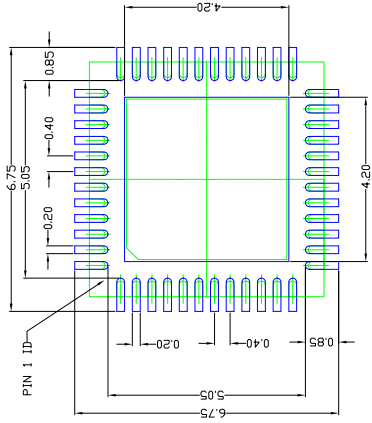
| APPROVALS | DATE | TITLE |
|-----------------|----------|-----------------------------------|
| DRAWN ϕ AC | 01/11/08 | ND/NDG 48 PACKAGE OUTLINE |
| CHECKED | | 6.0 x 6.0 mm BODY, EPAD 4.10mm SQ |
| | | 0.40 mm PITCH VFQFN |
| | | SIZE DRAWING No. |
| | | C PSC-4212-01 |
| | | REV 00 |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N REFERS TO THE NUMBER OF LEADS.
4. ND AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

Package Outline and Dimensions (NDG48), cont.

| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 5/18/16 | JH |



RECOMMENDED LAND PATTERN DIMENSION

- NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. TOP DOWN VIEW, AS VIEWED ON PCB.
 3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
 4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
 5. LAND PATTERN RECOMMENDATION PER IPC-7351B. GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | |
|-----------------------------|--|-----------------------------------|--------------|
| TOLERANCES UNLESS SPECIFIED | 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 | | |
| DECIMAL | ±0.1 | | |
| X± | | | |
| XX± | | | |
| XXX± | | | |
| APPROVALS | DATE | TITLE | REV |
| DRAWN <i>024C</i> | 01/11/08 | NDG48 PACKAGE OUTLINE | 00 |
| CHECKED | | 6.0 x 6.0 mm BODY, EPAD 4.10mm SQ | |
| | | 0.40 mm PITCH VFQFN | |
| | | DRAWING No. | |
| | | C | PSC-4212-01 |
| | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|---------------|---------------|
| 9DBV0941AKLF | Trays | 48-pin VFQFPN | 0 to +70° C |
| 9DBV0941AKLFT | Tape and Reel | 48-pin VFQFPN | 0 to +70° C |
| 9DBV0941AKILF | Trays | 48-pin VFQFPN | -40 to +85° C |
| 9DBV0941AKILFT | Tape and Reel | 48-pin VFQFPN | -40 to +85° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|------|-----------|------------|---|------------|
| A | RDW | 8/27/2014 | <ol style="list-style-type: none"> Updated front page text. Updated block diagram. Updated electrical tables. Updated test loads diagrams. Updated Smbus byte 2, 3 and 6 labeling. Functionality did not change. Updated min Vhigh on DIF outputs from 630mV to 660mV, correcting a typo. Corrected Conditions for Slew Rate in DIF Low-Power HCSL Outputs. Added additive phase jitter image. Move to final. | Various |
| B | RDW | 8/28/2014 | <ol style="list-style-type: none"> Corrected Supply Voltage in Absolute Maximum Ratings. Lowered additive phase jitter specs. | Various |
| C | RDW | 3/28/2016 | <ol style="list-style-type: none"> Revised front page text extensively. Added note about Spread Spectrum Compatibility to the features. Change pin name of VDDA1.8 to VDD1.8 and GNDA to GND to clarify that this part does not have a PLL. This is a document change only. There is no silicon change. Corrected OE8# to indicate an internal pull down, not a pull up. Added epad nomenclature to DS Updated package drawing to latest version - no package change. Added reference to AN-891. Updated "Current Consumption" table to remove references to VDDA1.8 Added "RMS additive phase jitter: 251fs" to phase noise plot Updated "Clock Input Parameters" table for consistency - no silicon change. Updated "Output Duty Cycle, Jitter, Skew and PLL Characteristics" and "Phase Jitter" tables to remove references to bypass mode. | 1-5,7-9 14 |
| D | RDW | 3/14/2017 | <ol style="list-style-type: none"> Removed "...bypass mode." reference in note 3 under Output Duty Cycle table. Corrected spelling errors/typos. Change VDDA to VDDO1.8 in Current Consumption table. Update Additive Phase Jitter conditions for PCIe Gen3. Updated package outline drawings. | 8,9,15,16 |



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