

THC63LVD1022

30Bit Color/150Mpps Dual-Link LVDS to LVCMOS converter

General Description

The THC63LVD1022 LVDS (Low Voltage Differential Signaling) converter is designed to support pixel data transmission between Host and Flat Panel Display up to Full-HD 1080p resolutions.

The THC63LVD1022 receives dual channel LVDS data stream and transmits LVTTTL/LVCMOS data through Dual Pixel Link Input / Single Link output conversion.

At a transmit data of 150Mpixel/sec, 30bits/pixel and 5bits of timing and control data (HSYNC, VSYNC, DE) are received at an effective rate of 525Mbps per LVDS channel.

Application

- Security Camera / Industrial Camera
- Medium and Small Size Panel
- Tablet PC / Notebook PC
- Multi Function Printer
- Industrial Equipment
- Medical Equipment Monitor

Features

- 20MHz to 75MHz 30bits/pixel dual-Link LVDS input
- Up to 150MHz 30bit s/pixel single port LVCMOS output
- Operating Temperature Range : 0 to 85°C
- LVDS input skew margin: ± 400 ps at 75MHz
- Dual input / Single output mode [clkout = 2x clkin]
- Output Enable / Disable mode supported
- No Special Start-up Sequence Required
- 100pin TQFP Package
- 3.3V single voltage power supply.
- PLL requires no external components.
- Environmental laws and regulations compliance (ex. EU RoHS)

Block Diagram

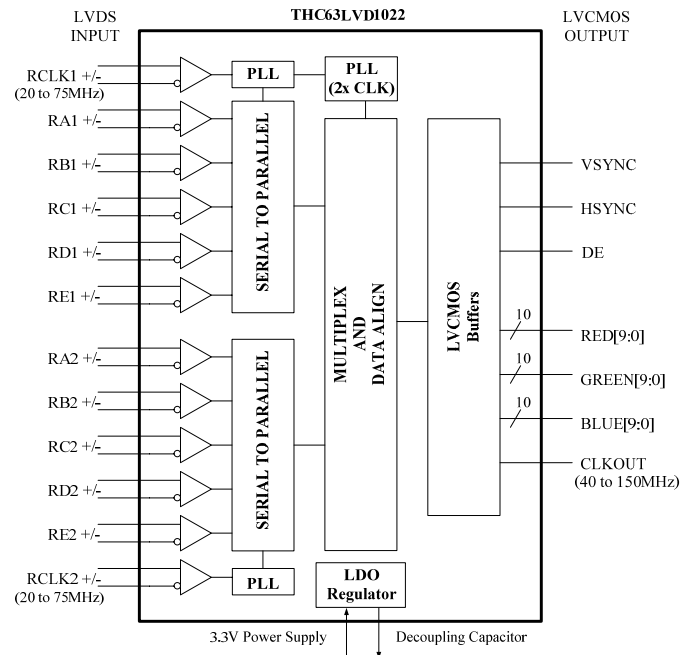


Figure 1. Block Diagram

Pin Diagram

THC63LVD1022

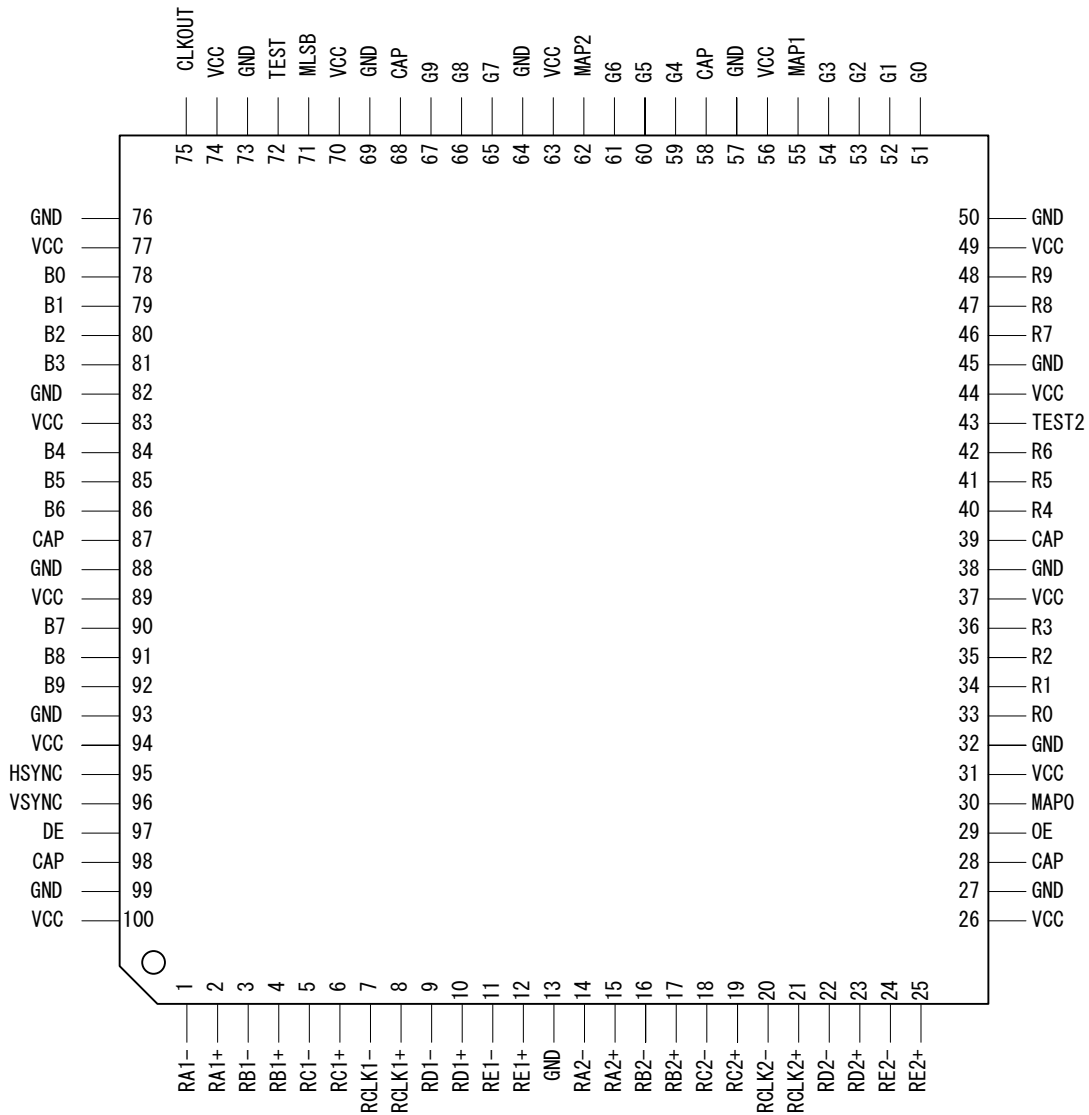


Figure 2. Pin Diagram

Pin Description

| Pin Name | Pin # | Direction | Type | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|------------|---|----------|--|--|--|-----|-----|-----|-----|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|
| RA1+, RA1- | 2, 1 | Input | LVDS | LVDS 1st Link Data In. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RB1+, RB1- | 4, 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RC1+, RC1- | 6, 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RD1+, RD1- | 10, 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RE1+, RE1- | 12, 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RCLK1+,RCLK1- | 8, 7 | | | LVDS Clock Input for 1st Link. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RA2+, RA2- | 15, 14 | | | LVDS 2nd Link Data In. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RB2+, RB2- | 17, 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RC2+, RC2- | 19, 18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RD2+, RD2- | 23, 22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RE2+, RE2- | 25, 24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RCLK2+,RCLK2- | 21, 20 | | | LVDS Clock Input for 2nd Link. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TEST, TEST2 | 72, 43 | | | Reserved L: Normal Operation (Table. 10) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| OE | 29 | | | Output Enable H: Normal Operation L: Fix Output signals(Hold the previous logic value) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MLSB | 71 | | | Output bit order selection H: MSB = 9 / LSB = 0 L: MSB = 0 / LSB = 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MAP2 ~ 0 | 62, 55, 30 | Output color mapping selection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th rowspan="2">MAP0:1:2</th> <th colspan="3">RGB</th> </tr> <tr> <th>Rch</th> <th>Gch</th> <th>Bch</th> </tr> </thead> <tbody> <tr> <td>HHH</td> <td>R</td> <td>G</td> <td>B</td> </tr> <tr> <td>HHL</td> <td>R</td> <td>B</td> <td>G</td> </tr> <tr> <td>HLH</td> <td>B</td> <td>R</td> <td>G</td> </tr> <tr> <td>HLL</td> <td>B</td> <td>G</td> <td>R</td> </tr> <tr> <td>LHH</td> <td>G</td> <td>R</td> <td>B</td> </tr> <tr> <td>LHL</td> <td>G</td> <td>B</td> <td>R</td> </tr> <tr> <td>LLH</td> <td>R</td> <td>G</td> <td>B</td> </tr> <tr> <td>LLL</td> <td>R</td> <td>G</td> <td>B</td> </tr> </tbody> </table> | MAP0:1:2 | RGB | | | Rch | Gch | Bch | HHH | R | G | B | HHL | R | B | G | HLH | B | R | G | HLL | B | G | R | LHH | G | R | B | LHL | G | B | R | LLH | R | G | B | LLL | R | G | B |
| MAP0:1:2 | RGB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Rch | Gch | Bch | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HHH | R | G | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HHL | R | B | G | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HLH | B | R | G | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HLL | B | G | R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LHH | G | R | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LHL | G | B | R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LLH | R | G | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LLL | R | G | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | LVTTL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 1. Pin Description

Pin Description (Continued)

| Pin Name | Pin # | Direction | Type | Description |
|----------|--|-----------|--------|---|
| DE | 97 | Output | LVCMOS | Data Enable Output |
| VSYNC | 96 | | | Vsync Output |
| HSYNC | 95 | | | Hsync Output |
| R9 ~ 0 | 48, 47, 46, 42, 41, 40, 36, 35, 34, 33 | | | Pixel Data Output(Rch) |
| G9 ~ 0 | 67, 66, 65, 61, 60, 59, 54, 53, 52, 51 | | | Pixel Data Output(Gch) |
| B9 ~ 0 | 92, 91, 90, 86, 85, 84, 81, 80, 79, 78 | | | Pixel Data Output(Bch) |
| CLKOUT | 75 | | | Clock Output |
| VCC | 26, 31, 37, 44, 49, 56, 63, 70, 74, 77, 83, 89, 94, 100 | - | | Power Supply Pins |
| GND | 13, 27, 32, 38, 45, 50, 57, 64, 69, 73, 76, 82, 88, 93, 99 | | | Ground Pins |
| CAP | 28, 39, 58, 68, 87, 98 | | | Decoupling cap. External 0.1uF or more capacitance required. |

Table 2. Pin Description

Absolute Maximum Ratings

| Parameter | Min | Max | Unit |
|---------------------------|------|-----------|------|
| Supply Voltage (VCC) | -0.3 | +4.0 | V |
| LVC MOS/TTL Input Voltage | -0.3 | VCC + 0.3 | V |
| LVDS Input Pin | -0.3 | VCC + 0.3 | V |
| Junction Temperature | - | +125 | °C |
| Storage Temperature | -55 | +125 | °C |

Table 3. Absolute Maximum Rating

Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit | |
|--------|-------------------------------|----------------|-----|-----|------|-----|
| - | All Supply Voltage | 3.0 | 3.3 | 3.6 | V | |
| Ta | Operating Ambient Temperature | 0 | 25 | +85 | °C | |
| - | Clock Frequency | LVDS Input | 20 | - | 75 | MHz |
| | | LVC MOS Output | 40 | - | 150 | |

Table 4. Recommended Operating Conditions

“Absolute Maximum Ratings” are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

“Absolute Maximum Rating” values also include behavior of overshooting and undershooting.

Equivalent LVDS Input Schematic Diagram

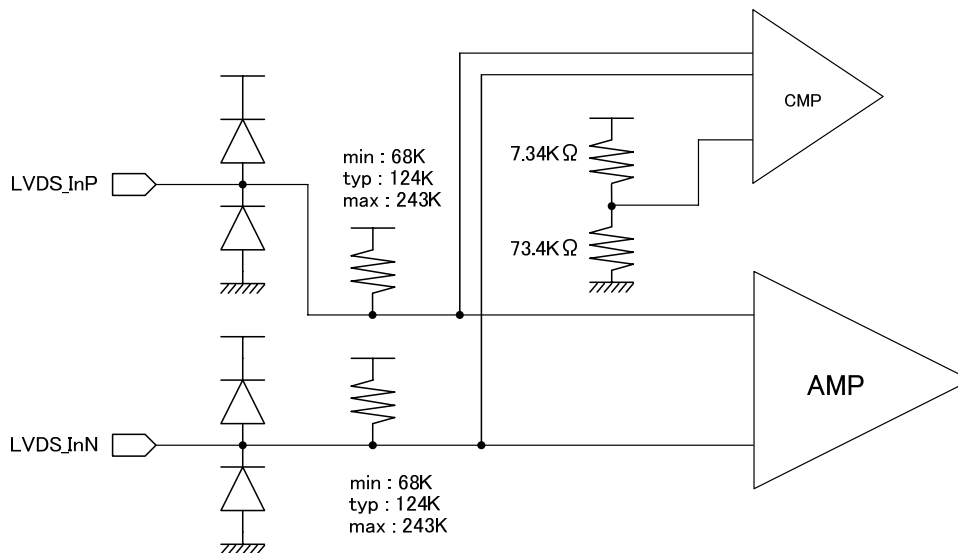


Figure 3. LVDS Input Schematic Diagram

Power Consumption

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Conditions | Typ* | Max | Unit |
|-------------------|--|-----------------------------|------|-----|------|
| I _{RCCW} | LVDS Receiver Operating Current Gray Scale Pattern (Fig.4) | RL=100Ω, CL=5pF, RCLK=75MHz | 139 | - | mA |
| | LVDS Receiver Operating Current Worst Case Pattern (Fig.5) | RL=100Ω, CL=5pF, RCLK=75MHz | - | - | mA |

* Typ values are at the conditions of VCC=3.3V and Ta = +25°C

Table 5. Power Consumption

Grayscale Pattern

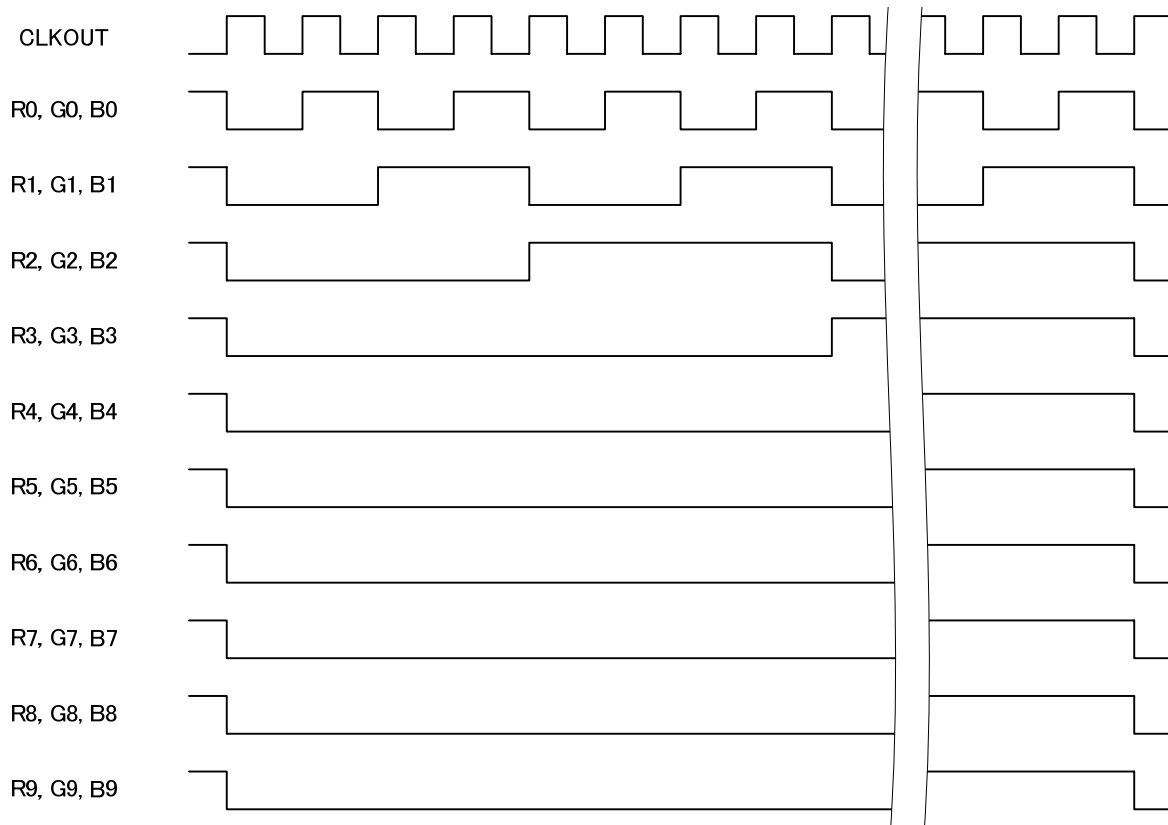


Figure 4. Grayscale Pattern

Worst Case Pattern

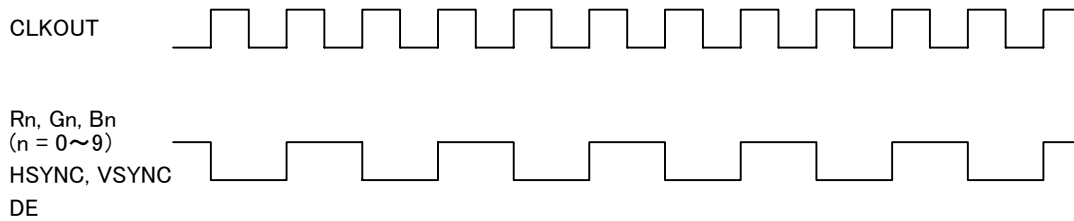


Figure 5. Worst Case Pattern

Electrical Characteristics

LVC MOS/TTL DC Specifications

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ* | Max | Unit |
|-----------------|---------------------------|--|-----|------|-----|------|
| V _{IH} | High Level Input Voltage | RS=VCC or GND | 2.0 | - | VCC | V |
| V _{IL} | Low Level Input Voltage | RS=VCC or GND | GND | - | 0.8 | V |
| VOH | High Level Output Voltage | I _{OH} =12mA(Data), 16mA(Clk) | 2.4 | - | - | V |
| VOL | Low Level Output Voltage | I _{OH} =12mA(Data), 16mA(Clk) | - | - | 0.4 | V |
| I _{IL} | Input Leakage Current | | - | - | ±1 | μA |
| P _D | Power Dissipation | | - | 0.46 | - | W |

*Typ values are at the conditions of VCC=3.3V and Ta = +25°C

Table 6. LVC MOS/TTL DC Specifications

LVDS Receiver DC Specifications

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ* | Max | Unit |
|---------------------|-----------------------------------|------------------------|------|------|-----|------|
| V _{IC} | Differential Input Common Voltage | | 0.6 | 1.2 | 1.8 | V |
| V _{ID} | Differential Voltage | | 100 | - | 600 | mV |
| V _{TH} | Differential Input High Threshold | V _{IC} = 1.2V | - | - | 100 | mV |
| V _{TL} | Differential Input Low Threshold | V _{IC} = 1.2V | -100 | - | - | mV |
| I _{INLVDS} | LVDS Input Current | | - | - | ±20 | μA |

*Typ values are at the conditions of VCC=3.3V and Ta = +25°C

Table 7. LVDS Receiver DC Specifications

LVC MOS/TTL & LVDS Receiver AC Specifications

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Unit | |
|-------------------|------------------------------|--|----------------------|--|------|----|
| t _{RCP} | CLK Period | RCLK1/2 | 13.3 | - | 50 | ns |
| | | CLKOUT | 6.6 | - | 25 | |
| t _{RCH} | CLKOUT High Time | 2/7 T _{RCP} | 4/7 T _{RCP} | 5/7 T _{RCP} | ns | |
| t _{RCL} | CLKOUT Low Time | 5/7 T _{RCP} | 3/7 T _{RCP} | 2/7 T _{RCP} | ns | |
| t _{DOUT} | LVC MOS Data OUT Period | 6.6 | - | 25 | ns | |
| t _{RS} | LVC MOS Data Setup to CLKOUT | 2.0 | - | 4.6 | ns | |
| t _{RH} | LVC MOS Data Hold to CLKOUT | 2.0 | - | 4.6 | ns | |
| t _{SK} | Receiver Skew Margin | -400 | - | 400 | ps | |
| t _{RIP1} | Input Data Position0 | - t _{SK} | 0 | + t _{SK} | ns | |
| t _{RIP0} | Input Data Position1 | t _{RCP} /7 - t _{SK} | t _{RCP} /7 | t _{RCP} /7 + t _{SK} | ns | |
| t _{RIP6} | Input Data Position2 | 2t _{RCP} /7 - t _{SK} | 2t _{RCP} /7 | 2t _{RCP} /7 + t _{SK} | ns | |
| t _{RIP5} | Input Data Position3 | 3t _{RCP} /7 - t _{SK} | 3t _{RCP} /7 | 3t _{RCP} /7 + t _{SK} | ns | |
| t _{RIP4} | Input Data Position4 | 4t _{RCP} /7 - t _{SK} | 4t _{RCP} /7 | 4t _{RCP} /7 + t _{SK} | ns | |
| t _{RIP3} | Input Data Position5 | 5t _{RCP} /7 - t _{SK} | 5t _{RCP} /7 | 5t _{RCP} /7 + t _{SK} | ns | |
| t _{RIP2} | Input Data Position6 | 6t _{RCP} /7 - t _{SK} | 6t _{RCP} /7 | 6t _{RCP} /7 + t _{SK} | ns | |
| t _{RPLL} | Phase Lock Loop Set | - | - | 1 | ms | |

* Typ values are at the conditions of VCC=3.3V and Ta = +25°C

Table 8. LVC MOS/TTL & LVDS Receiver AC Specifications

AC Timing Diagrams

LVC MOS Output

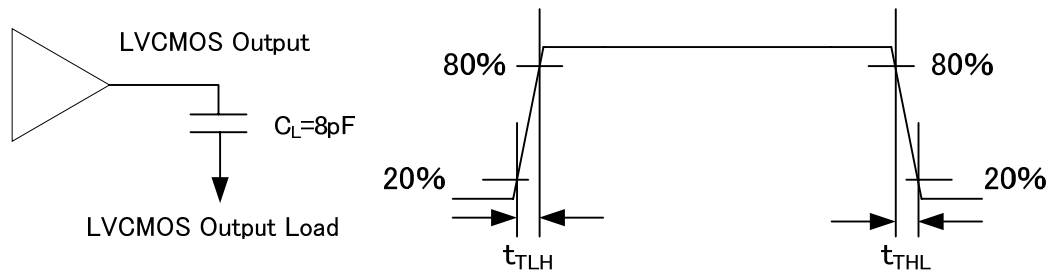


Figure 6. CLKOUT Transmission Time

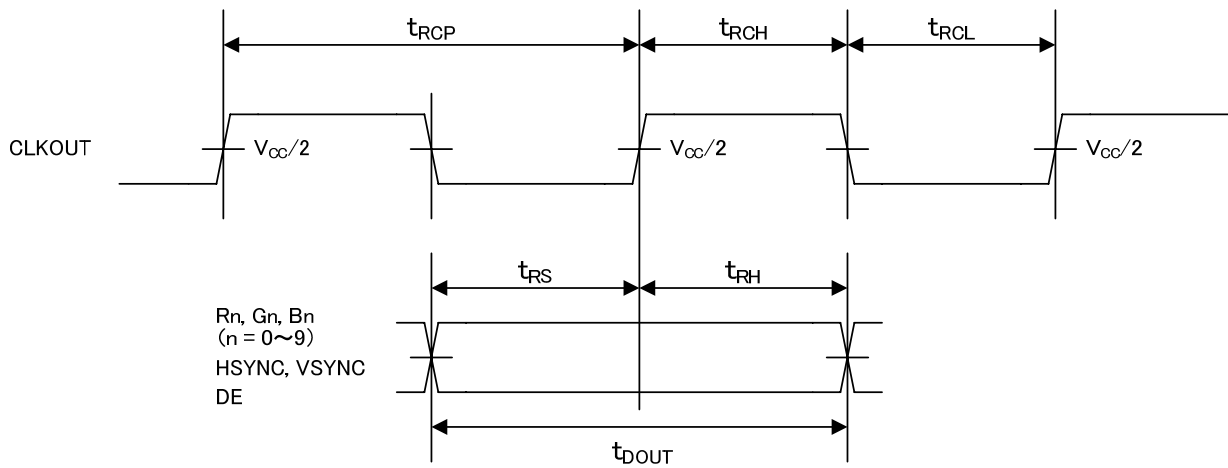


Figure 7. CLKOUT Period, High/Low Time, Setup/Hold Timing

LVDS Input Data Position

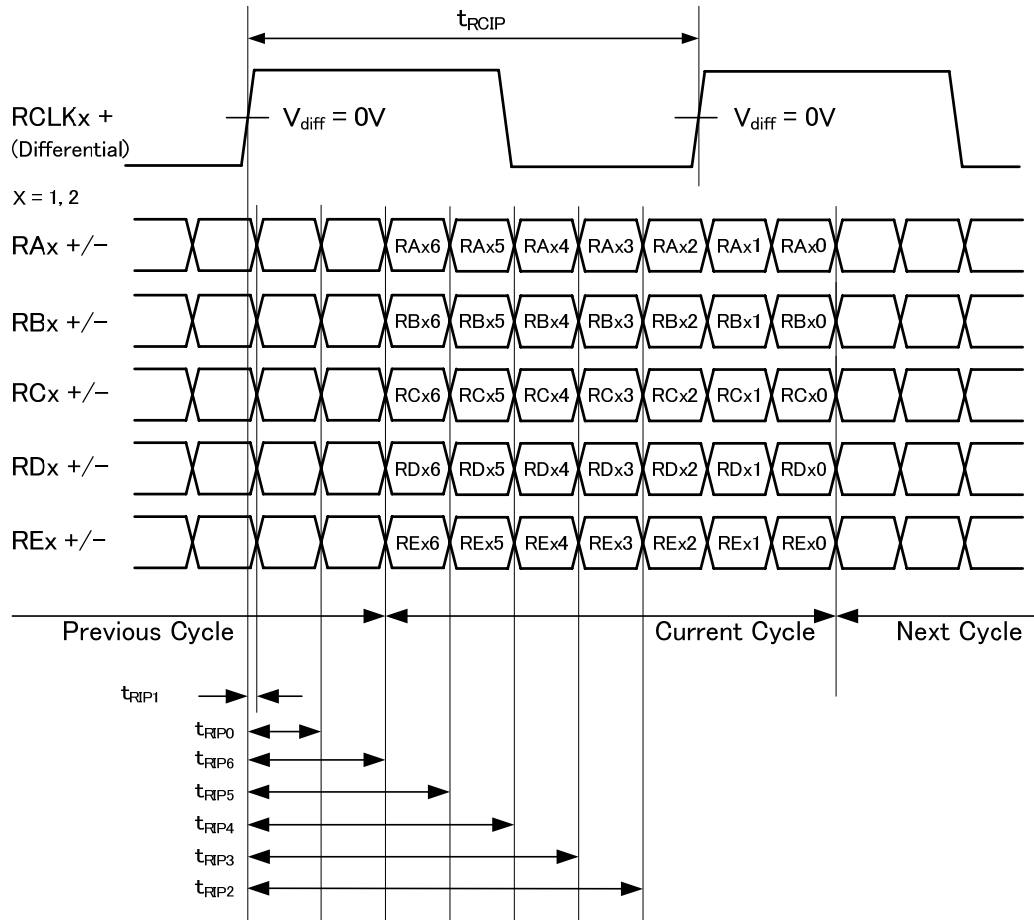


Figure 8. LVDS Input Data Position

Phase Lock Loop Set Time

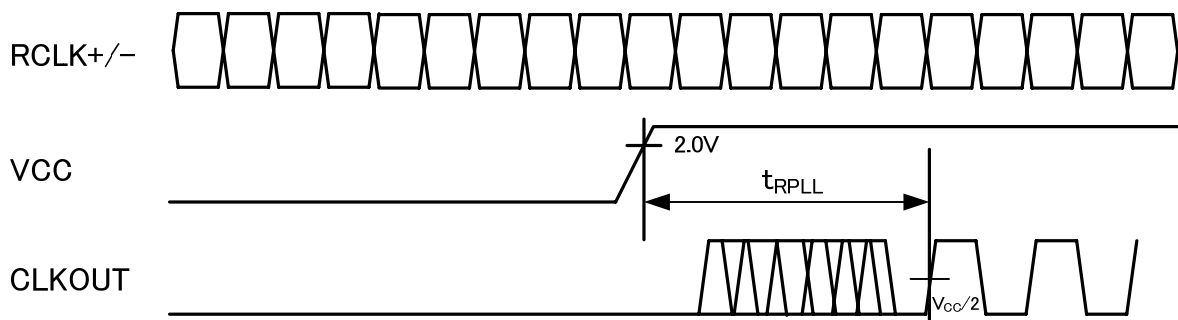


Figure 9. PLL Lock Set Time

LVDS Data Timing Diagram

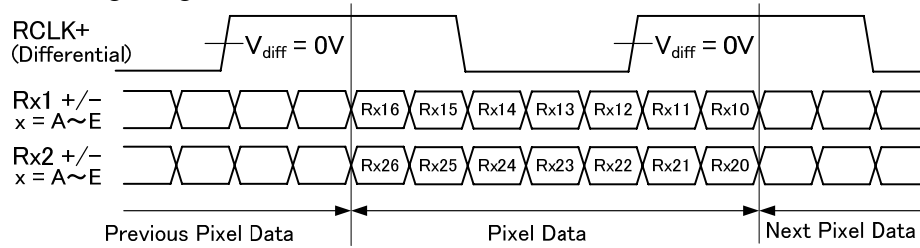


Figure 10. LVDS Data Timing Diagram

LVDS Input Data Mapping (MLSB=High, MAP[2:0]=High)

| LVDS Input Data (1 st Pixel Data) | 1 st pix data | LVDS Input Data (2 nd Pixel Data) | 2 nd pix data |
|--|--------------------------|--|--------------------------|
| RA10 | R4 (n) | RA20 | R4 (n+1) |
| RA11 | R5 (n) | RA21 | R5 (n+1) |
| RA12 | R6 (n) | RA22 | R6 (n+1) |
| RA13 | R7 (n) | RA23 | R7 (n+1) |
| RA14 | R8 (n) | RA24 | R8 (n+1) |
| RA15 | R9 (n) | RA25 | R9 (n+1) |
| RA16 | G4 (n) | RA26 | G4 (n+1) |
| RB10 | G5 (n) | RB20 | G5 (n+1) |
| RB11 | G6 (n) | RB21 | G6 (n+1) |
| RB12 | G7 (n) | RB22 | G7 (n+1) |
| RB13 | G8 (n) | RB23 | G8 (n+1) |
| RB14 | G9 (n) | RB24 | G9 (n+1) |
| RB15 | B4 (n) | RB25 | B4 (n+1) |
| RB16 | B5 (n) | RB26 | B5 (n+1) |
| RC10 | B6 (n) | RC20 | B6 (n+1) |
| RC11 | B7 (n) | RC21 | B7 (n+1) |
| RC12 | B8 (n) | RC22 | B8 (n+1) |
| RC13 | B9 (n) | RC23 | B9 (n+1) |
| RC14 | HSYNC | RC24 | - |
| RC15 | VSYNC | RC25 | - |
| RC16 | DE | RC26 | - |
| RD10 | R2 (n) | RD20 | R2 (n+1) |
| RD11 | R3 (n) | RD21 | R3 (n+1) |
| RD12 | G2 (n) | RD22 | G2 (n+1) |
| RD13 | G3 (n) | RD23 | G3 (n+1) |
| RD14 | B2 (n) | RD24 | B2 (n+1) |
| RD15 | B3 (n) | RD25 | B3 (n+1) |
| RD16 | - | RD26 | - |
| RE10 | R0 (n) | RE20 | R0 (n+1) |
| RE11 | R1 (n) | RE21 | R1 (n+1) |
| RE12 | G0 (n) | RE22 | G0 (n+1) |
| RE13 | G1 (n) | RE23 | G1 (n+1) |
| RE14 | B0 (n) | RE24 | B0 (n+1) |
| RE15 | B1 (n) | RE25 | B1 (n+1) |
| RE16 | - | RE26 | - |

Table 9. LVDS Input Data Mapping

Output Disable Mode

| Input Signal | Normal Mode Setting | Output Disable Mode Setting |
|---------------------|---------------------|-----------------------------|
| OE | H | L |
| TEST | L | H |
| TEST2 | L | L |
| MAP0 | X | H |
| MAP1 | X | H |
| MAP2 | X | H |
| Other Input Signals | X | X |

Table 10. Output Disable Mode Setting

| Output Signal | Normal Mode | Output Disable Mode |
|----------------------|------------------|---------------------|
| B9 | Normal Operation | L |
| Other Output Signals | | Hi-Z |

Table 11. Output Disable Mode Signal Definition

Typical Connection

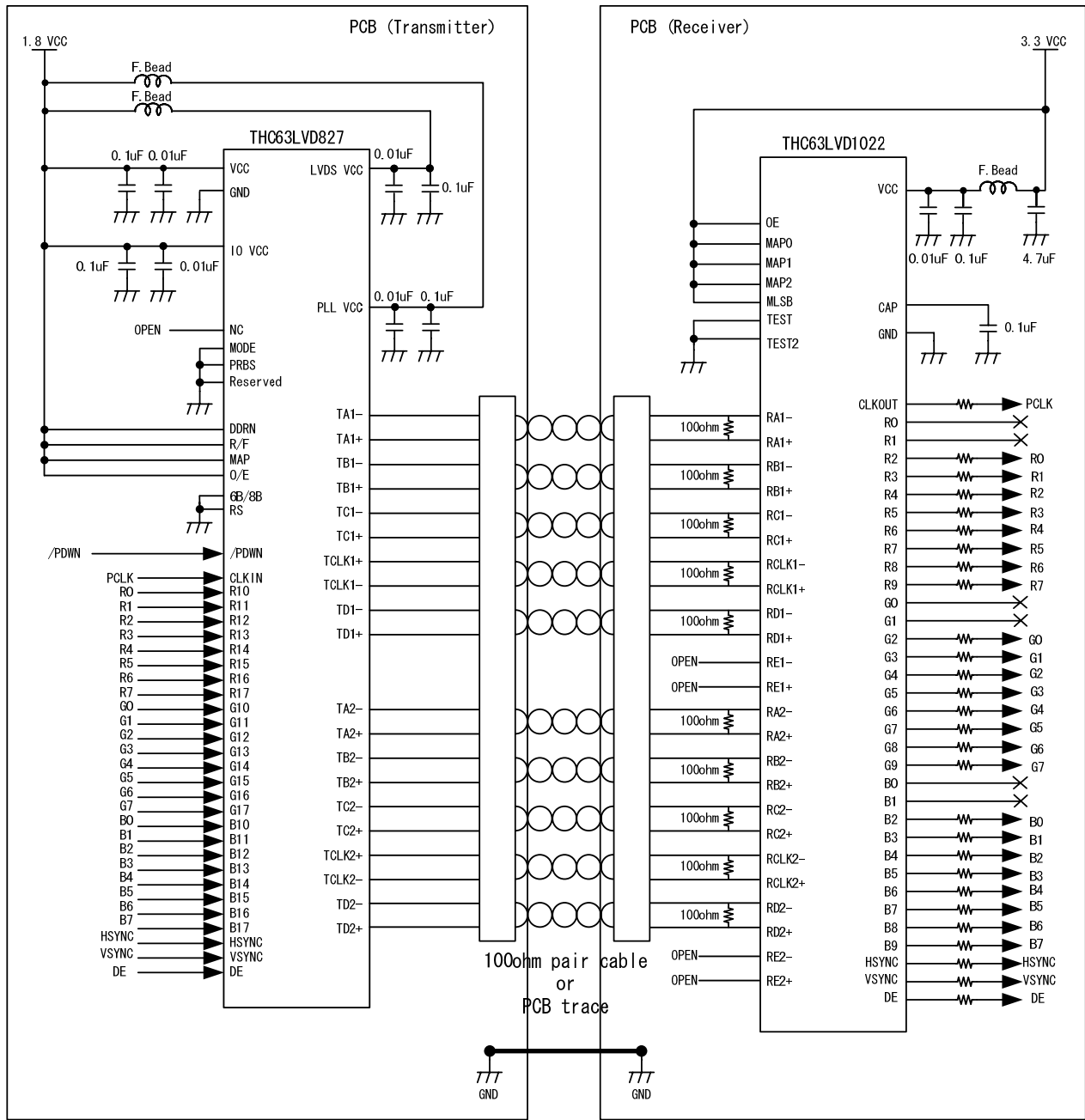


Figure 11. Typical Connection Diagram

Notes

1) Cable Connection and Disconnection

Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect each GND of the PCB which THC63LVD1022 and LVDS-Tx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3) Multi Drop Connection

Multi drop connection is not recommended.

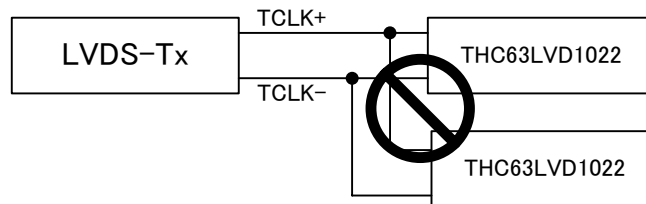


Figure 12. Multi Drop Connection

4) Asynchronous use

Asynchronous using such as following system is not recommended.

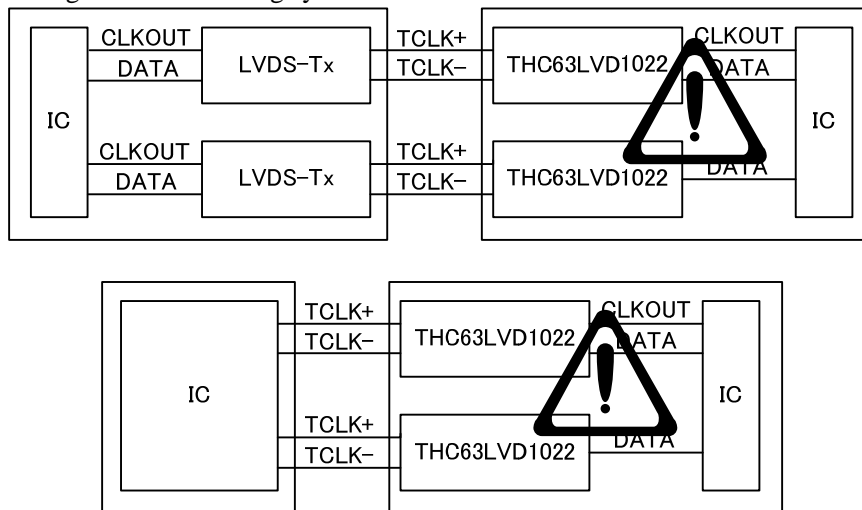


Figure 13. Asynchronous Use

Package

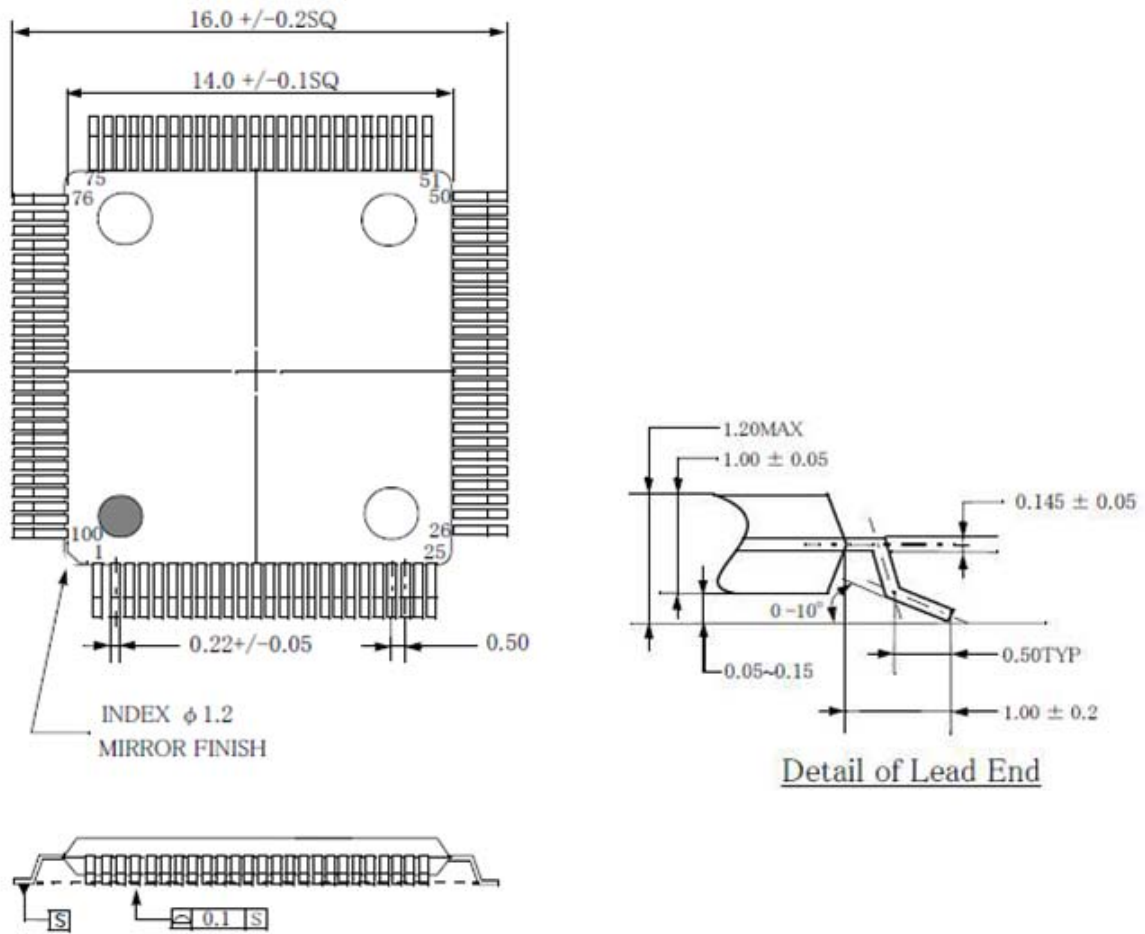


Figure 14. Package Diagram

Reference of Land Pattern

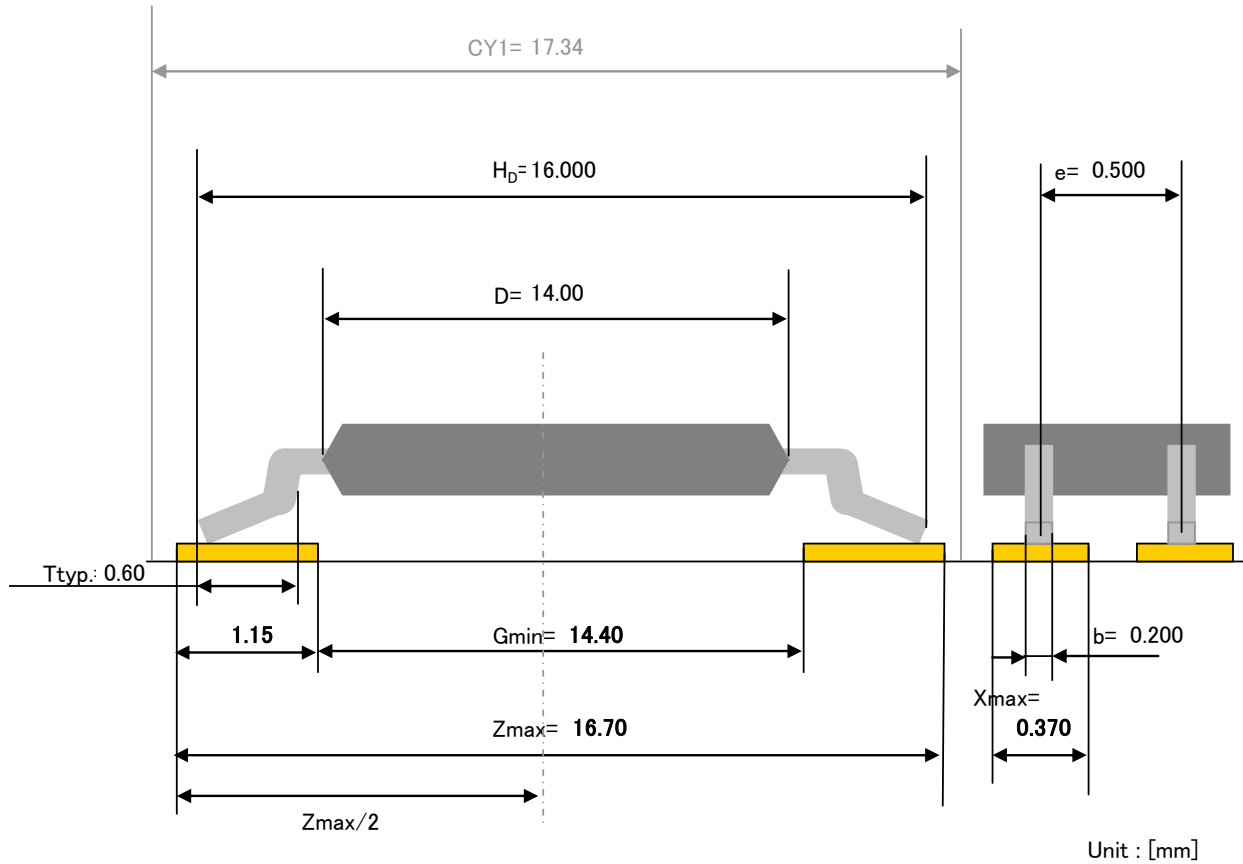


Figure 15. Reference of Land Pattern

The recommendation mounting method of THine device is reflow soldering.
The reference pattern is using the calculation result on condition of reflow soldering.

Notes

This land pattern design is a calculated value based on JEITA ET-7501.
Please take into consideration in an actual substrate design about enough the ease of mounting, the intensity of connection, the density of mounting, and the solder paste used, etc... The optimal land pattern size changes with these parameters. Please use the value shown by the land pattern as reference data.

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- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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