

## 1. General description

Passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

## 3. Applications

- General purpose switching and phase control
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances

## 4. Quick reference data

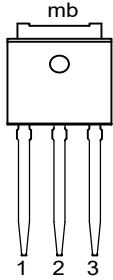

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RRM}$	repetitive peak reverse voltage		-	-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	75	A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$	-	-	82	A
$T_j$	junction temperature	<a href="#">[1]</a>	-	-	125	°C
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	50	200	μA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 100\text{ }\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	50	100	-	V/μs

[1] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p>IPAK (TO-251)</p>	 <p>sym037</p>
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT258U-600R	IPAK	plastic single-ended package (IPAK); 3 leads (in-line)	TO-251

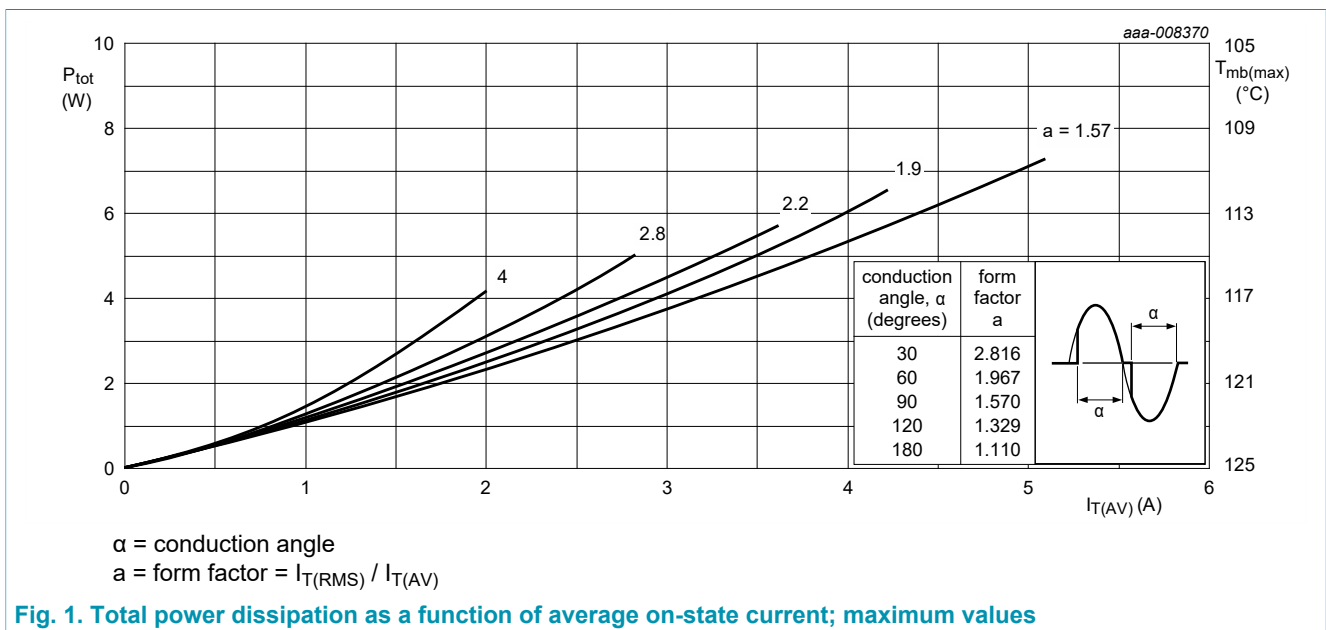
## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$V_{RRM}$	repetitive peak reverse voltage		-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 1</a>	-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	75	A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$	-	82	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	28	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_G = 1\text{ mA}$	-	50	A/ $\mu$ s
$I_{GM}$	peak gate current		-	2	A
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	°C
$T_j$	junction temperature		[1]	125	°C

[1] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.



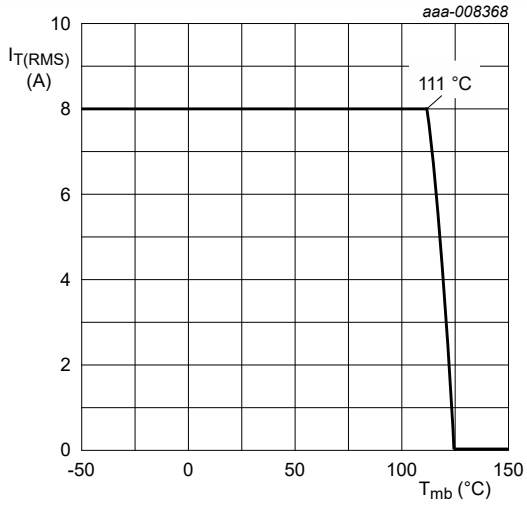
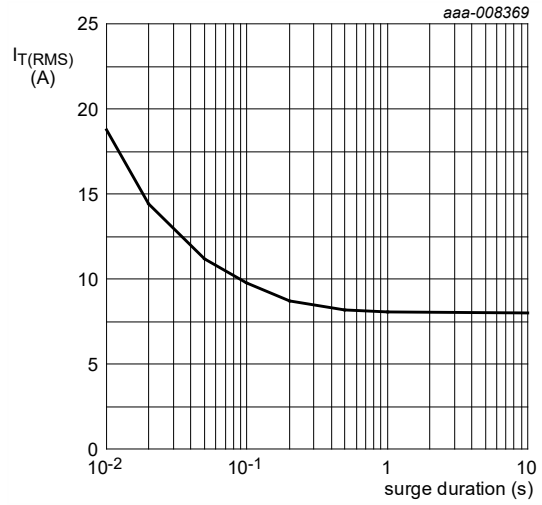


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz;  $T_{mb} = 111\text{ °C}$

Fig. 3. RMS on-state current as a function of surge duration; maximum values

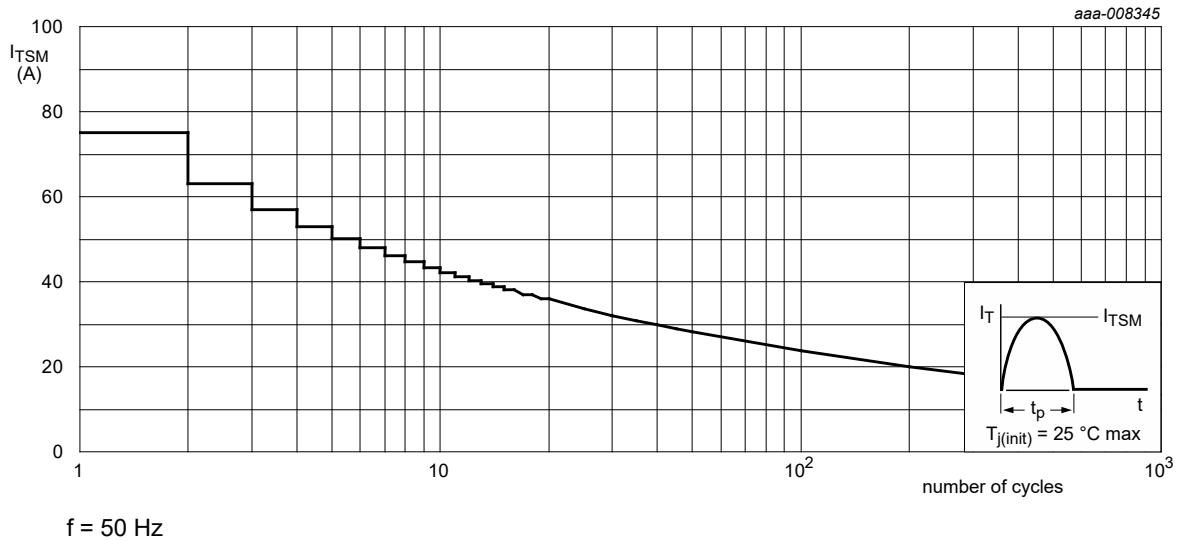
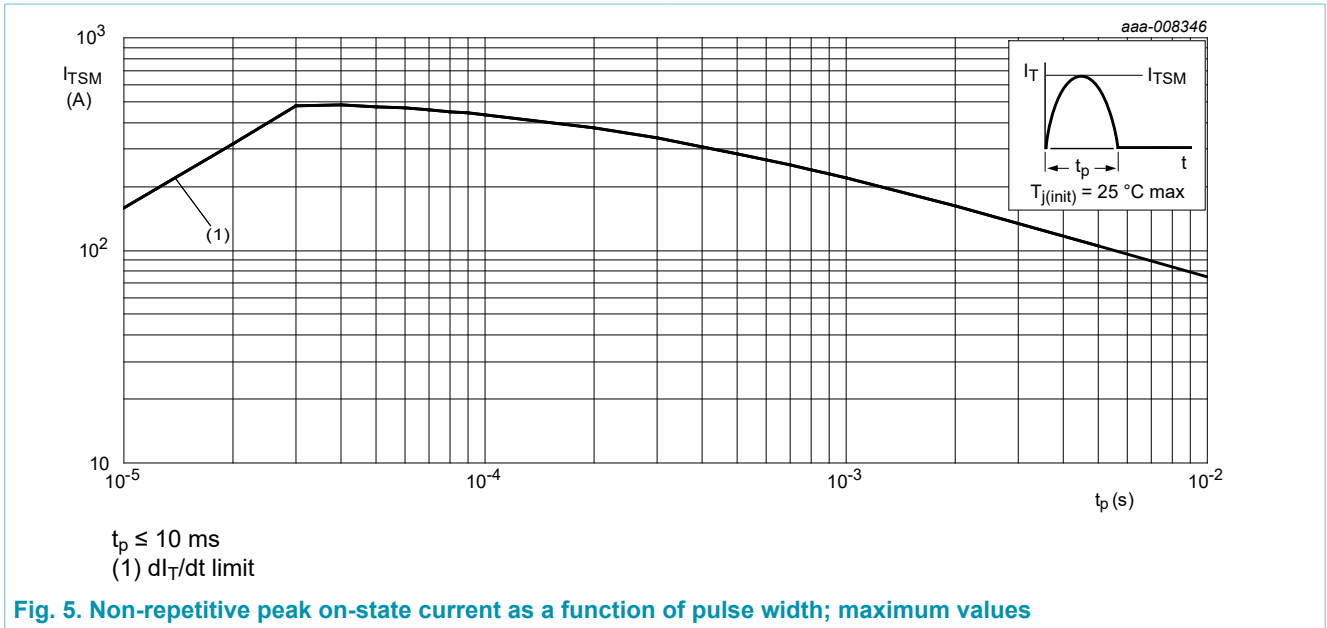


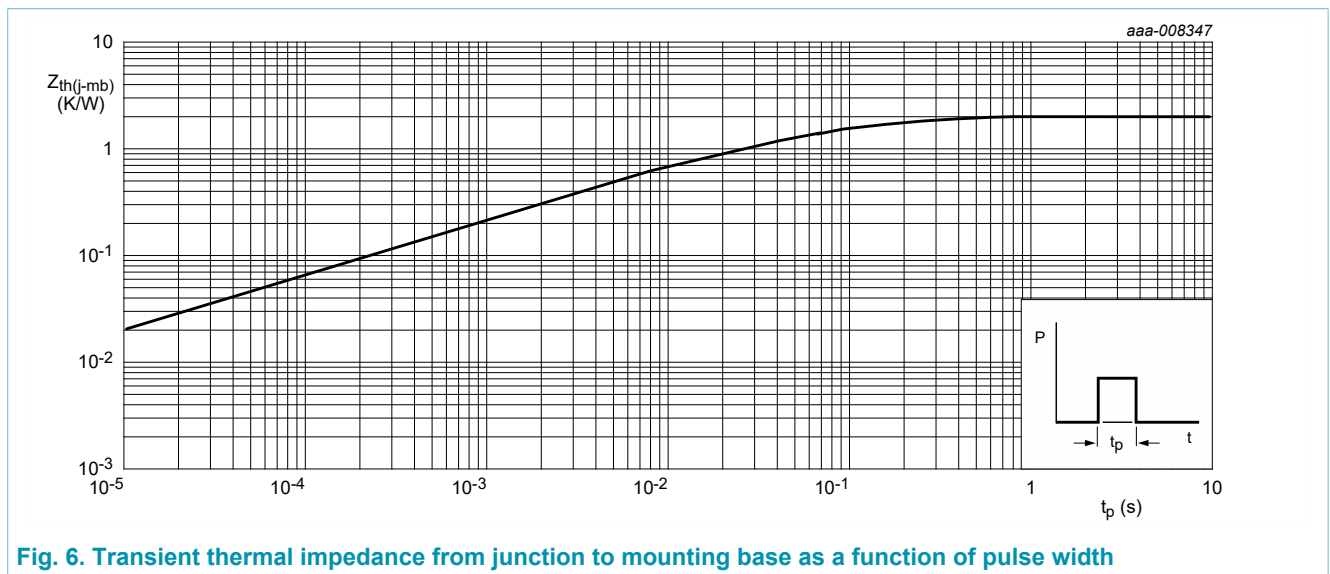
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



## 8. Thermal characteristics

Table 5. Thermal characteristics

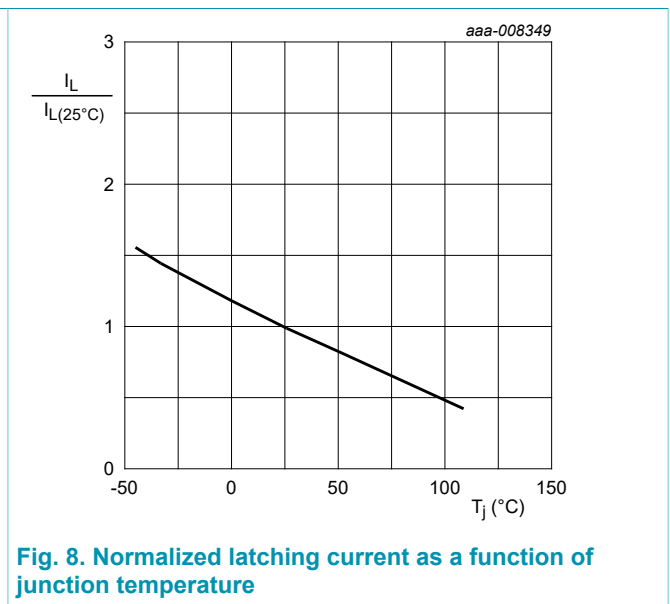
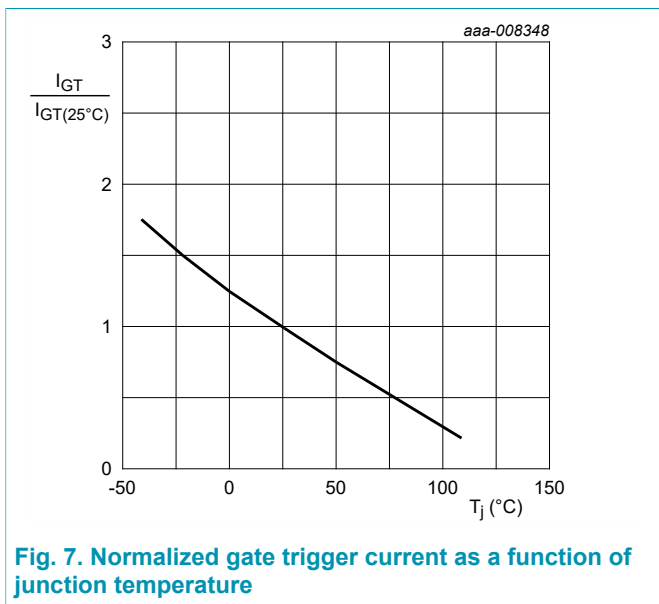
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 6</a>	-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	70	-	K/W



## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	50	200	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	0.4	10	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	0.3	6	mA
$V_T$	on-state voltage	$I_T = 16\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	1.3	1.6	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	0.4	1	V
		$V_D = 600\text{ V}; I_T = 0.1\text{ A}; T_j = 110\text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	0.1	0.2	-	V
$I_D$	off-state current	$V_D = 600\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
$I_R$	reverse current	$V_R = 600\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}; T_j = 125\text{ }^\circ\text{C}; R_{GK} = 100\text{ }\Omega;$ ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	50	100	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 10\text{ A}; V_D = 600\text{ V}; I_G = 5\text{ mA}; dI_G/dt = 0.2\text{ A}/\mu\text{s}; T_j = 25\text{ }^\circ\text{C}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 402\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{TM} = 12\text{ A}; V_R = 24\text{ V}; (dI_T/dt)_M = 10\text{ A}/\mu\text{s}; dV_D/dt = 2\text{ V}/\mu\text{s}; R_{GK(ext)} = 1\text{ k}\Omega; (V_{DM} = 67\%$ of $V_{DRM})$	-	100	-	$\mu\text{s}$



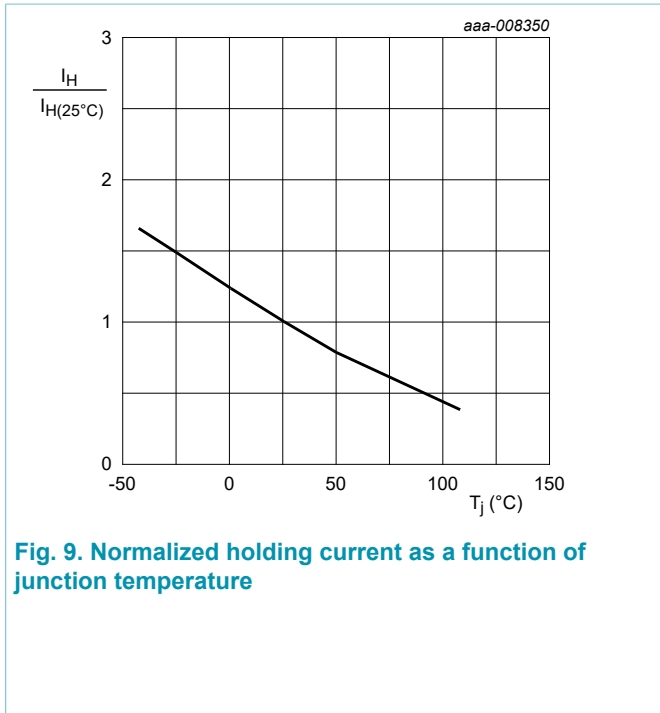


Fig. 9. Normalized holding current as a function of junction temperature

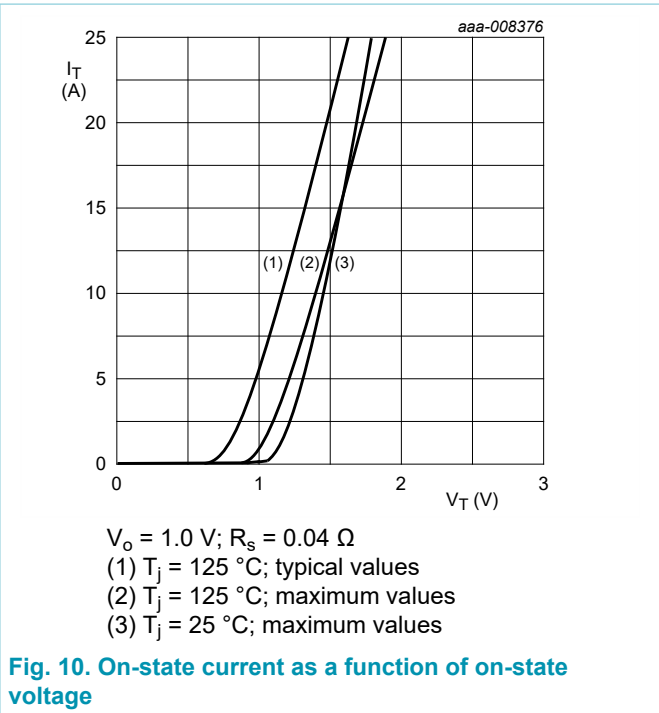


Fig. 10. On-state current as a function of on-state voltage

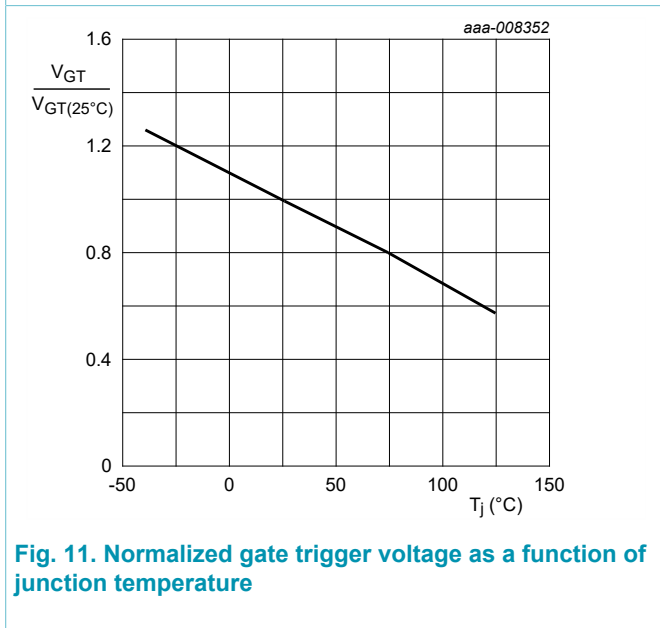


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

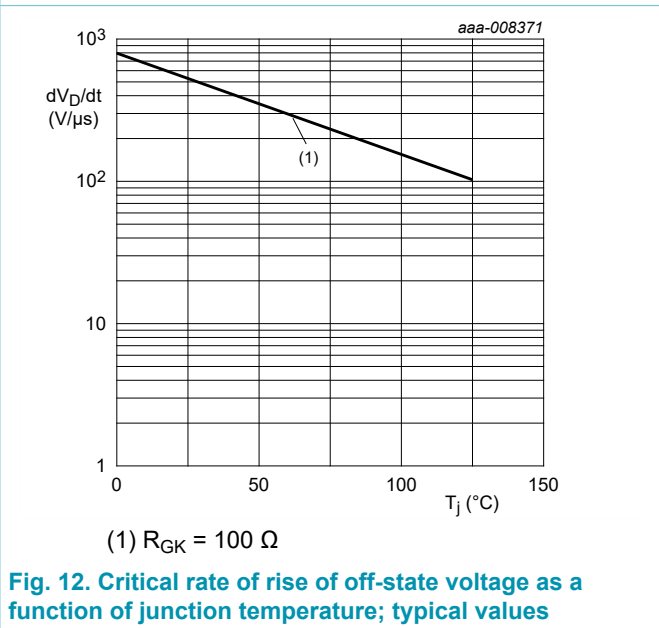


Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values



10. Package outline

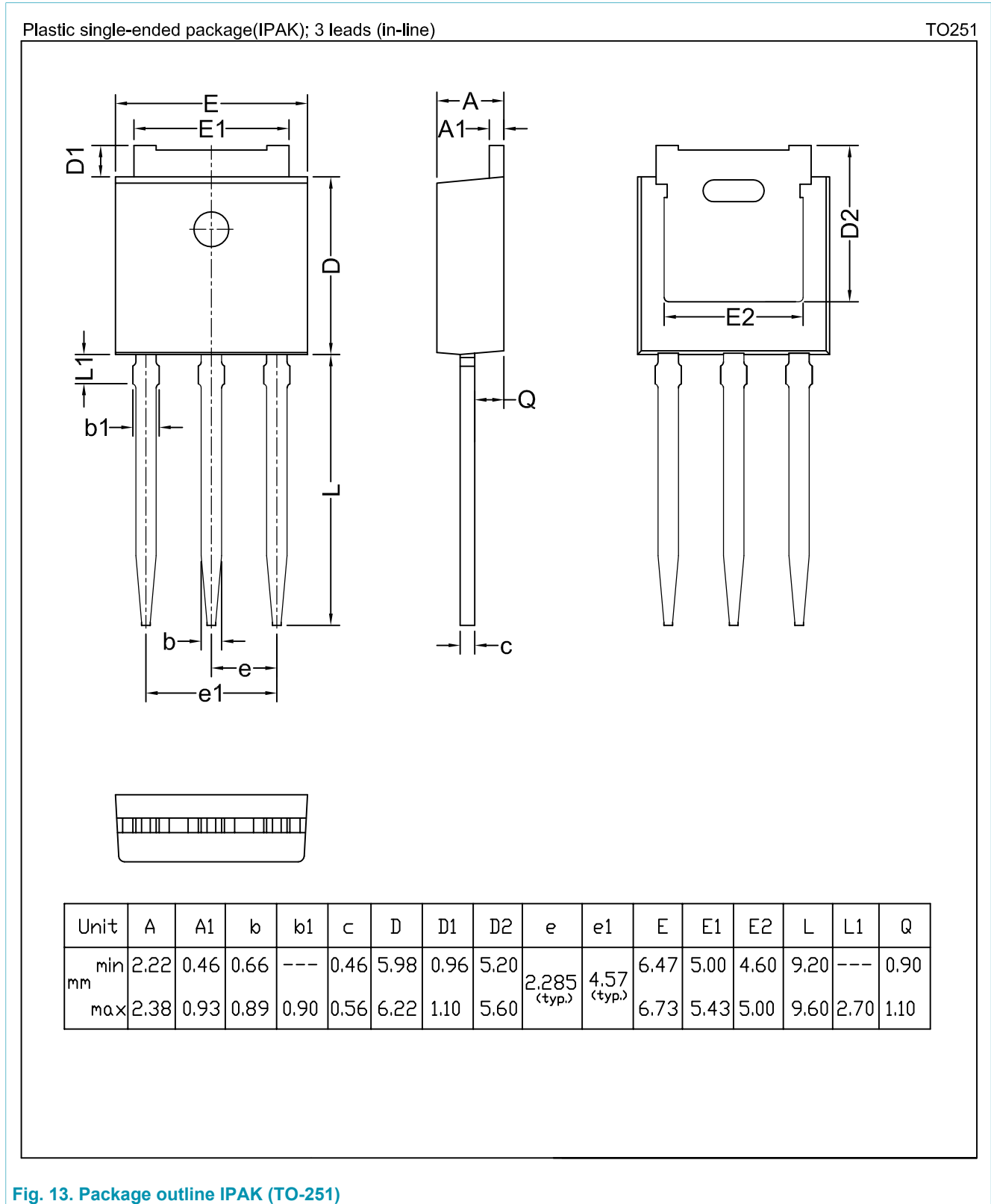


Fig. 13. Package outline IPAK (TO-251)

## 11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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