ANALOG DEVICES

Low Cost, Low Power, True RMS-to-DC Converter

Data Sheet **AD8436**

FEATURES

Delivers true rms or average rectified value of ac waveform
- **Fast settling at all input levels**
- **Accuracy: ±10 µV ± 0.25% of reading (B grade)**
- **Wide dynamic input range**
  - **100 µV rms to 3 V rms (8.5 V p-p) full-scale input range**
  - **Larger inputs with external scaling**
- **Wide bandwidth:**
  - **1 MHz for −3 dB (300 mV)**
  - **65 kHz for additional 1% error**
- **Zero converter dc output offset**
- **No residual switching products**
- **Specified at 300 mV rms input**
- **Accurate conversion with crest factors up to 10**
- **Low power: 300 µA typical at ±2.4 V**

High-Z FET separately powered input buffer
- **$R_{IN} \geq 10^{12}$ Ω, $C_{IN} \leq 2$ pF**

Precision dc output buffer

Wide power supply voltage range
- **Dual: ±2.4 V to ±18 V; single: 4.8 V to 36 V**

4 mm × 4 mm LFCSP and 8 mm × 6 mm QSOP packages

ESD protected

FUNCTIONAL BLOCK DIAGRAM

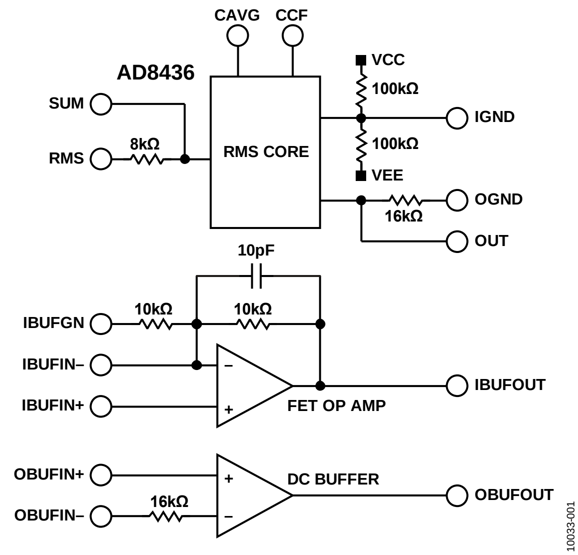

Figure 1.

GENERAL DESCRIPTION

The AD8436 is a new generation, translinear precision, low power, true rms-to-dc converter loaded with options. It computes a precise dc equivalent of the rms value of ac waveforms, including complex patterns such as those generated by switch mode power supplies and triacs. Its accuracy spans a wide range of input levels (see Figure 2) and temperatures. The ensured accuracy of ≤±0.5% and ≤10 µV output offset result from the latest Analog Devices, Inc., technology. The crest factor error is <0.5% for CF values between 1 and 10.

The AD8436 delivers true rms results at less cost than misleading peak, averaging, or digital solutions. There is no programming expense or processor overhead to consider, and the 4 mm × 4 mm package easily fits into tight applications. On-board buffer amplifiers enable the widest range of options for any rms-to-dc converter available, regardless of cost. For minimal applications, only a single external averaging capacitor is required. The built-in high impedance FET buffer provides an interface for external attenuators, frequency compensation, or driving low impedance loads. A matched pair of internal resistors enables an easily configurable gain-of-two or more, extending the usable input range even lower. The low power, precision input buffer makes the AD8436 attractive for use in portable multi-meters and other battery-powered applications.

The precision dc output buffer minimizes errors when driving low impedance loads with extremely low offset voltages, thanks to internal bias current cancellation. Unlike digital solutions, the AD8436 has no switching circuitry limiting performance at high or low amplitudes (see Figure 2). A usable response of <100 µV and >3 V extends the dynamic range with no external scaling, accommodating demanding low level signal conditions and allowing ample overrange without clipping.

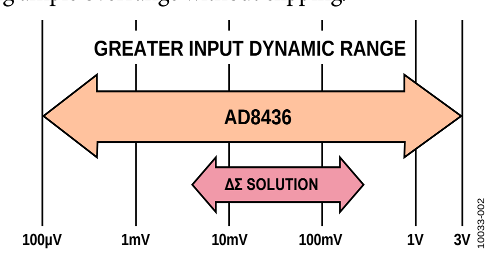

Figure 2. Usable Dynamic Range of the AD8436 vs. ΔΣ

The AD8436 operates from single or dual supplies of ±2.4 V (4.8 V) to ±18 V (36 V). A and J grades are available in a compact 4 mm × 4 mm, 20-lead chip-scale package; A and B grades are available in a 20-lead QSOP package. The operating temperature ranges are −40°C to 125°C for A and B grades and 0°C to 70°C for J grade.

Rev. B **Document Feedback**

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TABLE OF CONTENTS

REVISION HISTORY

1/13—Rev. A to Rev. B

Added B Grade Throughout ... Universal
Changes to Figure 1 and changes to General Description ... 1
Changes to Table 1 ... 3
Changes to Figure 3 ... 5
Changes to Figure 9 and Figure 10 ... 6
Changes to FET Input Buffer Section ... 11
Changes to Averaging Capacitor Considerations—RMS Accuracy Section and changes to Figure 28 ... 12
Deleted Capacitor Construction Section; added CAVG Capacitor Styles Section ... 13
Added Converting to Average Rectified Value Section ... 15
Changes to Figure 41 ... 16
Changes to Evaluation Board Section ... 17
Changes to Figure 48 ... 19
Changes to Outline Dimensions ... 20
Changes to Ordering Guide ... 21

7/12—Rev. 0 to Rev. A

Added 20-Lead QSOP ... Universal
Changes to Features Section and General Description Section ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Table 3 and added Figure 4 and added Table 4; Renumbered Sequentially ... 5
Changes to Equation 1 and change to Column One Heading in Table 5 ... 10
Changes to Averaging Capacitor Considerations—RMS Accuracy and to Post Conversion Ripple Reduction Filter and changes to Figure 27 Caption ... 12
Changes to Figure 30 to Figure 32 ... 13
Changes to Using the FET Input Buffer Section and Using the Output Buffer Section ... 14
Changes to Figure 38 and Figure 41 and added Converting to Rectified Average Value Section ... 15
Changes to Figure 41 ... 16
Changes to Figure 42 to Figure 46 ... 17
Changes to Figure 47 and Figure 48 ... 18
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 20

7/11—Revision 0: Initial Version

SPECIFICATIONS

e_{IN} = 300 mV (rms), frequency = 1 kHz sinusoidal, ac-coupled, $\pm V_S$ = ±5 V, T_A = 25°C, C_{AVG} = 10 μF, unless otherwise specified.

Table 1.

		AD8436A, AD8436J			AD8436B			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RMS CORE								
Conversion Error	Default conditions	±10 − 0.5	±0 ± 0	±10 + 0.5	±10 − 0.25	±0 ± 0	±10 + 0.25	μV/% rdg
Vs. Temperature	−40°C < T < 125 C		0.006			0.006		%/°C
Vs. Rail Voltage	±2.4 V to ±18 V		±0.013			±0.013		±%/V
Input V_{OS}	DC-coupled	−500	0	+500	−250	0	+250	μV
Output V_{OS}	AC-coupled input		0			0		V
Vs. Temperature	−40 C < T < 125°C		0.3			0.3		μV/°C
DC Reversal Error	DC-coupled, V_{IN} = ±300 mV	−1.5	0	+1.5	−1.0	0	+1.0	%
Nonlinearity	e_{IN} = 2 mV to 500 mV ac		±0.2			±0.2		%
Crest Factor Error	(Additional)							
1 < CF < 10	CCF = 0.1 μF	−0.5		+0.5	−0.5		+0.5	%
Peak Input Voltage		$-V_S$ − 0.7		$+V_S$ + 0.7	$-V_S$ − 0.7		$+V_S$ + 0.7	V
Input Resistance		7.92	8	8.08	7.92	8	8.08	kΩ
Response	V_{IN} = 300 mV rms							
1% Error	(Additional)		65			65		kHz
3 dB Bandwidth			1			1		MHz
Settling Time								
0.1%	Rising/falling		148/341			148/341		ms
0.01%	Rising/falling		158/350			158/350		ms
Output Resistance		15.68	16	16.32	15.68	16	16.32	kΩ
Supply Current	No input		325	365		325	365	μA
INPUT BUFFER								
Voltage Swing	G = 1							
Input	AC- or dc-coupled	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Output	AC-coupled to Pin RMS	$-V_S$ + 0.2		$+V_S$ − 0.2	$-V_S$ + 0.2		$+V_S$ − 0.2	mV
Offset Voltage		−1	0	+1	−0.5	0	+0.5	mV
Input Bias Current				50			50	pA
Input Resistance			10^{12}			10^{12}		Ω
Response	(Frequency)							
0.1 dB			950			950		kHz
3 dB Bandwidth			2.1			2.1		MHz
Supply Current		100	160	200	100	160	200	μA
Optional Gain Resistor		−9.9	+10	+10.1	−9.9	+10	+10.1	kΩ
Gain Error	G = ×1			0.05			0.05	%
OUTPUT BUFFER	$R_L = \infty$							
Offset Voltage	Connected to Pin OUT	−200	0	+200	−150	0	+150	μV
Input Current (I_B)			2	5[1]		2	5[1]	nA
Output Swing	(Voltage)	$-V_S + 50e^{-6}$		$+V_S$ − 1	$-V_S + 50e^{-6}$		$+V_S$ − 1	V
Output Drive Current		−0.5 (sink)		+15 (source)	−0.5 (sink)		+15 (source)	mA
Gain Error		0.003	0.01		0.003	0.01		%
Supply Current			40	70		40	70	μA
SUPPLY VOLTAGE								
Dual		±2.4		±18	±2.4		±18	V
Single		4.8		36	4.8		36	V

[1] I_B max measured at power up. Settles to typical value in <15 seconds.

ABSOLUTE MAXIMUM RATINGS

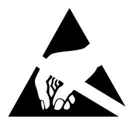
Table 2.

Parameter	Rating
Voltage	
Supply	±18 V
Input	$\pm V_S$
Differential Input	$+V_S$ and $-V_S$
Power Dissipation	
CP-20-10 LFCSP Without Thermal Pad	1.2 W
CP-20-10 LFCSP With Thermal Pad	2.1 W
RQ Package	1.1 W
Output Short-Circuit Duration	Indefinite
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +125°C
Lead Soldering (60 sec)	300°C
θ_{JA}	
CP-20-10 LFCSP Without Thermal Pad	86°C/W
CP-20-10 LFCSP With Thermal Pad	48°C/W
RQ-20 Package	95°C/W
ESD Rating	2 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

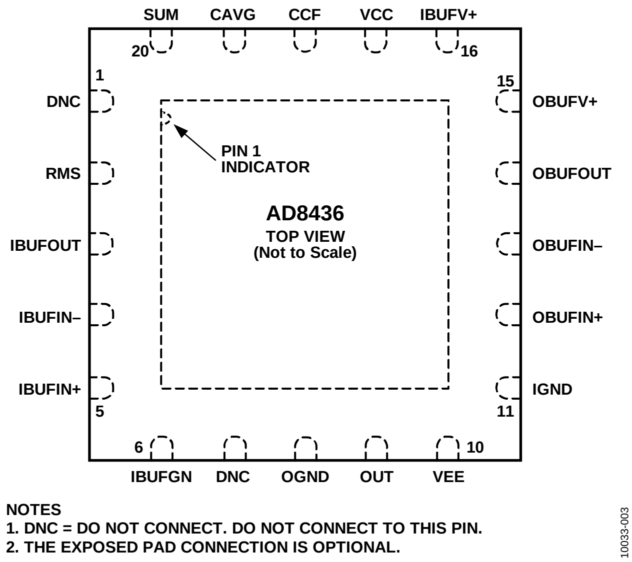


Figure 3. Pin Configuration, Top View, CP-20-10

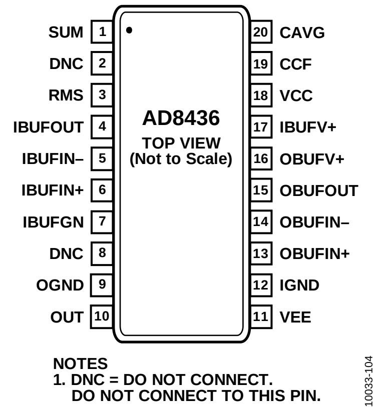


Figure 4. Pin Configuration, RQ-20

Table 3. Pin Function Descriptions, CP-20-10

Pin No.	Mnemonic	Description
1	DNC	Do Not Connect. Used for factory test.
2	RMS	AC Input to the RMS Core.
3	IBUFOUT	FET Input Buffer Output Pin.
4	IBUFIN–	FET Input Buffer Inverting Input Pin.
5	IBUFIN+	FET Input Buffer Noninverting Input Pin.
6	IBUFGN	Optional 10 kΩ Precision Gain Resistor.
7	DNC	Do Not Connect. Used for factory test.
8	OGND	Internal 16 kΩ I-to-V Resistor.
9	OUT	RMS Core Voltage or Current Output.
10	VEE	Negative Supply Rail.
11	IGND	Half Supply Node.
12	OBUFIN+	Output Buffer Noninverting Input Pin.
13	OBUFIN–	Output Buffer Inverting Input Pin.
14	OBUFOUT	Output Buffer Output Pin.
15	OBUFV+	Power Pin for the Output Buffer.
16	IBUFV+	Power Pin for the Input Buffer.
17	VCC	Positive Supply Rail for the RMS Core.
18	CCF	Connection for Crest Factor Capacitor.
19	CAVG	Connection for Averaging Capacitor.
20	SUM	Summing Amplifier Input Pin.
EP	DNC	Exposed Pad Connection to Ground Pad Optional.

Table 4. Pin Function Descriptions, RQ-20

Pin No.	Mnemonic	Description
1	SUM	Summing Amplifier Input Pin.
2	DNC	Do Not Connect. Used for factory test.
3	RMS	AC Input to the RMS Core.
4	IBUFOUT	FET Input Buffer Output Pin.
5	IBUFIN–	FET Input Buffer Inverting Input Pin.
6	IBUFIN+	FET Input Buffer Noninverting Input Pin.
7	IBUFGN	Optional 10 kΩ Precision Gain Resistor.
8	DNC	Do Not Connect. Used for factory test.
9	OGND	Internal 16 kΩ I-to-V Resistor.
10	OUT	RMS Core Voltage or Current Output.
11	VEE	Negative Supply Rail.
12	IGND	Half Supply Node.
13	OBUFIN+	Output Buffer Noninverting Input Pin.
14	OBUFIN–	Output Buffer Inverting Input Pin.
15	OBUFOUT	Output Buffer Output Pin.
16	OBUFV+	Power Pin for the Output Buffer.
17	IBUFV+	Power Pin for the Input Buffer.
18	VCC	Positive Supply Rail for the RMS Core.
19	CCF	Connection for Crest Factor Capacitor.
20	CAVG	Connection for Averaging Capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $\pm V_S$ = ±5 V, C_{AVG} = 10 µF, 1 kHz sine wave, unless otherwise indicated.

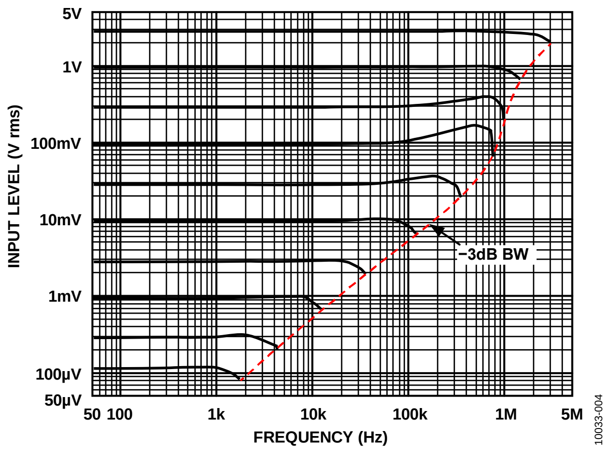


Figure 5. RMS Core Frequency Response (See Figure 21)

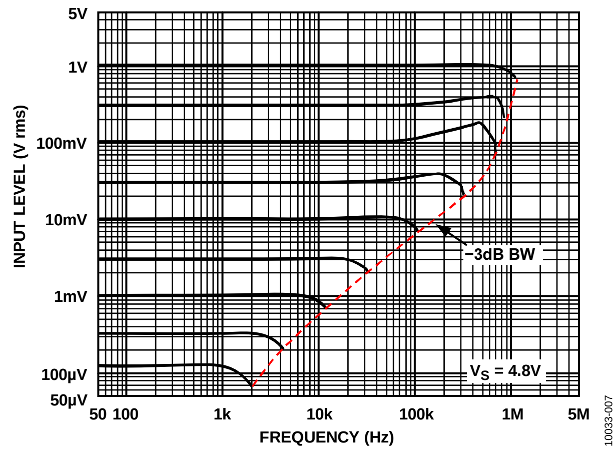


Figure 8. RMS Core Frequency Response with V_S = +4.8 V (See Figure 22)

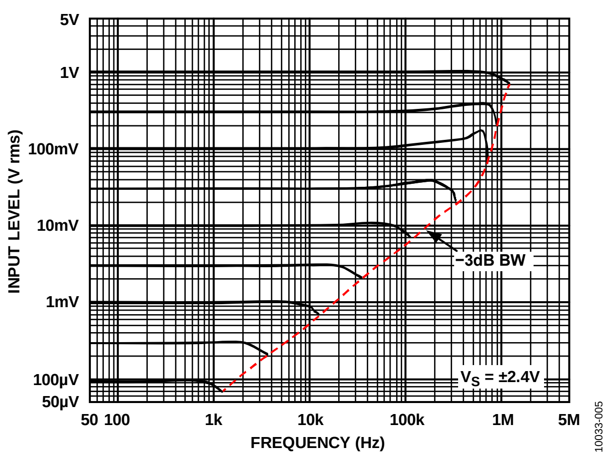


Figure 6. RMS Core Frequency Response with V_S = ±2.4 V (See Figure 21)

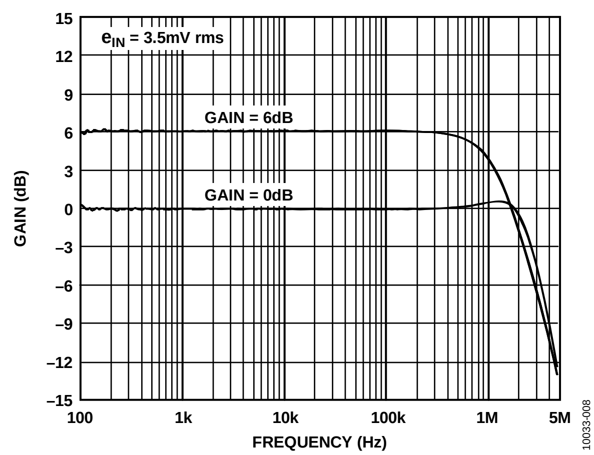


Figure 9. Input Buffer, Small Signal Bandwidth at 0 dB and 6 dB Gain

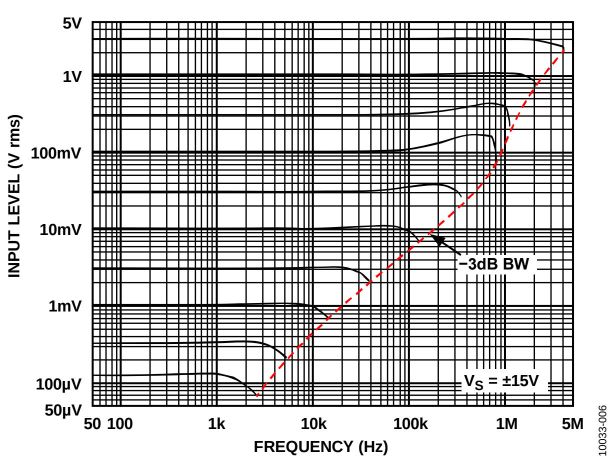


Figure 7. RMS Core Frequency Response with V_S = ±15 V (See Figure 21)

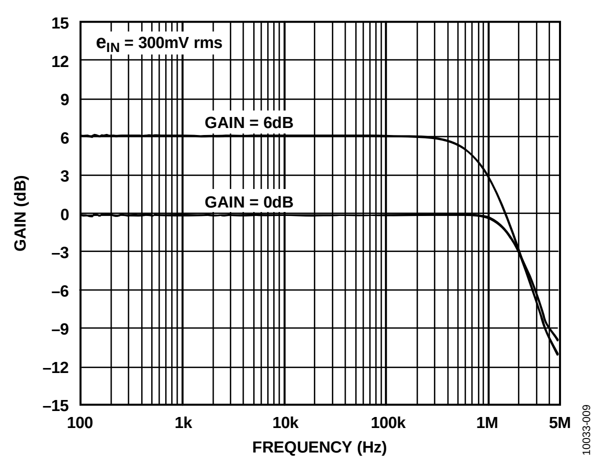


Figure 10. Input Buffer, Large Signal Bandwidth at 0 dB and 6 dB Gain

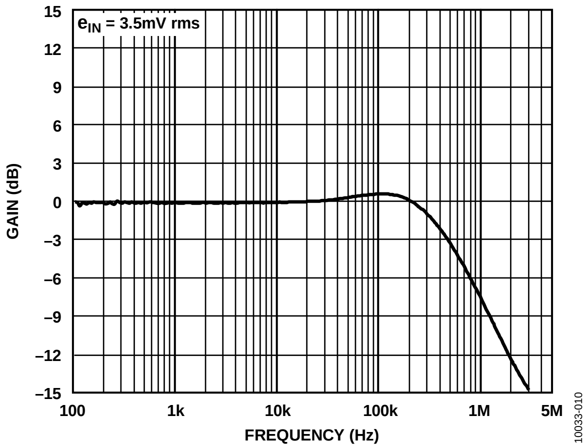


Figure 11. Output Buffer, Small Signal Bandwidth

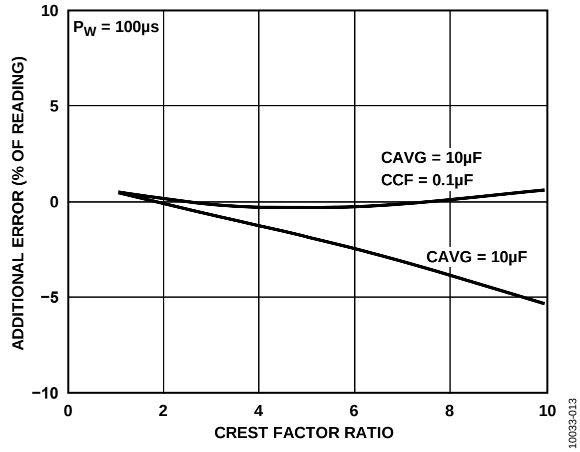


Figure 14. Crest Factor Error vs. Crest Factor for CAVG and CAVG and CCF Capacitor Combinations

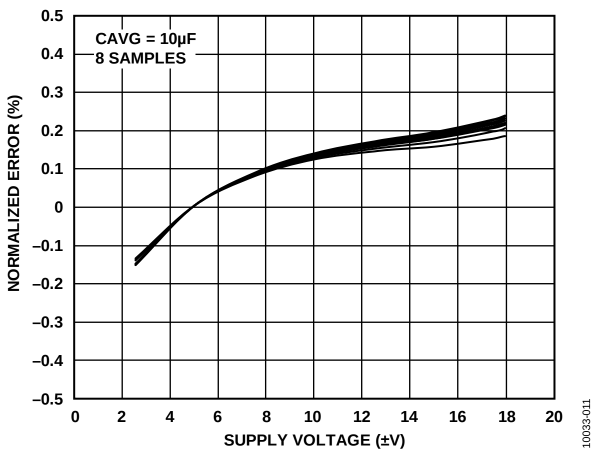


Figure 12. Additional Error vs. Supply Voltage

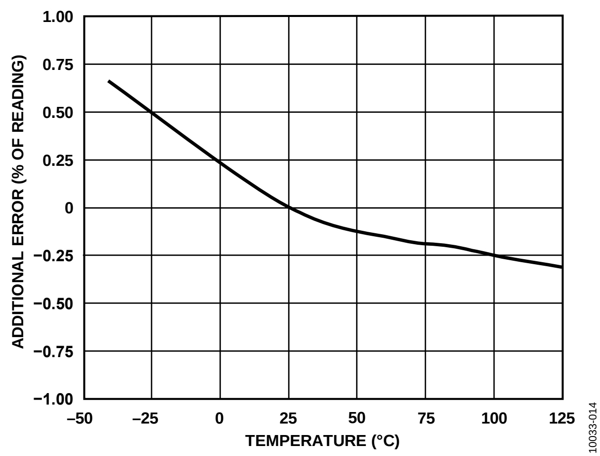


Figure 15. Additional Conversion Error vs. Temperature

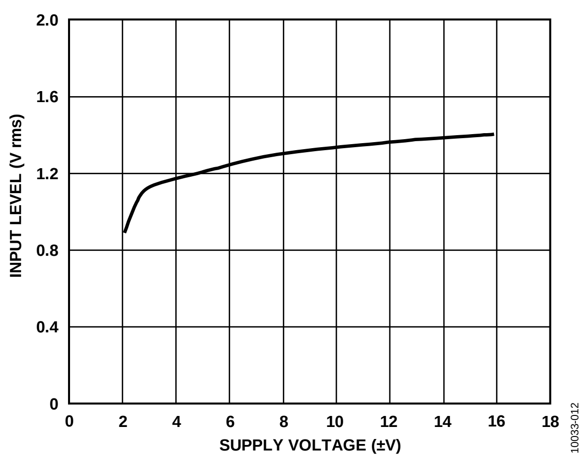


Figure 13. Core Input Voltage for 1% Error vs. Supply Voltage

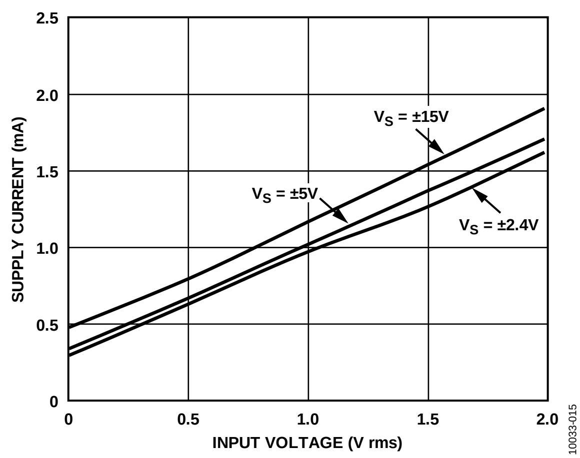


Figure 16. RMS Core Supply Current vs. Input for V_S = ±2.4 V, ±5 V, and ±15 V

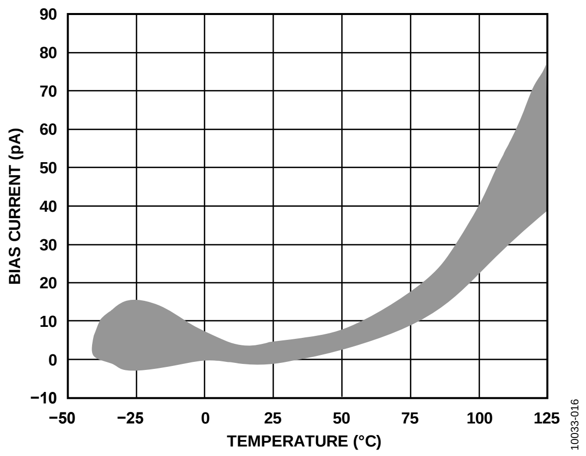


Figure 17. FET Input Buffer Bias Current vs. Temperature

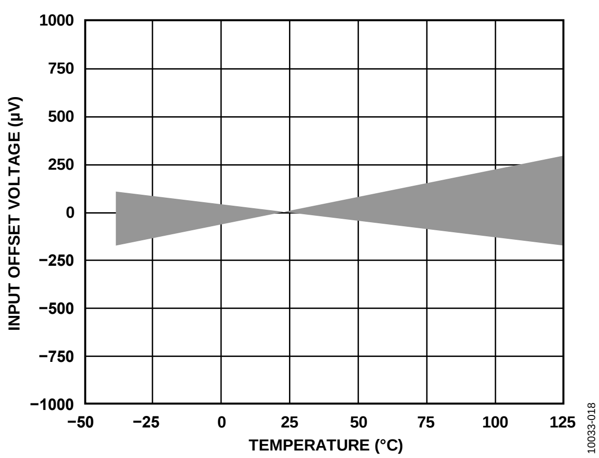


Figure 18. Input Offset Voltage of FET Buffer vs. Temperature

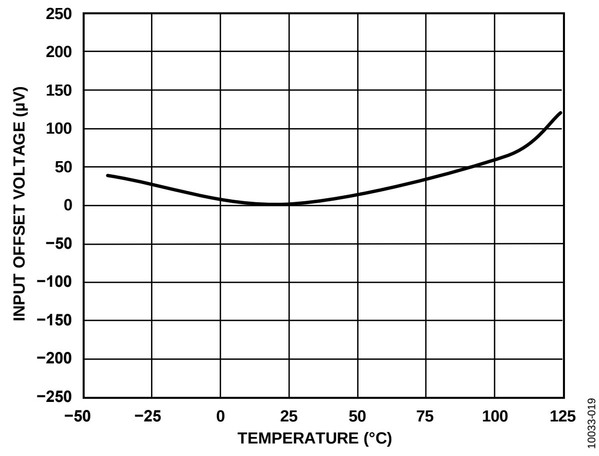


Figure 19. Output Buffer V_{OS} vs. Temperature

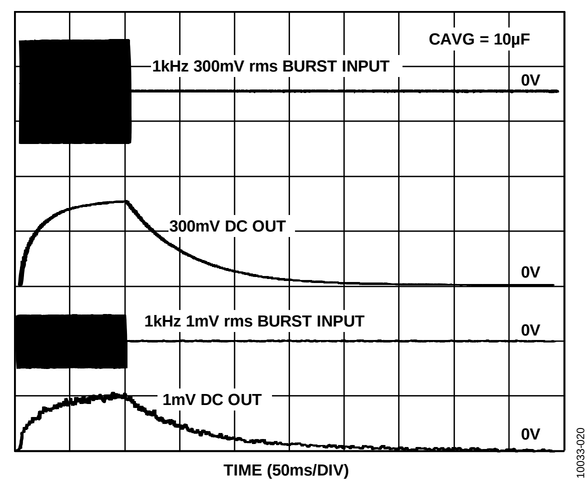


Figure 20. Transition Times with 1 kHz Burst at Two Input Levels (See Theory of Operation Section)

TEST CIRCUITS

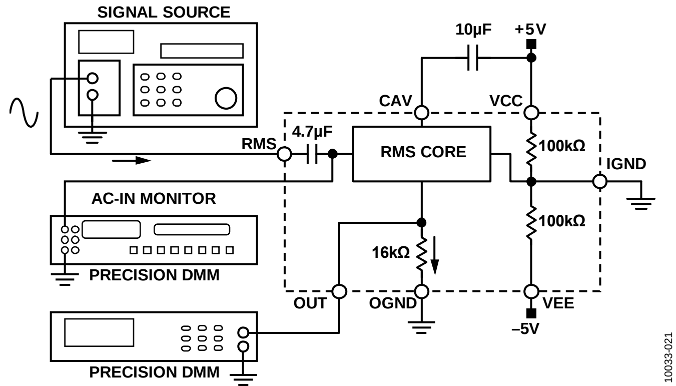


Figure 21. Core Response Test Circuit Using Dual Supplies

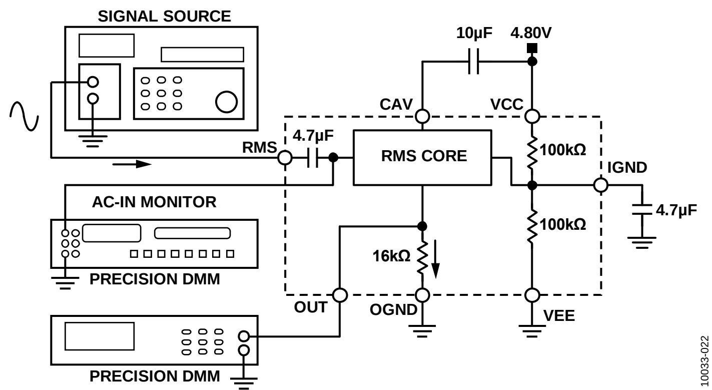


Figure 22. Core Response Test Circuit Using a Single Supply

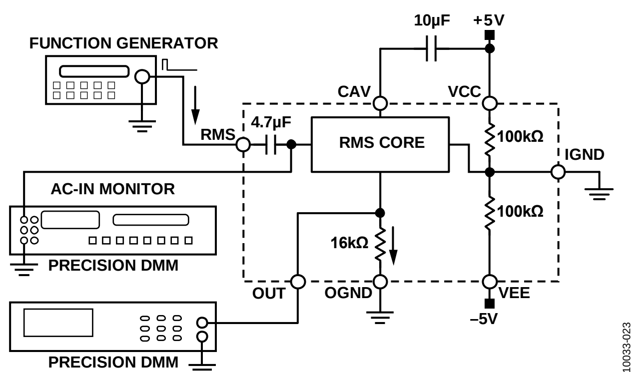


Figure 23. Crest Factor Test Circuit

THEORY OF OPERATION

OVERVIEW

The AD8436 is an implicit function rms-to-dc converter that renders a dc voltage dependent on the rms (heating value) of an ac voltage. In addition to the basic converter, this highly integrated functional circuit block includes two fully independent, optional amplifiers, a standalone FET input buffer amplifier and a precision dc output buffer amplifier (see Figure 1). The rms core includes a precision current responding full-wave rectifier and a log-antilog transistor array for current squaring and square rooting to implement the classic expression for rms (see Equation 1). For basic applications, the converter requires only an external capacitor, for averaging (see Figure 31). The optional on-board amplifiers offer utility and flexibility in a variety of applications without incurring additional circuit board footprint. For lowest power, the amplifier supply pins are left unconnected.

Why RMS?

The rms value of an ac voltage waveform is equal to the dc voltage providing the same heating power to a load. A common measurement technique for ac waveforms is to rectify the signal in a straightforward way using a diode array of some sort, resulting in the average value. The average value of various waveforms (sine, square, and triangular, for example) varies widely; true rms is the only metric that achieves equivalency for all ac waveforms. See Table 5 for non-rms-responding circuit errors.

The acronym "rms" means *root-mean-square* and reads as follows: "the square root of the average of the sum of the squares" of the peak values of any waveform. RMS is shown in the following equation:

$$e_{rms} = \sqrt{\frac{1}{T}\int_0^T V(t)^2 dt} \quad (1)$$

For additional information, select Section I of the 2nd edition of the *Analog Devices RMS-to-DC Applications Guide*.

RMS Core

The core consists of a voltage-to-current converter (precision resistor), absolute value, and translinear sections. The translinear section exploits the properties of the bipolar transistor junctions for squaring and root extraction (see Figure 24). The external capacitor (CAVG) provides for averaging the product. Figure 20 shows that there is no effect of signal input on the transition times, as seen in the dc output. Although the rms core responds to input voltages, the conversion process is current sensitive. If the rms input is ac-coupled, as recommended, there is no output offset voltage, as reflected in Table 1. If the rms input is dc-coupled, the input offset voltage is reflected in the output and can be calibrated as with any fixed error.

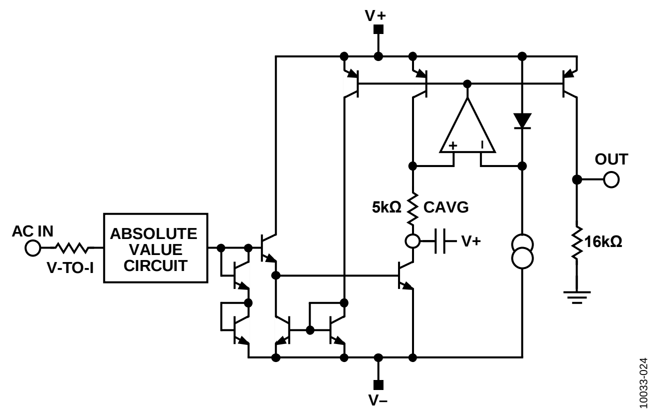


Figure 24. RMS Core Block Diagram

Table 5. General AC Parameters

Waveform Type (1 V Peak)	Crest Factor	RMS Value	Reading of an Average Value Circuit Calibrated to an RMS Sine Wave	Error (%)
Sine	1.414	0.707	0.707	0
Square	1.00	1.00	1.11	11.0
Triangle	1.73	0.577	0.555	−3.8
Noise	3	0.333	0.295	
Rectangular	2	0.5	0.278	−11.4
Pulse	10	0.1	0.011	−44
SCR				−89
DC = 50%	2	0.495	0.354	−28
DC = 25%	4.7	0.212	0.150	−30

The 16 kΩ resistor in the output converts the output current to a dc voltage that can be connected to the output buffer or to the circuit that follows. The output appears as a voltage source in series with 16 kΩ. If a current output is desired, the resistor connection to ground is left open and the output current is applied to a subsequent circuit, such as the summing node of a current summing amplifier. Thus, the core has both current and voltage outputs, depending on the configuration. For a voltage output with 0 Ω source impedance, use the output buffer. The offset voltage of the buffer is 25 µV or 50 µV, depending on the grade.

FET Input Buffer

Because the V-to-I input resistor value of the AD8436 rms core is 8 kΩ, a high input impedance buffer is often used between rms-dc converters and finite impedance sources. The optional JFET input op amp minimizes attenuation and uncouples common input amenities, such as resistive voltage dividers or resistors used to terminate current transformers. The wide bandwidth of the FET buffer is well matched to the rms core bandwidth so that no information is lost due to serial bandwidth effects. Although the input buffer consumes little current, the buffer supply is independently accessible and can be disconnected to reduce power.

Optional matched 10 kΩ input and feedback resistors are provided on chip. Consult the Applications Information section to learn how these resistors can be used. The 3 dB bandwidth of the input buffer is 2.7 MHz at 10 mV rms input and approximately 1.5 MHz at 1 V rms. The amplifier gain and bandwidth are sufficient for applications requiring modest gain or response enhancement to a few hundred kilohertz (kHz), if desired. Configurations of the input buffer are discussed in the Applications Information section.

Precision Output Buffer

The precision output buffer is a bipolar input amplifier, laser trimmed to cancel input offset voltage errors. As with the input buffer, the supply current is very low (<50 µA, typically), and the power can be disconnected for power savings if the buffer is not needed. Be sure that the noninverting input is also disconnected from the core output (OUT) if the buffer supply pin is disconnected. Although the input current of the buffer is very low, a laser-trimmed 16 kΩ resistor, connected in series with the inverting input, offsets any self-bias offset voltage.

The output buffer can be configured as a single or two-pole low-pass filter using circuits shown in the Applications Information section. Residual output ripple is reduced, without affecting the converted dc output. As the response approaches the low frequency end of the bandwidth, the ripple rises, dependent on the value of the averaging capacitor. Figure 27 shows the effects of four combinations of averaging and filter capacitors. Although the filter capacitor reduces the ripple for any given frequency, the dc error is unaffected. Of course, a larger value averaging capacitor can be selected, at a larger cost. The advantage of using a low-pass filter is that a small value of filter capacitor, in conjunction with the 16 kΩ output resistor, reduces ripple and permits a smaller averaging capacitor, effecting a cost savings. The recommended capacitor values for operation to 40 Hz are 10 µF for averaging and 3.3 µF for filter.

Dynamic Range

The AD8436 is a translinear rms-to-dc converter with exceptional dynamic range. Although accuracy varies slightly more at the extreme input values, the device still converts with no spurious noise or dropout. Figure 25 is a plot of the rms/dc transfer function near zero voltage. Unlike processor or other solutions, residual errors at very low input levels can be disregarded for most applications.

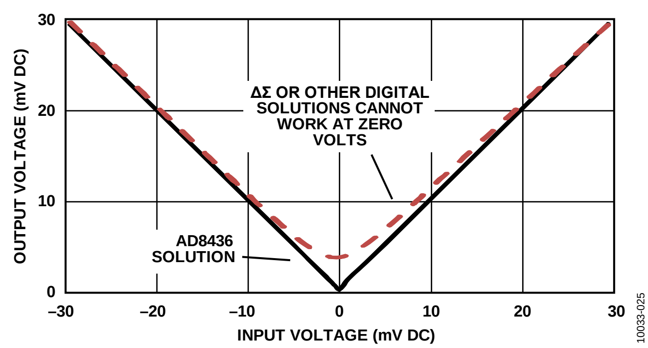


Figure 25. DC Transfer Function near Zero

APPLICATIONS INFORMATION

USING THE AD8436

This section describes the power supply and feature options, as well as the function and selection of averaging and filter capacitor values. Averaging and filtering options are shown graphically and apply to all circuit configurations.

Averaging Capacitor Considerations—RMS Accuracy

Typical AD8436 applications require only a single external capacitor (CAVG) connected to the CAVG pin (see Figure 31). The function of the averaging capacitor is to compute the mean (that is, average value) of the sum of the squares. Averaging (that is, integration) follows the rms core, where the input current is squared. The mean value is the average value of the squared input voltage over several input waveform periods. The rms error is directly affected by the number of periods averaged, as is the resultant peak-to-peak ripple.

The result of the conversion process is a dc component and a ripple component whose frequency is twice that of the input. The rms conversion accuracy depends on the value of CAVG, so the value selected need only be large enough to average enough periods at the lowest frequency of interest to yield the required rms accuracy.

Figure 28 is a plot of rms error vs. frequency for various averaging capacitor values. To use Figure 28, simply locate the frequency of interest and acceptable rms error on the horizontal and vertical scales, respectively. Then choose or estimate the next highest capacitor value adjacent to where the frequency and error lines intersect (for an example, see the orange circle in Figure 28).

Post Conversion Ripple Reduction Filter

Input rectification included in the AD8436 introduces a residual ripple component that is dependent on the value of CAVG and twice the input signal frequency for symmetrical input waveforms. For sampling applications such as a high resolution ADC, the ripple component may cause one or more LSBs to cycle, and low value display numerals to flash.

Ripple is reduced by increasing the value of the averaging capacitor, or by postconversion filtering. Ripple reduction following conversion is far more efficient because the ripple average value has been converted to its rms value. Capacitor values for postconversion filtering are significantly less than the equivalent averaging capacitor value for the same level of ripple reduction. This approach requires only a single capacitor connected to the OUT pin (see Figure 26). The capacitor value correlates to the simple frequency relation of ½ π R-C, where R is fixed at 16 kΩ.

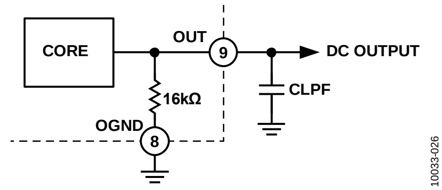


Figure 26. Simple One-Pole Post Conversion Filter

As seen in Figure 27, CAVG alone determines the rms error, and CLPF serves purely to reduce ripple. Figure 27 shows a constant rms error for CLPF values of 0.33 μF and 3.3 μF; only the ripple is affected.

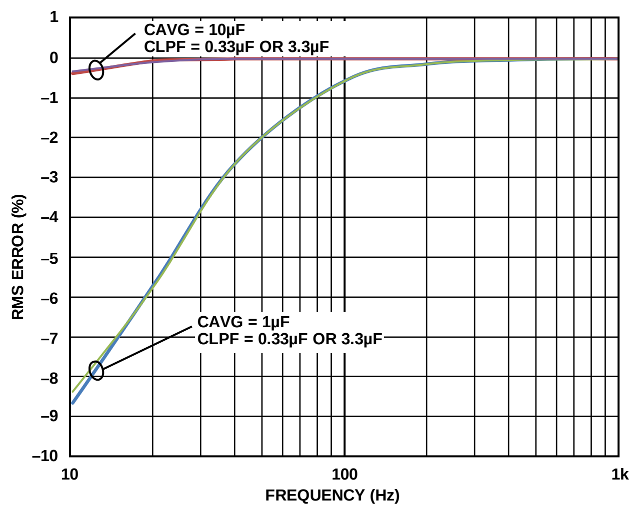


Figure 27. RMS Error vs. Frequency for Two Values of CAVG and CLPF (Note that only CAVG value affects rms error; CLPF has no effect.)

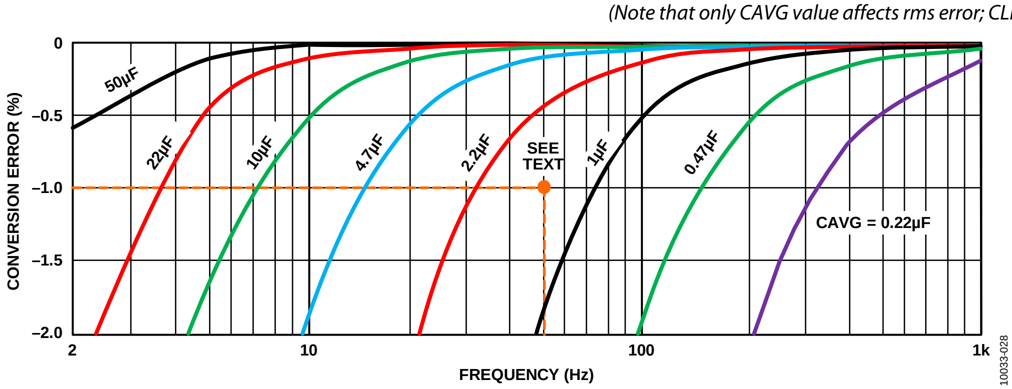


Figure 28. Conversion Error vs. Frequency for Various Values of CAVG

For simplicity, Figure 29 shows ripple vs. frequency for four combinations of CAVG and CLPF

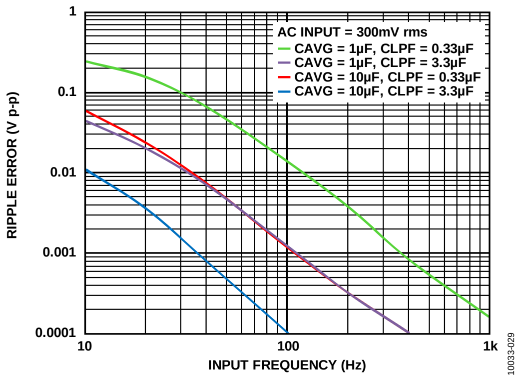


Figure 29. Residual Ripple Voltage for Various Filter Configurations

Figure 30 shows the effects of averaging and post-rms filter capacitors on transition and settling times using a 10-cycle, 50 Hz, 1 second period burst signal input to demonstrate time-domain behavior. In this instance, the averaging capacitor value was 10 µF, yielding a ripple value of 6 mV rms. A postconversion capacitor (CLPF) of 0.68 µF reduced the ripple to 1 mV rms. An averaging capacitor value of 82 µF reduced the ripple to 1 mV but extended the transition time (and cost) significantly.

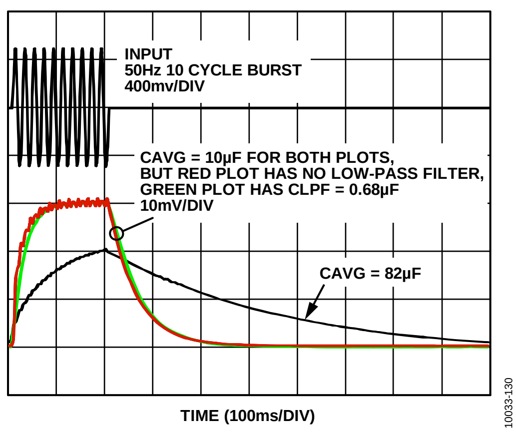


Figure 30. Effects of Various Filter Options on Transition Times

CAVG Capacitor Styles

When selecting a capacitor style for CAVG there are certain tradeoffs.

For general usage, such as most DMM or power measurement applications where input amplitudes are typically greater than 1 mV, surface mount tantalums are the best overall choice for space, performance, and economy.

For input amplitudes less than around a millivolt, low dc leakage capacitors, such as film or X8L MLCs, maintain rms conversion accuracy. Metalized polyester or similar film styles are best, as long as the temperature range is appropriate. X8L grade MLCs are rated for high temperatures (125°C or 150°C), but are available only up to 10 µF. Never use electrolytic capacitors, or X7R or lower grade ceramics.

Basic Core Connections

Many applications require only a single external capacitor for averaging. A 10 µF capacitor is more than adequate for acceptable rms errors at line frequencies and below.

The signal source sees the input 8 kΩ voltage-to-current conversion resistor at Pin RMS; thus, the ideal source impedance is a voltage source (0 Ω source impedance). If a non-zero signal source impedance cannot be avoided, be sure to account for any series connected voltage drop.

An input coupling capacitor must be used to realize the near-zero output offset voltage feature of the AD8436. Select a coupling capacitor value that is appropriate for the lowest expected operating frequency of interest. As a rule of thumb, the input coupling capacitor can be the same as or half the value of the averaging capacitor because the time constants are similar. For a 10 µF averaging capacitor, a 4.7 µF or 10 µF tantalum capacitor is a good choice (see Figure 31).

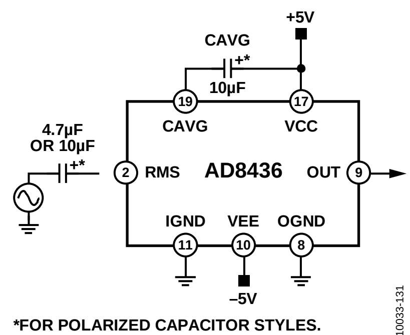


Figure 31. Basic Applications Circuit

Using a Capacitor for High Crest Factor Applications

The AD8436 contains a unique feature to reduce large crest factor errors. Crest factor is often overlooked when considering the requirements of rms-to-dc converters, but it is very important when working with signals with spikes or high peaks. The crest factor is defined as the ratio of peak voltage to rms. See Table 5 for crest factors for some common waveforms.

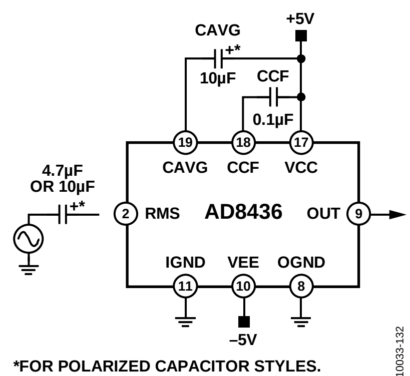


Figure 32. Connection for Additional Crest Factor Performance

Crest factor performance is mostly applicable for unexpected waveforms such as switching transients in switchmode power supplies. In such applications, most of the energy is in these peaks and can be destructive to the circuitry involved, although the average ac value can be quite low.

Figure 14 shows the effects of an additional crest factor capacitor of 0.1 µF and an averaging capacitor of 10 µF. The larger capacitor serves to average the energy over long spaces between pulses, while the CCF capacitor charges and holds the energy within the relatively narrow pulse.

Using the FET Input Buffer

The on-chip FET input buffer is an uncommitted FET input op amp used for driving the 8 kΩ I-to-V input resistor of the rms core. Pin IBUFOUT, Pin IBUFIN−, and Pin IBUFIN+ are the I/O, Pin IBUFINGN is an optional connection for gain in the input buffer, and Pin IBUFV+ connects power to the buffer. Connecting Pin IBUFV+ to the positive rail is the only power connection required because the negative rail is internally connected. Because the input stage is a FET and the input impedance must be very high to prevent loading of the source, a large value (10 MΩ) resistor is connected from midsupply at Pin IGND to Pin IBUFIN+ to prevent the input gate from floating high.

For unity gain, connect the IBUFOUT pin to the IBUFIN− pin. For a gain of 2×, connect the IBUFGN pin to ground. See Figure 9 and Figure 10 for large and small signal responses at the two built-in gain options.

The offset voltage of the input buffer is ≤500 µV, depending on grade. A capacitor connected between the buffer output pin (IBUFOUT) and the RMS pin is recommended so that the input buffer offset voltage does not contribute to the overall error. Select the capacitor value for least minimum error at the lowest operating frequency. Figure 33 is a schematic showing internal components and pin connections.

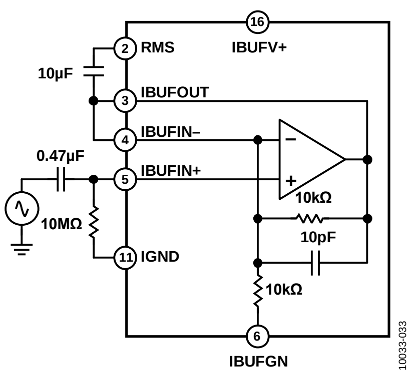


Figure 33. Connecting the FET Input Buffer

Capacitor coupling at the input and output of the FET buffer is recommended to avoid transferring the buffer offset voltage to the output. Although the FET input impedance is extremely high, the 10 MΩ centering resistor connected to IGND must be taken into account when selecting an input capacitor value. This is simply an impedance calculation using the lowest desired frequency, and finding a capacitor value based on the least attenuation desired.

Because the 10 kΩ resistors are closely matched and trimmed to a high tolerance, the input buffer gain can be increased to several hundred with an external resistor connected to Pin IBUFIN−.

The bandwidth diminishes at the typical rate of a decade per 20 dB of gain, and the output voltage range is constrained. The small signal response, shown in Figure 9, serves as a guide. For example, suppose one wanted to detect small input signals at power line frequencies? An external 10 Ω resistor connected from IBUFIN− to ground sets the gain to 101 and the 3 dB bandwidth to ~30 kHz, which is more than adequate for amplifying power line frequencies.

Using the Output Buffer

The AD8436 output buffer is a precision op amp optimized for high dc accuracy. Figure 34 shows a block diagram of the basic amplifier and I/O pins. The amplifier is often configured as a unity gain follower but is easily configured for gain, as a Sallen-Key low-pass filter (in conjunction with the built-in 16 kΩ I-to-V resistor). Note that an additional 16 kΩ on-chip precision resistor in series with the inverting input of the amplifier balances output offset voltages resulting from the bias current from the noninverting amplifier. The output buffer is disconnected from Pin OUT for precision core measurements.

As with the input FET buffer, the amplifier positive supply is disconnected when not needed. In normal circumstances, the buffers are connected to the same supply as the core. Figure 35 shows the signal connections to the output buffer. Note that the input offset voltage contribution by the bias currents are balanced by equal value series resistors, resulting in near zero offset voltage.

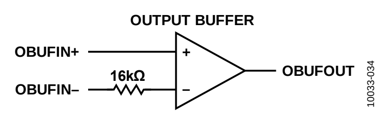


Figure 34. Output Buffer Block Diagram

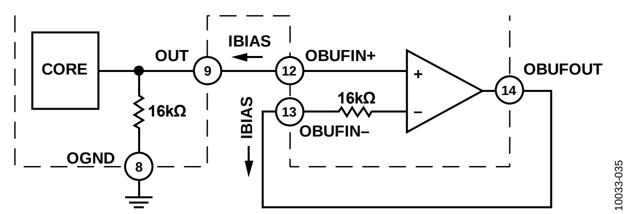


Figure 35. Basic Output Buffer Connections

For applications requiring ripple suppression in addition to the single-pole output filter described previously, the output buffer is configurable as a two-pole Sallen-Key filter using two external resistors and two capacitors. At just over 100 kHz, the amplifier has enough bandwidth to function as an active filter for low frequencies such as power line ripple. For a modest savings in cost and complexity, the external 16 kΩ feedback resistor can be omitted, resulting in slightly higher V_{OS} (80 µV).

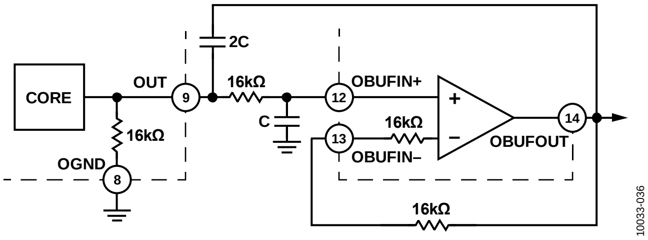


Figure 36. Output Buffer Amplifier Configured as a Two-Pole, Sallen-Key Low-Pass Filter

Configure the output buffer (see Figure 37) to invert dc output.

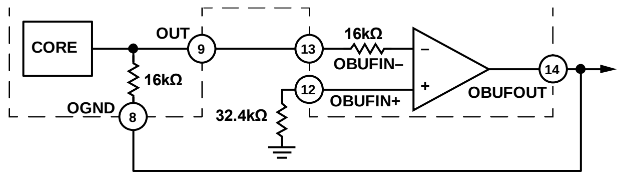


Figure 37. Inverting Output Configuration

Current Output Option

If a current output is required, connect the current output, OUT, to the destination load. To maximize precision, provide a means for external calibration to replace the internal trimmed resistor, which is bypassed. This configuration is useful for convenient summing of the AD8436 result with another voltage, or for polarity inversion.

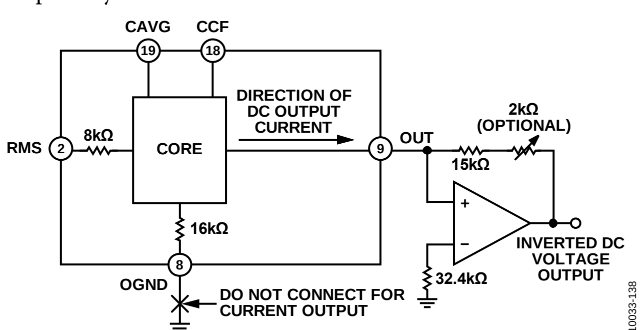


Figure 38. Connections for Current Output Showing Voltage Inversion

Single Supply

Connections for single supply operation are shown in Figure 39 and are similar to those for dual power supply when the device is ac-coupled. The analog inputs are all biased to half the supply voltage, but the output remains referred to ground because the output of the AD8436 is a current source. An additional bypass connection is required at IGND to suppress ambient noise.

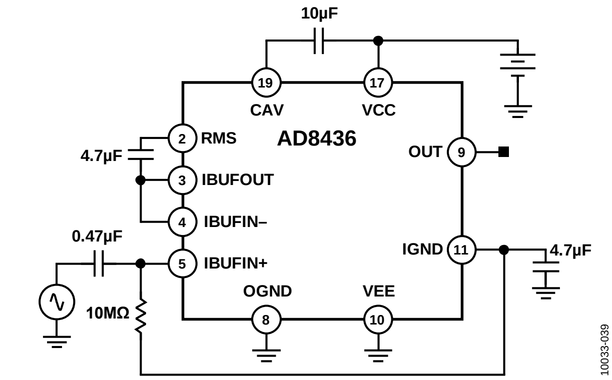


Figure 39. Connections for Single Supply Operation

Recommended Application

Figure 40 shows a circuit for a typical application for frequencies as low as power line, and above. The recommended averaging, crest factor and LPF capacitor values are 10 µF, 0.1 µF and 3.3 µF. Refer to the Using the Output Buffer section if additional low-pass filtering is required.

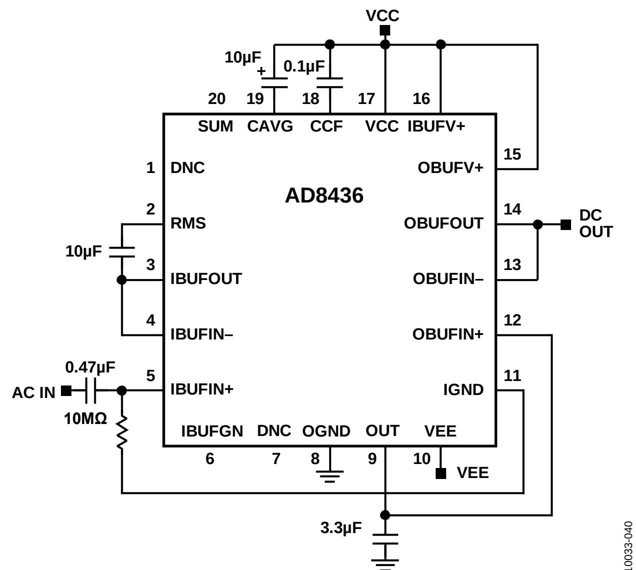


Figure 40. Typical Application Circuit

Converting to Average Rectified Value

To configure the AD8436 for rectified average instead of rms conversion, simply reduce the value of CAVG to 470 pF (see Figure 41). To enable both modes of operation, insert a switch between capacitor CAVG and Pin CAVG.

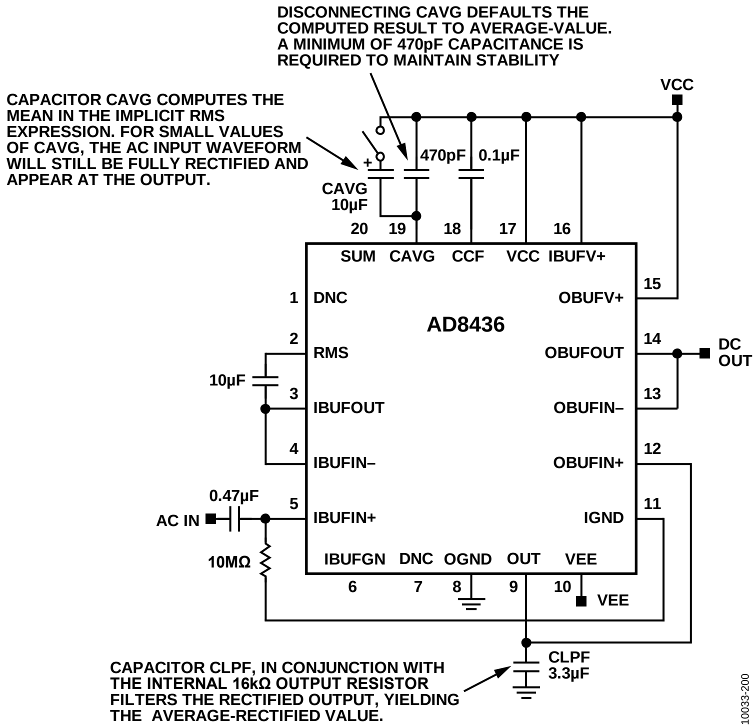


Figure 41. Configuration for Average Rectified Value

AD8436 EVALUATION BOARD

The AD8436-EVALZ provides a platform to evaluate AD8436 performance. The board is fully assembled, tested, and ready to use after the power and signal sources are connected. Figure 47 is a photograph of the board. Signal connections are located on the primary and secondary sides, with power and ground on the inner layers. Figure 42 to Figure 46 illustrate the various design details of the board, including basic layout and copper patterns. These figures are useful for reference for application designs.

A Word About Using the AD8436 Evaluation Board

The AD8436-EVALZ offers many options, without sacrificing simplicity. The board is tested and shipped with a 10 μF averaging capacitor (CAVG), 3.3 μF low-pass filter capacitor (C8) and a 0.1 μF (COPT) capacitor to optimize crest factor performance. To evaluate minimum cost applications, remove C8 and COPT. The functions of the five switches are listed in Table 6.

Table 6.

Switch	Function
CORE_BUFFER	Selects core or input buffer for the input signal
INCOUP	Selects ac or dc coupling to the core
SDCOUT	Selects the output buffer or the core output at the DCOUT BNC.
IBUF_VCC	Enable or disables the input buffer
OBUF_VCC	Enable or disables the output buffer

All the I/Os are provided with test points for easy monitoring with test equipment. The input buffer gain default is unity; for 2× gain, install a 0603 0 Ω resistor at Position R5. For higher IBUF gains, remove the 0 Ω resistor at Position RFBH (there is an internal 10 kΩ resistor from the OBUF_OUT to IBUFIN−) and install a smaller value resistor in Position RFBL. A 100 Ω resistor establishes a gain of 100×.

Single supply operation requires removal of Resistor R6 and installing a 0.1 μF capacitor in the same position for noise decoupling.

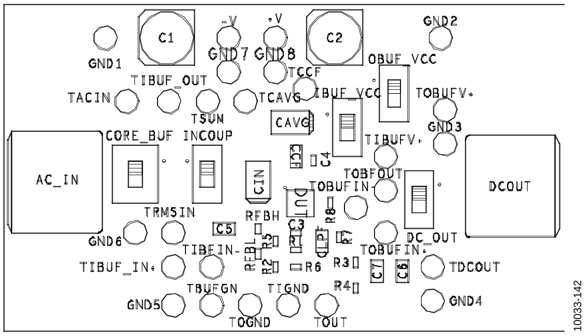


Figure 42. Assembly of the AD8436-EVALZ

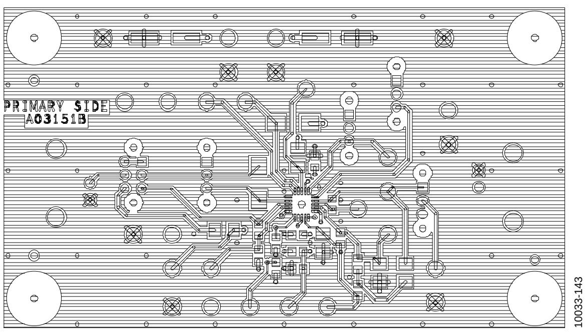


Figure 43. AD8436-EVALZ Primary Side Copper

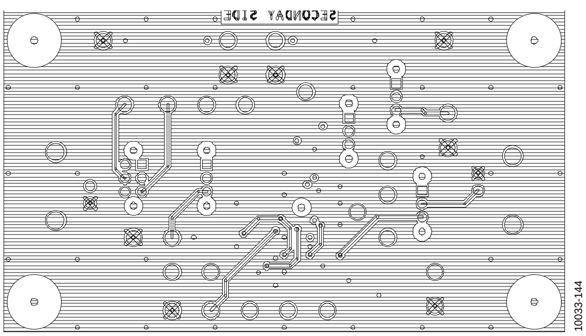


Figure 44. AD8436-EVALZ Secondary Side Copper

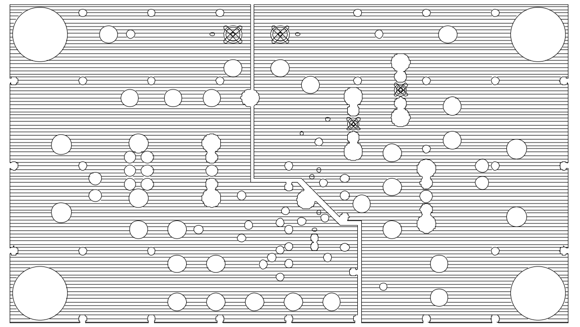


Figure 45. AD8436-EVALZ Power Plane

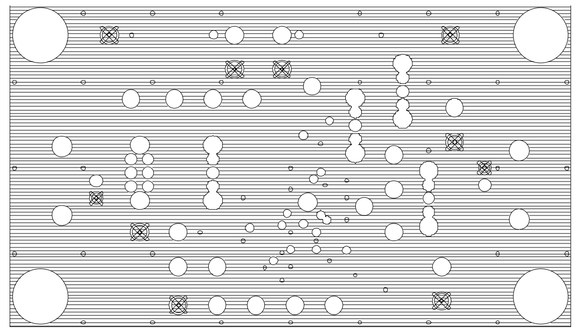


Figure 46. AD8436-EVALZ Ground Plane

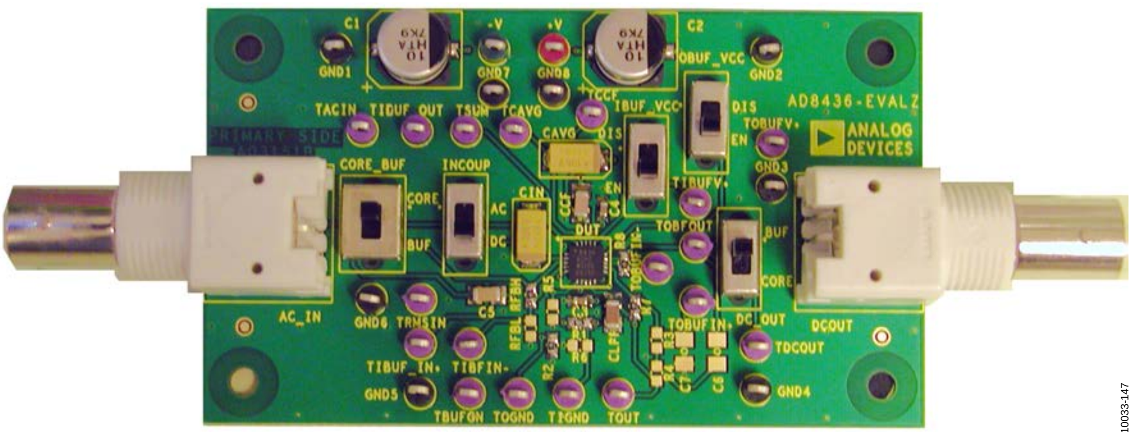
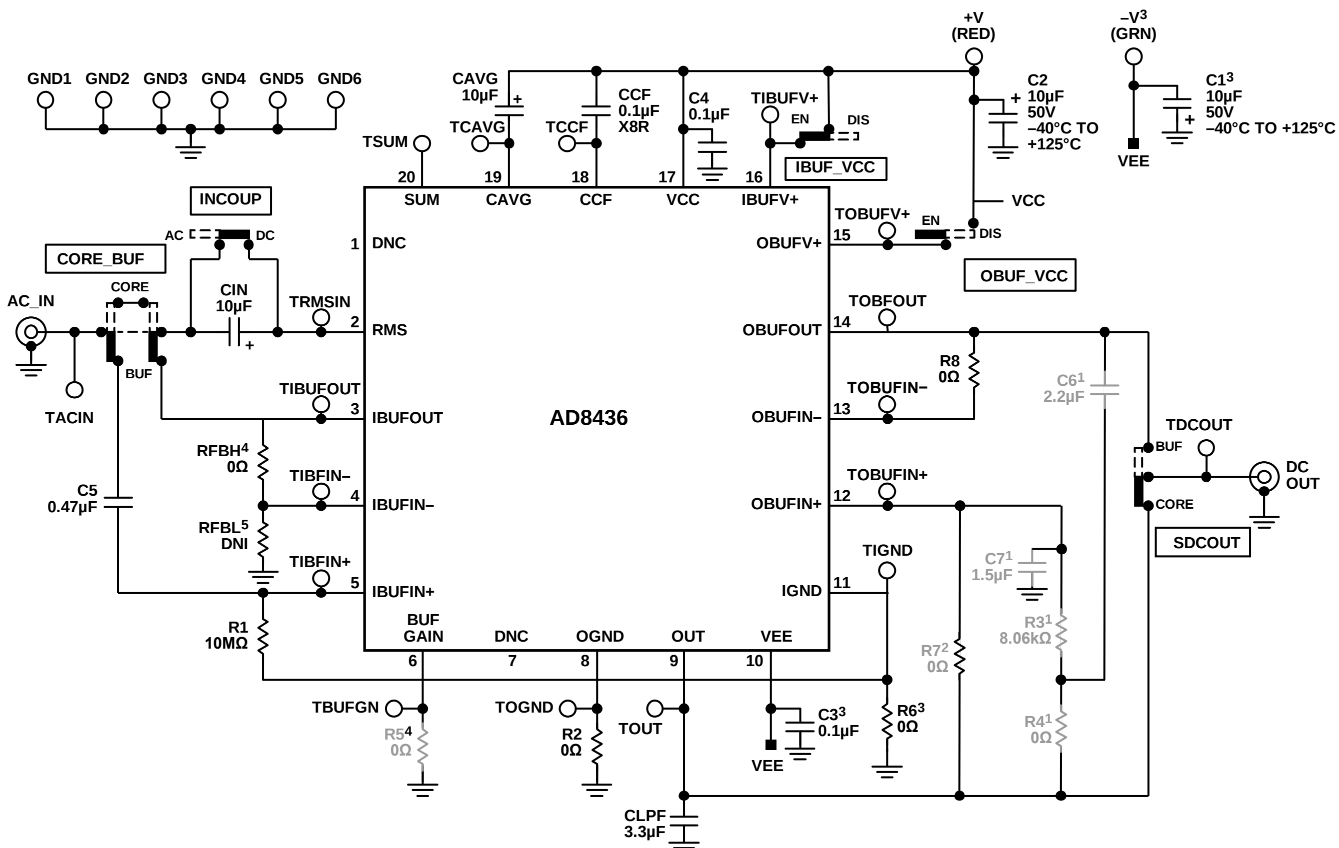


Figure 47. Photograph of the AD8436-EVALZ



[1]OPTIONAL COMPONENTS TO CONFIGURE IBUFOUT AS A FILTER.
[2]REMOVE R7 FOR CORE-ONLY TESTS.
[3]FOR SINGLE SUPPLY OPERATION, REMOVE R6, SHORT OR REPLACE C3 WITH A 0Ω RESISTOR AND CONNECT THE SUPPLY GROUND OR RETURN TO THE GREEN TEST LOOP –V.
[4]TO CONFIGURE THE FET INPUT BUFFER FOR GAIN OF 2, INSTALL 0Ω RESISTOR AT R5 AND REMOVE RFBH.
[5]RFBL IS USED TO CONFIGURE THE INPUT BUFFER FOR GAIN VALUES >2×.

Figure 48. Evaluation Board Schematic

OUTLINE DIMENSIONS

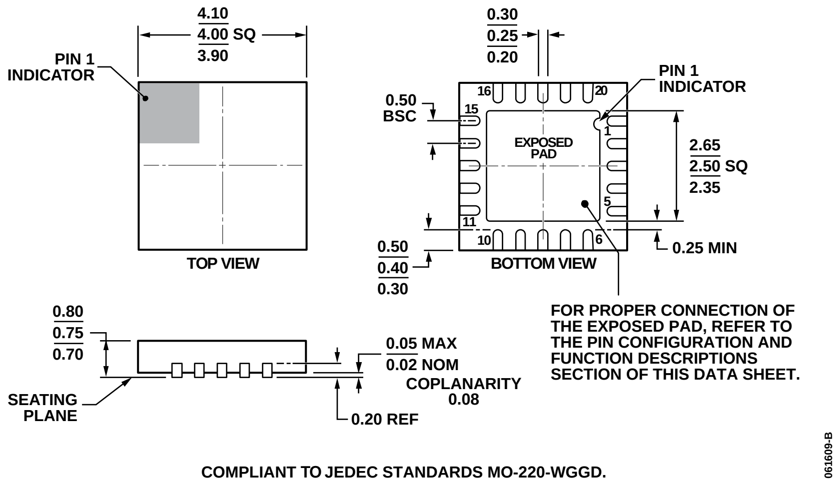


Figure 49. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in inches

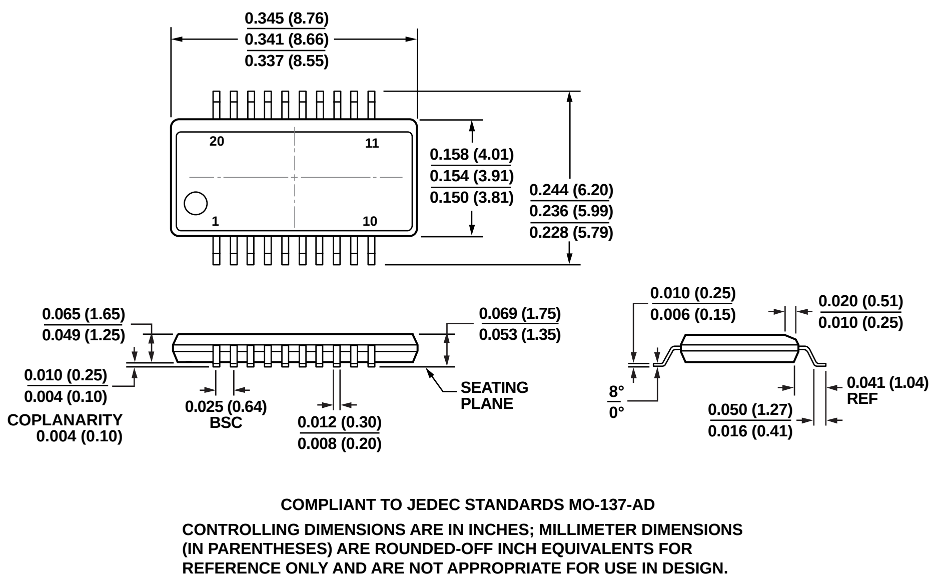


Figure 50. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8436ACPZ-R7	−40°C to +125°C	20-Lead Lead Frame Chip Scale [LFCSP_WQ]	CP-20-10
AD8436ACPZ-RL	−40°C to +125°C	20-Lead Lead Frame Chip Scale [LFCSP_WQ]	CP-20-10
AD8436ACPZ-WP	−40°C to +125°C	20-Lead Lead Frame Chip Scale [LFCSP_WQ]	CP-20-10
AD8436JCPZ-R7	0°C to +70°C	20-Lead Lead Frame Chip Scale [LFCSP_WQ]	CP-20-10
AD8436JCPZ-RL	0°C to +70°C	20-Lead Lead Frame Chip Scale [LFCSP_WQ]	CP-20-10
AD8436JCPZ-WP	0°C to +70°C	20-Lead Lead Frame Chip Scale [LFCSP_WQ]	CP-20-10
AD8436ARQZ-R7	−40°C to +125°C	20-Lead QSOP [RQ_20]	RQ-20
AD8436ARQZ-RL	−40°C to +125°C	20-Lead QSOP [RQ_20]	RQ-20
AD8436ARQZ	−40°C to +125°C	20-Lead QSOP [RQ_20]	RQ-20
AD8436BRQZ-R7	−40°C to +125°C	20-Lead QSOP [RQ_20]	RQ-20
AD8436BARQZ-RL	−40°C to +125°C	20-Lead QSOP [RQ_20]	RQ-20
AD8436BRQZ	−40°C to +125°C	20-Lead QSOP [RQ_20]	RQ-20
AD8436-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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NOTES

LifeElectronics
Живое партнерство

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- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

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