MIC3838/3839

Flexible Push-Pull PWM Controller

General Description

The MIC3838 and MIC3839 are a family of complementary output push-pull PWM control ICs that feature high speed and low power consumption. The MIC3838/9 are ideal for telecom level (36V to 75V) isolated step down dc/dc conversion applications where high output current, small size, and high efficiency are required

The MIC3838/9 are designed for high flexibility with minimum pin-count. The devices are easily configurable for either voltage-mode or current-mode control. Additionally, the MIC3838/9 can easily implement a volt-second clamp that automatically limits the duty cycle during input transients, allowing designers to use the smallest possible transformers and power components. A 3V reference output is also available that eliminates the need for an external reference.

The dual-ended push-pull architecture of the MIC3838/9 allows more efficient utilization of the transformer than single-ended topologies, allowing smaller size dc/dc solutions. Additionally, the out-of-phase push-pull topology allows a higher effective duty cycle, reducing input and output ripple as well as stress on the external components. The dead-time between the two outputs is adjustable between 60ns to 200ns, limiting the duty cycle of each output stage to less than 50%.

The MIC3838 has a turn-on threshold of 12.5V whereas the MIC3839 has a lower turn-on threshold of 4.3V. Both devices are available in a small size MSOP-10 package with an operating range of –40°C to +85°C.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

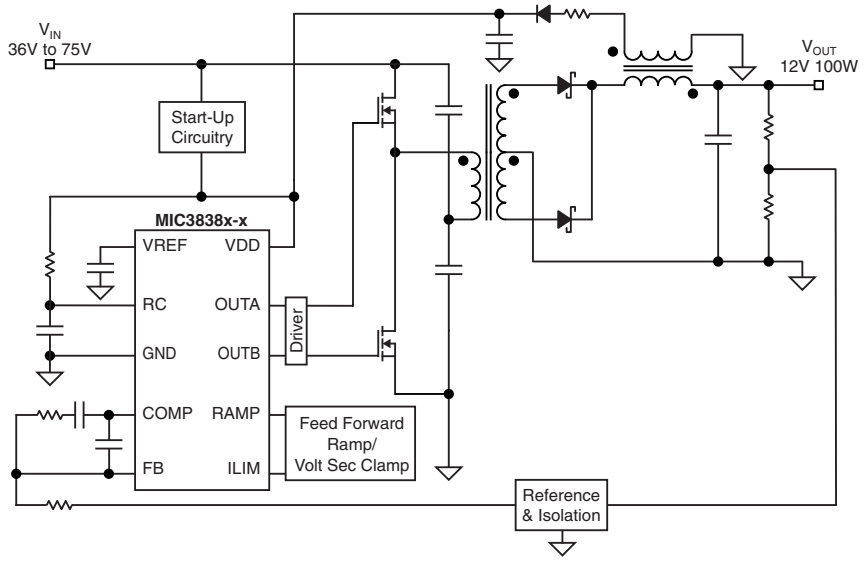
Features

- Dual output drive stages in push-pull configuration
- Configurable for current-mode or voltage-mode control
- Easily implements volt-second clamp
- Leading edge current-sense blanking
- 3V reference output available
- 130µA typical start-up current
- 1mA typical run current
- Operation to 1MHz
- On-chip error amplifier with 4MHz gain bandwidth product
- Internal soft start
- On-chip V_{DD} clamping
- Output drive stages capable of 500mA peak source current, 1A peak sink current

Applications

- High efficiency "brick" power supply modules
  - Half bridge converters
  - Full bridge converters
  - Push-pull converters
  - Voltage-fed push-pull converters
- Telecom equipment and power supplies
- Industrial power supplies
- 42V automotive power supplies
- Base stations
- Networking power supplies

Typical Application

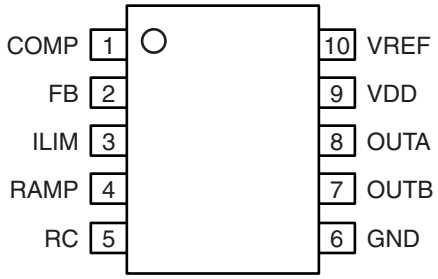


Voltage-Mode Half-Bridge Converter CIrcuit

Ordering Information

Part Number					
Standard	Lead-Free	Turn On Threshold	Turn Off Threshold	Temperature Range	Package
MIC3838BMM	MIC3838YMM	12.5V	8.3V	–40°C to +85°C	10-Pin MSOP
MIC3839BMM	MIC3839YMM	4.3V	4.1V	–40°C to +85°C	10-Pin MSOP

Pin Configuration



MSOP-10 (MM)

Pin Description

Pin Number	Pin Name	Pin Function
1	COMP	COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the MIC3838 is a true low-output impedance, 4MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND. The MIC3838 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.
2	FB	The inverting input to the error amplifier.
3	ILIM	The input to the peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.
4	RAMP	Input to the PWM comparator. Sawtooth ramp for PWM control. Allows for either current-mode or voltage-mode control. An internal MOSFET discharges the current sense filter capacitor.
5	RC	The oscillator programming pin. Only two components are required to program the oscillator, a resistor (tied between V_{DD} and RC), and a capacitor (tied between RC and GND). The approximate oscillator frequency is determined by the simple formula: $F_{OSCILLATOR} = \frac{1.41}{R \times C}$ The recommended range of timing resistors is between 7kΩ and 200kΩ and range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 7kΩ should be avoided. For best performance, keep the leads between components as short as possible. Separate ground and VDD traces to the external timing network are encouraged.
6	GND	Ground. Return path for signal and gate drive functions.

Pin Description

Pin Number	Pin Name	Pin Function
7, 8	OUTB, OUTA	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak source current, and 1A peak sink current. The output stages switch at half the oscillator frequency, in a push/pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This “dead time” between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60ns to 200ns and depends upon the values of the timing capacitor and resistor. The high-current output drivers consist of MOSFET output devices, which switch from V_{DD} to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external Schottky clamp diodes are not required.
9	VDD	The power input connection for this device. Total V_{DD} current is the sum of quiescent V_{DD} current and the average gate drive (OUT) current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from IOUT = Qg • F, where Qg is the total gate change of all MOSFETs (OUTA and OUTB) and F is oscillator switching frequency. To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible. A 1μF decoupling capacitor is recommended.
10	VREF	Internal 3V supply. Will source 1mA maximum.

Absolute Maximum Rating (Note 1)

Supply Voltage (I_{DD} ≤10mA) ..... +15V
Supply Current 20mA
OUTA/OUTB Source Current (peak) ..... –0.5A
OUTA/OUTB Sink Current (peak) 1.0A
COMP Pin ..... V_{DD}
Analog Inputs (FB, ILIM, RAMP) ..... –0.3V to V_{DD} +0.3V
NOT TO EXCEED 6V
Junction Temperature ..... –55°C to +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
ESD Rating, **Note 3** 2kV

Operating Ratings (Note 2)

V_{DD} Input Voltage (V_{DD}) ..... **Note 4**
Oscillator Frequency (f_{OSC}) ..... 10kHz to 1MHz
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
MSOP-10 (θ_{JA}) ..... 115°C/W

Electrical Characteristics (Note 5)

$T_A = T_J$ = –40°C to +85°C, V_{DD}=10V, **Note 10**,1μF capacitor from V_{DD} to GND, R=22kΩ, C=330pF.

Parameter	Condition	Min	Typ	Max	Units
Internal Reference Section					
Output voltage	I_{OUT} = 0mA	2.85	3.0	3.15	V
Line Regulation	MIC3838 9V ≤ V_{DD} ≤12V MIC3839 5V ≤ V_{DD} ≤12V		2	10	mV
Load Regulation	I_{OUT} = 1mA		14	30	mV
Oscillator Section					
Oscillator Frequency		180	200	220	kHz
Oscillator Amplitude/V_{DD}	**Note 6**	0.44	0.5	0.56	V/V_{DD}
Error Amp Section					
Input Voltage	COMP = 2V	1.95	2	2.05	V
Input Bias Current		–1		1	μA
Open Loop Voltage Gain	(Guaranteed by design)	60	80		dB
COMP Sink Current	FB = 2.2V, COMP = 1V	0.3	2.5		mA
COMP Source Current	FB = 1.3V, COMP = 3V, **Note 7**	–0.15	–0.5		mA
COMP PM Clamp Voltage	V_{FB} = 0V	3.1	3.6	4.0	V
PWM Section					
Maximum Duty Cycle	Measured at OUTA or OUTB	48	49	50	%
Minimum Duty Cycle	COMP = 0V			0	%
Current Sense Section					
Gain	Guaranteed by design, **Note 8**	1.9	2.2	2.5	V/V
I_{LIM} Maximum Input Signal	**Note 9**	0.45	0.5	0.55	V
I_{LIM} to Output Delay	COMP = 3V, I_{LIM} from 0mV to 600mV		70	200	ns
Ramp or I_{LIM} Source Current		–200			nA
Ramp or I_{LIM} Sink Current	Ramp = I_{LIM} = 0.5V, RC = 5.5V **Note 10**	5	10		mA
I_{LIM} Over Current Threshold		0.7	0.75	0.8	V
COMP to Ramp Offset	Ramp = I_{LIM} = 0V	0.35	0.8	1.2	V
Output Section					
OUT Low Level	I = 100mA		0.5	1	V
OUT High Level	I = –50mA, V_{DD} – OUT		0.5	1	V
Rise Time	C_L = 1nF		25	60	ns
Fall Time	C_L = 1nF		25	60	ns

Parameter	Condition	Min	Typ	Max	Units
Undervoltage Lockout Section					
Start Threshold	MIC3838, **Note 11**	11.5	12.5	13.5	V
	MIC3839	4.1	4.3	4.5	V
Minimum Operating Voltage	MIC3838	7.6	8.3	9	V
After Start	MIC3839	3.9	4.1	4.3	V
Hysteresis	MIC3838	3.5	4.2	5.1	V
	MIC3839	0.1	0.2	0.3	V
Soft Start Section					
COMP Rise Time	FB = 1.8V, Rise from 0.5V to 3V		2.5	20	ms
Overall Section					
Startup Current	V_{DD} < Start Threshold (MIC3839)		130	260	μA
Operating Supply Current	FB = 0V, Ramp = I_{LIM} = 0V, **Notes 11, 12**		1.5	2	mA
V_{DD} Zener Shunt Voltage	I_{DD} = 10mA, **Note 13**	13	14	15	V

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Note 4. Maximum operating voltage is equal to the V_{DD} (zener) shunt voltage. When operating at or near the shunt voltage, care must be taken to limit the V_{DD} pin current less than the 20mA V_{DD} maximum current rating.

Note 5. Specification for packaged product only.

Note 6. Measured at RC.

Note 7. COMP pin is internally clamped to 3.65V(typ.). COMP pin source current is measured at V_{COMP} = 3.0V to avoid interferring with clamp. Minimum source current is higher as V_{COMP} approaches V_{CLAMP}.

Note 8. Gain is defined by $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$, $0 \le V_{CS} \le 0.4V$.

Note 9. Parameter measured at trip point of latch with FB at 0V

Note 10. The internal current sink on the Ramp and I_{LIM} pin are designed to discharge an external filter capacitor. It is not intended to be a DC sink path. Internal discharge FET should be able to discharge the Volt-Sec clamp and feed-forward circuits in the figure below within 50ns.

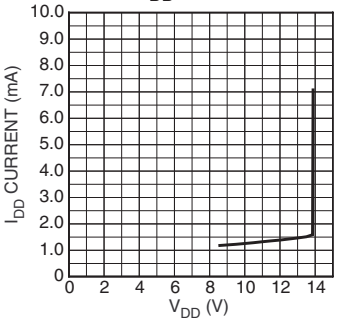
Note 11. For MIC3838, set V_{DD} above the start threshold before setting at 10V.

Note 12. Does not include current in the external oscillator network.

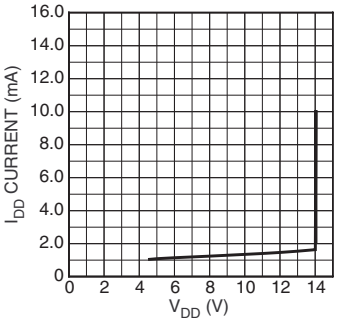
Note 13. Start threshold and Zener Shunt threshold track one another.

Typical Characteristics

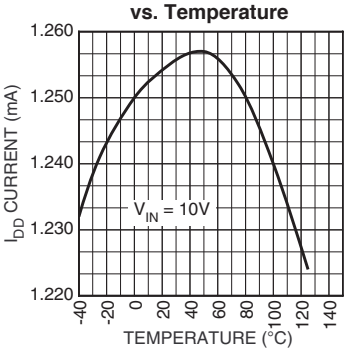
MIC3838 I_{DD} Current



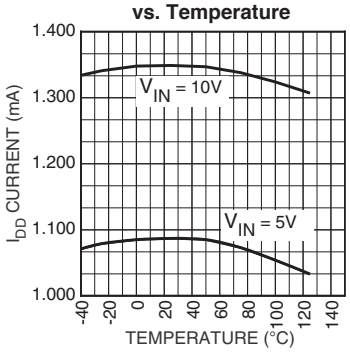
MIC3839 I_{DD} Current



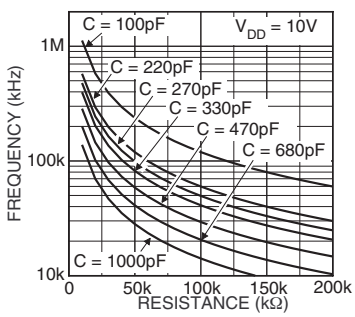
MIC3838 I_{DD} Current vs. Temperature



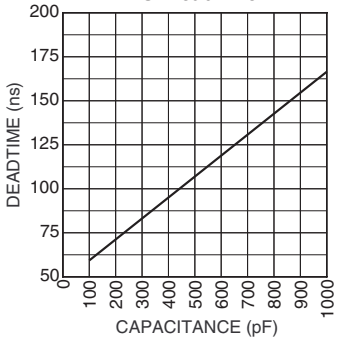
MIC3839 I_{DD} Current vs. Temperature



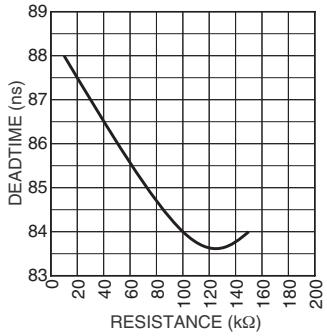
Oscillator Frequency vs. RC Values



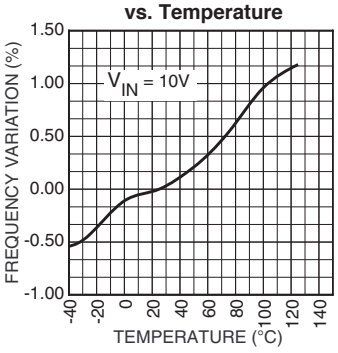
RC Pin Capacitance vs. Deadtime



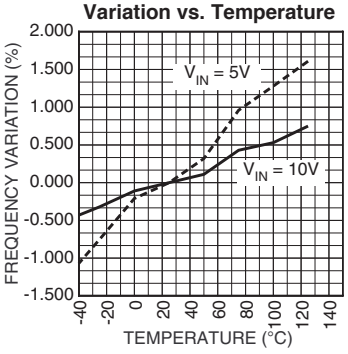
RC Pin Resistance vs. Deadtime



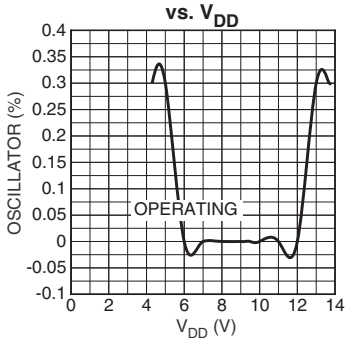
MIC3838 Oscillator Variation vs. Temperature



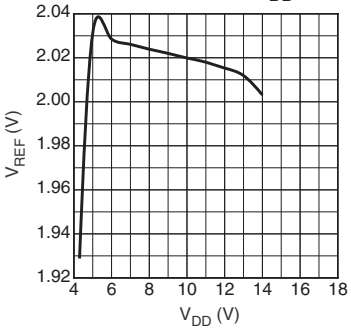
MIC3839 % Oscillator Variation vs. Temperature



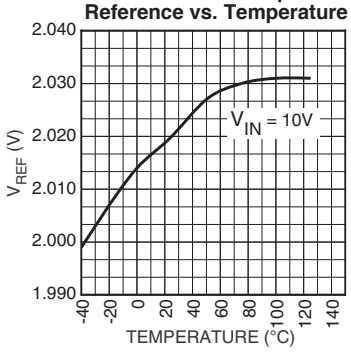
MIC3839 Oscillator Variation vs. V_{DD}



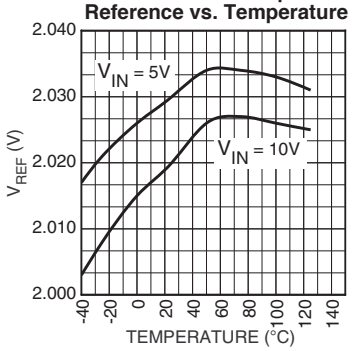
MIC3839 Error Amplifier Reference vs. V_{DD}



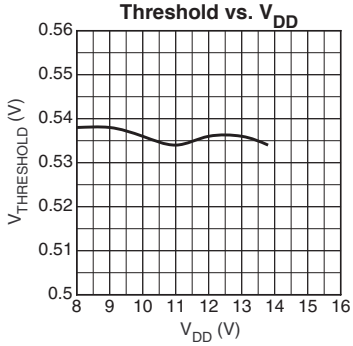
MIC3838 Error Amplifier Reference vs. Temperature



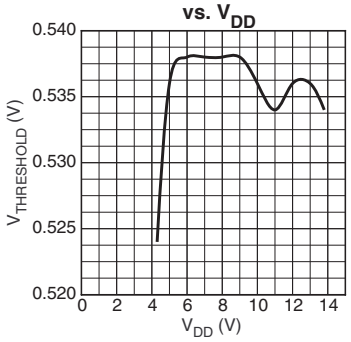
MIC3839 Error Amplifier Reference vs. Temperature



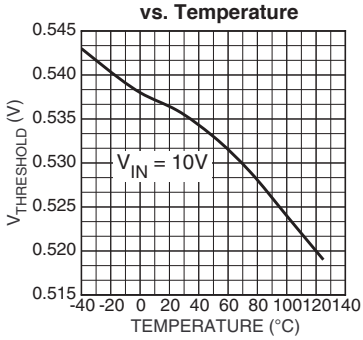
MIC3838 Current Limit Threshold vs. V_{DD}



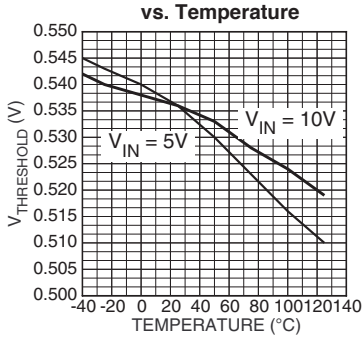
MIC3839 Peak Current Limit vs. V_{DD}



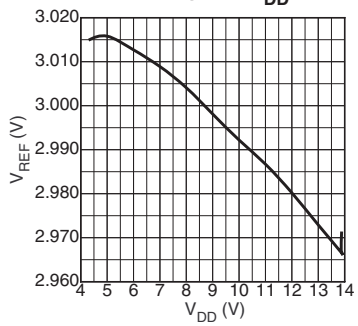
MIC3838 Peak Current Limit vs. Temperature



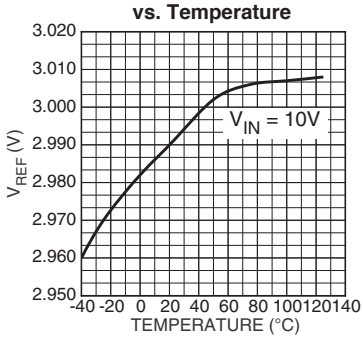
MIC3839 Peak Current Limit vs. Temperature



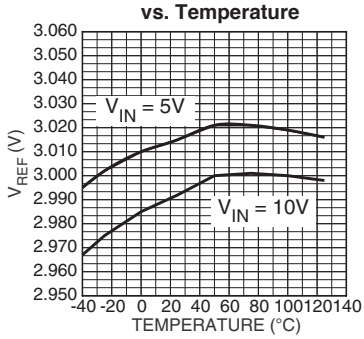
MIC3839 3V Reference Voltage vs. V_{DD}



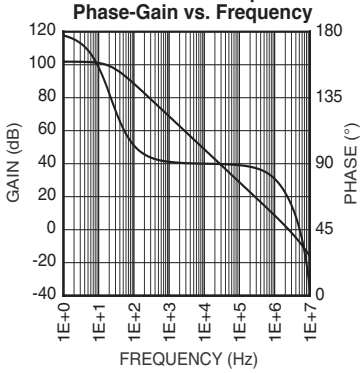
MIC3838 3V Reference vs. Temperature



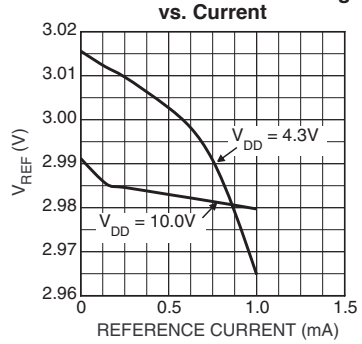
MIC3839 3V Reference vs. Temperature



MIC3838 Error Amplifier Phase-Gain vs. Frequency



MIC3839 3V Reference Voltage vs. Current



Functional Diagram

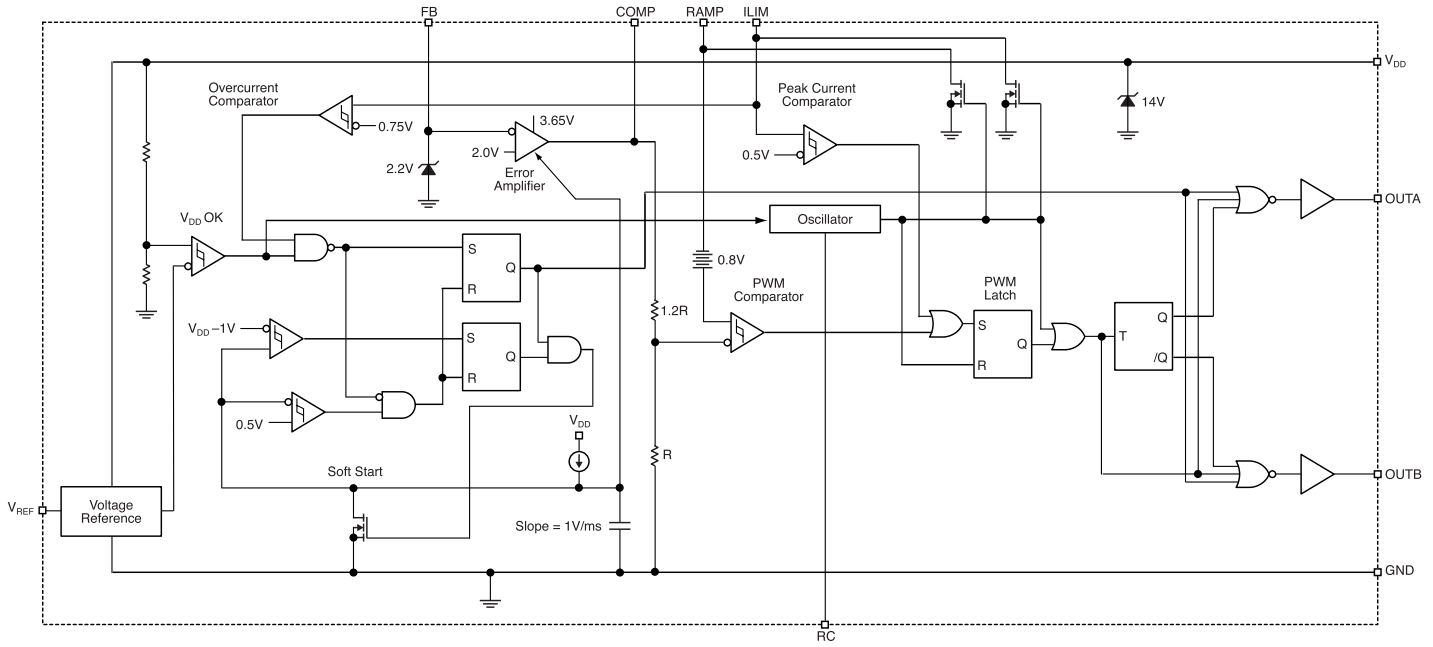


Figure 1. MIC3838 Block Diagram

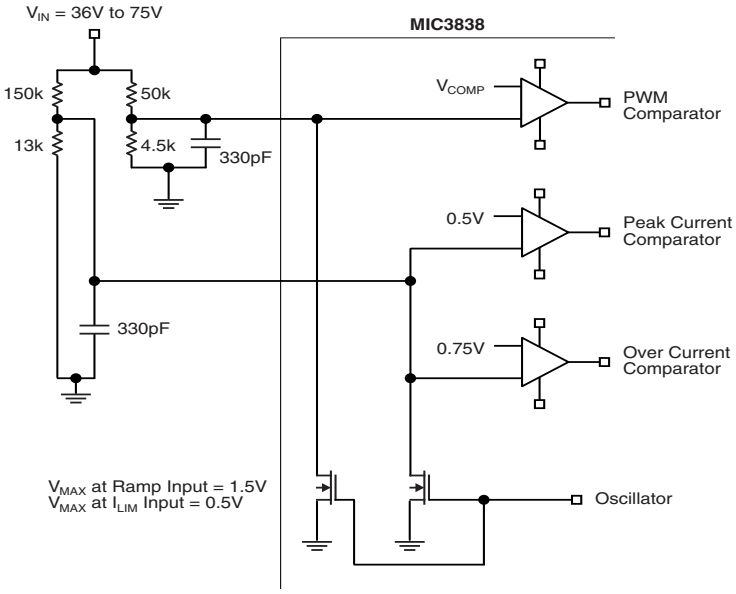


Figure 2. Volt Second Clamp and Voltage Feed Forward Circuit

Functional Description

The MIC3838/9 is a high-speed power supply controller with push-pull output drive capability. MIC3838 has a higher V_{DD} turn-on threshold and more hysteresis between V_{DD} turn-on and turn-off than the MIC3839. The outputs of the controller operate in a push-pull fashion with a guaranteed dead time between them. A block diagram of the MIC3838/9 controller is shown in Figure 1.

V_{DD} and Turn-on Sequence

The oscillator and output gate drive signals are disabled when V_{DD} is lower than the turn on threshold. Circuitry in the output drivers eliminates glitching or random pulsing during the start-up sequence. The oscillator is enabled when V_{DD} is applied and reaches the turn-on threshold. The V_{DD} comparator also turns off the internal soft-start discharge FET, slowly bringing up the COMP pin voltage.

The V_{DD} pin is internally clamped. As V_{DD} approaches this clamp voltage, the V_{DD} current will increase over the normal current draw of the IC. IDD currents greater than 20mA may cause excessive power dissipation in the MIC3838/9.

Soft Start

The soft start feature helps reduce surge currents at the power supply input source. An internal current source and capacitor ramp up from 0V to near V_{DD} at a typical rate of 1V/ms. The soft start feature limits the output voltage of the error amplifier at the COMP pin. As the soft start voltage rises, it allows the COMP pin voltage to rise, which in turn allows the duty cycle of the output drivers to increase. The internal soft start voltage is discharged and remains discharged during the following conditions:

1. The V_{DD} voltage drops below the turn-off threshold.
2. The voltage on the CS pin exceeds the overcurrent comparator threshold.

Once the internal soft start discharge FET is turned on, it cannot be turned off until the internal soft start voltage drops down below 0.5V. This insures a clean restart.

Oscillator

The oscillator operates at twice the switching frequency of either OUTA or OUTB. The oscillator generates a sawtooth waveform on the RC pin. The rising edge of the waveform is controlled by the external resistor/capacitor combination. The fall time is set by the on-resistance of the discharge FET (see Figure 3). The fall time sets the delay (dead time) between the turn-off of one output driver and the turn-on of the other driver. A toggle flip-flop insures that drive signals to OUTA and OUTB are alternated and therefore insures a maximum duty cycle of less than 50% for each output driver. Graphs of component values vs. oscillator frequency and dead time are shown in the typical characteristic section of this specification.

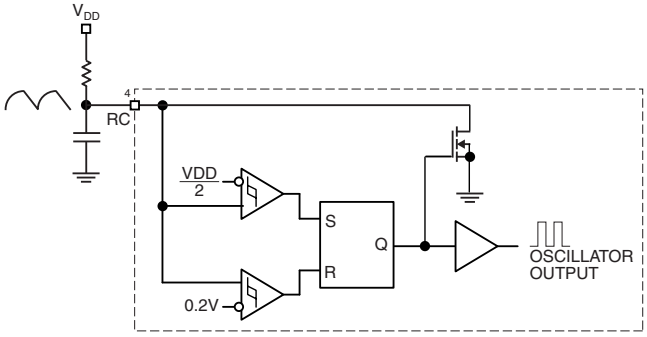


Figure 3. Oscillator

The voltage source to the resistor/capacitor timing components is V_{DD}. The internal turn-off comparator threshold in the oscillator circuit is $V_{DD}/2$. This allows the oscillator to track changes in V_{DD} and minimize frequency variations in the oscillator. The oscillator frequency can be roughly approximated using the following formula:

$$F_{OSCILLATOR} = \frac{1.41}{R \times C}$$

Where: frequency is in Hz
Resistance is in ohms
Capacitance is in Farads.

Graphs of oscillator frequency and dead time vs component values are shown in the Typical Characteristic section of this specification. The recommended range of timing resistors and capacitors is 7kΩ to 200kΩ and 100pF to 1000pF. To minimize oscillator noise and insure a stable waveform the following layout rules should be followed:

1. The higher impedance of capacitor values less than 100pF may causes the oscillator circuit to become more susceptible to noise. Parasitic pin and etch trace capacitances become a larger part of the total RC capacitance and may influence the desired switching frequency.
2. The circuit board etch between the timing resistor, capacitor, RC pin and ground must be kept as short as possible to minimize noise pickup and insure a stable oscillator waveform.
3. The ground lead of the capacitor must be routed close to the ground lead of the MIC3838/9.

Current Sensing and Overcurrent Protection

The features are:

- Peak current limit
- Overcurrent limit
- Internal current sense discharge
- Front edge blanking

In current mode control, a PWM comparator uses the inductor current signal and the error amplifier signal to determine the operating duty cycle. In the MIC3838/9 the signal at the CS pin is level shifted up before it reaches the PWM comparator as shown in Figure 1. This allows operation of the error amplifier and PWM comparator in a linear region.

There are two current limit thresholds in the MIC3838/9; peak current limit and overcurrent limit. The normal operating voltage at the I_{LIM} pin is designed less than these thresholds. A pulse-by-pulse current limit occurs when the inductor current signal at the I_{LIM} pin exceeds the peak current limit threshold. The on-time is terminated for the remainder of the switching cycle, regardless of whether OUTA or OUTB is active.

If the signal at the I_{LIM} pin goes past the peak threshold and exceeds the overcurrent limit threshold, the overcurrent limit comparator forces the soft start node to discharge and initiates a soft start reset.

An internal FET discharges the RAMP and I_{LIM} pins at the end of the oscillator charge time. The FET turns on when the voltage on the RC pin reaches the upper threshold ($V_{DD}/2$) and remains on for the duration of the RC pin discharge time and for typically 100ns after the start of the next on-time period. The 100ns period at the beginning of the on-time implements a front edge blanking feature that prevents false triggering of the PWM comparator due to noise spikes on the leading edge of the current turn-on signal. The front edge blanking also sets the minimum on-time for OUTA and OUTB. The timing diagram for the RAMP pin is shown in Figure 4.

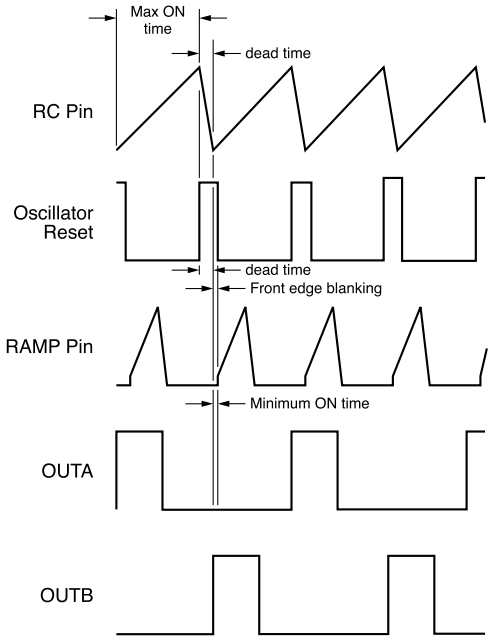


Figure 4. Timing Diagram

Error Amplifier

The error amplifier is part of the voltage control loop of the power supply. The FB pin is the inverting input to the error amplifier. The non-inverting input is internally connected to a reference voltage. The output of the error amplifier, COMP, is connected to the PWM comparator. A voltage divider between the error amplifier output (COMP pin) and the PWM comparator allows the error amplifier to operate in a linear region for better transient response. The output of the error amplifier (COMP pin) is clamped at typically 3.65V to prevent the COMP pin from rising up too high during startup or during a transient condition. This feature improves the transient response of the power supply.

Output Drivers

OUTA and OUTB are alternating output stages, which switch at half the oscillator frequency. A toggle flip-flop in the MIC3838/9 guarantee both outputs will not be on at the same time. The RC discharge time is the dead time, where both outputs are off. This provides an adjustable non-overlap time to prevent shoot through currents and transformer saturation in the power supply.

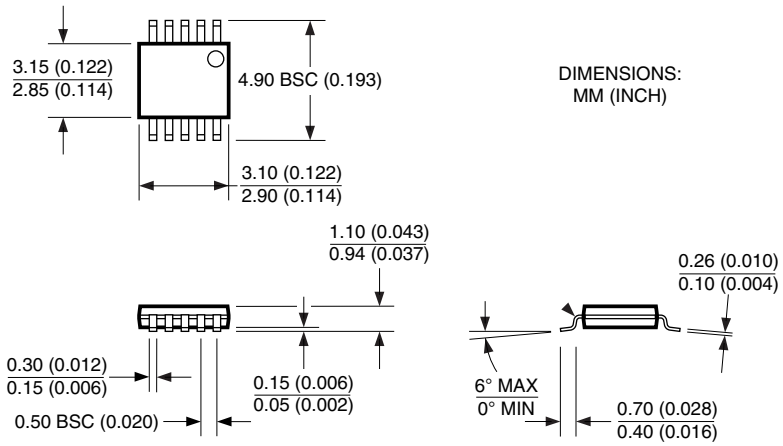
The output drivers are inhibited when V_{DD} is below the undervoltage threshold. Internal circuitry prevents the output drivers from glitching high when V_{DD} is first applied to the MIC3838/9 controller.

Decoupling and PCB Layout

PCB layout is critical to achieve reliable, stable and efficient operation. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. The following guidelines should be followed to insure proper operation of the circuit:

- Low level signal and power grounds should be kept separate and connected at only one location, preferably the ground pin of the control IC. The ground signals for the current sense, voltage feedback and oscillator should be grouped together. The return signals for the gate drives should be grouped together and a common connection made at the ground pin of the controller. The low level signals and their returns must be kept separate from the high current and high voltage power section of the power supply.
- Avoid running sensitive traces, such as the current sense and voltage feedback signals next to or under power components, such as the switching FETs and transformer.
- If a current sense resistor is used, it's ground end must be located very close to the ground pin of the MIC3838/9 controller. Careful PCB layout is necessary to keep the high current levels in the current sense resistor from running over the low level signals in the controller.
- A minimum 1μF bypass capacitor must be connected directly between the V_{DD} and GND pins of the MIC3838/9. An additional 0.1μF capacitor between the V_{DD} end of the oscillator frequency setting resistor and the ground end of the oscillator capacitor may be necessary if the resistor is a distance away from the main 1μF bypass capacitor

Package Information



10-Pin MSOP (MM)

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