

MC74HC164B

8-Bit Serial-Input/Parallel-Output Shift Register

High-Performance Silicon-Gate CMOS

The MC74HC164B is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC74HC164B is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs. Schmitt-trigger action at the Clock input enhances the device's tolerance to slower rise and fall times and immunity to noise of the input clock signal.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 V to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7-A Requirements
- Chip Complexity: 244 FETs or 61 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



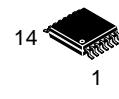
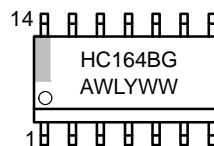
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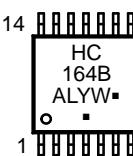
MARKING DIAGRAMS



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

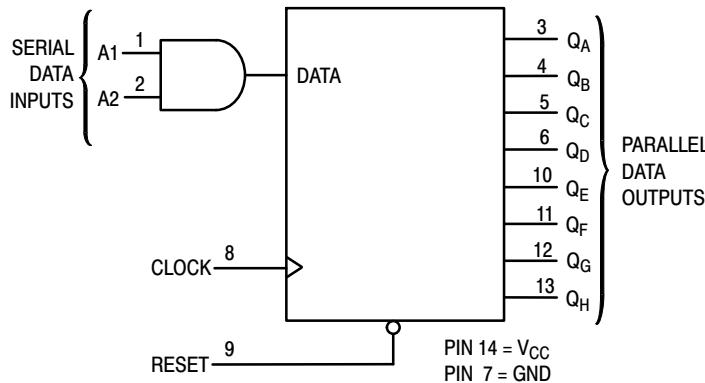
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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PIN ASSIGNMENT

A1	1	14	V _{CC}
A2	2	13	Q _H
Q _A	3	12	Q _G
Q _B	4	11	Q _F
Q _C	5	10	Q _E
Q _D	6	9	RESET
GND	7	8	CLOCK

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Outputs				
Reset	Clock	A1 A2	Q _A	Q _B	...	Q _H	
L	X	X X	L	L	...	L	
H	~	X X					No Change
H	~	H D	D	Q _{An}	...	Q _{Gn}	
H	~	D H	D	Q _{An}	...	Q _{Gn}	

D = data input

Q_{An} – Q_{Gn} = data shifted from the preceding stage on a rising edge at the clock input.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC164BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74HC164BDR2G		2500 / Tape & Reel
NLV74HC164BDR2G*		2500 / Tape & Reel
MC74HC164BDTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC164BDTR2G*		2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Package TSSOP Package	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V	
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C	
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	No Limit No Limit No Limit	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V_{T+} max	Maximum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1V$ $ I_{out} \leq 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	V
V_{T+} min	Minimum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1V$ $ I_{out} \leq 20\mu A$	2.0 3.0 4.5 6.0	1.0 1.5 2.3 3.0	0.95 1.45 2.25 2.95	0.95 1.45 2.25 2.95	V
V_{T-} max	Maximum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $ I_{out} \leq 20\mu A$	2.0 3.0 4.5 6.0	0.9 1.4 2.0 2.6	0.95 1.45 2.05 2.65	0.95 1.45 2.05 2.65	V
V_{T-} min	Minimum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $ I_{out} \leq 20\mu A$	2.0 3.0 4.5 6.0	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	V
V_{Hmax} (Note 1)	Maximum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{out} \leq 20\mu A$	2.0 3.0 4.5 6.0	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	V
V_{Hmin} (Note 1)	Minimum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{out} \leq 20\mu A$	2.0 3.0 4.5 6.0	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 2.4$ mA $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 2.4$ mA $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $V_{Hmin} > (V_{T+} \text{ min}) - (V_{T-} \text{ max})$; $V_{Hmax} = (V_{T+} \text{ max}) - (V_{T-} \text{ min})$.

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AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	10 20 40 50	10 20 35 45	10 20 30 40	MHz
$t_{PLH},$ t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 3.0 4.5 6.0	160 100 32 27	200 150 40 34	250 200 48 42	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	175 100 35 30	220 150 44 37	260 200 53 45	ns
$t_{TLH},$ t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$			pF	
		180				

TIMING REQUIREMENTS (Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0 3.0 4.5 6.0	25 15 7 5	35 20 8 6	40 25 9 6	ns
t_h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	50 26 12 10	60 35 15 12	75 45 20 15	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	50 26 12 10	60 35 15 12	75 45 20 15	ns

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 1, 2)

Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data-enable input. When only one serial input is used, the other must be connected to V_{CC}.

Clock (Pin 8)

Shift Register Clock. A positive-going transition on this pin shifts the data at each stage to the next stage. The shift

register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

Q_A – Q_H (Pins 3, 4, 5, 6, 10, 11, 12, 13)

Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

CONTROL INPUT

Reset (Pin 9)

Active-Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip-flops and sets Outputs Q_A – Q_H to the low level state.

SWITCHING WAVEFORMS

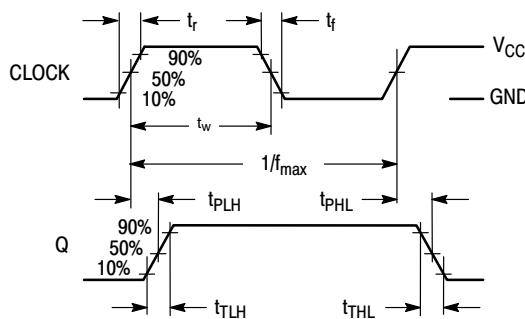


Figure 1.

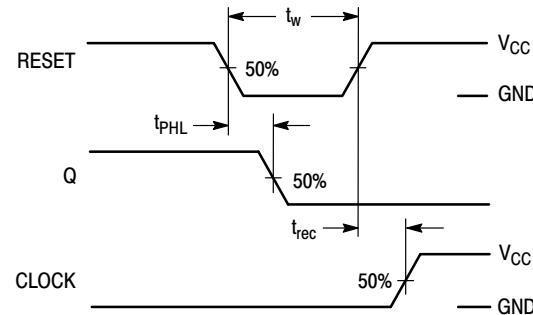


Figure 2.

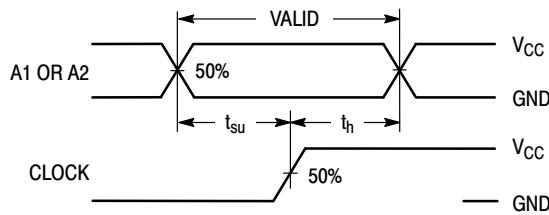
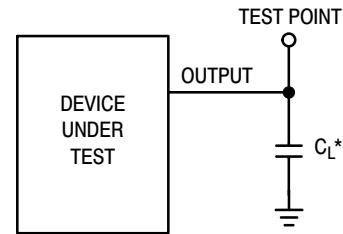


Figure 3.

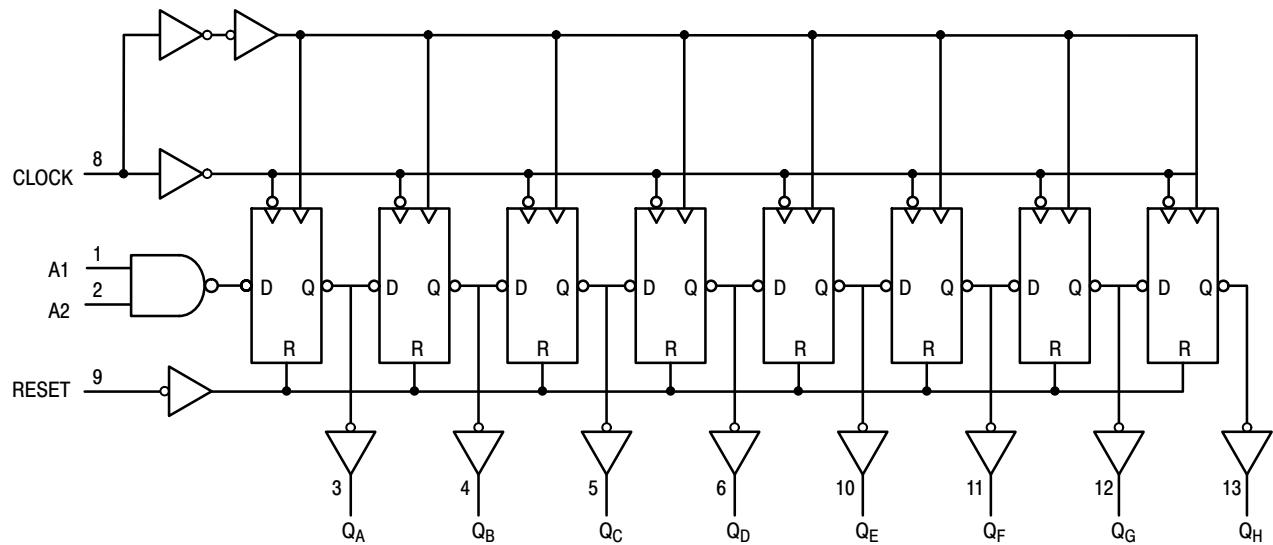


*Includes all probe and jig capacitance

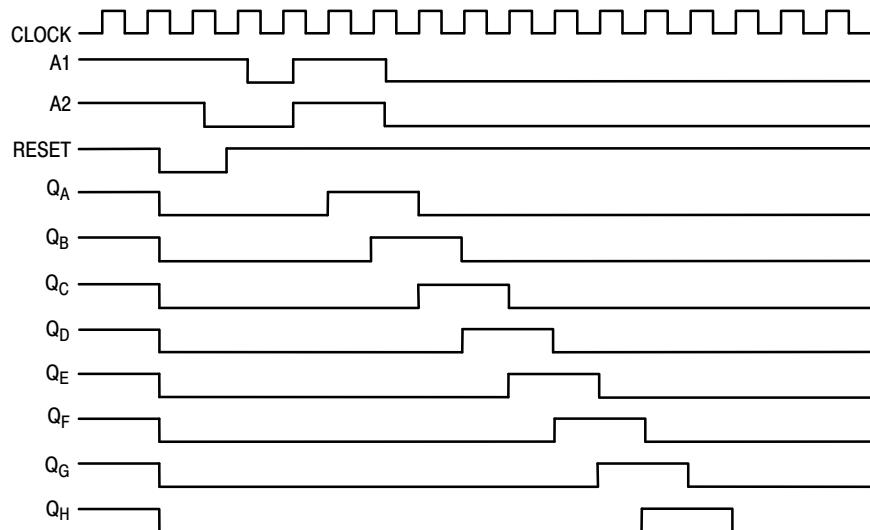
Figure 4. Test Circuit

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EXPANDED LOGIC DIAGRAM

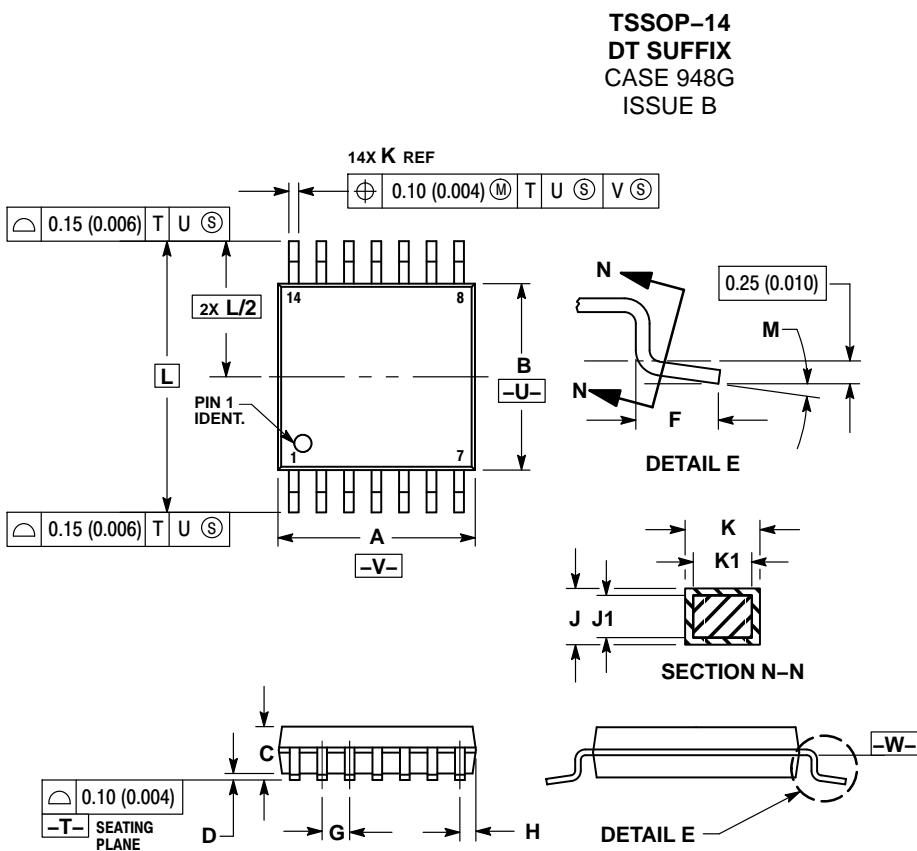


TIMING DIAGRAM



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PACKAGE DIMENSIONS

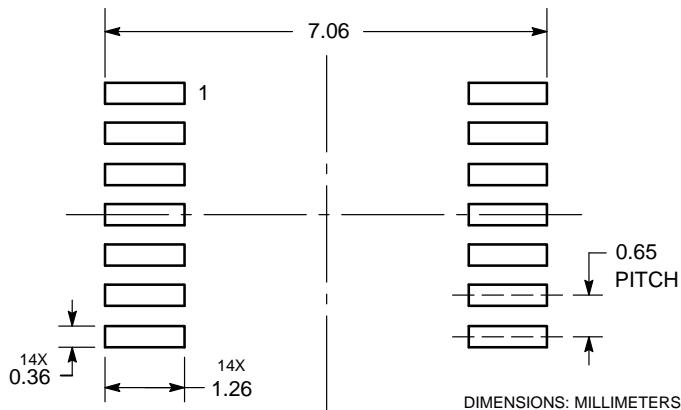


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

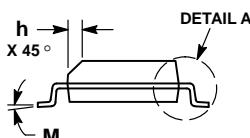
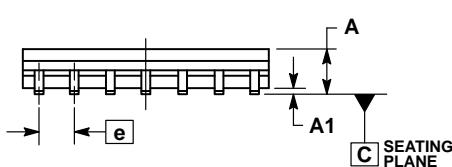
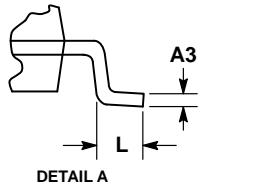
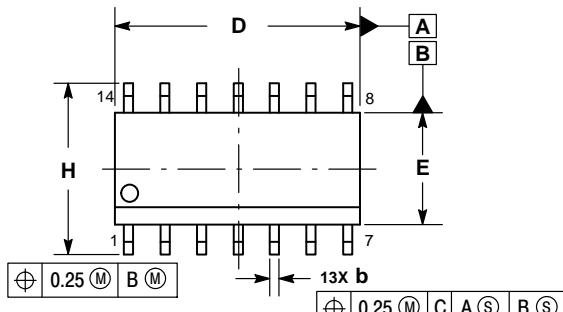


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC164B

PACKAGE DIMENSIONS

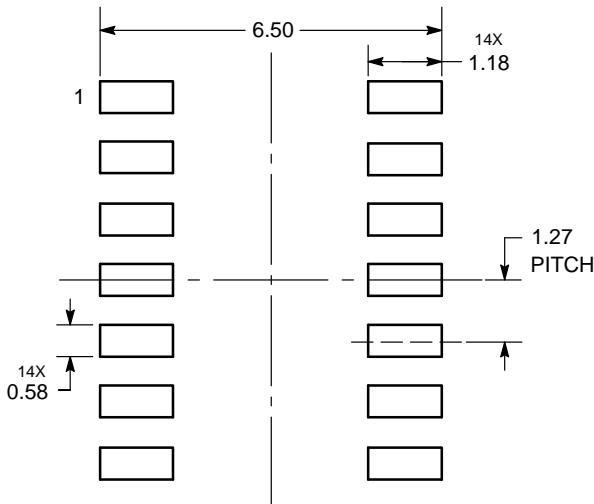
SOIC-14 NB
CASE 751A-03
ISSUE K



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC	—	0.050 BSC	—
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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"LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибуторских договоров

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Работу по проектам и поставку образцов.
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Конструкторский отдел помогает осуществить:

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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