zilog
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An IXYS Company

CMOS Z8 16K/32K EPROM MCUs

Z86E61/Z86E63 Microcontrollers

Product Specification

PS014404-0212

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Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page
Feb 2012	04	Globally updated for style and content.	All
Oct 2008	03	Updated pin descriptions.	11
May 2008	02	Added LQFP pin diagram (Standard and Programming modes); replaced 44-pin QFP with 44-pin LQFP for CR #10886.	7, 8
Nov 2001	01	Original issue.	All

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Overview

The Z86E61/Z86E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32KB of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP, 44-pin PLCC or 44-pin LQFP package styles, these devices are pin-compatible EPROM versions of the Z86C61/ 63. The ROMless pin option is available on the 44-pin versions only.

With 16KB/32KB of ROM and 236 bytes of general-purpose RAM, the Z86E61/Z86E63 MCU offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/Z86E63 MCU offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E61/Z86E63 MCU can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required. There are three basic address spaces available to support this configuration:

- Program memory
- Data memory
- 236 General-purpose registers

Features

The Z86E61 and Z86E63 MCUs offer the following features:

- 8-Bit CMOS microcontroller
- 40-pin DIP, 44-pin PLCC and 44-pin LQFP packages
- 4.5V to 5.5V operating range
- Clock speeds: 16MHz and 20MHz
- Low power consumption: 275 mW (max)
- Two Standby modes: STOP and HALT
- 32 Input/Output lines
- Full-duplex UART
- All digital inputs are TTL levels

- Auto Latches
- High-voltage protection on high-voltage inputs
- RAM and EPROM Protect
- EPROM:
  - 16KB Z86E61
  - 32KB Z86E63

- 256-byte Register File:
  - 236 bytes of General-Purpose RAM
  - 16 bytes of Control and Status registers
  - 4 bytes for ports

- Two programmable 8-bit Counter/Timers, each with 6-bit programmable prescaler
- Six vectored priority interrupts from eight different sources
- On-chip oscillator that accepts a crystal ceramic resonator, LC or external clock drive

To unburden the system from coping with real-time tasks such as counting/timing and serial data communication, the Z86E61/Z86E63 MCU offers two on-chip counter/timers with a large number of user selectable modes. See the block diagram in Figure 1.

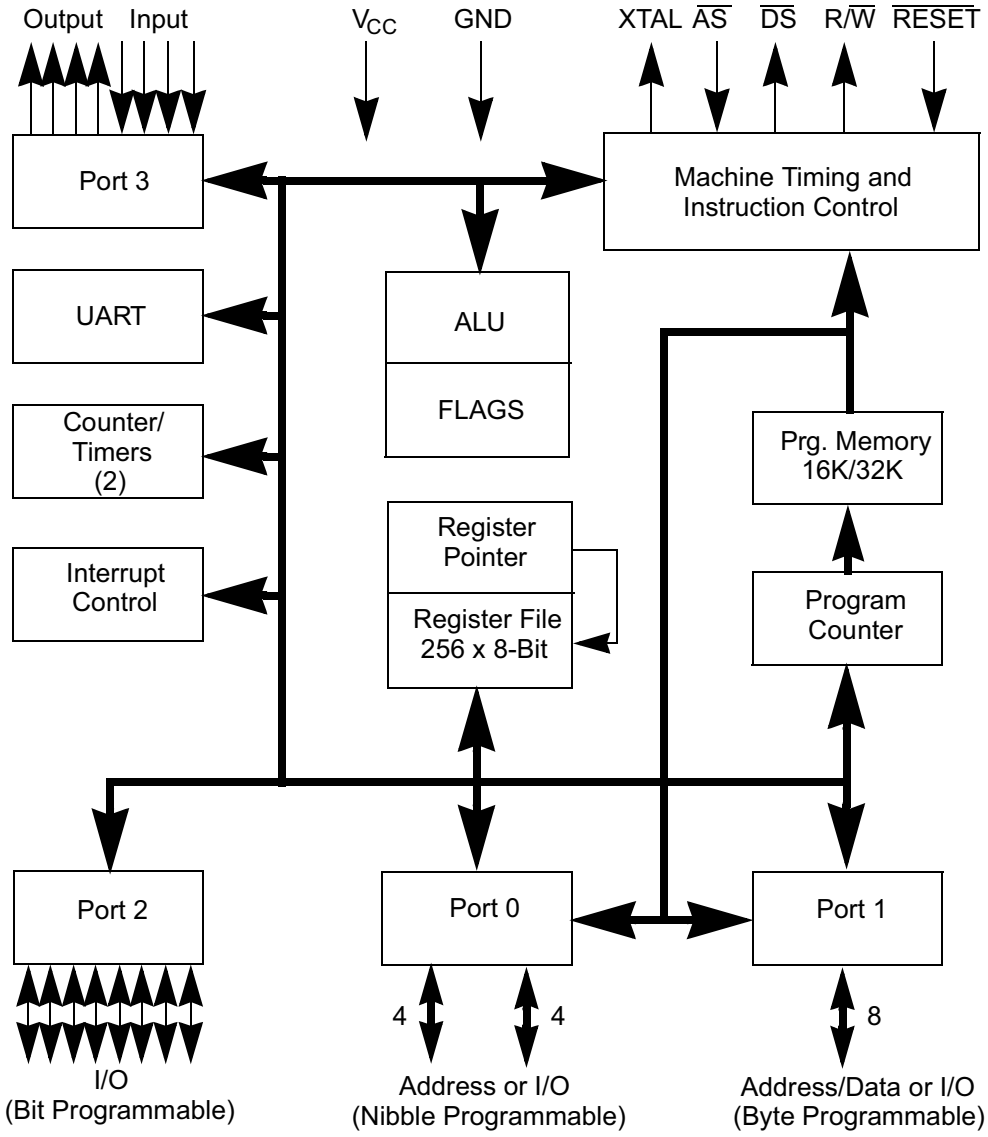


Figure 1. Z86E61/Z86E63 MCU Functional Block Diagram

Power connections follow the conventional descriptions listed in Table 24.

Table 24. Power Connection Conventions

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Pin Functions

The Z86E61/Z86E63 MCU is available in variety of package styles, programming modes and pin configurations. This section describes the pin signals and configurations for each of the 40-pin PDIP, 44-pin PLCC and 44-pin LQFP packages in both Standard and EPROM Programming modes.

Pin Signals

Figure 2 shows the pin-outs for the 40-pin PDIP Standard Mode package; Table 25 describes each pin.

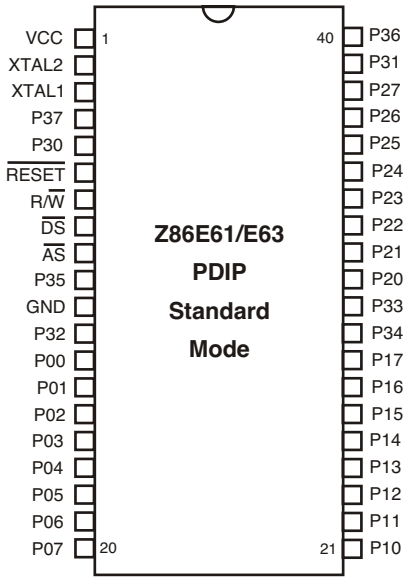


Figure 2. Z86E61/Z86E63 PDIP Pin Diagram, Standard Mode

Table 25. Z86E61/Z86E63 PDIP Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output

Table 25. Z86E61/Z86E63 PDIP Pin Description, Standard Mode (Continued)

Pin Signal	Description	I/O
$\overline{DS}$	Data Strobe	Output
$\overline{AS}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{RL}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 3 shows the pin-outs for the 40-pin PDIP EPROM Programming Mode package; Table 26 describes each pin.

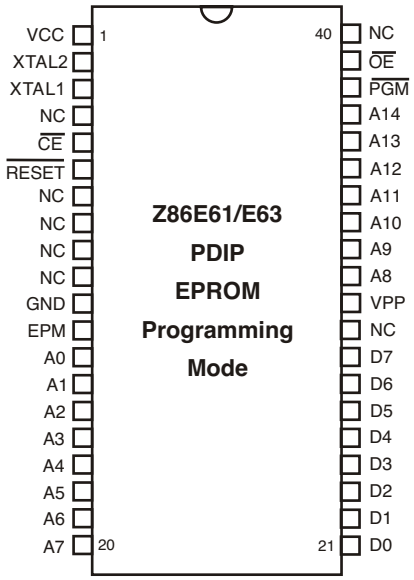


Figure 3. Z86E61/Z86E63 PDIP Pin Diagram, EPROM Programming Mode

Table 26. Z86E61/Z86E63 PDIP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 4 shows the pin-outs for the 44-pin LQFP Standard Mode package; Table 27 describes each pin.

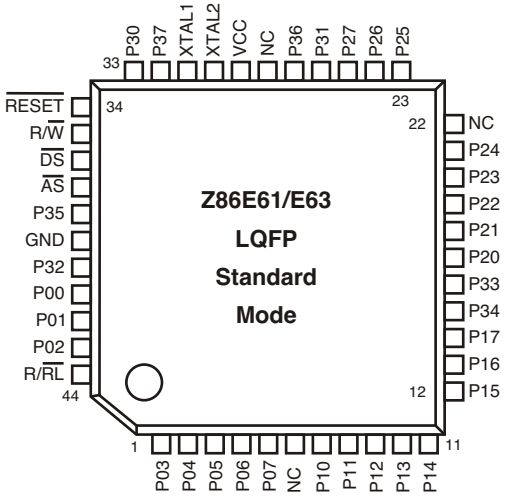


Figure 4. Z86E61/Z86E63 LQFP Pin Diagram, Standard Mode

Table 27. Z86E61/Z86E63 LQFP Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 5 shows the pin-outs for the 44-pin LQFP EPROM Programming Mode package; Table 28 describes each pin.

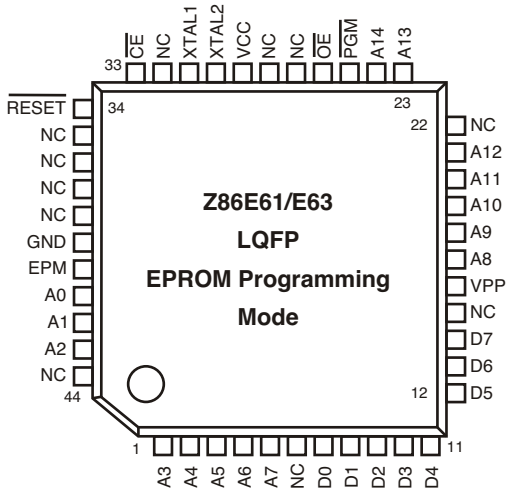


Figure 5. Z86E61/Z86E63 LQFP Pin Diagram, EPROM Programming Mode

Table 28. Z86E61/Z86E63 LQFP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 6 shows the pin-outs for the 44-pin PLCC Standard Mode package; Table 29 describes each pin.

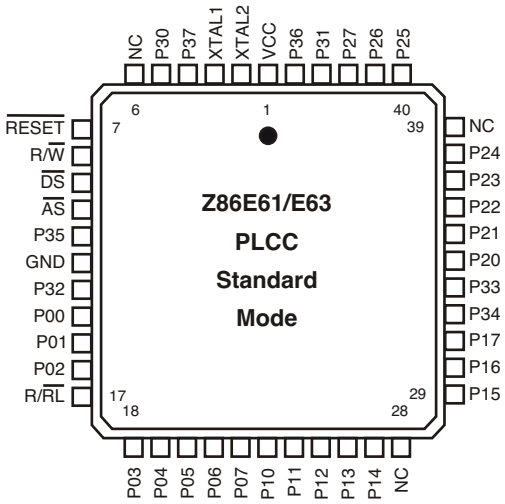


Figure 6. Z86E61/Z86E63 PLCC Pin Diagram, Standard Mode

Table 29. Z86E61/Z86E63 PLCC Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 7 shows the pin-outs for the 44-pin PLCC EPROM Programming Mode package; Table 30 describes each pin.

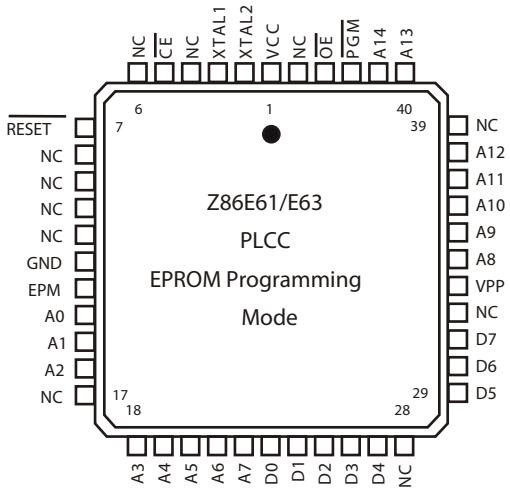


Figure 7. Z86E61/Z86E63 PLCC Pin Diagram, EPROM Programming Mode

Table 30. Z86E61/Z86E63 PLCC Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Pin Descriptions

This section describes the major Z86E61/Z86E63 MCU pin signals and ports.

ROMless (Input, Active Low)

Connecting this pin to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (see the Z86C91 product specification for more information). When pulled High to V_{CC}, the device functions as a normal Z86E61/Z86E63 EPROM version. This pin is only available on the 44-pin versions of the Z86E61/Z86E63 MCU.

DS (Output, Active Low)

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of DS. For WRITE operations, the falling edge of DS indicates that output data is valid.

AS (Output, Active Low)

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of AS. Under program control, AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL2, XTAL1

Crystal 2, Crystal 1 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (Output, Write Low)

The Read/Write signal is Low when the MCU is writing to the external program or data memory.

RESET (Input, Active Low)

To avoid asynchronous and noisy reset problems, the Z86E61/Z86E63 MCU is equipped with a reset filter of four external clocks (4TpC). If the external RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external RESET, whichever is longer. During the reset cycle, DS is held active Low while AS cycles at a rate of TpC/2. When RESET is deactivated, program execution begins at location `000Ch`. Power-up reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07–P00)

Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode Register.

In ROMless Mode, after a hardware reset, the Port 0 lines are defined as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode; see Figure 8.

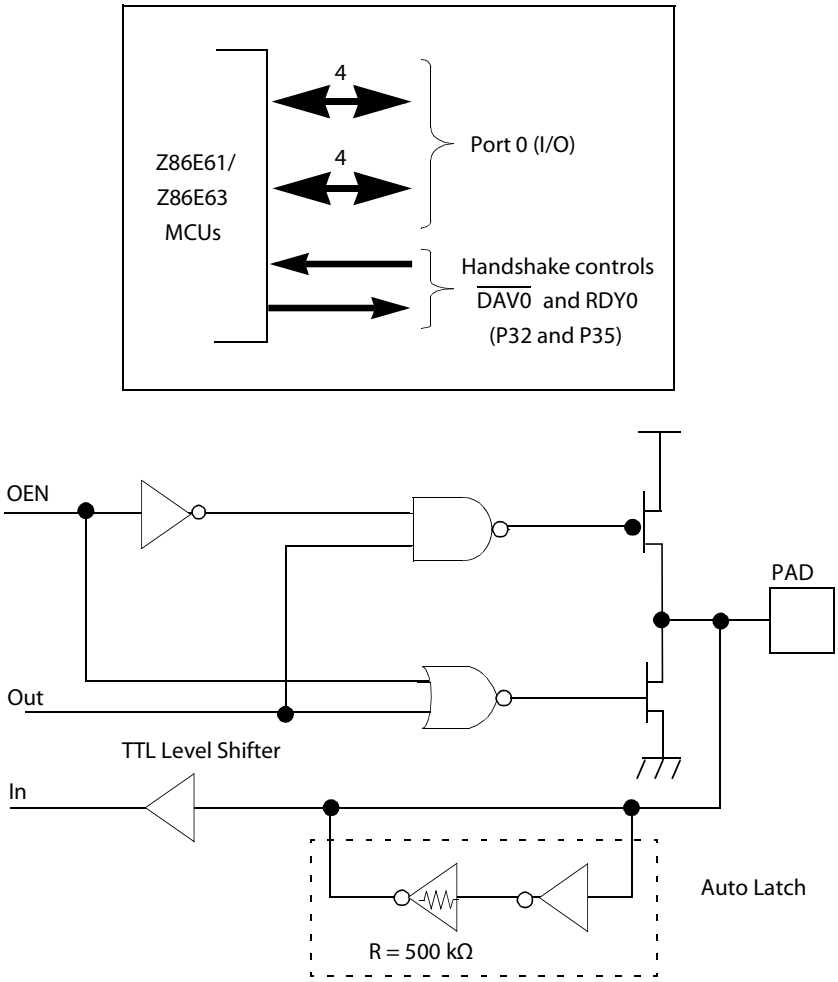


Figure 8. Port 0 Configuration

Port 1 (P17–P10)

Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7–A0) and Data (D7–D0) ports. For the Z86E61/Z86E63 MCU, these eight I/O lines can be programmed as input or output lines or are configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls RDY1 and DAV1.

Memory locations greater than 16384 (Z86E61) or 32768 (Z86E63) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multi-

plexed Address/ Data Mode. If more than 256 external locations are required, Port 0 must output the additional address lines.

Port 1 can be placed in high-impedance state along with Port 0, AS, DS, and R/W, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output; see Figure 9.

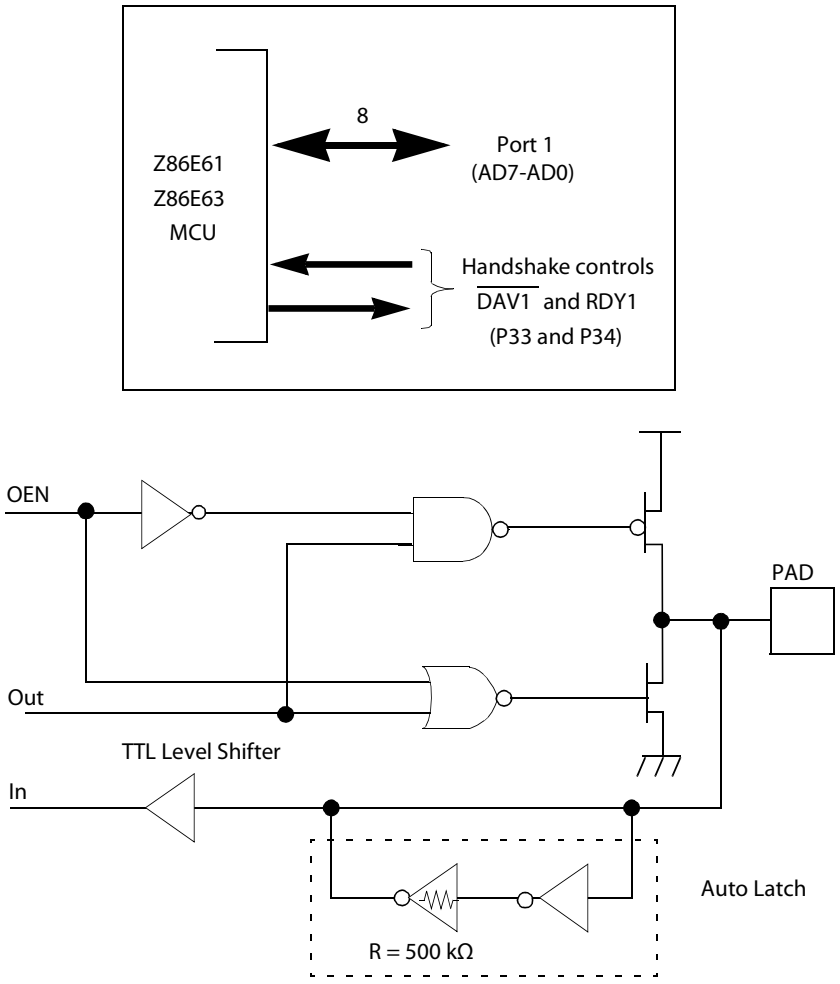


Figure 9. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bit programmable, bi-directional, CM0S compatible port. Each of these eight I/0 lines can be independently programmed as an input or output, or globally as an

open-drain output. Port 2 is always available for I/ 0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27; see Figure 10 and Table 31 on page 16).

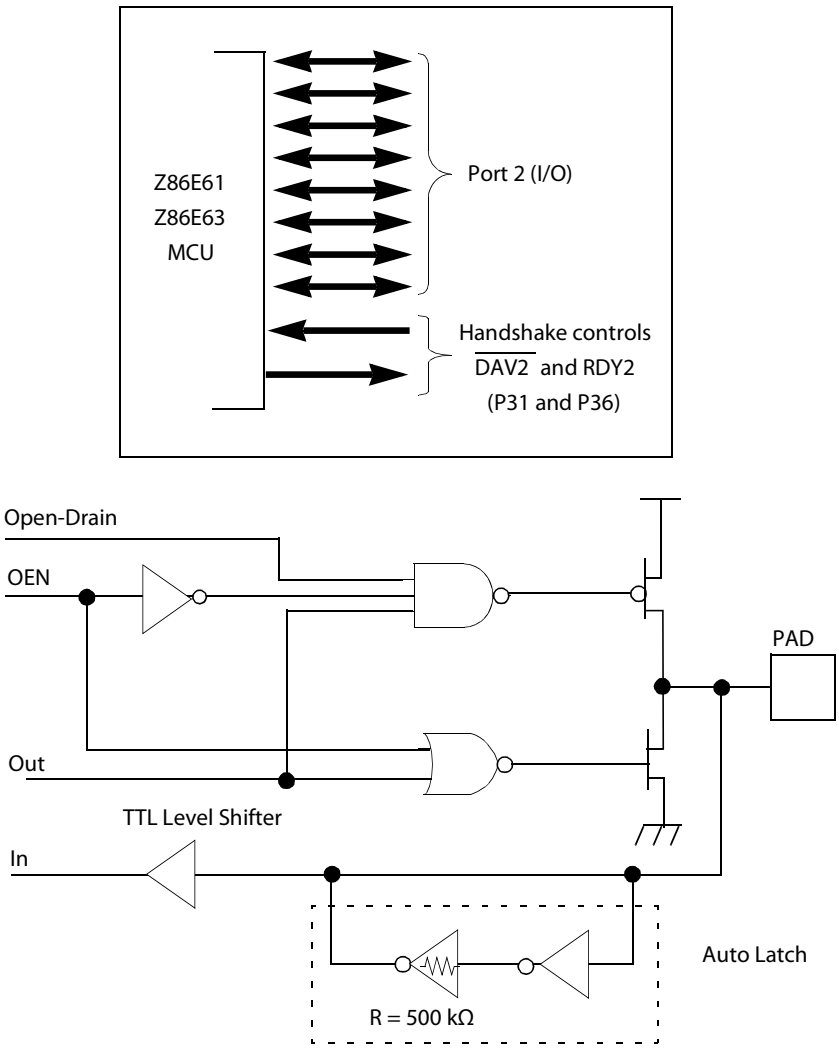


Figure 10. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33–P30) input and four-fixed (P37–P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively; see Figure 11.

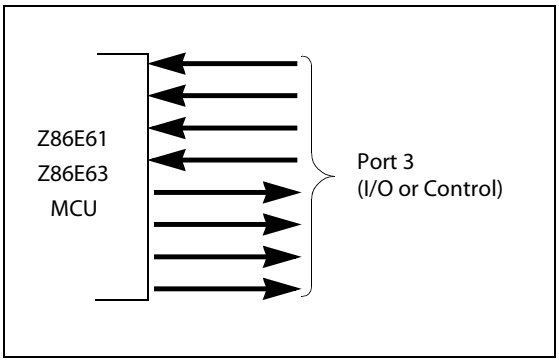


Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}) Data Memory Select ($\overline{DM}$) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = V_{PP}).

Table 31 lists the pin assignments for Port 3.

Table 31. Port 3 Pin Assignments*

Pin	I/O	CTCI	Interrupt	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	In	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	In	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	In	T_{IN}	IRQ0	D/R					EPM
P33	In	T_{IN}	IRQ1		D/R				V_{PP}
P34	Out	T_{OUT}			R/D			$\overline{DM}$	
P35	Out	T_{OUT}		R/D					
P36	Out	T_{OUT}				R/D			
P37	Out	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

Note: *HS = Handshake Signals; D = Data Available; R = Ready.

UART Operation. Port 3 lines, P37 and P30, are programmed as serial I/0 lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/ Timer0.

The Z86E61/Z86E63 MCU automatically adds a start bit and two stop bits to transmitted data; see Figure 12. Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

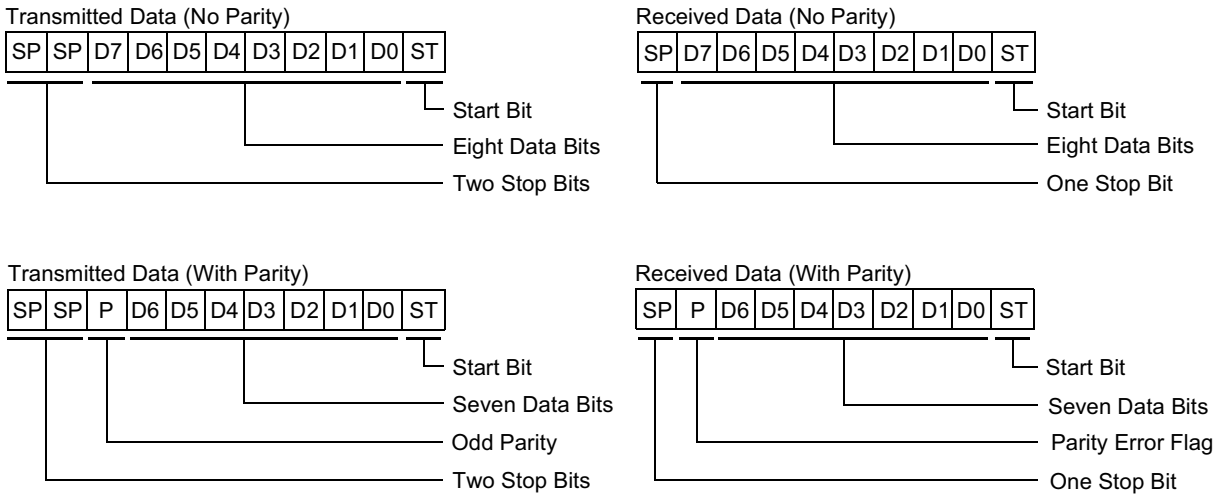


Figure 12. Serial Data Formats

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33–P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM Mode.

Address Space

This section describes the memory and addressing functions of the Z86E61/Z86E63 MCU.

Program Memory

The Z86E61/Z86E63 MCU can address 48KB (Z86E61) or 32KB (Z86E63) of external program memory; see Figure 13. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM Mode, byte 13 to byte 16383 (Z86E61) or 32767 (Z86E63) consists of on-chip EPROM. At addresses 16384 (Z86E61) or 32768 (Z86E63) and above, the Z86E61/Z86E63 MCU executes external program memory fetches. In ROMless Mode, the Z86E61/Z86E63 MCU can address up to 64KB of program memory. Program execution begins at external location 000C (HEX) after a reset.

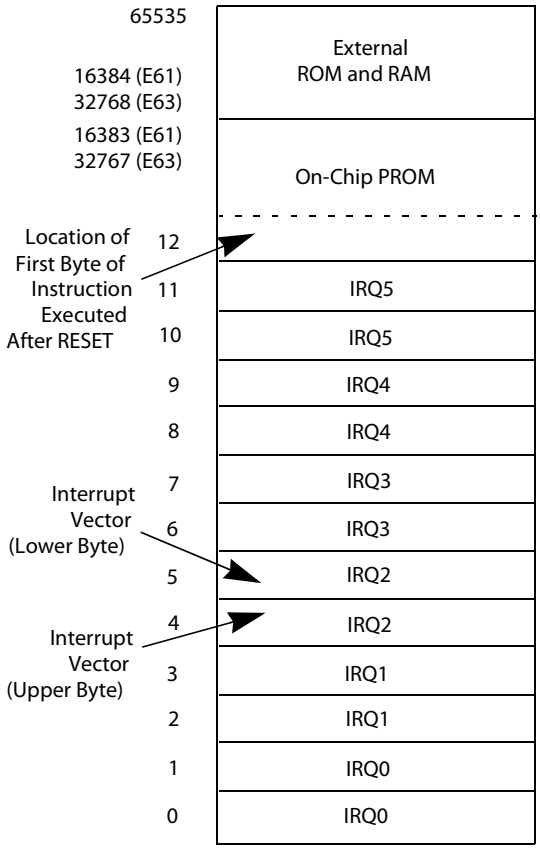


Figure 13. Program Memory Configuration

Data Memory

The EPROM version can address up to 48KB (Z86E61) or 32KB (Z86E63) of external data memory (DM) space beginning at location 16384 (Z86E61) or 32768 (Z86E63). The ROMless version can address up to 64KB of external data memory. External data memory may be included with, or separated from, the external program memory space. DM, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space; see Figure 14. The state of the DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (DM inactive) memory, and an LDE instruction references DATA (DM active Low) memory.

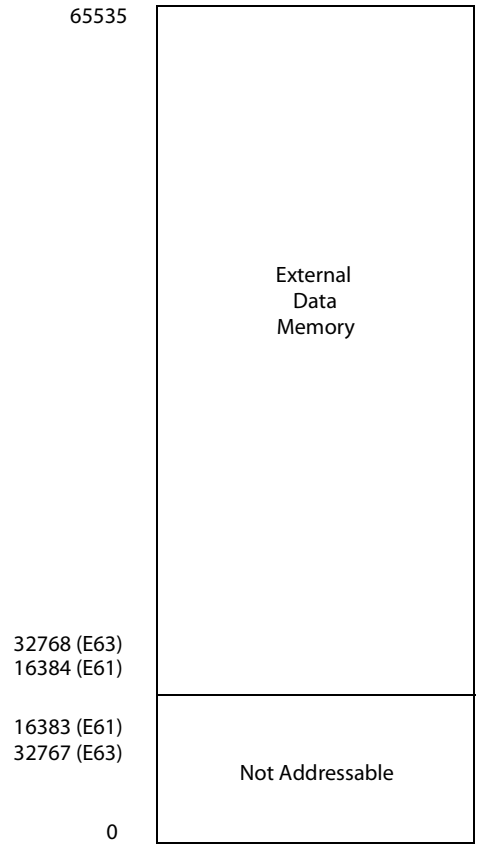


Figure 14. Data Memory Configuration

Register File

The register file consists of four I/0 port registers, 236 general-purpose registers, and 16 control and status registers, as shown in Figure 15. The instructions can access registers directly or indirectly through an 8-bit address field. The Z86E61/Z86E63 MCU also allows short 4-bit register addressing using the Register Pointer, which is shown in Figure 16. In 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

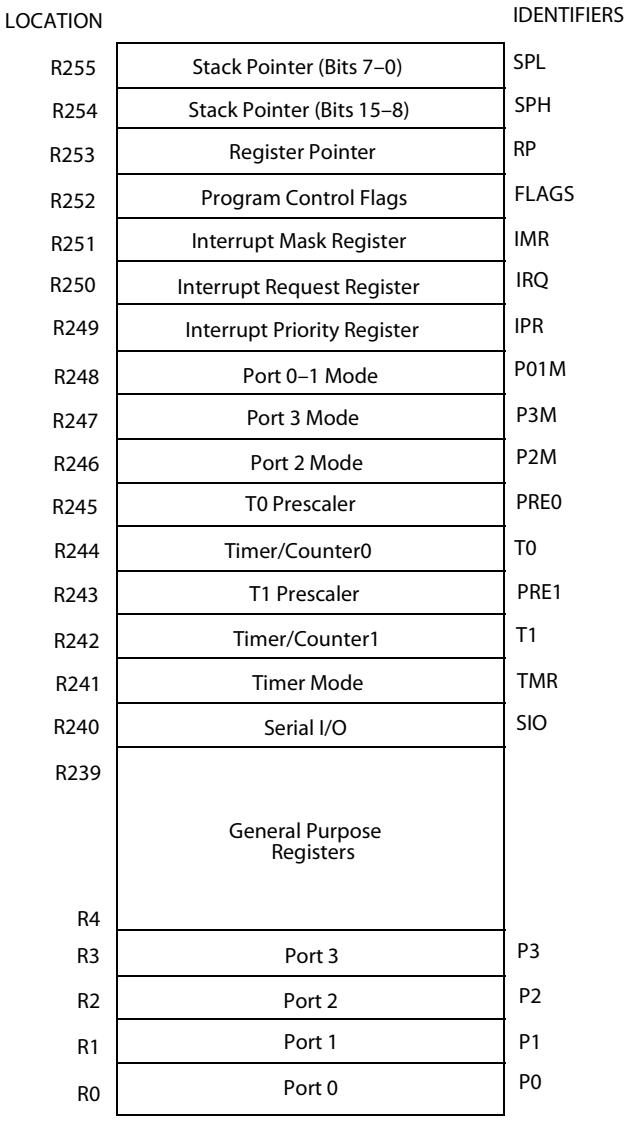


Figure 15. Register File

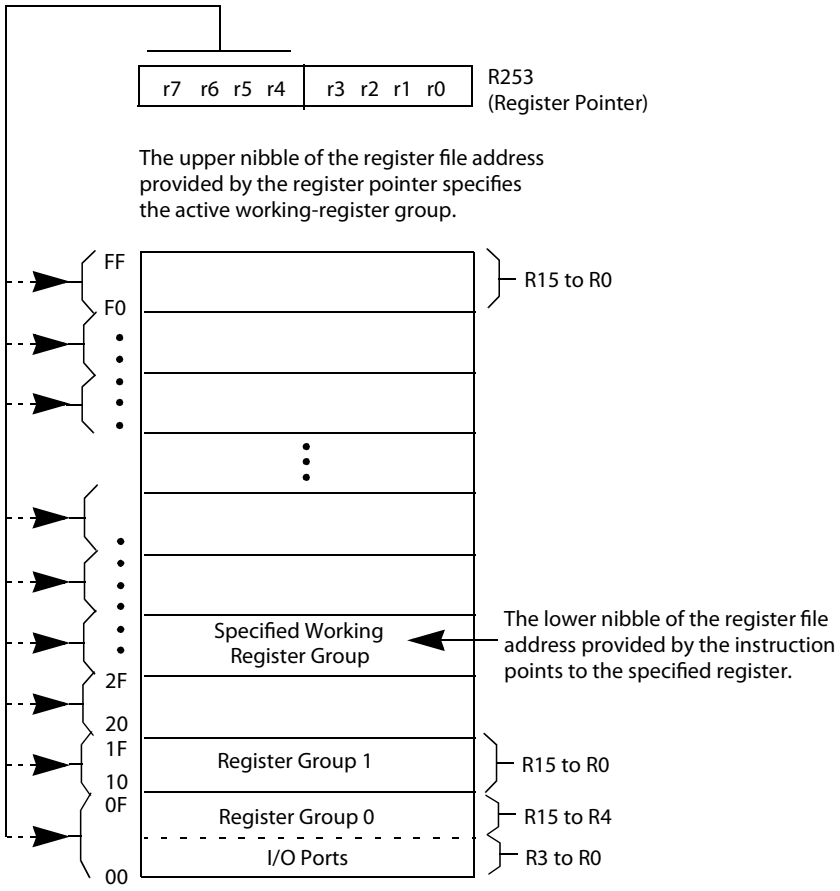


Figure 16. Register Pointer

Stack

The Z86E61/Z86E63 MCU has a 16-bit Stack Pointer (R255–R254) used for external stacks that reside anywhere in the data memory for the ROMless Mode, but only from 16384 (Z86E61) or 32768 (Z86E63) to 65535 in the EPROM Mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239–R4). The high byte of the Stack Pointer (SPH Bits 15–8) can be use as a general-purpose register when using internal stack only.

Functional Description

This section describes the counter/timer, interrupt, clock and timer mode functions of the Z86E61/Z86E63 MCU.

Counter/Timers

There are two 8-bit programmable counter/timers (T0–T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only, as shown in Figure 17.

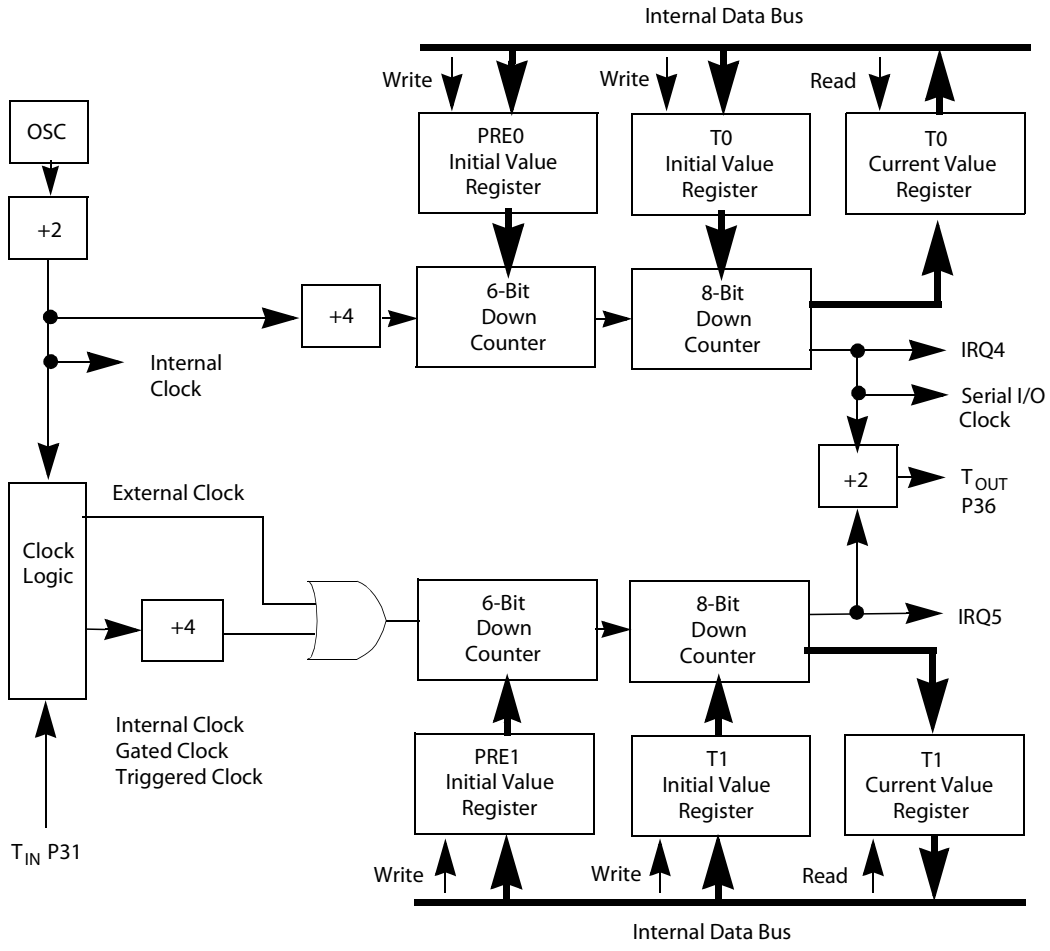


Figure 17. Counter/Timers Block Diagram

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (Single Pass Mode) or to automatically reload the initial value and continue counting (Modulo-n Continuous Mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

Interrupts

The Z86E61/Z86E63 MCU has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and two in the counter/timers; see Figure 18. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register; see Figure 40 on page 48.

All Z86E61/Z86E63 MCU interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

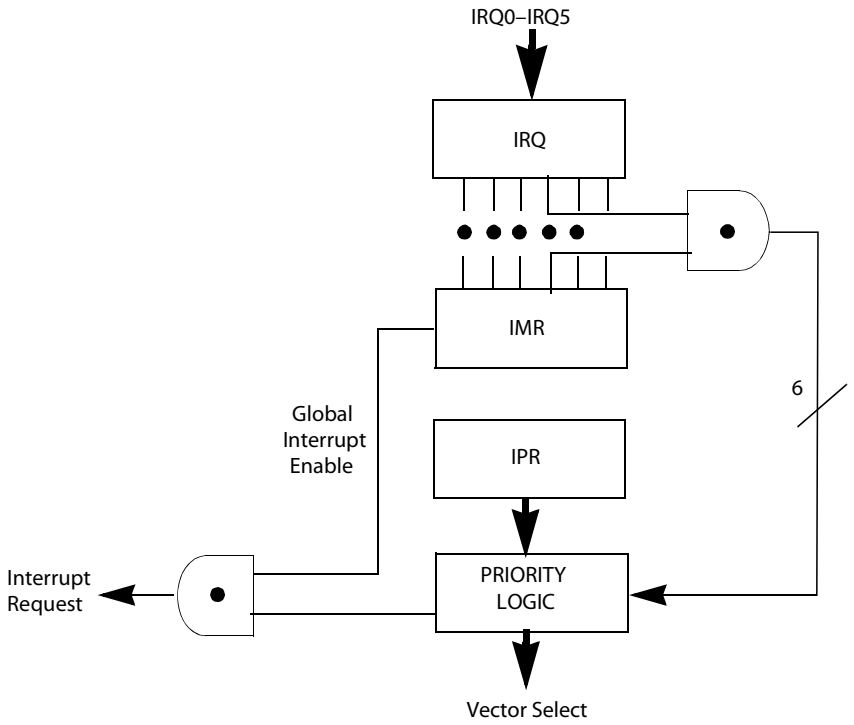


Figure 18. Interrupt Block Diagram

For the ROMless Mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the Flag Register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

Clock

The Z86E61/Z86E63 MCU's on-chip oscillator features a high gain, parallel resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max; series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground; see Figure 19.

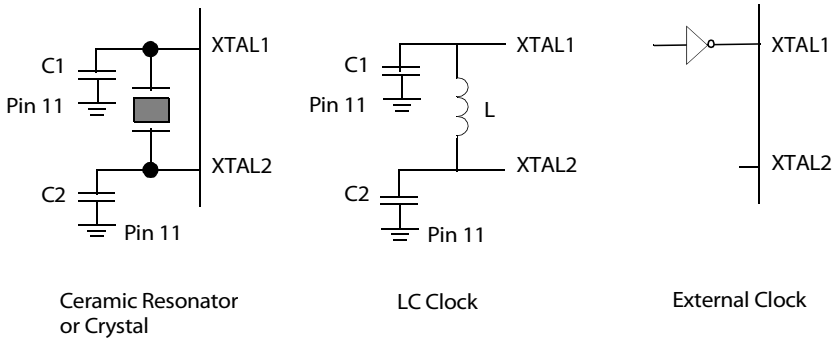


Figure 19. Oscillator Configuration

Note: The actual capacitor value is specified by the crystal manufacturer.

HALT

Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation, and reduces the standby current to 5µA (typical) or less. The STOP Mode is terminated by a reset, which causes the processor to restart the application program at address 000Ch.

To enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = 0FFH) immediately before the appropriate SLEEP instruction, as shown in the following code segment.

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP Mode
 or
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

Programming

This section describes the five user program modes available for programming the Z86E61/Z86E63 MCU, including signal descriptions for programming or reading the Z86E63 device.

Z86E61/Z86E63 User Modes

The Z86E61/Z86E63 MCU uses separate AC timing cycles for the different user modes available. Table 32 shows the Z86E61/Z86E63 MCU's user modes; Table 33 shows the timing of the programming waveforms.

Table 32. OTP Programming[1]

User/Test Mode	Device Pins							
Device Pin No.	P33	P32	P30	P31	P20			Port 1 Config Data
User Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	V_{CC}	
EPROM Read	Z[2]	V_H[3]	V_{IL}[4]	V_{IL}	V_{IH}	Addr	5.0V	Out
Program	V_{PP}[5]	V_{IH}	V_{IL}	V_{IH}[6]	V_{IL}	Addr	6.0V	In
Program Verify	V_{PP}[5]	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Addr	6.0V	Out
EPROM Protect	V_{PP}[5]	V_H	V_H	V_{IH}	V_{IL}	X[7]	6.0V	X
RAM Protect	V_{PP}	V_{IH}	V_H	V_{IH}	V_{IL}	X	6.0V	X

Notes:
1. I_{PP} during programming = 40 mA maximum; I_{CC} during programming, verify or read = 40 mA maximum.
2. Z = V_{IL} or V_{IH}.
3. V_H = 12.0 ± 0.5V.
4. V_{IL} = 0V.
5. V_{PP} = 12.0 ± 0.5V.
6. V_{IH} = 5V.
7. X = Not used in this mode.

Table 33. Timing of Programming Waveforms

Parameters	Name	Min	Max	Unit
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup Time	2		µs
4	V_{CC} Setup time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		µs

Table 33. Timing of Programming Waveforms (Continued)

Parameters	Name	Min	Max	Unit
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms

User MODE 1: EPROM Read

The Z86E61/Z86E63 EPROM read cycle is provided so that the user may read the Z86E61/Z86E63 MCU as a standard 27128 (Z86E61) or 27256 (Z86E63) EPROM. This is accomplished by driving the EPM pin (P32) to V_H and activating CE and OE. PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle.

Timing for the EPROM read cycle is shown in Figure 20.

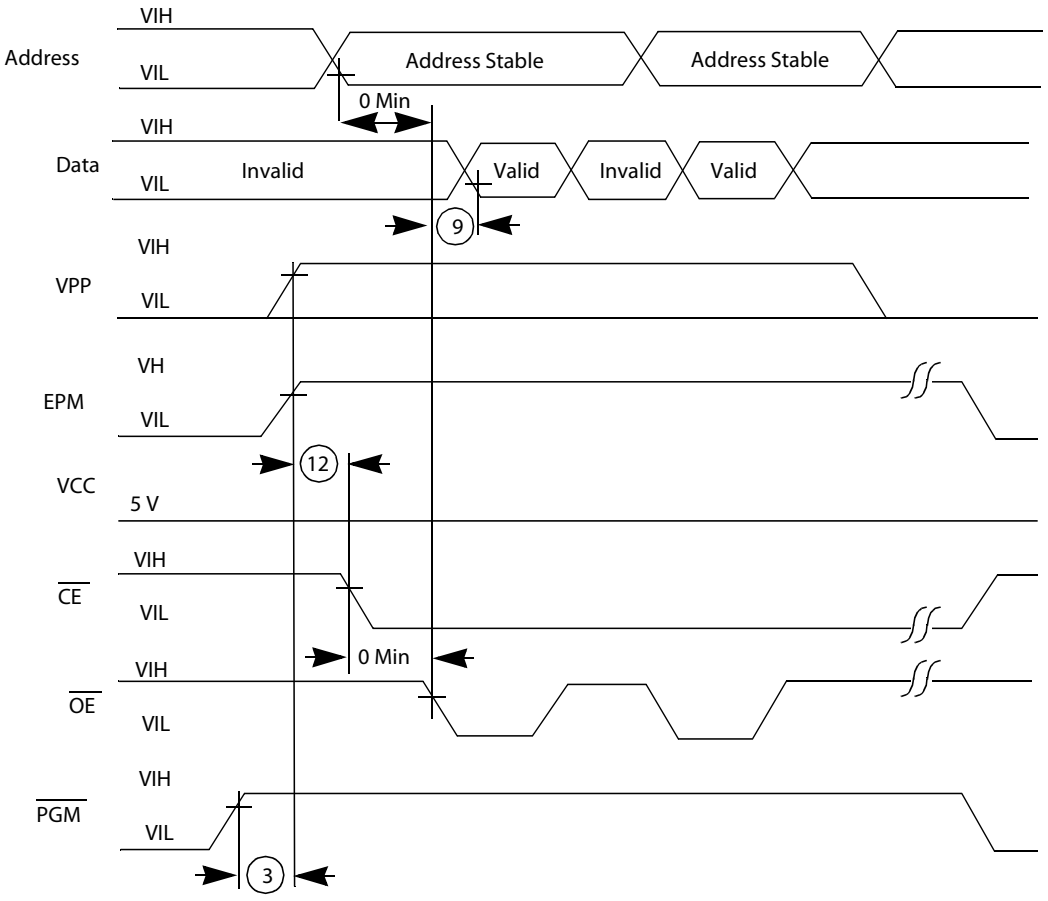


Figure 20. EPROM Read Timing

User MODE 2: EPROM Program

The Z86E61/Z86E63 MCU's Program function conforms to the Intelligent programming algorithm. The device is programmed with V_{CC}, at 6.0V and V_{PP} = 12.5V. Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E61/Z86E63 MCU programming cycle is shown in Figure 21.

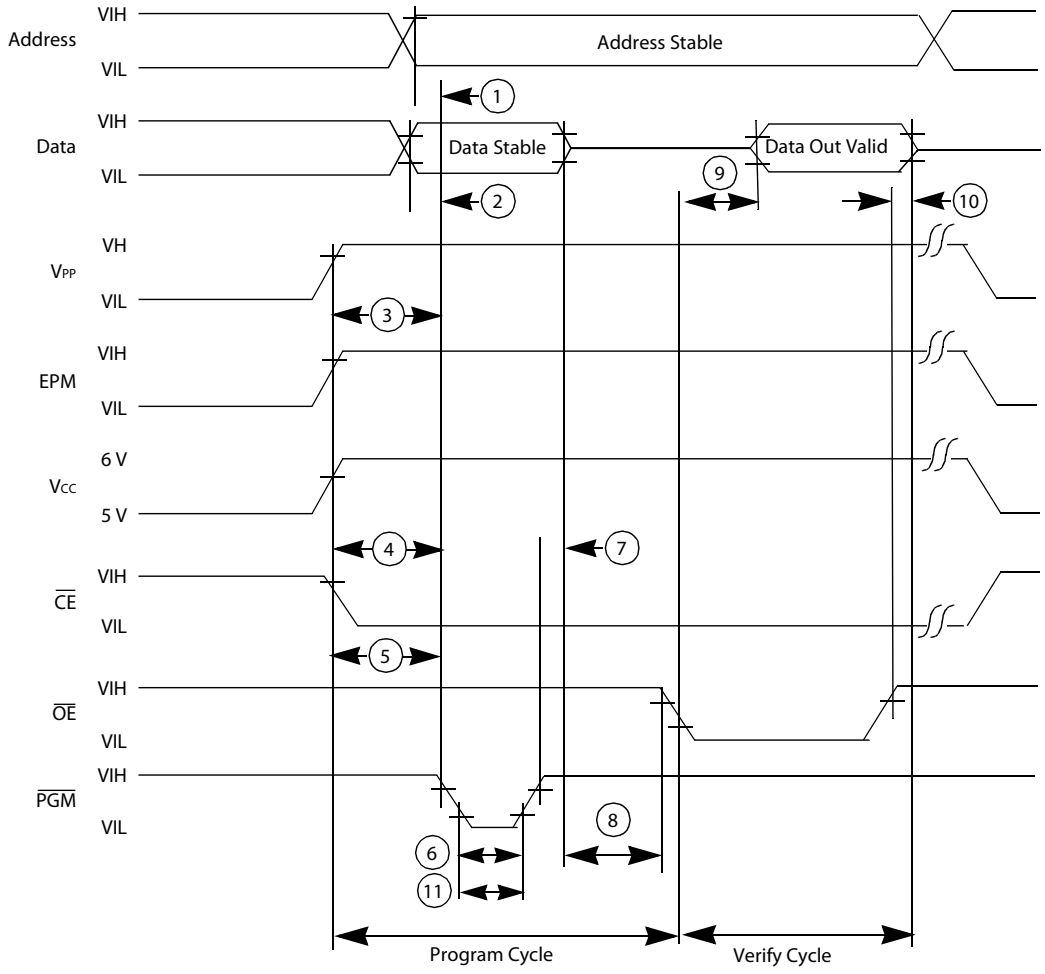


Figure 21. EPROM Program and Verify Timing

User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that V_{PP} is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 21.

User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E61/Z86E63 MCU. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding

mode and configuration registers), but first the user's program must set bit 6 of the IMR (R251). Timing is shown in Figure 22.

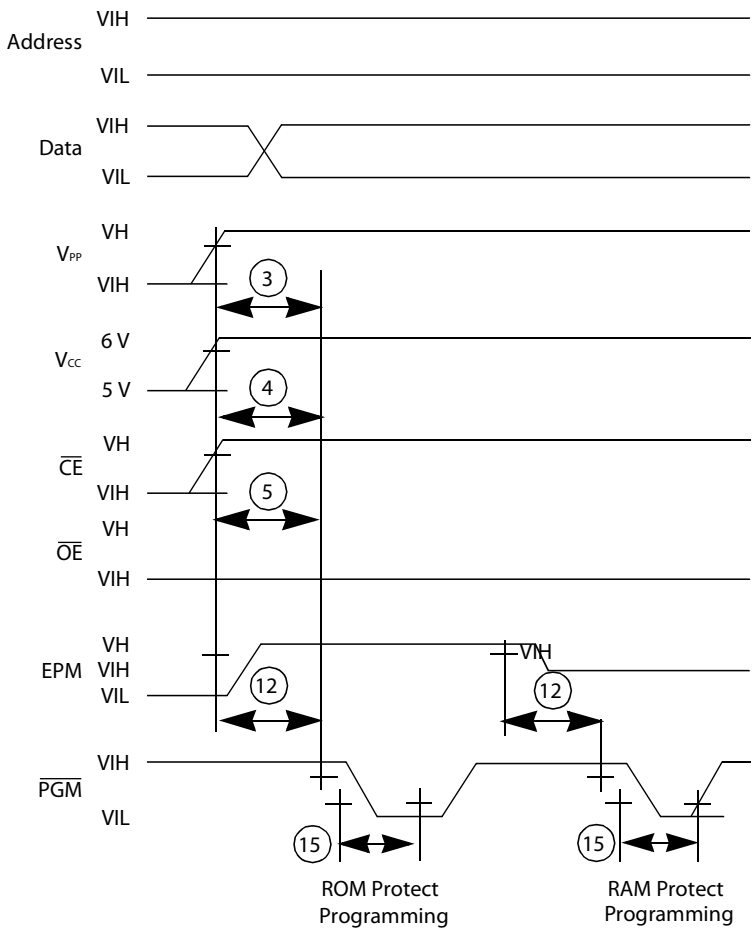


Figure 22. Programming EPROM and RAM Protect

Z86E63 Signal Description for EPROM Program/Read

The following signals are required to correctly program or read the Z86E63 device.

ADDR

The address must remain stable throughout the program read cycle. On both the Z86E61 and Z86E63 MCUs, all A0–A14 address lines must be driven at all times.

DATA

The I/O data bus must be stable during programming (OE High, PGM Low, V_{PP} High). During read the data bus outputs data.

XCLK

A clock is required to clock the RESET signal into the registers before programming. A constant clock can be applied, or the XCLK input can be toggled a minimum of 12 cycles before any programming or verify function begins. The maximum clock frequency to be applied when in the EPROM Mode is 12 MHz.

RESET. The reset input can be held to a constant Low or High value throughout normal programming. It must be held High to program the EPROM protect option bit. Also, any time the RESET input changes state the XCLK must be clocked a minimum of 12 times to clock the RESET through the reset filter.

OE. When the device is placed in EPROM Mode, the OE input also serves as the precharge for the sense amp. The precharge signal should be Low for the first half of the stable address and High for the second half. The PRECHG signal is inverted from the OE signal so the OE should be High on the first half and Low on the second half, or stable address. The EPROM output data should be sampled during the second half of stable address.

The access time of the EPROM is defined in later sections. This two part calculation of access time is required because this is a precharged sense amp with a precharge clock.

Programming Flow

Figure 23 shows the steps for programming the Z86E61/Z86E63 MCU.

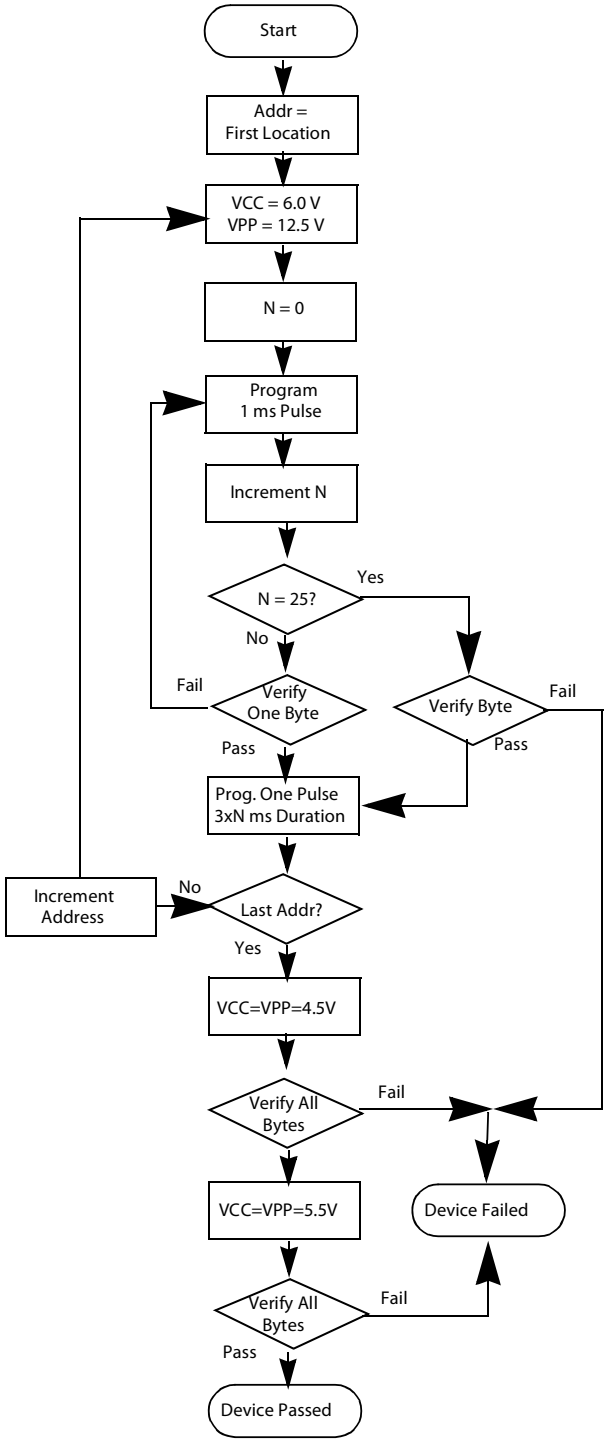


Figure 23. Intelligent Programming Flowchart

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 34 lists the absolute maximum ratings of the Z86E61/Z86E63 MCU.

Table 34. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65	+150	°C
T_A	Operating Ambient Temperature		See Note 2	°C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information on page 60.

Standard Test Conditions

The characteristics described in this document apply to standard test conditions, as noted. All voltages are referenced to GND, and positive current flows into the referenced pin; see Figure 24.

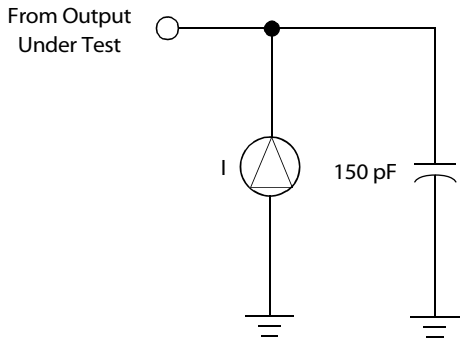


Figure 24. Test Load Diagram

DC Characteristics

Table 35 lists voltage and direct current characteristics for the Z86E61/Z86E63 MCU under differing conditions. Be advised that I_{CC2} requires loading TMR (F1Hh) with any value prior to STOP execution. Use the following sequence:

```
LD TMR,#00
NOP
STOP
```

Table 35. Direct Current Characteristics

Symbol	Parameter	Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} < 250µA.
	Max Input Voltage	13			V	P33–P30 Only.
V_{CH}	Clock Input High Voltage	3.8	V_{CC}+0.3		V	Driven by External Clock Generator.
V_{CL}	Clock Input Low Voltage	–0.3	0.8		V	Driven by External Clock Generator.
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3		V	
V_{IL}	Input Low Voltage	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –2.0mA.
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +2.0mA.
V_{RH}	Reset Input High Voltage	3.8	V_{CC}+0.3		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8		V	
I_{IL}	Input Leakage	–10	10		µA	V_{IN} = 0V, 5.25V.
I_{OL}	Output Leakage	–10	10		µA	V_{IN} = 0V, 5.25V.
I_{IR}	Reset Input Current		–50		µA	V_{CC}=+5.25V; V_{RL}=0V.
I_{CC}	Supply Current		50	25	mA	@ 16MHz.
			60	35	mA	@ 20MHz.
I_{CC1}	Standby Current		15	5	mA	HALT Mode @ 16MHz; V_{IN}=0V, V_{CC}
			20	10	mA	HALT Mode @ 20MHz; V_{IN}=0V, V_{CC}
I_{CC2}	Standby Current		20	5	µA	STOP Mode V_{IN}=0V, V_{CC}

Supply Current

Figure 25 shows the typical supply current values (in milliamps), for the Z86E61/Z86E63 MCU as a function of frequency (in megahertz).

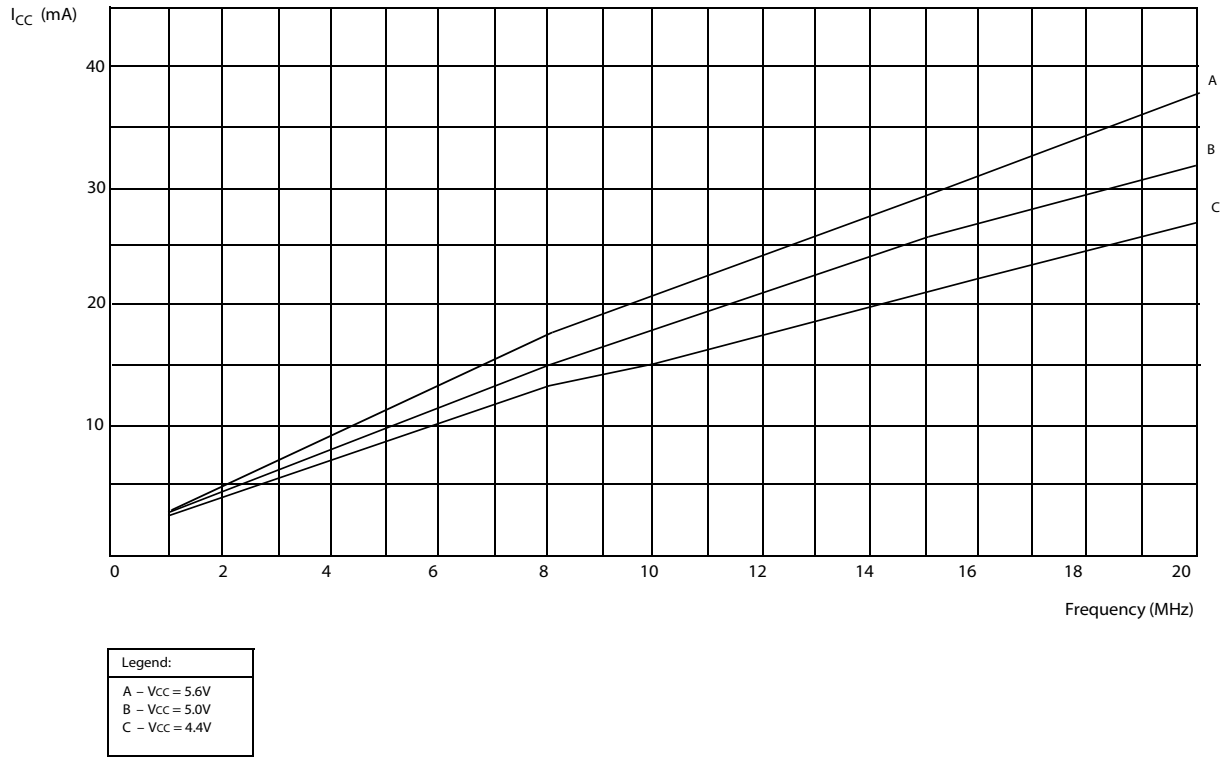


Figure 25. Typical I_{CC} vs. Frequency

Standby Current

Figure 26 shows the typical standby current values (in milliamps), for the Z86E61/ Z86E63 MCU as a function of frequency (in megahertz).

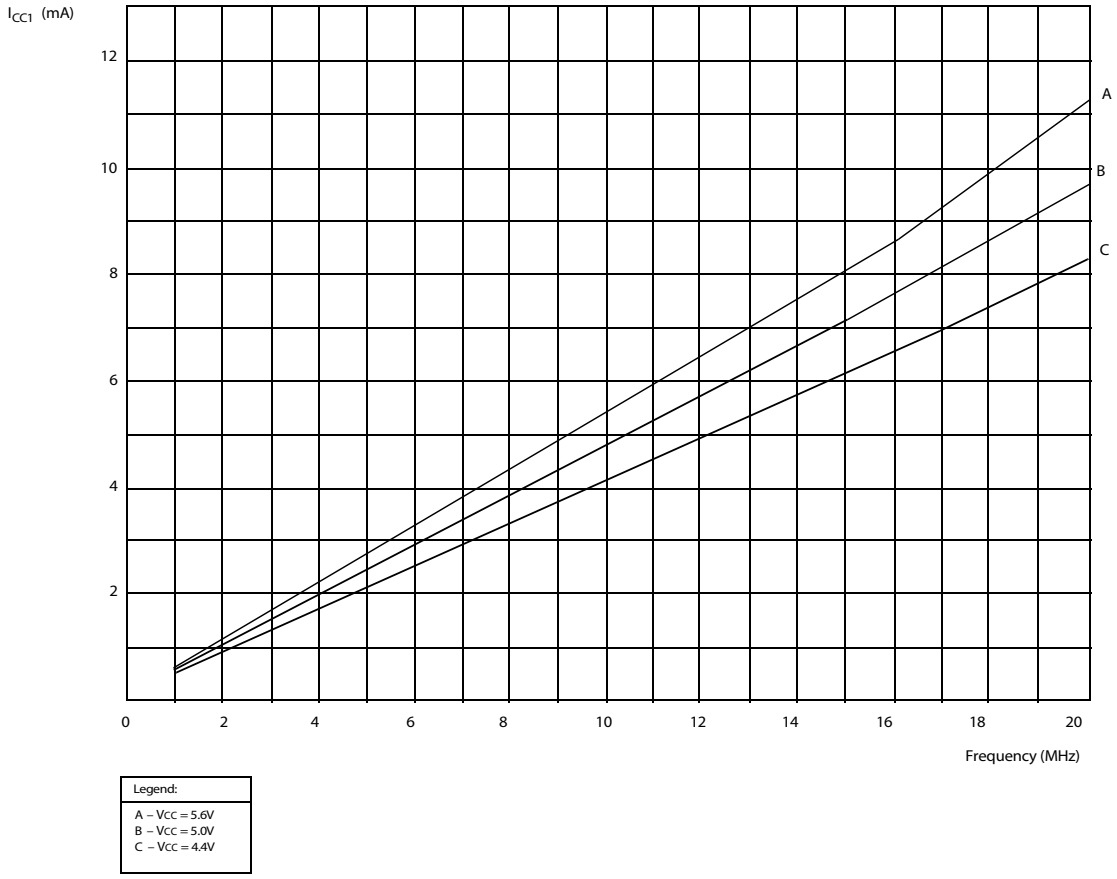


Figure 26. Typical I_{CC1} vs. Frequency

AC Characteristics

Figure 27 displays the timing characteristics for the Z86E61/Z86E63 MCU. The circled numbers in this figure reference a description in Table 36 of each symbol, its parameter and its frequency range for these 16MHz and 20MHz parts.

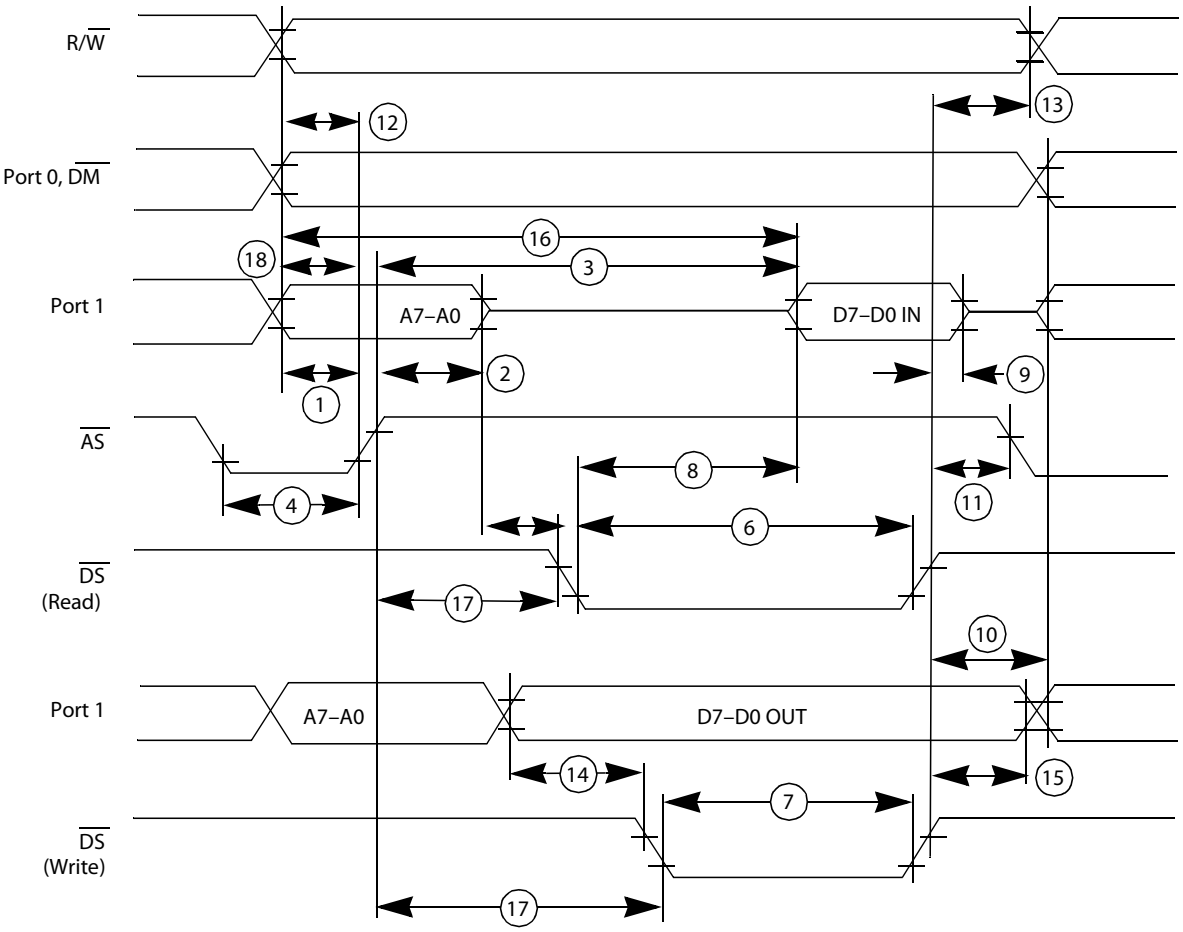


Figure 27. External I/O or Memory Read/Write Timing

Table 36 lists the alternating current characteristics for the Z86E61/Z86E63 MCU as they relate to Figure 27. Formulas for each parameter are listed in Table 37.

Table 36. External I/O or Memory Read and Write Timing

			T_A = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	Symbol	Parameter	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	20		26		ns	2,3
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	30		28		ns	2,3
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid		180		160	ns	2,3,4
4	TwAS	$\overline{AS}$ Low Width	35		36		ns	2,3
5	TdAZ(DS)	Address Float to DS Fall	0		0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	135		130		ns	2,3,4
7	TwDSW	$\overline{DS}$ (Write) Low Width	80		75		ns	2,3,4
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid		75		100	ns	2,3,4
9	ThDR(DS)	Read Data to DS Rise Hold Time	0		0		ns	2,3
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	35		48		ns	2,3
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	30		36		ns	2,3
12	TdR/W(AS)	R/W Valid to $\overline{AS}$ Rise Delay	20		32		ns	2,3
13	TdDS(R/W)	$\overline{DS}$ Rise to R//W Not Valid	30		36		ns	2,3
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	25		40		ns	2,3
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	30		40		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid		200		200	ns	2,3,4
17	TdAS(DS)	AS Rise to $\overline{DS}$ Fall Delay	40		48		ns	2,3
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	30		36		ns	2,3

Notes:
1. All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
2. Timing numbers given are for minimum TpC.
3. See Table 37.
4. When using extended memory timing, add 2 TpC.

Table 37. Clock-Dependent Formulas

Number	Symbol	Formula
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/$\overline{W}$)	0.8 TpC – 15
14	TdDW(DSW)	0.4 sTpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

Input and output handshake timing characteristics are shown in Figures 28 and 29 and described in Table 38.

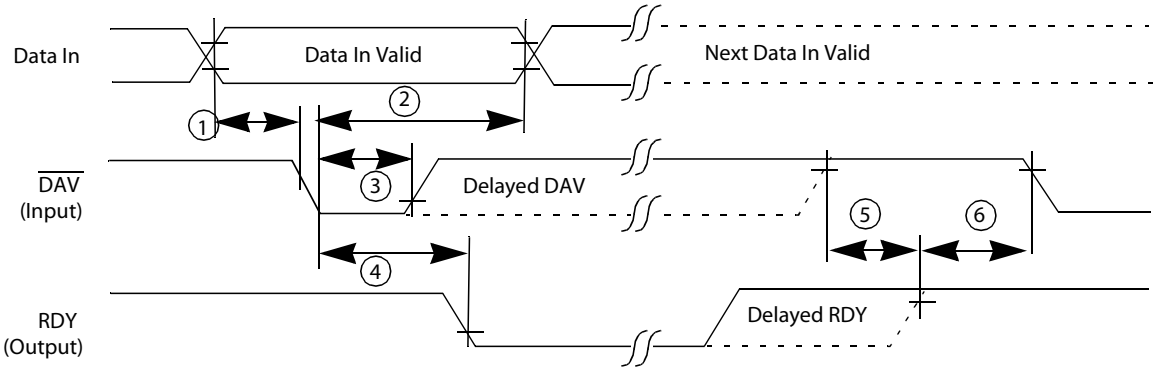


Figure 28. Input Handshake Timing

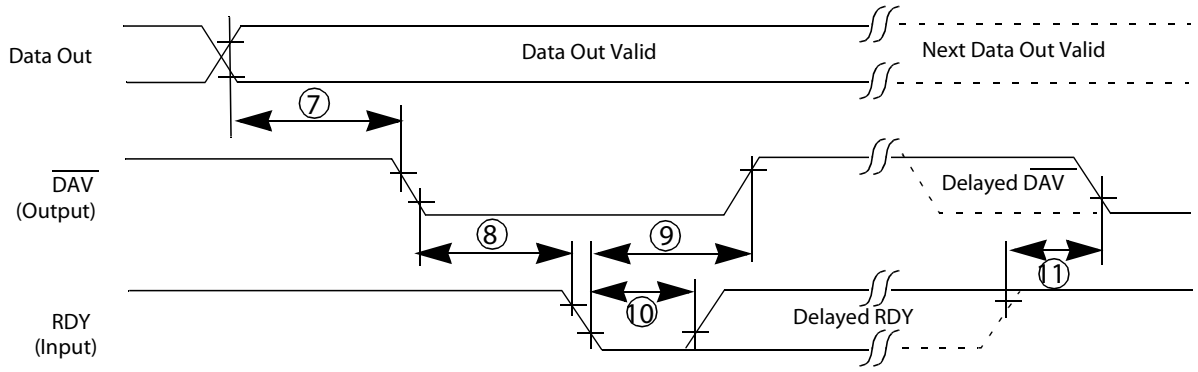


Figure 29. Output Handshake Timing

Table 38. Handshake Timing

			TA = 0°C to +70°				
			16 MHz		20 MHz		Data
No.	Symbol	Parameter	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115	OUT

Additional timing characteristics are shown in Figure 30 and described in Table 39.

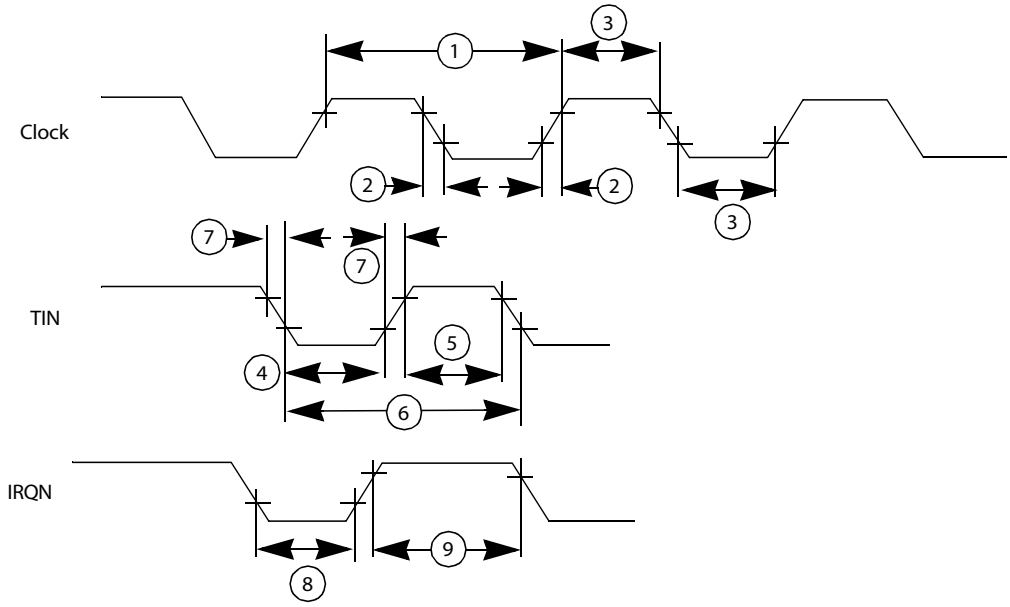


Figure 30. Additional Timing

Table 39. Additional Timing

			TA = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	62.5	1000	50	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		10		15	ns	1
3	TwC	Input Clock Width	21		37		ns	1
4	$TwT_{IN}L$	Timer Input Low Width	50		75		ns	2
5	$TwT_{IN}H$	Timer Input High Width	5TpC		5TpC			2
6	TpT_{IN}	Timer Input Period	8TpC		8TpC			2
7	TrT_{IN},TfT_{IN}	Timer Input Rise & Fall times	100		100		ns	2

Notes:
1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt request through Port 3 (P33–P31).
4. Interrupt request through Port 30.
5. Interrupt references request through Port 3.

Table 39. Additional Timing (Continued)

			TA = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	Symbol	Parameter	Min	Max	Min	Max	Units	Notes
8A	TwIL	Interrupt Request Input Low Times	70		50		ns	2,3
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC			2,4
9	TwIH	Interrupt Request Input High Times	5TpC		5TpC			2,5

Notes:
1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt request through Port 3 (P33–P31).
4. Interrupt request through Port 30.
5. Interrupt references request through Port 3.

Control Registers

Figures 31 through 46 provide brief bit descriptions of each of the Z86E61/Z86E63 MCU's control registers.

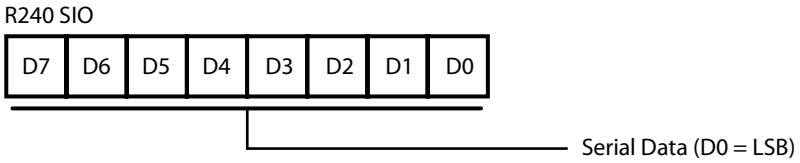


Figure 31. Serial I/O Register (F0H: Read/Write)

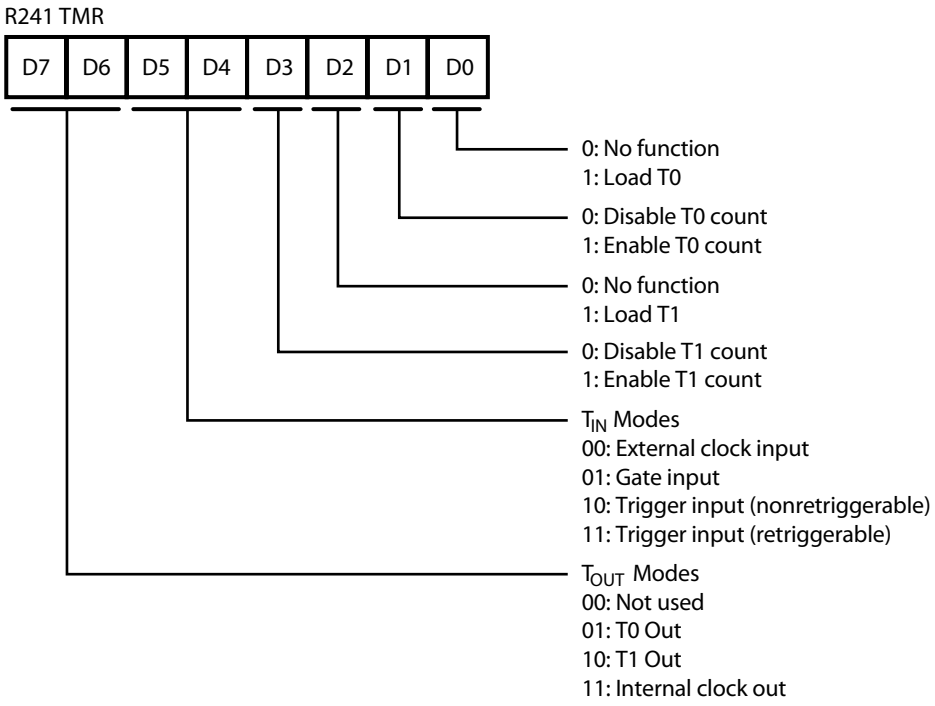


Figure 32. Timer Mode Register (F1H: Read/Write)

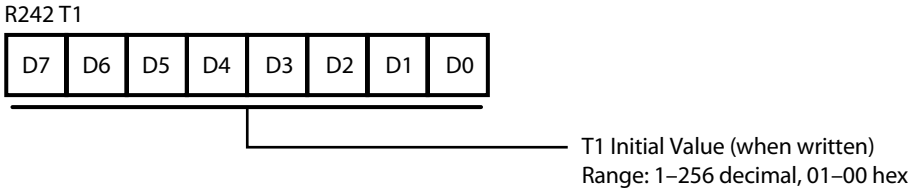


Figure 33. Counter/Timer 1 Register (F2H: Read/Write)

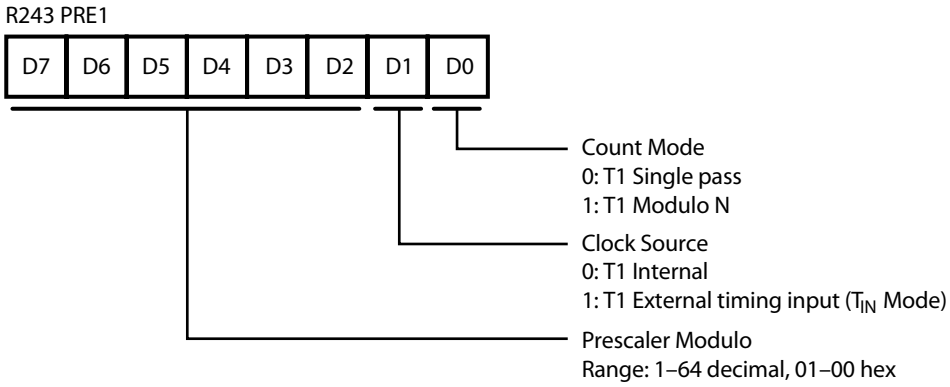


Figure 34. Prescaler 1 Register (F3H: Write Only)

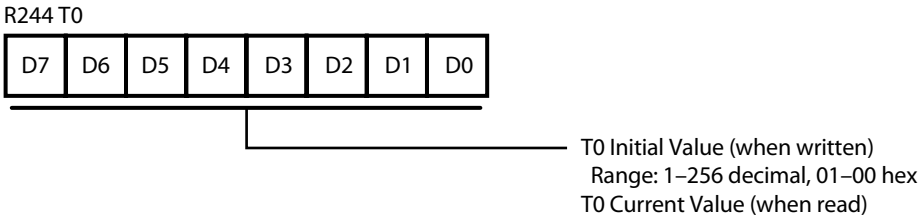


Figure 35. Counter/Timer 0 Register (F4H: Read/Write)

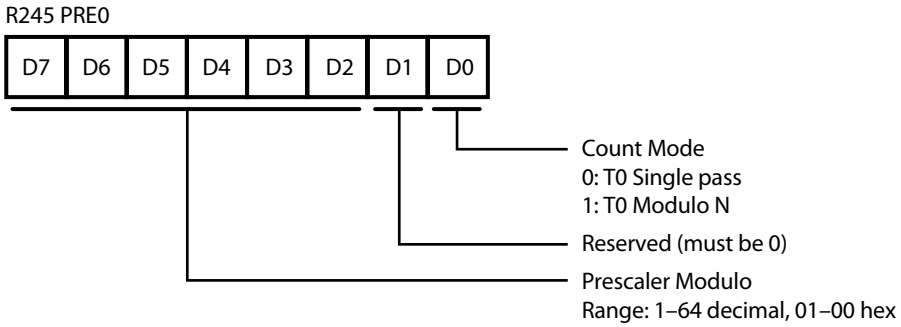


Figure 36. Prescaler 0 Register (F5H: Write Only)

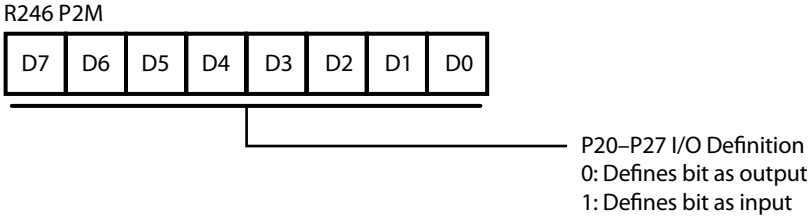


Figure 37. Port 2 Mode Register (F6H: Write Only)

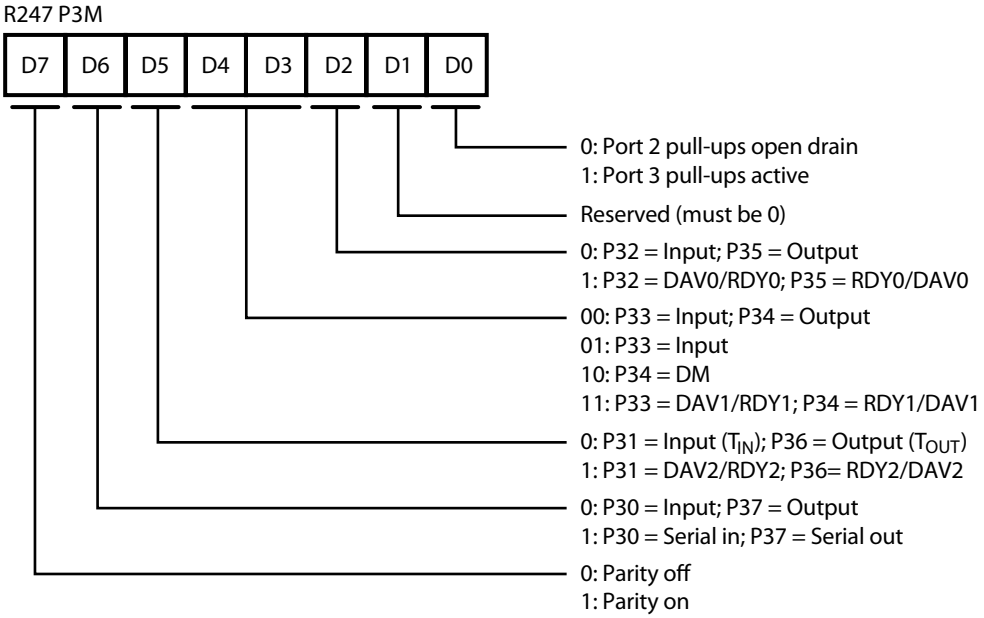


Figure 38. Port 3 Mode Register (F7H: Write Only)

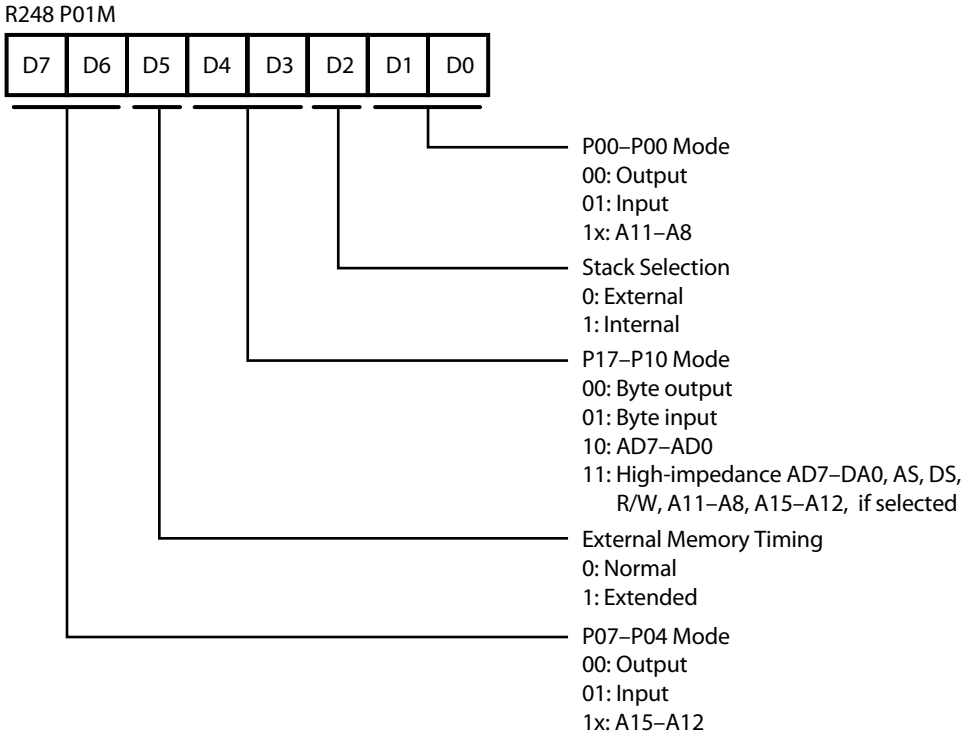


Figure 39. Port 0 and 1 Mode Register (F8H: Write Only)

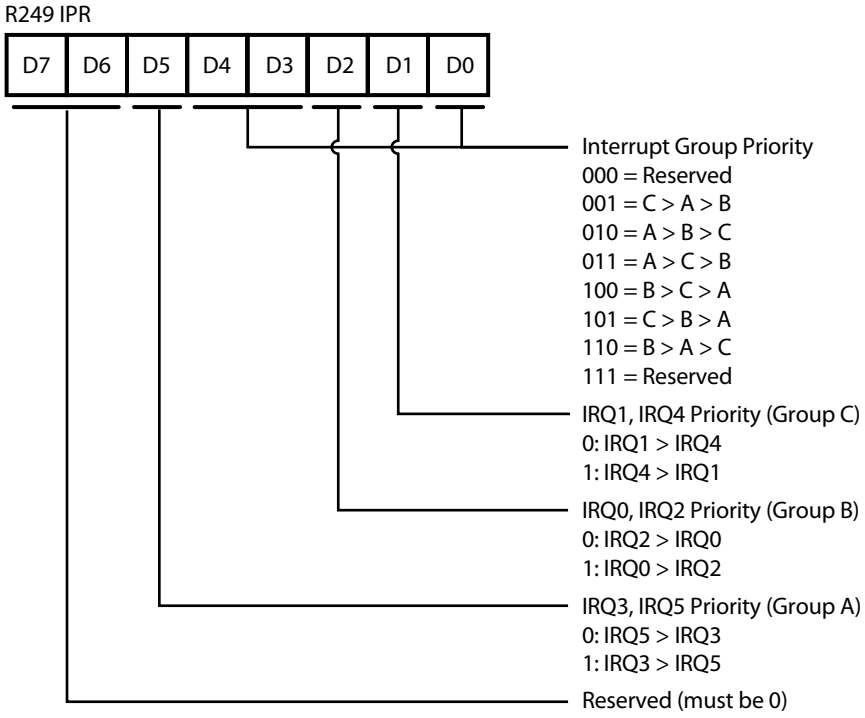


Figure 40. Interrupt Priority Register (F9H: Write Only)

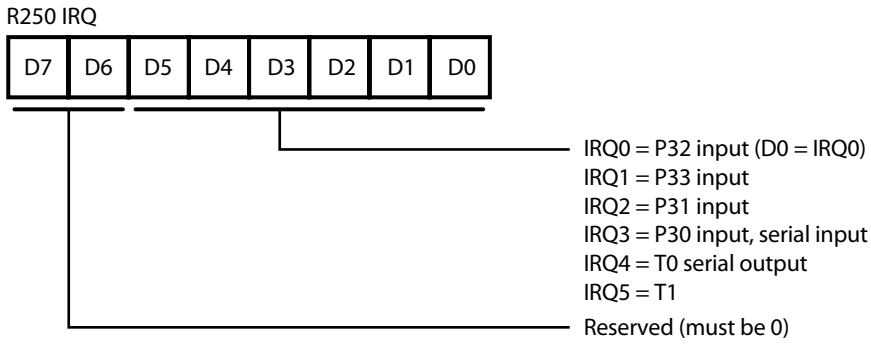


Figure 41. Interrupt Request Register (FAH: Read/Write)

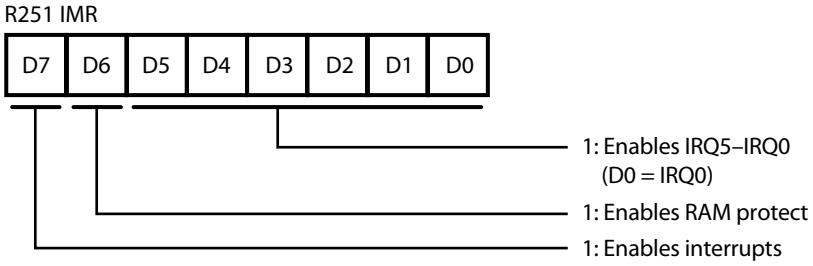


Figure 42. Interrupt Mask Register (FBH: Read/Write)

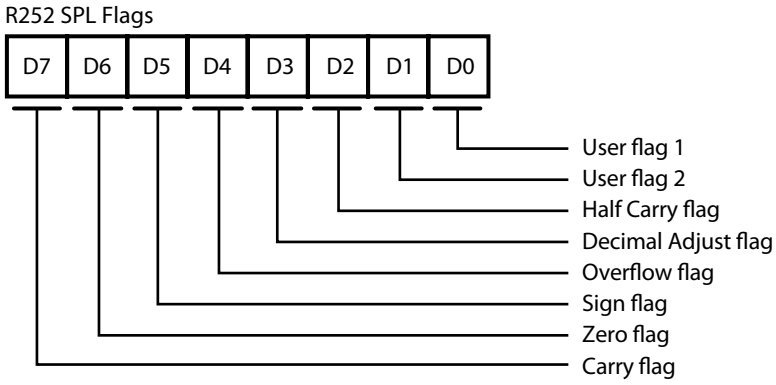


Figure 43. Flag Register (FCH: Read/Write)

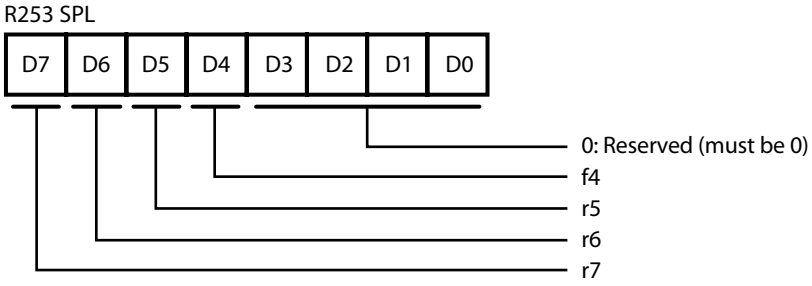


Figure 44. Register Pointer Register (FDH: Read/Write)

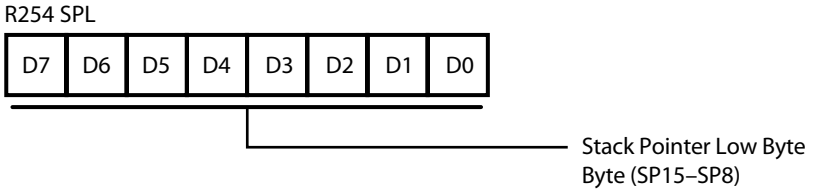


Figure 45. Stack Pointer Register (FEH: Read/Write)

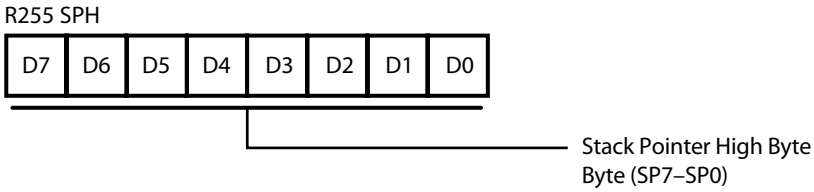


Figure 46. Stack Pointer Register (FFH: Read/Write)

Z8 Instruction Set

This section discusses the addressing modes, symbols, flags, condition codes and instruction formats that apply to the Z8 instruction set. A summary of the Z8 instruction set follows on page 55.

The notations listed in Table 40 are used to describe addressing modes and instruction operations.

Table 40. Instruction Set Notation

Notation	Definition
IRR	Indirect register pair or indirect working register pair address.
Irr	Indirect working register pair only.
X	Indexed address.
DA	Direct address.
RA	Relative address.
IM	Immediate.
R	Register or working register address.
r	Working register address only.
IR	Indirect register or indirect working register address.
Ir	Indirect working register address only.
RR	Register pair or working register pair address.

The symbols listed in Table 41are used to describe the Z8 instruction set.

Table 41. Instruction Set Symbols

Symbol	Definition
dst	Destination location or contents.
src	Source location or contents.
cc	Condition code.
@	Indirect address prefix.
SP	Stack Pointer.
PC	Program Counter.
FLAGS	Flag Register (Control Register 252).
RP	Register Pointer (R253).
IMR	Interrupt Mask Register (R251).

Control Register R252 contains the six flags shown in Table 42.

Table 42. R252 Flags

Symbol	Definition
C	Carry flag.
Z	Zero flag.
S	Sign flag.
V	Overflow flag.
D	Decimal Adjust flag.
H	Half Carry flag.

The flags in Table 42 can be affected by the symbols defined in Table 43.

Table 43. R252 Flags

Symbol	Definition
0	Clear to zero.
1	Set to one.
*	Set to clear according to operation.
–	Unaffected.
x	Undefined.

Table 44 defines the flags that are set for each condition code value.

Table 44. Condition Codes

Value	Mnemonic	Definition	Flags Set
0000	F	Never True (Always False)	
0001	LT	Less Than	(S XOR V) = 1
0010	LE	Less Than Or Equal To	[Z OR (S XOR V)] = 1
0011	ULE	Unsigned Less Than Or Equal	(C OR Z) = 1
0100	OV	Overflow	V = 0
0101	MI	Minus	S = 1
0110	EQ	Equal	Z = 1
0110	Z	Zero	Z = 1
0111	C	Carry	C = 1

Table 44. Condition Codes (Continued)

Value	Mnemonic	Definition	Flags Set
0111	ULT	Unsigned Less Than	C = 1
1000		Always True	
1001	GE	Greater Than Or Equal To	(S XOR V) = 0
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
1100	NOV	No Overflow	V = 0
1101	PL	Plus	S = 0
1110	NE	Not Equal	Z = 0
1110	NZ	Not Zero	Z = 0
1111	NC	No Carry	C = 0
1111	UGE	Unsigned Greater Than Or Equal To	C = 0

Instruction Formats

Figure 47 shows the one-, two- and three-byte formats used in the Z8 instruction set.

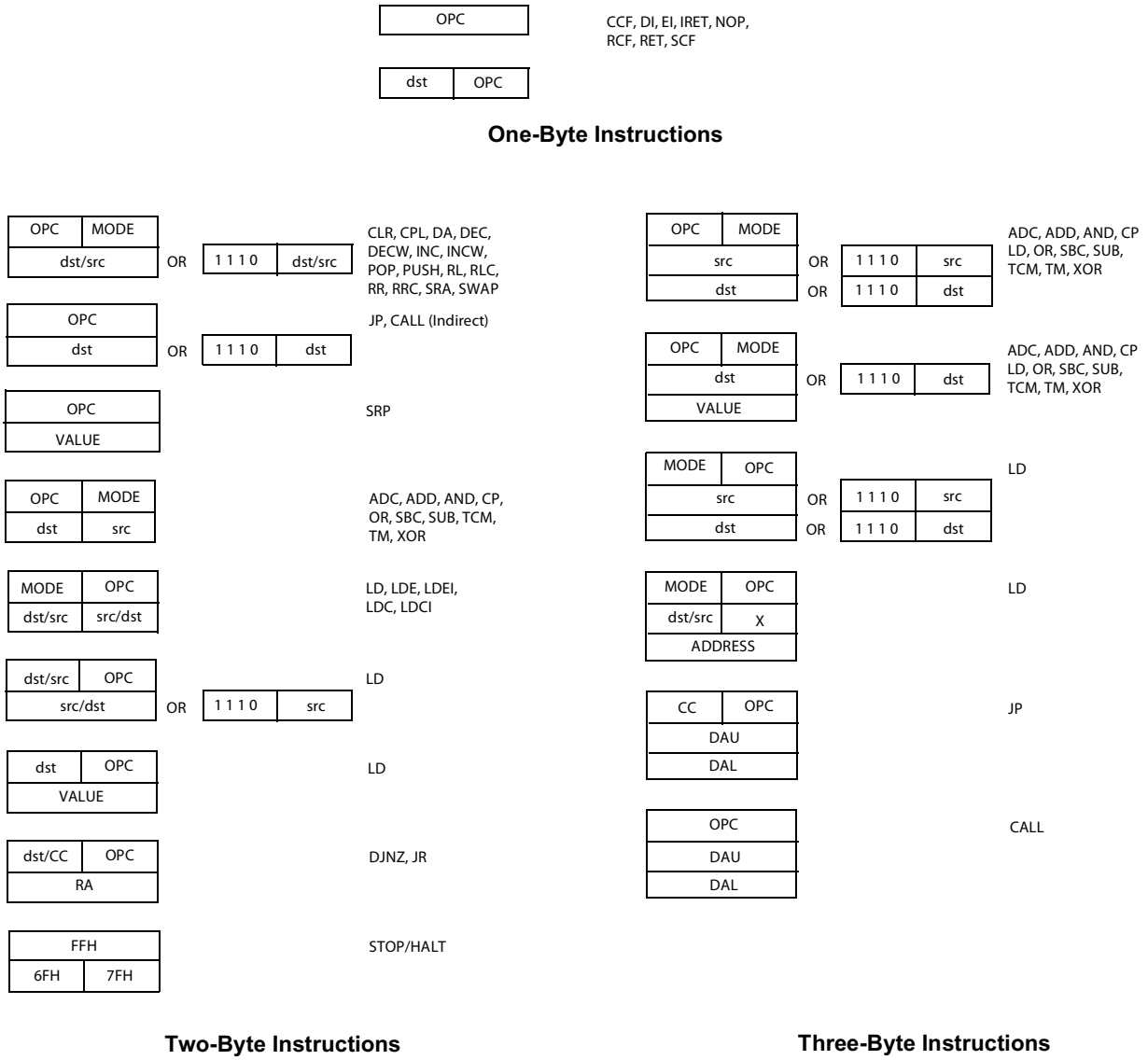


Figure 47. Instruction Formats

Instruction Summary

Table 45 summarizes each Z8 instruction by its operation, addressing mode, operation code, and the flag(s) each instruction affects.

Table 45. Instruction Summary

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst ← dst + src + C	See Note 1		1[]	*	*	*	*	0	*
ADD dst, src dst ← dst + src	See Note 1		0[]	*	*	*	*	0	*
AND dst, src dst ← dst AND src	See Note 1		5[]	–	*	*	0	–	–
CALL dst SP ← SP – 2 @ SP ← PC, PC ← dst	DA IRR		06 D4	–	–	–	–	–	–
CCF C ← NOT C			EF	*	–	–	–	–	–
CLR dst dst ← 0	R IR		B0 B11	–	–	–	–	–	–
COM dst dst ← NOT dst	R IR		60 61	–	*	*	0	–	–
CP dst, src dst – src	See Note 1		A[]	*	*	*	*	–	–
DA dst dst ← DA dst	R IR		40 41	*	*	*	X	–	–
DEC dst dst ← dst – 1	R IR		00 01	–	*	*	*	–	–
DECW dst dst ← dst – 1	R IR		80 81	–	*	*	*	–	–
DI IMR(7) ← 0			8F	–	–	–	–	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
DJNZ r, dst r ← r – 1 if r ≠ 0 PC ← PC + dst Range: +127, –128	RA		rA r = 0 – F	–	–	–	–	–	–
EI IRM(7) ← 1			BF	*	*	*	*	*	*
HALT			7F	–	–	–	–	–	–
INC dst dst ← dst + 1	r R IR		rE r = 0 – F 20 21	–	*	*	*	–	–
INCW dst dst ← dst + 1	RR IR		A0 A1	–	*	*	*	–	–
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR		cD c = 0 – F 30	–	–	–	–	–	–
JR cc, dst if cc is true, PC ← PC + dst Range: +127, –128	RA		cB c = 0 – F	–	–	–	–	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
LD dst, src dst ← src	r	Im	rC	–	–	–	–	–	–
	r	R	r8						
	R	r	r9						
			r = 0 – F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src dst ← src	r	Irr	C2	–	–	–	–	–	–
LDCI dst, src dst ← src r ← r + 1; rr ← rr + 1	Ir	Irr	C3	–	–	–	–	–	–
NOP			FF	–	–	–	–	–	–
OR dst, src dst ← dst OR src	See Note 1		4[1	–	*	*	0	–	–
POP dst ← @SP; SP ← SP + 1	R IR		50 51	–	–	–	–	–	–
PUSH src SP ← SP – 1; @SP ← src	R IR		70 71	–	–	–	–	–	–
RCF C ← 0			CF	0	–	–	–	–	–
RET PC ← @SP; SP ← SP + 2			AF	–	–	–	–	–	–
RL dst	R IR		90 91	*	*	*	*	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
RLC dst	R IR		10 11	*	*	*	*	–	–
RR dst	R IR		E0 E1	*	*	*	*	–	–
RRC dst	R IR		C0 C1	*	*	*	*	–	–
SBC dst, src dst ← dst ← src ← C	See Note 1		3[]	*	*	*	*	1	*
SCF C ← 1			DF	1	–	–	–	–	–
SRA dst	R IR		D0 D1	*	*	*	0	–	–
SRP dst RP ← src	Im		31	–	–	–	–	–	–
STOP			6F	1	–	–	–	–	–
SUB dst, src dst ← dst ← src	See Note 1		2[ ]	[	[	[	[	1	[
SWAP dst	R IR		F0 F1	X	*	*	X	–	–
TCM dst, src (NOT dst) AND src	See Note 1		6[ ]	–	*	*	0	–	–
TM dst, src dst AND src	See Note 1		7[ ]	–	*	*	0	–	–
XOR dst, src dst ← dst XOR src	See Note 1		B[ ]	–	*	*	0	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

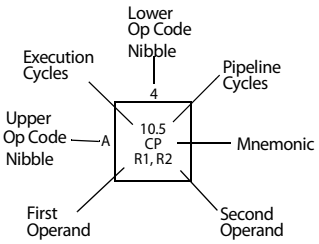
For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Op Code Map

Figure 48 shows a map of the Z86E61/Z86E63 MCU's operational codes.

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.6 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	8.5 ADD r1, Ir2	10.5 ADD R2,R1	10.5 ADD IR2, R1	10.5 ADD R1, 1M	10.5 ADD R1, 1M	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/0.0 JA cc, RA	6.5 LD r1, 1M	12/10.0 JP cc, DA	6.5 INC r1	
1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, 1M	10.5 ADC R1, 1M								
2	6.5 INC R1	6.6 WC IR1	6.5 SUB r1, r2	0.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R2, 1M	10.5 BUB IR1, 1M								
3	6.5 JP IRR1	6.1 SRP 1M	6.5 SBC r1, r2	6.5 OR r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, 1M	10.5 SBC IR1, 1M								
4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, 1M									
5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, 1M	10.5 TCM IR1, 1M								
6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, 1M	10.5 TCM IR1, 1M								6.0 STOP
7	10/12.1 PUSH R2	10/12.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, 1M	10.5 TM IR1, 1M								7.0 HALT
8	10.5 DECW RR1	10.5 DECW IR1	12.0 LDE r1, Irr2	18.0 LDEI r1, Irr2												6.1 DI
9	6.5 RL R1	6.5 RL IR1	12.0 LDE r1, Irr2	18.0 LDEI r1, Irr2												6.1 EI
A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, 1M	10.5 CP IR1, 1M								14.0 RET
B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR R2, R1	10.5 XOR R1, 1M	10.5 XOR IR1, 1M								16.0 IRET
C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Irr2	18.0 LDC Ir1, Irr2				10.5 LD r1, x, R2								6.5 RCF
D	6.5 SRA R1	6.5 SRA IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2	20.0 CALL* IRR1		20.0 CALL DA	10.5 LD 42, x, R1								6.5 SCF
E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, IR2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, 1M	10.5 LD IR1, 1M								6.5 CCF
F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2		10.5 LD R2, IR1										6.0 NOP
Bytes per instruction	2				3				2					3	1	



Legend:
R = 8-bit address
r = 4-bit address
R1 or r1 = dst address
R2 or r2 = src address

Sequence:
Op code, first operand, second operand

Note: *The 2-byte instruction appears as a 3-byte instruction; blank areas are not defined.

Figure 48. Op Code Map

Packaging

Zilog's Z86E61 and Z86E63 MCUs are available in the following packages:

- 40-pin Plastic Dual Inline Package (PDIP)
- 44-pin Low-Profile Quad Flat Package (LQFP)
- 44-pin Plastic Chip Carrier (PLCC)

Current diagrams for each of these packages are published in Zilog's Packaging Product Specification (PS0072), which is available free for download from the Zilog website.

Ordering Information

Order your Z86E61/Z86E63 MCU products from Zilog using the part numbers shown in Table 46. For more information about ordering, please consult your local Zilog sales office. The Sales Location page on the Zilog website lists all regional offices.

Table 46. Z86E61/Z86E63 MCU Ordering Matrix

Part Number	Frequency	Package	Temperature Range
Z86E61 MCU			
Z86E6116PSG	16MHz	40-pin PDIP	0°C to +70°C
Z86E6116VSG	16MHz	44-pin PLCC	0°C to +70°C
Z86E6116ASG	16MHz	44-pin LQFP	0°C to +70°C
Z86E6120PSG	20MHz	40-pin PDIP	0°C to +70°C
Z86E6120VSG	20MHz	44-pin PLCC	0°C to +70°C
Z86E6120ASG	20MHz	44-pin LQFP	0°C to +70°C
Z86E63 MCU			
Z86E6316PSG	16MHz	40-pin PDIP	0°C to +70°C
Z86E6316VSG	16MHz	44-pin PLCC	0°C to +70°C
Z86E6316ASG	16MHz	44-pin LQFP	0°C to +70°C
Z86E6320PSG	20MHz	40-pin PDIP	0°C to +70°C
Z86E6320VSG	20MHz	44-pin PLCC	0°C to +70°C
Z86E6320ASG	20MHz	44-pin LQFP	0°C to +70°C

Part Number Suffix Designations

Zilog part numbers consist of a number of components. For the Z86E61/Z86E63 MCU, these components are:

Environmental Flow
G = Lead-Free Packaging

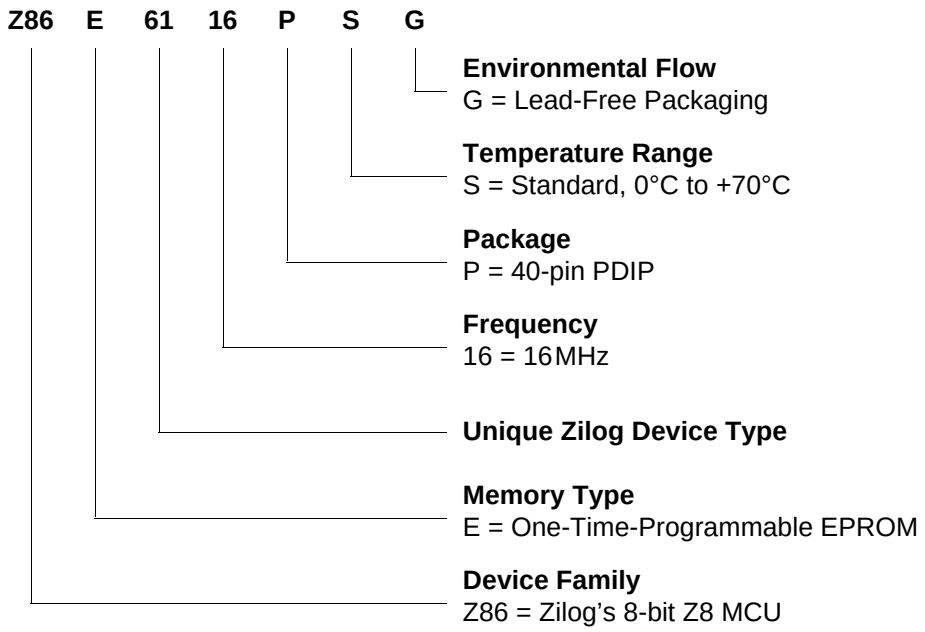
Temperature Range
S = 0ºC to +70ºC

Package
P = 40-pin Plastic DIP (PDIP)
V = 44-pin Plastic Chip Carrier (PLCC)
A = 44-pin Low-Profile Quad Flat Package (LQFP)

Frequency
16 = 16MHz
20 = 20MHz

Memory Type
E = One-Time-Programmable EPROM

Example. Part number Z86E6116PSC is an 8-bit Z8-powered MCU operating at a 16MHz frequency in a 40-pin PDIP package, operating within a 0ºC to +70ºC temperature range and built using lead-free solder.



Customer Support

To share comments, get your technical questions answered, or report issues you may be experiencing with our products, please visit Zilog's Technical Support page at http://support.zilog.com.

To learn more about this product, find additional documentation, or to discover other facets about Zilog product offerings, please visit the Zilog Knowledge Base at http://zilog.com/kb or consider participating in the Zilog Forum at http://zilog.com/forum.

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