CS43L36

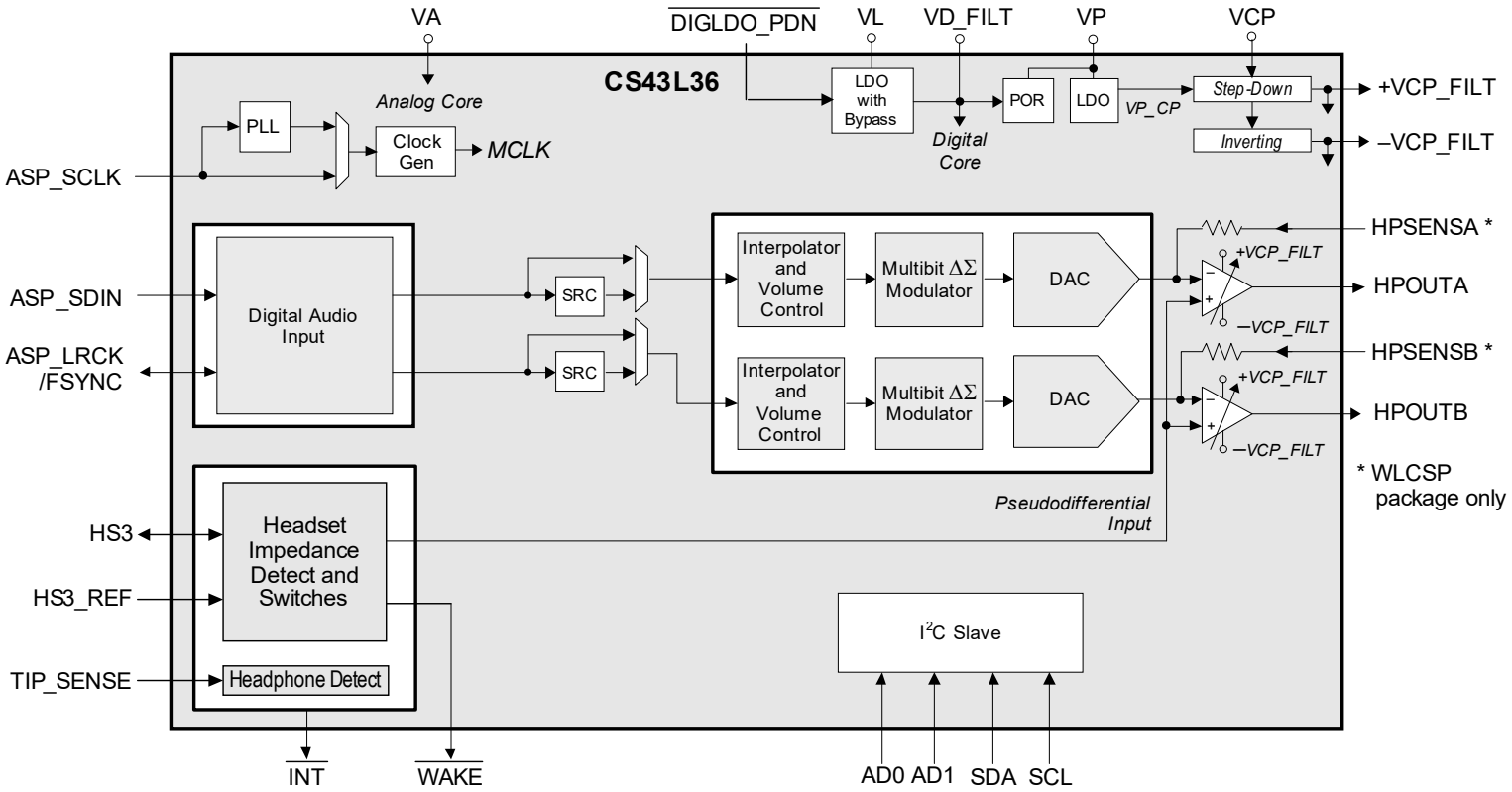
Low-Power, High-Performance Audio DAC with Class H Headphone Drivers

System Features

- Stereo headphone (HP) output with 114-dB dynamic range
  - Class H HP amplifier with four-level automatic or manual supply adjust
  - –98-dB THD+N into 30 Ω with 10-mW output power
  - 2 x 35 mW output power into 30 Ω with 0.018% THD+N
- Load detection
  - Headphone load detection of 15 or 30 Ω
  - Line-level load (3 kΩ) with capacitance detection
- Headphone insertion/removal detection with WAKE
- Audio serial port (ASP)
  - I²S (two channels) or TDM (up to four channels)
  - Slave or Hybrid-Master Mode (bit-clock slave and LRCK/FSYNC derived from bit clock)
  - Supports up to 32-bit audio
  - Sample rate support for 8 to 192 kHz
  - I²C control with interrupt output
- Integrated fractional-N PLL
  - Increases system-clock flexibility for audio processing
  - Reference clock sourced from I²S/TDM bit clock
- Bypassable SRCs for maximum flexibility
- Attenuation, mute, and volume controls for each output
- Integrated power management
  - Digital core operates from either an external 1.2-V supply or LDO from a 1.8-V supply.
  - Step-down charge pump improves HP efficiency
  - Independent peripheral power-down controls
  - Standby operation from VP with all other supplies powered off
  - VP monitor to detect and report brownout conditions
  - Low-impedance switching suppresses ground-noise

Applications

- Ultrabooks, tablets, and smartphones
- Digital headsets



General Description

The CS43L36 is a low-power, high dynamic-range, stereo audio DAC with integrated I²S/I²C/TDM interfaces designed for portable applications. The CS43L36 features support for up to 32-bit audio inputs and includes bypassable SRCs.

The bypassable fractional-N PLL sourced from the ASP SCLK allows for maximum flexibility in any system.

There is independent attenuation on each input along with volume adjustment and mute control.

The CS43L36 is available in 49-ball WLCSP package and a 40-pin QFN package, both supporting an extended commercial operational temperature range of –40°C to +85°C.

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1 Pin Assignments and Descriptions

This section shows pin assignments and describes pin functions.

1.1 WLCSP Pin Out (Through-Package View)

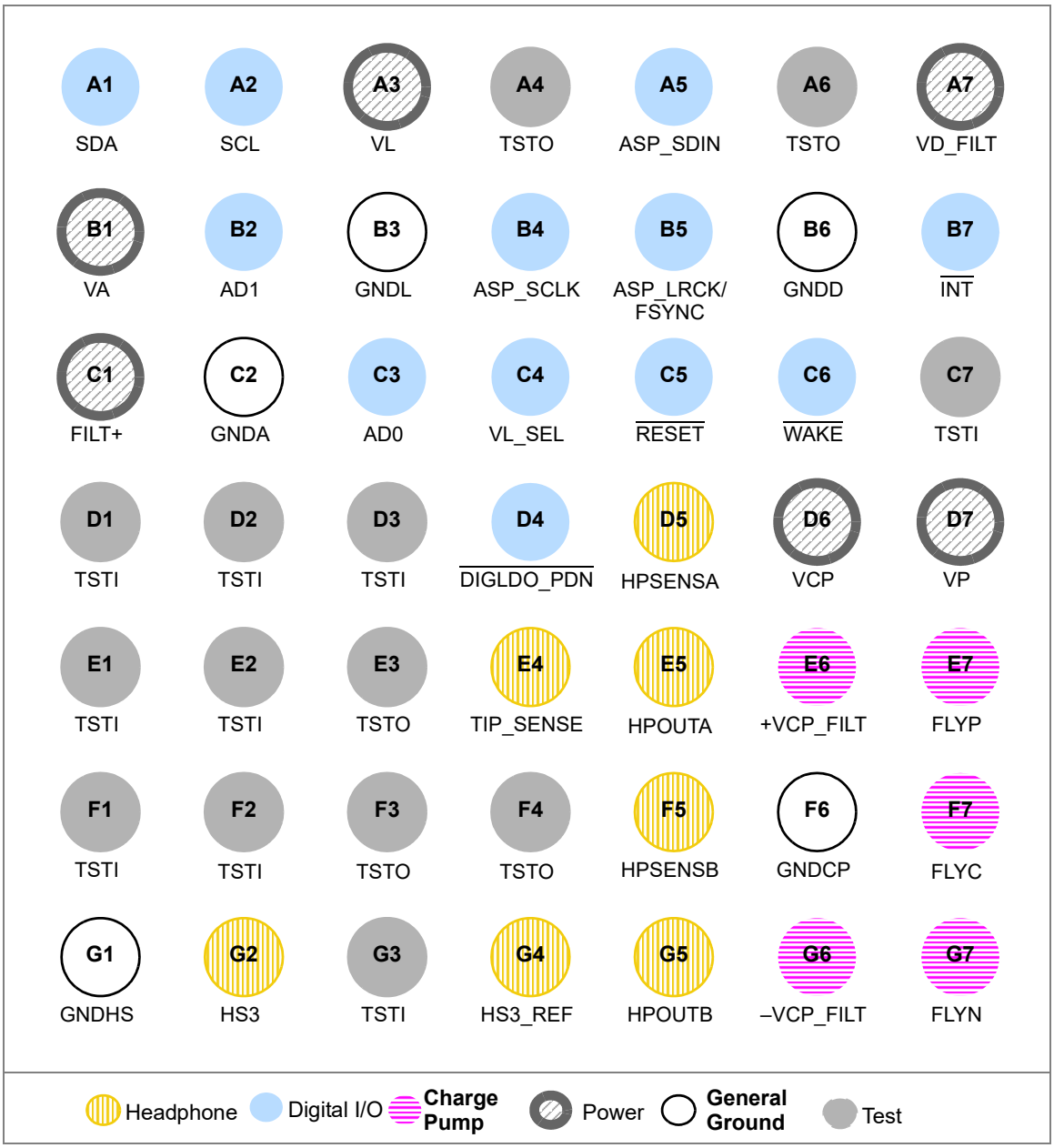


Figure 1-1. WLCSP Pin Diagram (Through-Package View)

1.2 QFN Pin Out (Through-Package View)

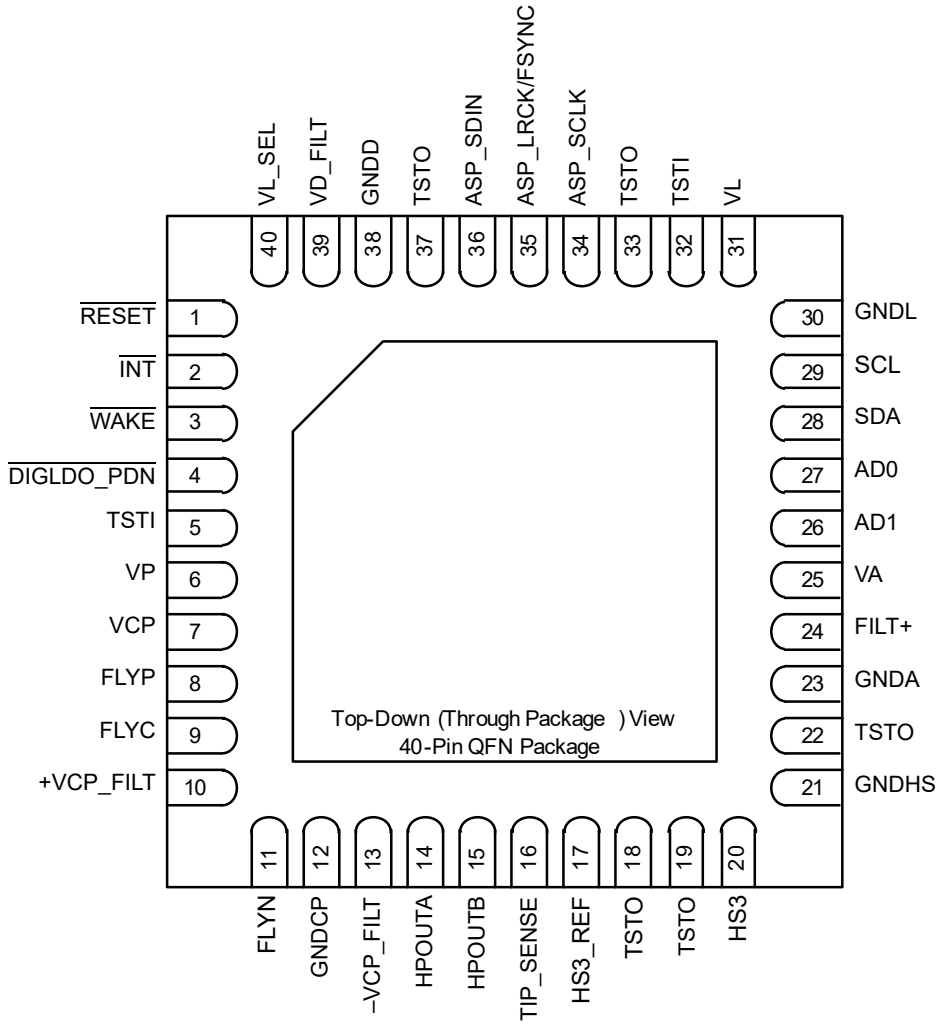


Figure 1-2. QFN Pin Diagram

1.3 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection[1]	Driver	Receiver	State at Reset
					Headphone				
HS3_REF	G4	17	VP	I	**Headset Connection Reference**. Input to pseudodifferential HP output reference	—	—	—	Input
HS3	G2	20	VP	I	**Headset Connections**. Input to headset and mic-button detection functions	—	—	—	Input
HPOUTA HPOUTB	E5 G5	14 15	±VCP_FILT	O	**Headphone Audio Output.** Ground-centered audio output.	—	—	—	—
HPSENSA HPSENSB	D5 F5	— —	±VCP_FILT	I	**Headphone Audio Sense Input.** Audio sense input. WLCSP package only	—	—	—	Input
TIP_SENSE	E4	16	VP	I	**Tip Sense.** Output can be set to wake the system. Independently configurable to be debounced on plug and unplug events.	—	Hi-Z	—	—

Table 1-1. Pin Descriptions *(Cont.)*

Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection[1]	Driver	Receiver	State at Reset
					Digital I/O				
AD0 AD1	C3 B2	27 26	VL	I	**I²C Address Input.** Address pins for I²C Instance ID [1:0] input.	—	—	Hysteresis on CMOS input	Input
ASP_LRCK/ FSYNC	B5	35	VL	I/O	**ASP Left/Right Clock or Frame Sync.** Left or right word select, or frame start sync for the ASP interface.	—	CMOS output	Hysteresis on CMOS input	Input
ASP_SCLK	B4	34	VL	I	**ASP/ Serial Data Clock.** Serial data-shift clock for the ASP interface in I²S/TDM Mode. Source clock used for internal master clock generation.	—	—	Hysteresis on CMOS input	Input
ASP_SDIN	A5	36	VL	I/O	**ASP Serial Data Input.** Serial data input and output in serial data input for the ASP interface in I²S/TDM mode.	—	CMOS output	Hysteresis on CMOS input	Input
$\overline{\text{DIGLDO\_PDN}}$	D4	4	VP	I	**Digital LDO Power Down.** Digital core logic LDO power down.	—	—	Hysteresis on CMOS input	Input
$\overline{\text{INT}}$	B7	2	VP	O	**Interrupt output.** Programmable, open-drain, active-low programmable interrupt output.	—	CMOS open-drain output	—	Output
$\overline{\text{RESET}}$	C5	1	VP	I	**Reset.** Hardware reset.	—	—	Hysteresis on CMOS input	Input
SCL	A2	29	VL	I	**I²C Clock.** Clock input for the I²C interface.	—	—	Hysteresis on CMOS input	Input
SDA	A1	28	VL	I/O	**I²C Input/Output.** I²C input and output.	—	CMOS open-drain output	Hysteresis on CMOS input	Input
VL_SEL	C4	40	VP	I	**VL Supply Voltage Select.** Select for VL power supply voltage level. Connect to VP for 1.8-V VL supply, connect to GNDD for 1.2-V VL supply	—	—	Hysteresis on CMOS input	Input
$\overline{\text{WAKE}}$	C6	3	VP	O	**Wake up.** Programmable, open-drain, active-low output. This outputs the state of the Mic S0 or HP wake detect.	—	Hi-Z, CMOS open-drain output	—	Output
					Charge Pump				
–VCP_FILT	G6	13	VCP/ VP[2]	O	**Inverting Charge Pump Filter Connection.** Power supply for the inverting charge pump that provides the negative rail for the HP amplifier.	—	—	—	—
+VCP_FILT	E6	10	VCP/ VP[2]	O	**Step Down Charge Pump Filter Connection.** Power supply for the step down charge pump that provides the positive rail for the HP amplifier.	—	—	—	—
FLYC	F7	9	VCP/ VP[2]	O	**Charge Pump Cap Common Node.** Common positive node for the HP amplifiers' step-down and inverting charge pumps' flying capacitors.	—	—	—	—
FLYN	G7	11	VCP/ VP[2]	O	**Charge Pump Cap Negative Node.** Negative node for the inverting charge pump's flying capacitor.	—	—	—	—
FLYP	E7	8	VCP/ VP[2]	O	**Charge Pump Cap Positive Node.** Positive node for HP amps' step-down charge pump's flying capacitor.	—	—	—	—
					Power				
FILT+	C1	24	VA	I	**Positive Voltage Reference.** Positive reference voltage for internal sampling circuits.	—	—	—	—
VA	B1	25	N/A	I	**Analog Power Supply.** Power supply for the internal analog section.	—	—	—	—
VCP	D6	7	N/A	I	**Charge Pump Power.** Power supply for the internal HP amplifiers charge pump.	—	—	—	—
VD_FILT	A7	39	N/A	I	**1.2-V Digital Core Power Supply.** Power supply for internal digital logic.	—	—	—	—
VL	A3	31	N/A	I	**I/O Power Supply.** Power supply for external interface and internal digital logic.	—	—	—	—

Table 1-1. Pin Descriptions *(Cont.)*

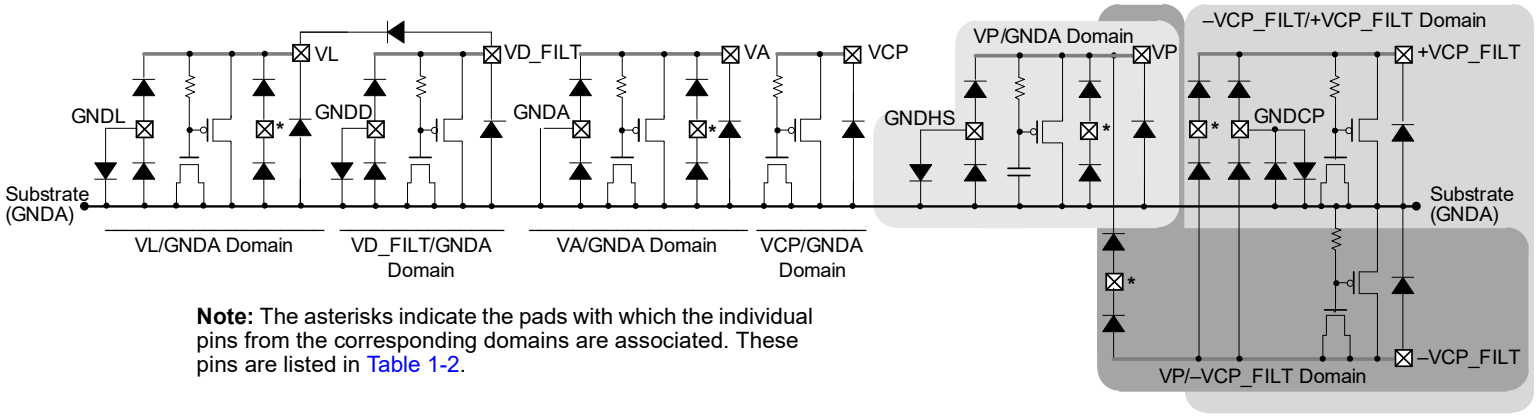
Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection[1]	Driver	Receiver	State at Reset
VP	D7	6	N/A	I	**High Voltage Interface Supply.** Power supply for high voltage interface.	—	—	—	—
					Ground				
GNDA	C2	23	N/A	I	**Analog Ground.** Ground reference for the internal analog section.	—	—	—	—
GNDL	B3	30	N/A	I	**Digital Ground.** Ground reference for interface section.	—	—	—	—
GNDHS	G1	21	N/A	I	**Headset Ground.** Ground reference for the internal analog section.	—	—	—	—
GNDCP	F6	12	N/A	I	**Charge Pump Ground.** Ground reference for the internal HP amplifiers charge pump.	—	—	—	—
GNDD	B6	38	N/A	I	**Digital Ground.** Ground reference for the internal digital circuits.	—	—	—	—
					Test				
TSTI	C7	5	N/A	I	**Test input.** Connect to GNDD	—	—	—	—
TSTI	D3	32	VL	I	**Test input.** Connect to GNDD.	—	—	—	—
TSTI	D1, E1, E2, F1, F2, G3	—	VP	I	**Test input.** Connect to GNDA.	—	—	—	—
TSTI	D2	—	VA	I	**Test input.** Connect to GNDA.	—	—	—	—
TSTO	A4, A6	33,37	VL	O	**Test output.** No connection	—	—	—	—
TSTO	E3, F3, F4	18,19, 22	VP	O	**Test output.** No connection	—	—	—	—

1. There are no internal connections for the CS43L36.
2. The power supply is determined by ADPTPWR setting (see Section 7.10.1). VP is used if ADPTPWR = 001 (VP_CP Mode) or when necessary for ADPTPWR = 111 (Adapt-to-Signal Mode).

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS43L36 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

Fig. 1-3 provides a composite view of the ESD domains showing the ESD protection paths between each pad and the substrate (GNDA) and the interrelations between some domains. Note that this figure represents the structure for the internal protection devices and that additional protections can be implemented as part of the integration into the board.



Note: The asterisks indicate the pads with which the individual pins from the corresponding domains are associated. These pins are listed in Table 1-2.

Figure 1-3. Composite ESD Topology

Table 1-2 shows the individual ESD domains and lists the pins associated with each domain.

Table 1-2. ESD Domains

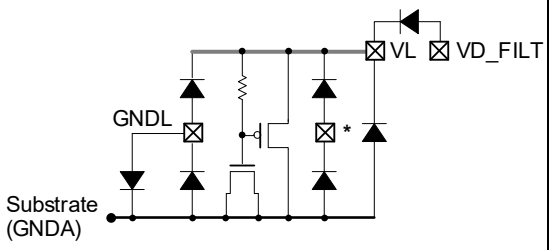
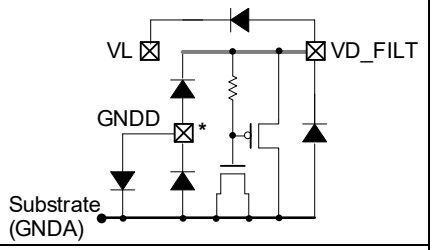
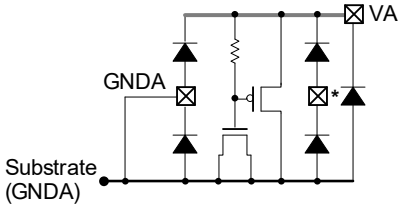
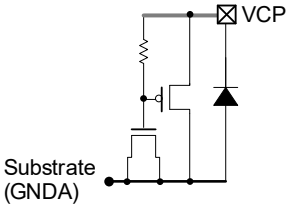
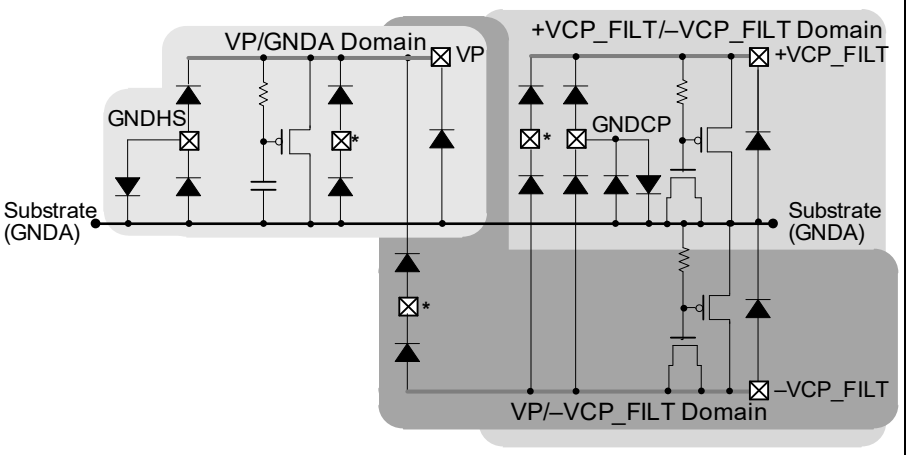
ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VL/ GNDA [1]	AD0 AD1 ASP_LRCK/FSYNC GNDL SCL SDA TSTO TSTO TSTI ASP_SCLK ASP_SDIN VD_FILT VL	
VD_FILT/ GNDA	VD_FILT GNDD TSTI	
VA/ GNDA	FILT+ GNDA TSTI VA	
VCP/ GNDA	VCP	

Table 1-2. ESD Domains *(Cont.)*

ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VP/ GNDA	GNDHS HS3 TSTO TSTI TSTI TSTO TSTO TSTI VP VL_SEL INT WAKE RESET DIGLDO_PDN	
+VCP_ FILT/ –VCP_ FILT	+VCP_FILT –VCP_FILT FLYN HPSENSA HPSENSB HPOUTA HPOUTB GNDCP	
VP/ –VCP_ FILT	FLYC FLYP HS3_REF TSTO TSTI TIP_SENSE	

1. See Section 5.5 for additional information regarding VD_FILT andVL.

2 Typical Connections

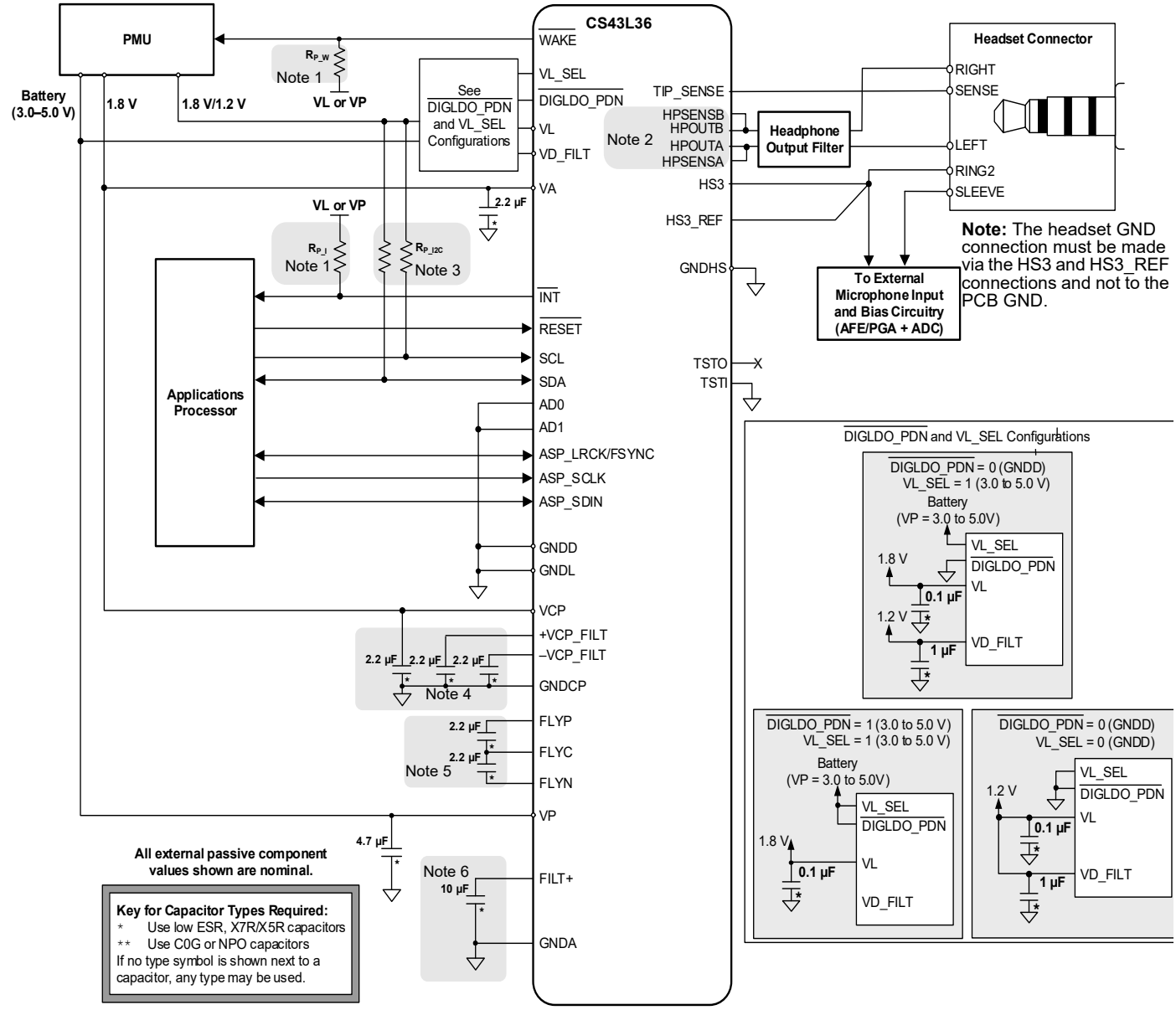


Figure 2-1. Typical Connection Diagram

Notes:

1. R_{P_I} and R_{P_W} values can be determined by the $\overline{INT}$ and $\overline{WAKE}$ pin specifications in Table 3-14.
2. HPSENSA and HPSENSB are supported only on the WLCSP package.
3. R_{P_I2C} values can be determined by the I^2C pull-up resistance specification in Table 3-13.
4. The headphone amplifier's output power and distortion ratings use the nominal capacitances shown. Larger capacitance reduces ripple on the internal amplifiers' supplies and, in turn, reduces distortion at high-output power levels. Smaller capacitance may not reduce ripple enough to achieve output power and distortion ratings. Because actual values of typical X7R/X5R ceramic capacitors deviate from nominal values by a percentage specified in the manufacturer's data sheet, capacitors must be selected for minimum output power and maximum distortion required. Higher value capacitors than those shown may be used, however lower value capacitors must not (values can vary from the nominal by ±20%). See Section 2.1.2 for additional details.
5. Series resistance in the path of the power supplies must be avoided. Any voltage drop on VCP directly affects the negative charge-pump supply (–VCP_FILT) and clips the audio output.
6. Lowering capacitance below the value shown affects PSRR, THD+N performance, and interchannel isolation and intermodulation.

2.1 Electromagnetic Compatibility (EMC) Circuitry

The circuit in Fig. 2-2 may be applied to signals not local to the CS43L36 (i.e., that traverse significant distances) for EMC.

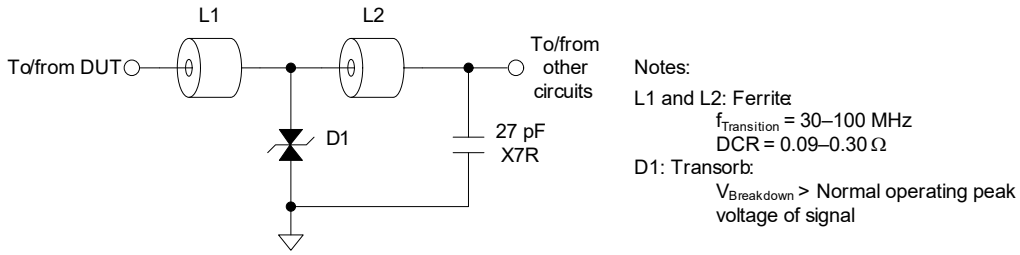


Figure 2-2. Optional EMC Circuit

2.1.1 Low-Profile Charge-Pump Capacitors

In the typical connection for analog mics (Fig. 2-1), the recommended capacitor values for the charge-pump circuitry are 2.2 µF, rated as X7R/X5R or better. The following low-profile versions of these capacitors are suitable for the application:

- Description: 2.2 µF ±20%, 6.3 V, X5R, 0201
- Manufacturer, Part Number: Murata, GRM033R60J225ME47, nominal height = 0.3 mm
- Manufacturer, Part Number: AVX, 02016D225MAT2A, nominal height = 0.33 mm

Note: Although the 0201 capacitors described are suitable, larger capacitors such as 0402 or larger may provide acceptable performance.

2.1.2 Ceramic Capacitor Derating

Note 4 in Fig. 2-1 highlights that ceramic capacitor derating factors can significantly affect in-circuit capacitance values and, in turn, CS43L36 performance. Under typical conditions, numerous types and brands of large-value ceramic capacitors in small packages exhibit effective capacitances well below their ±20% tolerance, with some being derated by as much as –50%. These same capacitors, when tested by a multimeter, read much closer to their rated value. A similar derating effect has not been observed with tantalum capacitors.

The derating observed varied with manufacturer and physical size: Larger capacitors performed better, as did ones from Kemet Electronics Corp. and TDK Corp. of any size. This derating effect is described in data sheets and in applications notes from capacitor manufacturers. For instance, as DC and AC voltages are varied from the standard test points (applied DC and AC voltages for standard test points versus PSRR test are 0 and 1 V_{RMS} @ 1 kHz versus 0.9 V and ~1 mV_{RMS} @ 20 Hz–20 kHz), it is documented that the capacitances vary significantly.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60 dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Offset error	The deviation of the midscale transition (111…111 to 000…000) from the ideal.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz) relative to the rms value of the signal. THD+N is measured at –1 and –20 dBFS for the analog input and at 0 and –20 dB for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.

Table 3-2. Recommended Operating Conditions

Test conditions: GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground.

Parameters		Symbol	Minimum	Maximum	Unit
DC power supply	Charge pump	VCP	1.66	1.94	V
	LDO regulator for digital [1] $\overline{\text{DIGLDO\_PDN}}$ = 0 and VL_SEL = 0	VD_FILT	1.10	1.30	V
	Serial interface control port $\overline{\text{DIGLDO\_PDN}}$ = 0 and VL_SEL = 0	VL	1.10	1.30	V
	VL_SEL = 1	VL	1.66	1.94	V
	Analog	VA	1.66	1.94	V
	Battery supply	VP	2.50 [2]	5.25	V
External voltage applied to pin [3,4]	TIP_SENSE pin	V_{INHI}	–VCP_FILT	VP	V
	±VCP_FILT domain pins [5]	V_{VCPF}	–VCP_FILT	+VCP_FILT	V
	VL domain pins	V_{VL}	0	VL	V
	VA domain pins	V_{VA}	0	VA	V
	VP domain pins	V_{VP}	0	VP	V
Ambient temperature		T_A	–40	+85	°C

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. If $\overline{\text{DIGLDO\_PDN}}$ is deasserted, no external voltage must be applied to VD_FILT.
2. Although device operation is guaranteed down to 2.5 V, device performance is guaranteed only down to 3.0 V. The following are affected when VP < 3.0 V: charge pump LDO, TIP_SENSE threshold.
3. The maximum over/undervoltage is limited by the input current.
4. Table 1-1 lists the power supply domain in which each CS43L36 pin resides.
5. ±VCP_FILT is specified in Table 3-8.

Table 3-3. Absolute Maximum Ratings

Test conditions: GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground.

Parameters		Symbol	Minimum	Maximum	Unit
DC power supply	Charge pump, LDO, serial/control, analog (see Section 4.9)	VL, VA, VCP	–0.3	2.33	V
	Digital core	VD_FILT	–0.3	1.55	V
	Battery	VP	–0.3	6.3	V
Input current [1]		I_{in}	—	±10	mA
Ambient operating temperature (power applied)		T_A	–50	+115	°C
Storage temperature		T_{stg}	–65	+150	°C

Caution: Stresses beyond "Absolute Maximum Ratings" levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2, "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supply pins. Transient currents of up to ±100 mA on analog input pins do not cause SCR latch-up.

Table 3-4. Combined DAC Digital, On-Chip Analog, and HPOUTx Filter Characteristics

Test conditions (unless specified otherwise): T_A = +25°C; MCLK = 12 MHz, MCLK_SRC_SEL = 0, Fs_{INT} = 48 kHz; path is internal routing engine to HPOUTx, analog and digital gains are all set to 0 dB; HPF disabled.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband	–0.05-dB corner –3.0-dB corner	— —	0.48 0.50	— —	Fs_{INT} Fs_{INT}
Passband ripple ($0.417x10^{-3}$ Fs_{INT} to 0.417 Fs_{INT}; normalized to $0.417x10^{-3}$ Fs_{INT})		–0.04	—	0.063	dB
Stopband attenuation (0.545 Fs_{INT} to Fs_{INT})		60	—	—	dB
Total group delay [2]		—	5.35/Fs_{INT}	—	s

1. Response scales with Fs_{INT} (based on internal MCLK). Specifications are normalized to Fs_{INT} and denormalized by multiplying by Fs_{INT}.
2. Informational only; group delay cannot be measured for this block by itself. An additional 5.5/Fs_{int} group delay may be present through the serial ports and internal audio bus.

Table 3-5. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise) Analog and digital gains are all set to 0 dB; T_A = +25°C.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband	–0.05-dB corner –3.0-dB corner	— —	$0.180x10^{-3}$ $19.5x10^{-6}$	— —	Fs_{INT} Fs_{INT}
Passband ripple ($0.417x10^{-3}$ Fs_{INT} to 0.417 Fs_{INT}; normalized to 0.417 Fs_{INT})		—	—	0.01	dB
Phase deviation @ $0.453x10^{-3}$ Fs_{INT}		—	2.45	—	°
Filter settling time [2]		—	$24.5x10^{3}$/Fs_{INT}	—	s

1. Response scales with Fs_{INT} (internal sample rate, based on MCLK). Specifications are normalized to Fs_{INT} and are denormalized by multiplying by Fs_{INT}.
2. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

Table 3-6. SDIN to HPOUTx with SRC-Enabled Datapath Characteristics

Test conditions (unless specified otherwise): LRCK = Fs_{INT} = Fs_{EXT} = 48 kHz; MCLK = 12 MHz; HPF disabled; passband/stopband levels normalized to $0.417x10^{-3}$ Fs_{EXT}; entire path characteristics including serial port + SRC + DAC + HPOUT.

Parameters [1]		Minimum	Typical	Maximum	Unit
Passband	–0.2-dB corner –3.0-dB corner	— —	0.463 0.466	— —	Fs_{EXT} Fs_{EXT}
Passband ripple ($0.417x10^{-3}$ Fs_{EXT} to 0.417 Fs_{EXT}; normalized to $0.417x10^{-3}$ Fs_{EXT})		–0.16	—	0.02	dB
Response at 0.5 Fs_{EXT}		—	—	–54.9	dB
Stopband rejection from 0.480 Fs_{EXT} to 0.524 Fs_{EXT}		55	—	—	dB
Stopband rejection from 0.524 Fs_{EXT} to 0.545 Fs_{EXT}		39	—	—	dB
Stopband rejection from 0.545 Fs_{EXT} to 3 Fs_{EXT}		60	—	—	dB
Square wave overshoot		—	—	3.1	dB
Group delay, bark-weighted average		—	—	34/Fs_{EXT}	s
Group delay	$Fs_{EXT} \le$ 48 kHz $Fs_{EXT} \ge$ 88.2 kHz)	— —	(15.8 ± 1.5)/Fs_{EXT} + 10.3/Fs_{INT} (20.1 ± 1)/Fs_{EXT} + (11.6 ± 0.5)/Fs_{INT}	— —	s s
SRC disabled group delay [2]		—	(15±1)/Fs	—	s

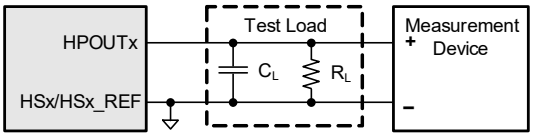
1. Fs_{EXT} is the external sample rate (LRCK/FSYNC frequency). Response scales with Fs_{EXT}.
2. This value varies by up to 1 Fs. If SRC is disabled, Fs = Fs_{OUT} = Fs_{IN}.

Table 3-7. Serial Data In-to-HPOUTx Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; input test signal is a 24-bit full-scale 997-Hz sine wave with 1 LSB of triangular PDF dither applied; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters can vary with VA; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V; VL = 1.8 V, VP = 3.6 V; VCP Mode; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_LRCK = Fs_{INT} = 48-kHz mode; MCLK = 12 MHz, MCLK_SRC_SEL = 0; volume = 0 dB; FULL_SCALE_VOL = 0 (0dB); HP load: R_L = 30 Ω, C_L = 1 nF (HPOUT_LOAD = 0) and R_L = 3 kΩ, C_L = 10 nF (HPOUT_LOAD = 1)SRC bypassed.

Parameter [1]				Minimum	Typical	Maximum	Unit
R_L = 3 kΩ VP_CP Mode	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2] (defined in Table 3-1)	18–24 bit	0 dB	—	–90	–84	dB
			–20 dB	—	–83	—	dB
			–60 dB	—	–51	–48	dB
		16 bit	0 dB	—	–88	–82	dB
			–20 dB	—	–73	—	dB
			–60 dB	—	–33	–27	dB
	Idle channel noise (A-weighted)			—	2.0	—	µV
	Full-scale output voltage [3]			1.50•VA	1.58•VA	1.66•VA	V_{PP}
R_L = 30 Ω VP_CP Mode	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2] (defined in Table 3-1)		Pout = 10 mW	—	–98	—	dB
			Pout = 35 mW	—	–75	–69	dB
	Full-scale output voltage [3]			1.50•VA	1.58•VA	1.66•VA	V_{PP}
	Output power [2]			—	35.0	—	mW
R_L = 15 Ω VCP Mode (FULL_SCALE_ VOL = 1 [–6 dB])	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
	THD+N [2] (defined in Table 3-1)		Pout = 17.3 mW	—	–75	–69	dB
	Full-scale output voltage [3]			0.71•VA	0.79•VA	0.86•VA	V_{PP}
	Output power [2]			—	17.3	—	mW
R_L = 15 Ω VP_CP Mode	Dynamic range	18–24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
Other characteristics (Table 3-1 gives parameter definitions.)	Interchannel isolation [3] (3 kΩ)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	80	—	dB
	Interchannel isolation [3] (30 Ω)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	70	—	dB
	Output offset voltage: mute [3,4] (ANA_MUTE_x = 1, see p. 77)		HPOUTx	—	±0.5	±1.0	mV
	Output offset voltage [3,4]		HPOUTx	—	±0.5	±2.5	mV
	Load resistance (R_L)		Normal operation [3]	15	—	—	Ω
	Load capacitance (C_L) [3,5]		HPOUT_LOAD = 0	—	—	1	nF
			HPOUT_LOAD = 1	—	—	10	nF
	Turn-on time [6]		SLOW_START_EN = 000	—	—	25	ms

1. One LSB of triangular PDF dither is added to data.
2. Because VCP settings lower than VA reduce the HP amplifier headroom, the specified THD+N performance at full-scale output voltage and power may not be achieved.
3. HP output test configuration. Symbolized component values are specified in the test conditions above.



4. Assumes no external impedance on HSx/HSx_REF. External impedance on HSx/HSx_REF affects the offset and step deviation. See Section 4.2.1.
5. Amplifier is guaranteed to be stable with either headphone load setting.
6. Turn-on time is measured from when the HP_PDN = 0 ACK signal is received to when the signal appears on the HP output. In most cases, enabling the SRC increases the turn-on time and may exceed the maximum specified value.

Table 3-8. DC Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VCP = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters			Minimum	Typical	Maximum	Unit
VCP_FILT (No load connected to HPOUTx.)	VP_CP Mode (ADPTPWR = 001)	+VCP_FILT	—	2.6	—	V
		–VCP_FILT	—	–2.6	—	V
	VCP Mode (ADPTPWR = 010)	+VCP_FILT	—	VCP	—	V
		–VCP_FILT	—	–VCP	—	V
	VCP/2 Mode (ADPTPWR = 011)	+VCP_FILT	—	VCP/2	—	V
		–VCP_FILT	—	–VCP/2	—	V
	VCP/3 Mode (ADPTPWR = 100)	+VCP_FILT	—	VCP/3	—	V
		–VCP_FILT	—	–VCP/3	—	V
HS3 ground switch resistance (Typical values have ±25% tolerance.)			—	0.5	—	Ω
Other DC filter	FILT+ voltage		—	VA	—	V
	HP output current limiter on threshold. See Section 4.3.4. [1]		80	115	160	mA
	VD_FILT and VL power-on reset threshold (V_{POR})	Up	—	0.777	—	V
		Down	—	0.628	—	V
HPOUT pull-down resistance [2,3]	HPOUT_PULLDOWN = 0000–0111, 1100		—	0.9	—	kΩ
	HPOUT_PULLDOWN = 1001		—	9.3	—	kΩ
	HPOUT_PULLDOWN = 1010		—	5.8	—	kΩ

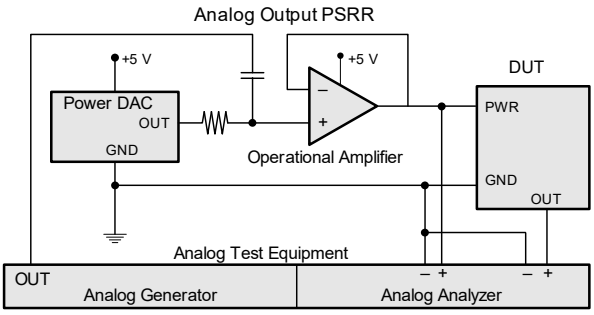
1. The HP output current limiter threshold spec is valid only while the Class H rails are in VCP Mode.
2. Typical values have ±20% tolerance.
3. Clamp is disabled (HPOUT_CLAMP = 1) and channel is powered down (HPOUT_PDN = 1).

Table 3-9. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters [1]		Minimum	Typical	Maximum	Unit
HPOUTx (–6-dB analog gain) PSRR with 100-mVpp signal AC coupled to VA supply [2]	217 Hz	—	75	—	dB
	1 kHz	—	75	—	dB
	20 kHz	—	70	—	dB
HPOUTx (–6-dB analog gain) PSRR with 100-mVpp signal AC-coupled to VCP supply [2]	217 Hz	—	85	—	dB
	1 kHz	—	85	—	dB
	20 kHz	—	65	—	dB
HPOUTx (0-dB analog gain) PSRR with 100-mVpp signal AC coupled to VP supply	217 Hz	—	80	—	dB
	1 kHz	—	80	—	dB
	20 kHz	—	60	—	dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.



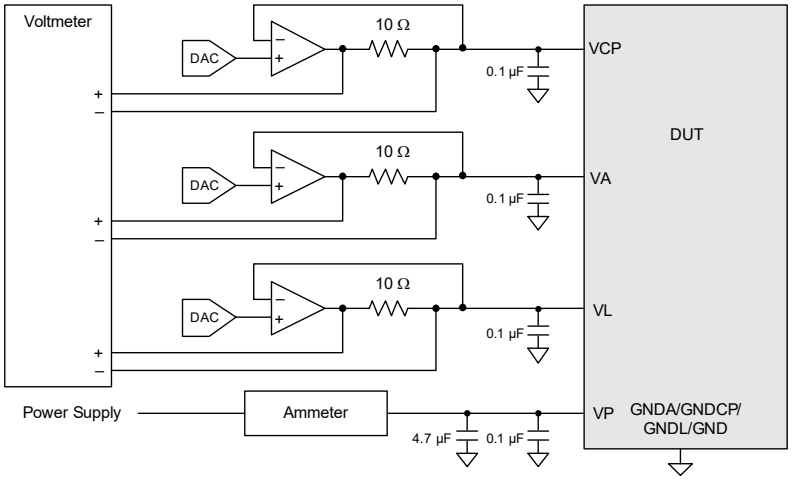
2. No load connected to any analog outputs.

Table 3-10. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; performance data taken with VA = VCP = VL = 1.8 V; DIGLDO_PDN is deasserted; VP = 3.6 V; T_A = +25°C; ASP_LRCK = 48-kHz Mode; Fs_{INT} = 48 kHz; SCLK = 12 MHz, MCLK_SRC_SEL = 0; volume= 0 dB; FULL_SCALE_VOL = 1 (–6 dB) for HPOUTx, TIP_SENSE_CTRL = 11, all other fields are set to defaults; no signal on any input; control port inactive; input clock/data are held low when not required; test load is R_L = 30 Ω and C_L = 1 nF for HPOUTx; measured values include currents consumed by the DAC and do not include current delivered to external loads unless specified otherwise (e.g., HPOUTx); see Fig. 3-1.

Use Cases			Class H Mode	Typical Current (µA)				Total Power (µW)
				i_{VA}	i_{VCP}	i_{VL}	i_{VP}	
1	A	Off [1]	—	0	0	0	3.1	11.16
2	A	Standby [2,3]	—	0	0	0	20	72.0
3	A	Standby (RCO Mode) [4,5]	—	0	0	343	31	729
4	A	Playback — Stereo HPOUT (no signal, HPOUT_LOAD = 0)	VCP/3	1413	1204	858	58	6464
	B	Stereo HPOUT (0.1 mW, HPOUT_LOAD = 0)	VCP/3	1441	2336	965	58	8744

1. Off configuration: Clock/data lines held low; $\overline{\text{RESET}}$ = LOW; VA = VL = VCP = 0 V; VP = 3.6 V.
2. Standby configuration: Clock/data lines held low; VA = VL = VCP = 0 V; VP = 3.6 V; M_HP_WAKE = 0 (unmasked).
3. SCLK_PRESENT = 1.
4. SCLK_PRESENT = 0 (RCO clocking).
5. Standby configuration (RCO clocking): Clock/data lines held low; VA = 0 V; VL = 1.8 V, VCP = 0 V, VP = 3.6 V; M_HP_WAKE = 0 (unmasked).



Note: The current draw on the VA, VCP, and VL power supply pins is derived from the measured voltage drop across a 10-Ω series resistor between the associated supply source and each voltage supply pin. Given the larger currents that are possible on the VP supply, an ammeter is used for the measurement.

Figure 3-1. Power Consumption Test Configuration

Table 3-11. Register Field Settings

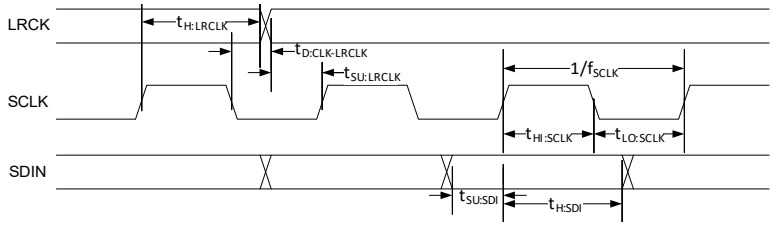
Use Cases		Register Fields and Settings				
		PDN_ALL	ASP_DAI_PDN	HP_PDN		Class H Mode p. 23
1	A	—	—	—		—
2	A	1	—	—		—
3	A	1	—	—		—
4	A	0	0	0		VCP/3
	B	0	0	0		VCP/3

Table 3-12. Digital Audio Interface Timing Characteristics

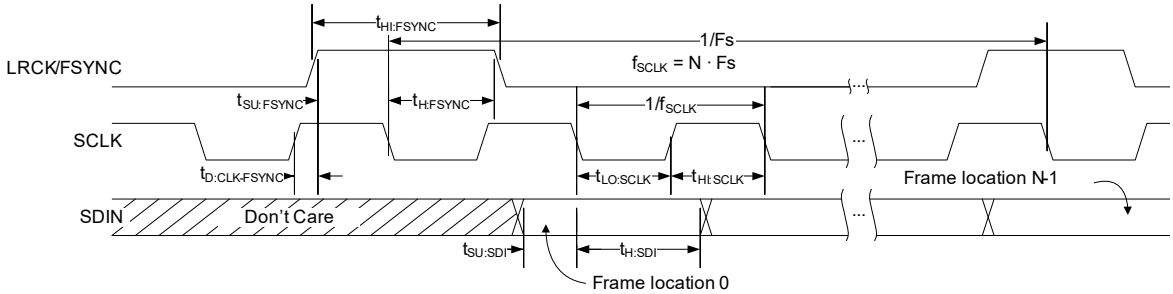
Test conditions (unless specified otherwise): GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; values are for both VL = 1.2 and 1.8 V; inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL; T_A = +25°C; C_{LOAD} = 30 pF (for VL = 1.2 V) and 60 pF (for VL = 1.8 V); input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-14); ASP_TX_HIZ_DLY = 00.

Parameters [1,2,3]			Symbol	Minimum	Typical	Maximum	Unit
ASP_SCLK frequency [4]			f_{SCLK}	0.973 [5]	—	25.81	MHz
SCLK high period [4]			$t_{HI:SCLK}$	18.5	—	—	ns
SCLK low period [4]			$t_{LO:SCLK}$	18.5	—	—	ns
SCLK duty cycle [4]			—	45	—	55	%
Hybrid-Master Mode	FSYNC/LRCK frame rate		—	0.99	—	1.01	Fs
	LRCK duty cycle		—	45	—	55	%
	FSYNC high period [6]		$t_{HI:FSYNC}$	1/f_{SCLK}	—	(n–1)/f_{SCLK}	s
	FSYNC/LRCK delay time after SCLK launching edge [7]	VL = 1.8 V VL = 1.2 V	$t_{D:CLK–LRCK}$	0 0	— —	15 17	ns ns
	SDIN setup time before SCLK latching edge [7]		$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [7]		$t_{H:SDI}$	5	—	—	ns
Slave Mode	FSYNC/LRCK frame rate		—	0.99	—	1.01	Fs
	FSYNC/LRCK duty cycle		—	45	—	55	%
	FSYNC/LRCK setup time before SCLK latching edge [7]		$t_{SU:LRCK}$	10	—	—	ns
	FSYNC/LRCK hold time after SCLK latching edge [7]		$t_{H:LRCK}$	5	—	—	ns
	SDIN hold time after SCLK latching edge [7]		$t_{H:SDI}$	5	—	—	ns
	FSYNC/LRCK duty cycle		—	45	—	55	%

1. Output clock frequencies follow SCLK frequency proportionally. Deviation of the bit-clock source from nominal supported rates is directly imparted to the output clock rate by the same factor (e.g., +100-ppm offset in the frequency of SCLK becomes a +100-ppm offset in MCLK and LRCK).
2. I²S interface timing. Note: SCPOL = 1



3. TDM interface timing. Note: SCPOL = 0



4. SCLK is mastered from an external device. The external device is expected to maintain SCLK timing specifications.
5. SCLK operation below 2.8224 MHz may result in degraded performance.
6. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK_HI is set to 511 SCLK periods and LRCK period is set to 512 SCLK periods.
7. Data is latched on the rising or falling edge of SCLK, as determined by ASP_SCPOL_IN_x and ASP_FSD (See Section 7.3.6 and Section 7.3.7).

Table 3-13. I²C Slave Port Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; min/max performance data taken with VL = 1.66–1.94 V (VL_SEL = VP) or VL = 1.1–1.3 V (VL_SEL = GNDD); inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; T_A = +25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS43L36 with the specified load capacitance.

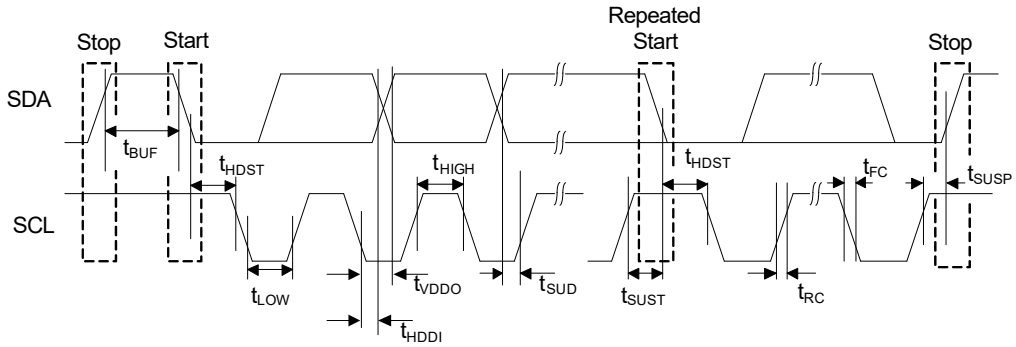
Parameter [2]		Symbol [3]	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{RC}	— — —	1000 300 120	ns ns ns

Table 3-13. I²C Slave Port Characteristics *(Cont.)*

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; min/max performance data taken with VL = 1.66–1.94 V (VL_SEL = VP) or VL = 1.1–1.3 V (VL_SEL = GNDD); inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; T_A = +25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS43L36 with the specified load capacitance.

Parameter [2]		Symbol [3]	Minimum	Maximum	Unit
Fall time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{FC}	— — —	300 300 120	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [4]		t_{HDDI}	0	—	ns
Output data valid (Data/Ack) [5]	Standard Mode Fast Mode Fast Mode Plus	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance	Fast Mode Plus Standard Mode, Fast Mode	C_B	— —	550 400	pF pF
SCL/SDA pull-up resistance [1]	VL = 1.2 V VL = 1.8 V	R_P	200 250	— —	Ω Ω
Switching time between RCO and PLL or SCLK [6]		—	150	—	µs

1. The minimum R_P value (see Fig. 2-1) is determined by using the maximum VL level, the minimum sink current strength of its respective output, and the maximum low-level output voltage, V_{OL}. The maximum R_P value may be determined by how fast its associated signal must transition (e.g., the lower the R_P value, the faster the I²C bus can operate for a given bus load capacitance). See the I²C bus specification referenced in Section 13.
2. All timing is relative to thresholds specified in Table 3-14, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
3. I²C control-port timing



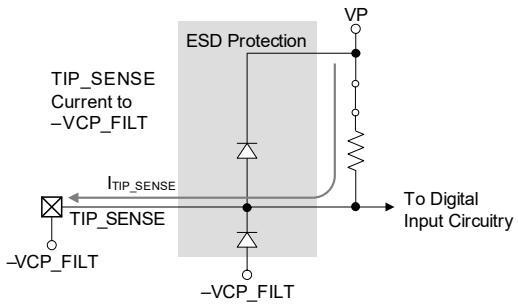
4. Data must be held long enough to bridge the SCL transition time, t_F.
5. Time from falling edge of SCL until data output is valid.
6. The switch between RCO and either SCLK or PLL occurs upon setting/clearing SCLK_PRESENT (see p. 64) and sending the I²C stop condition. An SCLK_PRESENT transition (0 to 1 or 1 to 0) starts a switch between RCO and the selected SCLK or PLL. An I²C stop condition is sent, after which a wait time of at least 150 µs is required before the next I²C transaction can begin using the newly selected clock.

Table 3-14. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; parameters can vary with VL and VP; min/max performance data taken with VCP = VA = 1.8 V, VD_FILT = 1.2 V; VP = 3.0–5.25 V; VL = 1.66–1.94 V (VL_SEL = VP) or VL = 1.1–1.3 V (VL_SEL = GNDD); T_A = +25°C; C_L = 60 pF.

Parameters [1]		Symbol	Min	Max	Unit
Input leakage current [2,3]	ASP_LRCK/FSYNC	I_{in}	—	±4	µA
	ASP_SCLK,ASP_SDIN		—	±3	µA
	TIP_SENSE		—	±100	nA
	SDA, SCL		—	±100	nA
	INT, WAKE, RESET		—	±100	nA
Internal weak pull-down		—	550	2450	kΩ
Input capacitance [2]		—	—	10	pF
INT or WAKE current sink (V_{OL} = 0.3 V maximum)		—	825	—	µA
VL Logic (non-I²C)	High-level output voltage (I_{OH} = –100 µA)	V_{OH}	0.9*VL	—	V
	Low-level output voltage	V_{OL}	—	0.1*VL	V
	High-level input voltage	V_{IH}	0.7*VL	—	V
	Low-level input voltage	V_{IL}	—	0.3*VL	V
VL Logic (I²C only)	Low-level output voltage	V_{OL}	—	0.2*VL	V
	High-level input voltage	V_{IH}	0.7*VL	—	V
	Low-level input voltage	V_{IL}	—	0.3*VL	V
	Hysteresis voltage	V_{HYS}	0.05*VL	—	V
VP Logic (excluding TIP_SENSE)	Low-level output voltage	V_{OL}	—	0.2	V
	High-level input voltage	V_{IH}	0.9	—	V
	Low-level input voltage	V_{IL}	—	0.2	V
TIP_SENSE [4]	High-level input voltage	V_{IH}	0.87*VP	—	V
	Low-level input voltage	V_{IL}	—	2.0	V
TIP_SENSE current to –VCP_FILT [4]	TIP_SENSE_CTRL = 11 (Short-Detect Mode)	I_{TIP_SENSE}	1.00	2.91	µA

1. See Table 1-1 for serial and control-port power rails.
2. Specification is per pin. The CS43L36 is not a low-leakage device, per the *MIPI Specification*. See Section 13.
3. Includes current through internal pull-up or pull-down resistors on pin.
4. TIP_SENSE input circuit. This circuit allows the TIP_SENSE signal to go as low as –VCP_FILT and as high as VP. Section 4.8.2 provides configuration details.



4 Functional Description

This section provides a general description of the CS43L36 architecture and detailed functional descriptions of the various blocks that make up the CS43L36. Fig. 4-1 shows the flow of signals through the CS43L36 and gives links to detailed descriptions of the respective sections.

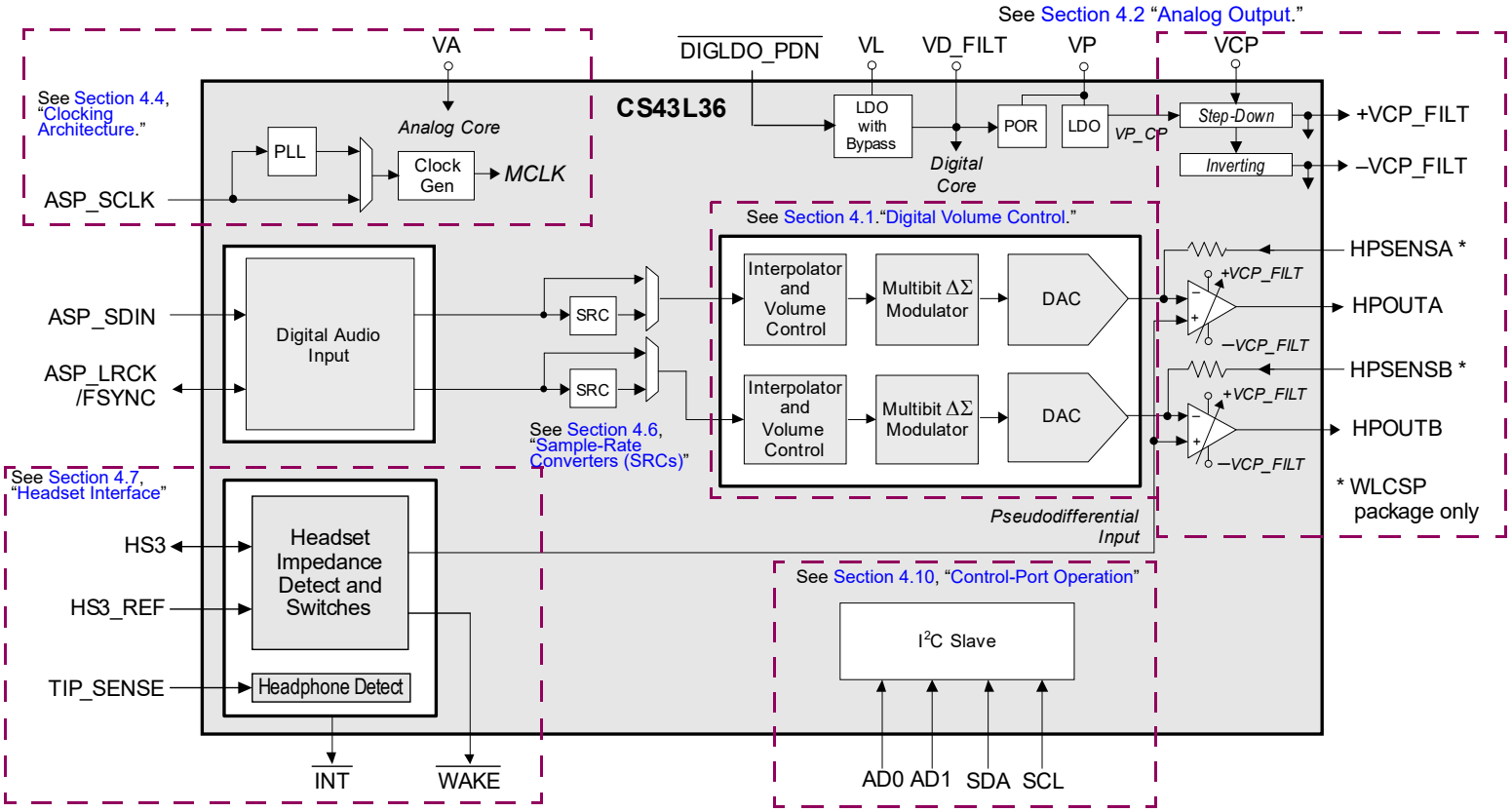


Figure 4-1. Overview of Signal Flow

The CS43L36 is an ultralow-power stereo DAC. The DAC feeds a stereo pseudodifferential output amplifier. The converters operate at a low oversampling ratio, maximizing power savings while maintaining high performance.

The serial data interface ports operate either at standard audio-sample rates as timing slaves or in Hybrid-Master Mode as a bit-clock slave generating LRCK internally. An onboard fractional-N PLL can be used to generate the internal-core timing ($MCLK_{INT}$) if the SCLK source is not one of the following rates (where N = 2 or 4):

- N x 5.6448 or 6.1440 MHz
- USB rates (N x 6 MHz)

The CS43L36 significantly reduces overall power consumption, with a very low-voltage digital core and with low-voltage Class H amplifiers (powered from an integrated LDO regulator and a step-down/inverting charge pump, respectively). The CS43L36 comprises the following subblocks:

- Volume control, described in Section 4.1, uses selectable attenuation to provide relative volume control and to avoid clipping.
- Analog outputs. The analog output block, described in Section 4.2, includes separate pseudodifferential headphone Class H amplifiers. An on-chip step-down/inverting charge pump creates a positive and negative voltage equal to the input or to either one-half or one-third of the input supply for the amplifiers, allowing an adaptable, full-scale output swing centered around ground. The resulting internal amplifier supply can be ±VCP/3, ±VCP/2, ±VCP, or ±2.5 V.

  The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to HP loads at lower supply voltages. The step-down architecture allows the amplifier's power supply to adapt to the required output signal. This adaptive power-supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.

- Class H amplifier. The HP output amplifiers, described in Section 4.3, use a patented Cirrus Logic four-mode Class H technology that maintains high performance and maximizes operating efficiency of a typical Class AB amplifier.
- Clocking architecture. Described in Section 4.4, the clock for the device can be supplied internally from an integrated fractional-N PLL using ASP_SCLK/ as the source clock or the internal PLL can be bypassed and derived directly from the input pin.
- Serial port. The CS43L36 TDM/I²S (ASP) port is a highly configurable serial port. See Section 4.5.

  The ASP can operate in TDM Mode, which includes full-duplex communication, flexible data structuring via control port registers, clock slave mode, and higher bandwidth, enabling more data to be transferred to and from the device.
- Sample-rate converters (SRCs). SRCs, described in Section 4.6, are used to bridge different sample rates at the serial ports within the digital-processing core. SRCs can be bypassed.
- Headset interface. This interface is described in Section 4.7.
- Power management. Several control registers provide independent power-down control of the analog and digital sections of the CS43L36, allowing operation in select applications with minimal power consumption. Power management considerations are described in Section 4.9.
- Control-port operation. The control port, described in Section 4.10, provides access to the registers for configuring the DAC. The control port operation may be completely asynchronous with respect to the audio sample rates. To avoid potential interference problems, control-port data pins must remain static if no operation is required.
- Resets. Section 4.11 describes the reset options—power-on reset (POR), asserting and $\overline{\text{RESET}}$.
- Interrupts. The CS43L36 includes an open-drain interrupt output, $\overline{\text{INT}}$. Interrupt mask registers control whether an event associated with an interrupt status/mask bit pair triggers the assertion of $\overline{\text{INT}}$. See Section 4.12.

Note that the following terms are used interchangeably in this document:

— ASP RX, DAI0, and DAC input

4.1 Digital Volume Control

The internal stereo volume control is shown in Fig. 4-2. Each input can be attenuated via CHx_VOLy. Outputs are available as a source for the DACs.

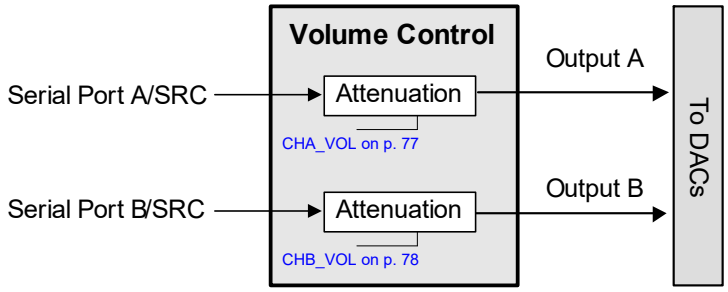


Figure 4-2. Digital Volume Control Subblocks

4.1.1 Attenuation Values

The volume control contains programmable attenuation blocks that are configured as described in the CHx_VOLy field descriptions in Section 7.11.1—Section 7.11.2. For all settings except 0 dB, attenuation on the mixer input includes an offset that increases as attenuation increases, as follows:

- For commonly used –6*n* dB ($n = \{1, 2, \text{etc.}\}$) attenuation settings, the offset rounds the attenuation exactly to the desired $1/2^n$ factor (e.g., 20Log(1/2) = 6.021 dB, not 6.000 dB).
- For attenuation settings other than –6*n* dB, the always positive offset provides slightly more attenuation, giving enough margin to avoid mixer clipping.

4.2 Analog Output

This section describes the headphone (HP) outputs. The CS43L36 provides an analog output that is fed from the mixer. Fig. 4-3 shows the general flow of the analog outputs.

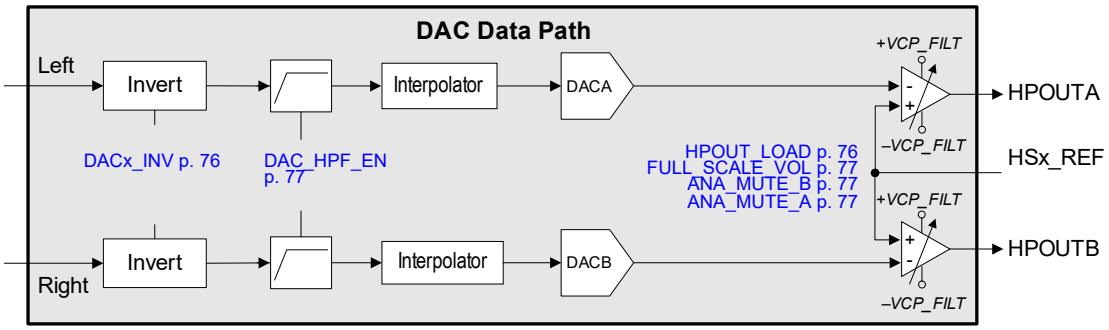


Figure 4-3. Analog-Output Signal Flow

The output path is sourced directly from the digital volume control output. The playback path uses advanced analog and digital signal-processing techniques to adapt to the input signal content and enhance dynamic range and power consumption of the playback path. The HP output must be muted before changing the state of FULL_SCALE_VOL (see p. 77), which sets the maximum HPOUT output voltage. See Table 3-7. HP outputs are muted by ANA_MUTE_B and ANA_MUTE_A (see p. 77).

Fig. 4-4 is an op-amp–level schematic for the analog output flow.

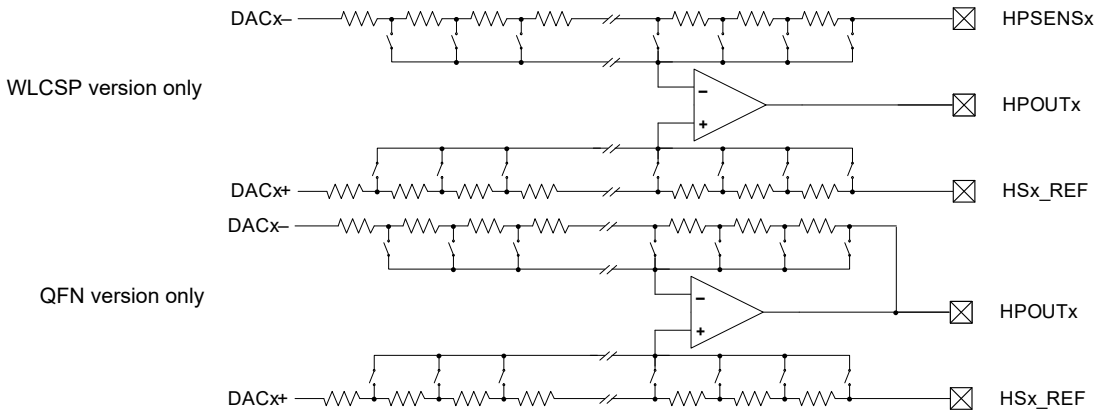


Figure 4-4. Op-Amp-Level Schematic—Analog Outputs

4.2.1 Pseudodifferential Outputs

The analog output amplifiers use a pseudodifferential output topology that allows the amplifier to monitor the ground potential at the load through the reference pins (HSx_REF). Minimize the impedance from the CS43L36 reference pin to the load ground (typically the connector ground). Impedance in this path affects analog output attenuation as well as the common-mode rejection of the output amplifier, which affects output offset and step deviation.

4.2.2 Output Load Detection

The CS43L36 can distinguish between the following output loads:

- R_L = 15, 30, or 3 kΩ
- C_L < ~2 nF (low capacitance); C_L > ~2 nF (high capacitance)

Note: Channels A and B must have matching loads, although load detection is performed using Channel A.

Before output load detection is initiated, the following steps must be performed:

1. HS-type information must be determined to run a headset load-detection sequence, as described in Section 4.8.

2. Power down the HP block: HP_PDN = 1 (see p. 63).
3. Mute the analog outputs: ANA_MUTE_B = ANA_MUTE_A = 1 (see p. 77).
4. Disable the DAC high-pass filter: DAC_HPF_EN = 0 (see p. 77).
   Note: Restore the previous setup after detection completes.
5. Set LATCH_TO_VP (see p. 75).
6. Set ADPTPWR = 100 (see p. 77).
7. Set the analog soft-ramp rate (ASR_RATE = 0111; see p. 61).
8. Set the digital soft-ramp rate (DSR_RATE = 0001; see p. 61).
9. After load detection completes, ASR_RATE, DSR_RATE, ADPTPWR, and DAC_HPF_EN must be restored to their previous values. See Section 4.3 for details.

After an HP-detect event, if HP_LD_EN is set (see p. 74), the CS43L36 proceeds to detect the resistance and capacitance of the output load. A 24-kHz tone is output on HPOUTA, and HS3 is measured using an internal resistor bank as a reference.

RLA_STAT (see p. 74) reports resistance-detection results for Channel A as follows:

- 00: 15 Ω
- 01: 30 Ω
- 10: 3 kΩ
- 11: Reserved

If the typical output resistance of less than ~300 Ω is indicated, a low-capacitance load is assumed. If the resistance is greater than 300 Ω, capacitance detection proceeds. After the detection sequence completes, HPLOAD_DET_DONE (see p. 74) is set. The results of capacitor detection is reported in CLA_STAT (see p. 74). This result can be used to program the value in HPOUT_LOAD(see p. 76), which determines the compensation of the headphone amplifier.

Notes:

- The HP path must be powered down before updating the HPOUT_LOAD setting and repowered afterwards.
- Low capacitance results were determined with C_L = 1 nF; high capacitance results were determined with C_L = 10 nF.

4.2.3 Slow Start Control

Volume control, DAC, and HP soft ramping is enabled through SLOW_START_EN (p. 62). If SLOW_START_EN = 111, changes to DAC/HP volumes are applied slowly by stepping through each volume-control setting with a delay between steps equal to an integer number of Fs periods. The delay between steps, which can vary from 1/Fs to 72/Fs periods, is set via DSR_RATE and ASR_RATE (see p. 61).

If ramping is disabled, changes occur immediately with the clock edge.

4.3 Class H Amplifier

Fig. 4-5 shows the Class H operation.

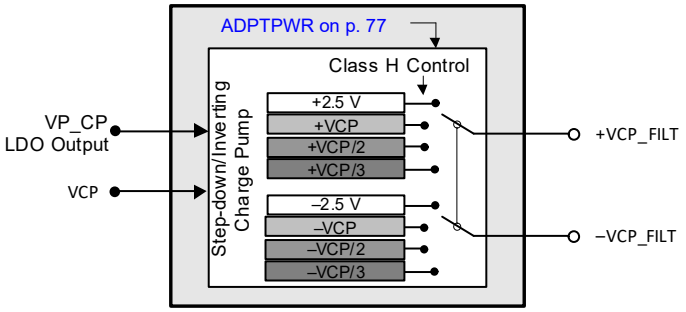


Figure 4-5. Class H Operation

The CS43L36 HP output amplifiers use a Cirrus Logic four-mode Class H technology, which maximizes operating efficiency of the typical Class AB amplifier while maintaining high performance. In a Class H amplifier design, the rail voltages supplied to the amplifier vary with the needs of the music passage being amplified. This conserves energy during low-power passages and when the program material is played back at low volume.

The internal charge pump, which creates the rail voltages for the HP amplifiers, is the central component of the four-mode Class H technology. The charge pump receives its input voltage from the voltage present on either the VCP or VP pin. From this voltage, the charge pump generates the differential rail voltages supplied to the amplifier output stages. The charge pump can supply four sets of differential rail voltages: ±2.5, ±VCP, ±VCP/2, and ±VCP/3.

Table 4-1 shows the nominal signal- and volume-level ranges if the amplifier is set to the adapt-to-signal mode explained in Section 4.3.1. In addition to adapting to the input signal, the Class H control is capable of monitoring the internal headphone amplifier supply to allow more efficient, load-dependent, automatic Smart Class H Mode selection. In fixed modes, if the signal level exceeds the maximum value of the indicated range, clipping can occur.

Table 4-1. Class H Supply Modes

Load		Mode	Class-H Supply Voltage	Signal-Level Range [1,2,3,4]
Resistance	Capacitance			
15 Ω	1 nF	0	±2.5 V	≥ –8 dB
		1	± VCP	–9 to –14 dB
		2	± VCP/2	–15 to –20 dB
		3	± VCP/3	≤ –21 dB
	10 nF	0	±2.5 V	≥ –9 dB
		1	± VCP	–10 to –14 dB
		2	± VCP/2	–15 to –19 dB
		3	± VCP/3	≤ –20 dB
30 Ω	1 or 10 nF	0	±2.5 V	≥ –4 dB
		1	± VCP	–5 to –11 dB
		2	± VCP/2	–12 to –16 dB
		3	± VCP/3	≤ –17 dB
3 kΩ	1 or 10 nF	0	±2.5 V	≥ –1 dB
		1	± VCP	–2 to –8 dB
		2	± VCP/2	–9 to –13 dB
		3	± VCP/3	≤ –14 dB

1. In Adapt-to-Signal Mode, volume level ranges are approximations but are within –0.5 dB from the values shown.
2. Relative to digital full scale with FULL_SCALE_VOL set to 0 dB.
3. In fixed modes, clipping occurs if the signal level exceeds the maximum of this range due to setting the amplifier's supply too low.
4. To optimize efficiency, smart Class H thresholds automatically vary based on load conditions.

4.3.1 Power Control Options

This section describes the supported types of operation: standard Class AB and adapt to signal. The set of rail voltages supplied to the amplifier output stages depends on the ADPTPWR setting, as described in Section 7.10.1.

4.3.1.1 Standard Class AB Operation (ADPTPWR = 001, 010, 011, or 100)

If ADPTPWR is set to 001, 010, 011, or 100, the rail voltages supplied to the amplifiers are held to ±2.5, ±VCP, ±VCP/2, or ±VCP/3, respectively. For these settings, the rail voltages supplied to the output stages are held constant, regardless of the signal level. In these settings, the CS43L36 amplifiers operate in a traditional Class AB configuration.

4.3.1.2 Adapt-to-Output Signal (ADPTPWR = 111)

If ADPTPWR = 111, the rail voltage sent to the amplifiers is based only on whether the signal sent to the amplifiers would cause the amplifiers to clip when operating on the lower set of rail voltages at certain threshold values.

- If clipping can occur, the control logic instructs the charge pump to provide the next higher set of rail voltages.
- If clipping could not occur, the control logic instructs the charge pump to provide the lower set of rail voltages, eliminating the need to advise the CS43L36 of volume settings external to the device.

4.3.2 Power-Supply Transitions

Charge-pump transitions from the lower to the higher set of rail voltages occur on the next FLYN/FLYP clock cycle. Despite the system's fast response time, the VCP_FILT pin's capacitive elements prevent rail voltages from changing instantly. Instead, the rail voltages ramp from the lower to the higher supply, based on the time constant created by the output impedance of the charge pump and the capacitor on the VCP_FILT pin (the transition time is approximately 20 µs).

Fig. 4-6 shows Class H supply switching. During this transition, a high dV/dt transient on the inputs may briefly clip the outputs before the rail voltages charge to the full higher supply level. This transitory clipping has been found to be inaudible in listening tests.

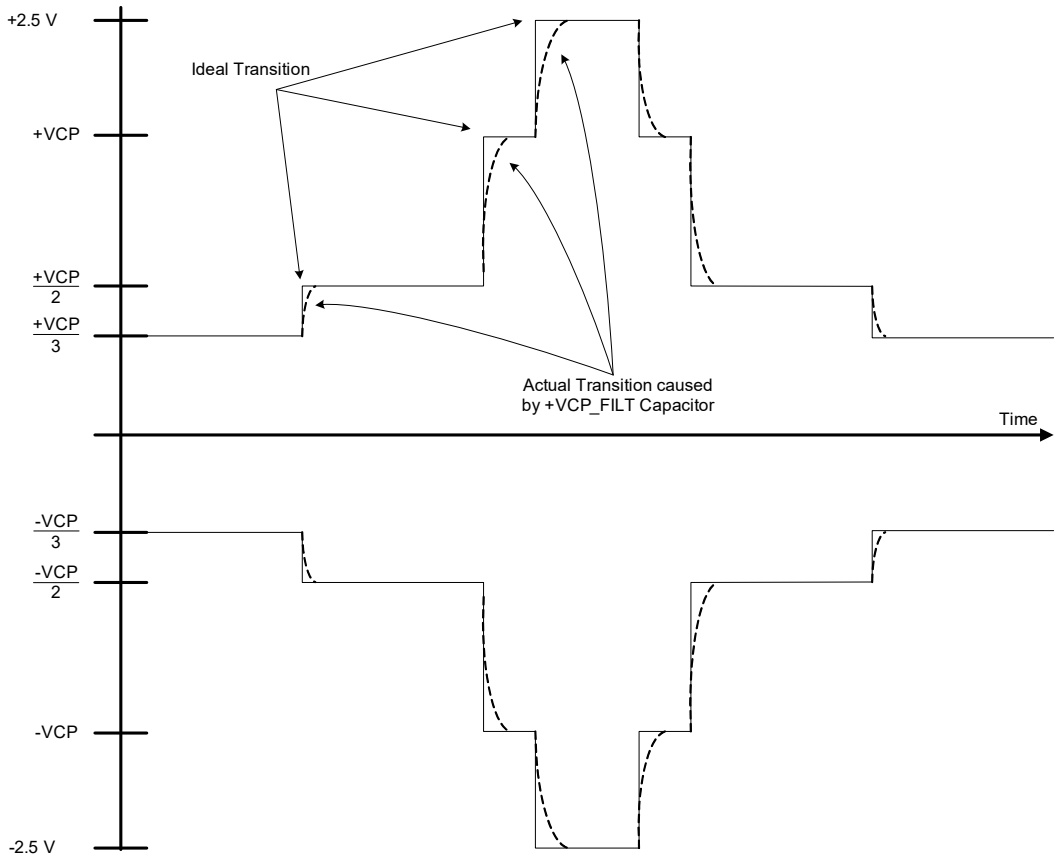


Figure 4-6. VCP_FILT Transitions—Headphone Output

When the charge pump transitions from the higher to the lower set of rail voltages, there is a 5.5-s delay before the charge pump supplies the lower rail voltages to the amplifiers. This hysteresis ensures that the charge pump does not toggle between the two rail voltages as signals approach the clip threshold. It also prevents clipping in the instance of repetitive high-level transients in the input signal. Fig. 4-7 shows this transitional behavior.

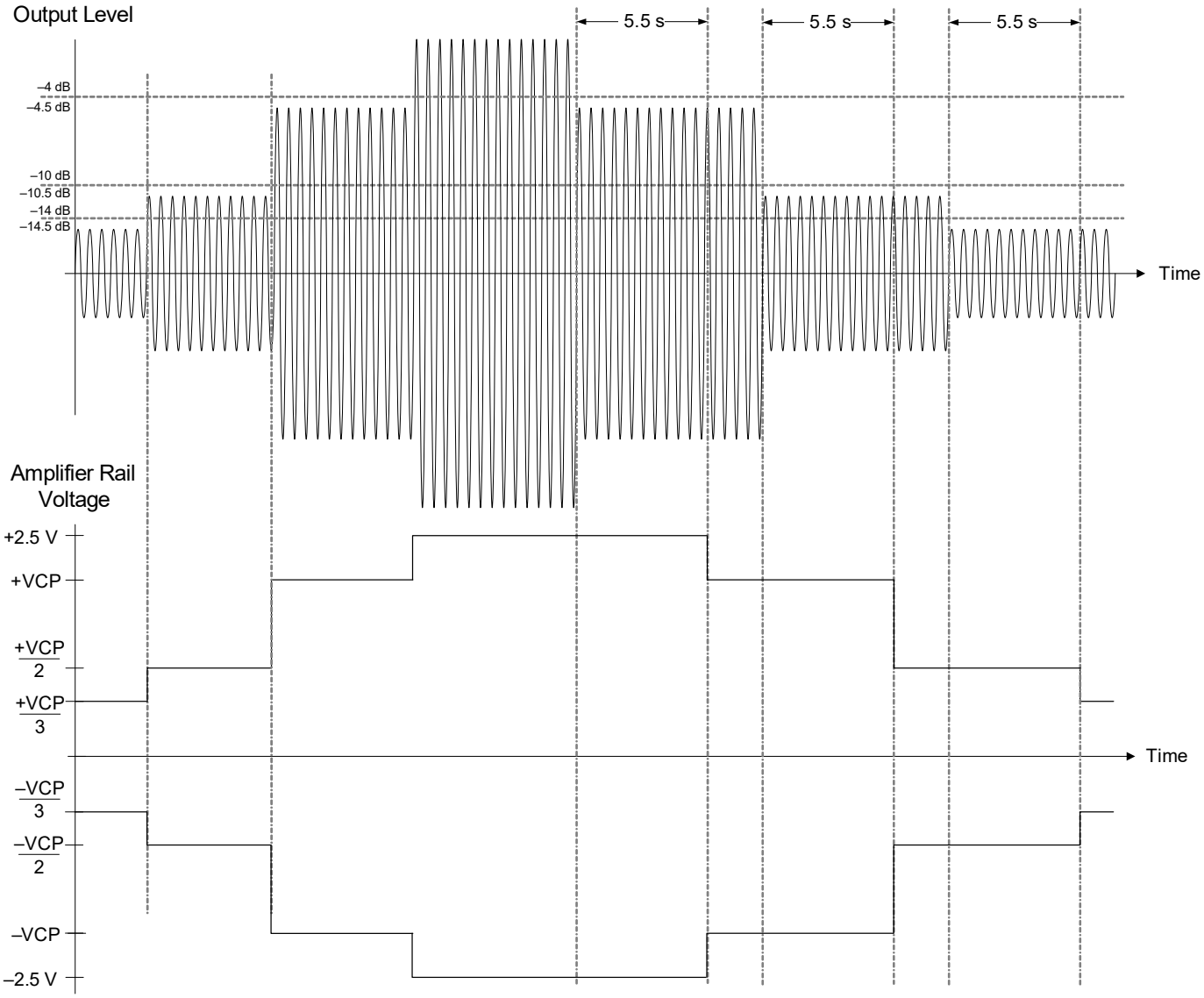


Figure 4-7. VCP_FILT Hysteresis—Headphone Output

4.3.3 Efficiency

As discussed in previous sections, amplifiers internal to the CS43L36 operate from one of four sets of rail voltages, based on the needs of the signal being amplified. Fig. 4-8 and Fig. 4-9 show power curves for all modes of operation and provides details regarding the power supplied to 15- and 30-Ω stereo loads versus the power drawn from the supply for each Class H mode.

If rail voltages are set to ±2.5 V, the amplifiers operate in their least efficient mode for low-level signals. If they are held at ±VCP, ±VCP/2, or ±VCP/3, amplifiers operate more efficiently, but are clipped if required to amplify a full-scale signal.

The adapt-to-signal trace shows the benefit of four-mode Class H operation. At lower output levels, amplifier output is represented by the ±VCP/3 or ±VCP/2 curve, depending on the signal level. At higher output levels, amplifier output is represented by the ±VCP or ±2.5-V curve. The duration for which the amplifiers operate within any of the four curves (±VCP/3, ±VCP/2, ±VCP, or ±2.5 V) depends on both the content and the output level of the material being amplified. The highest efficiency operation results from maintaining an output level that is close to, without exceeding, the clip threshold of the particular supply curve.

Note that the Adapt-to-Signal Mode trace in Fig. 4-8 shows that it never transitions to Mode 0, because FULL_SCALE_VOL = 1 (–6 dB) due to a 15-Ω stereo load.

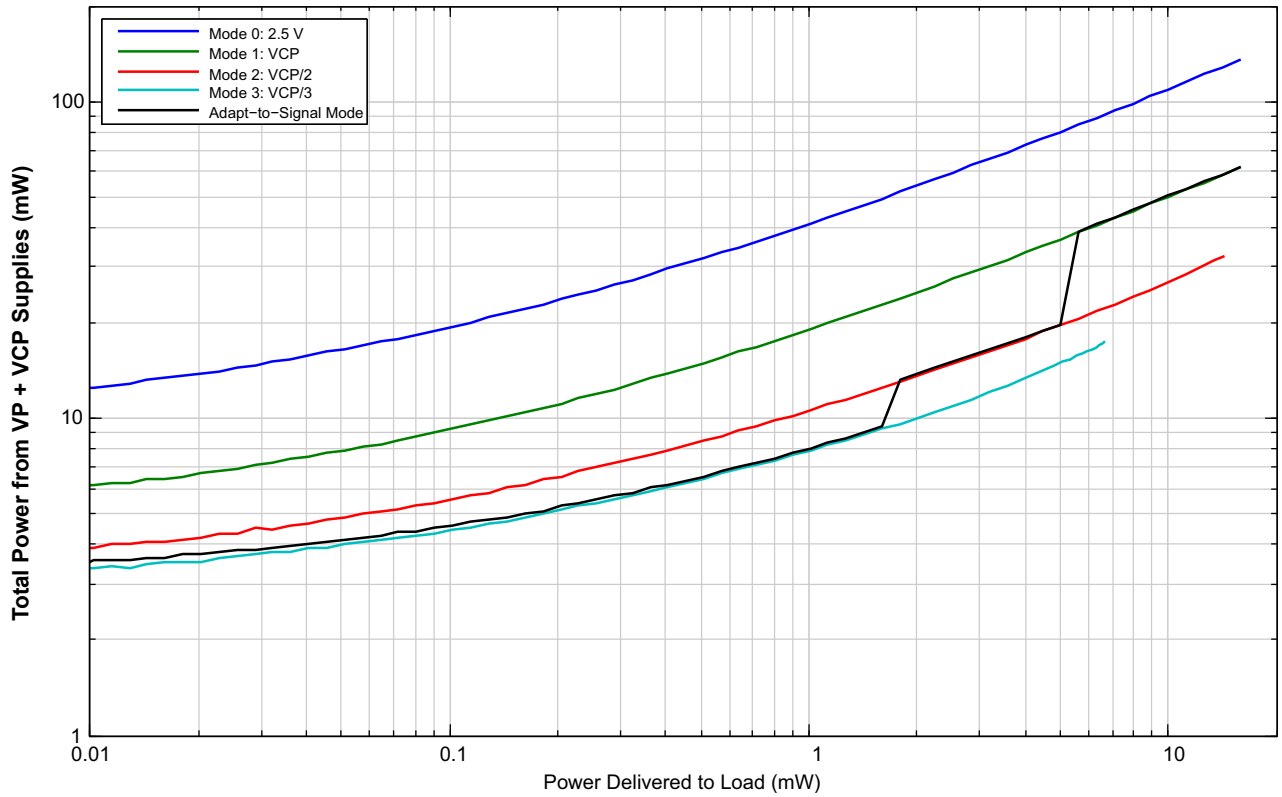


Figure 4-8. Class H Power-to-Load Versus Power from Supply (15 Ω, Stereo)

The Adapt-to-Signal Mode trace in Fig. 4-9 shows the transition to Mode 0, because FULL_SCALE_VOL = 0 (0 dB) due to a 30-Ω stereo load.

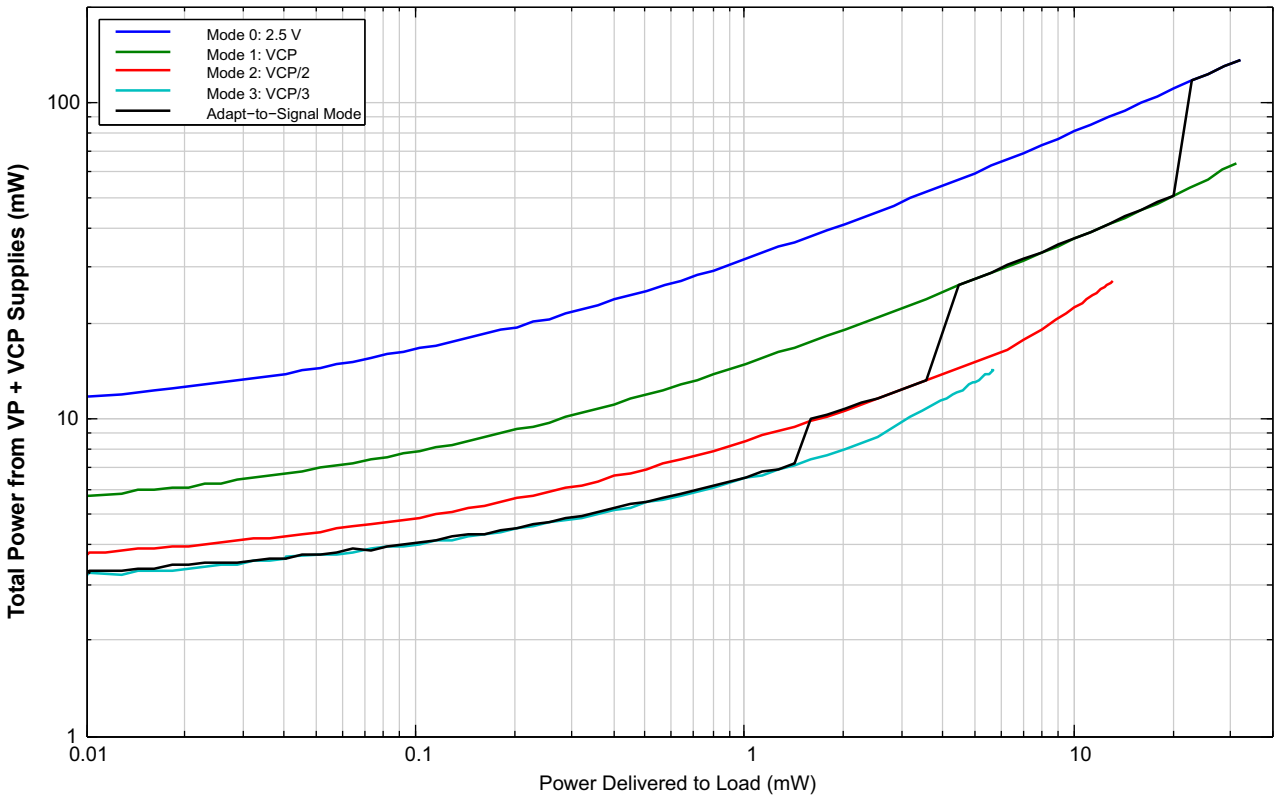


Figure 4-9. Class H Power-to-Load Versus Power from Supply (30 Ω, Stereo)

4.3.4 HP Current Limiter

The CS43L36 features built-in current-limit protection for the HP output. Table 3-8 lists the current limit threshold during the short-circuit conditions shown in Fig. 4-10. For HP amplifiers, current is from the internal charge-pump output, and, as such, applies the current from VCP or VP, depending on the mode.

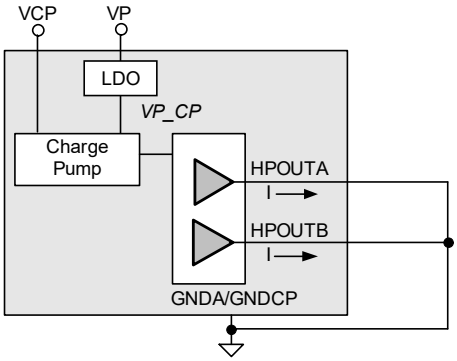


Figure 4-10. HP Short-Circuit Setup

4.4 Clocking Architecture

The CS43L36 offers several ways to support control, ASP operation, data conversion, and signal processing. Internal clocks are generated either from SCLK (ASP_SCLK) or from the integrated fractional-N PLL; see Fig. 4-11. Depending on the MCLK_SRC_SEL setting (see Fig. 4-12), $MCLK_{INT}$ is provided by one of the following methods:

- Externally sourced directly from the ASP_SCLK input pin
- Internally generated from an integrated fractional-N PLL with ASP_SCLK as a reference clock

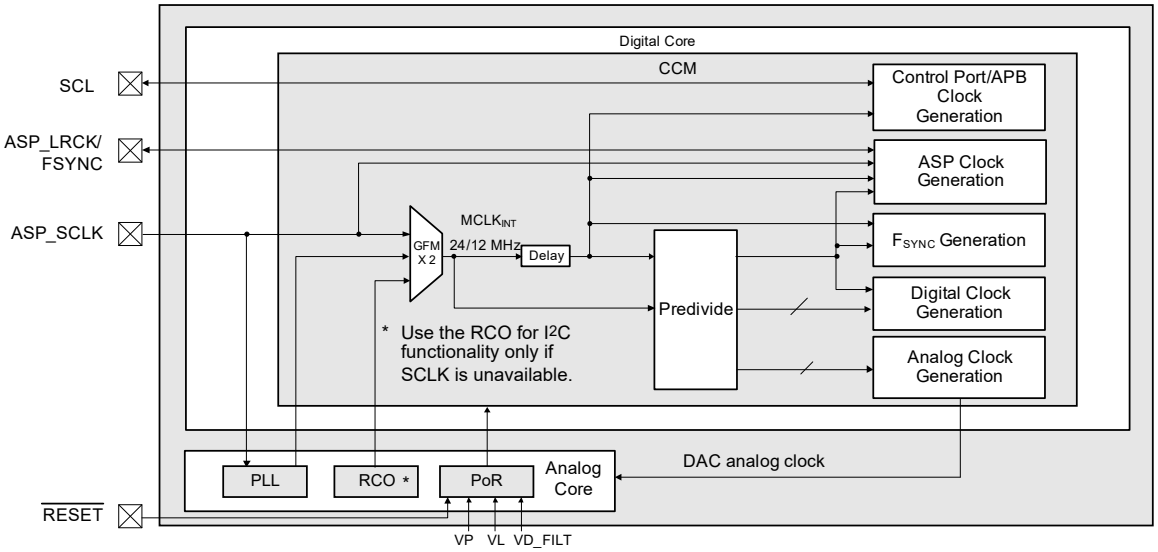


Figure 4-11. Clock Architecture Block Diagram

4.4.1 Start-Up Clocking Using the RC Oscillator (RCO)

At power on, an integrated low-power RCO, shown in Fig. 4-11, functions as the default clock for the digital core of the CS43L36, during which time SCLK is unavailable. A reset event always returns it to running off of the RCO. If SCLK is unavailable, RCO clocking must be used only for I²C functionality.

RCO is multiplexed with $MCLK_{INT}$ and fed to the I²C slave control port. The SCLK must become active and the RCO must be disabled before data conversion.

Note the following:

- OSC_SW_SEL_STAT (see p. 64) indicates the status of the clock switching (in transition, RCO, or SCLK/PLL). With the existing encoding, only one bit can physically change at a time, and the bit changing is always synchronous to the clock that is currently selected.
- OSC_PDNB_STAT (see p. 64) indicates the RCO power-down status.
- SCLK_PRESENT is used to determine the internal MCLK source. See Section 7.2.4 for details.

The clock-switch state machine uses the transition of SCLK_PRESENT to both initiate switches between the selected internal MCLK between the SCLK pin (SCLK_PRESENT = 1) or the internal RCO (SCLK_PRESENT = 0) and to send the I²C stop condition that each switching event requires. During switching, a delay of at least 150 µS is needed before additional successful I²C communication can begin to use the new clocking source.

Notes:

- Muting the system is recommended when a new clock source is chosen.
- For normal operation, SCLK—not RCO—must be used (SCLK_PRESENT = 1) for running the ASP data path.

4.4.1.1 Switching from RCO

With SCLK running, an SCLK_PRESENT 0-to-1 transition starts a switch from the RCO to the selected SCLK or PLL. This switch is superseded by any outstanding I²C transactions. After the I²C stop condition is sent, the transition begins, taking 150 µs to complete, during which time the system requires that no new I²C transactions be initiated. The next I²C transaction can begin after this 150-µs delay.

4.4.1.2 Switching to RCO

To stop SCLK, the system must revert to RCO clocking to ensure that I²C communications function properly. To power the RCO back up, SCLK_PRESENT must be cleared before stopping SCLK. A 1-to-0 SCLK_PRESENT transition generates a glitch-free mux switch timing from SCLK to RCO. SCLK must remain running during the transition and new I²C transactions must not be initiated for at least 150 µs after an I²C stop is received. The next I²C transaction cannot begin until after this 150 µs delay.

Failure to account for this 150 µs delay could cause I²C communications to fail.

4.4.2 $MCLK_{INT}$ Sources

The $MCLK_{INT}$ source is supplied directly from ASP_SCLK input pin or from the fractional-N PLL. MCLKDIV must be set according to the $MCLK_{INT}$ frequency, which must be set to either the 12-MHz region (11.2896–12.288 MHz) or the 24-MHz region (22.5792–24.576 MHz). Table 4-4 shows several examples. Table 4-2 lists further restrictions.

Table 4-2. $MCLK_{INT}$ Source Restrictions

$MCLK_{INT}$ Source	MCLK_SRC_SEL (see p. 65)	MCLKDIV (see p. 65)	Nominal ASP_SCLK Pin Frequency
ASP_SCLK	0	0	12 MHz
		1	24 MHz
Fractional-N PLL	1	0	12 MHz
		1	24 MHz

$MCLK_{INT}$ is switched through internal glitchless clock muxing. Doing so during operation may cause audible artifacts, but does not put the device into an unrecoverable state. Therefore, it is recommended to mute the system for at least 150 µs.

If $MCLK_{INT}$ is sourced from the PLL, on-the-fly frequency changes to the source may cause the PLL to go out of phase lock with the clock source. To reduce the risk of audible artifacts, it is recommended to mute the system first. Any necessary configuration changes based on the new clock source frequency must occur before unmuting the system.

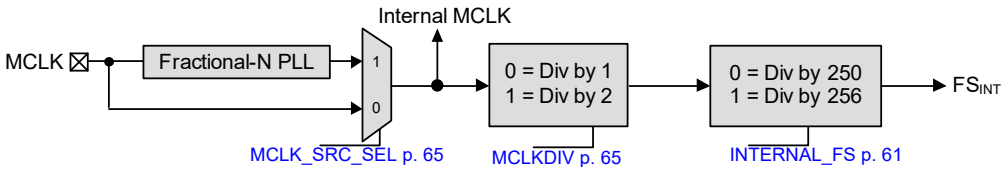


Figure 4-12. MCLK INT Source Switching

For proper internal Fs clocking, the INTERNAL_FS and MCLKDIV bits must be configured, as shown in Table 4-2.

Table 4-3. Determining Fs_{INT}

$MCLK_{INT}$ (MHz)	MCLKDIV (see p. 65)	INTERNAL_FS (see p. 61)	Resulting Fs_{INT} (kHz)
11.2896	0	1	44.1
12	0	0	48
12.288	0	1	48
22.5792	1	1	44.1
24	1	0	48
24.576	1	1	48

Note: The control-port frequency is equal to the $MCLK_{INT}$ frequency.

4.4.3 Fractional-N PLL

The CS43L36 has an integrated fractional-N PLL to support the clocking requirements of the internal analog circuits and converters. This PLL can be enabled or bypassed to suit system-clocking needs. The input reference clock for the PLL is the ASP_SCLK input pin. The reference clock frequency must be between 2.8224 and 25 MHz.

The PLL can be configured for a wide range of combinations of SCLK and $MCLK_{INT}$. PLL_REF_INV (see p. 67) can be used to invert the PLL reference clock. Table 4-4 lists common settings.

Table 4-4. Common PLL Setting Examples

SCLK (MHz)	MCLK_SRC_SEL (see p. 65) [1]	SCLK_PREDIV (see p. 67) [2]	PLL_DIV_INT (see p. 73)	PLL_DIV_FRAC (see p. 73) [2]	PLL_MODE (see p. 73)	PLL_DIVOUT (see p. 73) [3]	$MCLK_{INT}$ (MHz)	PLL_CAL_RATIO (see p. 73)	*n* [4]
1.024	1	00	0xAC	0x44 0000	01	0x10	11.2896	118	3
	1	00	0xBB	0x80 0000	11	0x10	12	125	3
	1	00	0xC0	0x00 0000	11	0x10	12.288	128	3
1.536	1	00	0x72	0xD8 0000	01	0x10	11.2896	118	2
	1	00	0x7D	0x00 0000	11	0x10	12	125	2
	1	00	0x80	0x00 0000	11	0x10	12.288	128	2
	1	00	0x7D	0x00 0000	11	0x08	24	125	4
	1	00	0x80	0x00 0000	11	0x08	24.576	128	4
2.048	1	00	0x56	0x22 0000	01	0x10	11.2896	88	2
	1	00	0x5D	0xC0 0000	11	0x10	12	94	2
	1	00	0x60	0x00 0000	11	0x10	12.288	96	2
2.8224	1	00	0x40	0x00 0000	11	0x10	11.2896	128	1
	1	00	0x40	0x00 0000	11	0x08	22.5792	128	2
3	1	00	0x3C	0x36 1134	11	0x10	11.2896	120	1
	1	00	0x40	0x00 0000	11	0x10	12	128	1
	1	00	0x40	0x00 0000	01	0x10	12.288	131	1
	1	00	0x40	0x00 0000	11	0x08	24	128	2
	1	00	0x40	0x00 0000	01	0x08	24.576	131	2
3.072	1	00	0x39	0x6C 0000	01	0x10	11.2896	118	1
	1	00	0x3E	0x80 0000	11	0x10	12	125	1
	1	00	0x40	0x00 0000	11	0x10	12.288	128	1
	1	00	0x3E	0x80 0000	11	0x08	24	125	2
	1	00	0x40	0x00 0000	11	0x08	24.576	128	2

Table 4-4. Common PLL Setting Examples *(Cont.)*

SCLK (MHz)	MCLK_SRC_SEL (see p. 65) [1]	SCLK_PREDIV (see p. 67) [2]	PLL_DIV_INT (see p. 73)	PLL_DIV_FRAC (see p. 73) [2]	PLL_MODE (see p. 73)	PLL_DIVOUT (see p. 73) [3]	$MCLK_{INT}$ (MHz)	PLL_CAL_RATIO (see p. 73)	*n* [4]
4.00	1	00	0x2D	0x28 8CE7	11	0x10	11.2896	90	1
	1	00	0x30	0x00 0000	11	0x10	12	96	1
	1	00	0x30	0x00 0000	01	0x10	12.288	98	1
4.096	1	00	0x2B	0x11 0000	01	0x10	11.2896	88	1
	1	00	0x2E	0xE0 0000	11	0x10	12	94	1
	1	00	0x30	0x00 0000	11	0x10	12.288	96	1
5.6448	1	01	0x40	0x00 0000	11	0x10	11.2896	128	1
	1	01	0x40	0x00 0000	11	0x08	22.5792	128	2
6	1	01	0x3C	0x36 1134	11	0x10	11.2896	120	1
	1	01	0x40	0x00 0000	11	0x10	12	128	1
	1	01	0x40	0x00 0000	01	0x10	12.288	131	1
	1	01	0x40	0x00 0000	11	0x08	24	128	2
	1	01	0x40	0x00 0000	01	0x08	24.576	131	2
6.144	1	01	0x39	0x6C 0000	01	0x10	11.2896	118	1
	1	01	0x3E	0x80 0000	11	0x10	12	125	1
	1	01	0x40	0x00 0000	11	0x10	12.288	128	1
	1	01	0x3E	0x80 0000	11	0x08	24	125	2
	1	01	0x40	0x00 0000	11	0x08	24.576	128	2
9.6	1	10	0x49	0x80 0000	01	0x10	11.2896	150	1
	1	10	0x50	0x00 0000	11	0x10	12	80	2
	1	10	0x50	0x00 0000	01	0x10	12.288	82	2
	1	10	0x49	0x80 0000	01	0x08	22.5792	150	2
	1	10	0x50	0x00 0000	11	0x08	24	107	3
	1	10	0x50	0x00 0000	01	0x08	24.576	109	3
11.2896	0	—	—	—	—	—	11.2896	—	—
	1	10	0x40	0x00 0000	11	0x08	22.5792	128	2
12	1	10	0x3C	0x36 1134	11	0x10	11.2896	120	1
	0	—	—	—	—	—	12.0000	—	—
	1	10	0x40	0x00 0000	01	0x10	12.288	131	1
	1	10	0x40	0x00 0000	11	0x08	24	128	2
	1	10	0x40	0x00 0000	01	0x08	24.576	131	2
12.2880	1	10	0x39	0x6C 0000	01	0x10	11.2896	118	1
	1	10	0x3E	0x80 0000	11	0x10	12	125	1
	0	—	—	—	—	—	12.2880	—	—
	1	10	0x3E	0x80 0000	11	0x08	24	125	2
	1	10	0x40	0x00 0000	11	0x08	24.576	128	2
13	1	10	0x39	0xAB 52B5	01	0x11	11.2896	111	1
	1	10	0x3B	0x13 B13B	11	0x10	12	118	1
	1	10	0x3B	0x13 B13B	01	0x10	12.288	121	1
19.2	1	11	0x49	0x80 0000	01	0x10	11.2896	150	1
	1	11	0x50	0x00 0000	11	0x10	12	80	2
	1	11	0x50	0x00 0000	01	0x10	12.288	82	2
	1	11	0x49	0x80 0000	01	0x08	22.5792	150	2
	1	11	0x50	0x00 0000	11	0x08	24	107	3
	1	11	0x50	0x00 0000	01	0x08	24.576	109	3
22.5792	1	11	0x40	0x00 0000	11	0x10	11.2896	128	1
	0	—	—	—	—	—	22.5792	—	—
24	1	11	0x3C	0x36 1134	11	0x10	11.2896	120	1
	1	11	0x40	0x00 0000	11	0x10	12	128	1
	1	11	0x40	0x00 0000	01	0x10	12.288	131	1
	0	—	—	—	—	—	24	—	—
	1	11	0x40	0x00 0000	01	0x08	24.576	131	2
24.576	1	11	0x39	0x6C 0000	01	0x10	11.2896	118	1
	1	11	0x3E	0x80 0000	11	0x10	12	125	1
	1	11	0x40	0x00 0000	11	0x10	12.288	128	1
	1	11	0x3E	0x80 0000	11	0x08	24	125	2
	0	—	—	—	—	—	24.576	—	—

Table 4-4. Common PLL Setting Examples *(Cont.)*

SCLK (MHz)	MCLK_SRC_SEL (see p. 65) [1]	SCLK_PREDIV (see p. 67) [2]	PLL_DIV_INT (see p. 73)	PLL_DIV_FRAC (see p. 73) [2]	PLL_MODE (see p. 73)	PLL_DIVOUT (see p. 73) [3]	$MCLK_{INT}$ (MHz)	PLL_CAL_RATIO (see p. 73)	*n* [4]
26	1	11	0x39	0xAB 52B5	01	0x11	11.2896	111	1
	1	11	0x3B	0x13 B13B	11	0x10	12	118	1
	1	11	0x3B	0x13 B13B	01	0x10	12.288	121	1

1. If MCLK_SRC_SEL = 0, the PLL is bypassed and can be powered down by clearing PLL_START (see p. 72).
2. Refer to the register description for the decode.
3. The text following this table explains the use of PLL_DIVOUT, shown by the example configurations in Section 4.4.3.1 and Section 4.4.3.2.
4. The variable *n* represents the divide ratio. See Eq. 4-2.

Powering up the PLL can be accomplished in several configurations. Table 4-4 shows example configurations; the sequences in Section 4.4.3.1 and Section 4.4.3.2 can be used as models.

$MCLK_{INT}$ combinations not shown in Table 4-4 can be determined by Eq. 4-1:

Equation 4-1. Configuring SCLK, $MCLK_{INT}$ Configurations

$$MCLK_{INT} = \frac{SCLK}{SCLK\_PREDIV} \times \frac{(PLL\_DIV\_INT + PLL\_DIV\_FRAC)}{(500/512 \text{ or } 1029/1024 \text{ or } 1)} \times \frac{1}{PLL\_DIVOUT}$$

The internal PLL output must be between ~150 and ~300 MHz. The PLL_DIVOUT value must be an even integer. To maximize flexibility in sample-rate choice, $MCLK_{INT}$ must be nominally 12 or 24 MHz.

PLL_CAL_RATIO determines the operating point for the internal VCO. For most configurations, the default value gives proper performance. However, to keep the VCO within range, some scenarios require PLL_CAL_RATIO to be set during the PLL power-up sequence (see Section 4.4.3). Use Eq. 4-2 to calculate the proper VCO setting at PLL start-up:

Equation 4-2. Calculating the PLL_CAL_RATIO

$$PLL\_CAL\_RATIO = \frac{MCLKINT \times 32 \times SCLK\_PREDIV}{n \times SCLK}$$

The value of *n* in Eq. 4-2 is determined by the following:

- If the result is less than or equal to 151, by default, *n* equals 1.
- If the result is less than 151, use the result to determine the PLL_CAL_RATIO setting.
- If the result is greater than 151, select another divide factor of *n* configurations for SCLK (where *n* = 2,3, …). The result must be between 50 and 151 (see the power-up sequence in Section 4.4.3.2). Use the same *n* value to multiply PLL_DIVOUT during the power-up sequence; see Step 2 in Section 4.4.3.1. The functional value must be restored (Step 8). The same is shown in both standard examples.

4.4.3.1 PLL Power-Up Sequence (Example: SCLK = 4.096 MHz and MCLKINT = 12.288 MHz)

In this example, SCLK = 4.096 MHz and MCLKINT = 12.288 MHz.

1. Set SCLK_PREDIV to Divide-by-1 Mode (0x00).
2. Set PLL_DIVOUT to Divide-by-16 Mode (0x10). This reflects a value of *n* = 1, because the PLL_CAL_RATIO generated by Eq. 4-2 equals 96. See that the PLL_DIVOUT entry for this configuration in Table 4-4 used a Divide-by-16 Mode (0x10).
3. Clear the three fractional factor registers, PLL_DIV_FRAC (see Section 7.5.2).
4. Set the integer factor, PLL_DIV_INT to 48 (0x30).
5. Set the PLL Mode multipliers, PLL_MODE to 11 to bypass both 500/512 and 1029/1024 factors (0x03).
6. Set the PLL_CAL_RATIO to 96 (0x60, see Section 7.5.5).
7. Turn on the PLL by setting PLL_START (see p. 72).
8. As part of a standard sequence, after at least 800 µs, the PLL_DIVOUT value would need to restored to 16 (0x10), which is unnecessary here because that value did not change.

4.4.3.2 PLL Power-Up Sequence (Example: SCLK = 12 MHz and MCLKINT = 24 MHz)

In this example, SCLK = 12 MHz and $MCLK_{INT}$ = 24 MHz.

1. Set SCLK_PREDIV to Divide-by-4 Mode (0x02).
2. Set PLL_DIVOUT to Divide-by-16 Mode (0x10). This reflects a value of *n* = 2, because the PLL_CAL_RATIO generated by Eq. 4-2 was greater than 151. See that the PLL_DIVOUT entry for this configuration in Table 4-4 used a Divide-by-8 Mode (0x08).
3. Clear the three fractional factor registers, PLL_DIV_FRAC.
4. Set the integer factor, PLL_DIV_INT to 64 (0x40).
5. Set the PLL mode multipliers, PLL_MODE to 11 to bypass both 500/512 and 1029/1024 factors (0x03).
6. Set the PLL_CAL_RATIO to 128 (0x80).
7. Turn on the PLL by setting PLL_START.
8. After at least 800 µs, the PLL_DIVOUT value must be restored from 16 to 8 (0x08).

4.4.3.3 Nonstandard PLL Setting (Example: SCLK = 19.2 MHz and MCLKINT = 12 MHz)

In this example, SCLK = 19.2 MHz and $MCLK_{INT}$ = 12 MHz. (Note that a power-up sequence similar to Section 4.4.3.2 is required for this configuration due to *n* = 1.)

- SCLK = 19.2 MHz = available reference clock.
- $MCLK_{INT}$ = 12 MHz = desired internal MCLK.
- SCLK_PREDIV = 11 = divide SCLK by 8 as reference to PLL.
- PLL_DIV_INT = 0x50 = multiply reference clock by 80, yielding PLL out = 192 MHz.
- PLL_DIV_FRAC = 0x00 0000 = fractional portion equal to zero.
- PLL_MODE = 11 = 500/512 and 1029/1024 multipliers are bypassed.
- PLL_DIVOUT = 0x10 = divide PLL out by 16 to achieve $MCLK_{INT}$ of 12 MHz.

Table 4-5 shows nonstandard PLL configurations.

Table 4-5. Nonstandard PLL Settings

SCLK (MHz)	MCLK_SRC_SEL (see p. 65)	SCLK_PREDIV (see p. 67)	PLL_DIV_INT (see p. 73)	PLL_DIV_FRAC (see p. 73)	PLL_MODE (see p. 73)	PLL_DIVOUT (see p. 73)	$MCLK_{INT}$ (MHz)	PLL_CAL_RATIO (see p. 73)	*n* [1]
9.6	1	10	0x6E	0x40 0000	01	0x18	11.2896	75	1
	1	10	0x50	0x00 0000	11	0x10	12	80	1
	1	10	0x50	0x00 0000	01	0x10	12.288	82	1
	1	10	0x6E	0x400000	01	0x0C	22.5792	150	1
	1	10	0x50	0x00 0000	11	0x08	24	80	2
	1	10	0x50	0x00 0000	01	0x08	24.576	82	2
19.2	1	11	0x6E	0x40 0000	01	0x18	11.2896	150	1
	1	11	0x50	0x00 0000	11	0x10	12	80	2
	1	11	0x50	0x00 0000	01	0x10	12.288	82	2
	1	11	0x6E	0x40 0000	01	0x0C	22.5792	150	2
	1	11	0x50	0x00 0000	11	0x08	24	107	3
	1	11	0x50	0x00 0000	01	0x08	24.576	109	3

1. The variable *n* represents the divide ratio. See Eq. 4-2.

As shown in Fig. 4-13, the input to the PLL is the ASP_SCLK input pin.

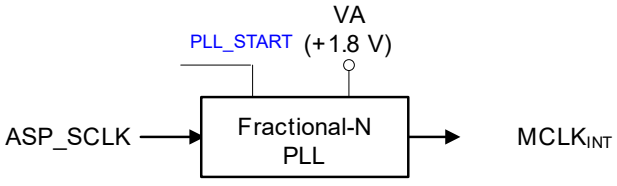


Figure 4-13. Clocking Architecture

4.4.3.4 Powering Down the PLL

To power down the PLL, clear PLL_START.

4.5 Audio Serial Port (ASP)

The CS43L36 has an ASP to communicate audio and voice data between system devices, such as application processors and Bluetooth® transceivers. ASP_SCLK_EN (see p. 66) must be set whenever DAI is used. The ASP can be configured to TDM, I²S, and left justified (LJ) audio interfaces.

Note: A maximum of two input channels are supported in TDM Mode.

4.5.1 Slave Mode Timing

The ASP can operate as a slave to another device's timing, requiring ASP_SCLK and ASP_LRCK/FSYNC to be mastered by the external device. If ASP_HYBRID_MODE is cleared (see p. 66), the serial port acts as a slave. If ASP_HYBRID_MODE is set, the port is in Hybrid-Master Mode (see Section 4.5.2).

In Slave Mode, ASP_SCLK and ASP_LRCK are inputs. Although the CS43L36 does not generate interface timings in Slave Mode, the expected LRCK and SCLK format must be programmed as it is in Hybrid-Master Mode. Table 4-8 shows supported serial-port sample rate examples. Note that some rates require use of the PLL and/or SRC.

4.5.2 Hybrid-Master Mode Timing

In Hybrid-Master Mode, ASP_LRCK is derived from ASP_SCLK; the ASP_SCLK/ASP_LRCK ratio must be N x F_S, where N is a large enough integer to support the total number of bits per ASP_LRCK period for the audio stream to be transferred. In either 50/50 Mode or I²S/LJ Mode, the ASP_SCLK/ASP_LRCK ratio must be N_E x F_S, where N_E is an even integer.

The serial port generates an internal LRCK/FSYNC from an externally mastered ASP_SCLK, allowing single clock-source mastering to the CS43L36. In Hybrid-Master Mode, the serial port must provide a left-right/frame sync signal (ASP_LRCK/FSYNC) given an externally generated bit clock (ASP_SCLK).

Table 4-6 shows supported serial-port sample-rate examples. Other rates are possible, but the rules stipulated above must be met. Note that some rates require use of the PLL or SRC.

Table 4-6. Supported Serial-Port Sample Rates

SCLK Frequency (MHz)	Serial Port Sample Rate (kHz)																	
	8.0	11.025	11.029	12	16	22.05	22.059	24	32	44.1	44.118	48	88.2	88.235	96	176.4	176.471	192
1.4112	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
2.8224	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
5.6448	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
11.2896	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
22.5792	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
1.024	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
2.048	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
4.096	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
8.192	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
2	x	—	—	—	x	—	—	—	—	—	—	—	—	—	—	—	—	—
3	x	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x	—
4	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
6	x	—	x	x	x	—	x	x	—	—	x	x	—	x	—	—	x	—
12	x	—	x	x	x	—	x	x	x	—	x	x	—	x	x	—	x	—
24	x	—	x	x	x	—	x	x	x	—	x	x	—	x	x	—	x	x
1.536	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
3.072	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
6.144	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
12.288	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
24.576	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
9.6	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
19.2	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x

Fig. 4-14 and Fig. 4-15 show the serial-port clocking architectures.

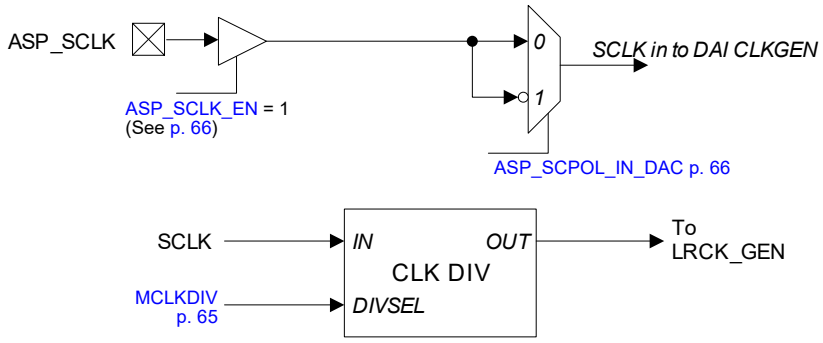


Figure 4-14. ASP SCLK Architecture

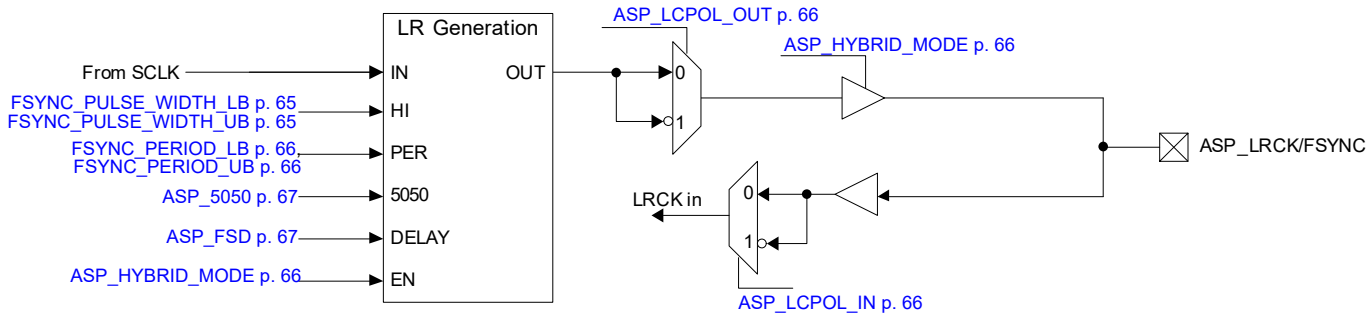


Figure 4-15. ASP LRCK Architecture

As shown in Fig. 4-16, the LRCK period (FSYNC_PERIOD_LB and FSYNC_PERIOD_UB, see p. 66) controls the number of SCLK periods per frame. This effectively sets the frame length and the number of SCLK periods per Fs. Frame length may be programmed in single SCLK period multiples from 16 to 4096 SCLK:Fs. If ASP_HYBRID_MODE (see p. 66) is set, the SCLK period multiples must be set to 2 * *n* * Fs, where $n \in \{8, 9, \ldots, 2048\}$.

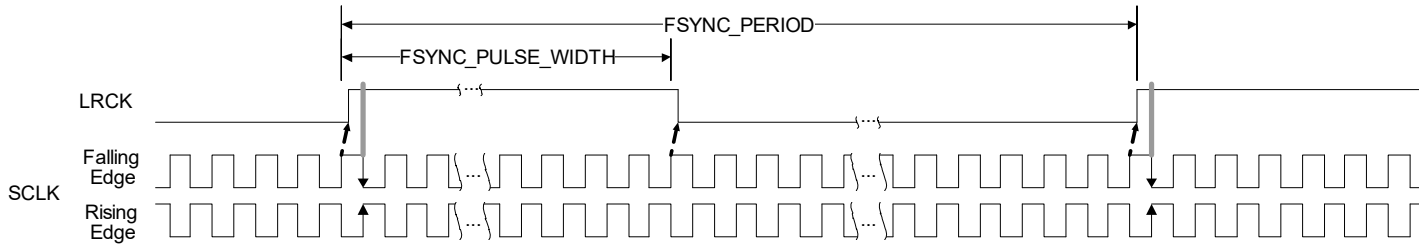


Figure 4-16. ASP LRCK Period, High Width

FSYNC_PULSE_WIDTH_LB and FSYNC_PULSE_WIDTH_UB (see p. 65) control the number of SCLK periods for which the LRCK signal is held high during each frame. Like the LRCK period, the LRCK-high width is programmable in single SCLK periods, from at least one period to at most the LRCK period minus one. That is, the LRCK-high width must be shorter than the LRCK period.

As shown in Fig. 4-17, if 50/50 Mode is enabled (ASP_5050 = 1, see p. 67), the LRCK high duration must be programmed to the LRCK period divided by two (rounded down to the nearest integer when the LRCK period is odd). When the serial port is in 50/50 Mode, setting the LRCK high duration to a value other than half of the period causes erroneous operation.

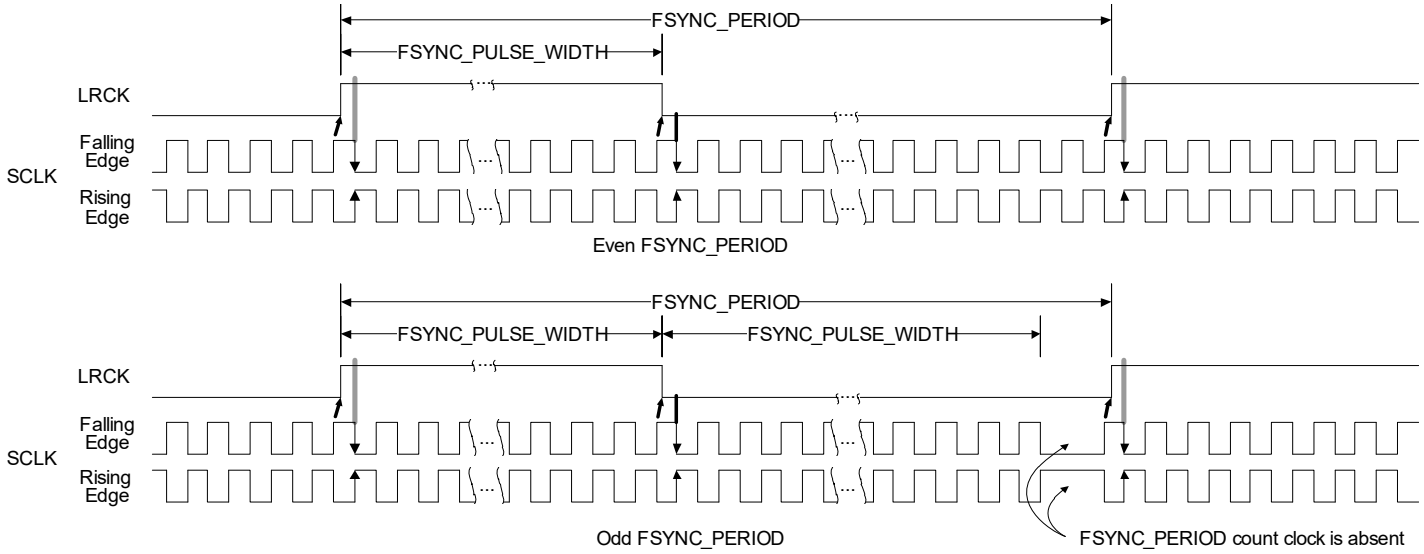


Figure 4-17. ASP LRCK Period, High Width, 50/50 Mode

Fig. 4-18 shows how LRCK frame start delay (ASP_FSD, see p. 67) controls the number of SCLK periods from LRCK synchronization edge to the start of frame data.

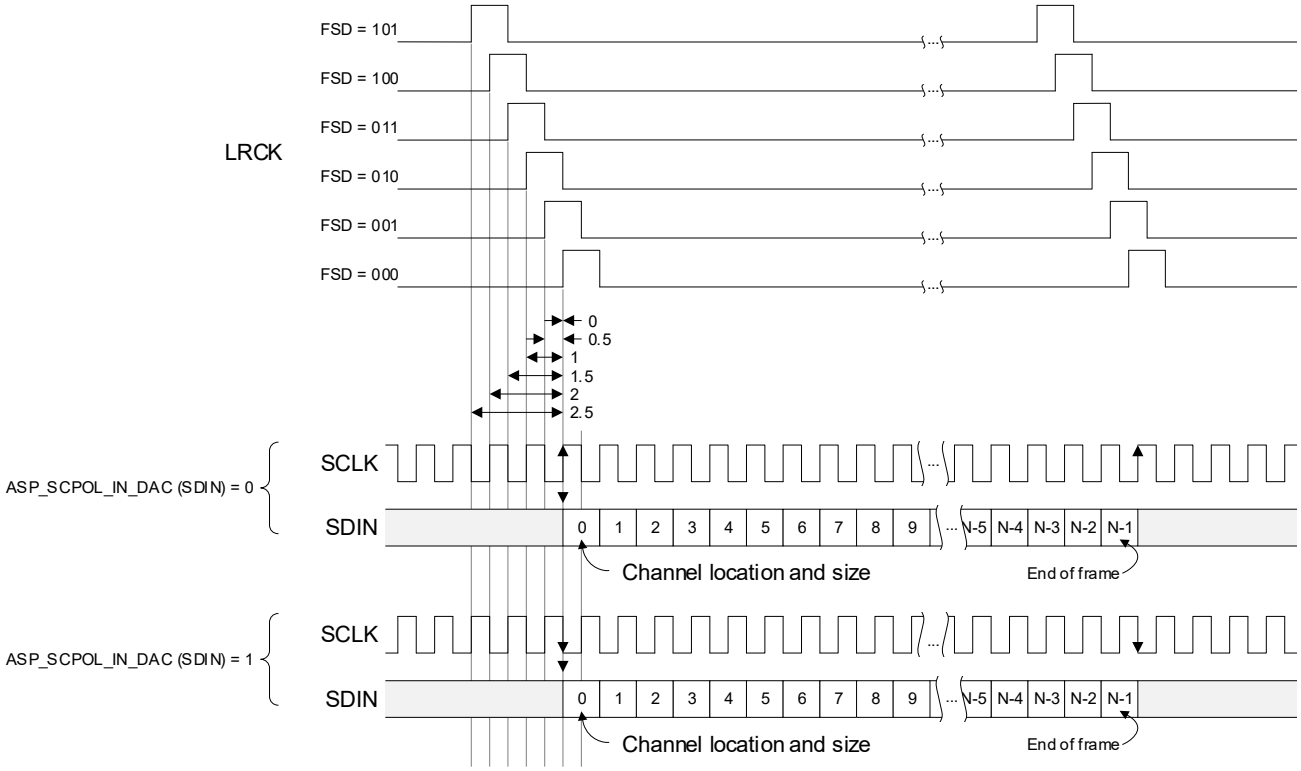


Figure 4-18. LRCK FSD and SCLK Polarity Example Diagram

4.5.3 Channel Location and Resolution

Each serial-port channel's location and offset is configured through the registers in Table 4-7. Location is programmable in single SCLK-period resolution. If set to the minimum location offset, a channel sends or receives on the first SCLK period of a new frame. Channel size is programmable in 8- to 32-bit byte resolutions. DAC ports are limited to 24 bits and truncate the 8 LSBs of a 32-bit audio stream.

Table 4-7. ASP Channel Controls

Channel	Resolution	MSB Location	LSB Location
ASP Receive DAI0 Channel 1	ASP_RX0_CH1_RES	ASP_RX0_CH1_BIT_ST_MSB	ASP_RX0_CH1_BIT_ST_LSB
ASP Receive DAI0 Channel 2	ASP_RX0_CH2_RES	ASP_RX0_CH2_BIT_ST_MSB	ASP_RX0_CH2_BIT_ST_LSB

Channel size and location must not be programmed such that channel data exceeds the frame boundary. In other words, channel size and offset must not exceed the expected SCLK per LRCK settings. Size and location must not be programmed such that data from a given SCLK period is assigned to more than one channel. However, an exception exists for the DAI as the same data can be used for both received channels' location, if desired. For an example, see Section 5.1.

Fig. 4-19 shows channel location and size. See ASP_RX0_2FS (p. 79).

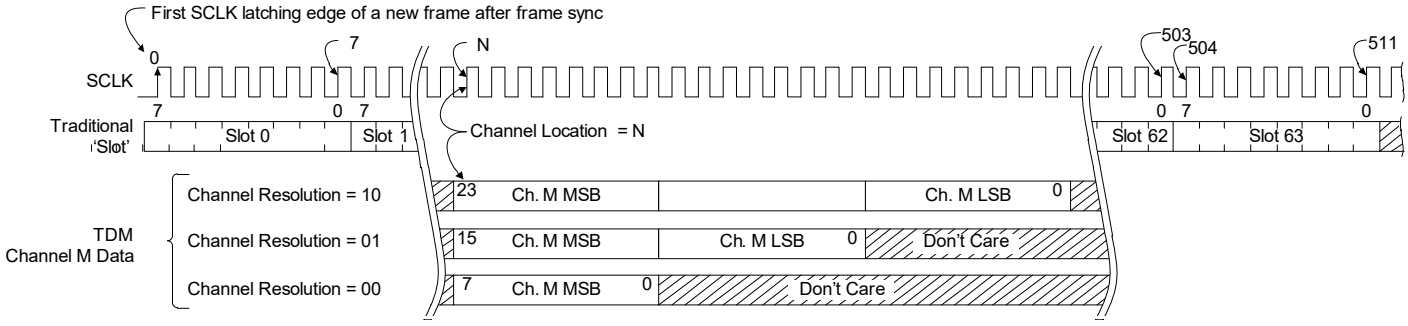


Figure 4-19. Example Channel Location and Size

4.5.4 Isochronous Serial-Port Operation

In Isochronous Mode, audio data can be transferred between the internal audio data paths and a serial port at isochronous frequencies slower than the LRCK frequency. In all cases, the sample rate/LRCK frequency ratio must be one for which there are points at which rising edges regularly align.

Notes: Combining an isochronous audio stream on a channel (or on multiple channels) concurrently with a native audio stream on another channel (or other multiple channels) is not supported.

In Isochronous Mode, if a stream's sample rate does not match the LRCK frequency, it must include nulls, indicated by the negative full-scale (NFS) code (1 followed by 0s) or by adding nonaudio bits (NSB Mode) to the data stream.

SP_RX_NFS_NSBB (see p. 78) selects between the NFS and NSB modes.In NFS Mode, to achieve a desired isochronous output sample rate, a null-insert block adds NFS samples to the output stream. NFS samples input to the null-insert block are incremented and are passed to the output as valid, nonnull samples.

In NSB Mode, a null-insert block adds 8 bits to the data stream and inserts null samples to achieve a desired isochronous output sample rate. Inserted null samples are defined as NFS including the nonaudio bits. NFS samples that are input to the null-insert block are passed as valid, nonnull samples to the output. Valid samples are indicated by a nonzero value in the null sample indicator bit. The null sample indicator bit is globally defined by the SP_RX_NSB_POS (see p. 78). Total data stream sample width, including the nonaudio bits, is N + 8 bits. Therefore, the maximum HD audio sample width is 24 bits in NSB Mode.

In NFS Mode, a null-remove block deletes null samples, restoring the stream's original sample rate. NFS samples that are input to the null-remove block are removed from the data stream as invalid, null samples.

In NSB Mode, a null-remove block deletes samples that have a zero null sample indicator bit, restoring the stream's original sample rate. Furthermore, the output data has the least-significant 8 bits of nonaudio data removed. Samples with a zero null sample indicator bit are removed from the data stream as invalid, null samples.

In either NSB or NFS Mode, setting the Rx rate fields (SP_RX_FS, see p. 79) matters only if an isochronous mode is selected via SP_RX_ISOC_MODE (see p. 78). Supported isochronous rates are 48k, 96k, and 192k. The ASPx Rx rate bits are used only to help determine when to remove nulls and to provide the correct f_{SI}/f_{SO} to the SRCs while in Isochronous Mode.

For null-remove operations, the rates do not need to match the actual data rate. Likewise, if data is being or captured at its native rate, these registers have no effect.

As Fig. 4-20 shows, the null-sample bit (NSB) flag may be any bit of the least-significant sample byte. NSB-encoded streams are assumed to contain 8 bits of nonaudio data as the LSB.

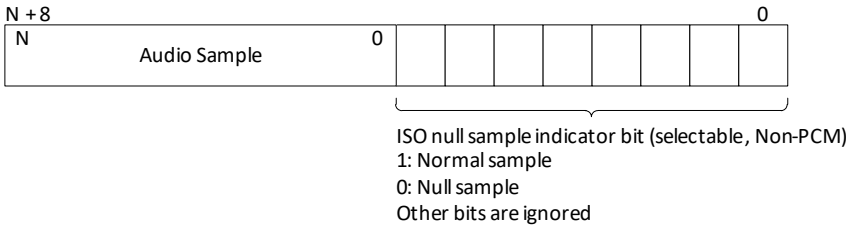


Figure 4-20. NSB Null Encoding

To send isochronous audio data to a serial port, the data pattern must be such that the LRCK/FSYNC transition preceding any given nonnull sample on the 48-kHz serial port does not deviate by more than one sample period from a virtual clock running at the desired sample rate. Use the following example to determine the data word as it appears on the serial port.

```
error = 0
for each LRCK
   if(error < 1/FLRCK)
     output = <<next sample>>
     error = error + (1/Fs - 1/FLRCK)
   else
     output = NULL
     error = error - 1/FLRCK
```

The null-sample sequences in Table 4-8 result from the example above for common sample rates. This method ensures that the internal receive data FIFO does not underrun or overrun, which would cause audio data loss. Depending on the internal audio data FIFOs' startup conditions and on the serial-port clock-phase relationships, isochronous data sent from a serial port may not adhere to the data patterns in Table 4-8. In all cases, the transmitted audio data rate matches the stream sample rate.

Table 4-8. Isochronous Input Data Pattern Examples

Sample Rate (kHz)	Isochronous Data Pattern for LRCK = 48 kHz
8.000	1_S5_N (repeat)
11.025	[[[1s3nx2]1s4n]x5 1s3n1s4n]x4 [[1s3nx2]1s4n]x4 1s3n1s4n [[[1s3nx2]1s4n]x5 1s3n1s4n]x3 [[1s3nx2]1s4n]x4 1s3n1s4n (repeat)
12.000	1_S3_N (repeat)
16.000	1_S2_N (repeat)
22.05	[[1s1nx6]1n [1s1nx6]1n [1s1nx5]1n]x8 [1s1nx6]1n [1s1nx5]1n (repeat)
24.000	1_S1_N (repeat)
32.000	2_S1_N (repeat)
44.100	[12s1n[11s1n]x2]x3 11s1n (repeat)
48.000	1_S (repeat)

Note: $_N$ = Null sample, $_S$ = Normal sample

4.5.5 50/50 Mode

Regardless of the state of ASP_LRCK/FSYNC, in 50/50 Mode (ASP_5050 = 1, see p. 67), the ASP can start a frame.

The ASP_STP setting (see p. 67) determines which LRCK/FSYNC phase starts a frame in 50/50 Mode, as follows:

- If ASP_STP = 0, the frame begins when LRCK/FSYNC transitions from high to low. See Fig. 4-21.

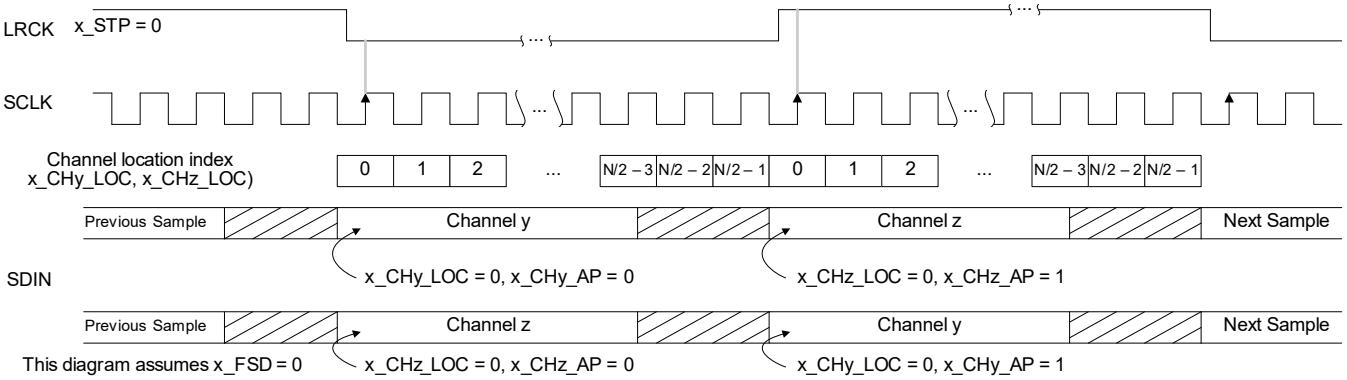


Figure 4-21. Example 50/50 Mode (ASP_STP = 0)

- If ASP_STP = 1, the frame begins when LRCK/FSYNC transitions from low to high. See Fig. 4-22.

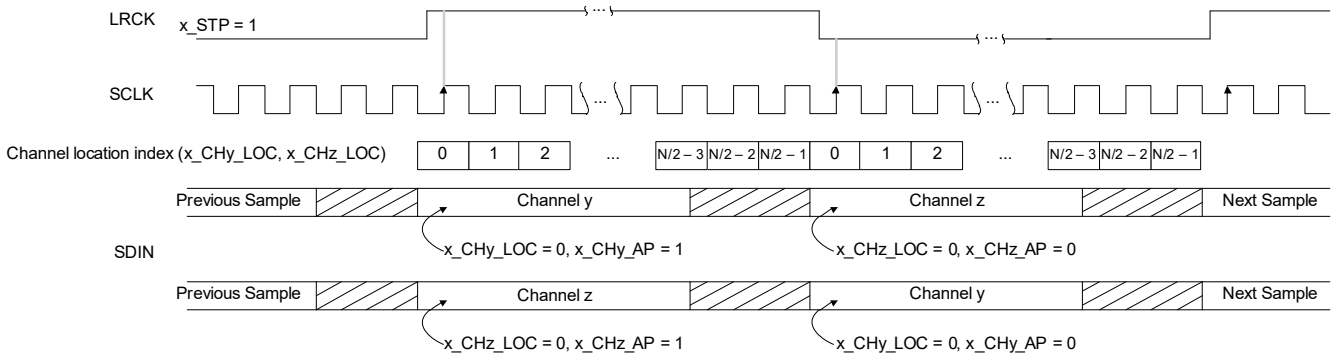


Figure 4-22. Example 50/50 Mode (ASP_STP = 1)

In 50/50 Mode, left and right channels are programmed independently to output when LRCK/FSYNC is high or low—that is, the channel-active phase. The active phase is controlled by ASP_RXx_CHy_AP (see Section 7.14). If x_AP = 1, the respective channel is output if LRCK/FSYNC is high. If x_AP = 0, the channel is output if LRCK/FSYNC is low.

Note: Active phase has no function if 50/50 Mode = 0 or ASP_RX1_2FS = 1.

In 50/50 Mode, the channel location (see Section 4.5.3) is calculated within the channel-active phase. If there are N bits in a frame, the location of the last bit of each active phase is equal to (N/2) – 1.

4.5.6 Serial Port Status

Each serial port has sticky, write-1-to-clear status bits related to capture paths. These bits are described in Section 7.4.3. Mask bits (Section 7.4.12) determine whether $\overline{\text{INT}}$ is asserted when a status bit is set. Table 4-9 provides an overview.

Table 4-9. Serial Port Status

Name	Direction	Description	Register Reference
Request Overload	Rx	Set when too many input buffers request processing at the same time. If all channel registers are properly configured, this error status should never be set.	ASPRX_OVLD p. 68
LRCK Error	Rx	Logical OR of LRCK Early and LRCK Late (see below).	ASPRX_ERROR p. 68
LRCK Early	Rx	Set when the number of SCLK periods per LRCK phase (high or low) is less than the expected count as determined by x_LCPR and x_LCHI. **Note:** The Rx LRCK early interrupt status is set during the first receive LRCK early event. Subsequent receive LRCK early events are indicated only if valid LRCK transitions are detected.	ASPRX_EARLY p. 68
LRCK Late	Rx	Set when the number of SCLK periods per LRCK phase (high or low) is greater than the expected count as determined by x_LCPR and x_LCHI.	ASPRX_LATE p. 68
No LRCK	Rx	**Note:** Set when the number of SCLK periods counted exceeds twice the value of LRCK period (x_LCPR) without an LRCK edge.	ASPRX_NOLRCK p. 68

4.5.7 Recommended Serial-Port Power-Up and Power-Down Strategies

Although multiple safeguards and controls are implemented to prevent a run on the FIFOs involved in passing data from the input port to the output port, the following power-up sequence is recommended. Section 5 gives detailed sequences.

1. Configure all playback channel characteristics—bit resolution, channel select, source (DAI), native/isochronous, sample rates, etc.
2. Power up playback, and ASRCs.
3. Release the PDN_ALL bit.
4. Power up the serial ports (DAI).

The following power-down sequence is recommended:

1. Power down the playback path.
2. Power down the serial ports.

4.6 Sample-Rate Converters (SRCs)

SRCs bridge different sample rates at the serial ports within the digital-processing core. SRCs are used for the following:

- Two ASP input channels (Channels 1 and 2).
- SRCs are bypassable by setting SRC_BYPASS_DAC (see p. 61).

An SRC's digital-processing side (as opposed to its serial-port side) connects to the DAC. Multirate DSP techniques are used to up-sample incoming data to a very high rate and then down-sample to the outgoing rate. Internal filtering is designed so that a full-input audio bandwidth of 20 kHz is preserved if the input and output sample rates are at least 44.1 kHz. If the output sample rate becomes less than the input sample rate, the input is automatically band limited to avoid aliasing artifacts in the output signal.

The following restrictions must be met:

- The F_{so}-to-F_{SI} ratio must be no more than 1:6 or 6:1. For example, if the DAC is at 48 kHz, the input to the SRC must be at least 8 kHz.
- SRC operation cannot be changed on-the-fly. Before changing the SRC operation (e.g., changing SRC frequencies or bypassing or adding the SRCs), the user must follow the power sequences provided in Section 4.5.7.
- The MCLK frequency must be as close as possible to, but not less than the minimum SRC MCLK frequency, $MCLK_{MIN}$, which must be at least 125 times the higher of the two sample rates (F_{SI} or F_{so}).

  For example, if F_{so} is 48 kHz and F_{SI} is 32 kHz, the MCLK must be as close as possible to, but not less than, an $MCLK_{MIN}$ of 6.0 MHz. The MCLK frequency for the SRCs is configured through CLK_IASRC_SEL (see p. 67).

Table 4-10 shows settings for the supported sample rates and corresponding $MCLK_{INT}$ frequencies.

Table 4-10. Supported Sample Rates and Corresponding $MCLK_{INT}$ Encodings

Fsint (kHz)	Serial Port Sample Rate (kHz)																	
	8.0	11.025	11.029	12	16	22.05	22.059	24	32	44.1	44.118	48	88.2	88.235	96	176.4	176.471	192
44.1	00	00	00	00	00	00	00	00	00	00	00	00	01	01	01	10	10	10
48	00	00	00	00	00	00	00	00	00	00	00	00	01	01	01	10	10	10

Note: SRC MCLKINT Freq= 00 (6 MHz), 01 (12 MHz), 11 (24 MHz), configured in CLK_IASRC_SEL (see p. 67)

Jitter in the incoming signal has little effect on rate-converter dynamic performance. It does not affect the output clock.

A digital PLL continually measures the heavily low-pass-filtered phase difference and the frequency ratio between input and output sample rate clocks. It uses the data to dynamically adjust coefficients of a linear time-varying filter that processes a synchronously oversampled version of the input data. The filter output is resampled to the output sample rate.

For input serial ports, input and output sample-rate clocks are respectively derived from the external serial-port sample clock (x_LRCK) and the internal Fs clock. FS_EN (see p. 67) must be set according to the F_{SI} or F_{so} SRC sample rates.

Minimize the SRCs' lock time by programming the serial-port interface sample rates into the x_FS registers (see Section 7.13.1). If the rates are unknown, programming these registers to "don't know" would likely increase lock times. Proper operation is not assured if sample rates are misprogrammed.

4.7 Headset Interface

Split digital-power domains (VD_FILT and VP) within the headset interface support an ultralow-power standby mode where only the VP supply is used. An output signal may be used to tell the system to wake from its low-power state when a headset plug is inserted or removed. The interface may be reset by three types of resets with progressively less effect.

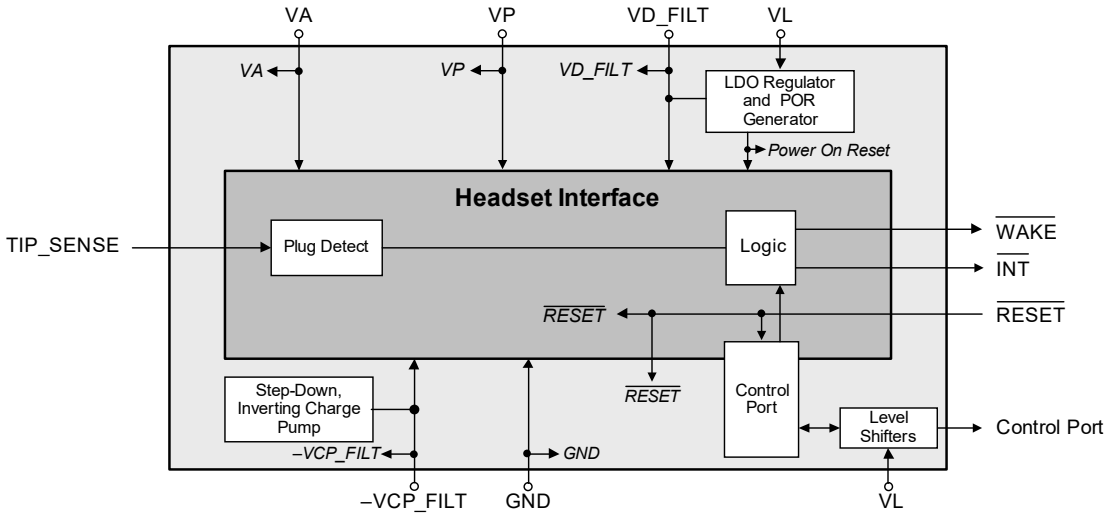


Figure 4-23. Headset Interface Block Diagram

The control port includes registers that source individually maskable interrupts. Event-change debouncing is used to filter applicable status registers. Latchable duplicate registers are used to pass information to the Standby Mode supply domain.

4.8 Plug Presence Detect

The CS43L36 uses TIP_SENSE to detect plug presence. The sense pin is debounced to filter out brief events before being reported to the corresponding presence-detect bit and generating an interrupt if appropriate.

4.8.1 Plug Types

The CS43L36 supports the following industry-standard plug types:

- Tip–Ring–Sleeve (TRS)—Consists of a segmented metal barrel with the tip connector used for HPOUTA, a ring connector used for HPOUTB, and a sleeve connector used for HSGND.
- Tip–Ring–Ring–Sleeve (TRRS)—Like TRS, with an additional ring connector for the mic connection. There are two common pinouts for TRRS plugs:
  - — One uses the tip for HPOUTA, the first ring for HPOUTB, the second ring for HSGND, and the sleeve for mic.
  - — The CS43L36 does not support OMTP, or China, headset, which swaps the third and fourth connections, so that the second ring carries mic and the sleeve carries HSGND.

4.8.2 Tip-Sense Methods

The following methods are used to detect the presence or absence of a plug:

- Tip sense (TS)—A sense pin is connected to a terminal on the receptacle such that, if no plug is inserted, the pin is floating. If a plug is inserted, the pin is shorted to the tip (T) terminal. The tip is sensed by having a small current source in the device pull up the pin if it is left floating (no plug). If a plug is inserted and the sense pin is shorted to HPOUTA, the sense

pin is assumed to be pulled low via clamps at the HP amp output when it is in power down. If the HP amp is running, the sense pin is shorted to the output signal and, therefore, is pulled below a certain threshold via the output stage of the HP amp. Thus, a low level at the sense pin indicates plug inserted, and a high level at the sense pin indicates plug removed.

- Inverted tip sense (ITS)—Like tip sense, but with a connector whose sense pin is shorted to the tip terminal if the plug is removed and is left floating if it is inserted. Therefore, a low level at the sense pin indicates plug removed and a high level at the sense pin indicates plug inserted. Inversion is controlled by the following:
  - The invert (TIP_SENSE_INV, p. 75), which goes to the analog and affects a number of other features.
  - The tip-sense invert (TS_INV, p. 64), which affects only the configuration bits in Section 6.2.

4.8.3 Tip-Sense Debounce Settings

Fig. 4-24 shows the tip-sense controls and the associated interrupt, status, and mask registers.

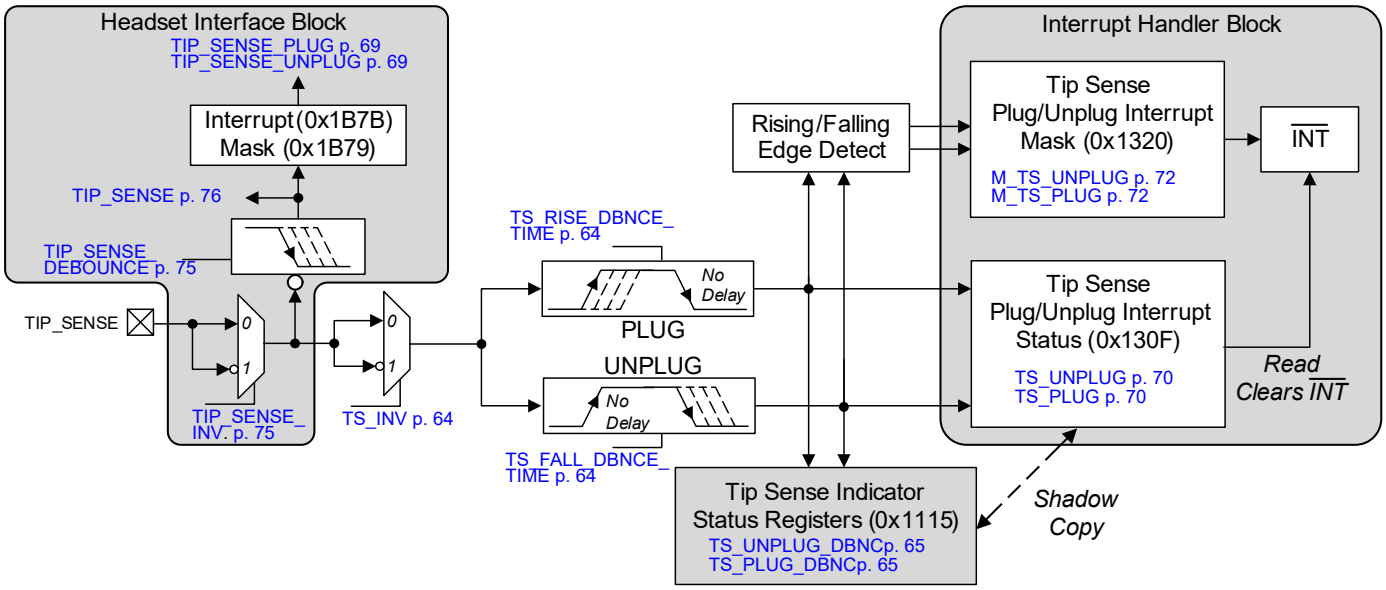


Figure 4-24. Tip-Sense Controls

The tip-sense debounce register fields behave and interact as follows:

- TS_UNPLUG_DBNC. Shows tip sense status after being unplugged with the associated debounce time.
- TS_PLUG_DBNC. Shows tip sense status after being plugged in with the associated debounce time.

Note: TS_INV must be set to have TS_PLUG/TS_PLUG_DBNC status match TIP_SENSE_PLUG status.

The debounce bits are described in Section 7.2.7. Multiple debounce settings can be configured for insertion, removal, and tip sense:

- TIP_SENSE_DEBOUNCE (see p. 75) controls the tip-sense removal debounce time.
- TS_FALL_DBNCE_TIME and TS_RISE_DBNCE_TIME (see p. 64) settings configure the corresponding debounce times.

4.8.4 Setup Instructions

The following steps are required to activate the tip-sense debounce interrupt status:

1. Clear PDN_ALL (see p. 63).
2. Set LATCH_TO_VP (see p. 75) to latch analog controls into analog circuits.
3. Write TIP_SENSE_CTRL (see p. 75) to 01 or 11 to enable debounce for tip sense plug/unplug.
4. Clear interrupt masks (0x1320, see Section 7.4.17).

Interrupt status (see Section 7.4.9) does not contain an event-capture latch—a read always yields the current condition.

Table 4-11 describes the plug/unplug status.

Table 4-11. Tip Plug/Unplug Status

Plug Status	Unplug Status	Interpretation
0	0	Tip is fully unplugged/not present
1	0	Reserved
0	1	Tip connection is in a transitional state
1	1	Tip is fully plugged/present

4.9 Power-Supply Considerations

Because some power supply combinations can produce unwanted system behavior, note the following:

- Control-port transactions can occur 1 ms after VP, VD_FILT, VCP, and VL exceed the minimum operating voltage.
- If VP supply is off, it is recommended that all other supplies are also off. VP must be the first supply turned on.
- $\overline{\text{RESET}}$ must be asserted until VP is valid.
- If VD_FILT is supplied externally ($\overline{\text{DIGLDO\_PDN}}$ = GND), VL must be supplied before VD_FILT, VA, VL, and VCP can come up in any order. Due to the VD_FILT POR, VD_FILT must be turned off before VA, VL, or VCP are turned off; otherwise, current could be drawn from supplies that remain on.

Table 4-12 shows the maximum current for each supply when VP is on, but other supplies are on or off (all clocks are off and all registers are set to default values, i.e., reset).

Table 4-12. Typical Leakage Current during Nonoperational Supply States (with VP Powered On)

Supply			Current (µA)				Notes
VCP	VA	VL	I_{Vp}	I_{VCP}	I_{VA}	I_{VL}	
Off	On	Off	14	0	0	0	VA may source or sink current
Off	On	On	25	0	0	328	VA may source or sink current
On	Off	Off	14	0	0	0	—
On	Off	On	25	0	0	328	—
On	On	Off	14	0	0	0	VA may source or sink current
On	On	On	25	0	0	328	—

Notes:
- Values shown reflect typical voltage and temperature. Leakage current may vary by orders of magnitude across the maximum and minimum recommended operating supply voltages and temperatures listed in Table 3-2.
- Test conditions: Clock/data lines are held low, $\overline{\text{RESET}}$ is held high, and all registers are set to their default values.

Table 4-13 shows requirements and available features for valid power-supply configurations.

Table 4-13. Valid Power-Supply Configurations

Configuration	Notes
On: VP Off: VD_FILT = VCP = VL = VA	Limited set of headset plug-detect and WAKE output features, see Section 4.7 and Section 4.8.
On: VP = VL Off: VD_FILT = VCP = VA = OFF	Limited set of headset plug-detect and WAKE output features, see Section 4.7 and Section 4.8. Digital I/O ESD diodes are powered to prevent conduction in pin-sharing applications.
On: VP = VD_FILT = VCP = VL = VA	Full chip functionality

4.9.1 VP Monitor

The CS43L36 voltage comparator monitors the VP power supply for potential brown-out conditions due to power-supply overload or other fault conditions. To perform according to specifications, VP is expected to remain above 3.0 V at all times. The VP monitor is enabled by setting VPMON_PDNB (see p. 64) and must be powered up after VP is above 3.0 V

to eliminate erroneous faulty condition detection. Fig. 4-25 shows the behavior of the VP monitor.

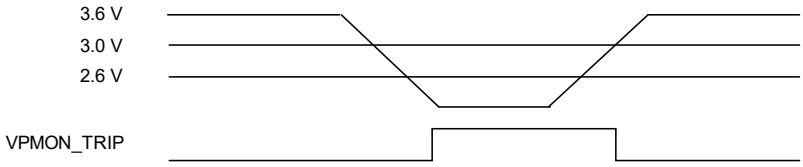


Figure 4-25. VP Monitor

The following describes the VP monitor behavior with respect to the voltage level:

- If VP drops below 3.0 V, TIP_SENSE performance may be compromised.
- If VP drops below 2.6 V, the VPMON_TRIP status bit is set (see p. 69). An interrupt is triggered if M_VPMON_TRIP = 0 (see p. 72). This bit must be unmasked/enabled only if VP is above the detection-voltage threshold. It must be masked/disabled by default to eliminate erroneous interrupts while VP is ramping or is known to be below the threshold voltage.
- A brown-out condition remains until VP returns to a voltage level above 3.0 V.
- The VP monitor circuit becomes unreliable at VP levels below 2.4 V as it may trigger a power-on reset sequence by the device.
- The VP monitor is intended to detect slow transitioning signals about the 2.6-V threshold. Pulses of short duration are filtered by the monitor and may not trigger at the 2.6-V threshold, but at a value much lower than expected.

4.10 Control-Port Operation

Control-port registers are accessed through the I²C interface, allowing the DAC to be configured for the desired operational modes and formats.

4.10.1 I²C Control-Port Operation

The I²C control port can operate completely asynchronously with the audio sample rates. However, to avoid interference problems, the I²C control port pins must remain static if no operation is required.

The control port uses the I²C interface, with the DAC acting as a slave device. The I²C control port can operate in the following modes, which are configured through the I²C debounce register in Section 7.1.9:

- Standard Mode (SM), with a bit rate of up to 100 kbit/s
- Fast Mode (FM), with a bit rate of up to 400 kbit/s
- Fast Mode Plus (FM+), with a bit rate of up to 1 Mbit/s.

Note: ASP_SCLK is not required to be on when the control port is accessed, for state machines affected by register settings to advance.

SDA is a bidirectional data line. Data is clocked into and out of the CS43L36 by the SCL clock. Fig. 4-26–Fig. 4-29 show signal timings for read and write cycles. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other SDA transitions occur while the clock is low.

The register address space is partitioned into 8-bit page spaces that each comprise up to 127 8-bit registers. Address 0x00 of each page is reserved as the page indicator, PAGE. Writing to address 0x00 of any page changes the page pointer to the address written to address 0x00.

To initiate a write to a particular register in the map, the page address, 0x00, must be written following the chip address. Subsequent accesses to register addresses are treated as offsets from the page address written in the initial transaction. To change the page address, initiate a write to address 0x00. To determine which page is active, read address 0x00.

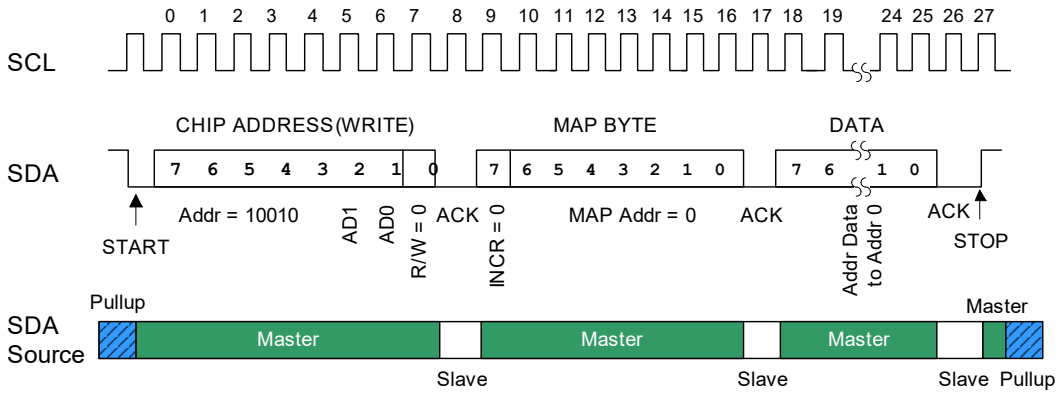


Figure 4-26. Control-Port Timing, I²C Write of Page Address

The first byte sent to the CS43L36 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write) in the LSB. To communicate with the CS43L36, the chip address field must match 1_0010, followed by the state of the AD1 and AD0 pins.

Note: Because AD0 and AD1 logic states are latched at POR, dynamic addressing is not supported.

If the operation is a write, the next byte is the memory address pointer (MAP); the 7 LSBs of the MAP byte select the address of the register to be read or written to next. The MSB of the MAP byte, INCR, selects whether autoincrementing is to be used (INCR = 1), allowing successive reads or writes of consecutive registers.

Each byte is separated by an acknowledge (ACK) bit, which the CS43L36 outputs after each input byte is read and is input to the CS43L36 from the microcontroller after each transmitted byte.

For write operations, the bytes following the MAP byte are written to the CS43L36 register addresses pointed to by the last received MAP address, plus however many autoincrements have occurred. Note that, while writing, any autoincrementing block accesses that go past the maximum 0x7F address write to address 0x00—the page address. The writes then continue to the newly selected page. Fig. 4-27 shows a write pattern with autoincrementing.

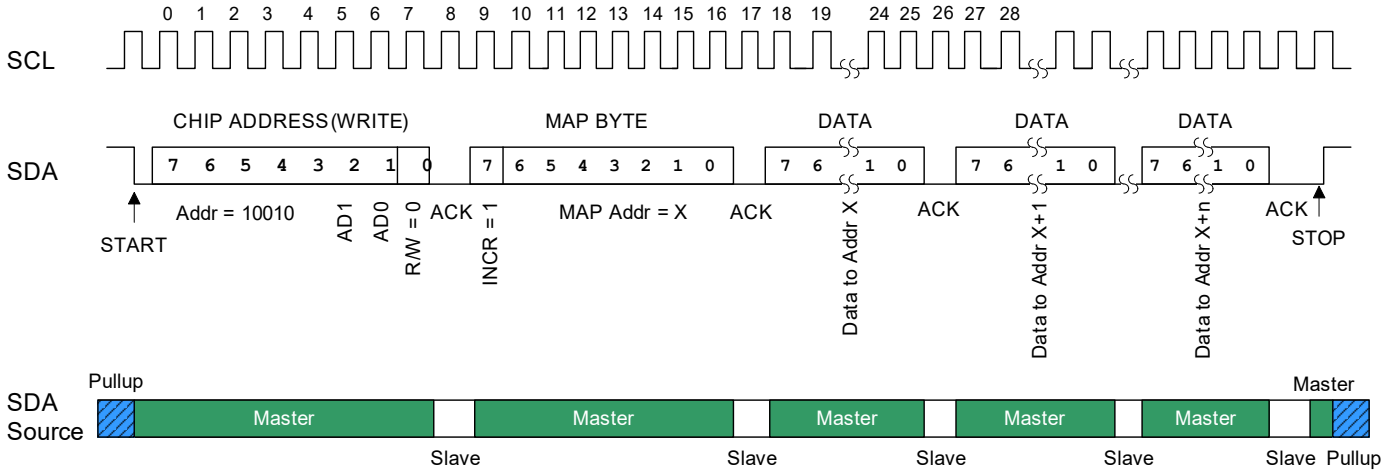


Figure 4-27. Control-Port Timing, I²C Writes with Autoincrement

For read operations, the contents of the register pointed to by the last received MAP address, plus however many autoincrements have occurred, are output in the next byte. While reading, any autoincrementing block access that goes past the maximum 0x7F address wraps around and continues reading from the same page address. Fig. 4-28 shows a read pattern following the write pattern in Fig. 4-27. Notice how read addresses are based on the MAP byte from Fig. 4-27.

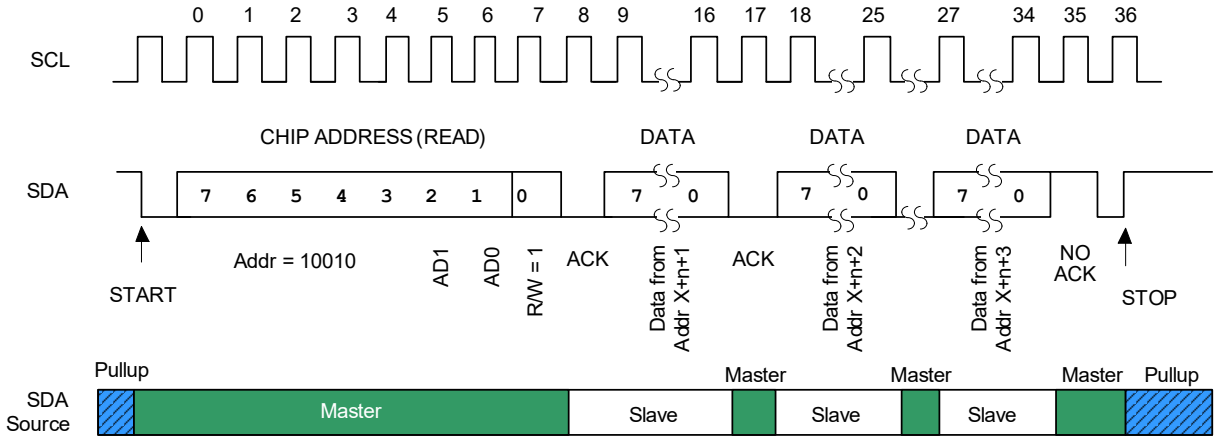


Figure 4-28. Control-Port Timing, I²C Reads with Autoincrement

To generate a read address not based on the last received MAP address, an aborted write operation can be used as a preamble (see Fig. 4-29). Here, a write operation is aborted (after the ACK for the MAP byte) by sending a Stop condition.

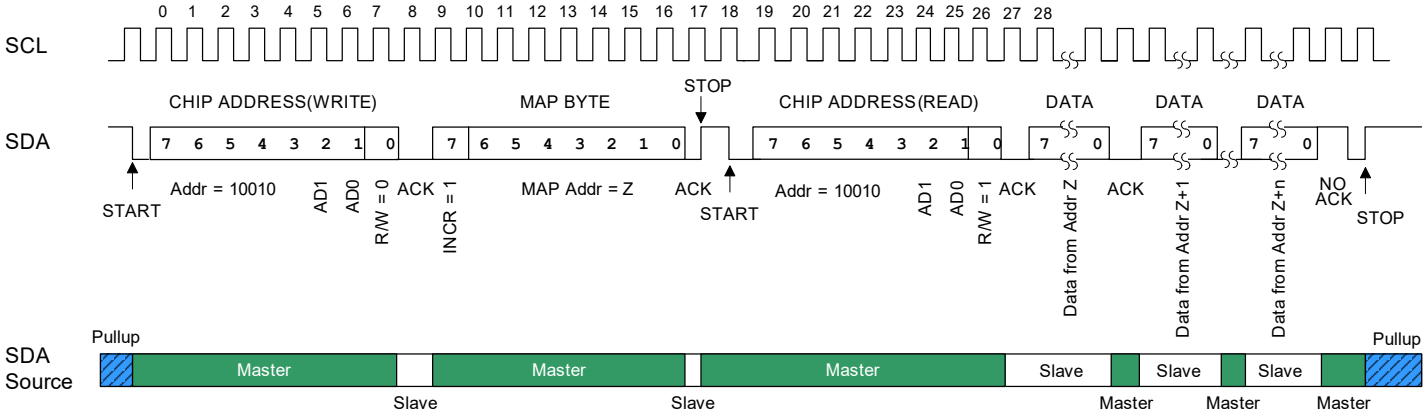


Figure 4-29. Control-Port Timing, I²C Reads with Preamble and Autoincrement

The following pseudocode illustrates an aborted write operation followed by a single read operation, assumes page address has been written. For multiple read operations, autoincrement would be set to on (as shown in Fig. 4-29).

```
Send start condition.
Send 10010(AD1)(AD0)0 (chip address and write operation).
Receive acknowledge bit.
Send MAP byte, autoincrement off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10010(AD1)(AD0)1 (chip address and read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.
```

4.11 Reset

The CS43L36 offers the reset options described in Table 4-14.

Table 4-14. Reset Summary

Reset	Cause	Result
Device hard reset	Asserting $\overline{\text{RESET}}$	If $\overline{\text{RESET}}$ is asserted, all registers (both VP and VD_FILT domains) and all state machines are immediately set to their defaults. No operation can begin until $\overline{\text{RESET}}$ is deasserted. Before normal operation can begin, $\overline{\text{RESET}}$ must be asserted at least once after the VP supply is first brought up.
Power-on reset (POR)	Power up	If VD_FILT is lower than the POR threshold, the VD_FILT register fields and the state machines are held in reset, setting them to their default values/states. This does not reset the VP registers. The POR releases the reset when the VD_FILT supply goes above the POR threshold. VL and VA supplies must be turned at the same time the VD_FILT supply is turned on.

4.12 Interrupts

The following sections describe the CS43L36 interrupt implementation.

4.12.1 Standard Interrupts

The interrupt output pin, $\overline{\text{INT}}$, is used to signal the occurrence of events within the device's interrupt status registers. Events can be masked individually by setting corresponding bits in the interrupt mask registers. Table 4-15 lists interrupt status and mask registers. The configuration of mask bits determines which events cause the immediate assertion of $\overline{\text{INT}}$:

- When an unmasked interrupt status event is detected, the status bit is set and $\overline{\text{INT}}$ is asserted.
- When a masked interrupt status event is detected, the interrupt status bit is set, but $\overline{\text{INT}}$ is not affected.

Once asserted, $\overline{\text{INT}}$ remains asserted until all status bits that are unmasked and set have been read. Interrupt status bits are sticky and read-to-clear: Once set, they remain set until the register is read and the associated interrupt condition is not present. If a condition is still present and the status bit is read, although $\overline{\text{INT}}$ is deasserted, the status bit remains set.

To clear status bits set due to initiation of a path or block, the status bits must be read after the corresponding module is enabled and before normal operation begins. Otherwise, unmasking previously set status bits causes assertion of INT.

Table 4-15. Interrupt Status Registers and Corresponding Mask Registers—0x13

Interrupt Source Status Register	Interrupt Mask Register
SRC Interrupt Status (Section 7.4.2)	SRC Interrupt Mask (Section 7.4.11)
ASP RX Interrupt Status (Section 7.4.3)	ASP RX Interrupt Mask (Section 7.4.12)
DAC Interrupt Status (Section 7.4.4)	DAC Interrupt Mask (Section 7.4.13)
Detect Interrupt Status 1 (Section 7.4.5)	Detect Interrupt Mask 1 (Section 7.7.5)
SRC Partial Lock Interrupt Status (Section 7.4.6)	SRC Partial Lock Interrupt Mask (Section 7.4.14)
VP Monitor Interrupt Status (Section 7.4.7)	VP Monitor Interrupt Mask (Section 7.4.15)
PLL Lock Interrupt Status (Section 7.4.8)	PLL Lock Mask (Section 7.4.16)

As Table 4-16 indicates, interrupt sources are categorized into two groups:

- Condition-based interrupt source bits are set when the condition is present and they remain set until the register is read and the condition that caused the bit to assert is no longer present.
- Event-based interrupt source bits are cleared when read. In the absence of subsequent source events, reading one of these status bits returns a 0.

Table 4-16. Interrupt Source Types

Group	Status Registers	Interrupt Source Type
Tip sense debounce (see Section 7.2.7)	TS_UNPLUG_DBNC TS_PLUG_DBNC	Event Event
Channel Overflow Interrupt (see Section 7.4.1)	CHA_OVFL CHB_OVFL	Event Event
Serial port (see Section 7.4.2, Section 7.4.3)	ASPRX_OVLD ASPRX_ERROR ASPRX_LATE ASPRX_EARLY [1] ASPRX_NOLRCK [1] SRC_IUNLK SRC_ILK	Event Event Event Event Condition Condition Condition
Global (see Section 7.4.4)	PDN_DONE	Condition
Headset (see Section 7.4.5)	TIP_SENSE_PLUG TIP_SENSE_UNPLUG	All are events.
DAC (see Section 7.4.6)	DAC_LK	Condition
VP monitor (see Section 7.4.7)	VPMON_TRIP	Condition
PLL (see Section 7.4.8)	PLL_LOCK	Condition
Tip sense plug/unplug status (see Section 7.4.9)	TS_UNPLUG TS_PLUG	Events. Although a true event interrupt clears when read, these dynamically reflect the state of the debounced input signal.

1. Reading this bit following an early LRCK/SM error/no LRCK returns a 1. Subsequent reads return a 0. Valid LRCK transitions or exiting the transmit overflow condition rearms the detection of the corresponding event. See Table 4-9 for details.

4.13 FILT+ Operation

FILT+ provides the internal voltage reference for the D/A converters. When powering-up the codec, FILT+ rises to its operating voltage in less than 10 ms when exiting from Power Down Mode (PDM) state.

If the integrated fractional-N PLL is enabled while the headphone interface is disabled when FILT+ is at its operating voltage, FILT+ will start discharging and drop to 0 V.

When the headphone interface is later enabled, it may take up to 1 second for FILT+ to rise again to its operating voltage. In this scenario, the headphone interface may begin operation before FILT+ is fully charged, causing unwanted distortion.

To prevent this issue, set PDN_ALL and clear PLL_START before applying any recommended power-up sequence.

5 System Applications

This section provides recommended procedures and instruction sequences for standard operations.

5.1 Power-Up Sequence

Note: Set PDN_ALL and clear PLL_START before applying any recommended power-up sequence.

Ex. 5-1 is the procedure for implementing HP playback from the ASP. This example sequence configures the CS43L36 for SCLK = 12.288 MHz, LRCK = 48 kHz, and TDM playback, in Slave Mode.

Example 5-1. Power-Up Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Apply all relevant power supplies, then assert $\overline{\text{RST}}$ before applying SCLK and LRCK to the CS43L36.			
2	Wait 2.5 ms.			
3	Power up the DAC.	Power Down Control 2. 0x1102	0x83	
		Reserved	100	—
		DISCHARGE_FILT+	0	FILT+ is not clamped to ground.
		SRC_PDN_OVERRIDE	0	SRC is powered up.
		Reserved	0	—
		DAC_SRC_PDNB	1	DAC SRC is powered up.
		Reserved	1	—
4	Configure the device's ASP and ASP SRC.			
	4.1 Configure switch from RCO to SCLK.	Oscillator Switch Control. 0x1107	0x01	
		Reserved	0000 000	—
		SCLK_PRESENT	1	SCLK is present.
	4.2 Power down the RCO.	Oscillator Switch Status. 0x1109	0x01	
		Reserved	0000 0	—
		OSC_PDNB_STAT	0	RCO powered down
		OSC_SW_SEL_STAT	01	RCO selected for internal MCLK
	4.3 Configure device's internal sample rate with the applied MCLK signal.	MCLK Control. 0x1009	0x02	
		Reserved	0000 00	—
		INTERNAL_FS	1	Internal sample rate is MCLK/256= 48 kHz.
		Reserved	0	—
	4.4 Select MCLK source.	MCLK Source Select. 0x1201	0x00	
		Reserved	0000 00	—
		MCLKDIV	0	Divide by 1.
		MCLK_SRC_SEL	0	SCLK pin is MCLK source.
	4.5 Configure the FSYNC period.	FSYNC Period, Lower Byte. 0x1205	0xFF	
		FSYNC_PERIOD_LB	1111 1111	256 SCLKs per LRCK lower byte.
	4.6 Configure the FSYNC period.	FSYNC Period, Upper Byte. 0x1206	0x00	
		FSYNC_PERIOD_UB	0000 0000	0 SCLKs per LRCK upper byte
	4.7 Configure FSYNC pulse width.	FSYNC Pulse Width, Lower Byte. 0x1203	0x1F	
		FSYNC_PULSE_WIDTH_LB	0001 1111	LRCK is one SCLK Wide.
	4.8 Configure the ASP clock.	ASP Clock Configuration 1. 0x1207	0x00	
		Reserved	00	—
		ASP_SCLK_EN	0	ASP SCLK disabled.
		ASP_HYBRID_MODE	0	LRCK is an input from an external source.
		Reserved	0	—
		ASP_SCPOL_IN_DAC	0	SCLK input drive polarity for DAC is normal.
		ASP_LCPOL_OUT	0	LRCK output drive polarity is normal.
		ASP_LCPOL_IN	0	LRCK input polarity (pad to logic) is normal.
	4.9 Configure the ASP frame.	ASP Frame Configuration. 0x1208	0x10	
		Reserved	000	—
		ASP_STP	1	Frame begins when LRCK transitions low to high
		ASP_5050	0	LRCK duty cycle per FSYNC_PULSE_WIDTH_LB/UB
		ASP_FSD	000	Zero SCLK frame start delay
	4.10 Configure serial port receive channel positions.	Serial Port Receive Channel Select. 0x2501	0x04	
		Reserved	0000	—
		SP_RX_CHB_SEL	01	SP RX Channel B position is 1.
		SP_RX_CHA_SEL	00	SP RX Channel A position is 0.
	4.11 Set receive sample rate.	Serial Port Receive Sample Rate. 0x2503	0x8C	
		Reserved	100	—
		SP_RX_FS	0 1100	SP receive sample rate = 48 kHz.
	4.12 Configure the SRC sample rate detection.	SRC Input Sample Rate. 0x2601	0x20	
		Reserved	0010	—
		SRC_SDIN_FS	0000	ASP sample rate is autodetected.

Example 5-1. Power-Up Sequence *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
	4.13 Configure Channel 2 size to 24 bits per sample.	ASP Receive DAI0 Channel 2 Phase and Resolution. 0x2A05	0x02	
		Reserved	0	—
		ASP_RX0_CH2_AP	0	In 50/50 mode, channel data valid if LRCK is low.
		Reserved	00 00	—
		ASP_RX_CH2_RES	10	Size is 24 bits per sample.
	4.14 Configure location of the Channel 2 MSB with respect to SOF.	ASP Receive DAI0 Channel 2 Bit Start MSB. 0x2A06	0x00	
		Reserved	0000 000	—
		ASP_RX0_CH2_BIT_ST_MSB	0	ASP receive bit start MSB = 0.
	4.15 Configure location of the Channel 2 LSB with respect to SOF.	ASP Receive DAI0 Channel 2 Bit Start LSB. 0x2A07	0x18	
		ASP_RX0_CH2_BIT_ST_LSB	0001 1000	ASP transmit bit start LSB = 24.
	4.16 Disable the SRC bypass.	Serial Port SRC Control. 0x1007	0x10	
		Reserved	0001	—
		I2C_DRIVE	0	I²C output drive strength normal
		Reserved	0	—
		SRC_BYPASS_DAC	0	SRC not bypassed for DAC path
		Reserved	0	—
5	Enable SCLK.	ASP Clock Configuration 1. 0x1207	0x20	
		Reserved	00	—
		ASP_SCLK_EN	1	ASP SCLK enabled.
		ASP_HYBRID_MODE	0	LRCK is an input generated from SCLK.
		Reserved	0	—
		ASP_SCPOL_IN_DAC	0	SCLK input drive polarity for DAC is normal.
		ASP_LCPOL_OUT	0	LRCK output drive polarity is normal.
		ASP_LCPOL_IN	0	LRCK input polarity (pad to logic) is normal.
6	Configure the DAC.	DAC Control 1. 0x1F01	0x00	
		Reserved	0000 00	—
		DACB_INV	0	DACA signal not inverted.
		DACA_INV	0	DACB signal not inverted.
7	Configure the appropriate volume controls and DAC source selects.			
	7.1 Set Mixer A input to 0 dB.	Channel A Input Volume. 0x2301	0x00	
		Reserved	00	—
		CHA_VOL	00 0000	Input A is set to 0 dB.
	7.2 Set Mixer B input to 0 dB.	Channel B Input Volume. 0x2303	0x00	
		Reserved	00	—
		CHB_VOL	00 0000	Input B is set to 0 dB.
8	Configure the HP control.	HP Control. 0x2001	0x03	
		Reserved	0000	—
		ANA_MUTE_B	0	Channel B is unmuted.
		ANA_MUTE_A	0	Channel A is unmuted.
		FULL_SCALE_VOL	1	Full-scale volume is -6dB for headphone output.
		Reserved	1	—
9	Power up the DAC/HP.	Power Down Control 1. 0x1101	0x96	
		Reserved	1	—
		ASP_DAI_PDN	0	ASP input path is powered up.
		MIXER_PDN	0	Mixer is powered up.
		Reserved	1	—
		HP_PDN	0	HPOUT powered up.
		Reserved	11	—
		PDN_ALL	0	DAC powered up.
10	The headphone amplifier is operational after 10 ms.			

5.2 Power-Down Sequence

Ex. 5-2 is the procedure for powering down the HP playback.

Example 5-2. Power-Down Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Configure the DAC/volume Channels.			
	1.1 Mute Volume A input.	Channel A Input Volume. 0x2301	0x3F	
		Reserved	00	—
		CHA_VOL	11 1111	Input A is muted.
	1.2 Mute Volume B input.	Channel B Input Volume. 0x2303	0x3F	
		Reserved	00	—
		CHB_VOL	11 1111	Input B is muted.
	1.3 Mute Channel A and B inputs.	HP Control. 0x2001	0x0F	
		Reserved	0000	—
		ANA_MUTE_B	1	Channel B is muted.
		ANA_MUTE_A	1	Channel A is muted.
		FULL_SCALE_VOL	1	Full-scale volume is –6 dB for headphone output.
		Reserved	1	—
	1.4 Disable SCLK.	ASP Clock Configuration 1. 0x1207	0x00	
		Reserved	00	—
		ASP_SCLK_EN	0	ASP SCLK disabled.
		ASP_HYBRID_MODE	0	LRCK is an output generated from SCLK.
		Reserved	0	—
		ASP_SCPOL_IN_DAC	0	SCLK input drive polarity for DAC is normal.
		ASP_LCPOL_OUT	0	LRCK output drive polarity is normal.
		ASP_LCPOL_IN	0	LRCK input polarity (pad to logic) is normal.
2	Power down the HP amplifier.	Power Down Control 1. 0x1101	0xFE	
		Reserved	1	—
		ASP_DAI_PDN	1	ASP input path is powered down
		MIXER_PDN	1	Mixer is powered down
		Reserved	1	—
		HP_PDN	1	HPOUT powered down
		Reserved	11	—
		PDN_ALL	0	DAC powered up
3	Power down the ASP and SRC.	Power Down Control 2. 0x1102	0x8C	
		Reserved	100	—
		DISCHARGE_FILT+	0	FILT+ is not clamped to ground.
		SRC_PDN_OVERRIDE	1	SRC is powered down.
		Reserved	1	—
		DAC_SRC_PDNB	0	DAC SRC is powered down.
		Reserved	0	—
4	Power down the DAC.	Power Down Control 1. 0x1101	0xFF	
		Reserved	1	—
		ASP_DAI_PDN	1	ASP input path is powered down
		MIXER_PDN	1	Mixer is powered down
		Reserved	1	—
		HP_PDN	1	HPOUT powered down
		Reserved	11	—
		PDN_ALL	1	DAC powered down.
5	Read PDN_DONE to confirm that the DAC is completely powered down.	DAC Interrupt Status. 0x1308	0x01	
		Reserved	0000 000	—
		PDN_DONE	1	Power-down done.
6	Repeat Step 5 until the PDN_DONE status bit indicates the DAC has powered down.			
7	Discharge the capacitor attached to the FILT+ pin.	Power Down Control 2. 0x1102	0x9C	
		Reserved	100	—
		DISCHARGE_FILT+	1	FILT+ is clamped to ground.
		SRC_PDN_OVERRIDE	1	SRC is powered down.
		Reserved	1	—
		DAC_SRC_PDNB	0	DAC SRC is powered down.
		Reserved	0	—
8	If required, remove the SCLK signal.			
9	If required, remove all relevant power supplies from the DAC.			

5.3 Page 0x30 Read Sequence

The following sequence is required to read from Page 0x30:

1. Power up Page 0x30 by clearing bit 7 of register 0x1102.
2. Enable Page 0x30 reads by writing the value 0x01 to register 0x1801.
3. Perform the read from Page 0x30.

5.4 PLL Clocking

Data-path logic is in the MCLK domain, where SCLK is expected to be 12 or 24 MHz. For clocking scenarios where ASP_SCLK is neither 12 nor 24 MHz, the PLL must be turned on to provide the desired internal MCLK. At startup, the system sets the SCLK bypass as default mode and switches to PLL output after it settles. PLL start-up time is a maximum of 1 ms.

5.5 VD_FILT/VL ESD Diode

Note the following:

- If VD_FILT is supplied externally, VL must be supplied before VD_FILT.
- If the internal LDO is enabled, it generates VD_FILT from VL.
- If the LDO is disabled ($\overline{\text{DIGLDO\_PDN}}$ asserted) and VD_FILT is supplied externally; however, the LDO diode could be forward biased in cases where VD_FILT is supplied first.
- If the LDO is disabled and VD_FILT and VL are respectively powered via separate 1.2- and 1.8-V supplies, it is recommended to have an ESD diode between VD_FILT and VL.

6 Register Quick Reference

Table 6-1 lists the register page addresses for each module.

Table 6-1. Register Base Addresses

Module Group	Page	Module	Reference
Chip-Level	0x10	Global	Section 6.1 on p. 53
	0x11	Power-down and headset detect	Section 6.2 on p. 54
	0x12	Clocking	Section 6.3 on p. 55
	0x13	Interrupt	Section 6.4 on p. 55
	0x14	Reserved	—
	0x15	Fractional-N PLL	Section 6.5 on p. 56
	0x16–0x18	Reserved	—
	0x19	Headphone load detect	Section 6.6 on p. 57
	0x1A	Reserved	—
Analog Input	0x1B	Headset Interface	Section 6.7 on p. 57
	0x1E	Reserved	—
Analog Outputs	0x1F	DAC	Section 6.8 on p. 58
	0x20	HP control	Section 6.9 on p. 58
	0x21	Class H	Section 6.10 on p. 58
	0x22	Reserved	—
Internal Modules	0x23	Mixer volume	Section 6.11 on p. 58
	0x24	Reserved	—
	0x25	AudioPort interface	Section 6.12 on p. 59
	0x26	SRC	Section 6.13 on p. 59
	0x27	Reserved	—
Serial Ports	0x28	Reserved	—
	0x29	Reserved	—
	0x2A	ASP receive	Section 6.14 on p. 59
—	0x2B–0x2F	Reserved	—
ID registers	0x30	ID registers	Section 6.15 on p. 60
—	0x31–0xFF	Reserved	—

Notes:

- Default values are shown below the bit field names.
- Default bits marked “x” are reserved or undetermined.
- Fields shown in red are controls that are also located in the VP power supply domain.
- Fields shown in turquoise are status indicators from the VP power supply domain that are selectively raw or sticky.
- Fields shown in orange are affected by the FREEZE bit (see p. 60).

6.1 Global Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94(Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x10—Global Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	0	0	0
0x01–0x04	Reserved	—							
		x	x	x	x	x	x	x	x
0x05	Revision ID (Read Only)	AREVID				MTLREVID			
p. 60		x	x	x	x	x	x	x	x
0x06	Freeze Control	—							FREEZE
p. 60		0	0	0	0	0	0	0	0
0x07	Serial Port SRC Control	—				I2C_DRIVE	—	SRC_BYPASS_DAC	—
p. 61		0	0	0	1	0	0	0	0

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94(Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x10—Global Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x08	MCLK Status (Read Only)	—						INTERNAL_FS_STAT	—
p. 61		0	0	0	0	0	0	x	0
0x09	MCLK Control	—						INTERNAL_FS	—
p. 61		0	0	0	0	0	0	1	0
0x0A	Soft Ramp Rate	ASR_RATE				DSR_RATE			
p. 61		1	0	1	0	0	1	0	0
0x0B	Slow Start Enable	—	SLOW_START_EN			—			
p. 62		0	1	1	1	0	0	0	0
0x0C–0x0D	Reserved	—							
		x	x	x	x	x	x	x	x
0x0E	I²C Debounce	I2C_SDA_DBNC_CNT			I2C_SDA_DBNC_EN	I2C_SCL_DBNC_CNT			I2C_SCL_DBNC_EN
p. 62		1	0	0	0	1	0	0	0
0x0F	I²C Stretch	I2C_STRETCH							
p. 62		0	0	0	0	0	0	1	1
0x10	I²C Timeout	MAS_I2C_NACK	MAS_TO_DIS	MAS_TO_SEL		ACC_TO_DIS	ACC_TO_SEL		
p. 62		1	0	1	1	0	1	1	1
0x11–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.2 Power-Down and Headset-Detect Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94(Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x11—Power-Down and Headset-Detect Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	0	0	1
0x01	Power Down Control 1	—	ASP_DAI_PDN	MIXER_PDN		HP_PDN	—		PDN_ALL
p. 63		1	1	1	1	1	1	1	1
0x02	Power Down Control 2	—			DISCHARGE_FILT+	SRC_PDN_OVERRIDE	—	DAC_SRC_PDNB	—
p. 63		1	0	0	0	0	1	0	0
0x03	Power Down Control 3	—					VPMON_PDNB	—	
p. 64		0	0	1	0	0	0	0	0
0x04–0x06	Reserved	—							
		x	x	x	x	x	x	x	x
0x07	Oscillator Switch Control	—							SCLK_PRESENT
p. 64		0	0	0	0	0	0	0	0
0x08	Reserved	—							
		x	x	x	x	x	x	x	x
0x09	Oscillator Switch Status (Read Only)	—					OSC_PDNB_STAT	OSC_SW_SEL_STAT	
p. 64		0	0	0	0	0	1	0	1
0x0A–0x12	Reserved	—							
		x	x	x	x	x	x	x	x
0x13	Tip Sense Control 1	TS_INV	—	TS_FALL_DBNCE_TIME			TS_RISE_DBNCE_TIME		
p. 64		0	0	0	1	1	0	1	1
0x15	Tip Sense Indicator Status (Read Only)	—				TS_UNPLUG_DBNC	TS_PLUG_DBNC	—	
p. 65		0	0	0	0	x	x	x	x
0x16–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.3 Clocking Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x12—Clocking Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	0	1	0
0x01	MCLK Source Select	—						MCLKDIV	MCLK_SRC_SEL
p. 65		0	0	0	0	0	0	0	0
0x02	Reserved	—							
		x	x	x	x	x	x	x	x
0x03	FSYNC Pulse Width Lower Byte	FSYNC_PULSE_WIDTH_LB							
p. 66		0	0	0	0	0	0	0	0
0x04	FSYNC Pulse Width Upper Byte	—					FSYNC_PULSE_WIDTH_UB		
p. 66		0	0	0	0	0	0	0	0
0x05	FSYNC Period Lower Byte	FSYNC_PERIOD_LB							
p. 66		1	1	1	1	1	0	0	1
0x06	FSYNC Period Upper Byte	—				FSYNC_PERIOD_UB			
p. 66		0	0	0	0	0	0	0	0
0x07	ASP Clock Configuration 1	—		ASP_SCLK_EN	ASP_HYBRID_MODE	—	ASP_SCPOL_IN_DAC	ASP_LCPOL_OUT	ASP_LCPOL_IN
p. 66		0	0	0	0	0	0	0	0
0x08	ASP Frame Configuration	—			ASP_STP	ASP_5050	ASP_FSD		
p. 67		0	0	0	1	0	0	0	0
0x09	Fs Rate Enable	—					FS_EN		
p. 67		0	0	0	0	0	0	0	0
0x0A	Input ASRC Clock Select	—						CLK_IASRC_SEL	
p. 67		0	0	0	0	0	0	0	0
0x0B	Reserved	—							
		x	x	x	x	x	x	x	x
0x0C	PLL Divide Configuration 1	—						SCLK_PREDIV	
p. 67		0	0	0	0	0	0	0	0
0x0D–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.4 Interrupt Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x13—Interrupt Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	0	1	1
0x01	Reserved	—							
		x	x	x	x	x	x	x	x
0x02	Channel Overflow Interrupt Status (Read Only)	—						CHA_OVFL	CHB_OVFL
p. 68		0	0	0	0	x	x	x	x
0x03	SRC Interrupt Status (Read Only)	—					SRC_IUNLK	—	SRC_ILK
p. 68		0	0	0	0	x	x	x	x
0x04	ASP RX Interrupt Status (Read Only)	—			ASPRX_OVLD	ASPRX_ERROR	ASPRX_LATE	ASPRX_EARLY	ASPRX_NOLRCK
p. 68		0	0	0	x	x	x	x	x
0x05–0x07	Reserved	—							
		x	x	x	x	x	x	x	x
0x08	DAC Interrupt Status (Read Only)	—							PDN_DONE
p. 69		0	0	0	0	0	0	x	x
0x09	Detect Status 1 (Read Only)	—	TIP_SENSE_PLUG	TIP_SENSE_UNPLUG	—				
p. 69		x	x	x	x	x	x	x	x
0x0A	Reserved	—							
		x	x	x	x	x	x	x	x

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x13—Interrupt Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x0B	DAC Lock Status (Read Only)	—	DAC_UNLK	—			DAC_LK	—	
p. 69		x	x	x	x	x	x	x	x
0x0C	Reserved	—							
		x	x	x	x	x	x	x	x
0x0D	VPMON Interrupt (Read Only)	—							VPMON_TRIP
p. 69		0	0	0	0	0	0	0	x
0x0E	PLL Lock (Read Only)	—							PLL_LOCK
p. 70		0	0	0	0	0	0	0	x
0x0F	Tip Sense Plug/Unplug Interrupt Status (Read Only)	—				TS_UNPLUG	TS_PLUG	—	
p. 70		x	x	x	x	x	x	x	x
0x10–0x16	Reserved	—							
		x	x	x	x	x	x	x	x
0x17	Channel Overflow Interrupt Mask	—						M_CHA_OVFL	M_CHB_OVFL
p. 70		0	0	0	0	1	1	1	1
0x18	SRC Interrupt Mask	—					M_SRC_IUNLK		M_SRC_ILK
p. 70		0	0	0	0	1	1	1	1
0x19	ASP RX Interrupt Mask	—			M_ASPRX_OVLD	M_ASPRX_ERROR	M_ASPRX_LATE	M_ASPRX_EARLY	M_ASPRX_NOLRCK
p. 71		0	0	0	1	1	1	1	1
0x1A	Reserved	—							
		x	x	x	x	x	x	x	x
0x1B	DAC Interrupt Mask	—							M_PDN_DONE
p. 71		0	0	0	0	0	0	1	1
0x1C	DAC Lock Mask		M_DAC_UNLK	—			M_DAC_LK	—	
p. 71		0	1	1	1	1	1	1	1
0x1D	Reserved	—							
		0	0	0	0	0	0	0	0
0x1E	VPMON Interrupt Mask	—							M_VPMON_TRIP
p. 72		0	0	0	0	0	0	0	1
0x1F	PLL Lock Mask	—							M_PLL_LOCK
p. 72		0	0	0	0	0	0	0	1
0x20	Tip Sense Plug/Unplug Interrupt Mask	—				M_TS_UNPLUG	M_TS_PLUG	—	
p. 72		0	0	0	0	1	1	1	1
0x21–0x7F	Reserved	—							
		0	0	0	0	0	0	0	0

6.5 Fractional-N PLL Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x15—Fractional-N PLL Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	1	0	1
0x01	PLL Control 1	—							PLL_START
p. 72		0	0	0	0	0	0	0	0
0x02	PLL Division Fractional Byte 0	PLL_DIV_FRAC[7:0]							
p. 73		0	0	0	0	0	0	0	0
0x03	PLL Division Fractional Byte 1	PLL_DIV_FRAC[15:8]							
p. 73		0	0	0	0	0	0	0	0
0x04	PLL Division Fractional Byte 2	PLL_DIV_FRAC[23:16]							
p. 73		0	0	0	0	0	0	0	0
0x05	Division Integer	PLL_DIV_INT[7:0]							
p. 73		0	1	0	0	0	0	0	0
0x06–0x07	Reserved	—							
		x	x	x	x	x	x	x	x

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x15—Fractional-N PLL Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x08	PLL Control 3	PLL_DIVOUT							
p. 73		0	0	0	1	0	0	0	0
0x09	Reserved	—							
		x	x	x	x	x	x	x	x
0x0A	PLL Calibration Ratio	PLL_CAL_RATIO							
p. 73		1	0	0	0	0	0	0	0
0x0B–0x1A	Reserved	—							
		x	x	x	x	x	x	x	x
0x1B	PLL Control 4	—						PLL_MODE	
p. 73		0	0	0	0	0	0	1	1
0x1C–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.6 HP Load Detect Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x19—HP Load Detect Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	1	0	0	1
0x01–0x24	Reserved	—							
		x	x	x	x	x	x	x	x
0x25	Load Detect R/C Status (Read Only)	—			CLA_STAT	—		RLA_STAT	
p. 74		0	0	0	0	0	0	0	0
0x26	HP Load Detect Done (Read Only)	—							HPLOAD_DET_DONE
p. 74		0	0	0	0	0	0	0	0
0x27	HP Load Detect Enable	—							HP_LD_EN
p. 74		0	0	0	0	0	0	0	0
0x28–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.7 Headset Interface Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1B—Headset Interface Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	1	0	1	1
0x01–0x6F	Reserved	—							
		x	x	x	x	x	x	x	x
0x70	Reserved	—							
		x	x	x	x	x	x	x	x
0x71	Wake Control	—	M_HP_WAKE	WAKEB_MODE	—				WAKEB_CLEAR
p. 74		1	1	0	0	0	0	0	0
0x72	Reserved	—							
		x	x	x	x	x	x	x	x
0x73	Tip Sense Control	TIP_SENSE_CTRL		TIP_SENSE_INV	—			TIP_SENSE_DEBOUNCE	
p. 75		0	0	0	0	0	0	1	0
0x74	Reserved	—							
		x	x	x	x	x	x	x	x
0x75	Mic Detect Control 1	LATCH_TO_VP	EVENT_STATUS_SEL	—					
p. 75		0	0	0	1	1	1	1	1
0x76	Reserved	—							
		x	x	x	x	x	x	x	x
0x77	Detect Status 1 (Read Only)	TIP_SENSE				—			
p. 76		x	x	0	x	x	x	x	x

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1B—Headset Interface Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x78	Reserved	—							
		x	x	x	x	x	x	x	x
0x79	Detect Interrupt Mask 1	—	M_TIP_SENSE_PLUG	M_TIP_SENSE_UNPLUG	—				
p. 76		1	1	1	0	0	0	0	0
0x7A–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.8 DAC Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1F—DAC Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	1	1	1	1
0x01	DAC Control 1	—						DACB_INV	DACA_INV
p. 76		0	0	0	0	0	0	0	0
0x02–0x05	Reserved	—							
		x	x	x	x	x	x	x	x
0x06	DAC Control 2	HPOUT_PULLDOWN				HPOUT_LOAD	HPOUT_CLAMP	DAC_HPF_EN	—
p. 76		0	0	0	0	0	0	1	0
0x07–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.9 HP Control Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x20—HP Control Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	0	0	0
0x01	HP Control	—				ANA_MUTE_B	ANA_MUTE_A	FULL_SCALE_VOL	—
p. 77		0	0	0	0	1	1	0	1
0x02–0x7F	Reserved	—							
		0	0	0	0	0	0	0	0

6.10 Class H Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x21—Class H Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	0	0	1
0x01	Class H Control	—					ADPTPWR		
p. 77		0	0	0	0	0	1	1	1
0x02–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.11 Mixer Volume Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x23—Mixer Volume Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	0	1	1
0x01	Channel A Input Volume	—		CHA_VOL					
p. 77		0	0	1	1	1	1	1	1
0x02	Reserved	—							
		x	x	x	x	x	x	x	x
0x03	Channel B Input Volume	—		CHB_VOL					
p. 78		0	0	1	1	1	1	1	1

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x23—Mixer Volume Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x04–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.12 AudioPort Interface Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x25—AudioPort Interface Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	1	0	1
0x01	Serial Port Receive Channel Select	—				SP_RX_CHB_SEL		SP_RX_CHA_SEL	
p. 78		0	0	0	0	0	1	0	0
0x02	Serial Port Receive Isochronous Control	—	SP_RX_RSYNC	SP_RX_NSB_POS			SP_RX_NFS_NSBB	SP_RX_ISOC_MODE	
p. 78		0	0	0	0	0	1	0	0
0x03	Serial Port Receive Sample Rate	—			SP_RX_FS				
p. 79		1	0	0	0	1	1	0	0
0x04–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.13 SRC Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x26—SRC Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	1	1	0
0x01	SRC Input Sample Rate	—			SRC_SDIN_FS				
p. 79		0	1	0	0	0	0	0	0
0x02–0x08	Reserved	—							
		x	x	x	x	x	x	x	x
0x09–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.14 Serial Port Receive Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x2A—Serial Port Receive Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	1	0	1	0
0x01	ASP Receive DAI0 Enable	—				ASP_RX0_CH2_EN	ASP_RX0_CH1_EN	—	
p. 79		0	0	0	0	0	0	0	0
0x02	ASP Receive DAI0 Channel 1 Phase and Resolution	—	ASP_RX0_CH1_AP	—				ASP_RX0_CH1_RES	
p. 79		0	0	0	0	0	0	1	1
0x03	ASP Receive DAI0 Channel 1 Bit Start MSB	—							ASP_RX0_CH1_BIT_ST_MSB
p. 80		0	0	0	0	0	0	0	0
0x04	ASP Receive DAI0 Channel 1 Bit Start LSB	ASP_RX0_CH1_BIT_ST_LSB							
p. 80		0	0	0	0	0	0	0	0
0x05	ASP Receive DAI0 Channel 2 Phase and Resolution	—	ASP_RX0_CH2_AP	—				ASP_RX0_CH2_RES	
p. 80		0	0	0	0	0	0	1	1
0x06	ASP Receive DAI0 Channel 2 Bit Start MSB	—							ASP_RX0_CH2_BIT_ST_MSB
p. 80		0	0	0	0	0	0	0	0
0x07	ASP Receive DAI0 Channel 2 Bit Start LSB	ASP_RX0_CH2_BIT_ST_LSB							
p. 80		0	0	0	0	0	0	0	0

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x2A—Serial Port Receive Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x08–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.15 ID Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94(Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x30—ID Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	1	0	0	0	0
0x01–0x13	Reserved	—							
		x	x	x	x	x	x	x	x
0x14	Subrevision	SUBREVISION							
p. 81		x	x	x	x	x	x	x	x
0x15	Device ID A and B (Read Only)	DEVIDA				DEVIDB			
p. 81		0	1	0	0	0	0	1	1
0x16	Device ID C and D (Read Only)	DEVIDC				DEVIDD			
p. 81		1	0	1	0	0	0	1	1
0x17	Device ID E (Read Only)	DEVIDE				—			
p. 81		0	1	1	0	x	x	x	x
0x–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

7 Register Descriptions

The tables in this section give bit assignments, definitions, and default states after power-up or reset. Reserved register fields must maintain default states. Section 6 describes the red, turquoise, and orange indicators.

7.1 Global Registers

7.1.1 Revision ID

Address 0x1005

	7	6	5	4	3	2	1	0
R/O	AREVID				MTLREVID			
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7:4	AREVID	Alpha revision. CS43L36 alpha revision level. AREVID and MTLREVID form the complete device revision ID (e.g.,: A0, B2). 0x00 … 0xFF
3:0	MTLREVID	Metal revision. CS43L36 metal revision level. AREVID and MTLREVID form the complete device revision ID (e.g.,: A0, B2). 0x00 … 0xFF

7.1.2 Freeze Control

Address 0x1006

	7	6	5	4	3	2	1	0
R/W	—							FREEZE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	FREEZE	Freeze registers. Configures a hold on all volume-control and power-down register settings. Use this bit only during normal operation after all circuit blocks in use have powered up. Using the bit when an affected circuit block is powering up could cause the change to occur immediately when power up completes (i.e., not gated by the FREEZE bit). Bits affected by FREEZE are shown in orange throughout Section 6 and Section 7. 0 (Default) Volume-control and power-down register changes take effect immediately. 1 Modifications made to volume-control and power-down registers take effect only after this bit is cleared.

7.1.3 Serial Port SRC Control

Address 0x1007

	7	6	5	4	3	2	1	0
R/W	—				I2C_DRIVE	—	SRC_BYPASS_DAC	—
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	I2C_DRIVE	I²C output drive strength. Selects drive strength used for the SDA output 0 (Default) Normal 1 Decreased
2	—	Reserved
1	SRC_BYPASS_DAC	Bypass SRC (DAC path). Determines the bypass of the input SRCs. See Section 4.6 for details. 0 (Default) No bypass 1 Bypass. SRC_SDIN_FS (see p. 79) must be set equal to Fs_{INT}.
0	—	Reserved

7.1.4 MCLK Status

Address 0x1008

	7	6	5	4	3	2	1	0
R/W	—						INTERNAL_FS_STAT	—
Default	0	0	0	0	0	0	x	0

Bits	Name	Description
7:2	—	Reserved
1	INTERNAL_FS_STAT	Internal sample rate status. Indicates the divide ratio from $MCLK_{INT}$ (set in INTERNAL_FS, see Section 7.1.5) to produce the internal sample rate for all converters. 0 Fs_{INT} = $MCLK_{INT}$/250. Indicates that the internal MCLK is 12 or 24 MHz. 1 Fs_{INT} = $MCLK_{INT}$/256. Indicates that the internal MCLK is 11.2896, 12.288, 22.5792, or 24.576 MHz.
0	—	Reserved

7.1.5 MCLK Control

Address 0x1009

	7	6	5	4	3	2	1	0
R/W	—						INTERNAL_FS	—
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:2	—	Reserved
1	INTERNAL_FS	Internal sample rate (Fs_{INT}). Selects the divide ratio from $MCLK_{INT}$ to produce the internal sample rate for all converters. See Table 4-4 for programming details. This bit always returns zero when read. Reports status in INTERNAL_FS_STAT. 0 Fs_{INT} = $MCLK_{INT}$/250. Set if internal MCLK is 12 or 24 MHz. 1 (Default) Fs_{INT} = $MCLK_{INT}$/256. Set if internal MCLK is 11.2896, 12.288, 22.5792, or 24.576 MHz. If $MCLK_{INT}$ 11.2896, 12, or 12.288 MHz, MCLKDIV must be 0. If it is 22.5792, 24, or 24.576 MHz, MCLKDIV must be 1.
0	—	Reserved

7.1.6 Soft Ramp Rate

Address 0x100A

	7	6	5	4	3	2	1	0
R/W	ASR_RATE				DSR_RATE			
Default	1	0	1	0	0	1	0	0

Bits	Name	Description
7:4	ASR_RATE	Analog soft-ramp rate (number of Fs periods between steps). Selects the soft ramp rate for all analog volumes. Step size = 1 dB or 2 dB for HPOUTx. See Section 4.2.2 for details. 0000 1 0010 4 0100 8 0110 12 1000 22 1010 (Default) 33 1100 44 1110 66 0001 2 0011 6 0101 11 0111 16 1001 24 1011 36 1101 48 1111 72
3:0	DSR_RATE	Digital soft-ramp rate (number of Fs periods between steps). Selects soft ramp rate for all digital volumes. Step size = 0.125 dB. 0000 1 0010 4 0100 (Default) 8 0110 12 1000 22 1010 33 1100 44 1110 66 0001 2 0011 6 0101 1 0111 16 1001 24 1011 36 1101 48 1111 72

7.1.7 Slow Start Enable

Address 0x100B

	7	6	5	4	3	2	1	0
R/W	—	SLOW_START_EN			—			
Default	0	1	1	1	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	SLOW_START_EN	Slow startup enable. Selects between fast and slow start-up times. See Section 4.2.3 for details. 000 Disabled. Shortens start-up time of the volume control, DAC, and HP. Useful for high-definition audio applications. 111 (Default) Enabled
3:0	—	Reserved

7.1.8 I²C Debounce

Address 0x100E

	7	6	5	4	3	2	1	0
R/W	I2C_SDA_DBNC_CNT			I2C_SDA_DBNC_EN	I2C_SCL_DBNC_CNT			I2C_SCL_DBNC_EN
Default	1	0	0	0	1	0	0	0

Bits	Name	Description
7:5	I2C_SDA_DBNC_CNT	I²C debounce count. Number of MCLKs to debounce SDA input **Note:** The I2C_SDA_DBNC_CNT and I2C_SCL_DBNC_CNT settings must be identical. 000 0 MCLKs 010 2 MCLKs 100 (Default) 4 MCLKs 110 6 MCLKs 001 1 MCLK 011 3 MCLKs 101 5 MCLKs 111 7 MCLKs
4	I2C_SDA_DBNC_EN	I²C SDA debounce enable. SDA debounce enable **Note:** The I2C_SDA_DBNC_EN and I2C_SCL_DBNC_EN settings must be identical. 0 (Default) Disabled. Must be 0 for Fast Mode or Fast-Mode Plus. 1 Enabled
3:1	I2C_SCL_DBNC_CNT	I²C SCL debounce count. Number of MCLKs to debounce SCL input **Note:** The I2C_SDA_DBNC_CNT and I2C_SCL_DBNC_CNT settings must be identical. 000 0 MCLKs 010 2 MCLKs 100 (Default) 4 MCLKs 110 6 MCLKs 001 1 MCLK 011 3 MCLKs 101 5 MCLKs 111 7 MCLKs
0	I2C_SCL_DBNC_EN	I²C SCL debounce count enable. **Note:** The settings of I2C_SDA_DBNC_EN and I2C_SCL_DBNC_EN must be identical. 0 (Default) Disabled. Must be 0 for Fast Mode or Fast-Plus Mode. 1 Enabled

7.1.9 I²C Stretch

Address 0x100F

	7	6	5	4	3	2	1	0
R/W	I2C_STRETCH							
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:0	I2C_STRETCH	I²C stretch. Number of additional MCLKs to clock stretch after the slave is ready 0000 0011 (Default) 3 MCLKs

7.1.10 I²C Timeout

Address 0x1010

	7	6	5	4	3	2	1	0
R/W	MAS_I2C_NACK	MAS_TO_DIS	MAS_TO_SEL		ACC_TO_DIS	ACC_TO_SEL		
Default	1	0	1	1	0	1	1	1

Bits	Name	Description
7	MAS_I2C_NACK	APB master I²C NACK. Determines whether clock stretching or a NACK occurs if an APB access is attempted and I²C is not APB master. 0 I²C clock stretches if an APB access is attempted while I²C is not APB master. 1 (Default) I²C NACKs if APB access is attempted while I²C is not APB master.
6	MAS_TO_DIS	APB master access timeout disable 0 (Default) Enabled 1 Disabled
5:4	MAS_TO_SEL	APB master access timeout select. Determines the timeout duration. 00 64 ms 01 128 ms 10 256 ms 11 (Default) 512 ms
3	ACC_TO_DIS	APB access timeout disable. 0 (Default) Enabled 1 Disabled

Bits	Name	Description
2:0	ACC_TO_SEL	APB access timeout select. Determines the timeout duration in MCLKs. 000 7 MCLKs 010 31 MCLKs 100 127 MCLKs 110 511 MCLKs 001 15 MCLKs 011 63 MCLKs 101 255 MCLKs 111 (Default) 65,535 MCLKs

7.2 Power Down and Headset Detects

7.2.1 Power Down Control 1

Address 0x1101

R/W	7	6	5	4	3	2	1	0
	—	ASP_DAI_PDN	MIXER_PDN	—	HP_PDN	—		PDN_ALL
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_DAI_PDN	ASP DAI0 input path power down. Configures ASP DAI0 SDIN path power state. 0 Powered up 1 (Default) Powered down. Setting this bit does not tristate the serial port clock.
5	MIXER_PDN	Mixer power down. Configures the mixer power state. 0 The mixer is powered up. 1 (Default) The mixer is powered down.
4	—	Reserved
3	HP_PDN	HPOUTx power down 0 The HP driver and DACx are powered up. 1 (Default) The HP driver and DACx are powered down.
2:1	—	Reserved
0	PDN_ALL	DAC power down. Configures the entire DAC's power state except for PLL_START. After power up (PDN_ALL: 1 → 0), individual subblocks are powered according to power-control programming. This bit is affected by LATCH_TO_VP (see p. 75). **Note:** The SRC power-down state depends on the SRC_PDN_OVERRIDE setting (see p. 63). 0 Powered up, per the individual *x*_PDN controls 1 (Default) Powered down. PDN_ALL must not be set without first enabling LATCH_TO_VP. After PDN_ALL is set and the entire DAC is powered down, PDN_DONE is set, indicating that SCLK can be removed.

7.2.2 Power Down Control 2

Address 0x1102

R/W	7	6	5	4	3	2	1	0
	—			DISCHARGE_FILT+	SRC_PDN_OVERRIDE	—	DAC_SRC_PDNB	—
Default	1	0	0	0	0	1	0	0

Bits	Name	Description
7:5	—	Reserved
4	DISCHARGE_FILT+	Discharge FILT+ capacitor. Configures the state of the FILT+ pin internal clamp. Before setting this bit, ensure that the VD_FILT device input is connected to a supply, as shown in Table 3-2. 0 (Default) FILT+ is not clamped to ground. 1 FILT+ is clamped to ground. This must be set only if PDN_ALL = 1. Discharge time with an external 2.2-µF capacitor on FILT+ is ~46 ms.
3	SRC_PDN_OVERRIDE	SRC power down override. Configures the SRCs' power states. 0 (Default) Power state control for the DAC SRCs, which are controlled by the following smart logic: • DAC SRCs are off if SRC_BYPASS_DAC = 1. • • If PDN_ALL = 1, all SRCs are off. • If PDN_ALL = 0 and the respective DAC bypass bits = 0, the following controls each SRC's power state: –If DAI0 is enabled, the DAC SRCs are powered up. 1 DAC SRCs are controlled by DAC_SRC_PDNB.
2	—	Reserved
1	DAC_SRC_PDNB	DAC SRC power down. Configures the DAC ASP power state if SRC_PDN_OVERRIDE = 1. 0 (Default) Power down 1 Power up audio DAC SRC only
0	—	Reserved

7.2.3 Power Down Control 3

Address 0x1103

	7	6	5	4	3	2	1	0
R/W			—			VPMON_PDNB	—	
Default	0	0	1	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	VPMON_PDNB	VPMON power down. VP monitor is described in Section 4.9.1. 0 (Default) Power down VPMON. 1 Power up VPMON.
1:0	—	Reserved

7.2.4 Oscillator Switch Control

Address 0x1107

	7	6	5	4	3	2	1	0
R/W				—				SCLK_PRESENT
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	SCLK_PRESENT	SCLK present. Used to select the internal MCLK source. See Section 4.4 for programming details. 0→1 transition starts switch from RCO to selected internal MCLK (SCLK must be running first). 1→0 transition starts switch from selected internal MCLK to RCO (SCLK must keep running during transition). 0 (Default) SCLK may be present, but the internal MCLK is sourced from the RCO. 1 SCLK is present and the internal MCLK is sourced from the SCLK pin.

7.2.5 Oscillator Switch Status

Address 0x1109

	7	6	5	4	3	2	1	0
R/O			—			OSC_PDNB_STAT	OSC_SW_SEL_STAT	
Default	0	0	0	0	0	1	x	x

Bits	Name	Description
7:3	—	Reserved
2	OSC_PDNB_STAT	RCO power-down status. Indicates the RCO power state. See Section 4.4 for programming details. 0 RCO powered down 1 (Default) RCO powered up
1:0	OSC_SW_SEL_STAT	RCO switch status. Indicates the RCO oscillator switch status. See Section 4.4 for programming details. 00 In transition 10–11Reserved 01 (Default) RCO selected for internal MCLK

7.2.6 Tip Sense Control 1

Address 0x1113

	7	6	5	4	3	2	1	0
R/W	TS_INV	—	TS_FALL_DBNCE_TIME			TS_RISE_DBNCE_TIME		
Default	0	0	0	1	1	0	1	1

Bits	Name	Description
7	TS_INV	Tip sense raw signal invert. Used to invert the raw signal from the tip-sense circuit. Reverses the meaning of TS_UNPLUG_DBNC and TS_PLUG_DBNC (see p. 65). 0 (Default) Not inverted 1 Inverted
6	—	Reserved
5:3	TS_FALL_DBNCE_TIME	Tip sense falling debounce time. Section 4.8.3 gives programming details. 000 0 ms 010 250 ms 100 750 ms 110 1.25 s 001 125 ms 011 (Default) 500 ms 101 1.0 s 111 1.5 s
2:0	TS_RISE_DBNCE_TIME	Tip sense rising debounce time. Section 4.8.3 gives programming details. 000 0 ms 010 250 ms 100 750 ms 110 1.25 s 001 125 ms 011 (Default) 500 ms 101 1.0 s 111 1.5 s

7.2.7 Tip Sense Indicator Status

Address 0x1115

	7	6	5	4	3	2	1	0
R/O	—				TS_UNPLUG_DBNC	TS_PLUG_DBNC	—	
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:4	—	Reserved
3	TS_UNPLUG_DBNC	Tip sense unplug debounce status. See Section 4.8.3 for details. Setting TS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
2	TS_PLUG_DBNC	Tip sense plug debounce status. See Section 4.8.3 for details. Setting TS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
1:0	—	Reserved

7.3 Clocking Registers

7.3.1 MCLK Source Select

Address 0x1201

	7	6	5	4	3	2	1	0
R/W	—						MCLKDIV	MCLK_SRC_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	MCLKDIV	Master clock divide ratio. Selects the divide ratio between the selected MCLK source and the $MCLK_{INT}$. Section 4.4.2 lists supported MCLK rates and their associated programming settings. 0 (Default) Divide by 1 (source $MCLK_{INT}$ = ~12 MHz). 1 Divide by 2 (source $MCLK_{INT}$ = ~24 MHz) **Note:** Change this field only if PDN_ALL = 1.
0	MCLK_SRC_SEL	Master clock source select. Selects the internal master clock source. For programming details and examples, see Section 4.4. 0 (Default) SCLK pin 1 PLL clock

7.3.2 FSYNC Pulse Width, Lower Byte

Address 0x1203

	7	6	5	4	3	2	1	0
R/W	FSYNC_PULSE_WIDTH_LB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	FSYNC_PULSE_WIDTH_LB	FSYNC pulse width LB. FSYNC_PULSE_WIDTH_UB | FSYNC_PULSE_WIDTH_LB provides an 11-bit field to set the duty cycle of LRCK in Hybrid-Master Mode. These combined value forms an integer number of SCLK periods within an LRCK frame that governs the LRCK high time. See Section 4.5.2 for usage details and Section 5 for a programming example. The value must be 1 less than the desired width of the LRCK pulse, measured in SCLK counts, as illustrated by the value below. FSYNC_PULSE_WIDTH_UB | FSYNC_PULSE_WIDTH_LB yield the following setting value: 000 0000 0000 (Default) LRCK is one SCLK wide.

7.3.3 FSYNC Pulse Width, Upper Byte

Address 0x1204

	7	6	5	4	3	2	1	0
R/W	—					FSYNC_PULSE_WIDTH_UB		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2:0	FSYNC_PULSE_WIDTH_UB	FSYNC pulse width UB. See description for FSYNC_PULSE_WIDTH_LB in Section 7.3.2. 000 (Default)

7.3.4 FSYNC Period, Lower Byte

Address 0x1205

	7	6	5	4	3	2	1	0
R/W	FSYNC_PERIOD_LB							
Default	1	1	1	1	1	0	0	1

Bits	Name	Description
7:0	FSYNC_PERIOD_LB	FSYNC period LB. FSYNC_PERIOD_UB | FSYNC_PERIOD_LB controls frequency (number of SCLKs per LRCK) of LRCK for ASP. Section 4.5.2 for details on how this register is used and Section 5 for a programming example. The final SCLKs per LRCK count is +1 of the value set in the UB|LB register field FSYNC_PERIOD_UB | FSYNC_PERIOD_LB yield the following setting values: 0x000 1 SCLK/LRCK … 0x0F9 (Default) 250 SCLKs/ LRCK … 0xFFF 4096 SCLKs/ LRCK

7.3.5 FSYNC Period, Upper Byte

Address 0x1206

	7	6	5	4	3	2	1	0
R/W	—				FSYNC_PERIOD_UB			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	FSYNC_PERIOD_UB	FSYNC period UB. See description for FSYNC_PERIOD_LB in Section 7.3.4. 0000 (Default)

7.3.6 ASP Clock Configuration 1

Address 0x1207

	7	6	5	4	3	2	1	0
R/W	—		ASP_SCLK_EN	ASP_HYBRID_MODE	—	ASP_SCPOL_IN_DAC	ASP_LCPOL_OUT	ASP_LCPOL_IN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ASP_SCLK_EN	ASP SCLK enable. Must be set if DAI functionality is used. 0 (Default) Disabled 1 Enabled
4	ASP_HYBRID_MODE	ASP Hybrid-Master Mode. Allows the internal LRCK to be generated from SCLK. See Fig. 4-15 for details. 0 (Default) LRCK is input from external source which is synchronous to SCLK (Slave Mode). 1 LRCK is an output generated from SCLK (Hybrid Master Mode).
3	—	Reserved
2	ASP_SCPOL_IN_DAC	ASP SCLK input polarity. Determines the polarity for the DAC path. See Fig. 4-15 for details. 0 (Default) SDIN latched on falling edge 1 SDIN latched on rising edge
1	ASP_LCPOL_OUT	ASP LRCK output drive polarity. Determines the polarity for the ASP LRCK output drive. See Fig. 4-15 for details. 0 (Default) Normal 1 Inverted
0	ASP_LCPOL_IN	ASP LRCK input polarity. Determines ASP LRCK input polarity (pad to logic). See Fig. 4-15 for details. 0 (Default) Normal 1 Inverted

7.3.7 ASP Frame Configuration

Address 0x1208

	7	6	5	4	3	2	1	0
R/W	—			ASP_STP	ASP_5050	ASP_FSD		
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	ASP_STP	ASP start phase. Controls which LRCK/FSYNC phase starts a frame. See Section 4.5.5 for details. 0 The frame begins when LRCK/FSYNC transitions from high to low 1 (Default) The frame begins when LRCK/FSYNC transitions from low to high
3	ASP_5050	ASP LRCK fixed 50/50 duty cycle. Determines whether the duty cycle is fixed or programmable. See Section 4.5.5 for details. 0 (Default) Programmable duty cycle. Determined by FSYNC_PULSE_WIDTH_LB (see p. 65), FSYNC_PULSE_WIDTH_UB, and FSYNC_PERIOD_xSB (see p. 66). 1 50/50 Mode. Fixed 50% duty cycle
2:0	ASP_FSD	ASP frame-start delay. Determines the delay before the start of an ASP frame in ASP_SCLK periods. See Section 4.5.2. 000 (Default) 0 delay 001 0.5 delay 010 1.0 delay … 101 2.5 delay 110–111 Reserved

7.3.8 FS Rate Enable

Address 0x1209

	7	6	5	4	3	2	1	0
R/W	—						FS_EN	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2:0	FS_EN	Fs rate enable. Provides enables for all internally generated Fs rates. 0 = disabled; 1 = enabled. Section 4.6 gives details. FS_EN[0] Enable IASRC 96K and lower rates. FS_EN[2] Enable IASRC 192, 176.4, and 176.471 K rates 00 (Default) All disabled

7.3.9 Input ASRC Clock Select

Address 0x120A

	7	6	5	4	3	2	1	0
R/W	—						CLK_IASRC_SEL	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	CLK_IASRC_SEL	Input ASRC clock select. Selects input ASRC $MCLK_{INT}$ frequency. See Section 4.6 for programming details. 00 (Default) 6 MHz 01 12 MHz 10 24 MHz 11 Reserved

7.3.10 PLL Divide Configuration 1

Address 0x120C

	7	6	5	4	3	2	1	0
R/W	—					PLL_REF_INV	SCLK_PREDIV	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	PLL_REF_INV	Invert PLL reference clock. See Table 4.4.3 for programming guidelines. 0 (Default) Normal 1 Inverted
1:0	SCLK_PREDIV	PLL reference divide select. See Table 4.4.3 for programming guidelines. 00 (Default) Divide by 1 01 Divide by 2 10 Divide by 4 11 Divide by 8

7.4 Interrupt Registers

7.4.1 Channel Overflow Interrupt Status

Address 0x1302

	7	6	5	4	3	2	1	0
R/O	—						CHA_OVFL	CHB_OVFL
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:2	—	Reserved
1	CHA_OVFL	Channel overflow. Indicates the overrange status in the corresponding signal path. Rising-edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask bit. 0 No digital clipping has occurred in the data path of the respective signal source. 1 Digital clipping has occurred in the data path of the respective signal source.
0	CHB_OVFL	

7.4.2 SRC Interrupt Status

Address 0x1303

	7	6	5	4	3	2	1	0
R/O	—					SRC_IUNLK	—	SRC_ILK
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:3	—	Reserved
2	SRC_IUNLK	SRC unlock status. Indicates SRC unlock status for the input path. Status is valid only if serial-port LRCK is toggling. 0 Locked 1 Unlocked
1	—	Reserved
0	SRC_ILK	SRC lock status. Indicates SRC lock status for the ASP input path. Status is valid only if serial-port LRCK is toggling. 0 Unlocked 1 Locked

7.4.3 ASP RX Interrupt Status

Address 0x1304

	7	6	5	4	3	2	1	0
R/O	—			ASPRX_OVLD	ASPRX_ERROR	ASPRX_LATE	ASPRX_EARLY	ASPRX_NOLRCK
Default	0	0	0	x	x	x	x	x

Bits	Name	Description
7:5	—	Reserved
4	ASPRX_OVLD	ASP RX request overload. Set when too many input buffers request processing at once. 0No interrupt 1 Interrupt detected. ASP RX cannot retrieve data from the internal input buffers because at least one of the following violations has occurred: —The ASP RX core clock frequency is less than SCLK/8. —The LRCK frame (non-50/50 Mode) or LRCK subframe (50/50 Mode) period is less than 16 SCLK periods (assuming the ASP RX core clock frequency is equal to SCLK/8).
3	ASPRX_ERROR	ASP RX LRCK error. Logical OR of ASPRX_LATE and ASPRX_EARLY, described below. 0 No interrupt 1 Interrupt detected
2	ASPRX_LATE	ASP RX LRCK late. Determines whether the number of SCLK periods per LRCK phase (high or low) is greater than the expected count, as determined by the FSYNC_PERIOD_xSB and FSYNC_PULSE_WIDTH_x fields. 0 No interrupt 1 Interrupt detected
1	ASPRX_EARLY	ASP RX LRCK early. Determines whether the number of SCLK periods per LRCK phase (high or low) is less than the expected count, as determined by FSYNC_PERIOD_xSB (see p. 66) and FSYNC_PULSE_WIDTH_x (see p. 65). 0 No interrupt 1 Interrupt detected
0	ASPRX_NOLRCK	ASP RX no LRCK. Determines whether the SCLK periods counted exceeds twice the value of LRCK period (FSYNC_PERIOD_xSB) without an LRCK edge. 0 No interrupt 1 Interrupt detected

7.4.4 DAC Interrupt Status

Address 0x1308

	7	6	5	4	3	2	1	0
R/O	—							PDN_DONE
Default	0	0	0	0	0	0	0	x

Bits	Name	Description
7:1	—	Reserved
0	PDN_DONE	Power-down done. Indicates when the DAC has powered down and MCLK can be stopped, as determined by various power-control and headset-interface register settings. 0 Not completely powered down 1 Powered down as a result of PDN_ALL having been set.

7.4.5 Detect Interrupt Status 1

Address 0x1309

	7	6	5	4	3	2	1	0
R/O	—	TIP_SENSE_PLUG	TIP_SENSE_UNPLUG			—		
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7	—	Reserved
6	TIP_SENSE_PLUG	Tip sense plug event. Indicates the undebounced status of a plug event on the TIP_SENSE pin.[1] 0 No HP plug event 1 HP plug event
5	TIP_SENSE_UNPLUG	Tip sense unplug event. Indicates the undebounced status of an unplug event on the TIP_SENSE pin.[1] 0 (Default) No HP unplug event 1 HP unplug event
4:0	—	Reserved

1. It is active only if TIP_SENSE_CTRL (p. 75) is configured so the tip-sense circuit is powered up. If the system is configured for standby operation, the sticky version of this bit (that also accounts for events that occurred during standby) can be read back after a wake event.

7.4.6 SRC Partial Lock Interrupt Status

Address 0x130B

	7	6	5	4	3	2	1	0
R/O	—	DAC_UNLK		—		DAC_LK		—
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7	—	Reserved
6	DAC_UNLK	ASP input SRC unlock status. 0 Locked 1 Unlocked
5:3	—	Reserved
2	DAC_LK	ASP input partial SRC lock status. 0 Unlocked 1 Locked
1:0	—	Reserved

7.4.7 VP Monitor Interrupt Status

Address 0x130D

	7	6	5	4	3	2	1	0
R/O	—							VPMON_TRIP
Default	0	0	0	0	0	0	0	x

Bits	Name	Description
7:1	—	Reserved
0	VPMON_TRIP	VP monitor interrupt. If the VP power supply falls below 2.6 V, this bit is set. See Section 4.9.1 for details. 0 No interrupt 1 Interrupt detected

7.4.8 PLL Lock Interrupt Status

Address 0x130E

	7	6	5	4	3	2	1	0
R/O	—							PLL_LOCK
Default	0	0	0	0	0	0	0	x

Bits	Name	Description
7:1	—	Reserved
0	PLL_LOCK	PLL lock. Indicates the lock state of the PLL. 0 No interrupt 1 Interrupt detected

7.4.9 Tip Sense Plug/Unplug Interrupt Status

Address 0x130F

	7	6	5	4	3	2	1	0
R/O	—				TS_UNPLUG	TS_PLUG	–	
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:4	—	Reserved
3	TS_UNPLUG	Tip sense unplug status. See Section 4.8.3 for details. Setting TS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
2	TS_PLUG	Tip sense plug status. See Section 4.8.3 for details. Setting TS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
1:0	—	Reserved

7.4.10 Mixer Interrupt Mask

Address 0x1317

	7	6	5	4	3	2	1	0
R/W	—						M_CHA_OVFL	M_CHB_OVFL
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:2	—	Reserved
1	M_CHA_OVFL	CHx_OVFL mask. 0 Unmasked 1 (Default) Masked
0	M_CHB_OVFL	

7.4.11 SRC Interrupt Mask

Address 0x1318

	7	6	5	4	3	2	1	0
R/W	—					M_SRC_IUNLK	—	M_SRC_ILK
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:3	—	Reserved
2	M_SRC_IUNLK	SRC_IUNLK mask. 0 Unmasked 1 (Default) Masked
1	—	Reserved
0	M_SRC_ILK	SRC_ILK mask. 0 Unmasked 1 (Default) Masked

7.4.12 ASP RX Interrupt Mask

Address 0x1319

R/W	7	6	5	4	3	2	1	0
	—			M_ASPRX_OVLD	M_ASPRX_ERROR	M_ASPRX_LATE	M_ASPRX_EARLY	M_ASPRX_NOLRCK
Default	0	0	0	1	1	1	1	1

Bits	Name	Description
7:5	—	Reserved
4	M_ASPRX_OVLD	ASPRX_OVFL mask. 0 Unmasked 1 (Default) Masked
3	M_ASPRX_ERROR	ASPRX_ERROR mask. 0 Unmasked 1 (Default) Masked
2	M_ASPRX_LATE	ASPRX_LATE mask. 0 Unmasked 1 (Default) Masked
1	M_ASPRX_EARLY	ASPRX_EARLY mask. 0 Unmasked 1 (Default) Masked
0	M_ASPRX_NOLRCK	ASPRX_NOLRCK mask. 0 Unmasked 1 (Default) Masked

7.4.13 DAC Interrupt Mask

Address 0x131B

R/W	7	6	5	4	3	2	1	0
	—							M_PDN_DONE
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:1	—	Reserved
0	M_PDN_DONE	PDN_DONE mask. 0 Unmasked 1 (Default) Masked

7.4.14 SRC Partial Lock Interrupt Mask

Address 0x131C

R/W	7	6	5	4	3	2	1	0
	—	M_DAC_UNLK	—			M_DAC_LK	—	
Default	0	1	1	1	1	1	1	1

Bits	Name	Description
7	—	Reserved
6	M_DAC_UNLK	ASP input unlock mask. 0 Unmasked 1 (Default) Masked
5–3	—	Reserved
2	M_DAC_LK	ASP input lock mask. 0 Unmasked 1 (Default) Masked
1:0	—	Reserved

7.4.15 VP Monitor Interrupt Mask

Address 0x131E

R/W	7	6	5	4	3	2	1	0
	—							M_VPMON_TRIP
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	M_VPMON_TRIP	VP monitor mask. 0 Unmasked. Unmask/enable this bit only when VP exceeds the detection voltage threshold; applicable to power-up conditions or if VP is not at its steady-state voltage. 1 (Default) Masked

7.4.16 PLL Lock Mask

Address 0x131F

R/W	7	6	5	4	3	2	1	0
	—							M_PLL_LOCK
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	M_PLL_LOCK	PLL lock mask. 0 Unmasked 1 (Default) Masked

7.4.17 Tip Sense Plug/Unplug Interrupt Mask

Address 0x1320

R/W	7	6	5	4	3	2	1	0
	—				M_TS_UNPLUG	M_TS_PLUG	—	
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:4	—	Reserved
3	M_TS_UNPLUG	Tip sense unplug mask. 0 Unmasked 1 (Default) Masked
2	M_TS_PLUG	Tip sense plug mask. 0 Unmasked 1 (Default) Masked
1:0	—	Reserved

7.5 Fractional-N PLL Registers

7.5.1 PLL Control 1

Address 0x1501

R/W	7	6	5	4	3	2	1	0
	—							PLL_START
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	PLL_START	PLL start. If MCLK_SRC_SEL = 0, the PLL is bypassed and can be powered down by clearing PLL_START. See Section 4.4.3. 0 (Default) Powered off. 1 Powered on

7.5.2 PLL Division Fractional Bytes 0–2

Address 0x1502–0x1504

R/W	7	6	5	4	3	2	1	0
0x1502	PLL_DIV_FRAC[7:0]							
0x1503	PLL_DIV_FRAC[15:8]							
0x1504	PLL_DIV_FRAC[23:16]							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_FRAC[7:0]	PLL fractional portion of divide ratio LSB. See Section 4.4.3 for details. There are 3 bytes of PLL feedback divider fraction portion: This is LSB byte; e.g., 0xFF means ($2^{-17} + 2^{-18} + \ldots +2^{-24}$) 0000 0000 (Default)
7:0	PLL_DIV_FRAC[15:8]	PLL fractional portion of divide ratio middle byte; e.g., 0xFF means ($2^{-9} + 2^{-10} + \ldots +2^{-16}$). See Section 4.4.3 for details. 0000 0000 (Default)
7:0	PLL_DIV_FRAC[23:16]	PLL fractional portion of divide ratio MSB; e.g., 0xFF means ($2^{-1} + 2^{-2} + \ldots +2^{-8}$). See Section 4.4.3 for details. 0000 0000 (Default)

7.5.3 PLL Division Integer

Address 0x1505

R/W	7	6	5	4	3	2	1	0
	PLL_DIV_INT							
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_INT	PLL integer portion of divide ratio. Integer portion of PLL feedback divider. See Section 4.4.3 for details. 0100 0000 (Default)

7.5.4 PLL Control 3

Address 0x1508

R/W	7	6	5	4	3	2	1	0
	PLL_DIVOUT							
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:0	PLL_DIVOUT	Final PLL clock output divide value. See Section 4.4.3 for configuration details. 0001 0000 (Default)

7.5.5 PLL Calibration Ratio

Address 0x150A

R/W	7	6	5	4	3	2	1	0
	PLL_CAL_RATIO							
Default	1	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_CAL_RATIO	PLL calibration ratio. See Section 4.4.3 for configuration details. Target value for PLL VCO calibration. 1000 0000 (Default)

7.5.6 PLL Control 4

Address 0x151B

R/W	7	6	5	4	3	2	1	0
	—						PLL_MODE	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	PLL_MODE	PLL bypass mode. Configures 500/512 and 1029/1024 factor bypasses. See Section 4.4.3 for configuration details. 00 Unsupported 01 500/512 only (1029/1024 bypassed) 10 1029/1024 only (500/512 bypassed) 11 (Default) Both bypassed

7.6 HP Load-Detect Registers

7.6.1 Load-Detect R/C Status

Address 0x1925

	7	6	5	4	3	2	1	0
R/O	—			CLA_STAT	—		RLA_STAT	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
4	CLA_STAT	Capacitor load-detection result for HPA. See Section 4.2.2 for details. **Note:** Low capacitance results were determined with C_L = 1 nF; high capacitance results were determined with C_L = 10 nF. 0 (Default) High capacitance ($C_L \geq$ ~2 nF) 1 Low capacitance ($C_L <$ ~2 nF)
1:0	RLA_STAT	Resistor load-detection result for HPA. See Section 4.2.2 for details. 00 (Default) 15 Ω 10 3 kΩ 01 30 Ω 11 Reserved

7.6.2 HP Load Detect Done

Address 0x1926

	7	6	5	4	3	2	1	0
R/O	—							HPLOAD_DET_DONE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	HPLOAD_DET_DONE	HP load detect done. Indicates whether HP load detection is finished. See Section 4.2.2 for details. 0 (Default) HP load is not finished. 1 HP load is finished.

7.6.3 HP Load Detect Enable

Address 0x1927

	7	6	5	4	3	2	1	0
R/O	—							HP_LD_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	HP_LD_EN	HP load detect enable. A 0-to-1 bit transition initiates load detection. See Section 4.2.2 for details. 0 (Default) Disabled 1 Enabled

7.7 Headset Interface Registers

7.7.1 Wake Control

Address 0x1B71

	7	6	5	4	3	2	1	0
R/W	—	M_HP_WAKE	WAKEB_MODE		—			WAKEB_CLEAR
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6	M_HP_WAKE	Mask tip sense wake.[1] Configures the mask for the tip-sense wake status. 0 Unmasked. The occurrence of a wake interrupt affects $\overline{\text{WAKE}}$. Before unmasking, pending wake events must be cleared via WAKEB_CLEAR. 1 (Default) Masked. The occurrence of a wake interrupt does not affect $\overline{\text{WAKE}}$.
5	WAKEB_MODE	$\overline{\text{WAKE}}$ output mode.[1] Configures the mode of operation for the $\overline{\text{WAKE}}$ output 0 (Default) Output is latched low after a trigger event until WAKEB_CLEAR is toggled. 1 Output follows the combination logic directly (nonlatched).
4:1	—	Reserved

Bits	Name	Description
0	WAKEB_CLEAR	$\overline{\text{WAKE}}$ output clear. Applicable only if WAKEB_MODE = 0 and an event triggers the $\overline{\text{WAKE}}$ output to latch low. 0 (Default) $\overline{\text{WAKE}}$ output normal operation. If WAKEB_MODE = 1, WAKEB_CLEAR does not deassert $\overline{\text{WAKE}}$, but clears TIP_SENSE_PLUG, TIP_SENSE_UNPLUG in the VP domain. 1 $\overline{\text{WAKE}}$ output deasserted (the TIP_SENSE_PLUG, TIP_SENSE_UNPLUG bits in the VP domain are also cleared).

1.This bit can be changed only if LATCH_TO_VP is enabled (see p. 75).

7.7.2 Tip Sense Control 2

Address 0x1B73

R/W	7	6	5	4	3	2	1	0
	TIP_SENSE_CTRL		TIP_SENSE_INV		—		TIP_SENSE_DEBOUNCE	
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:6	TIP_SENSE_CTRL	Tip sense control.Configures operation of the tip-sense circuit. **Note:** This bit can be updated only if LATCH_TO_VP (see p. 75) is enabled. 00 (Default) Disabled. The tip-sense circuit is powered down and does not report to the status registers (TIP_SENSE_PLUG and TIP_SENSE_UNPLUG in the VP domain are also cleared). 01 Digital input. Internal weak current source pull-up is disabled. 10 Reserved 11 Short detect. Internal weak current source pull-up is enabled.
5	TIP_SENSE_INV	Tip sense invert. Used to invert the signal from the tip-sense circuit. Updatable only if LATCH_TO_VP is enabled. 0 (Default) Not inverted 1 Inverted
4:2	—	Reserved
1:0	TIP_SENSE_DEBOUNCE	Tip sense debounce time. Sets tip sense unplug event (TIP_SENSE = 0) debounce time before status is reported. Timings are approximate and vary with $MCLK_{INT}$ and Fs_{INT}. 00 No debounce 01 200 ms 10 (Default) 500 ms 11 1000 ms

7.7.3 Mic Detect Control 1

Address 0x1B75

R/W	7	6	5	4	3	2	1	0
	LATCH_TO_VP	EVENT_STATUS_SEL			—			
Default	0	0	0	1	1	1	1	1

Bits	Name	Description
7	LATCH_TO_VP	Latch to VP registers. Controls the transfer of writable control registers in the VD_FILT supply domain to duplicate registers in the VP supply domain. Can be used to enable setting sticky status bits in the VP domain. 0 (Default) Inhibits the transfer of VD_FILT registers to VP registers (latched mode). Enables the setting of VP sticky status latches. 1 Transfers VD_FILT fields to VP fields (transparent mode). Disables setting of VP sticky status latches. Affected registers: • TIP_SENSE_CTRL on p. 75 • M_HP_WAKE on p. 74 • WAKEB_MODE p. 74 • TIP_SENSE_INV on p. 75 **Note:** The description of PDN_ALL on p. 63 describes the interdependency between LATCH_TO_VP and PDN_ALL.
6	EVENT_STATUS_SEL	Event status selection. Selects the level of processing on readable status originating in the VP supply domain. 0 (Default) Raw (unprocessed) status events are selected. 1 Sticky processed status events are selected. Affected registers: • TIP_SENSE_PLUG on p. 69 • • TIP_SENSE_UNPLUG on p. 69
5:0	—	Reserved

7.7.4 Detect Status 1

Address 0x1B77

R/O	7	6	5	4	3	2	1	0
	TIP_SENSE	—						
Default	x	x	0	x	x	x	x	x

Bits	Name	Description
7	TIP_SENSE	TIP_SENSE circuit status. The plug-to-unplug edge is debounced for the set debounce time (see TIP_SENSE_DEBOUNCE, p. 75). 0 HP not plugged in 1 HP plugged in
6:0	—	Reserved

7.7.5 Detect Interrupt Mask 1

Address 0x1B79

R/W	7	6	5	4	3	2	1	0
	—	M_TIP_SENSE_PLUG	M_TIP_SENSE_UNPLUG	—				
Default	1	1	1	0	0	0	0	0

Interrupt mask register bits serve as a mask for the interrupt sources in the interrupt status registers. Interrupts are described in Section 4.12.

Bits	Name	Description
7	—	Reserved
6	M_TIP_SENSE_PLUG	TIP_SENSE_PLUG mask 0 Unmasked 1 (Default) Masked
5	M_TIP_SENSE_UNPLUG	TIP_SENSE_UNPLUG mask 0 Unmasked 1 (Default) Masked
4:0	—	Reserved

7.8 DAC Control Registers

7.8.1 DAC Control 1

Address 0x1F01

R/W	7	6	5	4	3	2	1	0
	—						DACB_INV	DACA_INV
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	DACx_INV	DACx invert signal polarity. Configures the polarity of the DAC channel x signal. See Section 4.2 for details. 0 (Default) Not inverted 1 Inverted

7.8.2 DAC Control 2

Address 0x1F06

R/W	7	6	5	4	3	2	1	0
	HPOUT_PULLDOWN				HPOUT_LOAD	HPOUT_CLAMP	DAC_HPF_EN	—
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:4	HPOUT_PULLDOWN	Although bits 2:0 are independent, the final resistance from the resistor string is dictated by the lowest resistance chosen; e.g., if HPOUT_PULLDOWN = 1011, a nominal 6-kΩ pull-down resistance results even if 9.6-kΩ resistance is also selected. 0000 (Default) 0.9 kΩ 0001–0111 0.9 kΩ 1000 No pulldown 1001 9.3 kΩ 1010 5.8 kΩ 1011 Reserved 1100 0.9 kΩ 1101–1111 Reserved
3	HPOUT_LOAD	HP output load. Sets HP amplifier capacitive load capability. Table 3-7 gives output specifications. See Section 4.2 for details. 0 (Default) 1 nF Mode 1 10 nF Mode **Note:** The HP path must be powered down before reconfiguring this bit and repowered afterwards. See Section 4.2.2.

Bits	Name	Description
2	HPOUT_CLAMP	HPOUT clamp. Configures an override of the HPOUT clamp to ground when the channels are powered down. 0 (Default) Clamp to ground when channels are powered down. 1 Clamp is disabled when the channels are powered down. The pulldown to GNDA depends on the HPOUT_PULLDOWN setting.
1	DAC_HPF_EN	DAC high-pass filter enable. Configures the internal HPF before DAC. Changes to this bit must be made only if PDN_ALL = 1. See Section 4.2 for details. 0 Disabled. This must be cleared only for test purposes. 1 (Default) Enabled. The corner frequency is set to 0.935 Hz when Fs_{INT} = 48 kHz.
0	—	Reserved

7.9 HP Control Register

7.9.1 HP Control

Address 0x2001

R/W	7	6	5	4	3	2	1	0
	—				ANA_MUTE_B	ANA_MUTE_A	FULL_SCALE_VOL	—
Default	0	0	0	0	1	1	0	1

Bits	Name	Description
7:4	—	Reserved
3	ANA_MUTE_B	Analog mute Channel B. See Section 4.2 for details. 0 Unmuted 1 (Default) Muted
2	ANA_MUTE_A	Analog mute Channel A. See Section 4.2 for details. 0 Unmuted 1 (Default) Muted
1	FULL_SCALE_VOL	Full-scale volume. Determines the maximum volume for the headphone output. See Section 4.2 for details. 0 (Default) 0 dB 1 –6 dB. This setting is recommended if the load is approximately 15 Ω.
0	—	Reserved

7.10 Class H Register

7.10.1 Class H Control

Address 0x2101

R/W	7	6	5	4	3	2	1	0
	—					ADPTPWR		
Default	0	0	0	0	0	1	1	1

Bits	Name	Description
7:3	—	Reserved
2:0	ADPTPWR	Adaptive power adjustment. Configures how power to HP output amplifiers adapts to the output signal level. Section 4.2 gives detailed descriptions of supported settings. 000 Reserved 001 Fixed, Mode 0—VP_CP Mode (±2.5V) 010 Fixed, Mode 1—VCP Mode (±VCP) 011 Fixed, Mode 2 —VCP/2 Mode (±VCP/2) 100 Fixed, Mode 3 —VCP/3 Mode (±VCP/3) 101–110 Reserved 111 (Default) Adapt to signal. The output signal dynamically determines the voltage level.

7.11 Volume Control

7.11.1 Channel A Input Volume

Address 0x2301

R/W	7	6	5	4	3	2	1	0
	—		CHA_VOL					
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:6	—	Reserved
5:0	CHA_VOL	Input attenuation. Sets the attenuation level to be applied to various stereo digital inputs. See Section 4.1 for details. Each input can be muted or attenuated from –62 to 0 dB in 1-dB steps. 00 0000 0 dB 00 0001 –1.0 dB … 11 1110 –62.0 dB 11 1111 (Default) Mute.

7.11.2 Channel B Input Volume

Address 0x2303

	7	6	5	4	3	2	1	0
R/W	—		CHB_VOL					
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:6	—	Reserved
5:0	CHB_VOL	Input attenuation. Sets the attenuation level to be applied to various stereo digital inputs. See Section 4.1 for details. Each input can be muted or attenuated from –62 to 0 dB in 1-dB steps. 00 0000 0 dB 11 1110 –62.0 dB 00 0001 –1.0 dB … 11 1111 (Default) Mute.

7.12 AudioPort Interface Registers

7.12.1 Serial Port Receive Channel Select

Address 0x2501

	7	6	5	4	3	2	1	0
R/W	—				SP_RX_CHB_SEL		SP_RX_CHA_SEL	
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:4	—	Reserved
3:2	SP_RX_CHB_SEL	SP RX Channel B select for DAI0. Selects right input channel. See Section 5 for programming examples. 00 Channel 0 01 (Default) Channel 1 10 Channel 2 11 Channel 3
1:0	SP_RX_CHA_SEL	SP RX Channel A select for DAI0. Selects right input channel. 00 (Default) Channel 0 01 Channel 1 10 Channel 2 11 Channel 3

7.12.2 Serial Port Receive Isochronous Control

Address 0x2502

	7	6	5	4	3	2	1	0
R/W	—	SP_RX_RSYNC	SP_RX_NSB_POS			SP_RX_NFS_NSBB	SP_RX_ISOC_MODE	
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7	—	Reserved
6	SP_RX_RSYNC	Serial port receive synchronization. 0 (Default) Normal state 1 Recenter the FIFO. No read and writes when asserted
5:3	SP_RX_NSB_POS	Serial-port receive null-sample bit position. Selects the position of the null byte in the resultant 16-, 24-, or 32-bit sample. For all samples, if SP_RX_ISOC_MODE ≠ 00, SP_RX_NFS_NSBB = 0, the following applies: • For a 16-bit sample (8-bit audio + null byte), [23:16] is the null byte. • For a 24-bit sample (16-bit audio + null byte), [15:8] is the null byte. • For a 32-bit sample (24-bit audio + null byte), [7:0] is the null byte. **Note:** NSB Mode does not support 32-bit audio samples. The ASP_RXn_CHn_RES fields in Section 7.14 set the output resolution of the ASP receive channel samples. Clearing SP_RX_NSB_POS indicates that Bit 0 must be zero for the sample to be classified as a null. 000 (Default) 0 … 111 7
2	SP_RX_NFS_NSBB	Serial-port receive NSB/NFS Mode select. 0 NSB Mode valid only if SP_RX_ISOC_MODE ≠ 00. 1 (Default) NFS Mode
1:0	SP_RX_ISOC_MODE	Serial port receive isochronous mode. Selecting an isochronous mode allows for null removal. The ASP Rx rate bits (SP_RX_FS, see p. 79) are used only to help the device determine when to insert nulls. 00 (Default) Native mode 10 96k isochronous stream 01 48k isochronous stream 11 192k isochronous stream

7.12.3 Serial Port Receive Sample Rate

Address 0x2503

	7	6	5	4	3	2	1	0
R/W	—				SP_RX_FS			
Default	1	0	0	0	1	1	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	SP_RX_FS	SP receive sample rate. Configures the sample rate of the SRC F_{SI} when in Isochronous Mode. This setting autoscales when configuring for a isochronous rate of 96 or 192 kHz with respect to the 48-kHz isochronous rate, e.g., 24-kHz setting in isochronous rate of 48 kHz would be scaled to a 48-kHz setting in isochronous rate of 96 kHz. 0 0000 Reserved, 0 0100 12.000 kHz, 0 1000 24.000 kHz, 0 1100 (Default) 48.000 kHz, 1 0000 176.400 kHz 0 0001 8.00 kHz, 0 0101 16.000 kHz, 0 1001 32.000 kHz, 0 1101 88.200 kHz, 1 0001 176.472 kHz 0 0010 11.025 kHz, 0 0110 22.050 kHz, 0 1010 44.100 kHz, 0 1110 88.236 kHz, 1 0010 192.000 kHz 0 0011 11.0295 kHz, 0 0111 22.059 kHz, 0 1011 44.118 kHz, 0 1111 96.000 kHz, 1 0011–1 1111 Reserved

7.13 SRC Registers

7.13.1 SRC Input Sample Rate

Address 0x2601

	7	6	5	4	3	2	1	0
R/W	—				SRC_SDIN_FS			
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	SRC_SDIN_FS	SRC input sample rate. Must equal Fs_{INT} if SRC_BYPASS_DAC = 1. 0 0000 (Default) Don't know, 0 0100 12.000 kHz, 0 1000 24.000 kHz, 0 1100 48.000 kHz, 1 0000 176.400 kHz 0 0001 8.00 kHz, 0 0101 16.000 kHz, 0 1001 32.000 kHz, 0 1101 88.200 kHz, 1 0001 176.472 kHz 0 0010 11.025 kHz, 0 0110 22.050 kHz, 0 1010 44.100 kHz, 0 1110 88.236 kHz, 1 0010 192.000 kHz 0 0011 11.0295 kHz, 0 0111 22.059 kHz, 0 1011 44.118 kHz, 0 1111 96.000 kHz, 1 0011–1 1111 Reserved

7.14 Serial Port Receive Registers

7.14.1 ASP Receive Enable

Address 0x2A01

	7	6	5	4	3	2	1	0
R/W	—				ASP_RX0_CH2_EN	ASP_RX0_CH1_EN	—	ASP_RX0_2FS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:2	ASP_RX0_CH[2:1]_EN	ASP receive DAI0 enable. Determines whether the channel buffer gets populated. ASP_RX0_CH1_EN = Channel 1 ASP_RX0_CH2_EN = Channel 2 0 (Default) The corresponding channel buffer does not get populated. 1 The corresponding channel buffer is populated
1	—	Reserved
0	ASP_RX0_2FS	ASP receive DAI0 double-rate mode. 0 (Default) Standard sample rate, Fs (not doubled) 1 Sample rate is doubled, 2 Fs

7.14.2 ASP Receive DAI0 Channel 1 Phase and Resolution

Address 0x2A02

	7	6	5	4	3	2	1	0
R/W	—	ASP_RX0_CH1_AP			—		ASP_RX0_CH1_RES	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_RX0_CH1_AP	ASP receive DAI0 active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_RX0_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is valid if LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is valid when LRCK/FSYNC is high.

Bits	Name	Description
5:2	—	Reserved
1:0	ASP_RX0_CH1_RES	ASP Receive DAI0 channel bit width. Sets output resolution of the ASP receive DAI0 channel x samples. 00 8 bits per sample (only for isochronous NFS and native modes) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.14.3 ASP Receive DAI0 Channel 1 Bit Start MSB

Address 0x2A03

	7	6	5	4	3	2	1	0
R/W	—							ASP_RX0_CH1_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_RX0_CH1_BIT_ST_MSB	ASP receive DAI0 Channel 1 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.14.4 ASP Receive DAI0 Channel 1 Bit Start LSB

Address 0x2A04

	7	6	5	4	3	2	1	0
R/W	ASP_RX0_CH1_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX0_CH1_BIT_ST_LSB	ASP receive DAI0 Channel 1 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.14.5 ASP Receive DAI0 Channel 2 Phase and Resolution

Address 0x2A05

	7	6	5	4	3	2	1	0
R/W	—	ASP_RX0_CH2_AP	—				ASP_RX0_CH2_RES	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_RX0_CH2_AP	ASP receive DAI0 active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_RX0_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is input when LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is input when LRCK/FSYNC is high.
5:2	—	Reserved
1:0	ASP_RX0_CH2_RES	ASP receive DAI0 channel bit width. Sets the output resolution of the ASP receive DAI0 channel x samples. 00 8 bits per sample (valid only for isochronous NFS and native mode) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.14.6 ASP Receive DAI0 Channel 2 Bit Start MSB

Address 0x2A06

	7	6	5	4	3	2	1	0
R/W	—							ASP_RX0_CH2_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_RX0_CH2_BIT_ST_MSB	ASP receive DAI0 Channel 2 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.14.7 ASP Receive DAI0 Channel 2 Bit Start LSB

Address 0x2A07

	7	6	5	4	3	2	1	0
R/W	ASP_RX0_CH2_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX0_CH2_BIT_ST_LSB	ASP receive DAI0 Channel 2 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.15 ID Registers

7.15.1 Subrevision

Address 0x3014

	7	6	5	4	3	2	1	0
R/O	SUBREVISION							
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7:0	SUBREVISION	Subrevision. Identifies the CS43L36 subrevision. The Page 0x30 read sequence in Section 5.3 must be followed to read this register. 0000 0011 Initial version.

7.15.2 Device ID A and B

Address 0x3015

	7	6	5	4	3	2	1	0
R/O	DEVIDA				DEVIDB			
Default	0	1	0	0	0	0	1	1

7.15.3 Device ID C and D

Address 0x3016

	7	6	5	4	3	2	1	0
R/O	DEVIDC				DEVIDD			
Default	1	0	1	0	0	0	1	1

7.15.4 Device ID E

Address 0x3017

	7	6	5	4	3	2	1	0
R/O	DEVIDE				—			
Default	0	1	1	0	x	x	x	x

Bits	Name	Description
7:4	DEVIDA DEVIDC DEVIDE	Device ID code. Identifies the CS43L36. The Page 0x30 read sequence in Section 5.3 must be followed to read this register. DEVIDA 0x4 DEVIDB 0x3 DEVIDC 0xA Represents the “L” in the CS43L36. DEVIDD 0x3 DEVIDE 0x6
3:0	DEVIDB DEVIDD	

8 PCB Layout Considerations

The following sections provide general guidelines for PCB layout to ensure the best performance of the CS43L36.

8.1 Power Supply

As with any high-resolution converter, to realize its potential, the CS43L36 requires careful attention to power supply and grounding arrangements. Fig. 2-1 shows the recommended power arrangements, with VA and VCP connected to clean supplies. VL, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VL may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VL.

8.2 Grounding

Note the following:

- Extensive use of power and ground planes, ground-plane fill in unused areas, and surface-mount decoupling capacitors are recommended.
- Decoupling capacitors should be as close as possible to the CS43L36 pins.
- To minimize inductance effects, the low-value ceramic capacitor must be closest to the pin and mounted on the same side of the board as the CS43L36.
- To avoid unwanted coupling into the modulators, all signals, especially clocks, must be isolated from the FILT+ pin.
- The FILT+ capacitor must be positioned to minimize the electrical path from the pin to GNDA.
- The +VCP_FILT and –VCP_FILT capacitors must be positioned to minimize the electrical path from each respective pin to GNDCP.

8.3 QFN Thermal Pad

The CS43L36 comes in a compact QFN package, the underside of which reveals a large metal pad that serves as a thermal relief to provide maximum heat dissipation. This pad must mate with a matching copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. For best performance in split-ground systems, connect this thermal to GNDA.

9 Plots

9.1 Digital Filter Response

9.1.1 Highpass Filter—DAC

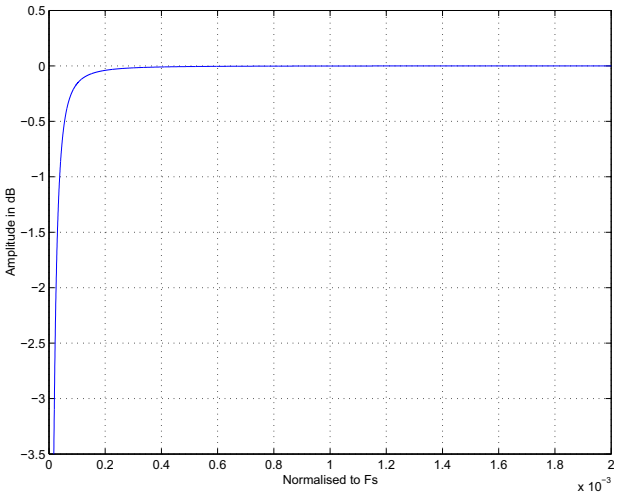


Figure 9-1. DAC HPF Response

9.1.2 DAC to HP, Fs_{int} = 44.118 kHz, MCLK = 136 x LRCK

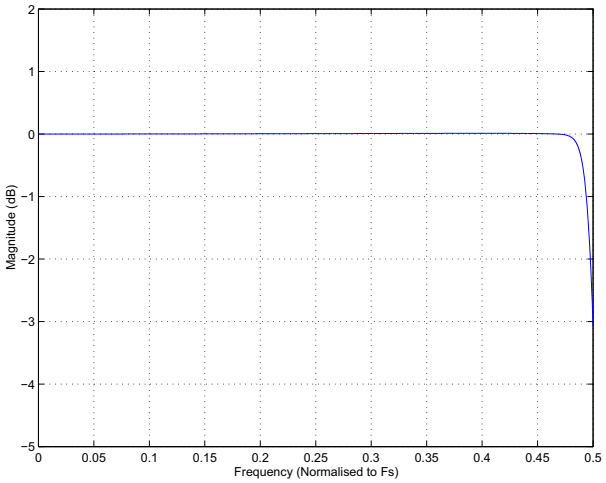


Figure 9-2. Passband—DAC, Fs_{int} = 44.118 kHz

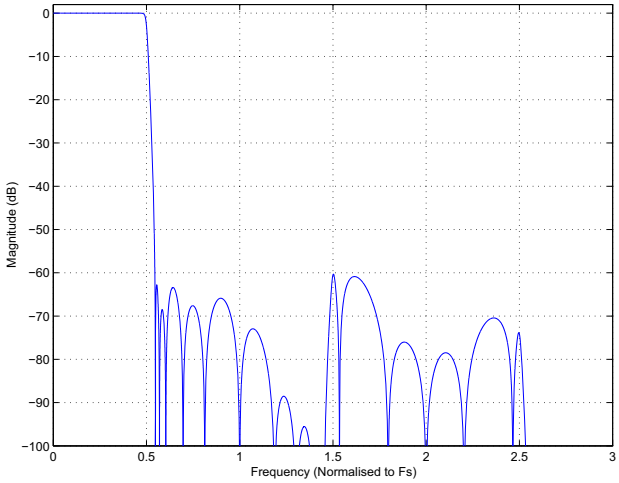


Figure 9-3. Stopband—DAC, Fs_{int} = 44.118 kHz

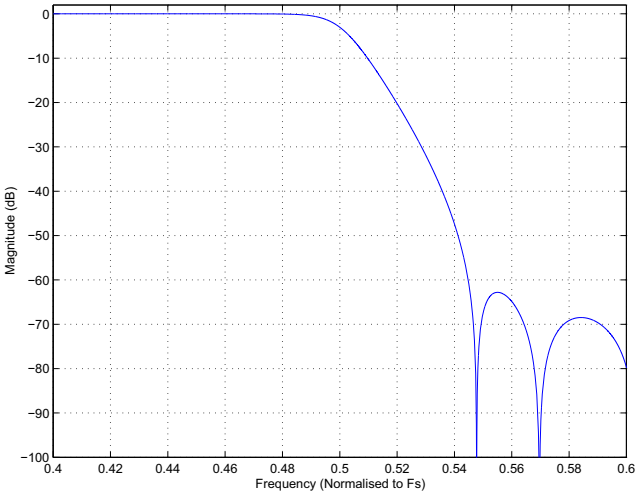


Figure 9-4. Transition Band—DAC, Fs_{int} = 44.118 kHz

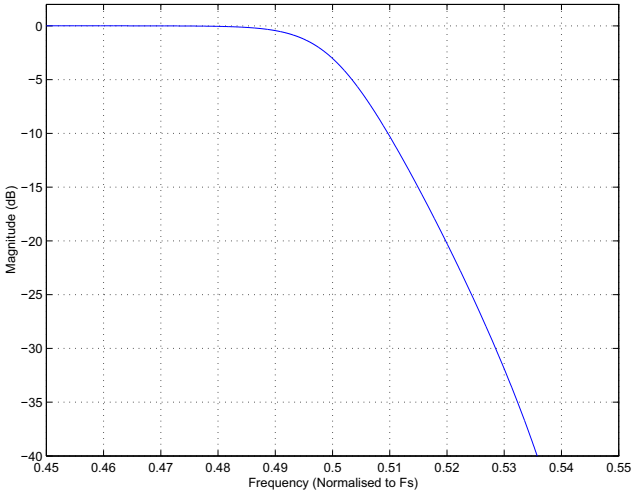


Figure 9-5. Transition Band (Detail)—DAC, Fs_{int} = 44.118 kHz

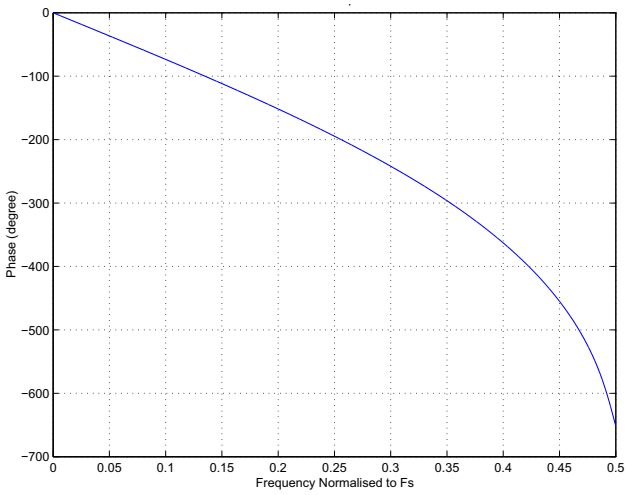


Figure 9-6. Phase Response—DAC, Fs_{int} = 44.118 kHz

9.1.3 DAC to HP, Fs_{int} = 48.000 kHz, MCLK = 125 x LRCK

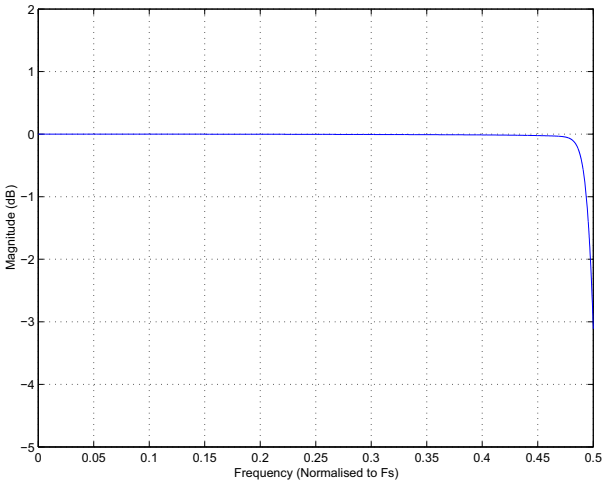


Figure 9-7. Passband—DAC, Fs_{int} = 48.000 kHz

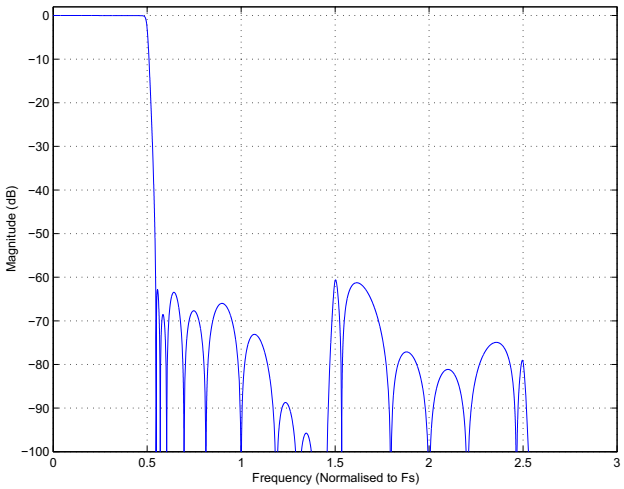


Figure 9-8. Stopband—DAC, Fs_{int} = 48.000 kHz

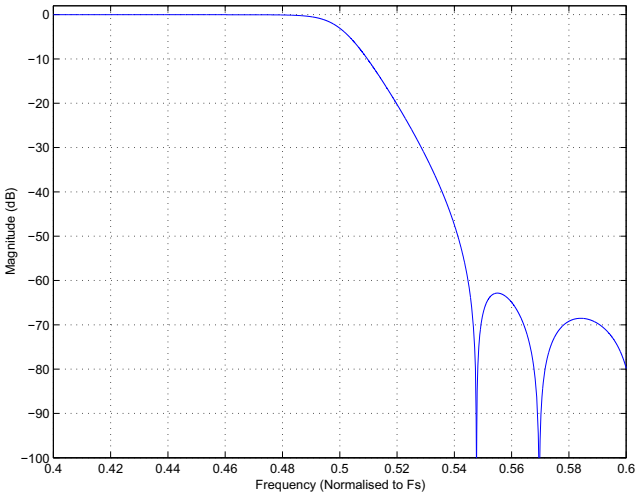


Figure 9-9. Transition Band—DAC, Fs_{int} = 48.000 kHz

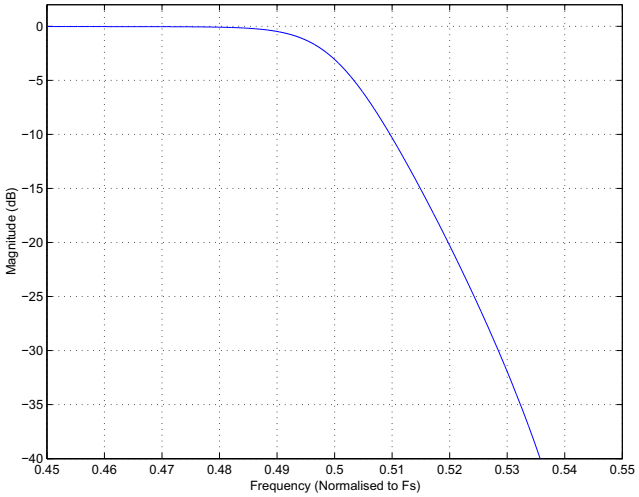


Figure 9-10. Transition Band (Detail)—DAC, Fs_{int} = 48.000 kHz

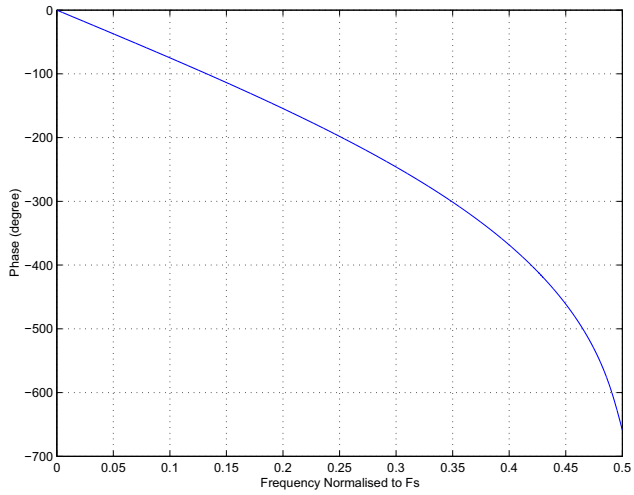


Figure 9-11. Phase Response—DAC, Fs_{int} = 48.000 kHz

9.1.4 SDIN ASRC, Fs_{INT} = 48 kHz

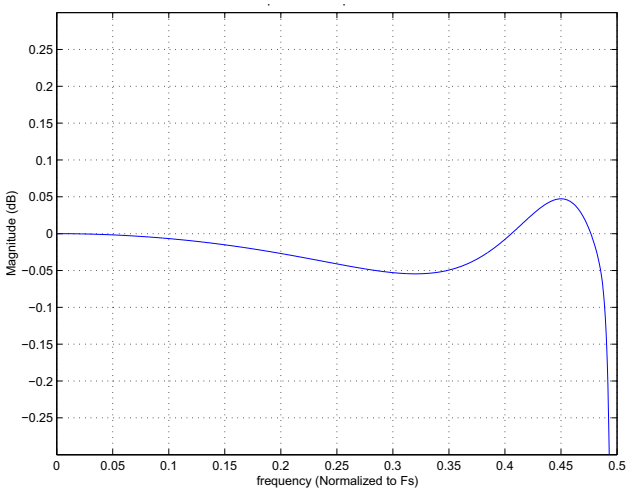


Figure 9-12. Passband—ASRC, Notch Disabled

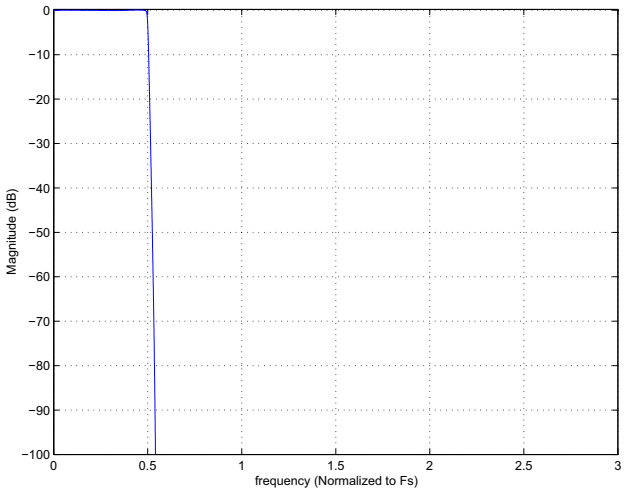


Figure 9-13. Stopband—ASRC, Notch Disabled

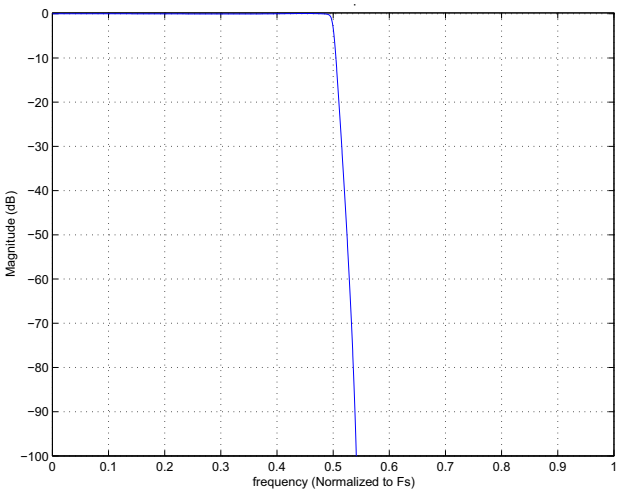


Figure 9-14. Transition Band—ASRC, Notch Disabled

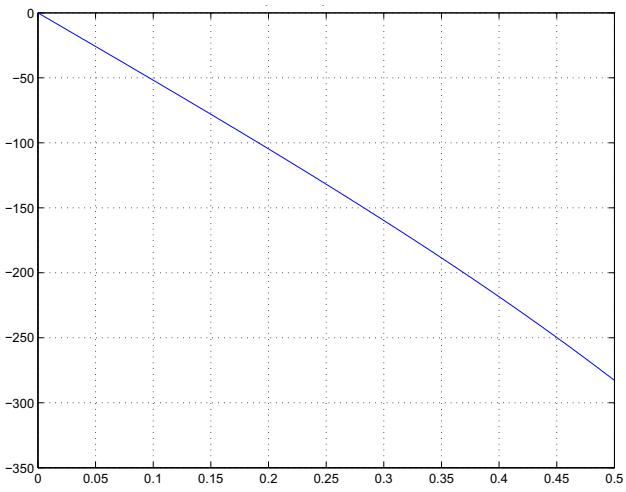
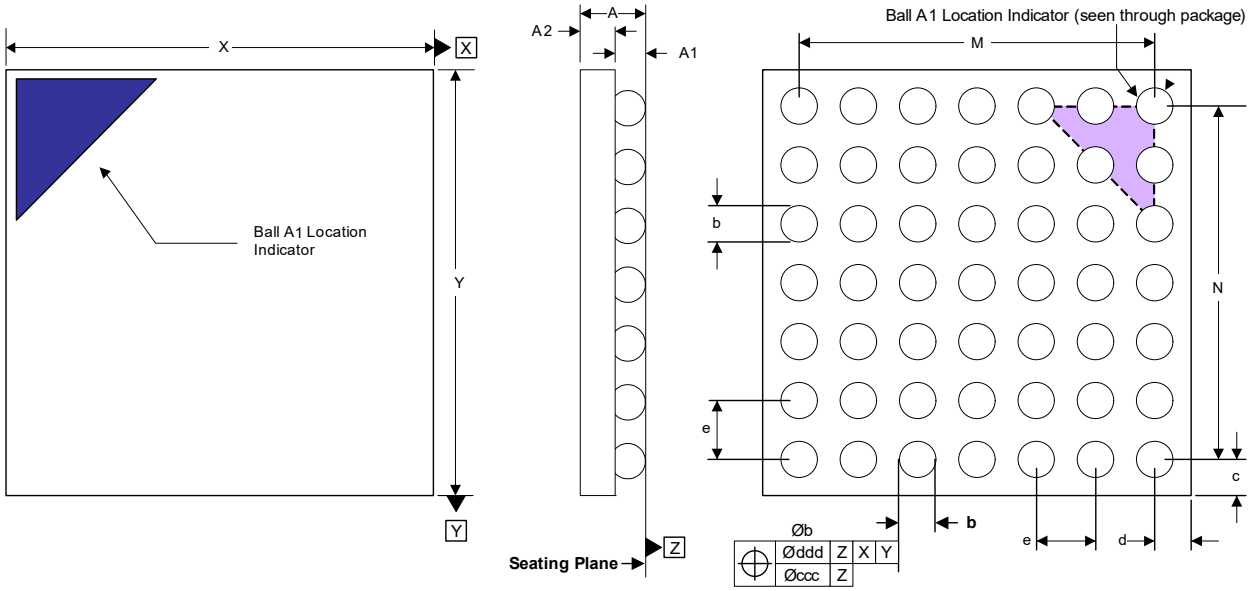


Figure 9-15. Phase Response—ASRC, Notch Disabled

10 Package Dimensions

10.1 WLCSP Package Dimensions



WAFER BACK SIDE SIDE VIEW BUMP SIDE

Notes:
- Dimensioning and tolerances per ASME Y 14.5M–1994.
- The Ball A1 position indicator is for illustration purposes only and may not be to scale.
- Dimension “b” applies to the solder sphere diameter and is measured at the maximum solder-ball diameter, parallel to primary Datum Z.

Table 10-1. WLCSP Package Dimensions

Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.443	0.474	0.505
A1	0.148	0.174	0.200
A2	0.284	0.300	0.316
M	BSC	2.100	BSC
N	BSC	2.100	BSC
b	0.225	0.250	0.300
c	REF	0.272	REF
d	REF	0.272	REF
e	BSC	0.350	BSC
X	2.614	2.644	2.674
Y	2.614	2.644	2.674
ccc = 0.015 ddd = 0.015			

Note: Controlling dimension is millimeters.

10.2 QFN Package Dimensions

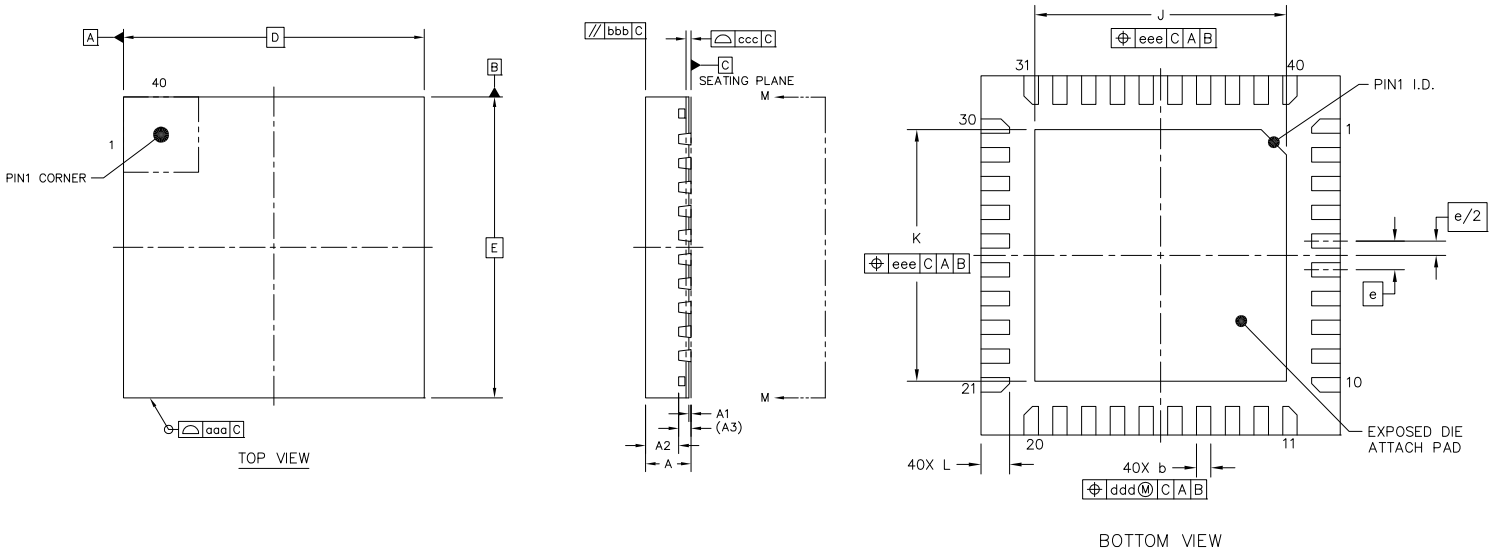


Table 10-2. QFN Package Dimensions

Dimension	mm		
	Minimum	Nominal	Maximum
A	0.7	0.75	0.8
A1	0.00	0.035	0.05
A2	—	0.55	0.67
A3		0.203 REF	
b	0.15	0.20	0.25
D		5.00 BSC	
K	3.4	3.5	3.6
e		0.40 BSC	
E		5.00 BSC	
J	3.4	3.5	3.6
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

11 Thermal Characteristics

Table 11-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter [1]	Symbol	QFN	WLCSP	Unit
Junction-to-ambient thermal resistance	θ_{JA}	35.0	52.0	°C/W
Junction-to-board thermal resistance	θ_{JB}	9.0	17.8	°C/W
Junction-to-case thermal resistance	θ_{JC}	0.98	0.15	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	8.9	17.7	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	0.19	0.04	°C/W

1. Thermal setup:
   Still air @ maximum allowed ambient temperature
   JEDEC 2s2p printed wiring board (JEDEC Standard JESD51-11, June 2001)
   Size: 114.5 x 101.5 x 1.6 mm

12 Ordering Information

Table 12-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Order #
CS43L36	Low-Power, High-Performance Audio DAC with Class H Headphone Drivers	40-pin QFN	Yes	Extended Commercial	–40 to +85°C	Tape and reel	CS43L36-CNZR
						Tray	CS43L36-CNZ
		49-ball WLCSP	Yes	Extended Commercial	–40 to +85°C	Tape and reel	CS43L36-CWZR

13 References

- NXP Semiconductors, UM10204 Rev. 06, April 2014, *The I²C-Bus Specification and User Manual*, http://www.nxp.com
- JEDEC Solid State Technology Association, *Guidelines for Reporting and Using Electronic Package Thermal Information*, *JEDEC Standard No. 51-12.01*, November 2012, http://www.jedec.org/

14 Revision History

Table 14-1. Revision History

Revision	Changes
F2 AUG '17	• Changed references to VD to VD_FILT in Section 5.5. • Updated VL/VD_FILT ordering in Section 4.9. • Relabelled the Y axes in Fig. 4-8 and Fig. 4-10 in Section 4.3.3.
F3 JAN '18	• Added missing text in first bullet in Section 5.5. • Updated QFN package dimensions diagram in Section 10.2 (Aesthetic only—no content change). • Added footnote 1 and updated package certification information in Table 12-1 (Nomenclature change only; no change to package).
F4 DEC '18	• Updated headset connection in Fig. 2-1. • Updated minimum and maximum values for the external voltage applied to pin parameter in Table 3-2. • Updated Footnote 2 and 3 in Table 3-12. • Added a note about interchangeable terms in Section 4. • Minor update to Step 8 in Section 4.2.2. • Minor update to last sentence in Section 4.4.1.2. • Updated Fig. 4-18. • Clarified behavior of VP Monitor in Section 4.9.1. • Added Section 4.13, FILT+ Operation. • Added a note about setting or clearing specific enable bits before performing any power-up sequence in Section 5.1. • Updated bit field names and descriptions for ASP Receive Enable in Section 6.14 and Section 7.14.1. • Corrected bit field value for PDN_ALL in Step 4 of Ex. 5-2. • Updated description for ASP_SCPOL_IN_DAC in Section 7.3.6. • Removed Footnote 1 in Table 12-1. • Updated legal boilerplate wording.

Important: Please check with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru