



## 28 Gbps, 4:1 MUX WITH PROGRAMMABLE OUTPUT VOLTAGE

### Typical Applications

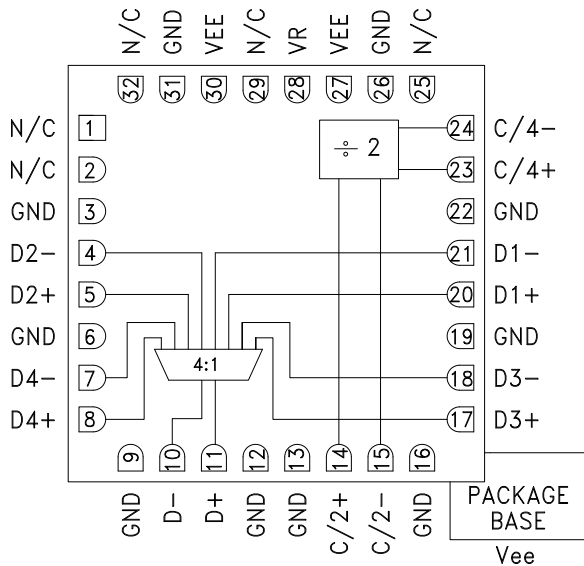
The HMC854LC5 is ideal for:

- SONET OC 192
- Broadband Test & Measurement
- Serial Data Transmission up to 28 Gbps
- Mux modes:
  - 4:1 @ 28 Gbps NRZ,
  - 2:1 @ 14 Gbps RZ and NRZ
- FPGA Interfacing

### Features

- Differential & Single-Ended Operation
- Half Rate Clock Input
- Quarter Rate Reference Clock Output
- Fast Rise and Fall Times: 16 ps
- Low Power Consumption: 510 mW typ.
- Programmable Differential
  - Output Voltage Swing: 700 - 1250 mV
- Single Supply: -3.3 V
- 32 Lead Ceramic 5x5 mm SMT Package: 25 mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC854LC5 is a 4:1 multiplexer designed for 28Gbps data serialization. The mux latches the four differential inputs on a rising edge of the input clock. The device uses both rising and falling edges of the half-rate clock to serialize the data. A quarter-rate clock output generated on chip can be used to synchronize data into the mux. The mux is DC coupled supporting broadband operation.

All clock and data inputs to the HMC854LC5 are CML and terminated on-chip with 50 ohms to the positive supply, GND, and may be DC or AC coupled. The differential outputs are source terminated to 50 ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 ohm ground terminated system, or drive devices with CML logic input. The HMC854LC5 also features an output level control pin, VR, which allows for loss compensation or signal level optimization. The HMC854LC5 operates from a single -3.3 V supply and is available in ROHS compliant 5x5 mm SMT package.

### Electrical Specifications, $T_A = +25^\circ\text{C}$ , $V_{ee} = -3.3\text{ V}$ , $VR = 0\text{ V}$

| Parameter                     | Conditions                                      | Min.          | Typ. | Max  | Units   |
|-------------------------------|---|---------------|------|------|---------|
| Power Supply Voltage          | $T > 75^\circ\text{C}$                          | -3.6<br>-3.45 | -3.3 | -3.0 | V<br>V  |
| Power Supply Current          |   |               | 155  |      | mA      |
| Maximum Data Rate             |   |               | 28   |      | Gbps    |
| Maximum Clock Rate, Half Rate |   |               | 14   |      | GHz     |
| Input Voltage Range, CML      |   | -1.5          |      | 0.5  | V       |
| Input Differential Voltage    |   | 100           |      | 2000 | mV      |
| Output Rise / Fall Time       | Differential, 20% - 80%                         |               | 16   |      | ps      |
| Random Jitter Jr              | rms   |               | 0.5  |      | ps rms  |
| Deterministic Jitter, Jd      | peak-to-peak, 2 <sup>15</sup> -1 PRBS input [1] |               | 4    |      | ps, p-p |

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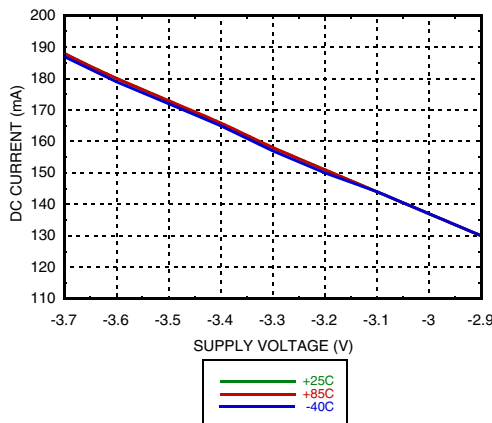


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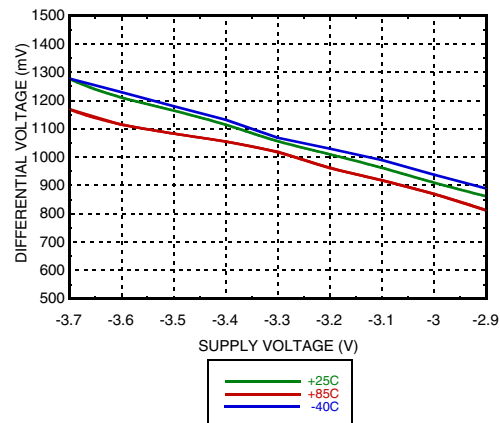
### Electrical Specifications (continued)

| Parameter   | Conditions                 | Min. | Typ. | Max | Units |
|---|----------------------------|------|------|-----|-------|
| Input Return Loss   | Frequency <12 GHz          |      | 10   |     | dB    |
| Output Amplitude  | Single-Ended, peak-to-peak |      | 500  |     | mVp-p |
|   | Differential, peak-to-peak |      | 1000 |     | mVp-p |
| Output High Voltage                                       |                            |      | 0    |     | mV    |
| Output Low Voltage  |                            |      | -500 |     | mV    |
| Output Return Loss  | Frequency <12 GHz          |      | 10   |     | dB    |
| Propagation Delay Clock to Data, Td <sub>pd</sub>         |                            |      | 126  |     | ps    |
| Propagation Delay Clock to Output Clock, Tc <sub>pd</sub> |                            |      | 135  |     | ps    |
| Set Up Time, t <sub>s</sub>                               |                            |      | -41  |     | ps    |
| Hold Time, t <sub>h</sub>                                 |                            |      | 50   |     | ps    |

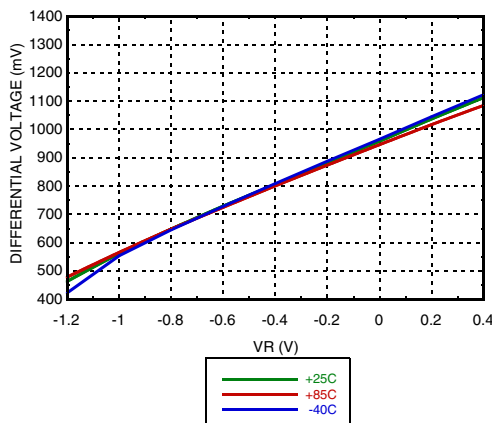
DC Current vs. Supply Voltage [1] [2]



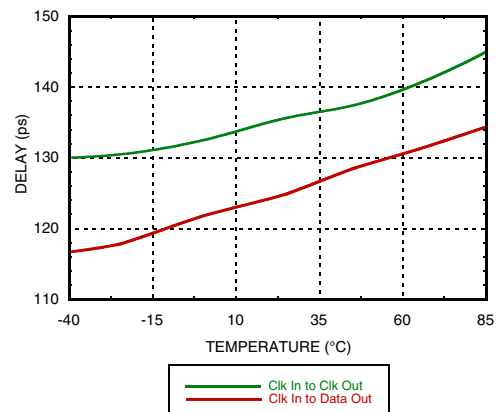
Output Differential vs. Supply Voltage [1] [2]



Output Differential vs. VR [2] [3]



Delay vs. Temperature [1] [3]



[1] VR = 0.0 V

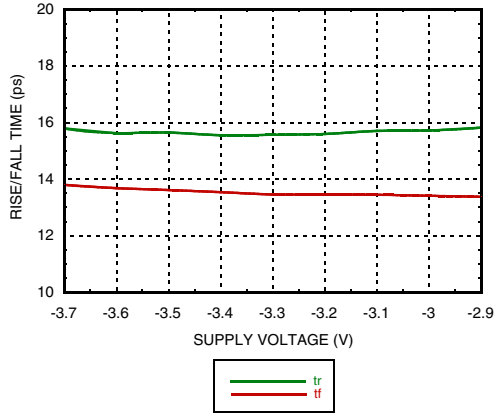
[2] Frequency = 28 Gbps

[3] Vee = -3.3 V

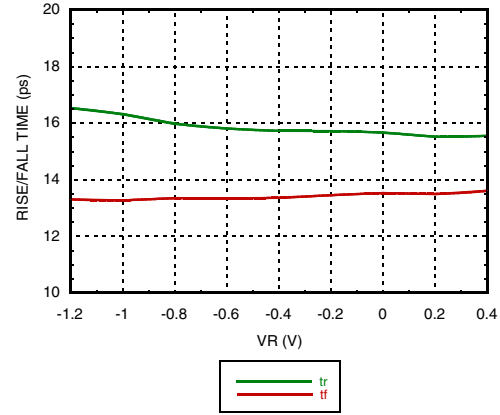


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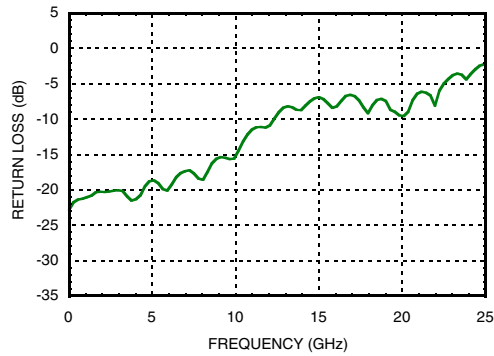
**Rise / Fall Time vs. Supply Voltage [1] [2]**



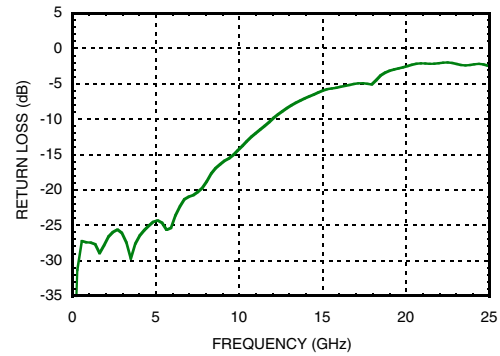
**Rise / Fall Time vs. VR [2] [4]**



**Input Return Loss vs. Frequency [1] [3] [4]**



**Output Return Loss vs. Frequency [3]**



[1] VR = 0.0 V

[2] Frequency = 28 Gbps

[3] Device measured on evaluation board with port extensions

[4] Vee = -3.3 V

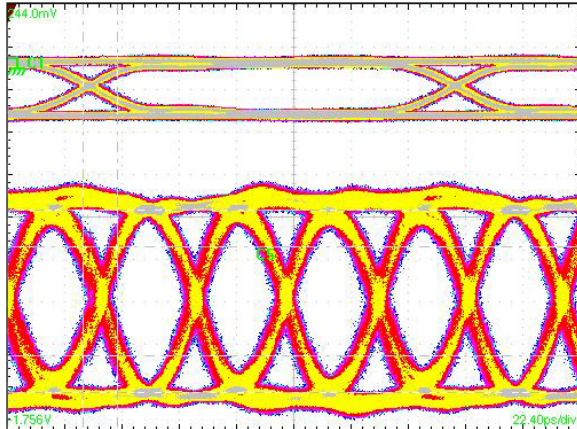
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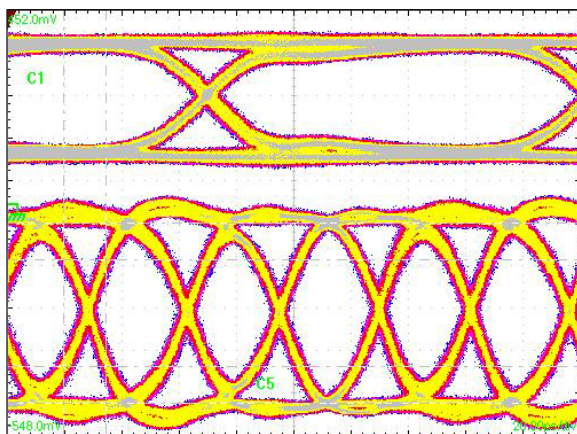
### Eye Diagram @ 28 Gbps



#### Test Conditions:

Single ended 550 mV data and 400 mV clock inputs. Pattern generated with four  $2^{15} - 1$  PN patterns applied to the inputs resulting in a Quasi-Periodic PRBS pattern at 28 Gbps. Measured using Tektronix CSA 8000

### Eye Diagram @ 30 Gbps



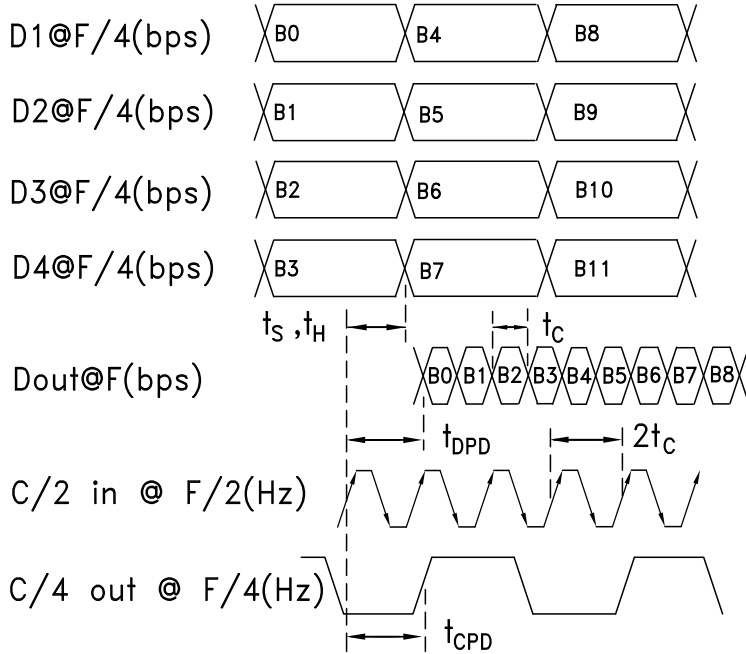
#### Test Conditions:

Single ended 550 mV data and 400 mV clock inputs. Pattern generated with four  $2^{15} - 1$  PN patterns applied to the inputs resulting in a Quasi-Periodic PRBS pattern at 30 Gbps. Measured using Tektronix CSA 8000



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**Timing Diagram**





## 28 Gbps, 4:1 MUX WITH PROGRAMMABLE OUTPUT VOLTAGE

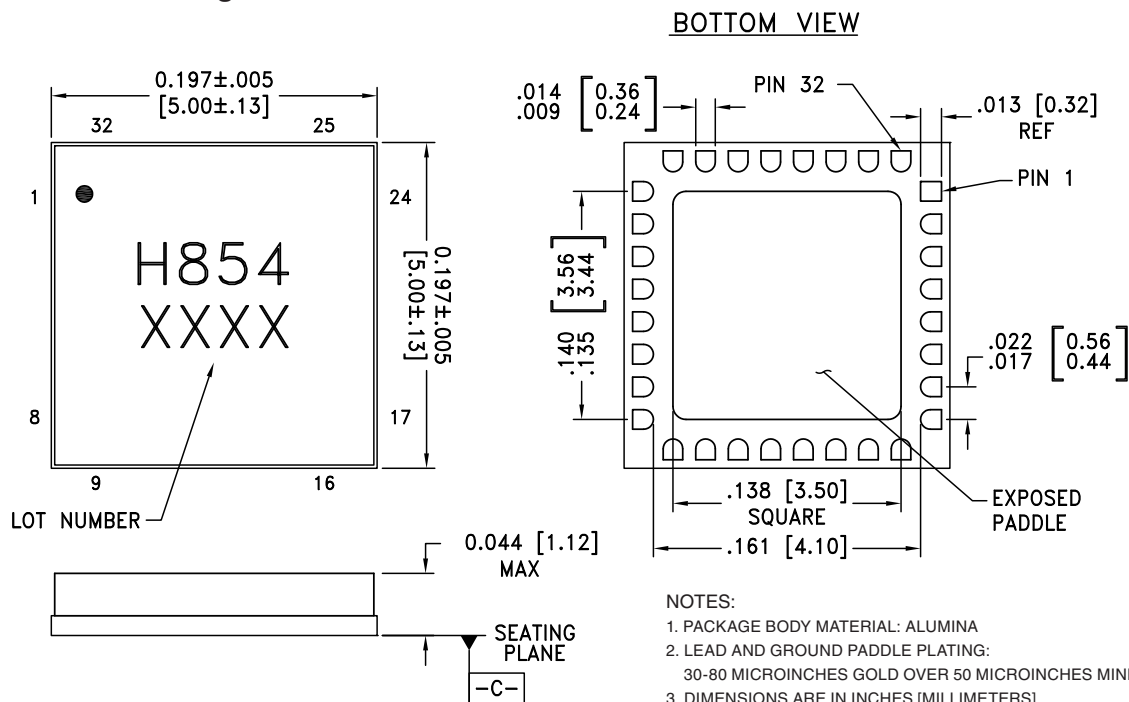
### Absolute Maximum Ratings

|  |                   |
|--|-------------------|
| Power Supply Voltage (Vee)   | -3.75 V to +0.5 V |
| Input Signals  | -2 V to +0.5 V    |
| Output Signals   | -1.5 V to +0.5 V  |
| Junction Temperature   | 125 °C            |
| Continuous Pdiss (T = 85 °C)<br>(derate 33 mW/°C above 85 °C)                    | 1.33 W            |
| Thermal Resistance (R <sub>th j-p</sub> )<br>Worse case device to package paddle | 30 °C/W           |
| Storage Temperature  | -65 °C to +150 °C |
| Operating Temperature  | -40 °C to +85 °C  |
| ESD Sensitivity (HBM)  | Class 1C          |



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

### Outline Drawing




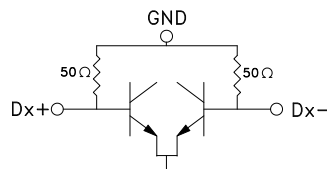
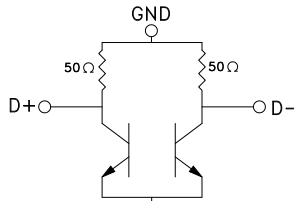
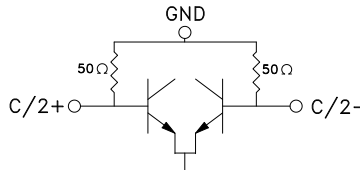
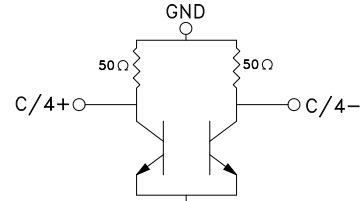
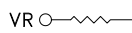
### Package Information

| Part Number | Package Body Material | Lead Finish      | MSL Rating          | Package Marking <sup>[2]</sup> |
|-------------|-----------------------|------------------|---------------------|--------------------------------|
| HMC854LC5   | Alumina, White        | Gold over Nickel | MSL3 <sup>[1]</sup> | H854<br>XXXX                   |

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX


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**Pin Descriptions**

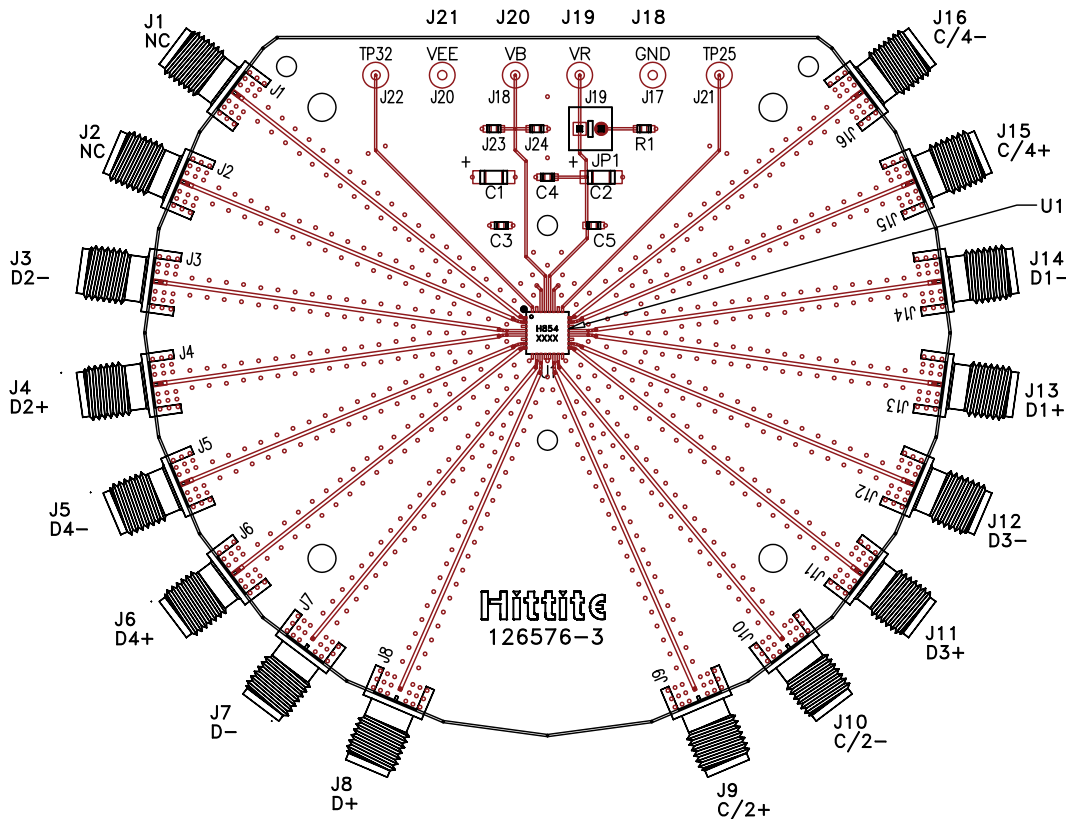
| Pin Number                          | Function                                     | Description   | Interface Schematic   |
|-------------------------------------|--|---|---|
| 1, 2, 25, 29, 32                    | N/C  | No connection necessary. These pins may be connected to RF/DC ground without affecting performance.                                 |   |
| 3, 6, 9, 12, 13, 16, 19, 22, 26, 31 | GND  | These pins must be connected to a high quality RF/DC ground.  |    |
| 4, 5, 7, 8, 17, 18, 20, 21          | D2-, D2+<br>D4-, D4+<br>D3+, D3-<br>D1+, D1- | Differential Data Inputs:<br>Current Mode Logic(CML) referenced to positive supply  |    |
| 10, 11                              | D-, D+                                       | Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply   |    |
| 14, 15                              | C/2+, C/2-                                   | Differential Half-Rate Clock Inputs: Current Mode Logic (CML) referenced to positive supply   |  |
| 23, 24                              | C/4+, C/4-                                   | Differential Quarter-Rate Clock Outputs: Current Mode Logic(CML) referenced to positive supply                                      |  |
| 27, 30, Package Base                | Vee  | These pins and the exposed paddle must be connected to the negative voltage supply.   |   |
| 28                                  | VR   | Output level control. Output level may be increased or decreased by applying a voltage to VR per "Output Differential vs. VR" plot. |  |





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**Evaluation PCB**



**List of Materials for Evaluation PCB 126578 [1]**

| Item               | Description                  |
|--------------------|------------------------------|
| J7 - J10           | PCB Mount K RF Connectors    |
| J3 - J6, J11 - J16 | PCB Mount SMA RF Connectors  |
| J18 - J21          | DC Pin                       |
| JP1                | 2 Position Header with Shunt |
| C1, C2             | 4.7 µF Capacitor, Tantalum   |
| C3 - C5            | 100 pF Capacitor, 0402 Pkg.  |
| R1                 | 10 Ohm Resistor, 0603 Pkg.   |
| U1                 | HMC854LC5 28 Gbps 4:1 Mux    |
| PCB [2]            | 126576 Evaluation Board      |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

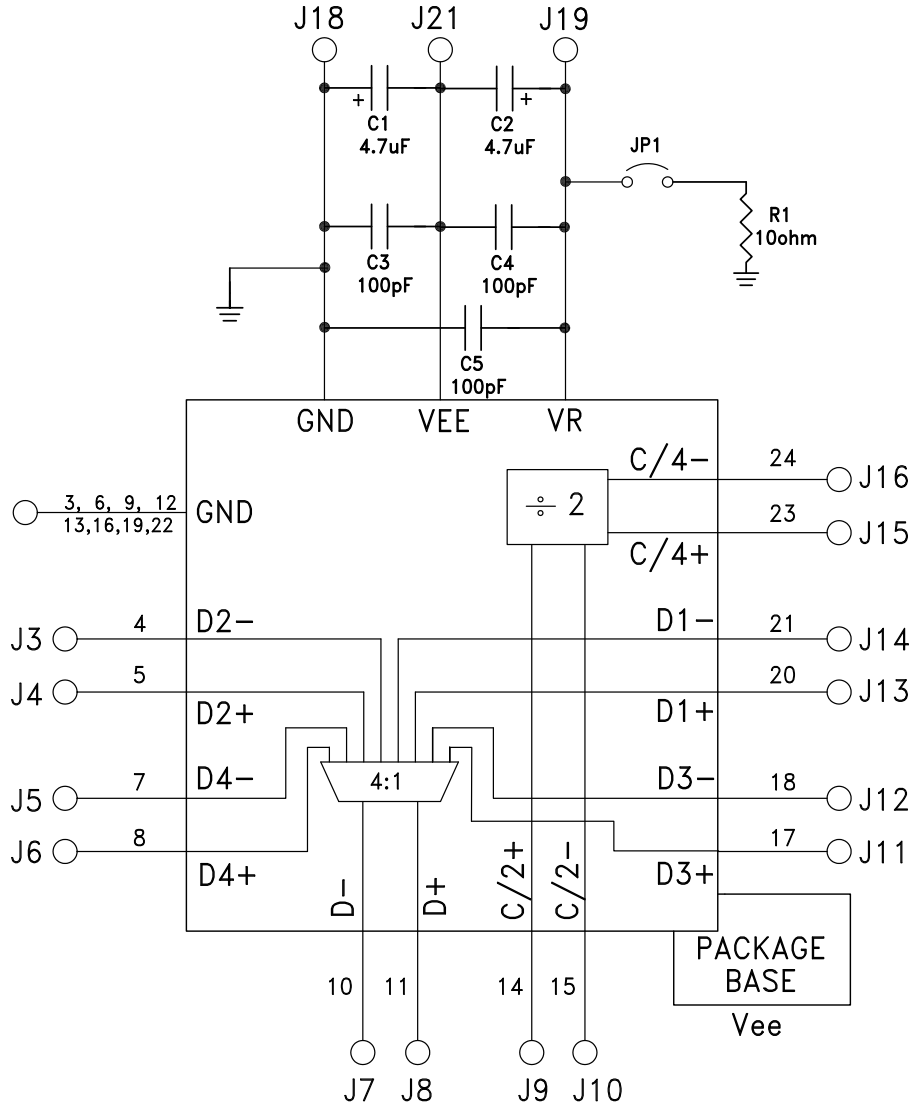
The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.





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**Application Circuit**



**28 Gbps, 4:1 MUX  
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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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