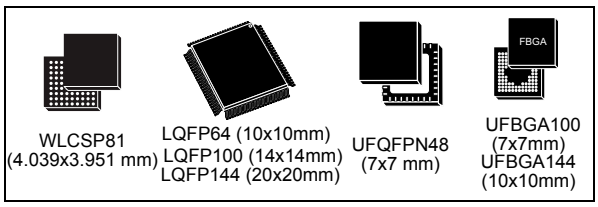
# STM32F423xH

## Arm®-Cortex®-M4 32b MCU+FPU, 125 DMIPS, 1.5MB Flash, 320KB RAM, USB OTG FS, 1 ADC, 2 DACs, 2 DFSDMs, AES

**Datasheet - production data**

## Features

- Dynamic Efficiency Line with eBAM (enhanced Batch Acquisition Mode)
  - 1.7 V to 3.6 V power supply
  - -40 °C to 85/105/125 °C temperature range
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 100 MHz, memory protection unit, 125 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - 1.5 Mbytes of Flash memory
  - 320 Kbytes of SRAM
  - Flexible external static memory controller with up to 16-bit data bus: SRAM, PSRAM, NOR Flash memory
  - Dual mode Quad-SPI interface
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.7 to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 112 µA/MHz (peripheral off)
  - Stop (Flash in Stop mode, fast wakeup time): 42 µA Typ.; 80 µA max @25 °C
  - Stop (Flash in Deep power down mode, slow wakeup time): 15 µA Typ.; 46 µA max @25 °C
  - Standby without RTC: 1.1 µA Typ.; 14.7 µA max at @85 °C
  - $V_{BAT}$ supply for RTC: 1 µA @25 °C
- 2x12-bit D/A converters
- 1×12-bit, 2.4 MSPS ADC: up to 16 channels
- 6x digital filters for sigma delta modulator, 12x PDM interfaces, with stereo microphone and sound source localization support
- General-purpose DMA: 16-stream DMA




- Up to 18 timers: up to twelve 16-bit timers, two 32-bit timers up to 100 MHz each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window), one SysTick timer, and a low-power timer
- Debug mode
  - Serial wire debug (SWD) & JTAG
  - Cortex®-M4 Embedded Trace Macrocell™
- Up to 114 I/O ports with interrupt capability
  - Up to 109 fast I/Os up to 100 MHz
  - Up to 114 five V-tolerant I/Os
- Up to 24 communication interfaces
  - Up to 4x $I^2C$ interfaces (SMBus/PMBus)
  - Up to 10 UARTS: 4 USARTs / 6 UARTs (2 x 12.5 Mbit/s, 2 x 6.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 5 SPI/I2Ss (up to 50 Mbit/s, SPI or I2S audio protocol), out of which 2 muxed full-duplex I2S interfaces
  - SDIO interface (SD/MMC/eMMC)
  - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with PHY
  - 3x CAN (2.0B Active)
  - 1xSAI
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- 128/256-bit hardware encryption accelerator (AES)
- All packages are ECOPACK®2

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32F423xH | STM32F423CH STM32F423MH STM32F423RH STM32F423VH STM32F423ZH |



This is information on a product in full production. www.st.com

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# 1 Introduction

This datasheet provides the description of the STM32F423xH microcontrollers.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

# 2 Description

The STM32F423xH devices are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 100 MHz. Their Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all Arm single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F423xH devices belong to the STM32F423xH access product lines (with products combining power efficiency, performance and integration) while adding a new innovative feature called Batch Acquisition Mode (BAM) allowing to save even more power consumption during data batching.

The STM32F423xH devices incorporate high-speed embedded memories (1.5 Mbytes of Flash memory, 320 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer a 12-bit ADC, two 12-bit DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timer for motor control, two general-purpose 32-bit timers and a low power timer.

They also feature standard and advanced communication interfaces.

- Up to four $I^2C$s, including one $I^2C$ supporting Fast-Mode Plus
- Five SPIs
- Five $I^2S$s out of which two are full duplex. To achieve audio class accuracy, the $I^2S$ peripherals can be clocked via a dedicate internal audio PLL or via an external clock to allow synchronization.
- Four USARTs and six UARTs
- An SDIO/MMC interface
- An USB 2.0 OTG full-speed interface
- Three CANs
- An SAI.

In addition, the STM32F423xH devices embed advanced peripherals:

- A flexible static memory control interface (FSMC)
- A Quad-SPI memory interface
- Two digital filter for sigma modulator (DFSDM) supporting microphone MEMs and sound source localization, one with two filters and up to four inputs, and the second one with four filters and up to eight inputs

The STM32F423xH devices embed an AES hardware accelerator.

They are offered in 7 packages ranging from 48 to 144 pins. The set of available peripherals depends on the selected package. The STM32F423xH operate in the – 40 to + 125 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F423xH microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub
- Wearable devices
- Connected objects
- Wifi modules

**Table 2. STM32F423xH features and peripheral counts**

| Peripherals | | STM32F423xH | | | | |
|---|---|---|---|---|---|---|
| Flash memory (Kbyte) | | 1536 | | | | |
| SRAM (Kbyte) | System | 320 (256 + 64) | | | | |
| FSMC memory controller | | - | 1(1) | 1(1) | 1(1) | 1 |
| FSMC LCD parallel interface Data bus size | | - | 8 | 16 | | |
| Quad-SPI memory interface | | - | 1 | | | |
| Timers | General-purpose | 10(2) | 10 | 10(3) | 10 | |
| | Advanced-control | 2(4) | 2 | | | |
| | Basic | 2 | | | | |
| | Low-power timer | 1 | | | | |
| Random number generator | | 1 | | | | |
| AES | | 1 | | | | |
| Comm. interfaces | SPI/ $I^2S$ | 5/5 (2 full duplex) | | | | |
| | $I^2C$ | 3 | | | | |
| | $I^2CFMP$ | 1 | | | | |
| | USART/UART | 3/3 | 4/3 | | 4/6 | |
| | SDIO/MMC | 1 | | | | |
| | USB/OTG FS Dual power rail | 1 No | | 1 Yes | 1 No | 1 Yes |
| | CAN | 3 | | | | |
| | SAI | 1 | | | | |
| Number of digital Filtersfor Sigma-delta modulator | | 6 | | | | |
| Number of channels | | 7 | 11 | 12 | | |
| GPIOs | | 36 | 50 | 60 | 81 | 114 |
| 12-bit ADC | | 1 | | | | |
| Number of channels | | 10 | 16 | | | |
| 12-bit DAC | | Yes | | | | |
| Number of channels | | 2 | | | | |
| Maximum CPU frequency | | 100 MHz | | | | |
| Operating voltage | | 1.7 to 3.6 V | | | | |
| Operating temperatures | | Ambient temperatures: – 40 to + 85 °C/– 40 to + 105 °C / – 40 to + 125 °C | | | | |
| | | Junction temperature: – 40 to + 130 °C | | | | |
| Package | | UFQFPN48 | LQFP64 | WLCSP81 | UFBGA100 LQFP100 | UFBGA144 LQFP144 |

1. 64 pins packages support only 8 bits multiplexed mode interface
   81 pins packages support 1 external memory of up to 64KB in multiplexed mode
   100 pins packages support 2 external memories of up to 64MB in multiplexed mode
   Refer to *Table 11: FSMC pin definition* for more detailed information.
2. 48 pins packages: TIM3 and TIM4: ETR pin not available.

3. 81 pins packages: TIM4: ETR pin not available.
4. 48 pins packages: TIM8:CH1, CH2, CH3 and CH4 pins not available.

## 2.1 Compatibility with STM32F4 series

The STM32F423xH are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F423xH can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

**Figure 1. Compatible board design for LQFP100 package**

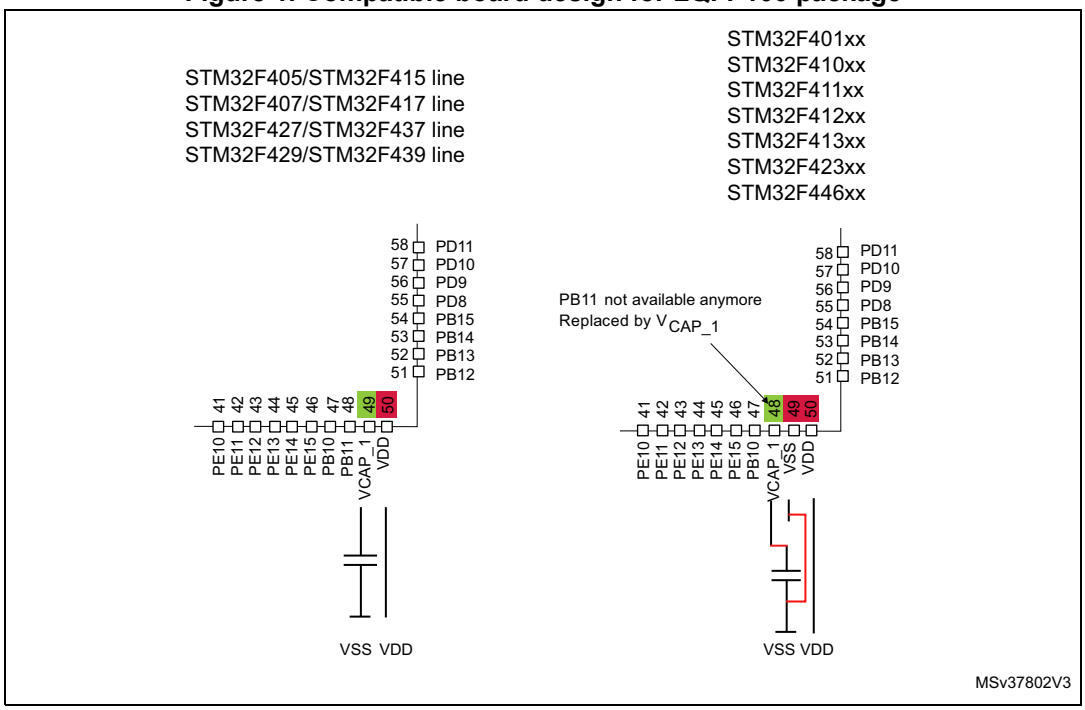


**Figure 2. Compatible board design for LQFP64 package**

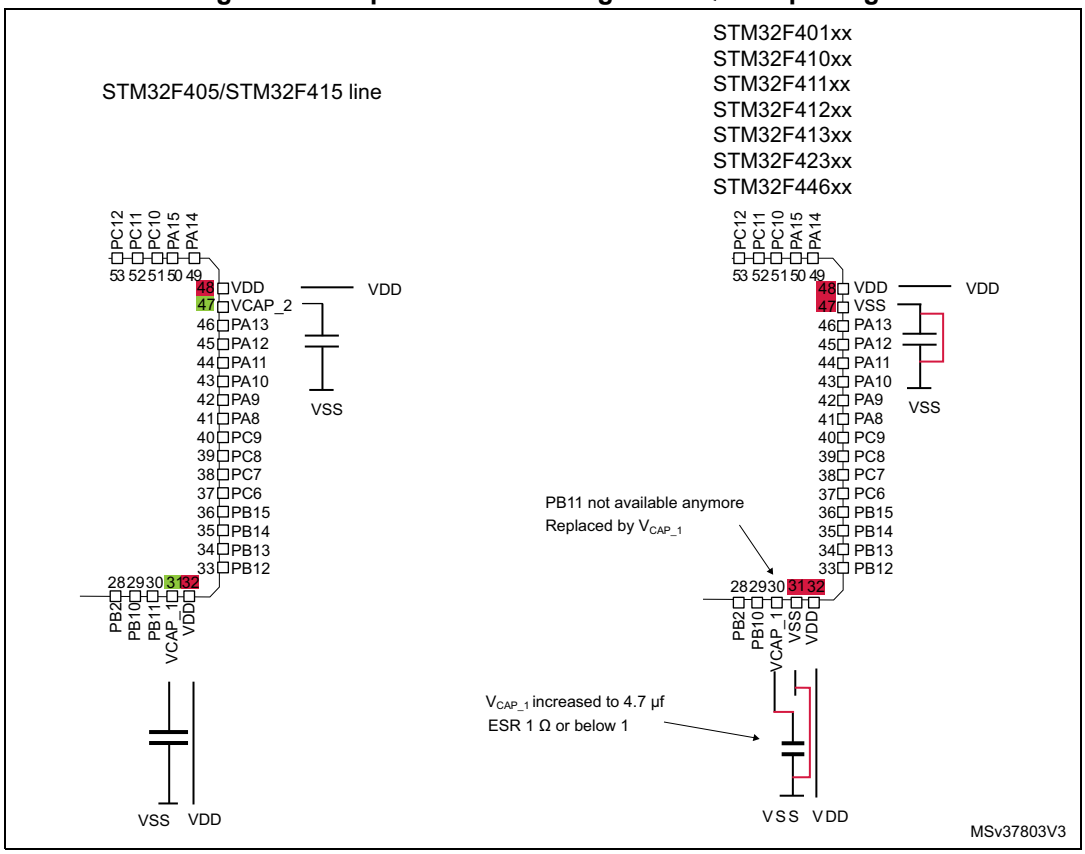



**Figure 3. Compatible board design for LQFP144 package**

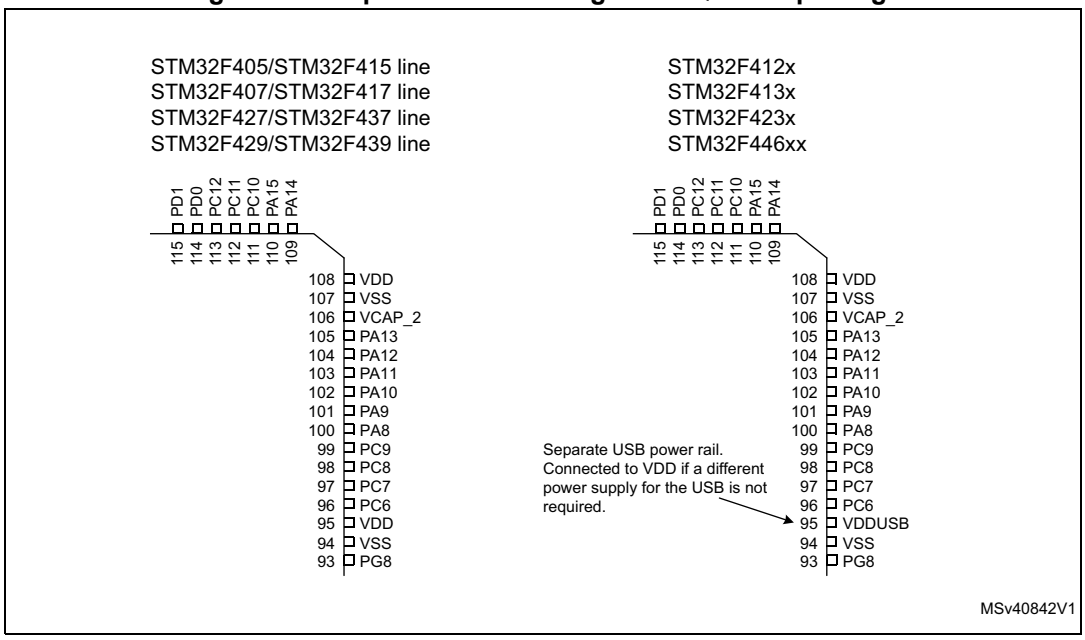
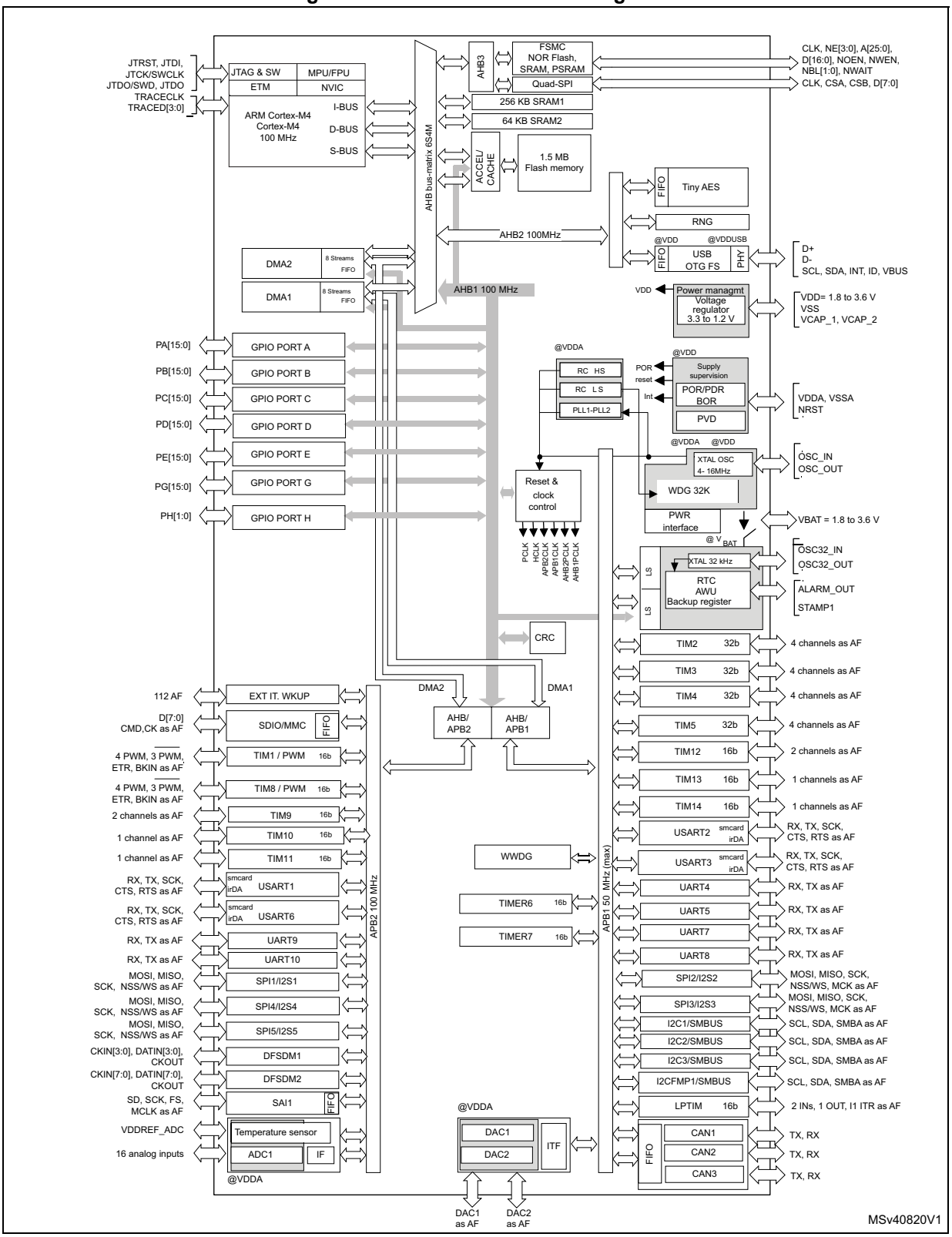


**Figure 4. STM32F423xH block diagram**




1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

# 3 Functional overview

## 3.1 Arm® Cortex®-M4 with FPU core with embedded Flash and SRAM

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F423xH devices are compatible with all Arm tools and software.

*Figure 4* shows the general block diagram of the STM32F423xH.

*Note: Cortex®-M4 with FPU is binary compatible with Cortex®-M3.*

## 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

## 3.3 Enhanced Batch Acquisition mode (eBAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the Flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the DFSDM directly to RAM (Flash and ART™ stopped) with the DMA using BAM followed by some very short processing from Flash allows to drastically reduce the power consumption of the application.

The BAM has been enhanced by adding SRAM2 that allows SRAM code to be executed through the Ibus and Dbus, thus improving code execution performance.

A dedicated application note (AN4515) describes how to implement the STM32F423xH BAM to allow the best power efficiency.

## 3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 3.5 Embedded Flash memory

The devices embed 1.5 Mbytes of Flash memory available for storing programs and data, plus 512 bytes of one-time programmable (OTP) memory organized in 16 blocks of 32 bytes, each which can be independently locked.

The user Flash memory area can be protected against read operations by an entrusted code (read protection or RDP). Different protection levels are available. The user Flash memory is divided into sectors, which can be individually protected against write operation. Flash sectors can also be protected individually against D-bus read accesses by using the proprietary readout protection (PCROP).

Refer to the product line reference manual for additional information on OTP area and protection features.

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see *Section 3.20: Low-power modes*).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time.

Before disabling the Flash, the code must be executed from the internal RAM.

## 3.6 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

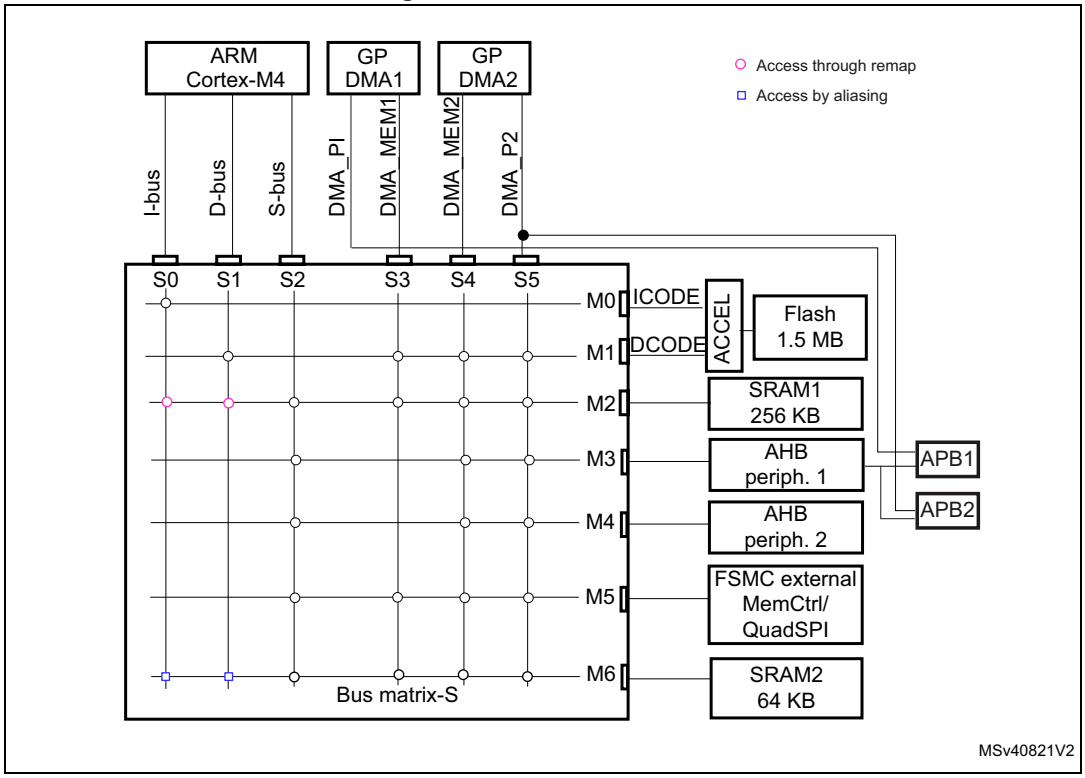
## 3.7 Embedded SRAM

All devices embed 320 Kbytes of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states.

## 3.8 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

**Figure 5. Multi-AHB matrix**




CPU can access SRAM1 memory via S-bus, when SRAM1 is mapped at the address range: 0x2000 0000 to 0x2003 FFFF.

CPU can access SRAM2 memory via S-bus, when SRAM2 is mapped at the address range: 0x2004 0000 to 0x2004 FFFF.

CPU can access SRAM1 memory via I-bus and D-bus, when SRAM1 is remapped at address 0x0000 0000 either by booting from RAM memory or by the remap mode.

CPU can access SRAM2 memory via I-bus and D-bus, when SRAM2 is mapped at the address range: 0x1000 0000 to 0x1000 FFFF.

Performance boosts up, when the CPU access SRAM memory via the I-bus.

## 3.9 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and $I^2S$
- $I^2C$ and $I^2CFMP$
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- DAC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter
- SAI.

## 3.10 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR Flash memory.

The main functions are:

- 8-,16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

### LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 3.11 Quad-SPI memory interface (QUAD-SPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting single, dual or quad-SPI Flash memories. It can work in direct mode through registers, external Flash status register polling mode and memory mapped mode. Up to 256 Mbyte of external Flash memory are mapped. They can be accessed in 8, 16 or 32-bit mode. Code execution is also supported. The opcode and the frame format are fully programmable. Communication can be performed either in single data rate or dual data rate.

## 3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 102 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

## 3.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

## 3.14 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB

buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the $I^2S$ master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

## 3.15 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using one of the interface listed in the *Table 3* or the USB OTG FS in device mode through DFU (device firmware upgrade).

**Table 3. Embedded bootloader interfaces**

| Package | USART1 PA9/ PA10 | USART2 PD6/ PD5 | USART3 PB11/ PB10 | I2C1 PB6/ PB7 | I2C2 PF0/ PF1 | I2C3 PA8/ PB4 | I2C FMP1 PB14/ PB15 | SPI1 PA4/ PA5/ PA6/ PA7 | SPI3 PA15/ PC10/ PC11/ PC12 | SPI4 PE11/ PE12/ PE13/ PE14 | CAN2 PB5/ PB13 | USB PA11 /P12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | Y | - | - | Y | - | Y | Y | Y | - | - | Y | Y |
| LQFP64 | Y | - | - | Y | - | Y | Y | Y | Y | - | Y | Y |
| WLCSP81 | Y | - | - | Y | - | Y | Y | Y | Y | Y | Y | Y |
| LQFP100 | Y | Y | - | Y | - | Y | Y | Y | Y | Y | Y | Y |
| LQFP144 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| UFBGA100 | Y | Y | Y | Y | - | Y | Y | Y | Y | Y | Y | Y |
| UFBGA144 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

## 3.16 Power supply schemes

- $V_{DD}$ = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through $V_{DD}$ pins. Requires the use of an external power supply supervisor connected to the $V_{DD}$ and NRST pins.
- $V_{SSA}$, $V_{DDA}$ = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively, with decoupling technique.

*Note: The $V_{DD}$/$V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to Section 3.17.2: Internal reset OFF). Refer to Table 4: Regulator ON/OFF and internal power supply supervisor availability to identify the packages supporting this option.*

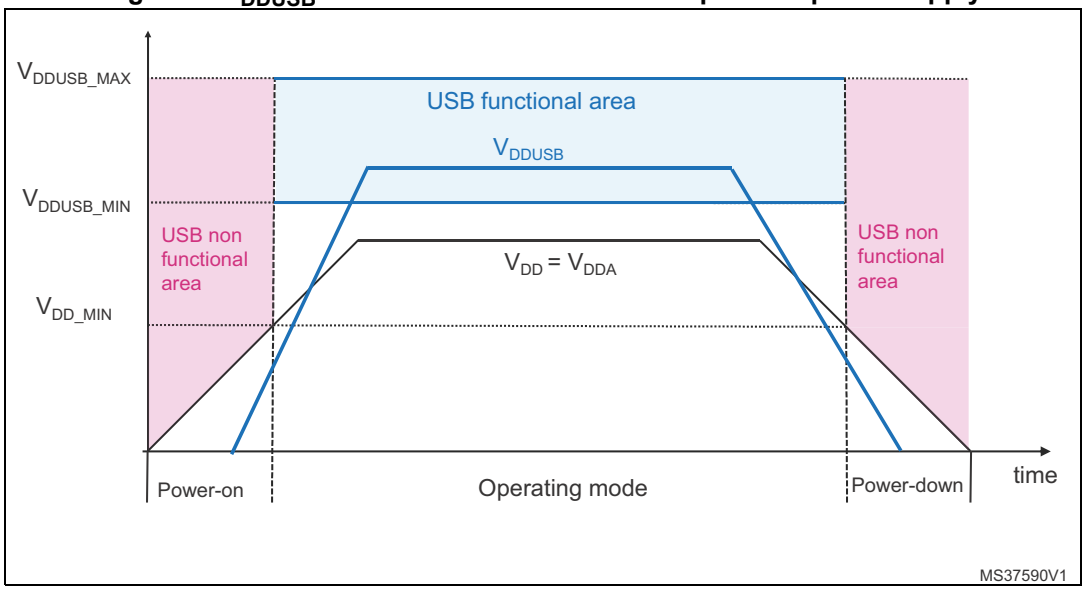
- $V_{BAT}$ = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.
- $V_{DDUSB}$ can be connected either to VDD or an external independent power supply (3.0 to 3.6 V) for USB transceivers.

  For example, when device is powered at 1.8 V, an independent power supply 3.3V can be connected to $V_{DDUSB}$. When the $V_{DDUSB}$ is connected to a separated power supply, it is independent from $V_{DD}$ or $V_{DDA}$ but it must be the last supply to be provided and the first to disappear.

The following conditions VDDUSB must be respected:

- During power-on phase ($V_{DD}$ < $V_{DD_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$
- During power-down phase ($V_{DD}$ < $V_{DD_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$
- $V_{DDUSB}$ rising and falling time rate specifications must be respected.
- In operating mode phase, $V_{DDUSB}$ could be lower or higher than VDD:
  - If USB is used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DDUSB_MIN}$ and $V_{DDUSB_MAX}$.
  - If USB is not used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DD_MIN}$ and $V_{DD_MAX}$.

Figure 6. $V_{DDUSB}$ connected to an external independent power supply




## 3.17 Power supply supervisor

### 3.17.1 Internal reset ON

This feature is available for $V_{DD}$ operating voltage range 1.8 V to 3.6 V.

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for an external reset circuit.

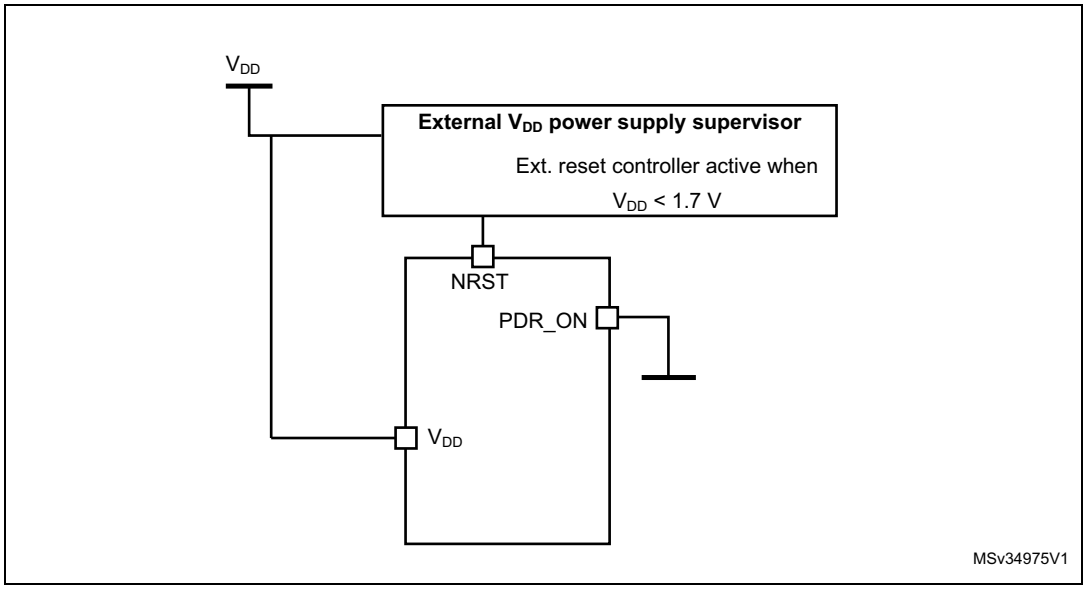
The device also features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor $V_{DD}$ and should set the device in reset mode when $V_{DD}$ is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

**Figure 7. Power supply supervisor interconnection with internal reset OFF(1)**




1. The PRD_ON pin is available only on WLCSP81, UFBGA100, UFBGA144 and LQFP144 packages.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$ functionality is no more available and VBAT pin should be connected to $V_{DD}$.

## 3.18 Voltage regulator

The regulator has three operating modes:

- Main regulator mode (MR)
- Low power regulator (LPR)
- Power-down

### 3.18.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run mode)

  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.
- LPR is used in the Stop mode

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Depending on the package, one or two external ceramic capacitors should be connected on the $V_{CAP_1}$ and $V_{CAP_2}$ pins. The $V_{CAP_2}$ pin is only available on 100- and 144-pin packages.

All packages have the regulator ON feature.

### 3.18.2 Regulator OFF

This feature is available only on UFBGA100 and UFBGA144 packages, which feature the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a $V_{12}$ voltage source through $V_{CAP_1}$ and $V_{CAP_2}$ pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.

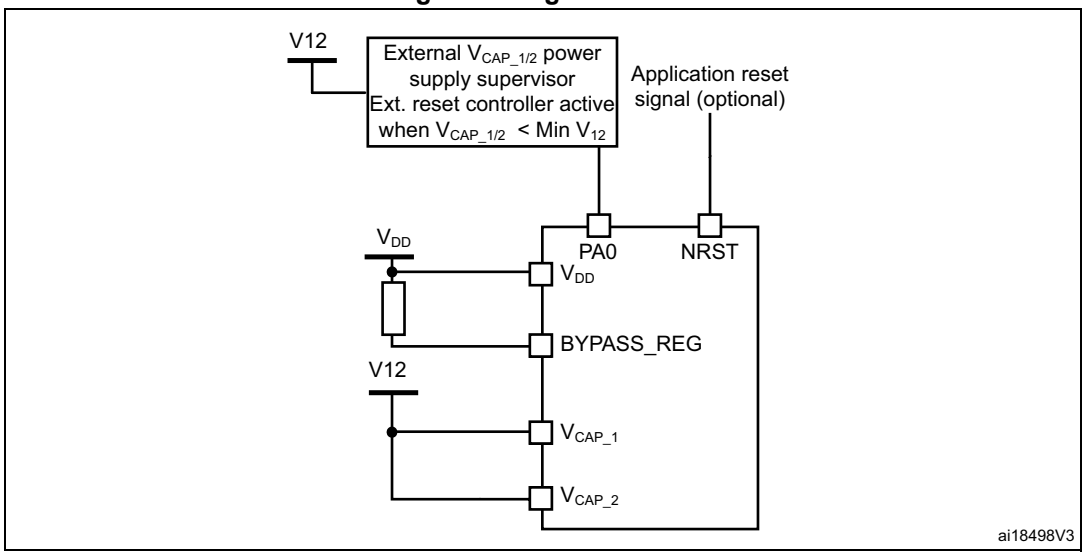
The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on $V_{12}$. An external power supply supervisor should be used to monitor the $V_{12}$ of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on $V_{12}$ power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the $V_{12}$ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

**Figure 8. Regulator OFF**

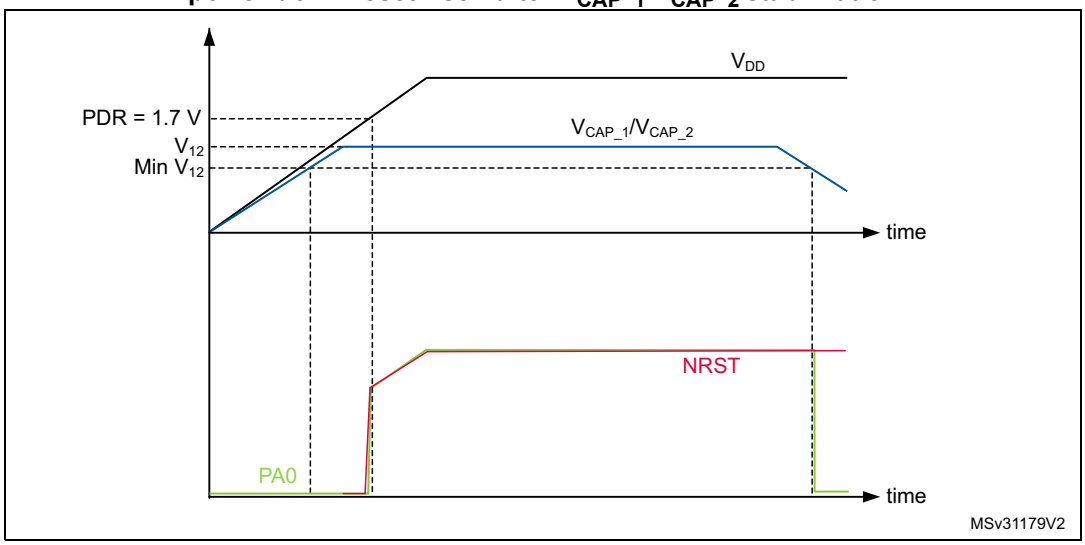



The following conditions must be respected:

- $V_{DD}$ should always be higher than $V_{CAP_1}$ and $V_{CAP_2}$ to avoid current injection between power domains.
- If the time for $V_{CAP_1}$ and $V_{CAP_2}$ to reach $V_{12}$ minimum value is faster than the time for $V_{DD}$ to reach 1.7 V, then PA0 should be kept low to cover both conditions: until $V_{CAP_1}$ and $V_{CAP_2}$ reach $V_{12}$ minimum value and until $V_{DD}$ reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for $V_{CAP_1}$ and $V_{CAP_2}$ to reach $V_{12}$ minimum value is slower than the time for $V_{DD}$ to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If $V_{CAP_1}$ and $V_{CAP_2}$ go below $V_{12}$ minimum value and $V_{DD}$ is higher than 1.7 V, then a reset must be asserted on PA0 pin.

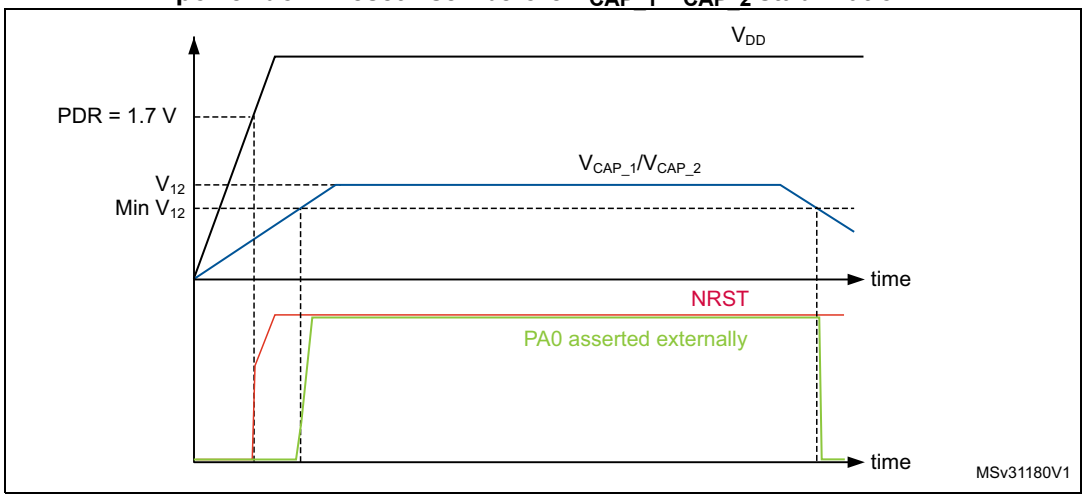
*Note: The minimum value of $V_{12}$ depends on the maximum frequency targeted in the application.*

**Figure 9. Startup in regulator OFF: slow $V_{DD}$ slope power-down reset risen after $V_{CAP_1}/V_{CAP_2}$ stabilization**




1. This figure is valid whatever the internal reset mode (ON or OFF).

**Figure 10. Startup in regulator OFF mode: fast $V_{DD}$ slope power-down reset risen before $V_{CAP_1}/V_{CAP_2}$ stabilization**




1. This figure is valid whatever the internal reset mode (ON or OFF).

### 3.18.3 Regulator ON/OFF and internal reset ON/OFF availability

**Table 4. Regulator ON/OFF and internal power supply supervisor availability**

| Package | Regulator ON | Regulator OFF | Power supply supervisor ON | Power supply supervisor OFF |
|---|---|---|---|---|
| UFQFPN48 | Yes | No | Yes | No |
| LQFP64 | Yes | No | Yes | No |
| WLCSP81 | Yes<br>BYPASS_REG<br>set to $V_{SS}$ | Yes<br>BYPASS_REG<br>set to $V_{DD}$ | Yes<br>PDR_ON<br>set to $V_{DD}$ | Yes<br>PDR_ON<br>set to $V_{SS}$ |
| LQFP100 | Yes | No | Yes | No |
| LQFP144 | Yes | No | Yes<br>PDR_ON<br>set to $V_{DD}$ | Yes<br>PDR_ON<br>set to $V_{SS}$ |
| UFBGA100 | Yes<br>BYPASS_REG<br>set to $V_{SS}$ | Yes<br>BYPASS_REG<br>set to $V_{DD}$ | | |
| UFBGA144 | Yes<br>BYPASS_REG<br>set to $V_{SS}$ | Yes<br>BYPASS_REG<br>set to $V_{DD}$ | | |

## 3.19 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when $V_{DD}$ power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.20: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the $V_{DD}$ supply when present or from the VBAT pin.

## 3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  To further reduce the power consumption, the Flash memory can be switched off before entering in Sleep mode. Note that this requires a code execution from the RAM.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on one of the WKUP pins, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

## 3.21 $V_{BAT}$ operation

The VBAT pin allows to power the device $V_{BAT}$ domain from an external battery, an external super-capacitor, or from $V_{DD}$ when no external battery and an external super-capacitor are present.

$V_{BAT}$ operation is activated when $V_{DD}$ is not present.

The VBAT pin supplies the RTC and the backup registers.

*Note: When the microcontroller is supplied from $V_{BAT}$, external interrupts and RTC alarm/events do not exit it from $V_{BAT}$ operation. When PDR_ON pin is not connected to $V_{DD}$ (internal Reset OFF), the $V_{BAT}$ functionality is no more available and VBAT pin should be connected to $V_{DD}$.*

## 3.22 Timers and watchdogs

The devices embed two advanced-control timer, ten general-purpose timers, two basic timers, one low-power timer, two watchdog timers and a SysTick timer.

All timer counters can be frozen in debug mode.

*Table 5* compares the features of the advanced-control and general-purpose timers.

**Table 5. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary output | Max. interface clock (MHz) | Max. timer clock (MHz) |
|---|---|---|---|---|---|---|---|---|---|
| Advanced-control | TIM1, TIM8 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 100 | 100 |
| General purpose | TIM2, TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 50 | 100 |
| | TIM3, TIM4 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 50 | 100 |
| | TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 100 | 100 |
| | TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 100 | 100 |
| | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 50 | 100 |
| | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 50 | 100 |

Table 5. Timer feature comparison (continued)

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complemen-tary output | Max. interface clock (MHz) | Max. timer clock (MHz) |
|---|---|---|---|---|---|---|---|---|---|
| Basic timers | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 50 | 100 |
| Low-power timer | LPTIM1 | 16-bit | Up | Between 1 and 128 | No | 2 | No | 50 | 100 |

### 3.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1/8) can be seen as three-phase PWM generator multiplexed on 4 independent channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as a 16-bit PWM generator, they have full modulation capability (0-100%).

The advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

### 3.22.2 General-purpose timers (TIMx)

There are elven synchronizable general-purpose timers embedded in the STM32F423xH (see *Table 5* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F423xH devices include 4 full-featured general-purpose timers: TIM2. TIM3, TIM4 and TIM5. TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter plus a 16-bit prescaler. They all features four

independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 15 input capture/output compare/PWMs

TIM2. TIM3, TIM4 and TIM5 general-purpose timers can operate together or in conjunction with the other general-purpose timers and TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM output.

TIM2. TIM3, TIM4 and TIM5 channels have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13 and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13 and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with TIM2. TIM3, TIM4 and TIM5 full-featured general-purpose timers or used as simple time bases.

### 3.22.3 Basic timer (TIM6, TIM7)

TIM6 and TIM7 timers are basic 16-bit timers. They support independent DMA request generation.

### 3.22.4 Low-power timer (LPTIM1)

The low-power timer (LPTIM1) features an independent clock and runs in Stop mode if it is clocked by LSE, LSI or by an external clock. LPTIM1 is able to wakeup the devices from Stop mode.

The low-power timer main features are the following:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB1 clock
  - External clock source over LPTIM1 input (working even with no internal clock source running, used by the pulse counter application)
- Programmable digital glitch filter
- Encoder mode
- Active in Stop mode.

### 3.22.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 3.22.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.22.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.23 Inter-integrated circuit interface ($I^2C$)

The devices feature up to four $I^2C$ bus interfaces which can operate in multimaster and slave modes:

- One $I^2C$ interface supports the Standard mode (up to 100 kHz), Fast-mode (up to 400 kHz) modes and Fast-mode plus (up to 1 MHz).
- Three $I^2C$ interfaces support the Standard mode (up to 100 KHz) and the Fast mode (up to 400 KHz). Their frequency can be increased up to 1 MHz. For more details on the complete solution, refer to the nearest STMicroelectronics sales office.

All $I^2C$ interfaces features 7/10-bit addressing mode and 7-bit addressing mode (as slave) and embed a hardware CRC generation/verification.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 6*).

**Table 6. Comparison of I2C analog and digital filters**

| | Analog filter | Digital filter |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |

## 3.24 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) as well as six universal asynchronous receiver transmitters (UART4, UART5, UART7, UART8, UART9 and UART10).

These ten interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. USART1, USART6, UART9 and UART10 can communicate at speeds up to 12.5 Mbit/s. The other interfaces communicate at up to 6.25 bit/s.

USART1, USART2, USART3 and USART6 provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

**Table 7. USART feature comparison**

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|---|---|---|---|---|---|---|---|---|---|
| USART1 | X | X | X | X | X | X | 6.25 | 12.5 | APB2 (max. 100 MHz) |
| USART2 | X | X | X | X | X | X | 3.12 | 6.25 | APB1 (max. 50 MHz) |
| USART3 | X | X | X | X | X | X | 3.12 | 6.25 | APB1 (max. 50 MHz) |
| UART4 | X | - | X | - | X | - | 3.12 | 6.25 | APB1 (max. 50 MHz) |
| UART5 | X | - | X | - | X | - | 3.12 | 6.25 | APB1 (max. 50 MHz) |
| USART6 | X | X | X | X | X | X | 6.25 | 12.5 | APB2 (max. 100 MHz) |
| UART7 | X | - | X | - | X | - | 3.12 | 6.25 | APB1 (max. 50 MHz) |
| UART8 | X | - | X | - | X | - | 3.12 | 6.25 | APB1 (max. 50 MHz) |
| UART9 | X | - | X | - | X | - | 6.25 | 12.5 | APB2 (max. 100 MHz) |
| UART10 | X | - | X | - | X | - | 6.25 | 12.5 | APB2 (max. 100 MHz) |

## 3.25 Serial peripheral interface (SPI)

The devices feature five SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4 and SPI5 can communicate at up to 50 Mbit/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interfaces can be configured to operate in TI mode for communications in master mode and slave mode.

## 3.26 Inter-integrated sound ($I^2S$)

Five standard $I^2S$ interfaces (multiplexed with SPI1 to SPI5) are available. They can be operated in master or slave mode, in simplex communication mode, and full duplex mode for I2S2 and I2S3. All $I^2S$ interfaces can be configured to operate with a 16-/32-bit resolution as an input or output channel. I2Sx audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All $I^2Sx$ interfaces can be served by the DMA controller.

## 3.27 Serial Audio interface (SAI1)

The serial audio interface (SAI1) is based on two independent audio sub-blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub-blocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 can be served by the DMA controller.

## 3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio $I^2S$ and SAI applications. It allows to achieve error-free $I^2S$ sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

Different sources can be selected for the I2S master clock of the APB1 and the I2S master clock of the APB2. This gives the flexibility to work with two different audio sampling frequencies. The different possible sources are the main PLL, the PLLI2S, HSE or HSI clocks or an external clock provided through a pin (external PLL or CODEC output)

Different sources can also be selected for the SAI. The different possible sources are the main PLL, the PLLI2S, HSE or HSI clocks or an external clock provided through a pin (external PLL or CODEC output).

The PLLI2S configuration can be modified to manage an $I^2S$/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

## 3.29 Digital filter for sigma-delta modulators (DFSDM)

The device embeds two DFSDMs:

- DFSDM1 has 2 digital filters modules and 4 external input serial channels (transceivers) or alternately 2 internal parallel inputs support.
- DFSDM2 features 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 4 internal parallel inputs support.

The amount of filters defines the number of conversions which can be performed simultaneously.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. It is also possible to introduce a programmable delay between different microphones (beamforming feature). DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

**Table 8. DFSDM feature comparison**

| DFSDM instance | External input serial channels | External input parallel channels | Digital filters |
|---|---|---|---|
| DFSDM1 | 4 | 2 | 2 |
| DFSDM2 | 8 | 4 | 4 |

## 3.30 Dynamic tuning of PDM delays for sound source localization

A mechanism is implemented on top of the DFSDM allowing to dynamically tune PDM delays of each microphone without the need to add external delay lines.

Audio application with several microphones require strong microphones placement constraints, as the distance between the microphones must be a multiple of v/F where v is the speed of the sound and F is the PCM sampling frequency.

The designed mechanism removes this constraint by programming delays for each digital microphone with the granularity of the PDM clock rate prior to the conversion into PCM rate.

The tuning delay is performed by a clock skipping technique.

The strong benefits of such mechanism coupled with DFSDM are:

- Possibility to place the digital microphones close to each other
- No need for external delay lines
- The delay tuning is done in hardware, preventing the use of MIPs crunching algorithms
- Possibility to change the delay tuning on the fly
- The low power consumption and CPU time released due to the DFSDM hardware PDM to PCM conversion

The impacted audio application are beam forming and sound source localization

## 3.31 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC/eMMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

## 3.32 Controller area network (bxCAN)

The three CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for CAN1 and CAN2, and 512 bytes for CAN3.

## 3.33 Universal serial bus on-the-go full-speed (USB_OTG_FS)

The devices embed a USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with USB 2.0 and OTG 1.0 specifications. It features software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock, which is generated by a PLL connected to the HSE oscillator. The Battery Charging Detection (BCD) can detect and identify the type of port it is connected to (standard USB or charger). The charging type can also be detected: Dedicated Charging Port (DCP), Charging Downstream Port (CDP) and Standard Downstream Port (SDP).

Some packages provide a dedicated USB power rail allowing to supply the USB from a different voltage that the rest of the device. As an example, the device can be powered with the minimum specified supply voltage while the USB runs at the level defined by the standard.

The main USB OTG FS features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Support of session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed when bus-powered devices are connected
- Link Power Management (LPM)
- Battery Charging Detection (BCD) supporting DCP, CDP and SDP

## 3.34 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

## 3.35 Advanced encryption standard hardware accelerator (AES)

The devices embed an AES hardware accelerator can be used to both encipher and decipher data using AES algorithm.

The AES peripheral supports:

- Encryption/Decryption using AES Rijndael Block Cipher algorithm
- NIST FIPS 197 compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (4x 32-bit registers)
- Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois Counter Mode (GCM), Galois Message Authentication Code mode (GMAC) and Cipher Message Authentication Code mode (CMAC) supported.
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit, 256-bit key length
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer.
- Register access supporting 32-bit data width only.
- One 128-bit Register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode.
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, and one for outcoming data.
- Suspend a message if another message with a higher priority needs to be processed.

## 3.36 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

## 3.37 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

## 3.38 Digital to analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This digital interface supports the following features:

- Two DAC output channels
- 8-bit or 12-bit output mode
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input voltage reference ($V_{REF+}$)

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

## 3.39 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

## 3.40 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## 3.41 Embedded Trace Macrocell™

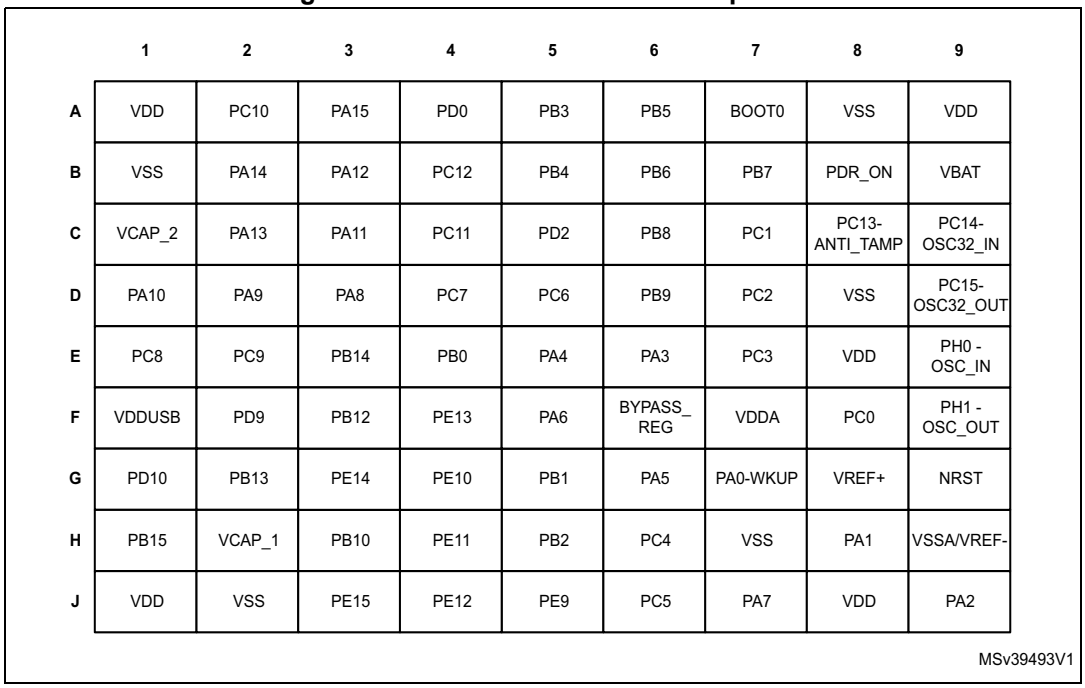
The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F423xH through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

# 4 Pinouts and pin description

## 4.1 WLCSP81 pinout description

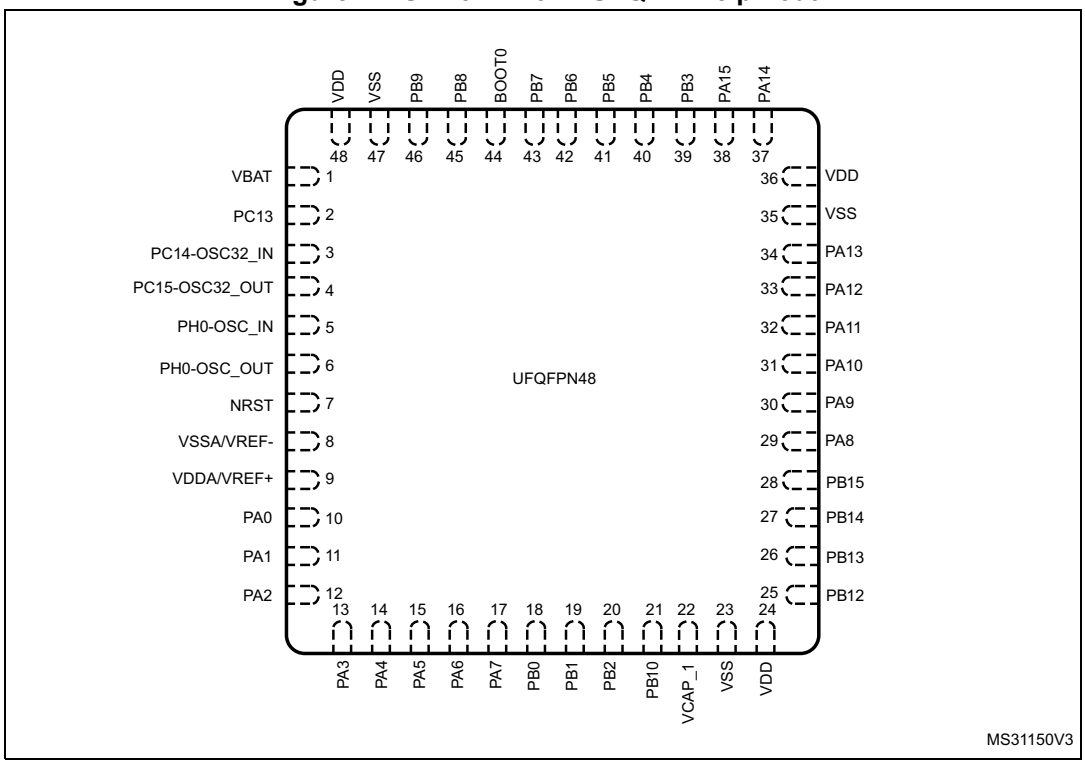
**Figure 11. STM32F423xH WLCSP81 pinout**




1. The above figure shows the package top view.

## 4.2 UFQFPN48 pinout description

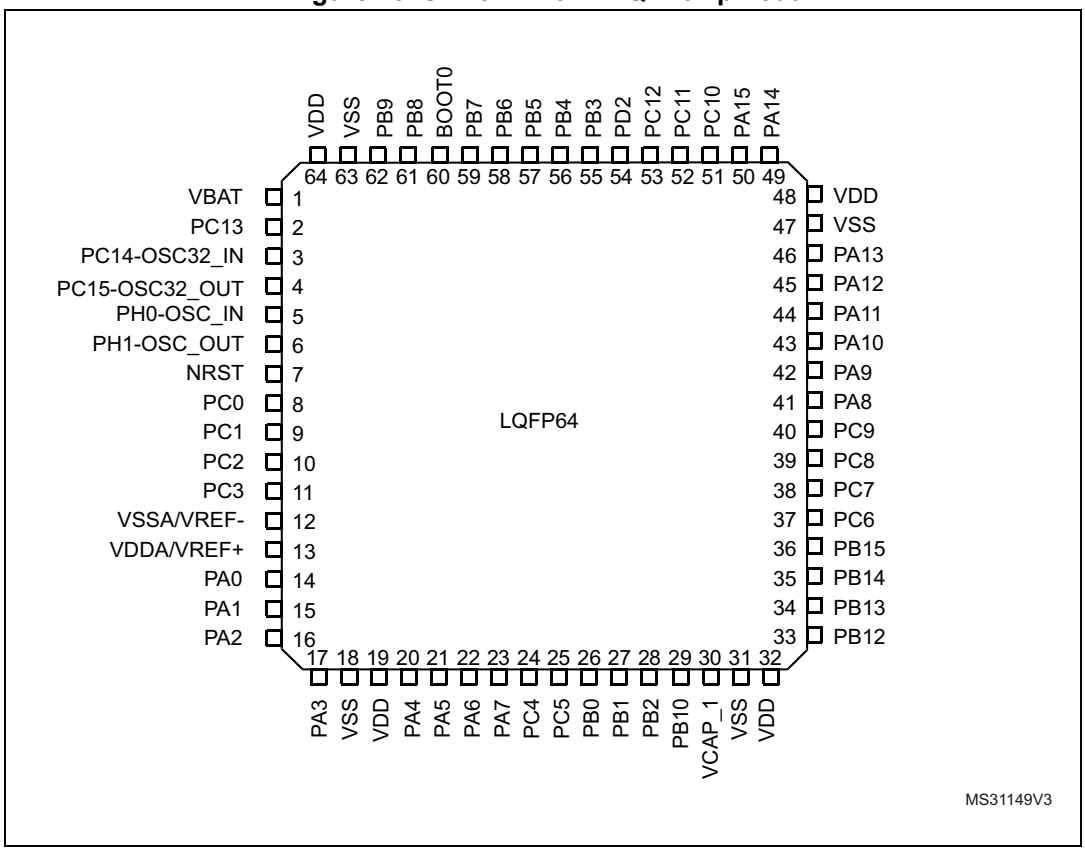
**Figure 12. STM32F423xH UFQFPN48 pinout**




1. The above figure shows the package top view.

## 4.3 LQFP64 pinout description

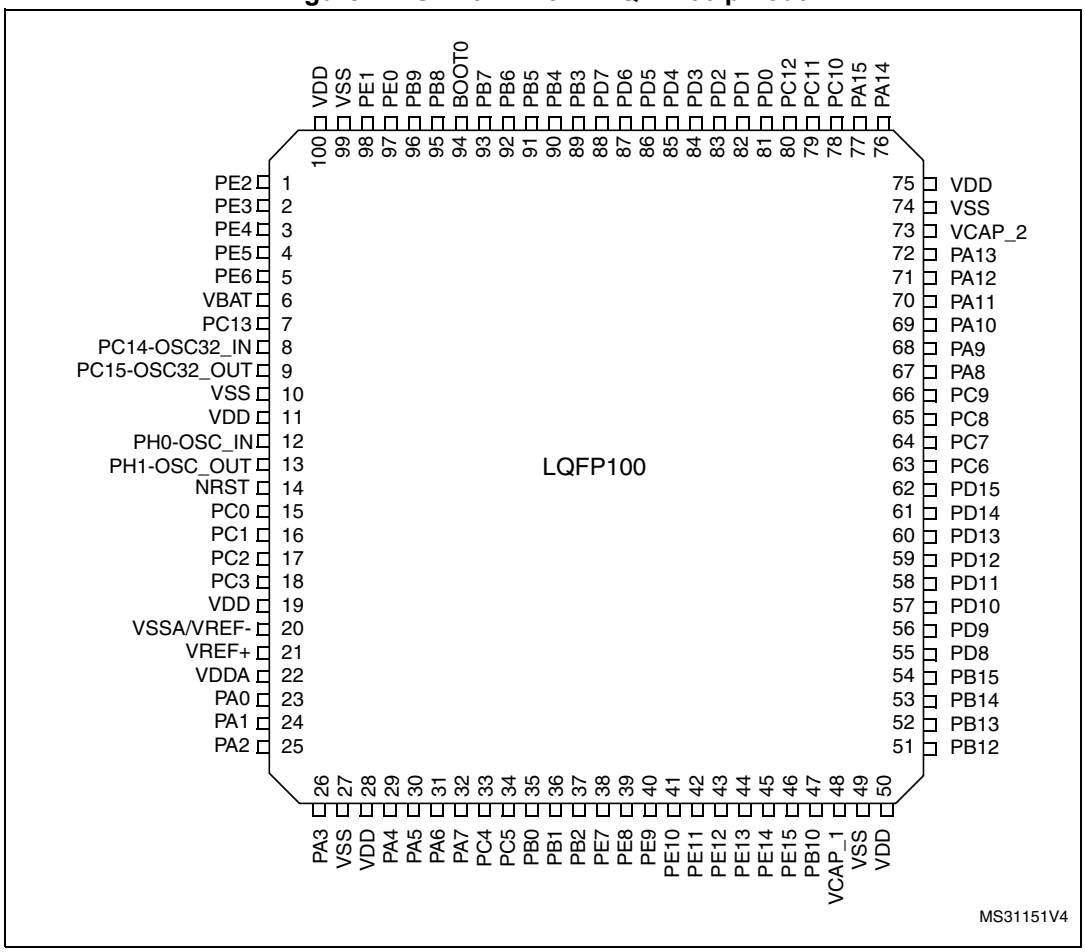
**Figure 13. STM32F423xH LQFP64 pinout**




1. The above figure shows the package top view.

## 4.4 LQFP100 pinout description

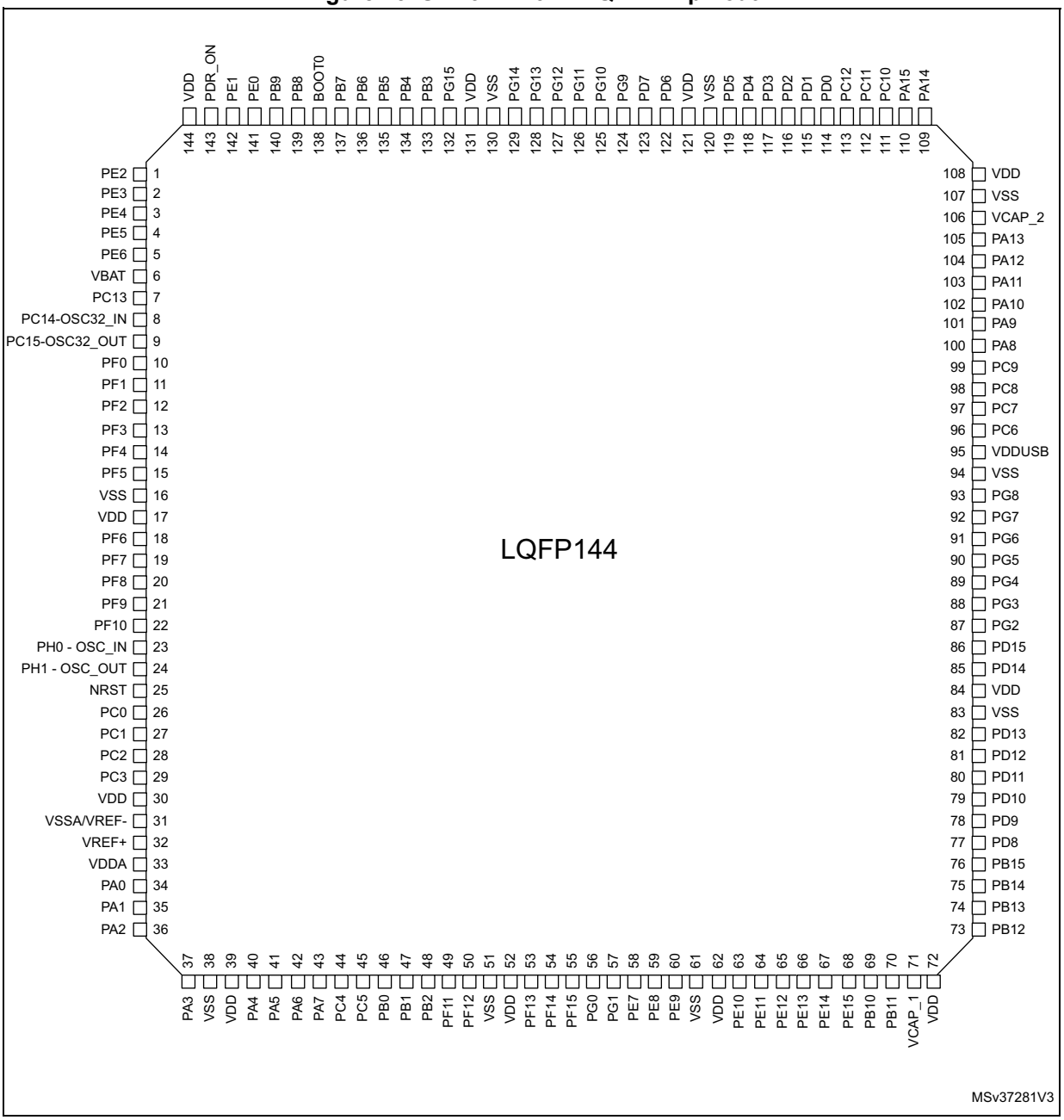
**Figure 14. STM32F423xH LQFP100 pinout**




1. The above figure shows the package top view.

## 4.5 LQFP144 pinout description

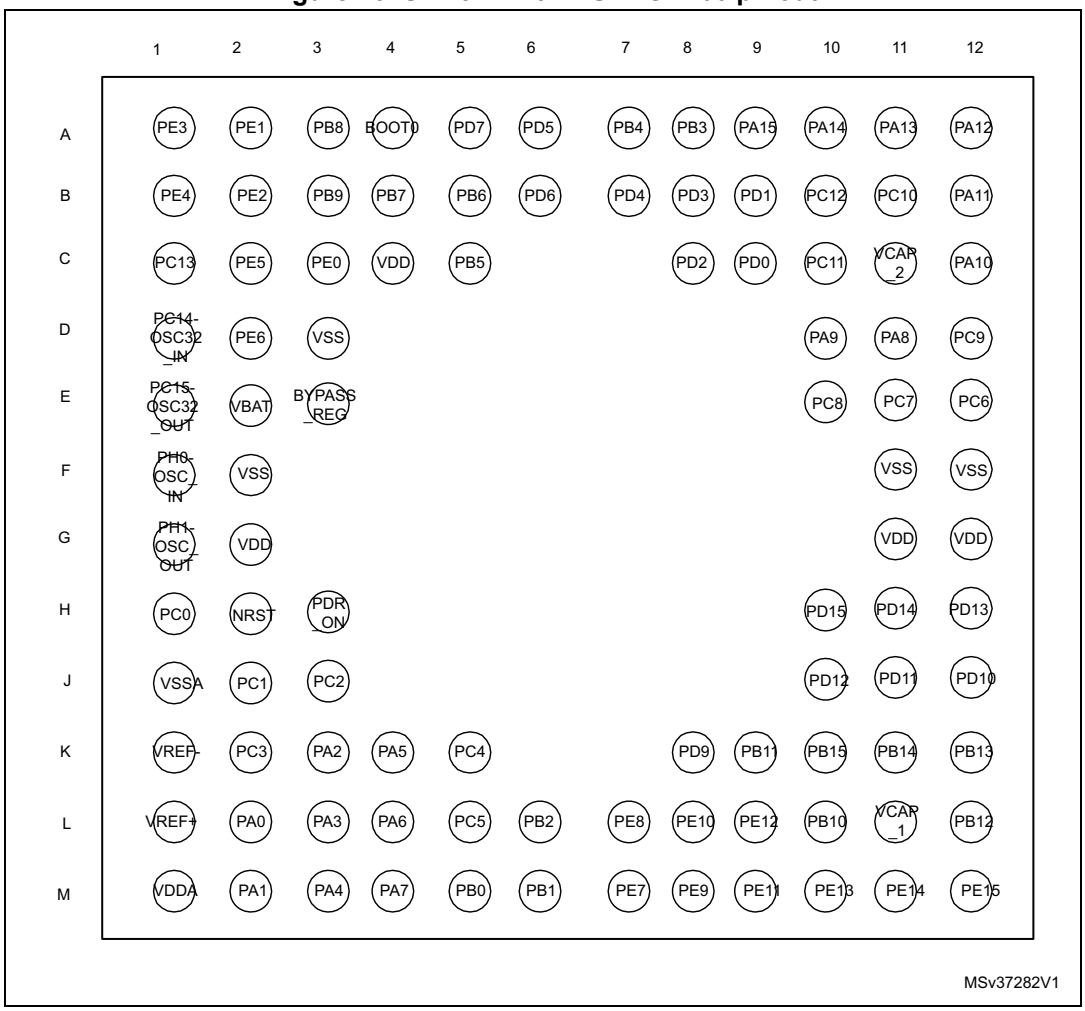
**Figure 15. STM32F423xH LQFP144 pinout**




1. The above figure shows the package top view.

## 4.6 UFBGA100 pinout description

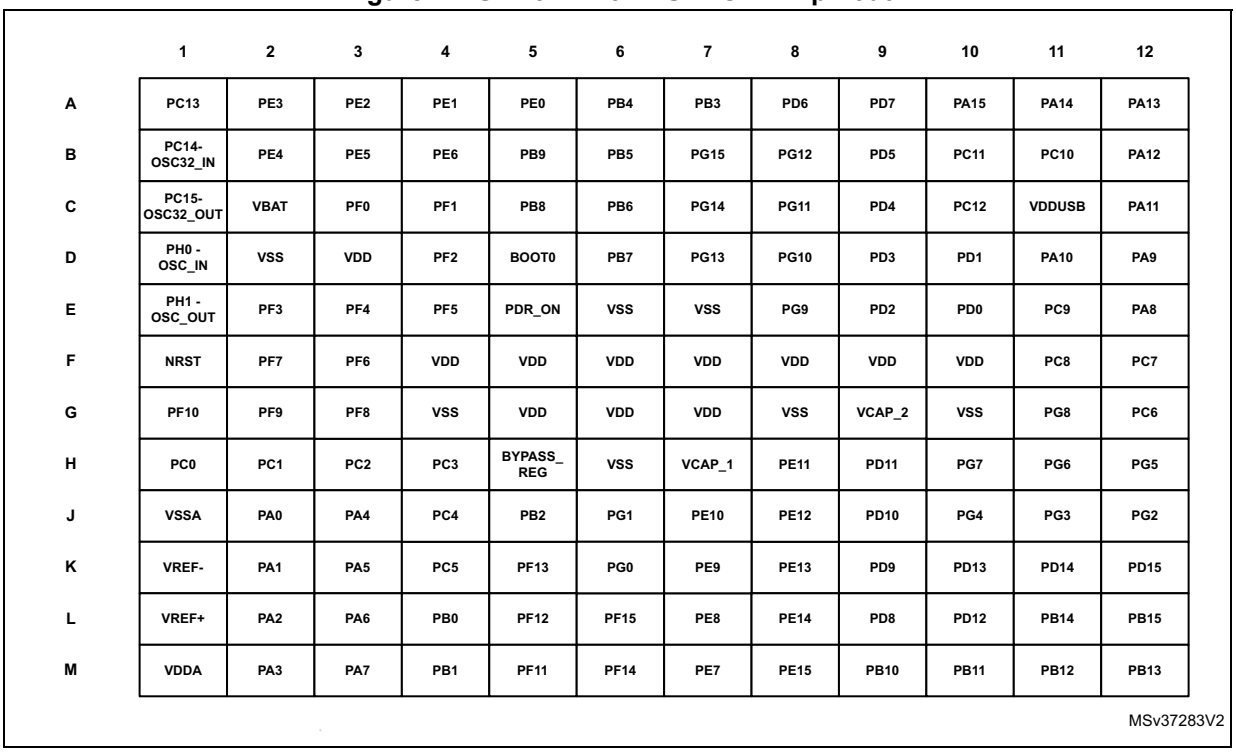
**Figure 16. STM32F423xH UFBGA100 pinout**




1. The above figure shows the package top view.

## 4.7 UFBGA144 pinout description

**Figure 17. STM32F423xH UFBGA144 pinout**



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PC13 | PE3 | PE2 | PE1 | PE0 | PB4 | PB3 | PD6 | PD7 | PA15 | PA14 | PA13 |
| B | PC14-OSC32_IN | PE4 | PE5 | PE6 | PB9 | PB5 | PG15 | PG12 | PD5 | PC11 | PC10 | PA12 |
| C | PC15-OSC32_OUT | VBAT | PF0 | PF1 | PB8 | PB6 | PG14 | PG11 | PD4 | PC12 | VDDUSB | PA11 |
| D | PH0 - OSC_IN | VSS | VDD | PF2 | BOOT0 | PB7 | PG13 | PG10 | PD3 | PD1 | PA10 | PA9 |
| E | PH1 - OSC_OUT | PF3 | PF4 | PF5 | PDR_ON | VSS | VSS | PG9 | PD2 | PD0 | PC9 | PA8 |
| F | NRST | PF7 | PF6 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | PC8 | PC7 |
| G | PF10 | PF9 | PF8 | VSS | VDD | VDD | VDD | VSS | VCAP_2 | VSS | PG8 | PC6 |
| H | PC0 | PC1 | PC2 | PC3 | BYPASS_REG | VSS | VCAP_1 | PE11 | PD11 | PG7 | PG6 | PG5 |
| J | VSSA | PA0 | PA4 | PC4 | PB2 | PG1 | PE10 | PE12 | PD10 | PG4 | PG3 | PG2 |
| K | VREF- | PA1 | PA5 | PC5 | PF13 | PG0 | PE9 | PE13 | PD9 | PD13 | PD14 | PD15 |
| L | VREF+ | PA2 | PA6 | PB0 | PF12 | PF15 | PE8 | PE14 | PD8 | PD12 | PB14 | PB15 |
| M | VDDA | PA3 | PA7 | PB1 | PF11 | PF14 | PE7 | PE15 | PB10 | PB11 | PB12 | PB13 |

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1. The above figure shows the package top view.

## 4.8 Pins definition

**Table 9. Legend/abbreviations used in the pinout table**

| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input/ output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | FTf | 5 V tolerant I/O, I2C FM+ option |
| | TC | Standard 3.3 V I/O |
| | TTa | 3.3 V tolerant I/O directly connected to DAC |
| | B | Dedicated BOOT0 pin |
| | NRST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |

**Table 9. Legend/abbreviations used in the pinout table (continued)**

| Name | Abbreviation | Definition |
|---|---|---|
| Alternate functions | Functions selected through GPIOx_AFR registers | |
| Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 10. STM32F423xH pin definition**

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | NC | 1 | B2 | A3 | 1 | PE2 | I/O | FT | (2) | TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, SAI1_MCLK_A, QUADSPI_BK1_IO2, UART10_RX, FSMC_A23, EVENTOUT | - |
| - | - | NC | 2 | A1 | A2 | 2 | PE3 | I/O | FT | (2) | TRACED0, SAI1_SD_B, UART10_TX, FSMC_A19, EVENTOUT | - |
| - | - | NC | 3 | B1 | B2 | 3 | PE4 | I/O | FT | (2)(3) | TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, SAI1_SD_A, DFSDM1_DATIN3, FSMC_A20, EVENTOUT | - |
| - | - | NC | 4 | C2 | B3 | 4 | PE5 | I/O | FT | (2) | TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, SAI1_SCK_A, DFSDM1_CKIN3, FSMC_A21, EVENTOUT | - |
| - | - | NC | 5 | D2 | B4 | 5 | PE6 | I/O | FT | (2)(3) | TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, SAI1_FS_A, FSMC_A22, EVENTOUT | - |
| 1 | 1 | B9 | 6 | E2 | C2 | 6 | VBAT | S | - | - | - | VBAT |
| 2 | 2 | C8 | 7 | C1 | A1 | 7 | PC13-ANTI_TAMP | I/O | FT | (4)(5) | EVENTOUT | TAMP_1 |
| 3 | 3 | C9 | 8 | D1 | B1 | 8 | PC14-OSC32_IN | I/O | FT | (4)(5)(6) | EVENTOUT | OSC32_IN |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| 4 | 4 | D9 | 9 | E1 | C1 | 9 | PC15-OSC32_OUT | I/O | FT | (4)(6) | EVENTOUT | OSC32_OUT |
| - | - | - | - | - | C3 | 10 | PF0 | I/O | FT | - | I2C2_SDA, FSMC_A0, EVENTOUT | - |
| - | - | - | - | - | C4 | 11 | PF1 | I/O | FT | - | I2C2_SCL, FSMC_A1, EVENTOUT | - |
| - | - | - | - | - | D4 | 12 | PF2 | I/O | FT | - | I2C2_SMBA, FSMC_A2, EVENTOUT | - |
| - | - | - | - | - | E2 | 13 | PF3 | I/O | FT | - | TIM5_CH1, FSMC_A3, EVENTOUT | - |
| - | - | - | - | - | E3 | 14 | PF4 | I/O | FT | - | TIM5_CH2, FSMC_A4, EVENTOUT | - |
| - | - | - | - | - | E4 | 15 | PF5 | I/O | FT | - | TIM5_CH3, FSMC_A5, EVENTOUT | - |
| - | - | D8 | 10 | F2 | D2 | 16 | VSS | S | - | - | - | - |
| - | - | E8 | 11 | G2 | D3 | 17 | VDD | S | - | - | - | - |
| - | - | - | - | - | F3 | 18 | PF6 | I/O | FT | - | TRACED0, TIM10_CH1, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT | - |
| - | - | - | - | - | F2 | 19 | PF7 | I/O | FT | - | TRACED1, TIM11_CH1, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT | - |
| - | - | - | - | - | G3 | 20 | PF8 | I/O | FT | - | SAI1_SCK_B, UART8_RX, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT | - |
| - | - | - | - | - | G2 | 21 | PF9 | I/O | FT | - | SAI1_FS_B, UART8_TX, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT | - |
| - | - | - | - | - | G1 | 22 | PF10 | I/O | FT | - | TIM1_ETR, TIM5_CH4, EVENTOUT | - |
| 5 | 5 | E9 | 12 | F1 | D1 | 23 | PH0 - OSC_IN | I/O | FT | (6) | EVENTOUT | OSC_IN |
| 6 | 6 | F9 | 13 | G1 | E1 | 24 | PH1 - OSC_OUT | I/O | FT | (6) | EVENTOUT | OSC_OUT |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| 7 | 7 | G9 | 14 | H2 | F1 | 25 | NRST | I/O | RST | - | - | NRST |
| - | 8 | F8 | 15 | H1 | H1 | 26 | PC0 | I/O | FT | - | LPTIM1_IN1, DFSDM2_CKIN4, SAI1_MCLK_B, EVENTOUT | ADC1_IN10, WKUP2 |
| - | 9 | C7 | 16 | J2 | H2 | 27 | PC1 | I/O | FT | - | LPTIM1_OUT, DFSDM2_DATIN4, SAI1_SD_B, EVENTOUT | ADC1_IN11, WKUP3 |
| - | 10 | D7 | 17 | J3 | H3 | 28 | PC2 | I/O | FT | - | LPTIM1_IN2, DFSDM2_DATIN7, SPI2_MISO, I2S2ext_SD, SAI1_SCK_B, DFSDM1_CKOUT, FSMC_NWE, EVENTOUT | ADC1_IN12 |
| - | 11 | E7 | 18 | K2 | H4 | 29 | PC3 | I/O | FT | - | LPTIM1_ETR, DFSDM2_CKIN7, SPI2_MOSI/I2S2_SD, SAI1_FS_B, FSMC_A0, EVENTOUT | ADC1_IN13 |
| - | - | - | 19 | - | - | 30 | VDD | S | - | - | - | - |
| 8 | 12 | H9 | 20 | J1 | J1 | 31 | VSSA | S | - | - | - | - |
| - | - | - | - | K1 | K1 | - | VREF- | S | - | - | - | - |
| - | - | G8 | 21 | L1 | L1 | 32 | VREF+ | S | - | - | - | - |
| 9 | 13 | F7 | 22 | M1 | M1 | 33 | VDDA | S | - | - | - | - |
| 10 | 14 | G7 | 23 | L2 | J2 | 34 | PA0 | I/O | FT | - | TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, EVENTOUT | ADC1_IN0, WKUP1 |
| 11 | 15 | H8 | 24 | M2 | K2 | 35 | PA1 | I/O | FT | - | TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, EVENTOUT | ADC1_IN1 |
| 12 | 16 | J9 | 25 | K3 | L2 | 36 | PA2 | I/O | FT | - | TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, FSMC_D4/FSMC_DA4, EVENTOUT | ADC1_IN2 |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| 13 | 17 | E6 | 26 | L3 | M2 | 37 | PA3 | I/O | FT | - | TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, SAI1_SD_B, FSMC_D5/FSMC_DA5, EVENTOUT | ADC1_IN3 |
| - | 18 | H7 | 27 | - | - | 38 | VSS | S | - | - | - | - |
| - | - | F6 | - | E3 | H5 | - | BYPASS_ REG | I | FT | - | - | - |
| - | 19 | J8 | 28 | - | F4 | 39 | VDD | S | - | - | - | - |
| 14 | 20 | E5 | 29 | M3 | J3 | 40 | PA4 | I/O | TTa | - | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DFSDM1_DATIN1, FSMC_D6/FSMC_DA6, EVENTOUT | ADC1_IN4, DAC_OUT1 |
| 15 | 21 | G6 | 30 | K4 | K3 | 41 | PA5 | I/O | TTa | - | TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, DFSDM1_CKIN1, FSMC_D7/FSMC_DA7, EVENTOUT | ADC1_IN5, DAC_OUT2 |
| 16 | 22 | F5 | 31 | L4 | L3 | 42 | PA6 | I/O | FT | - | TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, DFSDM2_CKIN1, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT | ADC1_IN6 |
| 17 | 23 | J7 | 32 | M4 | M3 | 43 | PA7 | I/O | FT | - | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, DFSDM2_DATIN1, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT | ADC1_IN7 |
| - | 24 | H6 | 33 | K5 | J4 | 44 | PC4 | I/O | FT | - | DFSDM2_CKIN2, I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT | ADC1_IN14 |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | 25 | J6 | 34 | L5 | K4 | 45 | PC5 | I/O | FT | - | DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT | ADC1_IN15 |
| 18 | 26 | E4 | 35 | M5 | L4 | 46 | PB0 | I/O | FT | - | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT | ADC1_IN8 |
| 19 | 27 | G5 | 36 | M6 | M4 | 47 | PB1 | I/O | FT | - | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI5_NSS/I2S5_WS, DFSDM1_DATIN0, QUADSPI_CLK, EVENTOUT | ADC1_IN9 |
| 20 | 28 | H5 | 37 | L6 | J5 | 48 | PB2 | I/O | FT | - | LPTIM1_OUT, DFSDM1_CKIN0, QUADSPI_CLK, EVENTOUT | BOOT1 |
| - | - | - | - | - | M5 | 49 | PF11 | I/O | FT | - | TIM8_ETR, EVENTOUT | - |
| - | - | - | - | - | L5 | 50 | PF12 | I/O | FT | - | TIM8_BKIN, FSMC_A6, EVENTOUT | - |
| - | - | - | - | - | G4 | 51 | VSS | S | - | - | - | - |
| - | - | - | - | - | G5 | 52 | VDD | S | - | - | - | - |
| - | - | - | - | - | K5 | 53 | PF13 | I/O | FT | - | I2CFMP1_SMBA, FSMC_A7, EVENTOUT | - |
| - | - | - | - | - | M6 | 54 | PF14 | I/O | FTf | - | I2CFMP1_SCL, FSMC_A8, EVENTOUT | - |
| - | - | - | - | - | L6 | 55 | PF15 | I/O | FTf | - | I2CFMP1_SDA, FSMC_A9, EVENTOUT | - |
| - | - | - | - | - | K6 | 56 | PG0 | I/O | FT | - | CAN1_RX, UART9_RX, FSMC_A10, EVENTOUT | - |
| - | - | - | - | - | J6 | 57 | PG1 | I/O | FT | - | CAN1_TX, UART9_TX, FSMC_A11, EVENTOUT | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | NC | 38 | M7 | M7 | 58 | PE7 | I/O | FT | (2) | TIM1_ETR, DFSDM1_DATIN2, UART7_Rx, QUADSPI_BK2_IO0, FSMC_D4/FSMC_DA4, EVENTOUT | - |
| - | - | NC | 39 | L7 | L7 | 59 | PE8 | I/O | FT | (2) | TIM1_CH1N, DFSDM1_CKIN2, UART7_Tx, QUADSPI_BK2_IO1, FSMC_D5/FSMC_DA5, EVENTOUT | - |
| - | - | J5 | 40 | M8 | K7 | 60 | PE9 | I/O | FT | - | TIM1_CH1, DFSDM1_CKOUT, QUADSPI_BK2_IO2, FSMC_D6/FSMC_DA6, EVENTOUT | - |
| - | - | - | - | - | H6 | 61 | VSS | S | - | - | - | - |
| - | - | - | - | - | G6 | 62 | VDD | S | - | - | - | - |
| - | - | G4 | 41 | L8 | J7 | 63 | PE10 | I/O | FT | - | TIM1_CH2N, DFSDM2_DATIN0, QUADSPI_BK2_IO3, FSMC_D7/FSMC_DA7, EVENTOUT | - |
| - | - | H4 | 42 | M9 | H8 | 64 | PE11 | I/O | FT | - | TIM1_CH2, DFSDM2_CKIN0, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, FSMC_D8/FSMC_DA8, EVENTOUT | - |
| - | - | J4 | 43 | L9 | J8 | 65 | PE12 | I/O | FT | - | TIM1_CH3N, DFSDM2_DATIN7, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, FSMC_D9/FSMC_DA9, EVENTOUT | - |
| - | - | F4 | 44 | M10 | K8 | 66 | PE13 | I/O | FT | - | TIM1_CH3, DFSDM2_CKIN7, SPI4_MISO, SPI5_MISO, FSMC_D10/FSMC_DA10, EVENTOUT | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | G3 | 45 | M11 | L8 | 67 | PE14 | I/O | FT | - | TIM1_CH4, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, DFSDM2_DATIN1, FSMC_D11/FSMC_DA11, EVENTOUT | - |
| - | - | J3 | 46 | M12 | M8 | 68 | PE15 | I/O | FT | - | TIM1_BKIN, DFSDM2_CKIN1, FSMC_D12/FSMC_DA12, EVENTOUT | - |
| 21 | 29 | H3 | 47 | L10 | M9 | 69 | PB10 | I/O | FTf | - | TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, I2S3_MCK, USART3_TX, I2CFMP1_SCL, DFSDM2_CKOUT, SDIO_D7, EVENTOUT | - |
| - | - | NC | - | K9 | M10 | 70 | PB11 | I/O | FT | - | TIM2_CH4, I2C2_SDA, I2S2_CKIN, USART3_RX, EVENTOUT | - |
| 22 | 30 | H2 | 48 | L11 | H7 | 71 | VCAP_1 | S | - | - | - | - |
| 23 | 31 | J2 | 49 | F12 | - | - | VSS | S | - | - | - | - |
| 24 | 32 | J1 | 50 | G12 | G7 | 72 | VDD | S | - | - | - | - |
| 25 | 33 | F3 | 51 | L12 | M11 | 73 | PB12 | I/O | FT | - | TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SPI4_NSS/I2S4_WS, SPI3_SCK/I2S3_CK, USART3_CK, CAN2_RX, DFSDM1_DATIN1, UART5_RX, FSMC_D13/FSMC_DA13, EVENTOUT | - |
| 26 | 34 | G2 | 52 | K12 | M12 | 74 | PB13 | I/O | FT | - | TIM1_CH1N, I2CFMP1_SMBA, SPI2_SCK/I2S2_CK, SPI4_SCK/I2S4_CK, USART3_CTS, CAN2_TX, DFSDM1_CKIN1, UART5_TX, EVENTOUT | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| 27 | 35 | E3 | 53 | K11 | L11 | 75 | PB14 | I/O | FTf | - | TIM1_CH2N, TIM8_CH2N, I2CFMP1_SDA, SPI2_MISO, I2S2ext_SD, USART3_RTS, DFSDM1_DATIN2, TIM12_CH1, FSMC_D0/FSMC_DA0, SDIO_D6, EVENTOUT | - |
| 28 | 36 | H1 | 54 | K10 | L12 | 76 | PB15 | I/O | FTf | - | RTC_REFIN, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT | - |
| - | - | NC | 55 | - | L9 | 77 | PD8 | I/O | FT | (2) | USART3_TX, FSMC_D13/FSMC_DA13, EVENTOUT | - |
| - | - | F2 | 56 | K8 | K9 | 78 | PD9 | I/O | FT | - | USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT | - |
| - | - | G1 | 57 | J12 | J9 | 79 | PD10 | I/O | FT | (7) | USART3_CK, UART4_TX, FSMC_D15/FSMC_DA15, EVENTOUT | - |
| - | - | NC | 58 | J11 | H9 | 80 | PD11 | I/O | FT | (2) | DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT | - |
| - | - | NC | 59 | J10 | L10 | 81 | PD12 | I/O | FTf | (2) | TIM4_CH1, DFSDM2_CKIN2, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT | - |
| - | - | NC | 60 | H12 | K10 | 82 | PD13 | I/O | FTf | (2) | TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT | - |
| - | - | - | - | - | G8 | 83 | VSS | S | - | - | - | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | - | - | - | F8 | 84 | VDD | S | - | - | - | - |
| - | - | NC | 61 | H11 | K11 | 85 | PD14 | I/O | FTf | (2) | TIM4_CH3, I2CFMP1_SCL, DFSDM2_CKIN0, UART9_RX, FSMC_D0/FSMC_DA0, EVENTOUT | - |
| - | - | NC | 62 | H10 | K12 | 86 | PD15 | I/O | FTf | (2) | TIM4_CH4, I2CFMP1_SDA, DFSDM2_DATIN0, UART9_TX, FSMC_D1/FSMC_DA1, EVENTOUT | - |
| - | - | - | - | - | J12 | 87 | PG2 | I/O | FT | - | FSMC_A12, EVENTOUT | - |
| - | - | - | - | - | J11 | 88 | PG3 | I/O | FT | - | FSMC_A13, EVENTOUT | - |
| - | - | - | - | - | J10 | 89 | PG4 | I/O | FT | - | FSMC_A14, EVENTOUT | - |
| - | - | - | - | - | H12 | 90 | PG5 | I/O | FT | - | FSMC_A15, EVENTOUT | - |
| - | - | - | - | - | H11 | 91 | PG6 | I/O | FT | - | QUADSPI_BK1_NCS, EVENTOUT | - |
| - | - | - | - | - | H10 | 92 | PG7 | I/O | FT | - | USART6_CK, EVENTOUT | - |
| - | - | - | - | - | G11 | 93 | PG8 | I/O | FT | - | USART6_RTS, EVENTOUT | - |
| - | - | - | - | - | - | 94 | VSS | S | - | - | - | - |
| - | - | - | - | - | F10 | - | VDD | S | - | - | - | - |
| - | - | F1 | - | - | C11 | 95 | VDDUSB | S | - | - | - | - |
| - | 37 | D5 | 63 | E12 | G12 | 96 | PC6 | I/O | FTf | - | TIM3_CH1, TIM8_CH1, I2CFMP1_SCL, I2S2_MCK, DFSDM1_CKIN3, DFSDM2_DATIN6, USART6_TX, FSMC_D1/FSMC_DA1, SDIO_D6, EVENTOUT | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | 38 | D4 | 64 | E11 | F12 | 97 | PC7 | I/O | FTf | - | TIM3_CH2, TIM8_CH2, I2CFMP1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, DFSDM2_CKIN6, USART6_RX, DFSDM1_DATIN3, SDIO_D7, EVENTOUT | - |
| - | 39 | E1 | 65 | E10 | F11 | 98 | PC8 | I/O | FT | - | TIM3_CH3, TIM8_CH3, DFSDM2_CKIN3, USART6_CK, QUADSPI_BK1_IO2, SDIO_D0, EVENTOUT | - |
| - | 40 | E2 | 66 | D12 | E11 | 99 | PC9 | I/O | FT | - | MCO_2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S2_CKIN, DFSDM2_DATIN3, QUADSPI_BK1_IO0, SDIO_D1, EVENTOUT | - |
| 29 | 41 | D3 | 67 | D11 | E12 | 100 | PA8 | I/O | FT | - | MCO_1, TIM1_CH1, I2C3_SCL, DFSDM1_CKOUT, USART1_CK, UART7_RX, USB_FS_SOF, CAN3_RX, SDIO_D1, EVENTOUT | - |
| 30 | 42 | D2 | 68 | D10 | D12 | 101 | PA9 | I/O | FT | - | TIM1_CH2, DFSDM2_CKIN3, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, USB_FS_VBUS, SDIO_D2, EVENTOUT | - |
| 31 | 43 | D1 | 69 | C12 | D11 | 102 | PA10 | I/O | FT | - | TIM1_CH3, DFSDM2_DATIN3, SPI2_MOSI/I2S2_SD, SPI5_MOSI/I2S5_SD, USART1_RX, USB_FS_ID, EVENTOUT | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| 32 | 44 | C3 | 70 | B12 | C12 | 103 | PA11 | I/O | FT | - | TIM1_CH4, DFSDM2_CKIN5, SPI2_NSS/I2S2_WS, SPI4_MISO, USART1_CTS, USART6_TX, CAN1_RX, USB_FS_DM, UART4_RX, EVENTOUT | - |
| 33 | 45 | B3 | 71 | A12 | B12 | 104 | PA12 | I/O | FT | - | TIM1_ETR, DFSDM2_DATIN5, SPI2_MISO, SPI5_MISO, USART1_RTS, USART6_RX, CAN1_TX, USB_FS_DP, UART4_TX, EVENTOUT | - |
| 34 | 46 | C2 | 72 | A11 | A12 | 105 | PA13 | I/O | FT | - | JTMS-SWDIO, EVENTOUT | - |
| - | - | C1 | 73 | C11 | G9 | 106 | VCAP_2 | S | - | - | - | - |
| 35 | 47 | B1 | 74 | F11 | G10 | 107 | VSS | S | - | - | - | - |
| - | 48 | - | 75 | G11 | - | - | VDD | S | - | - | - | - |
| 36 | - | A1 | - | - | F9 | 108 | VDD | S | - | - | - | - |
| 37 | 49 | B2 | 76 | A10 | A11 | 109 | PA14 | I/O | FT | - | JTCK-SWCLK, EVENTOUT | - |
| 38 | 50 | A3 | 77 | A9 | A10 | 110 | PA15 | I/O | FT | - | JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART1_TX, UART7_TX, SAI1_MCLK_A, CAN3_TX, EVENTOUT | - |
| - | 51 | A2 | 78 | B11 | B11 | 111 | PC10 | I/O | FT | - | DFSDM2_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, QUADSPI_BK1_IO1, SDIO_D2, EVENTOUT | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | 52 | C4 | 79 | C10 | B10 | 112 | PC11 | I/O | FT | - | DFSDM2_DATIN5, I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, FSMC_D2/FSMC_DA2, SDIO_D3, EVENTOUT | - |
| - | 53 | B4 | 80 | B10 | C10 | 113 | PC12 | I/O | FT | - | SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, FSMC_D3/FSMC_DA3, SDIO_CK, EVENTOUT | - |
| - | - | A4 | 81 | C9 | E10 | 114 | PD0 | I/O | FT | - | DFSDM2_CKIN6, CAN1_RX, UART4_RX, FSMC_D2/FSMC_DA2, EVENTOUT | - |
| - | - | NC | 82 | B9 | D10 | 115 | PD1 | I/O | FT | (2) | DFSDM2_DATIN6, CAN1_TX, UART4_TX, FSMC_D3/FSMC_DA3, EVENTOUT | - |
| - | 54 | C5 | 83 | C8 | E9 | 116 | PD2 | I/O | FT | - | TIM3_ETR, DFSDM2_CKOUT, UART5_RX, FSMC_NWE, SDIO_CMD, EVENTOUT | - |
| - | - | NC | 84 | B8 | D9 | 117 | PD3 | I/O | FT | (2) | TRACED1, SPI2_SCK/I2S2_CK, DFSDM1_DATIN0, USART2_CTS, QUADSPI_CLK, FSMC_CLK, EVENTOUT | - |
| - | - | NC | 85 | B7 | C9 | 118 | PD4 | I/O | FT | (2) | DFSDM1_CKIN0, USART2_RTS, FSMC_NOE, EVENTOUT | - |
| - | - | NC | 86 | A6 | B9 | 119 | PD5 | I/O | FT | (2) | DFSDM2_CKOUT, USART2_TX, FSMC_NWE, EVENTOUT | - |
| - | - | - | - | - | E7 | 120 | VSS | S | - | - | - | - |
| - | - | - | - | - | F7 | 121 | VDD | S | - | - | - | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | NC | 87 | B6 | A8 | 122 | PD6 | I/O | FT | (2) | SPI3_MOSI/I2S3_SD, DFSDM1_DATIN1, USART2_RX, FSMC_NWAIT, EVENTOUT | - |
| - | - | NC | 88 | A5 | A9 | 123 | PD7 | I/O | FT | (2) | DFSDM1_CKIN1, USART2_CK, FSMC_NE1, EVENTOUT | - |
| - | - | - | - | - | E8 | 124 | PG9 | I/O | FT | - | USART6_RX, QUADSPI_BK2_IO2, FSMC_NE2, EVENTOUT | - |
| - | - | - | - | - | D8 | 125 | PG10 | I/O | FT | - | FSMC_NE3, EVENTOUT | - |
| - | - | - | - | - | C8 | 126 | PG11 | I/O | FT | - | CAN2_RX, UART10_RX, EVENTOUT | - |
| - | - | - | - | - | B8 | 127 | PG12 | I/O | FT | - | USART6_RTS, CAN2_TX, UART10_TX, FSMC_NE4, EVENTOUT | - |
| - | - | - | - | - | D7 | 128 | PG13 | I/O | FT | - | TRACED2, USART6_CTS, FSMC_A24, EVENTOUT | - |
| - | - | - | - | - | C7 | 129 | PG14 | I/O | FT | - | TRACED3, USART6_TX, QUADSPI_BK2_IO3, FSMC_A25, EVENTOUT | - |
| - | - | - | - | - | - | 130 | VSS | S | - | - | - | - |
| - | - | - | - | - | F6 | 131 | VDD | S | - | - | - | - |
| - | - | - | - | - | B7 | 132 | PG15 | I/O | FT | - | USART6_CTS, EVENTOUT | - |
| 39 | 55 | A5 | 89 | A8 | A7 | 133 | PB3 | I/O | FTf | - | JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, UART7_RX, I2C2_SDA, SAI1_SD_A, CAN3_RX, EVENTOUT | - |

Table 10. STM32F423xH pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| 40 | 56 | B5 | 90 | A7 | A6 | 134 | PB4 | I/O | FT | - | JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, UART7_TX, I2C3_SDA, SAI1_SCK_A, CAN3_TX, SDIO_D0, EVENTOUT | - |
| 41 | 57 | A6 | 91 | C5 | B6 | 135 | PB5 | I/O | FT | - | LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, SAI1_FS_A, UART5_RX, SDIO_D3, EVENTOUT | - |
| 42 | 58 | B6 | 92 | B5 | C6 | 136 | PB6 | I/O | FT | - | LPTIM1_ETR, TIM4_CH1, I2C1_SCL, DFSDM2_CKIN7, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, UART5_TX, SDIO_D0, EVENTOUT | - |
| 43 | 59 | B7 | 93 | B4 | D6 | 137 | PB7 | I/O | FT | - | LPTIM1_IN2, TIM4_CH2, I2C1_SDA, DFSDM2_DATIN7, USART1_RX, FSMC_NL, EVENTOUT | - |
| 44 | 60 | A7 | 94 | A4 | D5 | 138 | BOOT0 | I | B | - | - | VPP |
| 45 | 61 | C6 | 95 | A3 | C5 | 139 | PB8 | I/O | FT | - | LPTIM1_OUT, TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, DFSDM2_CKIN1, CAN1_RX, I2C3_SDA, UART5_RX, SDIO_D4, EVENTOUT | - |
| 46 | 62 | D6 | 96 | B3 | B5 | 140 | PB9 | I/O | FT | - | TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM2_DATIN1, CAN1_TX, I2C2_SDA, UART5_TX, SDIO_D5, EVENTOUT | - |

**Table 10. STM32F423xH pin definition (continued)**

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | NC | 97 | C3 | A5 | 141 | PE0 | I/O | FT | (2) | TIM4_ETR, DFSDM2_CKIN4, UART8_Rx, FSMC_NBL0, EVENTOUT | - |
| - | - | NC | 98 | A2 | A4 | 142 | PE1 | I/O | FT | (2) | DFSDM2_DATIN4, UART8_Tx, FSMC_NBL1, EVENTOUT | - |
| 47 | 63 | A8 | 99 | D3 | E6 | - | VSS | S | - | - | - | - |
| - | - | B8 | - | H3 | E5 | 143 | PDR_ON | I | FT | - | - | - |
| 48 | 64 | A9 | 100 | C4 | F5 | 144 | VDD | S | - | - | - | - |

1. Function availability depends on the chosen device.
2. NC (Not Connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra power consumption in low power mode.
3. Compatibility issue on alternate function pin PE4 SAI1_SD_A and PE6 SAI1_FS_A: Pins have been swapped versus other MCUs supporting those alternate SAI functions on those pins
4. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F413/423 reference manual.
6. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
7. Incompatibility issue on alternate function with other MCUs supporting UART4: UART4_TX wrongly mapped to PD10 instead of PC10

**Table 11. FSMC pin definition**

| Pins | FSMC | | 64 pins | 81 pins | 100 pins | 144 pins |
|---|---|---|---|---|---|---|
| | LCD/NOR/ PSRAM/SRAM | NOR/PSRAM Mux | | | | |
| PE2 | A23 | A23 | - | - | Yes | Yes |
| PE3 | A19 | A19 | - | - | Yes | Yes |
| PE4 | A20 | A20 | - | - | Yes | Yes |
| PE5 | A21 | A21 | - | - | Yes | Yes |
| PE6 | A22 | A22 | - | - | Yes | Yes |
| PF0 | A0 | - | - | - | - | Yes |

Table 11. FSMC pin definition (continued)

| Pins | FSMC | | 64 pins | 81 pins | 100 pins | 144 pins |
|---|---|---|---|---|---|---|
| | LCD/NOR/ PSRAM/SRAM | NOR/PSRAM Mux | | | | |
| PF1 | A1 | - | - | - | - | Yes |
| PF2 | A2 | - | - | - | - | Yes |
| PF3 | A3 | - | - | - | - | Yes |
| PF4 | A4 | - | - | - | - | Yes |
| PF5 | A5 | - | - | - | - | Yes |
| PC2 | NWE | NWE | Yes | Yes | Yes | Yes |
| PC3 | A0 | - | Yes | Yes | Yes | Yes |
| PA2 | D4 | DA4 | Yes | Yes | Yes | Yes |
| PA3 | D5 | DA5 | Yes | Yes | Yes | Yes |
| PA4 | D6 | DA6 | Yes | Yes | Yes | Yes |
| PA5 | D7 | DA7 | Yes | Yes | Yes | Yes |
| PC4 | NE4 | NE4 | Yes | Yes | Yes | Yes |
| PC5 | NOE | NOE | Yes | Yes | Yes | Yes |
| PF12 | A6 | - | - | - | - | Yes |
| PF13 | A7 | - | - | - | - | Yes |
| PF14 | A8 | - | - | - | - | Yes |
| PF15 | A9 | - | - | - | - | Yes |
| PG0 | A10 | - | - | - | - | Yes |
| PG1 | A11 | - | - | - | - | Yes |
| PE7 | D4 | DA4 | - | - | Yes | Yes |
| PE8 | D5 | DA5 | - | - | Yes | Yes |
| PE9 | D6 | DA6 | - | Yes | Yes | Yes |
| PE10 | D7 | DA7 | - | Yes | Yes | Yes |
| PE11 | D8 | DA8 | - | Yes | Yes | Yes |
| PE12 | D9 | DA9 | - | Yes | Yes | Yes |
| PE13 | D10 | DA10 | - | Yes | Yes | Yes |
| PE14 | D11 | DA11 | - | Yes | Yes | Yes |
| PE15 | D12 | DA12 | - | Yes | Yes | Yes |
| PB12 | D13 | DA13 | Yes | Yes | Yes | Yes |
| PB14 | D0 | DA0 | Yes | Yes | Yes | Yes |
| PD8 | D13 | DA13 | - | - | - | Yes |
| PD9 | D14 | DA14 | - | Yes | Yes | Yes |
| PD10 | D15 | DA15 | - | Yes | Yes | Yes |

Table 11. FSMC pin definition (continued)

| Pins | FSMC | | 64 pins | 81 pins | 100 pins | 144 pins |
|---|---|---|---|---|---|---|
| | LCD/NOR/ PSRAM/SRAM | NOR/PSRAM Mux | | | | |
| PD11 | A16 | A16 | - | - | Yes | Yes |
| PD12 | A17 | A17 | - | - | Yes | Yes |
| PD13 | A18 | A18 | - | - | Yes | Yes |
| PD14 | D0 | DA0 | - | - | Yes | Yes |
| PD15 | D1 | DA1 | - | - | Yes | Yes |
| PG2 | A12 | - | - | - | - | Yes |
| PG3 | A13 | - | - | - | - | Yes |
| PG4 | A14 | - | - | - | - | Yes |
| PG5 | A15 | - | - | - | - | Yes |
| PC6 | D1 | DA1 | Yes | Yes | Yes | Yes |
| PC11 | D2 | DA2 | Yes | Yes | Yes | Yes |
| PC12 | D3 | DA3 | Yes | Yes | Yes | Yes |
| PD0 | D2 | DA2 | - | Yes | Yes | Yes |
| PD1 | D3 | DA3 | - | - | Yes | Yes |
| PD2 | NWE | NWE | Yes | Yes | Yes | Yes |
| PD3 | CLK | CLK | - | - | Yes | Yes |
| PD4 | NOE | NOE | - | - | Yes | Yes |
| PD5 | NWE | NWE | - | - | Yes | Yes |
| PD6 | NWAIT | NWAIT | - | - | Yes | Yes |
| PD7 | NE1 | NE1 | - | - | Yes | Yes |
| PG9 | NE2 | NE2 | - | - | - | Yes |
| PG10 | NE3 | NE3 | - | - | - | Yes |
| PG12 | NE4 | NE4 | - | - | - | Yes |
| PG13 | A24 | A24 | - | - | - | Yes |
| PG14 | A25 | A25 | - | - | - | Yes |
| PB7 | NL | NL | Yes | Yes | Yes | Yes |
| PE0 | NBL0 | NBL0 | - | - | Yes | Yes |
| PE1 | NBL1 | NBL1 | - | - | Yes | Yes |

## 4.9 Alternate functions

**Table 12. STM32F423xH alternate functions**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_ AF | TIM1/2/ LPTIM1 | TIM3/4/5 | DFSDM2/ TIM8/9/10/11 | I2C1/2/3/ I2CFMP1 | SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4 | SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2 | SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3 | DFSDM1/ USART3/4/ 5/6/7/8/ CAN1 | I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI | SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS | UART4/ UART5/ UART9/ UART10 /CAN3 | FSMC /SDIO | - | RNG | SYS_ AF |
| Port A | PA0 | - | TIM2_CH1/ TIM2_ ETR | TIM5_ CH1 | TIM8_ETR | - | - | - | USART2_ CTS | UART4_ TX | - | - | - | - | - | - | EVENT OUT |
| | PA1 | - | TIM2_CH2 | TIM5_ CH2 | - | - | SPI4_MOSI/I 2S4_SD | - | USART2_ RTS | UART4_ RX | QUADSPI_ BK1_IO3 | - | - | - | - | - | EVENT OUT |
| | PA2 | - | TIM2_CH3 | TIM5_ CH3 | TIM9_CH1 | - | I2S2_CKIN | - | USART2_ TX | - | - | - | - | FSMC_D4/ FSMC_DA4 | - | - | EVENT OUT |
| | PA3 | - | TIM2_CH4 | TIM5_ CH4 | TIM9_CH2 | - | I2S2_MCK | - | USART2_ RX | - | - | SAI1_SD_B | - | FSMC_D5/ FSMC_DA5 | - | - | EVENT OUT |
| | PA4 | - | - | - | - | - | SPI1_NSS/I2 S1_WS | SPI3_NSS/I 2S3_WS | USART2_ CK | DFSDM1_ DATIN1 | - | - | - | FSMC_D6/ FSMC_DA6 | - | - | EVENT OUT |
| | PA5 | - | TIM2_CH1/ TIM2_ ETR | - | TIM8_CH1N | - | SPI1_SCK/I2 S1_CK | - | - | DFSDM1_ CKIN1 | - | - | - | FSMC_D7/ FSMC_DA7 | - | - | EVENT OUT |
| | PA6 | - | TIM1_ BKIN | TIM3_ CH1 | TIM8_BKIN | - | SPI1_MISO | I2S2_MCK | DFSDM2_ CKIN1 | - | TIM13_ CH1 | QUADSPI_B K2_IO0 | - | SDIO_ CMD | - | - | EVENT OUT |
| | PA7 | - | TIM1_ CH1N | TIM3_ CH2 | TIM8_ CH1N | - | SPI1_MOSI/I 2S1_SD | - | DFSDM2_ DATIN1 | - | TIM14_ CH1 | QUADSPI_B K2_IO1 | - | - | - | - | EVENT OUT |
| | PA8 | MCO_1 | TIM1_CH1 | - | - | I2C3_ SCL | - | DFSDM1_ CKOUT | USART1_ CK | UART7_ RX | - | USB_FS_ SOF | CAN3_ RX | SDIO_ D1 | - | - | EVENT OUT |
| | PA9 | - | TIM1_CH2 | - | DFSDM2_ CKIN3 | I2C3_ SMBA | SPI2_SCK/I2 S2_CK | - | USART1_ TX | - | - | USB_FS_ VBUS | - | SDIO_ D2 | - | - | EVENT OUT |
| | PA10 | - | TIM1_CH3 | - | DFSDM2_ DATIN3 | - | SPI2_MOSI/I 2S2_SD | SPI5_MOSI/ I2S5_SD | USART1_ RX | - | - | USB_FS_ ID | - | - | - | - | EVENT OUT |
| | PA11 | - | TIM1_CH4 | - | DFSDM2_ CKIN5 | - | SPI2_NSS/I2 S2_WS | SPI4_MISO | USART1_ CTS | USART6_ TX | CAN1_RX | USB_FS_ DM | UART4_ RX | - | - | - | EVENT OUT |
| | PA12 | - | TIM1_ETR | - | DFSDM2_ DATIN5 | - | SPI2_MISO | SPI5_MISO | USART1_ RTS | USART6_ RX | CAN1_TX | USB_FS_ DP | UART4_ TX | - | - | - | EVENT OUT |
| | PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT OUT |
| | PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT OUT |
| | PA15 | JTDI | TIM2_CH1/ TIM2_ ETR | - | - | - | SPI1_NSS/ I2S1_WS | SPI3_NSS/ I2S3_WS | USART1_ TX | UART7_ TX | - | SAI1_ MCLK_A | CAN3_ TX | - | - | - | EVENT OUT |

**Table 12. STM32F423xH alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/2/ LPTIM1 | TIM3/4/5 | DFSDM2/ TIM8/9/10/11 | I2C1/2/3/ I2CFMP1 | SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4 | SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2 | SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3 | DFSDM1/ USART3/4/ 5/6/7/8/ CAN1 | I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI | SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS | UART4/ UART5/ UART9/ UART10 /CAN3 | FSMC /SDIO | - | RNG | SYS_AF |
| Port B | PB0 | - | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | - | - | SPI5_SCK/I2S5_CK | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | - | - | SPI5_NSS/I2S5_WS | - | DFSDM1_DATIN0 | QUADSPI_CLK | - | - | - | - | - | EVENTOUT |
| | PB2 | - | LPTIM1_OUT | - | - | - | - | DFSDM1_CKIN0 | - | - | QUADSPI_CLK | - | - | - | - | - | EVENTOUT |
| | PB3 | JTDO-SWO | TIM2_CH2 | - | - | I2CFMP1_SDA | SPI1_SCK/I2S1_CK | SPI3_SCK/I2S3_CK | USART1_RX | UART7_RX | I2C2_SDA | SAI1_SD_A | CAN3_RX | - | - | - | EVENTOUT |
| | PB4 | JTRST | - | TIM3_CH1 | - | - | SPI1_MISO | SPI3_MISO | I2S3ext_SD | UART7_TX | I2C3_SDA | SAI1_SCK_A | CAN3_TX | SDIO_D0 | - | - | EVENTOUT |
| | PB5 | - | LPTIM1_IN1 | TIM3_CH2 | - | I2C1_SMBA | SPI1_MOSI/I2S1_SD | SPI3_MOSI/I2S3_SD | - | - | CAN2_RX | SAI1_FS_A | UART5_RX | SDIO_D3 | - | - | EVENTOUT |
| | PB6 | - | LPTIM1_ETR | TIM4_CH1 | - | I2C1_SCL | - | DFSDM2_CKIN7 | USART1_TX | - | CAN2_TX | QUADSPI_BK1_NCS | UART5_TX | SDIO_D0 | - | - | EVENTOUT |
| | PB7 | - | LPTIM1_IN2 | TIM4_CH2 | - | I2C1_SDA | - | DFSDM2_DATIN7 | USART1_RX | - | - | - | - | FSMC_NL | - | - | EVENTOUT |
| | PB8 | - | LPTIM1_OUT | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | - | SPI5_MOSI/I2S5_SD | DFSDM2_CKIN1 | CAN1_RX | I2C3_SDA | - | UART5_RX | SDIO_D4 | - | - | EVENTOUT |
| | PB9 | - | - | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS/I2S2_WS | DFSDM2_DATIN1 | - | CAN1_TX | I2C2_SDA | - | UART5_TX | SDIO_D5 | - | - | EVENTOUT |
| | PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | SPI2_SCK/I2S2_CK | I2S3_MCK | USART3_TX | - | I2CFMP1_SCL | DFSDM2_CKOUT | - | SDIO_D7 | - | - | EVENTOUT |
| | PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | I2S2_CKIN | - | USART3_RX | - | - | - | - | - | - | - | EVENTOUT |
| | PB12 | - | TIM1_BKIN | - | - | I2C2_SMBA | SPI2_NSS/I2S2_WS | SPI4_NSS/I2S4_WS | SPI3_SCK/I2S3_CK | USART3_CK | CAN2_RX | DFSDM1_DATIN1 | UART5_RX | FSMC_D13/FSMC_DA13 | - | - | EVENTOUT |
| | PB13 | - | TIM1_CH1N | - | - | I2CFMP1_SMBA | SPI2_SCK/I2S2_CK | SPI4_SCK/I2S4_CK | - | USART3_CTS | CAN2_TX | DFSDM1_CKIN1 | UART5_TX | - | - | - | EVENTOUT |
| | PB14 | - | TIM1_CH2N | - | TIM8_CH2N | I2CFMP1_SDA | SPI2_MISO | I2S2ext_SD | USART3_RTS | DFSDM1_DATIN2 | TIM12_CH1 | FSMC_D0/FSMC_DA0 | - | SDIO_D6 | - | - | EVENTOUT |
| | PB15 | RTC_REFIN | TIM1_CH3N | - | TIM8_CH3N | I2CFMP1_SCL | SPI2_MOSI/I2S2_SD | - | - | DFSDM1_CKIN2 | TIM12_CH2 | - | - | SDIO_CK | - | - | EVENTOUT |

**Table 12. STM32F423xH alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/2/ LPTIM1 | TIM3/4/5 | DFSDM2/ TIM8/9/10/11 | I2C1/2/3/ I2CFMP1 | SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4 | SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2 | SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3 | DFSDM1/ USART3/4/ 5/6/7/8/ CAN1 | I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI | SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS | UART4/ UART5/ UART9/ UART10 /CAN3 | FSMC /SDIO | - | RNG | SYS_AF |
| Port C | PC0 | - | LPTIM1_IN1 | - | DFSDM2_CKIN4 | - | - | - | SAI1_MCLK_B | - | - | - | - | - | - | - | EVENTOUT |
| | PC1 | - | LPTIM1_OUT | - | DFSDM2_DATIN4 | - | - | - | SAI1_SD_B | - | - | - | - | - | - | - | EVENTOUT |
| | PC2 | - | LPTIM1_IN2 | - | DFSDM2_DATIN7 | - | SPI2_MISO | I2S2ext_SD | SAI1_SCK_B | DFSDM1_CKOUT | - | - | - | FSMC_NWE | - | - | EVENTOUT |
| | PC3 | - | LPTIM1_ETR | - | DFSDM2_CKIN7 | - | SPI2_MOSI/I2S2_SD | - | SAI1_FS_B | - | - | - | - | FSMC_A0 | - | - | EVENTOUT |
| | PC4 | - | - | - | DFSDM2_CKIN2 | - | I2S1_MCK | - | - | - | - | QUADSPI_BK2_IO2 | - | FSMC_NE4 | - | - | EVENTOUT |
| | PC5 | - | - | - | DFSDM2_DATIN2 | I2CFMP1_SMBA | - | - | USART3_RX | - | - | QUADSPI_BK2_IO3 | - | FSMC_NOE | - | - | EVENTOUT |
| | PC6 | - | - | TIM3_CH1 | TIM8_CH1 | I2CFMP1_SCL | I2S2_MCK | DFSDM1_CKIN3 | DFSDM2_DATIN6 | USART6_TX | - | FSMC_D1/ FSMC_DA1 | - | SDIO_D6 | - | - | EVENTOUT |
| | PC7 | - | - | TIM3_CH2 | TIM8_CH2 | I2CFMP1_SDA | SPI2_SCK/ I2S2_CK | I2S3_MCK | DFSDM2_CKIN6 | USART6_RX | - | DFSDM1_DATIN3 | - | SDIO_D7 | - | - | EVENTOUT |
| | PC8 | - | - | TIM3_CH3 | TIM8_CH3 | - | - | - | DFSDM2_CKIN3 | USART6_CK | QUADSPI_BK1_IO2 | - | - | SDIO_D0 | - | - | EVENTOUT |
| | PC9 | MCO_2 | - | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S2_CKIN | - | DFSDM2_DATIN3 | - | QUADSPI_BK1_IO0 | - | - | SDIO_D1 | - | - | EVENTOUT |
| | PC10 | - | - | - | DFSDM2_CKIN5 | - | - | SPI3_SCK/ I2S3_CK | USART3_TX | - | QUADSPI_BK1_IO1 | - | - | SDIO_D2 | - | - | EVENTOUT |
| | PC11 | - | - | - | DFSDM2_DATIN5 | - | I2S3ext_SD | SPI3_MISO | USART3_RX | UART4_RX | QUADSPI_BK2_NCS | FSMC_D2/ FSMC_DA2 | - | SDIO_D3 | - | - | EVENTOUT |
| | PC12 | - | - | - | - | - | - | SPI3_MOSI/ I2S3_SD | USART3_CK | UART5_TX | - | FSMC_D3/FSMC_DA3 | - | SDIO_CK | - | - | EVENTOUT |
| | PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

**Table 12. STM32F423xH alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/2/ LPTIM1 | TIM3/4/5 | DFSDM2/ TIM8/9/10/11 | I2C1/2/3/ I2CFMP1 | SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4 | SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2 | SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3 | DFSDM1/ USART3/4/ 5/6/7/8/ CAN1 | I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI | SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS | UART4/ UART5/ UART9/ UART10 /CAN3 | FSMC /SDIO | - | RNG | SYS_AF |
| Port D | PD0 | - | - | - | DFSDM2_CKIN6 | - | - | - | - | - | CAN1_RX | - | UART4_RX | FSMC_D2/ FSMC_DA2 | - | - | EVENTOUT |
| | PD1 | - | - | - | DFSDM2_DATIN6 | - | - | - | - | - | CAN1_TX | - | UART4_TX | FSMC_D3/ FSMC_DA3 | - | - | EVENTOUT |
| | PD2 | - | - | TIM3_ETR | DFSDM2_CKOUT | - | - | - | - | UART5_RX | - | FSMC_NWE | - | SDIO_CMD | - | - | EVENTOUT |
| | PD3 | TRACED1 | - | - | - | - | SPI2_SCK/ I2S2_CK | DFSDM1_DATIN0 | USART2_CTS | - | QUADSPI_CLK | - | - | FSMC_CLK | - | - | EVENTOUT |
| | PD4 | - | - | - | - | - | - | DFSDM1_CKIN0 | USART2_RTS | - | - | - | - | FSMC_NOE | - | - | EVENTOUT |
| | PD5 | - | - | - | DFSDM2_CKOUT | - | - | - | USART2_TX | - | - | - | - | FSMC_NWE | - | - | EVENTOUT |
| | PD6 | - | - | - | - | - | SPI3_MOSI/ I2S3_SD | DFSDM1_DATIN1 | USART2_RX | - | - | - | - | FSMC_NWAIT | - | - | EVENTOUT |
| | PD7 | - | - | - | - | - | - | DFSDM1_CKIN1 | USART2_CK | - | - | - | - | FSMC_NE1 | - | - | EVENTOUT |
| | PD8 | - | - | - | - | - | - | - | USART3_TX | - | - | - | - | FSMC_D13/FSMC_DA13 | - | - | EVENTOUT |
| | PD9 | - | - | - | - | - | - | - | USART3_RX | - | - | - | - | FSMC_D14/FSMC_DA14 | - | - | EVENTOUT |
| | PD10 | - | - | - | - | - | - | - | USART3_CK | UART4_TX | - | - | - | FSMC_D15/FSMC_DA15 | - | - | EVENTOUT |
| | PD11 | - | - | - | DFSDM2_DATIN2 | I2CFMP1_SMBA | - | - | USART3_CTS | - | QUADSPI_BK1_IO0 | - | - | FSMC_A16 | - | - | EVENTOUT |
| | PD12 | - | - | TIM4_CH1 | DFSDM2_CKIN2 | I2CFMP1_SCL | - | - | USART3_RTS | - | QUADSPI_BK1_IO1 | - | - | FSMC_A17 | - | - | EVENTOUT |
| | PD13 | - | - | TIM4_CH2 | - | I2CFMP1_SDA | - | - | - | - | QUADSPI_BK1_IO3 | - | - | FSMC_A18 | - | - | EVENTOUT |
| | PD14 | - | - | TIM4_CH3 | - | I2CFMP1_SCL | - | - | - | - | - | DFSDM2_CKIN0 | UART9_RX | FSMC_D0/ FSMC_DA0 | - | - | EVENTOUT |
| | PD15 | - | - | TIM4_CH4 | - | I2CFMP1_SDA | - | - | - | - | - | DFSDM2_DATIN0 | UART9_TX | FSMC_D1/ FSMC_DA1 | - | - | EVENTOUT |

**Table 12. STM32F423xH alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/2/ LPTIM1 | TIM3/4/5 | DFSDM2/ TIM8/9/10/11 | I2C1/2/3/ I2CFMP1 | SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4 | SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2 | SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3 | DFSDM1/ USART3/4/ 5/6/7/8/ CAN1 | I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI | SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS | UART4/ UART5/ UART9/ UART10 /CAN3 | FSMC /SDIO | - | RNG | SYS_AF |
| Port E | PE0 | - | - | TIM4_ ETR | DFSDM2_ CKIN4 | - | - | - | - | UART8_ Rx | - | - | - | FSMC_ NBL0 | - | - | EVENT OUT |
| | PE1 | - | - | - | DFSDM2_ DATIN4 | - | - | - | - | UART8_ Tx | - | - | - | FSMC_ NBL1 | - | - | EVENT OUT |
| | PE2 | TRACE CLK | - | - | - | - | SPI4_SCK /I2S4_CK | SPI5_SCK/ I2S5_CK | SAI1_ MCLK_A | - | QUADSPI_ BK1_IO2 | - | UART10 _RX | FSMC_A23 | - | - | EVENT OUT |
| | PE3 | TRACE D0 | - | - | - | - | - | - | SAI1_SD_B | - | - | - | UART10 _TX | FSMC_A19 | - | - | EVENT OUT |
| | PE4 | TRACE D1 | - | - | - | - | SPI4_NSS/ I2S4_WS | SPI5_NSS/ I2S5_WS | SAI1_SD_A | DFSDM1_ DATIN3 | - | - | - | FSMC_A20 | - | - | EVENT OUT |
| | PE5 | TRACE D2 | - | - | TIM9_CH1 | - | SPI4_MISO | SPI5_MISO | SAI1_SCK_ A | DFSDM1_ CKIN3 | - | - | - | FSMC_A21 | - | - | EVENT OUT |
| | PE6 | TRACE D3 | - | - | TIM9_CH2 | - | SPI4_MOSI/I 2S4_SD | SPI5_MOSI/ I2S5_SD | SAI1_FS_A | - | - | - | - | FSMC_A22 | - | - | EVENT OUT |
| | PE7 | - | TIM1_ETR | - | - | - | - | DFSDM1_ DATIN2 | - | UART7_ Rx | - | QUADSPI_ BK2_IO0 | - | FSMC_D4/ FSMC_DA4 | - | - | EVENT OUT |
| | PE8 | - | TIM1_ CH1N | - | - | - | - | DFSDM1_ CKIN2 | - | UART7_ Tx | - | QUADSPI_ BK2_IO1 | - | FSMC_D5/ FSMC_DA5 | - | - | EVENT OUT |
| | PE9 | - | TIM1_CH1 | - | - | - | - | DFSDM1_ CKOUT | - | - | - | QUADSPI_ BK2_IO2 | - | FSMC_D6/ FSMC_DA6 | - | - | EVENT OUT |
| | PE10 | - | TIM1_ CH2N | - | DFSDM2_ DATIN0 | - | - | - | - | - | - | QUADSPI_ BK2_IO3 | - | FSMC_D7/ FSMC_DA7 | - | - | EVENT OUT |
| | PE11 | - | TIM1_ CH2 | - | DFSDM2_ CKIN0 | - | SPI4_NSS/ I2S4_WS | SPI5_NSS/ I2S5_WS | - | - | - | - | - | FSMC_D8/ FSMC_DA8 | - | - | EVENT OUT |
| | PE12 | - | TIM1_ CH3N | - | DFSDM2_ DATIN7 | - | SPI4_SCK/ I2S4_CK | SPI5_SCK/ I2S5_CK | - | - | - | - | - | FSMC_D9/ FSMC_DA9 | - | - | EVENT OUT |
| | PE13 | - | TIM1_ CH3 | - | DFSDM2_ CKIN7 | - | SPI4_MISO | SPI5_MISO | - | - | - | - | - | FSMC_D10/ FSMC_DA10 | - | - | EVENT OUT |
| | PE14 | - | TIM1_ CH4 | - | - | - | SPI4_MOSI/I 2S4_SD | SPI5_MOSI/ I2S5_SD | - | - | - | DFSDM2_ DATIN1 | - | FSMC_D11/ FSMC_DA11 | - | - | EVENT OUT |
| | PE15 | - | TIM1_ BKIN | - | - | - | - | - | - | - | - | DFSDM2_ CKIN1 | - | FSMC_D12/F SMC_DA12 | - | - | EVENT OUT |

**Table 12. STM32F423xH alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/2/ LPTIM1 | TIM3/4/5 | DFSDM2/ TIM8/9/10/11 | I2C1/2/3/ I2CFMP1 | SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4 | SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2 | SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3 | DFSDM1/ USART3/4/ 5/6/7/8/ CAN1 | I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI | SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS | UART4/ UART5/ UART9/ UART10 /CAN3 | FSMC /SDIO | - | RNG | SYS_AF |
| Port F | PF0 | - | - | - | - | I2C2_SDA | - | - | - | - | - | - | - | FSMC_A0 | - | - | EVENTOUT |
| | PF1 | - | - | - | - | I2C2_SCL | - | - | - | - | - | - | - | FSMC_A1 | - | - | EVENTOUT |
| | PF2 | - | - | - | - | I2C2_SMBA | - | - | - | - | - | - | - | FSMC_A2 | - | - | EVENTOUT |
| | PF3 | - | - | TIM5_CH1 | - | - | - | - | - | - | - | - | - | FSMC_A3 | - | - | EVENTOUT |
| | PF4 | - | - | TIM5_CH2 | - | - | - | - | - | - | - | - | - | FSMC_A4 | - | - | EVENTOUT |
| | PF5 | - | - | TIM5_CH3 | - | - | - | - | - | - | - | - | - | FSMC_A5 | - | - | EVENTOUT |
| | PF6 | TRACED0 | - | - | TIM10_CH1 | - | - | - | SAI1_SD_B | UART7_Rx | QUADSPI_BK1_IO3 | - | - | - | - | - | EVENTOUT |
| | PF7 | TRACED1 | - | - | TIM11_CH1 | - | - | - | SAI1_MCLK_B | UART7_Tx | QUADSPI_BK1_IO2 | - | - | - | - | - | EVENTOUT |
| | PF8 | - | - | - | - | - | - | - | SAI1_SCK_B | UART8_RX | TIM13_CH1 | QUADSPI_BK1_IO0 | - | - | - | - | EVENTOUT |
| | PF9 | - | - | - | - | - | - | - | SAI1_FS_B | UART8_TX | TIM14_CH1 | QUADSPI_BK1_IO1 | - | - | - | - | EVENTOUT |
| | PF10 | - | TIM1_ETR | TIM5_CH4 | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PF11 | - | - | - | TIM8_ETR | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PF12 | - | - | - | TIM8_BKIN | - | - | - | - | - | - | - | - | FSMC_A6 | - | - | EVENTOUT |
| | PF13 | - | - | - | - | I2CFMP1_SMBA | - | - | - | - | - | - | - | FSMC_A7 | - | - | EVENTOUT |
| | PF14 | - | - | - | - | I2CFMP1_SCL | - | - | - | - | - | - | - | FSMC_A8 | - | - | EVENTOUT |
| | PF15 | - | - | - | - | I2CFMP1_SDA | - | - | - | - | - | - | - | FSMC_A9 | - | - | EVENTOUT |

**Table 12. STM32F423xH alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/2/ LPTIM1 | TIM3/4/5 | DFSDM2/ TIM8/9/10/11 | I2C1/2/3/ I2CFMP1 | SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4 | SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2 | SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3 | DFSDM1/ USART3/4/ 5/6/7/8/ CAN1 | I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI | SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS | UART4/ UART5/ UART9/ UART10 /CAN3 | FSMC /SDIO | - | RNG | SYS_AF |
| Port G | PG0 | - | - | - | - | - | - | - | - | - | CAN1_RX | - | UART9_RX | FSMC_A10 | - | - | EVENTOUT |
| | PG1 | - | - | - | - | - | - | - | - | - | CAN1_TX | - | UART9_TX | FSMC_A11 | - | - | EVENTOUT |
| | PG2 | - | - | - | - | - | - | - | - | - | - | - | - | FSMC_A12 | - | - | EVENTOUT |
| | PG3 | - | - | - | - | - | - | - | - | - | - | - | - | FSMC_A13 | - | - | EVENTOUT |
| | PG4 | - | - | - | - | - | - | - | - | - | - | - | - | FSMC_A14 | - | - | EVENTOUT |
| | PG5 | - | - | - | - | - | - | - | - | - | - | - | - | FSMC_A15 | - | - | EVENTOUT |
| | PG6 | - | - | - | - | - | - | - | - | - | - | QUADSPI_BK1_NCS | - | - | - | - | EVENTOUT |
| | PG7 | - | - | - | - | - | - | - | - | USART6_CK | - | - | - | - | - | - | EVENTOUT |
| | PG8 | - | - | - | - | - | - | - | - | USART6_RTS | - | - | - | - | - | - | EVENTOUT |
| | PG9 | - | - | - | - | - | - | - | - | USART6_RX | QUADSPI_BK2_IO2 | - | - | FSMC_NE2 | - | - | EVENTOUT |
| | PG10 | - | - | - | - | - | - | - | - | - | - | - | - | FSMC_NE3 | - | - | EVENTOUT |
| | PG11 | - | - | - | - | - | - | - | - | - | CAN2_RX | - | UART10_RX | - | - | - | EVENTOUT |
| | PG12 | - | - | - | - | - | - | - | - | USART6_RTS | CAN2_TX | - | UART10_TX | FSMC_NE4 | - | - | EVENTOUT |
| | PG13 | TRACED2 | - | - | - | - | - | - | - | USART6_CTS | - | - | - | FSMC_A24 | - | - | EVENTOUT |
| | PG14 | TRACED3 | - | - | - | - | - | - | - | USART6_TX | QUADSPI_BK2_IO3 | - | - | FSMC_A25 | - | - | EVENTOUT |
| | PG15 | - | - | - | - | - | - | - | - | USART6_CTS | - | - | - | - | - | - | EVENTOUT |
| PortH | PH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PH1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

# 5 Memory mapping

The memory map is shown in *Figure 18*.

**Figure 18. Memory map**

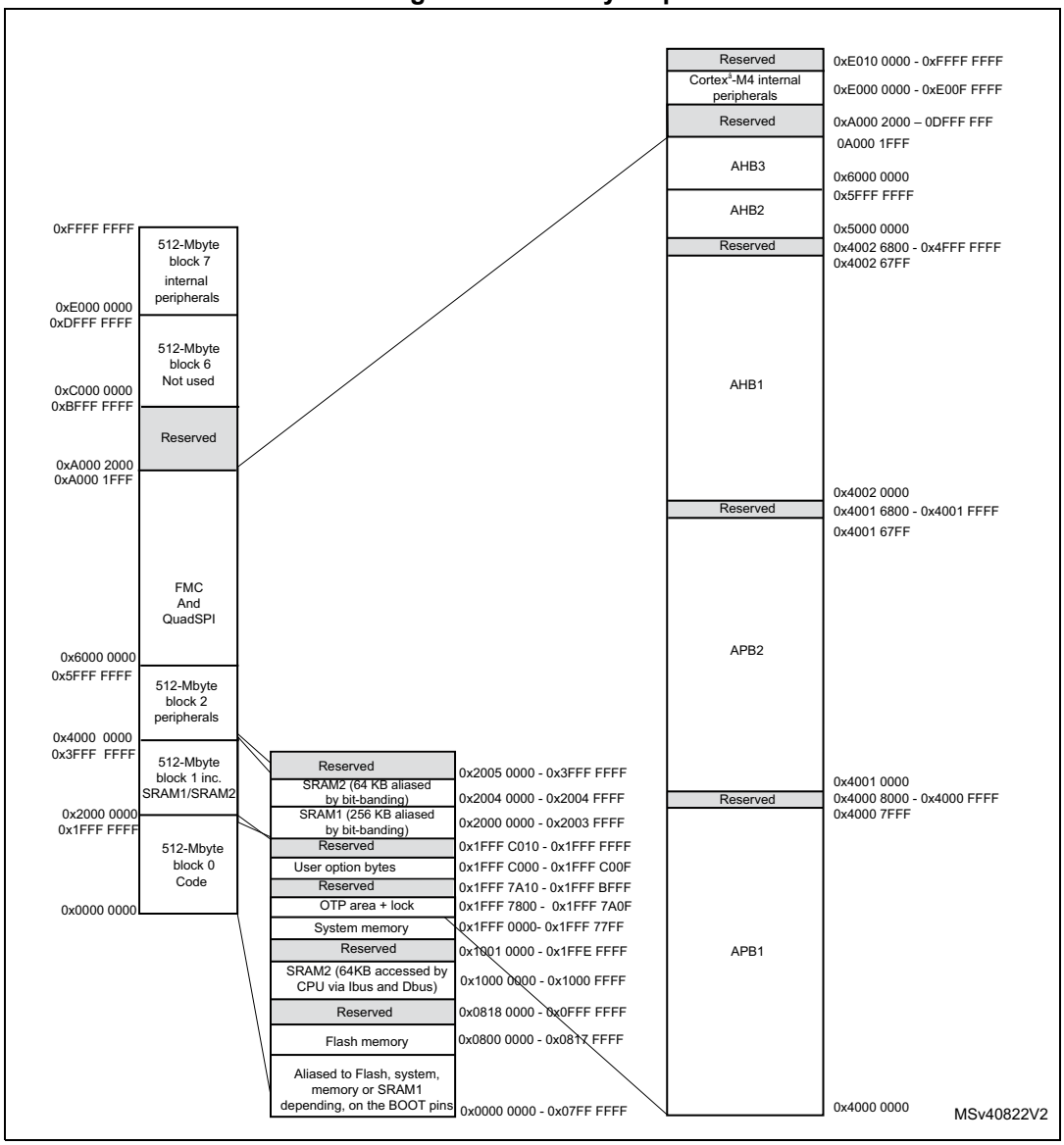


**Table 13. STM32F423xH register boundary addresses**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0xE010 0000 - 0xFFFF FFFF | Reserved |
| Cortex®-M4 | 0xE000 0000 - 0xE00F FFFF | Cortex-M4 internal peripherals |
| AHB3 | 0xA000 2000 - 0xDFFF FFFF | Reserved |
| | 0xA000 1000 - 0xA000 1FFF | QuadSPI control register |
| | 0xA000 0000 - 0xA000 0FFF | FSMC control register |
| | 0x9000 0000 - 0x9FFF FFFF | QUADSPI |
| | 0x7000 0000 - 0x08FFF FFFF | Reserved |
| | 0x6000 0000 - 0x6FFF FFFF | FSMC |
| AHB2 | 0x5006 0C00 - 0x5FFF FFFF | Reserved |
| | 0x5006 0800 0x5006 0BFF | RNG |
| | 0x5006 0400 - 0x5006 07FF | Reserved |
| | 0x5006 0000 - 0x5006 03FF | AES |
| | 0x5004 0000 - 0x5005 FFFF | Reserved |
| | 0x5000 0000 - 0x5003 FFFF | USB OTG FS |
| AHB1 | 0x4002 6800 - 0x4FFF FFFF | Reserved |
| | 0x4002 6400 - 0x4002 67FF | DMA2 |
| | 0x4002 6000 - 0x4002 63FF | DMA1 |
| | 0x4002 4000 - 0X4002 5FFF | Reserved |
| | 0x4002 3C00 - 0x4002 3FFF | Flash interface register |
| | 0x4002 3800 - 0x4002 3BFF | RCC |
| | 0x4002 3400 - 0x4002 37FF | Reserved |
| | 0x4002 3000 - 0x4002 33FF | CRC |
| | 0x4002 2000 - 0x4002 2FFF | Reserved |
| | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | 0x4002 1800 - 0x4002 1BFF | GPIOG |
| | 0x4002 1400 - 0x4002 17FF | GPIOF |
| | 0x4002 1000 - 0x4002 13FF | GPIOE |
| | 0x4002 0C00 - 0x4002 0FFF | GPIOD |
| | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | 0x4002 0400 - 0x4002 07FF | GPIOB |
| | 0x4002 0000 - 0x4002 03FF | GPIOA |

Table 13. STM32F423xH register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| APB2 | 0x4001 6800- 0x4001 FFFF | Reserved |
| | 0x4001 6400 - 0x4001 67FF | DFSDM2 |
| | 0x4001 6000 - 0x4001 63FF | DFSDM1 |
| | 0x4001 5C00 - 0x4001 5FFF | Reserved |
| | 0x4001 5800 - 0x4001 5BFF | SAI1 |
| | 0x4001 5400 - 0x4001 57FF | Reserved |
| | 0x4001 5000 - 0x4001 53FF | SPI5/I2S5 |
| | 0x4001 4C00 - 0x4001 4FFF | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | TIM11 |
| | 0x4001 4400 - 0x4001 47FF | TIM10 |
| | 0x4001 4000 - 0x4001 43FF | TIM9 |
| | 0x4001 3C00 - 0x4001 3FFF | EXTI |
| | 0x4001 3800 - 0x4001 3BFF | SYSCFG |
| | 0x4001 3400 - 0x4001 37FF | SPI4/I2S4 |
| | 0x4001 3000 - 0x4001 33FF | SPI1/I2S1 |
| | 0x4001 2C00 - 0x4001 2FFF | SDIO |
| | 0x4001 2400 - 0x4001 2BFF | Reserved |
| | 0x4001 2000 - 0x4001 23FF | ADC1/2/3 |
| | 0x4001 1C00 - 0x4001 1FFF | UART10 |
| | 0x4001 1800 - 0x4001 1BFF | UART9 |
| | 0x4001 1400 - 0x4001 17FF | USART6 |
| | 0x4001 1000 - 0x4001 13FF | USART1 |
| | 0x4001 0800 - 0x4001 0FFF | Reserved |
| | 0x4001 0400 - 0x4001 07FF | TIM8 |
| | 0x4001 0000 - 0x4001 03FF | TIM1 |

Table 13. STM32F423xH register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| APB1 | 0x4000 8000 - 0x4000 FFFF | Reserved |
| | 0x4000 7C00 - 0x4000 7FFF | UART8 |
| | 0x4000 7800 - 0x4000 7BFF | UART7 |
| | 0x4000 7400 - 0x4000 77FF | DAC1 |
| | 0x4000 7000 - 0x4000 73FF | PWR |
| | 0x4000 6C00- 0x4000 6FFF | CAN3 |
| | 0x4000 6800- 0x4000 6BFF | CAN2 |
| | 0x4000 6400- 0x4000 67FF | CAN1 |
| | 0x4000 6000- 0x4000 63FF | I2CFMP1 |
| | 0x4000 5C00 - 0x4000 5FFF | I2C3 |
| | 0x4000 5800 - 0x4000 5BFF | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | UART5 |
| | 0x4000 4C00 - 0x4000 4FFF | UART4 |
| | 0x4000 4800 - 0x4000 4BFF | USART3 |
| | 0x4000 4400 - 0x4000 47FF | USART2 |
| | 0x4000 4000 - 0x4000 43FF | I2S3ext |
| | 0x4000 3C00 - 0x4000 3FFF | SPI3 / I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | SPI2 / I2S2 |
| | 0x4000 3400 - 0x4000 37FF | I2S2ext |
| | 0x4000 3000 - 0x4000 33FF | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | RTC & BKP Registers |
| | 0x4000 2400 - 0x4000 27FF | LPTIM1 |
| | 0x4000 2000 - 0x4000 23FF | TIM14 |
| | 0x4000 1C00 - 0x4000 1FFF | TIM13 |
| | 0x4000 1800 - 0x4000 1BFF | TIM12 |
| | 0x4000 1400 - 0x4000 17FF | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | TIM2 |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.3 V (for the 1.7 V ≤ $V_{DD}$ ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2 σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 19*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 20*.

**Figure 19. Pin loading conditions**

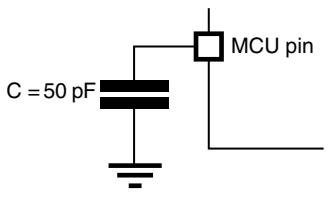
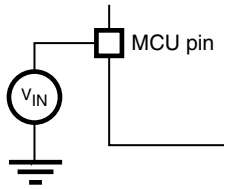
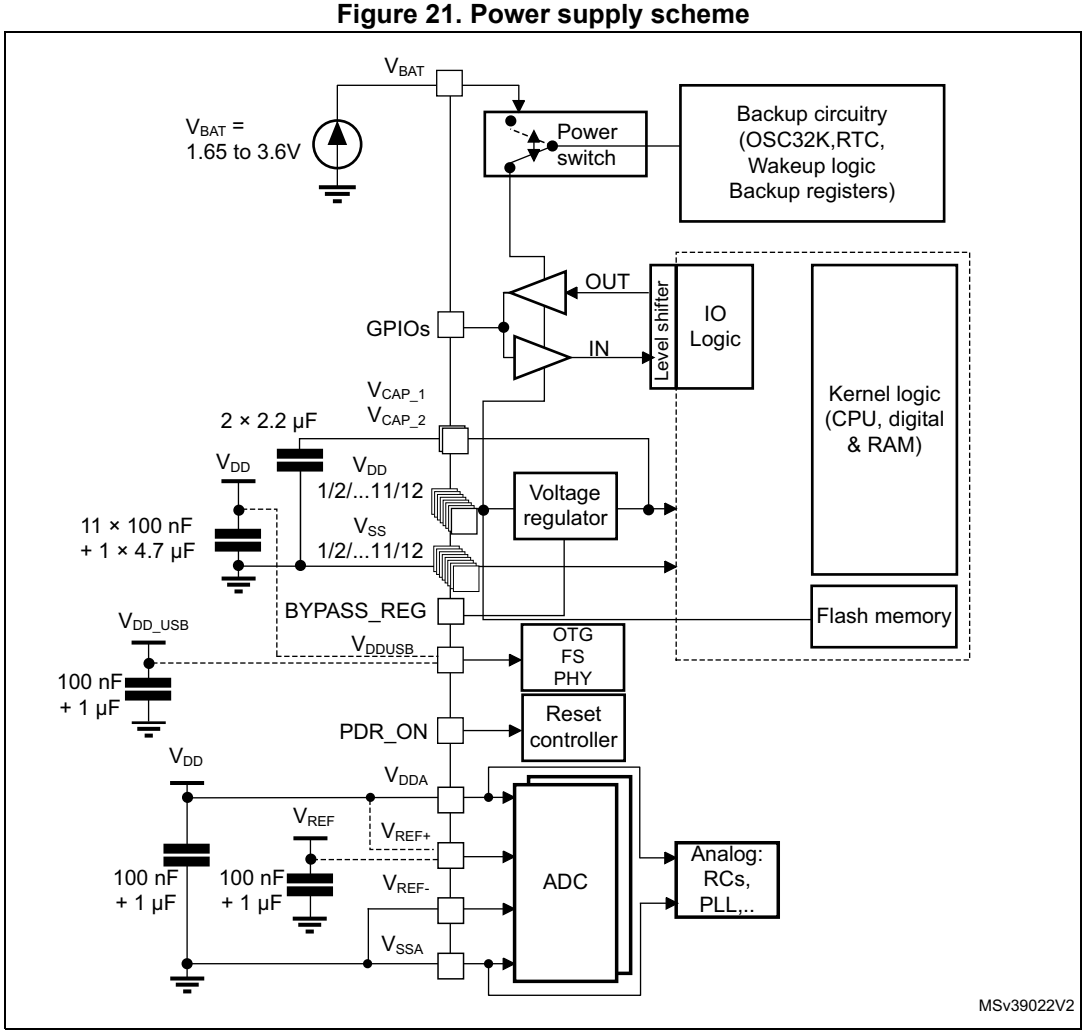



**Figure 20. Input voltage measurement**



### 6.1.6 Power supply scheme

**Figure 21. Power supply scheme**

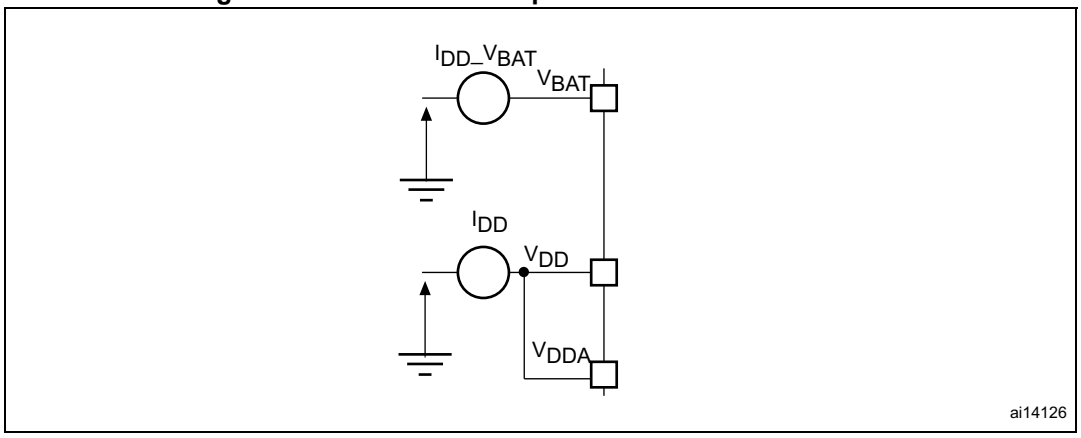



1. To connect PDR_ON pin, refer to Section: Power supply supervisor.
2. The 4.7 µF ceramic capacitor must be connected to one of the $V_{DD}$ pin.
3. VCAP_2 pad is only available on 100-pin and 144-pin packages.
4. $V_{DDA}$=$V_{DD}$ and $V_{SSA}$=$V_{SS}$.
5. $V_{DDUSB}$ is a dedicated independent USB power supply for the on-chip full-speed OTG PHY module and associated DP/DM GPIOs. $V_{DDUSB}$ value does not depend on the $V_{DD}$ and $V_{DDA}$ values, but it must be the last supply to be provided and the first to disappear.

**Caution:** Each power supply pair (for example $V_{DD}$/$V_{SS}$, $V_{DDA}$/$V_{SSA}$) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

### 6.1.7 Current consumption measurement

**Figure 22. Current consumption measurement scheme**




## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics*, and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 14. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{DD}$, $V_{DDUSB}$ and $V_{BAT}$)(1) | –0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on FT and TC pins(2) | $V_{SS}$–0.3 | $V_{DD}$+4.0 | |
| | Input voltage on TTa pins | $V_{SS}$–0.3 | 4.0 | |
| | Input voltage on any other pin | $V_{SS}$–0.3 | 4.0 | |
| | Input voltage for BOOT0 | $V_{SS}$ | 9.0 | |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins including $V_{REF-}$ | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)* | | |

1. All main power ($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum value must always be respected. Refer to *Table 15* for the values of the maximum allowed injected current.

**Table 15. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD_x}$ power lines (source)(1) | 180 | mA |
| $\Sigma I_{VSS}$ | Total current out of sum of all $V_{SS_x}$ ground lines (sink)(1) | -180 | |
| $\Sigma I_{VDDUSB}$ | Total current into $V_{DDUSB}$ power lines (source) | 25 | |
| $I_{VDD}$ | Maximum current into each $V_{DD_x}$ power line (source)(1) | 100 | |
| $I_{VSS}$ | Maximum current out of each $V_{SS_x}$ ground line (sink)(1) | -100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/O and control pin | -25 | |
| $\Sigma I_{IO}$ | Total output current sunk by sum of all I/O and control pins (2) | 120 | |
| | Total output current sunk by sum of all USB I/Os | 25 | |
| | Total output current sourced by sum of all I/Os and control pins(2) | -120 | |
| $I_{INJ(PIN)}$ (3) | Injected current on FT and TC pins (4) | – 5/ + 0 | |
| | Injected current on NRST and B pins (4) | | |
| | Injected current on TTa pins(5) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(6) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by VIN>VDDA in the same time a negative injection is induced by VIN<VSS. IINJ(PIN) must never be exceeded. Refer to *Table 14* for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 16. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | |
| $T_{LEAD}$ | Maximum lead temperature during soldering (WLCSP81, LQFP64/100/144, UFQFPN48, UFBGA100/144) | see note (1) | |

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 17. General operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01 | 0 | - | 64 | MHz |
| | | Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10 | 0 | - | 84 | |
| | | Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11 | 0 | - | 100 | |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | - | 50 | MHz |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | - | 100 | MHz |
| $V_{DD}$ | Standard operating voltage | - | 1.7(1) | - | 3.6 | V |
| $V_{DDA}$(2)(3) | Analog operating voltage (ADC limited to 1.2 M samples) | Must be the same potential as $V_{DD}$(4) | 1.7(1) | - | 2.4 | V |
| | Analog operating voltage (ADC limited to 2.4 M samples) | | 2.4 | - | 3.6 | |
| $V_{DDUSB}$ | USB supply voltage (supply voltage for PA11 and PA12 pins) | USB not used | 1.7 | 3.3 | 3.6 | V |
| | | USB used(5) | 3.0 | - | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | 1.65 | - | 3.6 | V |
| $V_{12}$ | Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins | VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz | 1.08(6) | 1.14 | 1.20(6) | V |
| | | VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz | 1.20(6) | 1.26 | 1.32(6) | |
| | | VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz | 1.26 | 1.32 | 1.38 | |
| $V_{12}$ | Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins | Max frequency 64 MHz | 1.10 | 1.14 | 1.20 | V |
| | | Max frequency 84 MHz | 1.20 | 1.26 | 1.32 | |
| | | Max frequency 100 MHz | 1.26 | 1.32 | 1.38 | |

**Table 17. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage on RST, FT and TC pins(7) | 2 V ≤ $V_{DD}$ ≤ 3.6 V | –0.3 | - | 5.5 | V |
| | | $V_{DD}$ ≤ 2 V | –0.3 | - | 5.2 | |
| | Input voltage on TTa pins | - | - 0.3 | - | $V_{DDA}$ + 0.3 | |
| | Input voltage on BOOT0 pin | - | 0 | - | 9 | |
| $P_D$ | Power dissipation at TA = 85°C for range 6 or TA = 105°C for range 7(8) | UFQFPN48 | - | - | 625 | mW |
| | | WLCSP81 | - | - | 504 | |
| | | LQFP64 | - | - | 426 | |
| | | LQFP100 | - | - | 465 | |
| | | LQFP144 | | - | 571 | |
| | | UFBGA100 | - | - | 351 | |
| | | UFBGA144 | - | - | 417 | |
| | Power dissipation at TA = 125°C for range 3(8) | UFQFPN48 | - | - | 156 | |
| | | WLCSP81 | - | - | 126 | |
| | | LQFP64 | - | - | 106 | |
| | | LQFP100 | - | - | 116 | |
| | | LQFP144 | - | - | 143 | |
| | | UFBGA100 | - | - | 088 | |
| | | UFBGA144 | - | - | 104 | |
| $T_A$ | Ambient temperature for range 6 | Maximum power dissipation | –40 | - | 85 | °C |
| | | Low power dissipation(9) | –40 | - | 105 | |
| | Ambient temperature for range 7 | Maximum power dissipation | –40 | - | 105 | |
| | | Low power dissipation(9) | –40 | - | 125 | |
| | Ambient temperature for range 3 | Maximum power dissipation | –40 | - | 125 | |
| | | Low power dissipation(9) | –40 | - | 130 | |
| $T_J$ | Junction temperature range | Range 6 | –40 | - | 105 | |
| | | Range 7 | –40 | - | 125 | |
| | | Range 3 | –40 | - | 130 | |

1. $V_{DD}/V_{DDA}$ minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. When the ADC is used, refer to *Table 75: ADC characteristics*.
3. If $V_{REF+}$ pin is present, it must respect the following condition: $V_{DDA}$-$V_{REF}$+ < 1.2 V.
4. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and power-down operation.
5. Only the DM ($P_{A11}$) and DP ($P_{A12}$) pads are supplied through $V_{DDUSB}$. For application where the $V_{BUS}$ ($P_{A9}$) is directly connected to the chip, a minimum $V_{DD}$ supply of 2.7V is required.
(some application examples are shown in appendix B)
6. Guaranteed by test in production
7. To sustain a voltage higher than $V_{DD}$+0.3, the internal Pull-up and Pull-Down resistors must be disabled

8. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$.
9. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$.

**Table 18. Features depending on the operating power supply range**

| Operating power supply range | ADC operation | Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$) | Maximum Flash memory access frequency with wait states (1)(2) | I/O operation | Clock output frequency on I/O pins(3) | Possible Flash memory operations |
|---|---|---|---|---|---|---|
| $V_{DD}$ =1.7 to 2.1 V(4) | Conversion time up to 1.2 Msps | 16 MHz(5) | 100 MHz with 6 wait states | – No I/O compensation | up to 30 MHz | 8-bit erase and program operations only |
| $V_{DD}$ = 2.1 to 2.4 V | Conversion time up to 1.2 Msps | 18 MHz | 100 MHz with 5 wait states | – No I/O compensation | up to 30 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.4 to 2.7 V | Conversion time up to 2.4 Msps | 20 MHz | 100 MHz with 4 wait states | – I/O compensation works | up to 50 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.7 to 3.6 V(6) | Conversion time up to 2.4 Msps | 25 MHz | 100 MHz with 3 wait states | – I/O compensation works | – up to 100 MHz when $V_{DD}$ = 3.0 to 3.6 V<br>– up to 50 MHz when $V_{DD}$ = 2.7 to 3.0 V | 32-bit erase and program operations |

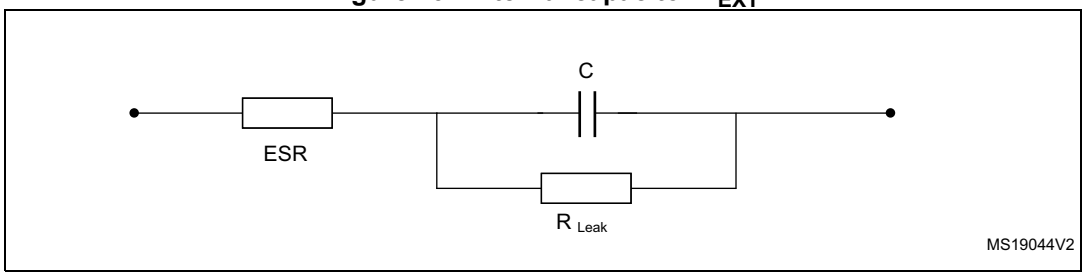
1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. Refer to *Table 61: I/O AC characteristics* for frequencies vs. external load.
4. $V_{DD}/V_{DDA}$ minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
5. Prefetch available over the complete VDD supply range.
6. The voltage range for the USB full speed embedded PHY can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

### 6.3.2 VCAP_1/VCAP_2 external capacitors

Stabilization for the main regulator is achieved by connecting the external capacitor $C_{EXT}$ to the VCAP_1 and VCAP_2 pins. For packages supporting only 1 VCAP pin, the 2 CEXT capacitors are replaced by a single capacitor.

$C_{EXT}$ is specified in *Table 19*.

**Figure 23. External capacitor $C_{EXT}$**




1. Legend: ESR is the equivalent series resistance.

**Table 19. VCAP_1/VCAP_2 operating conditions(1)**

| Symbol | Parameter | Conditions |
|---|---|---|
| CEXT | Capacitance of external capacitor with the pins VCAP_1 and VCAP_2 available | 2.2 µF |
| ESR | ESR of external capacitor with the pins VCAP_1 and VCAP_2 available | < 2 Ω |
| CEXT | Capacitance of external capacitor with a single VCAP pin available | 4.7 µF |
| ESR | ESR of external capacitor with a single VCAP pin available | < 1 Ω |

1. When bypassing the voltage regulator, the two 2.2 µF $V_{CAP}$ capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

### 6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for $T_A$.

**Table 20. Operating conditions at power-up / power-down (regulator ON)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | 20 | ∞ | |

### 6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for $T_A$.

**Table 21. Operating conditions at power-up / power-down (regulator OFF)(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | Power-up | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | Power-down | 20 | ∞ | |
| $t_{VCAP}$ | $V_{CAP_1}$ and $V_{CAP_2}$ rise time rate | Power-up | 20 | ∞ | |
| | $V_{CAP_1}$ and $V_{CAP_2}$ fall time rate | Power-down | 20 | ∞ | |

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when $V_{DD}$ reach below 1.08 V.

*Note: This feature is only available for UFBGA100 and UFBGA144 packages.*

### 6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage @ 3.3V.

**Table 22. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.09 | 2.14 | 2.19 | V |
| | | PLS[2:0]=000 (falling edge) | 1.98 | 2.04 | 2.08 | |
| | | PLS[2:0]=001 (rising edge) | 2.23 | 2.30 | 2.37 | |
| | | PLS[2:0]=001 (falling edge) | 2.13 | 2.19 | 2.25 | |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.45 | 2.51 | |
| | | PLS[2:0]=010 (falling edge) | 2.29 | 2.35 | 2.39 | |
| | | PLS[2:0]=011 (rising edge) | 2.54 | 2.60 | 2.65 | |
| | | PLS[2:0]=011 (falling edge) | 2.44 | 2.51 | 2.56 | |
| | | PLS[2:0]=100 (rising edge) | 2.70 | 2.76 | 2.82 | |
| | | PLS[2:0]=100 (falling edge) | 2.59 | 2.66 | 2.71 | |
| | | PLS[2:0]=101 (rising edge) | 2.86 | 2.93 | 2.99 | |
| | | PLS[2:0]=101 (falling edge) | 2.65 | 2.84 | 3.02 | |
| | | PLS[2:0]=110 (rising edge) | 2.96 | 3.03 | 3.10 | |
| | | PLS[2:0]=110 (falling edge) | 2.85 | 2.93 | 2.99 | |
| | | PLS[2:0]=111 (rising edge) | 3.07 | 3.14 | 3.21 | |
| | | PLS[2:0]=111 (falling edge) | 2.95 | 3.03 | 3.09 | |
| $V_{PVDhyst}$(2) | PVD hysteresis | - | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Falling edge | 1.60(1) | 1.68 | 1.76 | V |
| | | Rising edge | 1.64 | 1.72 | 1.80 | |

**Table 22. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PDRhyst}$(2) | PDR hysteresis | - | - | 40 | - | mV |
| $V_{BOR1}$ | Brownout level 1 threshold | Falling edge | 2.13 | 2.19 | 2.24 | V |
| | | Rising edge | 2.23 | 2.29 | 2.33 | |
| $V_{BOR2}$ | Brownout level 2 threshold | Falling edge | 2.44 | 2.50 | 2.56 | |
| | | Rising edge | 2.53 | 2.59 | 2.63 | |
| $V_{BOR3}$ | Brownout level 3 threshold | Falling edge | 2.75 | 2.83 | 2.88 | |
| | | Rising edge | 2.85 | 2.92 | 2.97 | |
| $V_{BORhyst}$(2) | BOR hysteresis | - | - | 100 | - | mV |
| $T_{RSTTEMPO}$(2)(3) | POR reset timing | - | 0.5 | 1.5 | 3.0 | ms |
| $I_{RUSH}$(2) | In-Rush current on voltage regulator power-on (POR or wakeup from Standby) | - | - | 160 | 200 | mA |
| $E_{RUSH}$(2) | In-Rush energy on voltage regulator power-on (POR or wakeup from Standby) | $V_{DD}$ = 1.7 V, $T_A$ = 125 °C, $I_{RUSH}$ = 171 mA for 31 µs | - | - | 5.4 | µC |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.
3. The reset timing is measured from the power-on (POR reset or wakeup from $V_{BAT}$) to the instant when first instruction is fetched by the user application code.

### 6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 22: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both $f_{HCLK}$ frequency and VDD ranges (refer to *Table 18: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to $f_{HCLK}$ frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for $V_{DD}$ = 3.6 V and a maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

**Table 23. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$= 25 °C | $T_A$= 25 °C | $T_A$=85 °C | $T_A$=105 °C | $T_A$=125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON, all peripherals enabled(2)(3) | 100 | 32.9 | 34.96 | 35.30 | 37.21 | 40.79 | mA |
| | | | 84 | 26.5 | 28.13 | 28.58 | 30.50 | 33.96 | |
| | | | 64 | 18.3 | 19.44 | 20.11 | 21.76 | 25.03 | |
| | | | 50 | 14.4 | 15.28 | 16.12 | 17.95 | 21.11 | |
| | | | 25 | 7.5 | 8.10 | 9.35 | 11.09 | 14.38 | |
| | | | 20 | 6.4 | 6.99 | 8.17 | 9.96 | 13.17 | |
| | | HSI, PLL off, all peripherals enabled(2)(3) | 16 | 4.6 | 5.17 | 6.42 | 8.28 | 11.46 | |
| | | | 1 | 0.7 | 1.28 | 2.64 | 4.30 | 7.66 | |
| | | External clock, PLL ON, all peripherals disabled(3) | 100 | 15.4 | 16.43 | 17.35 | 19.17 | 22.85 | |
| | | | 84 | 12.4 | 13.28 | 14.32 | 16.12 | 19.67 | |
| | | | 64 | 8.7 | 9.36 | 10.38 | 12.06 | 15.31 | |
| | | | 50 | 6.9 | 7.47 | 8.54 | 10.36 | 13.49 | |
| | | | 25 | 3.7 | 4.27 | 5.47 | 7.17 | 10.45 | |
| | | | 20 | 3.2 | 3.72 | 5.01 | 6.67 | 10.02 | |
| | | HSI, PLL off, all peripherals disabled(3) | 16 | 2.3 | 2.80 | 4.05 | 5.90 | 9.07 | |
| | | | 1 | 0.6 | 1.14 | 2.51 | 4.16 | 7.51 | |

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.

3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

**Table 24. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$= 25 °C | $T_A$= 25 °C | $T_A$= 85 °C | $T_A$= 105 °C | $T_A$= 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON, all peripherals enabled(2) | 100 | 33.3 | 35.32(3) | 35.65 | 37.65 | 41.26(3) | mA |
| | | | 84 | 26.8 | 28.45(3) | 28.97 | 30.82 | 34.39(3) | |
| | | | 64 | 18.6 | 19.74(3) | 20.35 | 22.11 | 25.35(3) | |
| | | | 50 | 14.6 | 15.57 | 16.41 | 18.21 | 21.46 | |
| | | | 25 | 7.8 | 8.37 | 9.64 | 11.32 | 14.68 | |
| | | | 20 | 6.7 | 7.25 | 8.40 | 10.25 | 13.45 | |
| | | HSI, PLL OFF(4), all peripherals enabled(2) | 16 | 4.6 | 4.96 | 6.39 | 8.20 | 11.54 | |
| | | | 1 | 0.8 | 0.86 | 2.51 | 4.34 | 7.65 | |
| | | External clock, PLL ON, all peripherals disabled(2) | 100 | 15.7 | 16.74(3) | 17.62 | 19.50 | 23.16(3) | |
| | | | 84 | 12.7 | 13.57(3) | 14.60 | 16.38 | 19.98(3) | |
| | | | 64 | 9.0 | 9.62(3) | 10.60 | 12.37 | 15.58(3) | |
| | | | 50 | 7.1 | 7.69 | 8.79 | 10.63 | 13.79 | |
| | | | 25 | 4.0 | 4.52 | 5.68 | 7.44 | 10.68 | |
| | | | 20 | 3.4 | 4.03 | 5.23 | 6.90 | 10.27 | |
| | | HSI, PLL OFF, all peripherals disabled(2) | 16 | 2.3 | 2.44 | 4.00 | 5.81 | 9.13 | |
| | | | 1 | 0.6 | 0.70 | 2.35 | 4.18 | 7.49 | |

1. Guaranteed by characterization results.
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

**Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON, all peripherals enabled(2)(3) | 100 | 30.2 | 32.03 | 32.71 | 34.69 | 38.46 | mA |
| | | | 84 | 24.3 | 25.77 | 26.58 | 28.47 | 32.16 | |
| | | | 64 | 16.8 | 17.80 | 18.66 | 20.53 | 23.85 | |
| | | | 50 | 13.2 | 14.05 | 15.12 | 16.85 | 20.27 | |
| | | | 25 | 7.1 | 7.62 | 8.92 | 10.81 | 14.11 | |
| | | | 20 | 6.1 | 6.69 | 7.95 | 9.72 | 13.09 | |
| | | HSI, PLL OFF, all peripherals enabled(2) | 16 | 4.4 | 4.99 | 6.28 | 8.18 | 11.45 | |
| | | | 1 | 0.9 | 1.50 | 2.88 | 4.58 | 8.00 | |
| | | External clock, PLL ON(4) all peripherals disabled(2) | 100 | 12.6 | 13.46 | 14.75 | 16.68 | 20.54 | |
| | | | 84 | 10.2 | 10.90 | 12.25 | 14.10 | 17.84 | |
| | | | 64 | 7.2 | 7.70 | 8.95 | 10.81 | 14.14 | |
| | | | 50 | 5.7 | 6.26 | 7.56 | 9.26 | 12.72 | |
| | | | 25 | 3.2 | 3.77 | 5.11 | 6.82 | 10.26 | |
| | | | 20 | 2.9 | 3.41 | 4.79 | 6.49 | 9.92 | |
| | | HSI, PLL OFF, all peripherals disabled(2) | 16 | 2.1 | 2.63 | 3.91 | 5.80 | 9.06 | |
| | | | 1 | 0.8 | 1.34 | 2.72 | 4.42 | 7.86 | |

1. Guaranteed by characterization results..
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Refer to *Table 47* and RM0383 for the possible PLL VCO setting

**Table 26. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON(2), all peripherals enabled(3) | 100 | 30.7 | 32.85(4) | 33.30 | 35.37 | 39.08 | mA |
| | | | 84 | 24.7 | 26.48 | 27.15 | 28.94 | 32.65 | |
| | | | 64 | 17.2 | 18.36 | 19.14 | 20.88 | 24.29 | |
| | | | 50 | 13.6 | 14.54 | 15.45 | 17.27 | 20.58 | |
| | | | 25 | 7.4 | 7.97 | 9.23 | 11.05 | 14.42 | |
| | | | 20 | 6.4 | 6.99 | 8.18 | 10.03 | 13.32 | |
| | | HSI, PLL OFF, all peripherals enabled(3) | 16 | 4.5 | 5.04 | 6.32 | 8.23 | 11.50 | |
| | | | 1 | 1.0 | 1.50 | 2.89 | 4.59 | 8.01 | |
| | | External clock, PLL ON(2) all peripherals disabled(3) | 100 | 13.1 | 14.36 | 15.33 | 17.25 | 20.98 | |
| | | | 84 | 10.7 | 11.67 | 12.73 | 14.56 | 18.21 | |
| | | | 64 | 7.5 | 8.23 | 9.40 | 11.13 | 14.52 | |
| | | | 50 | 6.1 | 6.74 | 7.89 | 9.61 | 12.98 | |
| | | | 25 | 3.5 | 4.19 | 5.37 | 7.08 | 10.48 | |
| | | | 20 | 3.2 | 3.71 | 5.02 | 6.72 | 10.15 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | 2.1 | 2.67 | 3.95 | 5.84 | 9.10 | |
| | | | 1 | 0.8 | 1.35 | 2.72 | 4.43 | 7.87 | |

1. Guaranteed by characterization results.
2. Refer to *Table 47* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
4. Tested in production.

**Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON(2), all peripherals enabled(3) | 100 | 39.9 | 42.46 | 43.17 | 45.32 | 49.19 | mA |
| | | | 84 | 32.6 | 34.71 | 35.45 | 37.58 | 41.24 | |
| | | | 64 | 24.2 | 25.86 | 26.73 | 28.47 | 31.96 | |
| | | | 50 | 19.7 | 21.01 | 22.00 | 23.74 | 27.26 | |
| | | | 25 | 10.8 | 11.55 | 12.83 | 14.66 | 18.03 | |
| | | | 20 | 9.2 | 9.82 | 11.16 | 13.09 | 16.36 | |
| | | HSI, PLL OFF, all peripherals enabled(3) | 16 | 6.8 | 7.33 | 8.77 | 10.69 | 14.00 | |
| | | | 1 | 1.2 | 1.83 | 3.08 | 4.83 | 8.19 | |
| | | External clock, PLL ON(2) all peripherals disabled(3) | 100 | 22.3 | 24.11 | 25.26 | 27.35 | 31.11 | |
| | | | 84 | 18.5 | 20.00 | 21.15 | 23.20 | 26.87 | |
| | | | 64 | 14.6 | 15.81 | 17.02 | 18.74 | 22.20 | |
| | | | 50 | 12.2 | 13.14 | 14.45 | 16.18 | 19.66 | |
| | | | 25 | 7.0 | 7.52 | 8.95 | 10.84 | 14.19 | |
| | | | 20 | 6.0 | 6.58 | 7.95 | 9.74 | 13.07 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | 4.5 | 4.97 | 6.40 | 8.30 | 11.59 | |
| | | | 1 | 1.0 | 1.61 | 2.94 | 4.65 | 8.05 | |

1. Guaranteed by characterization results.
2. Refer to *Table 47* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

**Table 28. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON, all peripherals enabled(2)(3) | 100 | 36.1 | 38.48 | 39.08 | 40.91 | 44.59 | mA |
| | | | 84 | 30.6 | 32.60 | 33.14 | 35.10 | 38.56 | |
| | | | 64 | 23.9 | 25.67 | 26.27 | 27.94 | 31.19 | |
| | | | 50 | 18.9 | 20.32 | 21.04 | 22.85 | 26.10 | |
| | | | 25 | 10.8 | 11.63 | 12.75 | 14.56 | 17.87 | |
| | | | 20 | 9.2 | 9.84 | 11.06 | 12.98 | 16.23 | |
| | | HSI, PLL OFF, all peripherals enabled(2)(3) | 16 | 7.1 | 7.69 | 9.02 | 10.87 | 14.25 | |
| | | | 1 | 1.2 | 1.84 | 3.10 | 4.84 | 8.20 | |
| | | External clock, PLL ON(3) all peripherals disabled | 100 | 18.6 | 20.33 | 21.23 | 23.15 | 26.71 | |
| | | | 84 | 16.5 | 18.09 | 19.01 | 20.81 | 24.29 | |
| | | | 64 | 14.3 | 15.76 | 16.67 | 18.28 | 21.50 | |
| | | | 50 | 11.5 | 12.57 | 13.53 | 15.33 | 18.49 | |
| | | | 25 | 7.0 | 7.67 | 8.90 | 10.76 | 14.05 | |
| | | | 20 | 6.0 | 6.68 | 7.87 | 9.65 | 12.96 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | 4.8 | 5.33 | 6.66 | 8.49 | 11.86 | |
| | | | 1 | 1.0 | 1.62 | 2.95 | 4.66 | 8.06 | |

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

**Table 29. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON, all peripherals enabled(2) | 100 | 42.3 | 45.08 | 45.76 | 47.88 | 51.71 | mA |
| | | | 84 | 34.6 | 36.87 | 37.58 | 39.64 | 43.32 | |
| | | | 64 | 25.5 | 27.18 | 27.93 | 29.90 | 33.23 | |
| | | | 50 | 20.2 | 21.55 | 22.50 | 24.34 | 27.73 | |
| | | | 25 | 10.9 | 11.61 | 12.87 | 14.72 | 18.08 | |
| | | | 20 | 9.3 | 9.86 | 11.20 | 13.13 | 16.41 | |
| | | HSI, PLL OFF, all peripherals enabled | 16 | 6.9 | 7.37 | 8.81 | 10.72 | 14.04 | |
| | | | 1 | 1.2 | 1.83 | 3.09 | 4.83 | 8.19 | |
| | | External clock, PLL ON(2) all peripherals disabled | 100 | 24.7 | 26.76 | 27.84 | 29.93 | 33.66 | |
| | | | 84 | 20.5 | 22.18 | 23.25 | 25.33 | 28.98 | |
| | | | 64 | 15.9 | 17.13 | 18.23 | 20.18 | 23.46 | |
| | | | 50 | 12.7 | 13.68 | 14.95 | 16.71 | 20.13 | |
| | | | 25 | 7.1 | 7.57 | 9.01 | 10.88 | 14.25 | |
| | | | 20 | 6.1 | 6.61 | 7.98 | 9.80 | 13.11 | |
| | | HSI, PLL OFF, all peripherals disabled | 16 | 4.5 | 5.00 | 6.44 | 8.33 | 11.63 | |
| | | | 1 | 1.0 | 1.61 | 2.94 | 4.65 | 8.06 | |

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

**Table 30. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON, all peripherals enabled(2) | 100 | 42.9 | 45.86 | 45.76 | 47.88 | 51.71 | mA |
| | | | 84 | 35.4 | 37.90 | 38.16 | 40.01 | 43.26 | |
| | | | 64 | 26.2 | 28.19 | 28.74 | 30.37 | 33.54 | |
| | | | 50 | 20.7 | 22.32 | 22.50 | 24.34 | 27.73 | |
| | | | 25 | 11.1 | 11.87 | 12.87 | 14.72 | 18.08 | |
| | | | 20 | 9.4 | 10.05 | 11.26 | 13.16 | 16.46 | |
| | | HSI, PLL OFF, all peripherals enabled | 16 | 7.1 | 7.72 | 9.06 | 10.90 | 14.29 | |
| | | | 1 | 1.2 | 1.84 | 3.10 | 4.84 | 8.20 | |
| | | External clock, PLL ON(2) all peripherals disabled | 100 | 25.4 | 27.83 | 27.84 | 29.93 | 33.66 | |
| | | | 84 | 21.4 | 23.44 | 24.10 | 25.77 | 29.04 | |
| | | | 64 | 16.6 | 18.31 | 19.17 | 20.72 | 23.86 | |
| | | | 50 | 13.2 | 15.10 | 14.95 | 16.71 | 20.13 | |
| | | | 25 | 7.2 | 7.90 | 9.01 | 10.88 | 14.25 | |
| | | | 20 | 6.2 | 6.83 | 8.05 | 9.88 | 13.15 | |
| | | HSI, PLL OFF, all peripherals disabled | 16 | 4.8 | 5.37 | 6.70 | 8.52 | 11.89 | |
| | | | 1 | 1.0 | 1.62 | 2.96 | 4.67 | 8.07 | |

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

**Table 31. Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Sleep mode** | All peripherals enabled(2)(3), External clock, PLL ON, Flash deep power down | 100 | 21.6 | 22.97(4) | 23.91 | 25.99 | 29.72 | mA |
| | | | 84 | 17.4 | 18.50 | 19.59 | 21.42 | 25.09 | |
| | | | 64 | 12.0 | 12.81 | 13.87 | 15.73 | 19.00 | |
| | | | 50 | 9.5 | 10.15 | 11.33 | 13.22 | 16.44 | |
| | | | 25 | 5.2 | 5.79 | 7.11 | 8.82 | 12.18 | |
| | | | 20 | 4.6 | 5.17 | 6.41 | 8.28 | 11.48 | |
| | | All peripherals enabled(2)(3), HSI, PLL OFF, Flash deep power down | 16 | 3.0 | 3.24 | 4.78 | 6.60 | 9.94 | |
| | | | 1 | 0.7 | 0.76 | 2.41 | 4.23 | 7.55 | |
| | | All peripherals enabled(2)(3), External clock, PLL ON Flash ON | 100 | 22.0 | 23.42 | 24.45 | 26.41 | 30.24 | |
| | | | 84 | 17.7 | 18.91 | 19.98 | 21.85 | 25.56 | |
| | | | 64 | 12.4 | 13.17 | 14.30 | 16.07 | 19.48 | |
| | | | 50 | 9.8 | 10.48 | 11.72 | 13.53 | 16.90 | |
| | | | 25 | 5.5 | 6.05 | 7.41 | 9.11 | 12.55 | |
| | | | 20 | 4.9 | 5.42 | 6.72 | 8.57 | 11.89 | |
| | | All peripherals enabled(2)(3), HSI, PLL ON, Flash ON | 16 | 3.3 | 3.51 | 5.06 | 6.91 | 10.30 | |
| | | | 1 | 0.9 | 1.01 | 2.67 | 4.52 | 7.88 | |
| | | All peripherals disabled, External clock, PLL ON(2), Flash deep power down | 100 | 3.5 | 4.17 | 5.56 | 7.54 | 11.23 | |
| | | | 84 | 2.9 | 3.48 | 4.94 | 6.76 | 10.40 | |
| | | | 64 | 2.2 | 2.73 | 3.94 | 5.80 | 8.98 | |
| | | | 50 | 1.8 | 2.38 | 3.57 | 5.42 | 8.60 | |
| | | | 25 | 1.3 | 1.86 | 3.11 | 4.82 | 8.12 | |
| | | | 20 | 1.3 | 1.90 | 3.13 | 4.85 | 8.15 | |
| | | All peripherals disabled, HSI, PLL OFF(2), Flash deep power down | 16 | 0.6 | 0.68 | 2.33 | 4.16 | 7.47 | |
| | | | 1 | 0.5 | 0.59 | 2.24 | 4.07 | 7.38 | |
| | | All peripherals disabled, External clock, PLL ON(2), Flash ON | 100 | 4.0 | 4.54 | 5.97 | 8.09 | 11.74 | |
| | | | 84 | 3.3 | 3.87 | 5.32 | 7.19 | 10.84 | |
| | | | 64 | 2.5 | 3.04 | 4.33 | 6.15 | 9.47 | |
| | | | 50 | 2.2 | 2.69 | 3.93 | 5.82 | 9.04 | |
| | | | 25 | 1.6 | 2.13 | 3.37 | 5.20 | 8.46 | |
| | | | 20 | 1.6 | 2.16 | 3.39 | 5.22 | 8.48 | |
| | | All peripherals disabled, HSI, PLL OFF(2), Flash ON | 16 | 0.9 | 0.96 | 2.62 | 4.47 | 7.82 | |
| | | | 1 | 0.7 | 0.85 | 2.50 | 4.36 | 7.71 | |

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Tested in production.

**Table 32. Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Sleep mode** | External clock, PLL ON, Flash deep power down, all peripherals enabled(2) | 100 | 21.2 | 22.64 | 23.56 | 25.66 | 29.30 | mA |
| | | | 84 | 17.1 | 18.20 | 19.27 | 21.14 | 24.75 | |
| | | | 64 | 11.8 | 12.53 | 13.59 | 15.47 | 18.66 | |
| | | | 50 | 9.3 | 9.88 | 11.06 | 12.94 | 16.11 | |
| | | | 25 | 5.0 | 5.52 | 6.83 | 8.61 | 11.88 | |
| | | | 20 | 4.4 | 4.93 | 6.16 | 8.03 | 11.19 | |
| | | HSI, PLL OFF(2), Flash deep power down, all peripherals enabled | 16 | 3.0 | 3.53 | 4.91 | 6.57 | 9.94 | |
| | | | 1 | 0.6 | 1.19 | 2.55 | 4.21 | 7.57 | |
| | | External clock, PLL ON(2) all peripherals enabled, Flash ON | 100 | 21.7 | 23.10 | 24.09 | 26.12 | 29.90 | |
| | | | 84 | 17.4 | 18.61 | 19.72 | 21.55 | 25.27 | |
| | | | 64 | 12.1 | 12.89 | 13.98 | 15.84 | 19.18 | |
| | | | 50 | 9.6 | 10.20 | 11.43 | 13.32 | 16.62 | |
| | | | 25 | 5.2 | 5.80 | 7.19 | 8.91 | 12.33 | |
| | | | 20 | 4.6 | 5.18 | 6.47 | 8.37 | 11.63 | |
| | | HSI, PLL OFF(2), all peripherals enabled, Flash ON | 16 | 3.2 | 3.79 | 5.17 | 6.88 | 10.32 | |
| | | | 1 | 0.9 | 1.43 | 2.80 | 4.50 | 7.92 | |
| | | All peripherals disabled, External clock, PLL ON(2), Flash deep power down | 100 | 3.3 | 3.82 | 5.34 | 7.25 | 10.97 | |
| | | | 84 | 2.7 | 3.22 | 4.70 | 6.54 | 10.13 | |
| | | | 64 | 1.9 | 2.48 | 3.70 | 5.55 | 8.71 | |
| | | | 50 | 1.6 | 2.13 | 3.35 | 5.15 | 8.35 | |
| | | | 25 | 1.0 | 1.61 | 2.90 | 4.57 | 7.91 | |
| | | | 20 | 1.1 | 1.66 | 2.93 | 4.59 | 7.93 | |
| | | All peripherals disabled, HSI, PLL OFF(2), Flash deep power down | 16 | 0.6 | 1.12 | 2.49 | 4.14 | 7.49 | |
| | | | 1 | 0.5 | 1.04 | 2.40 | 4.06 | 7.40 | |
| | | All peripherals disabled, External clock, PLL ON(2), Flash ON | 100 | 3.7 | 4.28 | 5.76 | 7.83 | 11.49 | |
| | | | 84 | 3.1 | 3.60 | 5.11 | 6.96 | 10.64 | |
| | | | 64 | 2.3 | 2.80 | 4.09 | 5.96 | 9.23 | |
| | | | 50 | 1.9 | 2.44 | 3.70 | 5.59 | 8.82 | |
| | | | 25 | 1.3 | 1.89 | 3.18 | 4.94 | 8.27 | |
| | | | 20 | 1.4 | 1.92 | 3.20 | 4.97 | 8.29 | |
| | | All peripherals disabled, HSI, PLL OFF(2), Flash ON | 16 | 0.8 | 1.38 | 2.75 | 4.44 | 7.87 | |
| | | | 1 | 0.7 | 1.25 | 2.65 | 4.34 | 7.77 | |

1. Guaranteed by characterization results.

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

**Table 33. Typical and maximum current consumptions in Stop mode - $V_{DD}$ = 1.7 V**

| Symbol | Conditions | Parameter | Typ(1) | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD_STOP}$ | Flash in Stop mode, all oscillators OFF, no independent watchdog | Main regulator usage | 111.7 | 157.9 | 713.7 | 1323.5 | 2315.1 | µA |
| | | Low power regulator usage | 42.3 | 80.1 | 594.1 | 1167.6 | 2097.6 | |
| | Flash in Deep power down mode, all oscillators OFF, no independent watchdog | Main regulator usage | 77.9 | 113.1 | 568.3 | 1073.6 | 1883.7 | |
| | | Low power regulator usage | 19.7 | 55.8 | 561.3 | 1123.2 | 2026.0 | |
| | | Low power low voltage regulator usage | 15.3 | 46.3 | 490.8 | 991.3 | 1793.9 | |

1. Guaranteed by characterization results.

**Table 34. Typical and maximum current consumption in Stop mode - $V_{DD}$=3.6 V**

| Symbol | Conditions | Parameter | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD_STOP}$ | Flash in Stop mode, all oscillators OFF, no independent watchdog | Main regulator usage | 114.4 | 161.6(2) | 723.0 | 1339.0 | 2342.7(2) | µA |
| | | Low power regulator usage | 44.1 | 82.5(2) | 600.6 | 1179.3 | 2119.1 | |
| | Flash in Deep power down mode, all oscillators OFF, no independent watchdog | Main regulator usage | 80.6 | 116.7 | 572.3 | 1079.2 | 1896.3 | |
| | | Low power regulator usage | 21.4 | 58.9 | 567.9 | 1134.5 | 2049.6 | |
| | | Low power low voltage regulator usage | 17.0 | 49.0(2) | 497.4 | 1003.6 | 1817.0(2) | |

1. Guaranteed by characterization results.
2. Tested in production.

**Table 35. Typical and maximum current consumption in Standby mode - $V_{DD}$= 1.7 V**

| Symbol | Parameter | Conditions | Typ(1) | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD_STBY}$ | Supply current in Standby mode | Low-speed oscillator (LSE in low drive mode) and RTC ON | 2.3 | 3.7 | 15.9 | 32.5 | 76.8 | µA |
| | | Low-speed oscillator (LSE in high drive mode) and RTC ON | 2.9 | 4.3 | 16.5 | 33.1 | 77.4 | |
| | | RTC and LSE OFF | 1.1 | 2.5 | 14.7 | 31.3 | 75.6 | |

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization results.

**Table 36. Typical and maximum current consumption in Standby mode - $V_{DD}$= 3.6 V**

| Symbol | Parameter | Conditions | Typ(1) | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD_STBY}$ | Supply current in Standby mode | Low-speed oscillator (LSE in low drive mode) and RTC ON | 3.7 | 5.2 | 20.6 | 40.5 | 82.7 | µA |
| | | Low-speed oscillator (LSE in high drive mode) and RTC ON | 4.5 | 6.0 | 21.4 | 41.3 | 83.5 | |
| | | RTC and LSE OFF | 2.5 | 4.0 | 19.4 | 39.3 | 81.5(3) | |

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization, not tested in production unless otherwise specified.
3. Tested in production.

**Table 37. Typical and maximum current consumptions in $V_{BAT}$ mode**

| Symbol | Parameter | Conditions(1) | Typ | | | | Max(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| | | | $V_{BAT}$ = 1.7 V | $V_{BAT}$= 2.4 V | $V_{BAT}$ = 3.3 V | $V_{BAT}$ = 3.6 V | $V_{BAT}$ = 3.6 V | | | |
| $I_{DD_VBAT}$ | Backup domain supply current | Low-speed oscillator (LSE in low-drive mode) and RTC ON | 0.74 | 0.84 | 1.04 | 1.24 | 3.00 | 5.00 | 10.00 | µA |
| | | Low-speed oscillator (LSE in high-drive mode) and RTC ON | 1.51 | 1.64 | 1.89 | 2.00 | 3.80 | 5.80 | 11.60 | |
| | | RTC and LSE OFF | 0.03 | 0.03 | 0.04 | 0.04 | 2.00 | 4.00 | 8.00 | |

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a $C_L$ of 6 pF for typical values.
2. Guaranteed by characterization results.

**Figure 24. Typical $V_{BAT}$ current consumption (LSE and RTC ON/LSE oscillator "low power" mode selection)**

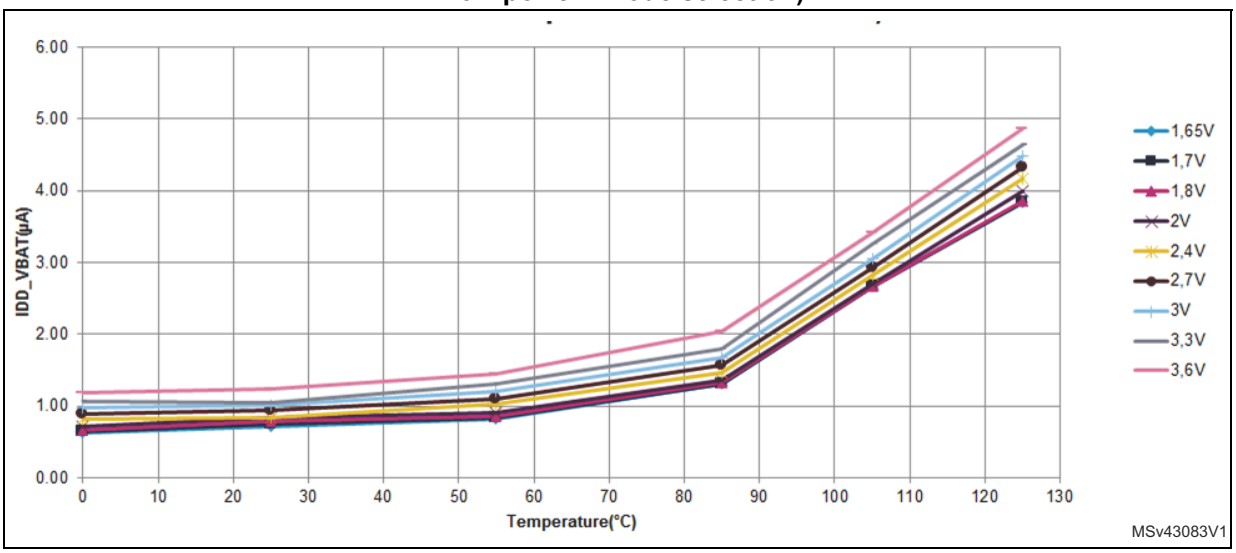
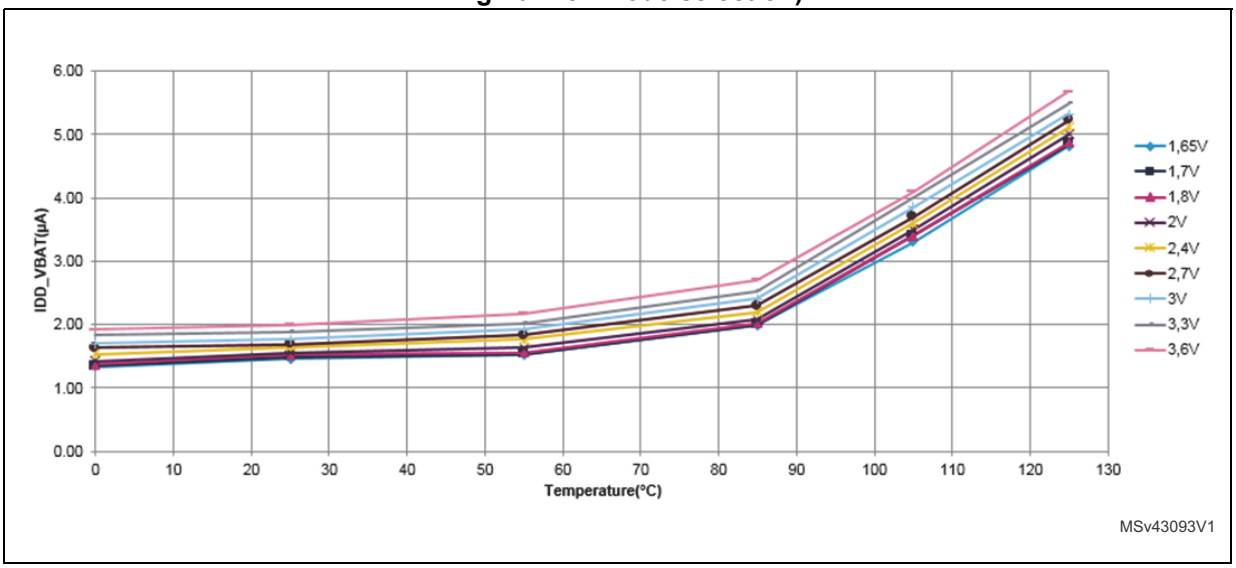



**Figure 25. Typical $V_{BAT}$ current consumption (LSE and RTC ON/LSE oscillator "high drive" mode selection)**



### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

**I/O static current consumption**

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 59: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

**I/O dynamic current consumption**

In addition to the internal peripheral current consumption (see *Table 39: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 38. Switching output I/O current consumption**

| Symbol | Parameter | Conditions[1] | I/O toggling frequency ($f_{SW}$) | Typ | Unit |
|---|---|---|---|---|---|
| IDDIO | I/O switching current | $V_{DD}$ = 3.3 V<br>C = $C_{INT}$ | 2 MHz | 0.05 | mA |
| | | | 8 MHz | 0.15 | |
| | | | 25 MHz | 0.45 | |
| | | | 50 MHz | 0.85 | |
| | | | 60 MHz | 1.00 | |
| | | | 84 MHz | 1.40 | |
| | | | 90 MHz | 1.67 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 0 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.10 | |
| | | | 8 MHz | 0.35 | |
| | | | 25 MHz | 1.05 | |
| | | | 50 MHz | 2.20 | |
| | | | 60 MHz | 2.40 | |
| | | | 84 MHz | 3.55 | |
| | | | 90 MHz | 4.23 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ =10 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.20 | |
| | | | 8 MHz | 0.65 | |
| | | | 25 MHz | 1.85 | |
| | | | 50 MHz | 2.45 | |
| | | | 60 MHz | 4.70 | |
| | | | 84 MHz | 8.80 | |
| | | | 90 MHz | 10.47 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 22 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.25 | |
| | | | 8 MHz | 1.00 | |
| | | | 25 MHz | 3.45 | |
| | | | 50 MHz | 7.15 | |
| | | | 60 MHz | 11.55 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 33 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.32 | |
| | | | 8 MHz | 1.27 | |
| | | | 25 MHz | 3.88 | |
| | | | 50 MHz | 12.34 | |

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with $f_{HCLK}$ = 100 MHz,
  - scale 2 with $f_{HCLK}$ = 84 MHz,
  - scale 3 with $f_{HCLK}$ = 64 MHz.
- Ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

**Table 39. Peripheral current consumption**

| Peripheral | | $I_{DD}$ (Typ) | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| AHB1 | GPIOA | 1.89 | 1.82 | 1.64 | µA/MHz |
| | GPIOB | 1.75 | 1.68 | 1.52 | |
| | GPIOC | 1.70 | 1.64 | 1.48 | |
| | GPIOD | 1.72 | 1.65 | 1.48 | |
| | GPIOE | 1.78 | 1.71 | 1.55 | |
| | GPIOF | 1.68 | 1.62 | 1.45 | |
| | GPIOG | 1.66 | 1.61 | 1.44 | |
| | GPIOH | 0.72 | 0.69 | 0.63 | |
| | CRC | 0.30 | 0.30 | 0.28 | |
| | DMA1(1) | 1.75N + 3.14 | 1.66N + 3.00 | 1.49N + 2.70 | |
| | DMA2(1) | 1.79N + 3.29 | 1.71N + 3.14 | 1.53N + 2.82 | |
| AHB2 | RNG | 0.72 | 0.70 | 0.63 | µA/MHz |
| | USB_OTG_FS | 19.26 | 18.37 | 16.47 | |
| | AES | 2.75 | 2.63 | 2.36 | |
| AHB3 | FSMC | 5.42 | 5.18 | 4.64 | µA/MHz |
| | QSPI | 10.33 | 9.86 | 8.84 | |

**Table 39. Peripheral current consumption (continued)**

| Peripheral | | $I_{DD}$ (Typ) | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| APB1 | AHB-APB1 bridge | 0.90 | 0.88 | 0.81 | µA/MHz |
| | TIM2 | 13.08 | 12.48 | 11.16 | |
| | TIM3 | 9.98 | 9.50 | 8.50 | |
| | TIM4 | 9.88 | 9.43 | 8.44 | |
| | TIM5 | 13.14 | 12.52 | 11.19 | |
| | TIM6 | 1.94 | 1.86 | 1.66 | |
| | TIM7 | 1.86 | 1.79 | 1.56 | |
| | TIM12 | 5.56 | 5.29 | 4.72 | |
| | TIM13 | 3.44 | 3.29 | 2.94 | |
| | TIM14 | 3.66 | 3.48 | 3.09 | |
| | LPTIM1 | 7.34 | 7.00 | 6.25 | |
| | WWDG | 0.64 | 0.62 | 0.53 | |
| | SPI2/I2S2 | 3.02 | 2.88 | 2.56 | |
| | SPI3/I2S3 | 3.06 | 2.90 | 2.59 | |
| | USART2 | 3.30 | 3.14 | 2.81 | |
| | USART3 | 3.32 | 3.14 | 2.81 | |
| | UART4 | 3.18 | 3.02 | 2.69 | |
| | UART5 | 3.26 | 3.10 | 2.75 | |
| | I2C1 | 3.20 | 3.05 | 2.72 | |
| | I2C2 | 3.30 | 3.14 | 2.81 | |
| | I2C3 | 3.26 | 3.10 | 2.78 | |
| | I2CFMP1 | 5.22 | 4.98 | 4.44 | |
| | CAN1 | 5.58 | 5.31 | 4.75 | |
| | CAN2 | 5.14 | 4.88 | 4.38 | |
| | CAN3 | 5.70 | 5.43 | 4.84 | |
| | PWR | 0.90 | 0.86 | 0.75 | |
| | DAC1 | 2.14 | 2.05 | 1.81 | |
| | UART7 | 3.08 | 2.93 | 2.59 | |
| | UART8 | 3.10 | 2.95 | 2.63 | |

**Table 39. Peripheral current consumption (continued)**

| Peripheral | | $I_{DD}$ (Typ) | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| APB2 | AHB-APB2 bridge | 0.10 | 0.11 | 0.09 | µA/MHz |
| | TIM1 | 6.78 | 6.46 | 5.80 | |
| | TIM8 | 6.94 | 6.62 | 5.94 | |
| | USART1 | 3.14 | 3.00 | 2.69 | |
| | USART6 | 3.12 | 2.98 | 2.67 | |
| | UART9 | 2.89 | 1.98 | 1.75 | |
| | UART10 | 2.91 | 2.00 | 1.77 | |
| | ADC1 | 3.45 | 3.29 | 2.95 | |
| | SDIO | 3.54 | 3.37 | 3.03 | |
| | SPI1 | 1.52 | 1.46 | 1.31 | |
| | SPI4 | 1.50 | 1.43 | 1.28 | |
| | SYSCFG | 0.58 | 0.55 | 0.50 | |
| | EXT1 | 0.91 | 0.86 | 0.78 | |
| | TIM9 | 2.95 | 2.81 | 2.53 | |
| | TIM10 | 1.88 | 1.79 | 1.61 | |
| | TIM11 | 1.86 | 1.77 | 1.59 | |
| | SPI5 | 1.50 | 1.43 | 1.30 | |
| | SAI | 2.89 | 2.75 | 2.47 | |
| | DFSDM1 | 4.43 | 4.21 | 3.80 | |
| | DFSDM2 | 7.08 | 6.76 | 6.05 | |
| Bus Matrix | | 4.06 | 3.87 | 3.45 | |

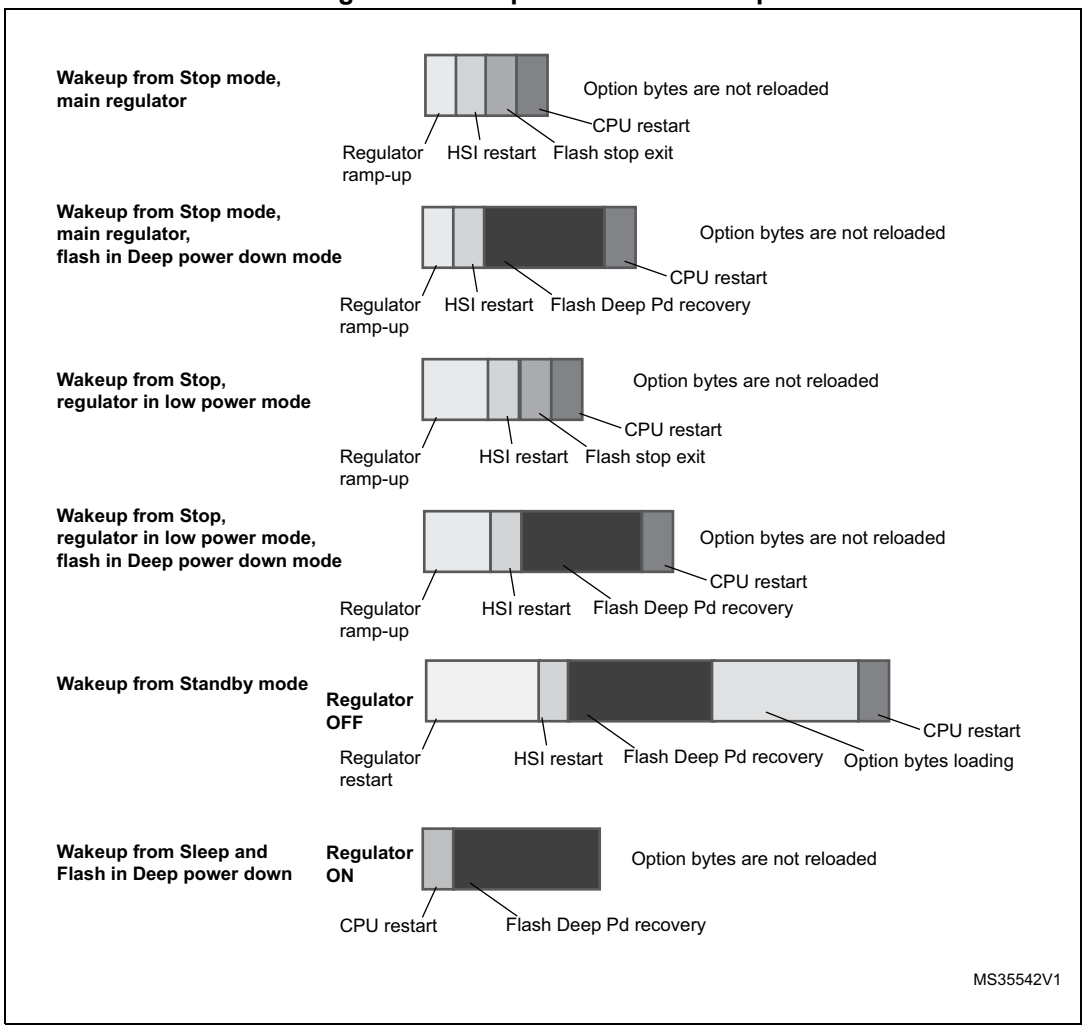
1. N is the number of stream enable (1...8).

### 6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 40* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0/PC0/PC1) pins are used to wakeup from Standby, Stop and Sleep modes.

**Figure 26. Low-power mode wakeup**




All timings are derived from tests performed under ambient temperature and $V_{DD}$=3.3 V.

**Table 40. Low-power mode wakeup timings(1)**

| Symbol | Parameter | Conditions | Min(1) | Typ(1) | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{WUSLEEP}$ | Wakeup from Sleep mode | - | - | 4 | 6 | clk cycles |
| $t_{WUSLEEPFDSM}$ | | Flash memory in Deep power down mode | - | - | 50.0 | µs |
| $t_{WUSTOP}$ | Wakeup from STOP mode Code execution on Flash | Main regulator | - | 12.7 | 15.0 | |
| | | Main regulator, Flash memory in Deep power down mode | - | 104.1 | 120.0 | |
| | | Wakeup from Stop mode, regulator in low power mode(2) | - | 20.9 | 28.0 | |
| | | Regulator in low power mode, Flash memory in Deep power down mode(2) | - | 112.5 | 130.0 | |
| | | Regulator in low power mode low voltage, Flash memory in Deep power down mode | - | 112.5 | 130.0 | |
| $t_{WUSTOP}$ | Wakeup from STOP mode code execution on RAM(3) | Main regulator with Flash in Stop mode or Deep power down(2) | - | 4.2 | 7.0 | |
| | | Wakeup from Stop mode, regulator in low power mode and Flash in Stop mode or Deep power down | - | 12.6 | 20.0 | |
| $t_{WUSTDBY}$ | Wakeup from Standby mode | - | - | 328.2 | 400.0 | |
| $t_{WUFLASH}$ | Wakeup of Flash | From Flash_Stop mode | - | - | 11.0 | |
| | | From Flash Deep power down mode | - | - | 40.0 | |

1. Guaranteed by characterization results.
2. The specification is valid for wakeup from regulator in low power mode or low power low voltage mode, since the timing difference is negligible.
3. For the faster wakeup time for code execution on RAM, the Flash must be in STOP or DeepPower Down mode (see reference manual RM0430).

## 6.3.8 External clock source characteristics

### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 59*. However, the recommended clock input waveform is shown in *Figure 27*.

The characteristics given in *Table 41* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions

summarized in *Table 17*.

**Table 41. High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE_ext}$ | External user clock source frequency(1) | | 1 | - | 50 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time(1) | | 5 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | - | - | 10 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | | - | 5 | - | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | 45 | - | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 59*. However, the recommended clock input waveform is shown in *Figure 28*.

The characteristics given in *Table 42* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

**Table 42. Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE_ext}$ | User External clock source frequency(1) | | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{f(LSE)}$ | OSC32_IN high or low time(1) | | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

Figure 27. High-speed external clock source AC timing diagram

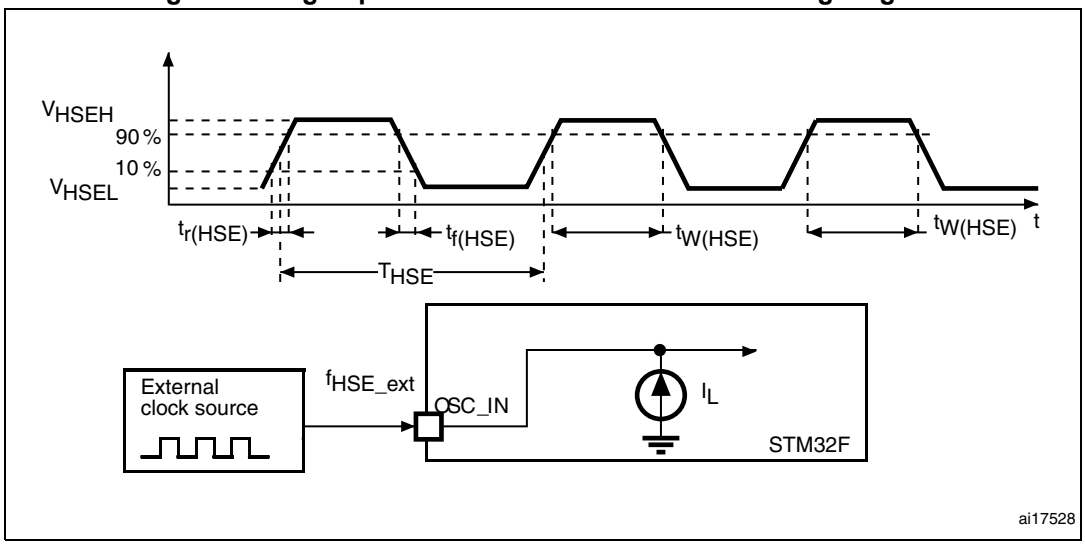
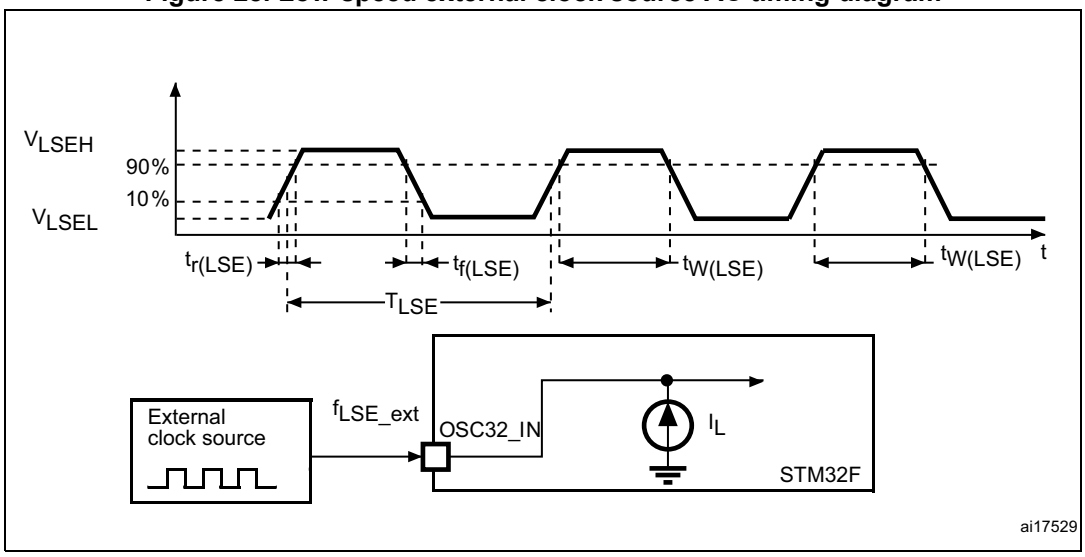



Figure 28. Low-speed external clock source AC timing diagram




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 43. HSE 4-26 MHz oscillator characteristics(1)**

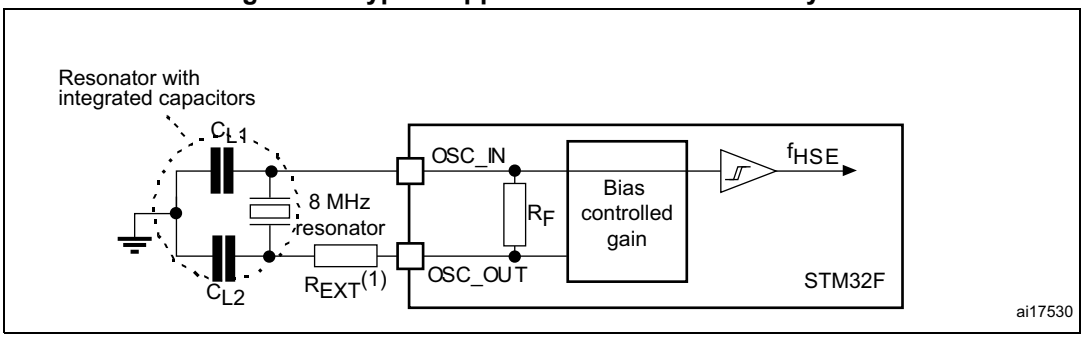
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC_IN}$ | Oscillator frequency | | 4 | - | 26 | MHz |
| $R_F$ | Feedback resistor | | - | 200 | - | kΩ |
| $I_{DD}$ | HSE current consumption | $V_{DD}$=3.3 V, ESR= 30 Ω, $C_L$=5 pF @25 MHz | - | 450 | - | µA |
| | | $V_{DD}$=3.3 V, ESR= 30 Ω, $C_L$=10 pF @25 MHz | - | 530 | - | |
| $ACC_{HSE}$(2) | HSE accuracy | - | -500 | - | 500 | ppm |
| $G_{m_crit_max}$ | Maximum critical crystal $g_m$ | Startup | - | - | 1 | mA/V |
| $t_{SU(HSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 29*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 29. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as

possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

**Table 44. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1)**

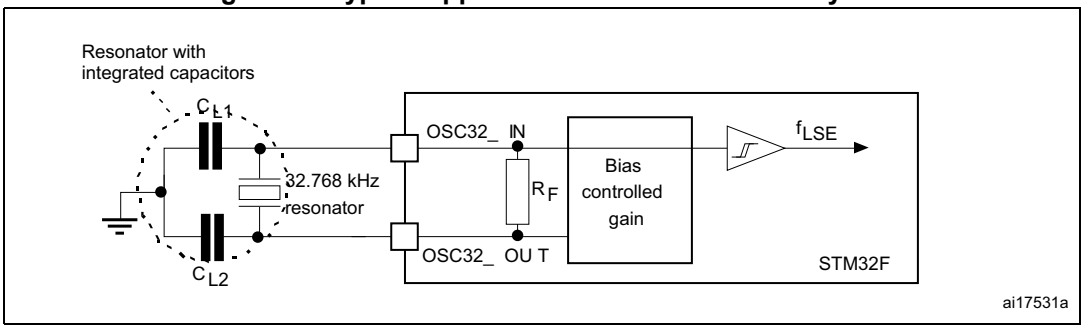
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | 18.4 | - | MΩ |
| $I_{DD}$ | LSE current consumption | Low-power mode (default) | - | - | 1 | µA |
| | | High-drive mode | - | - | 3 | |
| $ACC_{LSE}$ (2) | LSE accuracy | - | -500 | - | 500 | ppm |
| $G_m$_crit_max | Maximum critical crystal $g_m$ | Startup, low-power mode | - | - | 0.56 | µA/V |
| | | Startup, high-drive mode | - | - | 1.50 | |
| $t_{SU(LSE)}$ (3) | startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. Refer to the application note AN2867.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is guaranteed by characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

*For information about the LSE high-power mode, refer to the reference manual RM0383.*

**Figure 30. Typical application with a 32.768 kHz crystal**



### 6.3.9 Internal clock source characteristics

The parameters given in *Table 45* and *Table 46* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

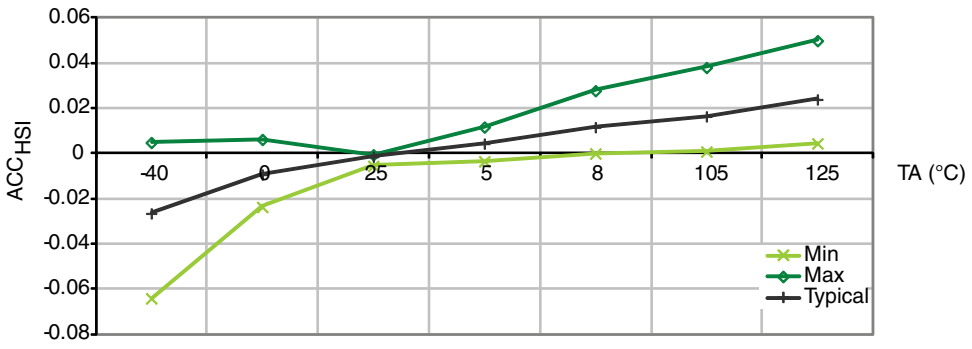
#### High-speed internal (HSI) RC oscillator

**Table 45. HSI oscillator characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 16 | - | MHz |
| $ACC_{HSI}$ | HSI user trimming step(2) | - | - | - | 1 | % |
| | Accuracy of the HSI oscillator | $T_A$ = – 40 to 125 °C(3) | –8 | - | 6.75 | % |
| | | $T_A$ = – 40 to 105 °C(3) | –8 | - | 4.5 | % |
| | | $T_A$ = –10 to 85 °C(3) | –4 | - | 4 | % |
| | | $T_A$ = 25 °C(4) | –1 | - | 1 | % |
| $t_{su(HSI)}$(2) | HSI oscillator startup time | - | - | 2.2 | 4 | µs |
| $I_{DD(HSI)}$(2) | HSI oscillator power consumption | - | - | 60 | 80 | µA |

1. $V_{DD}$ = 3.3 V, $T_A$ = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design
3. Based on characterization
4. Factory calibrated, parts not soldered.

**Figure 31. $ACC_{HSI}$ versus temperature**




1. Guaranteed by characterization results.

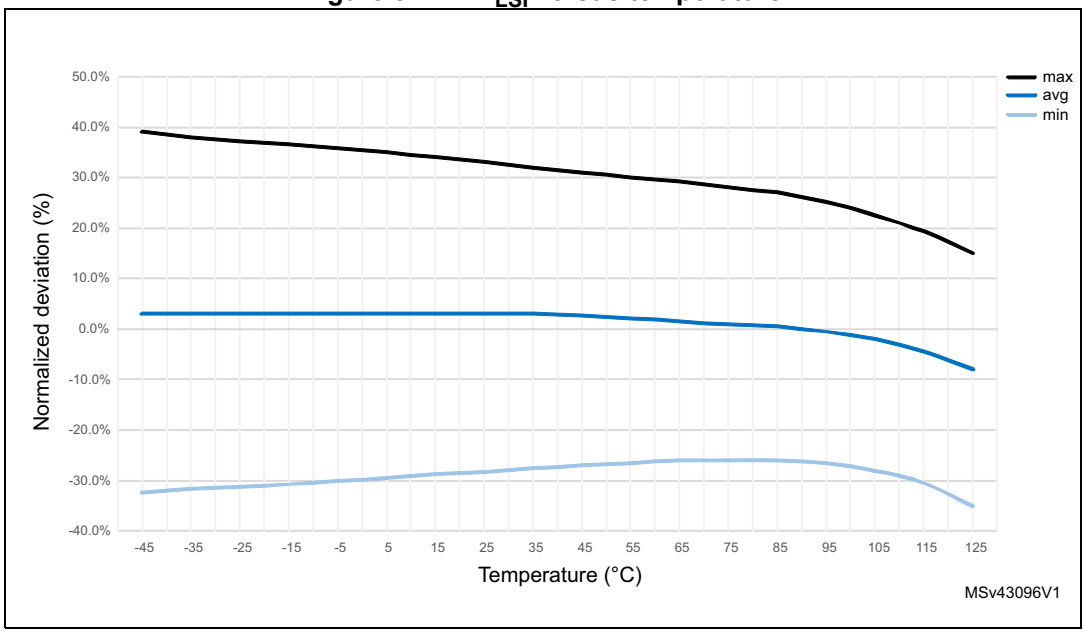
## Low-speed internal (LSI) RC oscillator

**Table 46. LSI oscillator characteristics (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$ (2) | Frequency | 16.1 | 32.0 | 47.0 | kHz |
| $t_{su(LSI)}$ (3) | LSI oscillator startup time | - | 15.0 | 40.0 | µs |
| $I_{DD(LSI)}$ (3) | LSI oscillator power consumption | - | 0.4 | 0.6 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 125 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

**Figure 32. $ACC_{LSI}$ versus temperature**



### 6.3.10 PLL characteristics

The parameters given in *Table 47* and *Table 48* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 47. Main PLL characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{PLL_IN}$ | PLL input clock(1) | - | | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLLP_OUT}$ | PLLP multiplier output clock | - | | 24 | - | 100 | |
| $f_{PLLQ_OUT}$ | 48 MHz PLLQ multiplier output clock | - | | - | 48 | 75 | |
| $f_{PLLR_OUT}$ | PLLR multiplier output clock for I2S and SAI | - | | - | - | 216 | |
| $f_{VCO_OUT}$ | PLL VCO output | - | | 100 | - | 432 | |
| $t_{LOCK}$ | PLL lock time | VCO freq = 100 MHz | | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | | 100 | - | 300 | |
| Jitter(3) | Cycle-to-cycle jitter | System clock 100 MHz | RMS | - | 25 | - | ps |
| | | | peak to peak | - | ±150 | - | |
| | Period Jitter | | RMS | - | 15 | - | |
| | | | peak to peak | - | ±200 | - | |
| | Bit Time CAN jitter | Cycle to cycle at 1 MHz on 1000 samples. | | - | 330 | - | |
| $I_{DD(PLL)}$(4) | PLL power consumption on VDD | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLL)}$(4) | PLL power consumption on VDDA | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.30<br>0.55 | - | 0.40<br>0.85 | |

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

**Table 48. PLLI2S (audio PLL) characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{PLL_IN}$ | PLL input clock(1) | - | | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLLI2SQ_OUT}$ | 48 MHz PLLI2SQ multiplier output clock | - | | - | 48 | 75 | |
| $f_{PLLI2SR_OUT}$ | PLLI2SR multiplier output clock for I2S and SAI | - | | - | - | 216 | |
| $f_{VCO_OUT}$ | PLLI2S VCO output | - | | 100 | - | 432 | |
| $t_{LOCK}$ | PLLI2S lock time | VCO freq = 100 MHz | | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | | 100 | - | 300 | |
| Jitter(3) | Master I2S clock jitter | Cycle to cycle at 12.288 MHz on 48 kHz period, N=432, R=5 | RMS | - | 90 | - | ps |
| | | | peak to peak | - | ±280 | - | |
| | | Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples | | - | 90 | - | |
| | WS I2S clock jitter | Cycle to cycle at 48 KHz on 1000 samples | | - | 400 | - | |
| $I_{DD(PLLI2S)}$(4) | PLLI2S power consumption on $V_{DD}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLLI2S)}$(4) | PLLI2S power consumption on $V_{DDA}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.30<br>0.55 | - | 0.40<br>0.85 | |

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

### 6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 55: EMI characteristics for LQFP144*). It is available only on the main PLL.

**Table 49. SSCG parameter constraints**

| Symbol | Parameter | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $f_{Mod}$ | Modulation frequency | - | - | 10 | kHz |
| md | Peak modulation depth | 0.25 | - | 2 | % |
| MODEPER * INCSTEP | (Modulation period) * (Increment Step) | - | - | $2^{15}$-1 | - |

1. Guaranteed by design.

**Equation 1**

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL_IN} / (4 \times f_{Mod})]$$

$f_{PLL_IN}$ and $f_{Mod}$ must be expressed in Hz.

As an example:

If $f_{PLL_IN}$ = 1 MHz, and $f_{MOD}$ = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

**Equation 2**

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

$f_{VCO_OUT}$ must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126 md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(peak)$$

*Figure 33* and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is $f_{PLL_OUT}$ nominal.

$T_{mode}$ is the modulation period.

md is the modulation depth.

**Figure 33. PLL output clock waveforms in center spread mode**

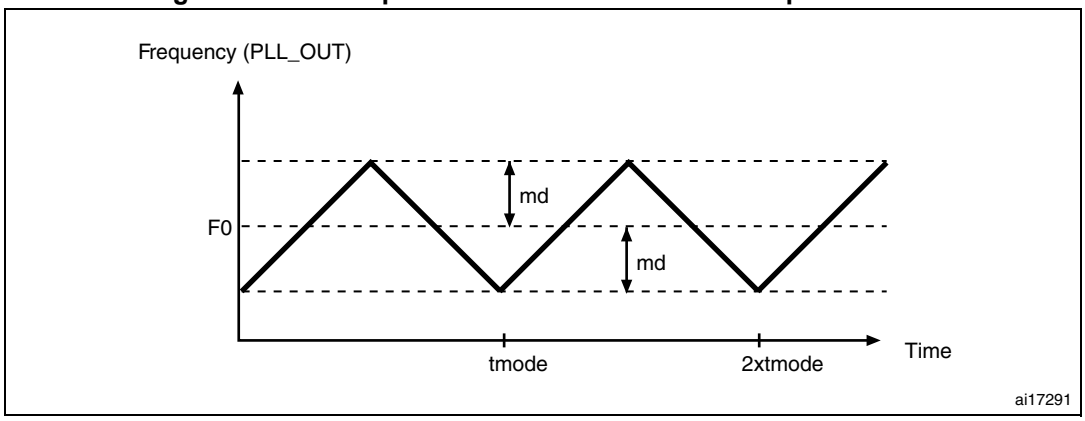
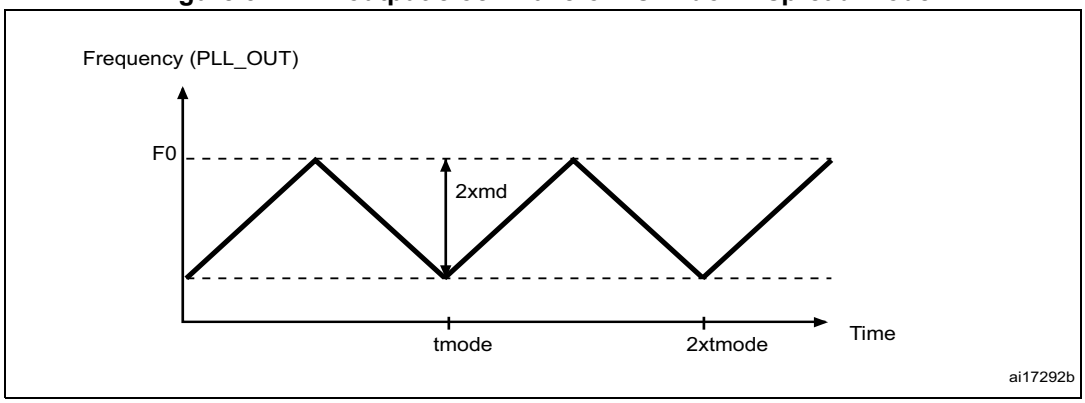



**Figure 34. PLL output clock waveforms in down spread mode**




## 6.3.12 Memory characteristics

### Flash memory

The characteristics are given at $T_A$ = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

**Table 50. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Write / Erase 8-bit mode, $V_{DD}$ = 1.7 V | - | 5 | - | mA |
| | | Write / Erase 16-bit mode, $V_{DD}$ = 2.1 V | - | 8 | - | |
| | | Write / Erase 32-bit mode, $V_{DD}$ = 3.3 V | - | 12 | - | |

**Table 51. Flash memory programming**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Word programming time | Program/erase parallelism (PSIZE) = x 8/16/32 | - | 16 | 100(2) | µs |
| $t_{ERASE16KB}$ | Sector (16 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 400 | 800 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 300 | 600 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 250 | 500 | |
| $t_{ERASE64KB}$ | Sector (64 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 1200 | 2400 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 700 | 1400 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 550 | 1100 | |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 2 | 4 | s |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 1.3 | 2.6 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 1 | 2 | |
| $t_{ME}$ | Mass erase time | Program/erase parallelism (PSIZE) = x 8 | - | 24 | 48 | s |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 15 | 30 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 11 | 22 | |
| $V_{prog}$ | Programming voltage | 32-bit program operation | 2.7 | - | 3.6 | V |
| | | 16-bit program operation | 2.1 | - | 3.6 | V |
| | | 8-bit program operation | 1.7 | - | 3.6 | V |

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

**Table 52. Flash memory programming with $V_{PP}$ voltage**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Double word programming | $T_A$ = 0 to +40 °C<br>$V_{DD}$ = 3.3 V<br>$V_{PP}$ = 8.5 V | - | 16 | 100(2) | µs |
| $t_{ERASE16KB}$ | Sector (16 KB) erase time | | - | 230 | - | ms |
| $t_{ERASE64KB}$ | Sector (64 KB) erase time | | - | 490 | - | |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | | - | 875 | - | |
| $t_{ME}$ | Mass erase time | | - | 9.8 | - | s |
| $V_{prog}$ | Programming voltage | - | 2.7 | - | 3.6 | V |
| $V_{PP}$ | $V_{PP}$ voltage range | - | 7 | - | 9 | V |
| $I_{PP}$ | Minimum current sunk on the $V_{PP}$ pin | - | 10 | - | - | mA |
| $t_{VPP}$(3) | Cumulative time during which $V_{PP}$ is applied | - | - | - | 1 | hour |

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. $V_{PP}$ should only be connected during programming/erasing.

**Table 53. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{END}$ | Endurance | $T_A$ = –40 to +85 °C (temp. range 6)<br>$T_A$ = –40 to +105 °C (temp. range 7)<br>$T_A$ = –40 to +125 °C (temp. range 3) | 10 | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle(2) at $T_A$ = 85 °C | 30 | Years |
| | | 1 kcycle(2) at $T_A$ = 105 °C | 10 | |
| | | 1 kcycle(2) at $T_A$ = 125 °C | 3 | |
| | | 10 kcycle(2) at $T_A$ = 55 °C | 20 | |

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

### 6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 55*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 54. EMS characteristics for LQFP144 package**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP144<br>$T_A$ = +25 °C, $f_{HCLK}$ = 100 MHz,<br>conforms to IEC 61000-4-2 | 1B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP144<br>$T_A$ = +25 °C, $f_{HCLK}$ = 100 MHz,<br>conforms to IEC 61000-4-4 | 3B |

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP81.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

**Software recommendations**

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

**Table 55. EMI characteristics for LQFP144**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{CPU}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/100 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP144 package, conforming to IEC 61967-2, EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled. | 0.1 to 30 MHz | 13 | dBµV |
| | | | 30 to 130 MHz | 21 | |
| | | | 130 MHz to 1 GHz | 25 | |
| | | | 1 GHz to 2 GHz | 19 | |
| | | | EMI Level | 4 | - |

## 6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 56. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to ANSI/ESD STM5.3.1, UFBGA144, UFBGA100, LQFP144, LQFP100, WLCSP81, LQFP64 | 3 | 250 | |
| | | $T_A$ = +25 °C conforming to ANSI/ESD STM5.3.1, UFQFPN48 | 4 | 500 | |

1. Guaranteed by characterization results.

### Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

**Table 57. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +125 °C conforming to JESD78A | II level A |

## 6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 58*.

**Table 58. I/O current injection susceptibility(1)**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0, PDR_ON, BYPASS_REG | - 0 | 0 | mA |
| | Injected current on NRST | - 0 | NA | |
| | Injected current on PE6, PC13, PC14, PC15, PF0, PF1, PF2, PC0, PC1, PC2, PC3 | - 0 | NA | |
| | Injected current on any other FT and FTf pins | - 5 | NA | |
| | Injected current on any other pins | - 5 | + 5 | |

1. NA = not applicable.

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

## 6.3.16 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

**Table 59. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | FT, TTa, TC and NRST I/O input low level voltage | 1.7 V≤$V_{DD}$≤3.6 V | - | - | $0.3V_{DD}$(1) | V |
| | BOOT0 I/O input low level voltage | 1.75 V≤$V_{DD}$ ≤3.6 V, -40 °C≤$T_A$ ≤125 °C | - | - | $0.1V_{DD}$+0.1(2) | |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤125 °C | - | - | | |
| $V_{IH}$ | FT, TTa, TC and NRST I/O input high level voltage(6) | 1.7 V≤$V_{DD}$≤3.6 V | $0.7V_{DD}$(1) | - | - | V |
| | BOOT0 I/O input high level voltage | 1.75 V≤$V_{DD}$ ≤3.6 V, -40 °C≤$T_A$ ≤125 °C | $0.17V_{DD}$+0.7(2) | - | - | |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤125 °C | | | | |
| $V_{HYS}$(3) | FT, TTa, TC and NRST I/O input hysteresis | 1.7 V≤$V_{DD}$≤3.6 V | 10% $V_{DD}$(2)(4) | - | - | V |
| | BOOT0 I/O input hysteresis | 1.75 V≤$V_{DD}$ ≤3.6 V, -40 °C≤$T_A$ ≤125 °C | 0.1 | - | - | |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤125 °C | | | | |

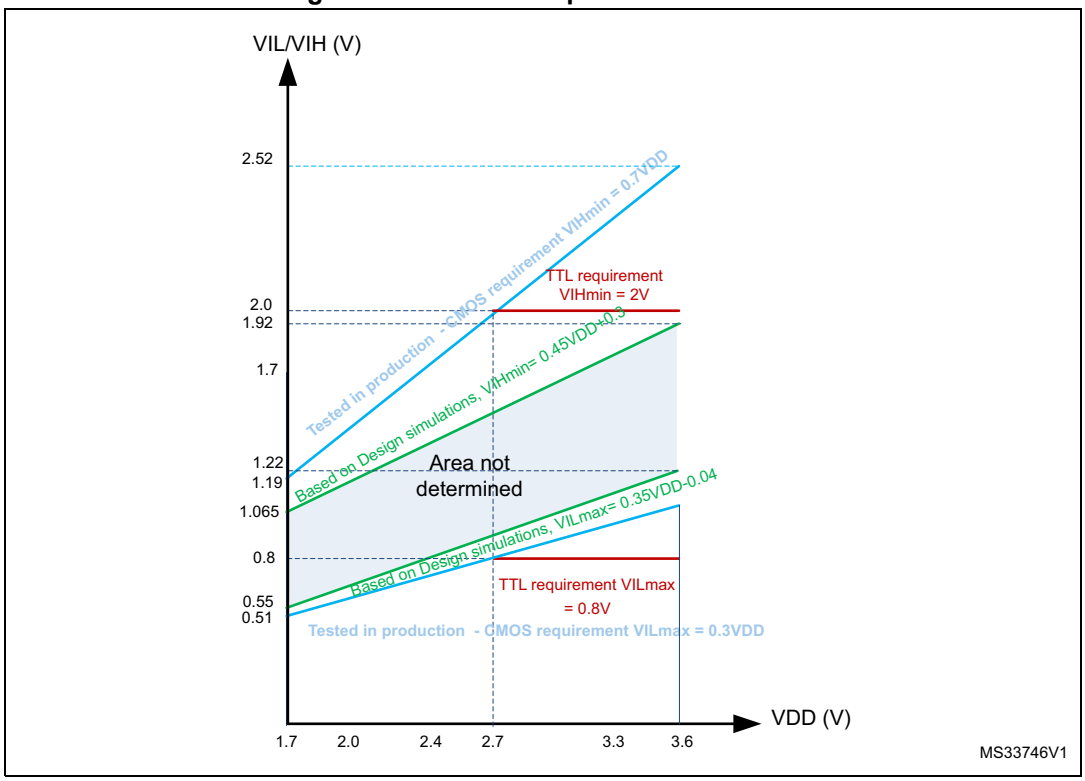
**Table 59. I/O static characteristics (continued)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{lkg}$ | I/O input leakage current (5) | | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |
| | I/O FT/TC input leakage current (6) | | $V_{IN}$ = 5 V | - | - | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(7) | All pins except for PA10 (OTG_FS_ID) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| | | PA10 (OTG_FS_ID) | - | 7 | 10 | 14 | |
| $R_{PD}$ | Weak pull-down equivalent resistor(8) | All pins except for PA10 (OTG_FS_ID) | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | |
| | | PA10 (OTG_FS_ID) | - | 7 | 10 | 14 | |
| $C_{IO}$ | I/O pin capacitance | | - | - | 5 | - | pF |

1. Guaranteed by test in production.
2. Guaranteed by design.
3. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
4. With a minimum of 200 mV.
5. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 58: I/O current injection susceptibility*
6. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 58: I/O current injection susceptibility*
7. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
8. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in *Figure 35*.

Figure 35. FT/TC I/O input characteristics




## Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed $V_{OL}/V_{OH}$) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 15*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 15*).

## Output voltage levels

Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

**Table 60. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin | CMOS port(2) $I_{IO}$ = +8 mA 2.7 V ≤$V_{DD}$ ≤3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–0.4 | - | |
| $V_{OL}$ (1) | Output low level voltage for an I/O pin | TTL port(2) $I_{IO}$ =+8 mA 2.7 V ≤$V_{DD}$ ≤3.6 V | - | 0.4 | V |
| $V_{OH}$ (3) | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = + 20 mA 2.7 V ≤$V_{DD}$ ≤3.6 V | - | 1.3(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–1.3(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = + 6 mA 1.8 V ≤$V_{DD}$ ≤3.6 V | - | 0.4(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–0.4(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +4 mA 1.7 V ≤$V_{DD}$ ≤3.6 V | - | 0.4(5) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–0.4(5) | - | |
| $V_{OLFM}$(1) | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO}$ = + 20 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | V |
| $V_{OLFM}$(1) | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO}$ = + 10 mA 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | V |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
4. Guaranteed by characterization results.
5. Guaranteed by design.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 36* and *Table 61*, respectively.

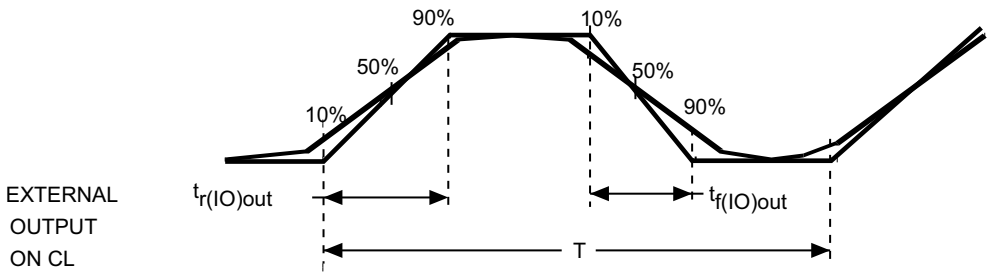
Unless otherwise specified, the parameters given in *Table 61* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 61. I/O AC characteristics(1)(2)**

| OSPEEDRy [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ ≥ 2.70 V | - | - | 4 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$≥ 1.7 V | - | - | 2 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 8 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 4 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ = 1.7 V to 3.6 V | - | - | 100 | ns |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ ≥ 2.70 V | - | - | 25 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ ≥ 1.7 V | - | - | 12.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 20 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ ≥2.7 V | - | - | 10 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ ≥ 1.7 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 6 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 10 | |
| 10 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 40 pF, $V_{DD}$ ≥ 2.70 V | - | - | 50(4) | MHz |
| | | | $C_L$ = 40 pF, $V_{DD}$ ≥ 1.7 V | - | - | 25 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 100(4) | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 50(4) | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 40 pF, $V_{DD}$≥ 2.70 V | - | - | 6 | ns |
| | | | $C_L$ = 40 pF, $V_{DD}$≥ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 2.70 V | - | - | 4 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.7 V | - | - | 6 | |
| 11 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 30 pF, $V_{DD}$ ≥ 2.70 V | - | - | 100(4) | MHz |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥ 1.7 V | - | - | 50(4) | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ ≥ 2.70 V | - | - | 4 | ns |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥ 1.7 V | - | - | 6 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 2.70 V | - | - | 2.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.7 V | - | - | 4 | |
| FM+ | Fmax | Maximum frequency | $C_L$ = 50 pF, 1.6 ≤ $V_{DD}$ ≤ 3.6 V | - | - | 1 | MHz |
| | Tf | Output high to low level fall time | | - | - | 5 | ns |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10 | - | - | ns |

1. Guaranteed by characterization results.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 36*.
4. For maximum frequencies above 50 MHz and $V_{DD}$ > 2.4 V, the compensation cell should be used.

**Figure 36. I/O AC characteristics definition**




Maximum frequency is achieved if ($t_r$ + $t_f$) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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## 6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 59*).

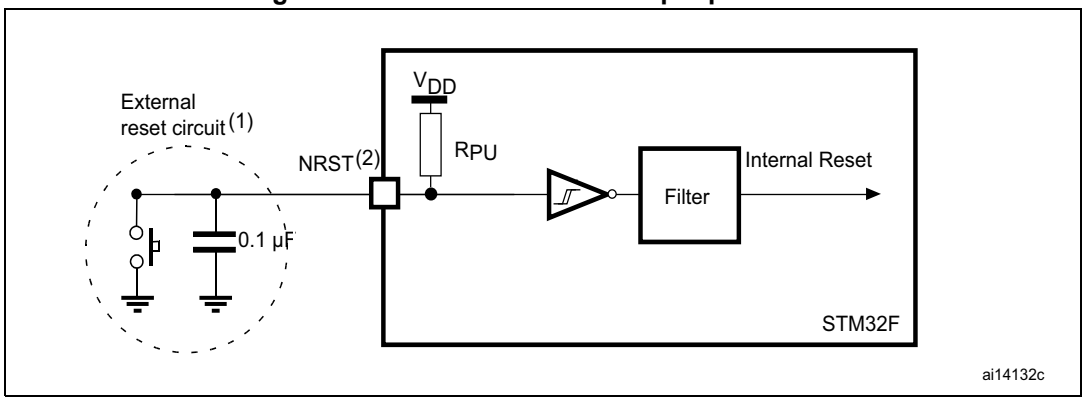
Unless otherwise specified, the parameters given in *Table 62* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*. Refer to *Table 59: I/O static characteristics* for the values of VIH and VIL for NRST pin.

**Table 62. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up equivalent resistor(1) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(2) | NRST Input filtered pulse | - | - | - | 100 | ns |
| $V_{NF(NRST)}$(2) | NRST Input not filtered pulse | $V_{DD}$ > 2.7 V | 300 | - | - | ns |
| $T_{NRST_OUT}$ | Generated reset pulse duration | Internal Reset source | 20 | - | - | µs |

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

**Figure 37. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 62*. Otherwise the reset is not taken into account by the device.

## 6.3.18 TIM timer characteristics

The parameters given in *Table 63* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 63. TIMx characteristics(1)(2)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 100 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 11.9 | - | ns |
| | | AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 100 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 11.9 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK}$ = 100 MHz | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | | 0 | 50 | MHz |
| $Res_{TIM}$ | Timer resolution | | - | 16/32 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | $f_{TIMxCLK}$ = 100 MHz | 0.0119 | 780 | µs |
| $t_{MAX_COUNT}$ | Maximum possible count with 32-bit counter | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 100 MHz | - | 51.1 | S |

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 is 50 MHz and on APB2 is up to 100 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

## 6.3.19 Communications interfaces

### $I^2C$ interface characteristics

The $I^2C$ interface meets the requirements of the standard $I^2C$ communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The $I^2C$ characteristics are described in *Table 64*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

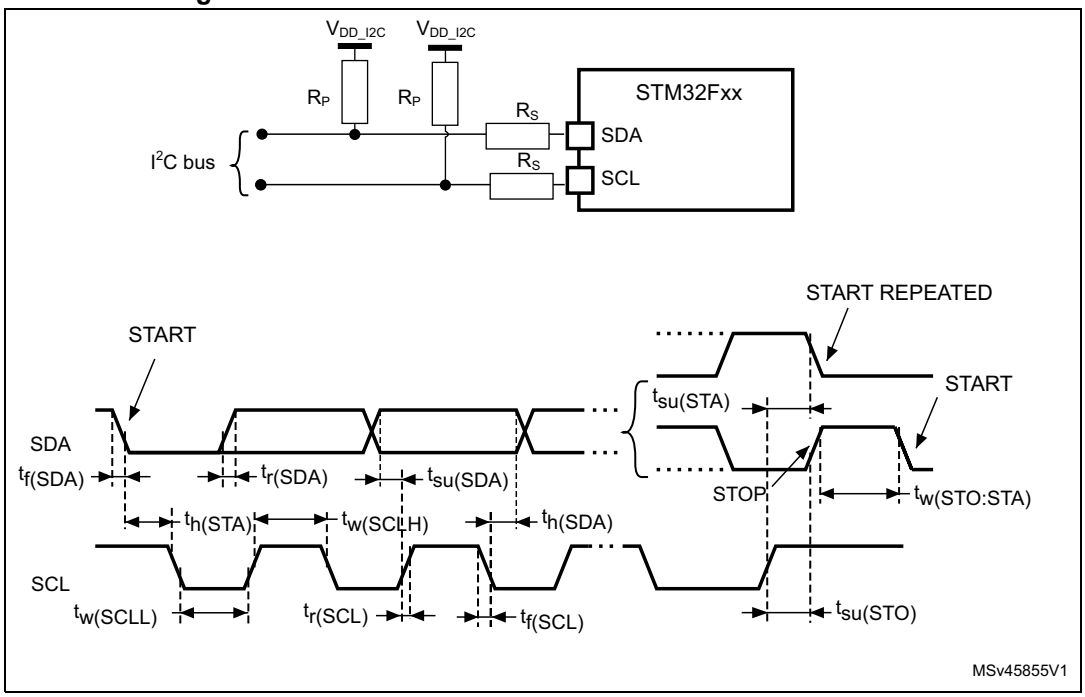
The $I^2C$ bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The $I^2C$ bus frequency can be increased up to 1 MHz. For more details about the complete solution, contact your local ST sales representative.

**Table 64. $I^2C$ characteristics**

| Symbol | Parameter | Standard mode $I^2C$(1)(2) | | Fast mode $I^2C$(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.70 | - | 1.30 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.60 | - | |
| $t_{su(SDA)}$ | SDA setup time | 0.25 | - | 0.10 | - | |
| $t_{h(SDA)}$ | SDA data hold time | 0 | - | 0 | - | |
| $t_{v(SDA,ACK)}$ | SDA data hold time | - | 3.45(3) | - | 0.90(4) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 0.100 | - | 0.30 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 0.30 | - | 0.30 | |
| $t_{h(STA)}$ | Start condition hold time | 4 | - | 0.6 | - | |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 4 | - | 0.60 | - | |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.70 | - | 1.3 | - | |
| $t_{SP}$ | Pulse width of the spikes that are suppressed by the analog filter for standard fast mode | - | - | 0.05 | 0.10(5) | |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. Guaranteed by design.
2. $f_{PCLK1}$ must be at least 2 MHz to achieve standard mode $I^2C$ frequencies. It must be at least 4 MHz to achieve fast mode $I^2C$ frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum $I^2C$ fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above $t_{SP}$ (max)

**Figure 38. I²C bus AC waveforms and measurement circuit**




1. $R_S$ = series protection resistor.
2. $R_P$ = external pull-up resistor.
3. $V_{DD_I2C}$ is the I2C bus power supply.

**Table 65. SCL frequency ($f_{PCLK1}$= 50 MHz, $V_{DD}$ = $V_{DD_I2C}$ = 3.3 V)(1)(2)**

| $f_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | $R_P$ = 4.7 kΩ |
| 400 | 0x8019 |
| 300 | 0x8021 |
| 200 | 0x8032 |
| 100 | 0x0096 |
| 50 | 0x012C |
| 20 | 0x02EE |

1. $R_P$ = External pull-up resistance, $f_{SCL}$ = I²C speed
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

### FMPI$^2$C characteristics

The following table presents FMPI$^2$C characteristics.

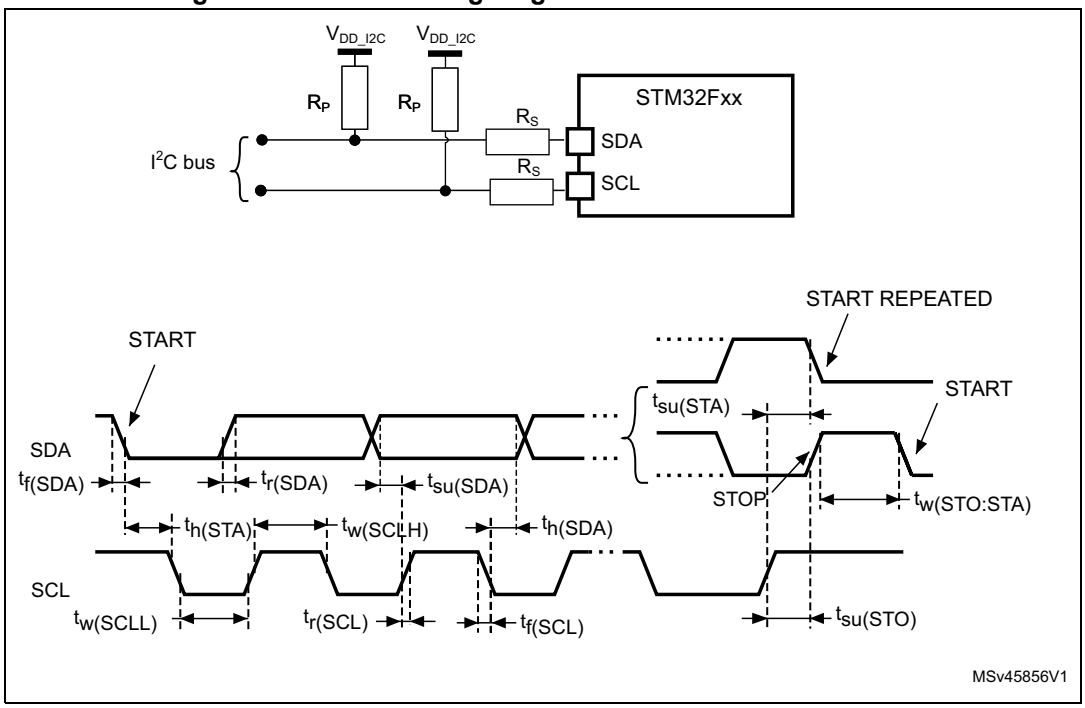
Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output function characteristics (SDA and SCL).

**Table 66. FMPI$^2$C characteristics(1)**

| | Parameter | Standard mode | | Fast mode | | Fast+ mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{FMPI2CC}$ | $F_{MPI2CCLK}$ frequency | 2 | - | 8 | - | 18 | - | µs |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | 0.5 | - | |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | 0.26 | - | |
| $t_{su(SDA)}$ | SDA setup time | 0.25 | - | 0.10 | - | 0.05 | - | |
| $t_{H(SDA)}$ | SDA data hold time | 0 | - | 0 | - | 0 | - | |
| $t_{v(SDA,ACK)}$ | Data, ACK valid time | - | 3.45 | - | 0.9 | - | 0.45 | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1.0 | - | 0.30 | - | 0.12 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 0.30 | - | 0.30 | -0 | 0.12 | |
| $t_{h(STA)}$ | Start condition hold time | 4 | - | 0.6 | - | 0.26 | - | |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | - | 0.6 | - | 0.26 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 4 | - | 0.6 | - | 0.26 | - | |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | - | 1.3 | - | 0.5 | - | |
| $t_{SP}$ | Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode | - | - | 0.05 | 0.1 | 0.05 | 0.1 | |
| $C_b$ | Capacitive load for each bus Line | - | 400 | - | 400 | - | 550(2) | pF |

1. Based on characterization results.
2. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:
   $t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$
   $R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

**Figure 39. FMPI$^2$C timing diagram and measurement circuit**



### SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 67* for the SPI interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 67. SPI dynamic characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode,<br>SPI1,4,5<br>3.0 V < $V_{DD}$ < 3.6 V | - | - | 50 | MHz |
| | | Master mode,<br>SPI1,4,5<br>2.7 V < $V_{DD}$ < 3.6 V | - | - | 42 | |
| | | Master mode<br>SPI1,4,5<br>1.7 V < $V_{DD}$ < 3.6 V | - | - | 25 | |
| | | Master transmitter mode<br>SPI1,4,5<br>1.71 V < $V_{DD}$ < 3.6 V | - | - | 50 | |
| | | Slave receiver mode<br>SPI1,4,5<br>1.71 V < $V_{DD}$ < 3.6 V | - | - | 50 | |
| | | Slave mode transmitter/full duplex<br>SPI1,4,5<br>2.7 V < $V_{DD}$ < 3.6 V | - | - | 40(2) | |
| | | Slave mode transmitter/full duplex<br>SPI1,4,5<br>1.71 V < $V_{DD}$ < 3.6 V | - | - | 26 | |
| | | Master & Slave mode,<br>SPI2/3<br>1.71 V < $V_{DD}$ < 3.6 V | - | - | 25 | |
| $t_{su(NSS)}$ | NSS setup time | Slave mode, SPI presc = 2 | $4*T_{PCLK}$ | - | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode, SPI presc = 2 | $2*T_{PCLK}$ | - | - | ns |
| $t_{w(SCKH)}$<br>$t_{w(SCKL)}$ | SCK high and low time | Master mode | $T_{PCLK}$ - 2 | $T_{PCLK}$ | $T_{PCLK}$ +2 | ns |
| $t_{su(MI)}$ | Data input setup time | Master mode | 2.5 | - | - | ns |
| $t_{su(SI)}$ | | Slave mode | 4.5 | - | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 5 | - | - | ns |
| $t_{h(SI)}$ | | Slave mode | 2 | - | - | |

**Table 67. SPI dynamic characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{a(SO)}$ | Data output access time | Slave mode | 7 | - | 21 | ns |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 5 | - | 12 | ns |
| $t_{v(SO)}$ | Data output valid time | Slave mode (after enable edge), 2.7 V < $V_{DD}$ < 3.6 V | - | 7 | 12.5 | ns |
| | | Slave mode (after enable edge), 1.71 V < $V_{DD}$ < 3.6 V | - | 7 | 19 | |
| $t_{v(MO)}$ | | Master mode | - | 2 | 3 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode 1.71 V < $V_{DD}$ < 3.6 V | 6 | - | - | ns |
| $t_{h(MO)}$ | | Master mode | 1.5 | - | - | |

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

**Figure 40. SPI timing diagram - slave mode and CPHA = 0**

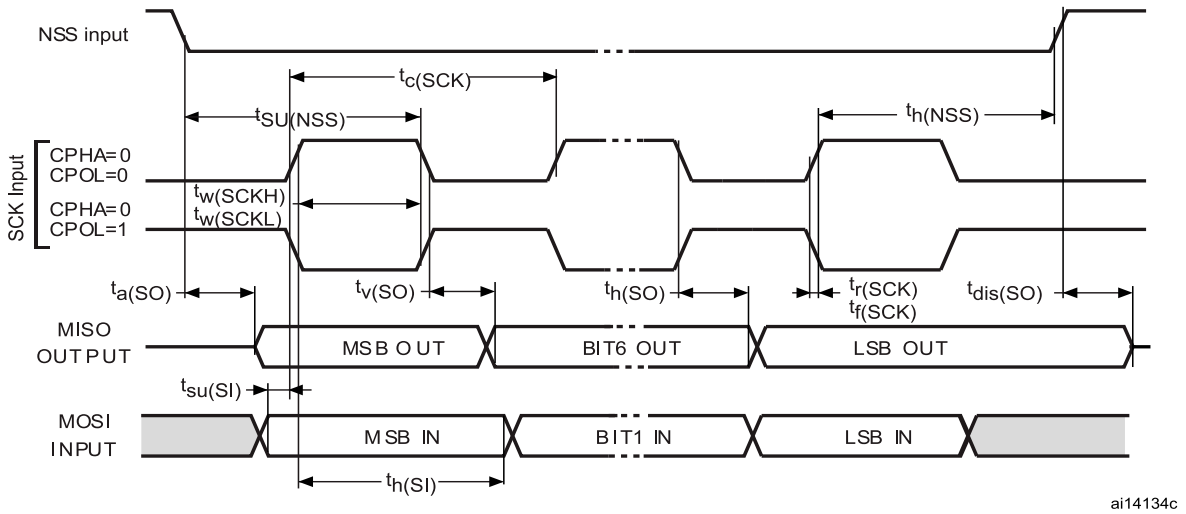


**Figure 41. SPI timing diagram - slave mode and CPHA = 1**

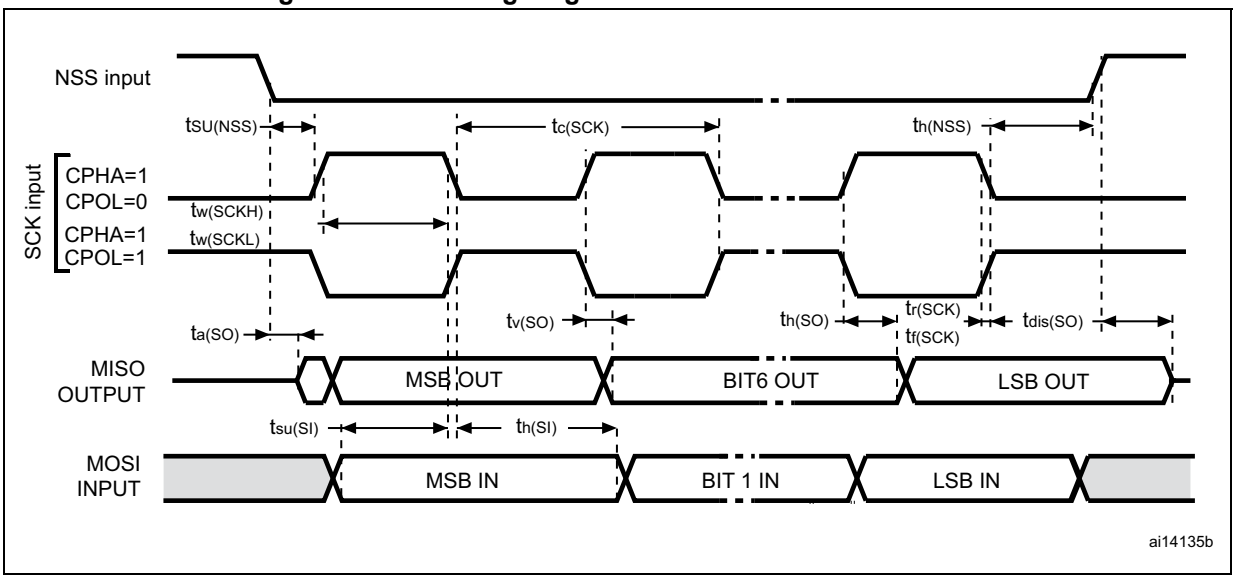
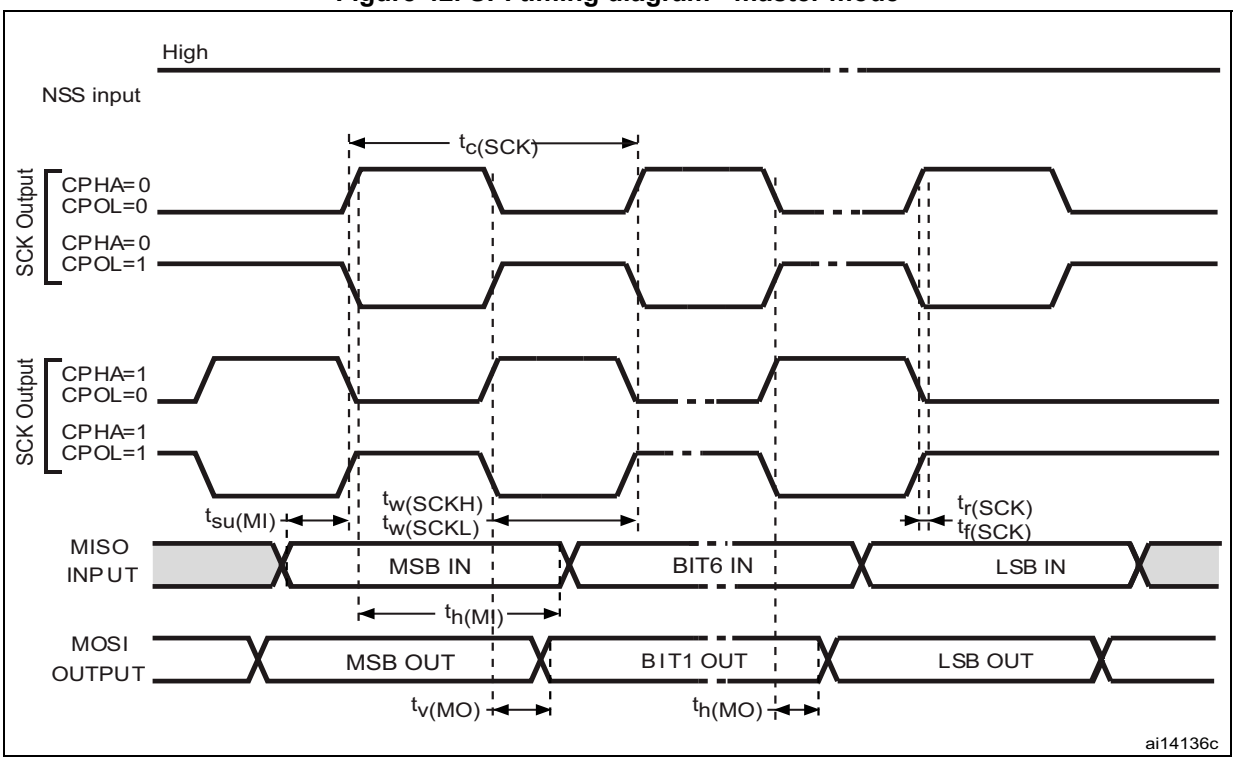



**Figure 42. SPI timing diagram - master mode**



### I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 68* for the I²S interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

**Table 68. I²S dynamic characteristics(1)**

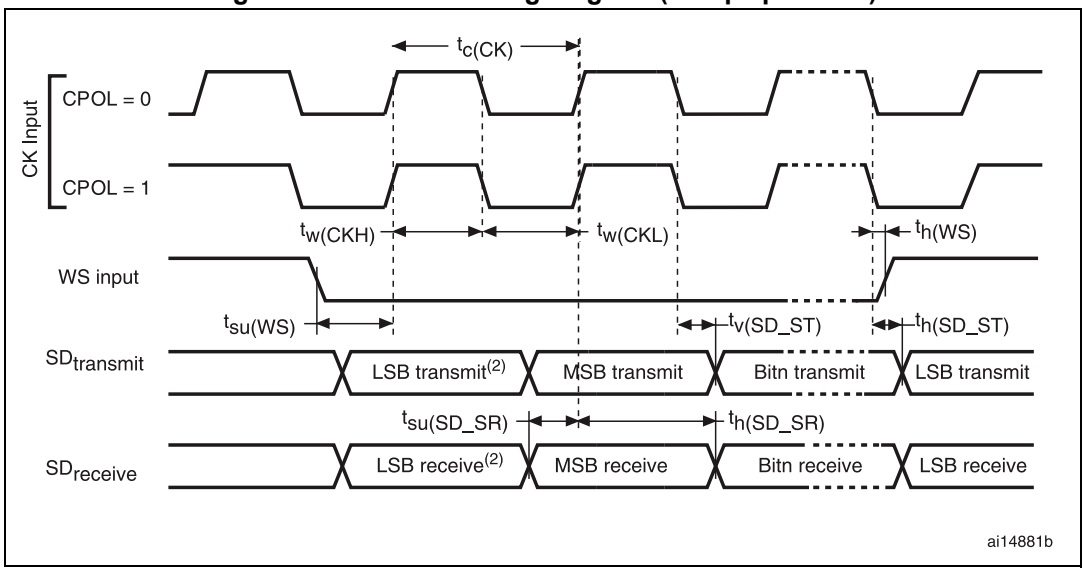
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCK}$ | I2S Main clock output | - | 256 * 8K | 256 * Fs(2) | MHz |
| $f_{CK}$ | I2S clock frequency | Master data: 32 bits | - | 64 * Fs | MHz |
| | | Slave data: 32 bits | - | 64 * Fs | |
| $D_{CK}$ | I2S clock frequency duty cycle | Slave receiver | 30 | 70 | % |
| $t_{v(WS)}$ | WS valid time | Master mode | - | 3.5 | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 1.5 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 2.5 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 0.5 | - | |
| $t_{su(SD_MR)}$ | Data input setup time | Master receiver | 3 | - | |
| $t_{su(SD_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{h(SD_MR)}$ | Data input hold time | Master receiver | 5 | - | |
| $t_{h(SD_SR)}$ | | Slave receiver | 1.5 | - | |
| $t_{v(SD_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 15 | |
| $t_{v(SD_MT)}$ | | Master transmitter (after enable edge) | - | 6 | |
| $t_{h(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 3.5 | - | |
| $t_{h(SD_MT)}$ | | Master transmitter (after enable edge) | 1.5 | - | |

1. Guaranteed by characterization results.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

*Note: Refer to the I2S section of RM0430 reference manual for more details on the sampling frequency ($F_S$).*

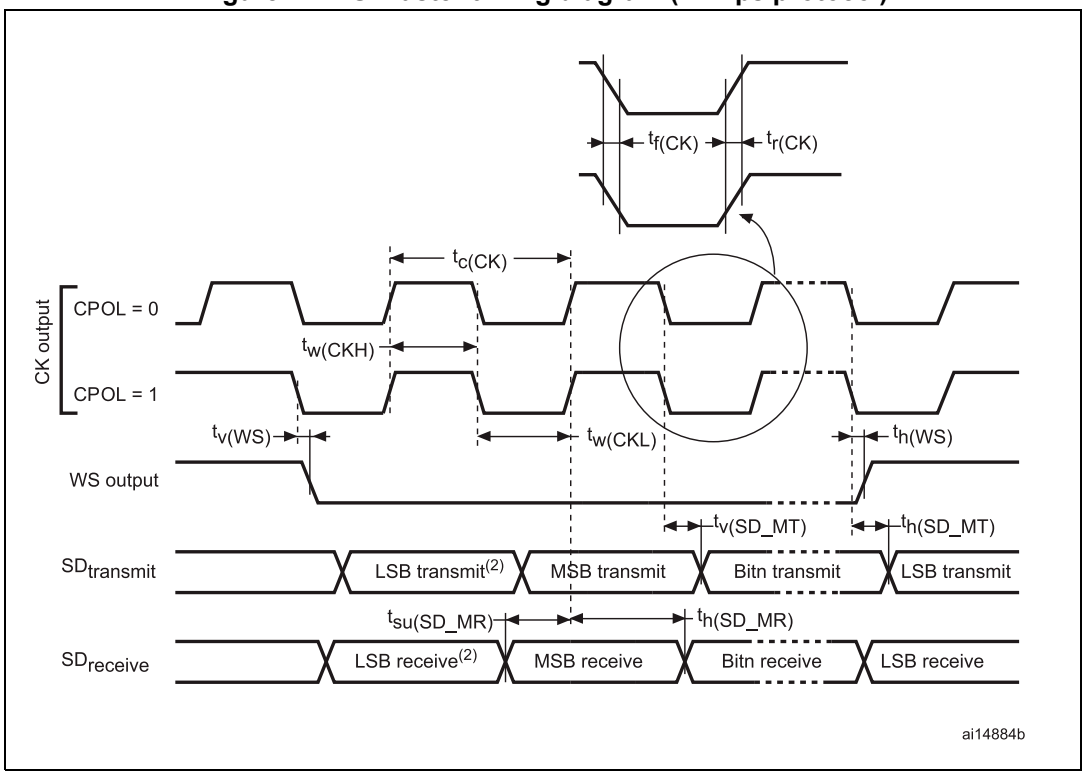
*$f_{MCK}$, $f_{CK}$, and $D_{CK}$ values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. $D_{CK}$ depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). $F_S$ maximum value is supported for each mode/condition.*

**Figure 43. I²S slave timing diagram (Philips protocol)**




1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 44. I²S master timing diagram (Philips protocol)**




1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### SAI characteristics

Unless otherwise specified, the parameters given in *Table 69* for SAI are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

**Table 69. SAI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCKL}$ | SAI Main clock output | - | 256 * 8K | 256 * Fs(2) | MHz |
| $F_{SCK}$ | SAI clock frequency | Master data: 32 bits | - | 128 * Fs | MHz |
| | | Slave data: 32 bits | - | 128 * Fs | |
| $t_{v(FS)}$ | FS valid time | Master mode 2.7 V <= $V_{DD}$ <= 3.6 V | - | 19 | ns |
| | | Master mode 1.71 V <= $V_{DD}$ <= 3.6 V | - | 28 | |
| $t_{h(FS)}$ | FS hold time | Master mode | 13 | - | |
| | | Slave mode | 0 | - | |
| $t_{su(FS)}$ | FS setup time | Slave mode | 3 | - | |
| $t_{su(SD_A_MR)}$ | Data input setup time | Master receiver | 0.5 | - | |
| $t_{su(SD_B_SR)}$ | | Slave receiver | 1.5 | - | |
| $t_{h(SD_A_MR)}$ | Data input hold time | Master receiver | 5 | - | |
| $t_{h(SD_B_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{v(SD_B_ST)}$ | Data output valid time | Slave transmitter (after enable edge) 2.7 V <= $V_{DD}$ <= 3.6 V | - | 15 | |
| | | Slave transmitter (after enable edge) 1.71 V <= $V_{DD}$ <= 3.6 V | - | 28 | |
| $t_{h(SD_B_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 10 | - | |
| $t_{v(SD_A_MT)}$ | Data output valid time | Master transmitter (after enable edge) 2.7 V <= $V_{DD}$ <= 3.6 V | - | 15 | |
| | | Master transmitter (after enable edge) 1.71 V <= $V_{DD}$ <= 3.6 V | - | 29 | |
| $t_{h(SD_A_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 13 | - | |

1. Guaranteed by characterization results.
2. 256 * Fs maximum corresponds to 45 MHz (APB2 maximum frequency)

**Figure 45. SAI master timing waveforms**

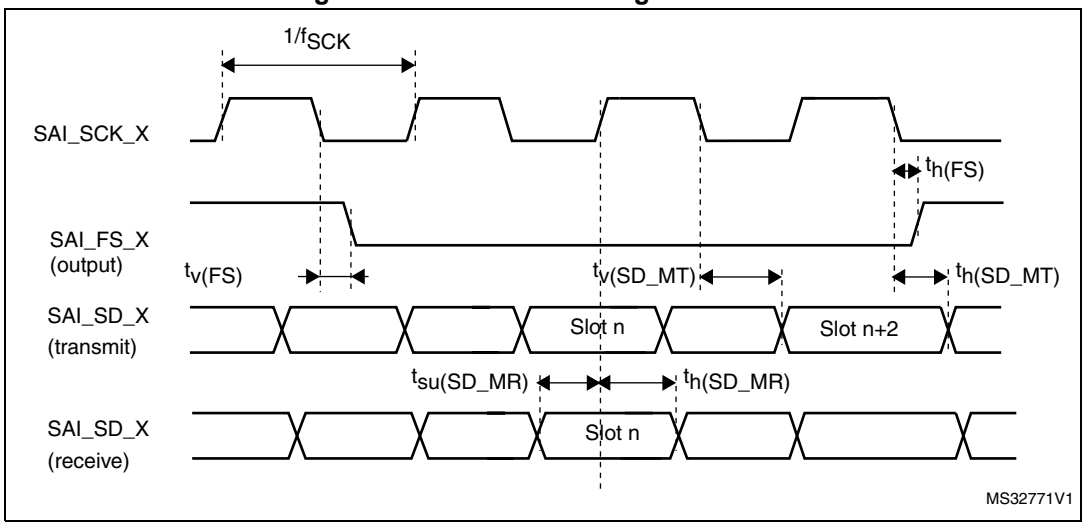
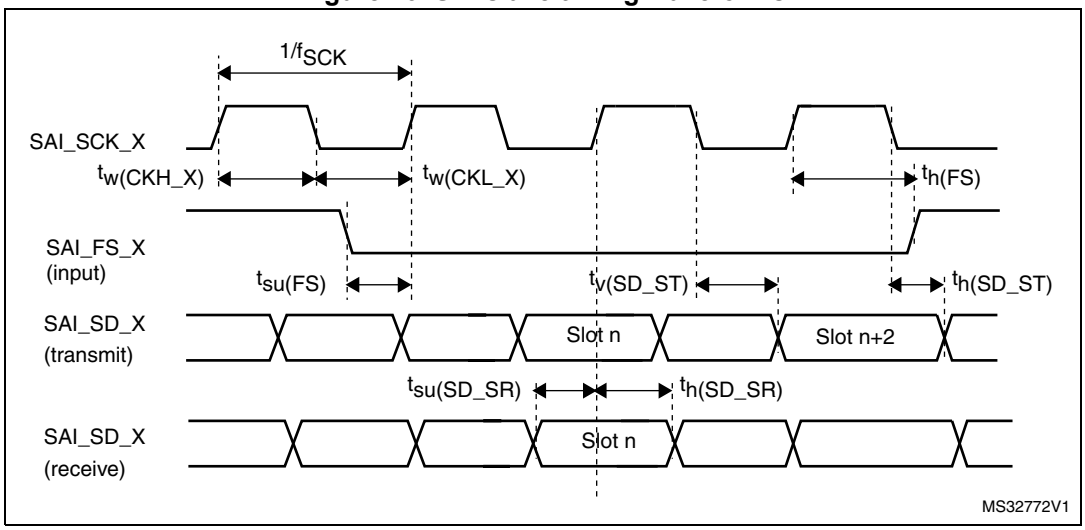



**Figure 46. SAI slave timing waveforms**



### QSPI interface characteristics

Unless otherwise specified, the parameters given in the following tables for QSPI are derived from tests performed under the ambient temperature, $f_{AHB}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C=20pF
- Measurement points are done at CMOS levels: 0.5VDD

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics.

**Table 70. QSPI dynamic characteristics in SDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | QSPI clock frequency | 2.7 V < $V_{DD}$ < 3.6 V<br>$C_{load}$ = 20 pF | - | - | 100 | MHz |
| | | 1.71 V < $V_{DD}$ < 3.6 V<br>$C_{load}$ = 15 pF | - | - | 80 | |
| $t_{w(CKH)}$ | QSPI clock high and low | - | $t_{(CK)}$ / 2 - 1 | - | $t_{(CK)}$ / 2 | ns |
| $t_{w(CKL)}$ | | | $t_{(CK)}$ / 2 | - | $t_{(CK)}$ / 2 + 1 | |
| $t_{s(IN)}$ | Data input setup time | - | 1.5 | - | - | |
| $t_{h(IN)}$ | Data input hold time | - | 3 | - | - | |
| $t_{v(OUT)}$ | Data output valid time | 2.7 V < $V_{DD}$ < 3.6 V | - | 0.5 | 1 | |
| | | 1.71 V < $V_{DD}$ < 3.6 V | - | 0.5 | 3 | |
| $t_{h(OUT)}$ | Data output hold time | - | 0 | - | 0 | |

1. Guaranteed by characterization results.

**Table 71. QSPI dynamic characteristics in DDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | QSPI clock frequency | 2.7 V < $V_{DD}$ < 3.6 V<br>$C_{load}$ = 20 pF | - | - | 80 | MHz |
| | | 1.71 V< $V_{DD}$ < 3.6 V<br>$C_{load}$ = 15 pF | - | - | 70 | |

**Table 71. QSPI dynamic characteristics in DDR mode(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(CKH)}$ | QSPI clock high and low time | - | $t_{(CK)}$ / 2 - 1 | - | $t_{(CK)}$ / 2 | ns |
| $t_{w(CKL)}$ | | | $t_{(CK)}$ / 2 | - | $t_{(CK)}$ / 2 + 1 | |
| $t_{sr(IN)}$, $t_{sf(IN)}$ | Data input setup time | 2.7 V < $V_{DD}$ < 3.6 V | 0.5 | - | - | |
| | | 1.71 V < $V_{DD}$ < 3.6 V | 0.5 | - | - | |
| $t_{hr(IN)}$, $t_{hf(IN)}$ | Data input hold time | 2.7 V<$V_{DD}$<3.6 V | 2 | - | - | |
| | | 1.71 V<$V_{DD}$<3.6 V | 2 | - | - | |
| $t_{vr(OUT)}$, $t_{vf(OUT)}$ | Data output valid time | 2.7 V<$V_{DD}$<3.6 V | - | 8.5 | 9 | |
| | | 1.71 V<$V_{DD}$<3.6 V | - | 8.5 | 11.5 | |
| $t_{hr(OUT)}$, $t_{hf(OUT)}$ | Data output hold time | - | 7.5 | - | - | |

1. Guaranteed by characterization results.

## USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

**Table 72. USB OTG FS startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB OTG FS transceiver startup time | 1 | µs |

1. Guaranteed by design.

**Table 73. USB OTG FS DC electrical characteristics**

| Symbol | | Parameter | Conditions | Min.(1) | Typ. | Max.(1) | Unit |
|---|---|---|---|---|---|---|---|
| Input levels | $V_{DD}$ | USB OTG FS operating voltage | | 3.0(2) | - | 3.6 | V |
| | $V_{DI}$(3) | Differential input sensitivity | I(USB_FS_DP/DM) | 0.2 | - | - | V |
| | $V_{CM}$(3) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | - | 2.5 | |
| | $V_{SE}$(3) | Single ended receiver threshold | | 1.3 | - | 2.0 | |
| Output levels | $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(4) | - | - | 0.3 | V |
| | $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(4) | 2.8 | - | 3.6 | |
| $R_{PD}$ | | PA11, PA12 (USB_FS_DM/DP) | $V_{IN}$ = $V_{DD}$ | 17 | 21 | 24 | kΩ |
| | | PA9 (OTG_FS_VBUS) | | 0.65 | 1.1 | 2.0 | |
| $R_{PU}$ | | PA11, PA12 (USB_FS_DM/DP) | $V_{IN}$ = $V_{SS}$ | 1.5 | 1.8 | 2.1 | |
| | | PA9 (OTG_FS_VBUS) | $V_{IN}$ = $V_{SS}$ | 0.25 | 0.37 | 0.55 | |

1. All the voltages are measured from the local ground potential.

2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V $V_{DD}$ voltage range.
3. Guaranteed by design.
4. $R_L$ is the load connected on the USB OTG FS drivers.

*Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.*

**Figure 47. USB OTG FS timings: definition of data signal rise and fall time**

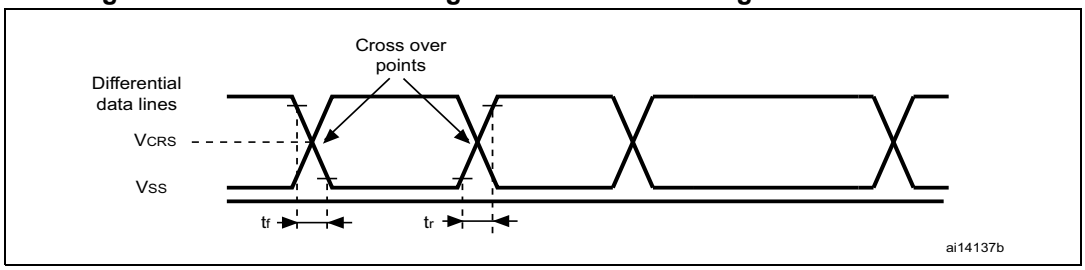



**Table 74. USB OTG FS electrical characteristics(1)**

| Driver characteristics | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

## CAN (controller area network) interface

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

### 6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 75* are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 17*.

**Table 75. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | $V_{DDA} - V_{REF+} < 1.2$ V | 1.7(1) | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | 1.7(1) | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | - | 0 | - | |
| $f_{ADC}$ | ADC clock frequency | $V_{DDA}$ = 1.7(1) to 2.4 V | 0.6 | 15 | 18 | MHz |
| | | $V_{DDA}$ = 2.4 to 3.6 V | 0.6 | 30 | 36 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 30 MHz, 12-bit resolution | - | - | 1764 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2)(4) | Sampling switch resistance | - | - | - | 6 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | 4 | 7 | pF |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.100 | µs |
| | | - | - | - | 3(5) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.067 | µs |
| | | - | - | - | 2(5) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 30 MHz | 0.100 | - | 16 | µs |
| | | - | 3 | - | 480 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | - | - | 2 | 3 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 30 MHz 12-bit resolution | 0.50 | - | 16.40 | µs |
| | | $f_{ADC}$ = 30 MHz 10-bit resolution | 0.43 | - | 16.34 | µs |
| | | $f_{ADC}$ = 30 MHz 8-bit resolution | 0.37 | - | 16.27 | µs |
| | | $f_{ADC}$ = 30 MHz 6-bit resolution | 0.30 | - | 16.20 | µs |
| | | 9 to 492 ($t_S$ for sampling +n-bit resolution for successive approximation) | | | | $1/f_{ADC}$ |

**Table 75. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_S$(2) | Sampling rate ($f_{ADC}$ = 30 MHz, and $t_S$ = 3 ADC cycles) | 12-bit resolution Single ADC | - | - | 2 | Msps |
| $I_{VREF+}$(2) | ADC $V_{REF}$ DC current consumption in conversion mode | - | - | 300 | 500 | µA |
| $I_{VDDA}$(2) | ADC $V_{DDA}$ DC current consumption in conversion mode | - | - | 1.6 | 1.8 | mA |

1. $V_{DDA}$ minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$.
4. $R_{ADC}$ maximum value is given for $V_{DD}$=1.7 V, and minimum value for $V_{DD}$=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 75*.

**Equation 1: $R_{AIN}$ max formula**

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

**Table 76. ADC accuracy at $f_{ADC}$ = 18 MHz(1)**

| Symbol | Parameter | Test conditions | Typ | Max(2) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ =18 MHz<br>$V_{DDA}$ = 1.7 to 3.6 V<br>$V_{REF}$ = 1.7 to 3.6 V<br>$V_{DDA} - V_{REF}$ < 1.2 V | ±3 | ±4 | LSB |
| EO | Offset error | | ±2 | ±3 | |
| EG | Gain error | | ±1 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±2 | ±3 | |

1. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
2. Guaranteed by characterization results.

**Table 77. ADC accuracy at $f_{ADC}$ = 30 MHz(1)**

| Symbol | Parameter | Test conditions | Typ | Max(2) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ = 30 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 2.4 to 3.6 V, $V_{REF}$ = 1.7 to 3.6 V, $V_{DDA}$ –$V_{REF}$ < 1.2 V | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±4 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±1.5 | ±3 | |

1. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
2. Guaranteed by characterization results.

**Table 78. ADC accuracy at $f_{ADC}$ = 36 MHz(1)**

| Symbol | Parameter | Test conditions | Typ | Max(2) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ =36 MHz, $V_{DDA}$ = 2.4 to 3.6 V, $V_{REF}$ = 1.7 to 3.6 V $V_{DDA}$ –$V_{REF}$ < 1.2 V | ±4 | ±7 | LSB |
| EO | Offset error | | ±2 | ±3 | |
| EG | Gain error | | ±3 | ±6 | |
| ED | Differential linearity error | | ±2 | ±3 | |
| EL | Integral linearity error | | ±3 | ±6 | |

1. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
2. Guaranteed by characterization results.

**Table 79. ADC dynamic accuracy at $f_{ADC}$ = 18 MHz - limited test conditions(1)**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ =18 MHz $V_{DDA}$ = $V_{REF+}$= 1.7 V Input Frequency = 20 kHz Temperature = 25 °C | 10.3 | 10.4 | - | bits |
| SINAD | Signal-to-noise and distortion ratio | | 64 | 64.2 | - | dB |
| SNR | Signal-to-noise ratio | | 64 | 65 | - | |
| THD | Total harmonic distortion | | - | -72 | -67 | |

1. Guaranteed by characterization results.

**Table 80. ADC dynamic accuracy at $f_{ADC}$ = 36 MHz - limited test conditions(1)**

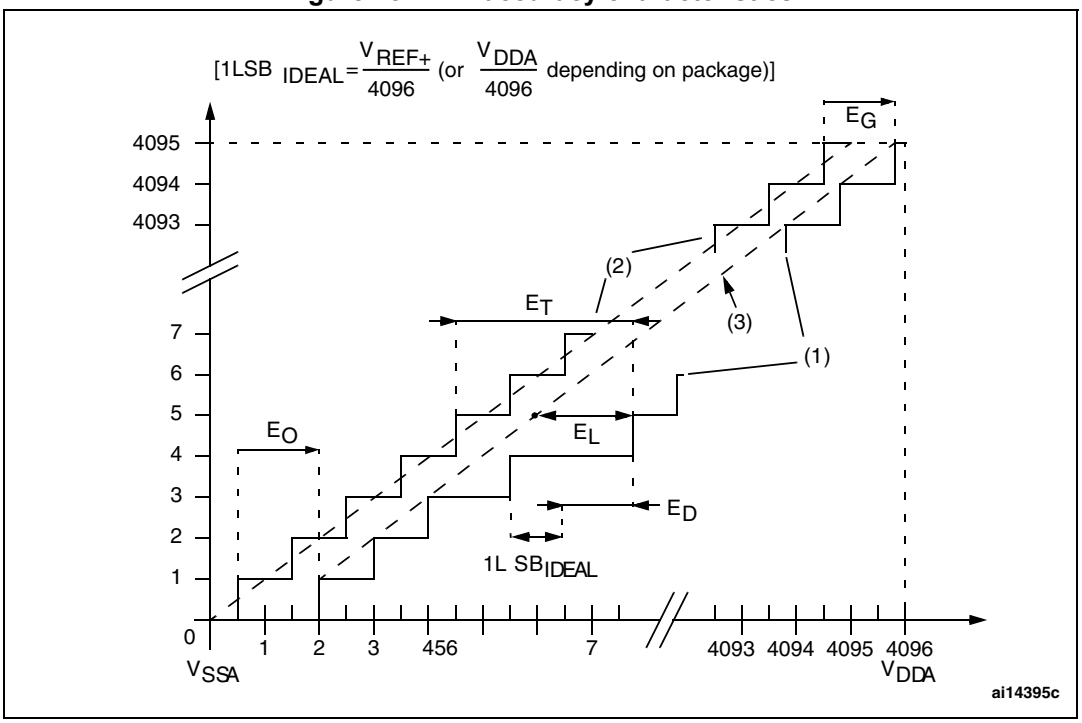
| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ = 36 MHz $V_{DDA}$ = $V_{REF+}$ = 3.3 V Input Frequency = 20 kHz Temperature = 25 °C | 10.6 | 10.8 | - | bits |
| SINAD | Signal-to noise and distortion ratio | | 66 | 67 | - | dB |
| SNR | Signal-to noise ratio | | 64 | 68 | - | |
| THD | Total harmonic distortion | | - | -72 | -70 | |

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

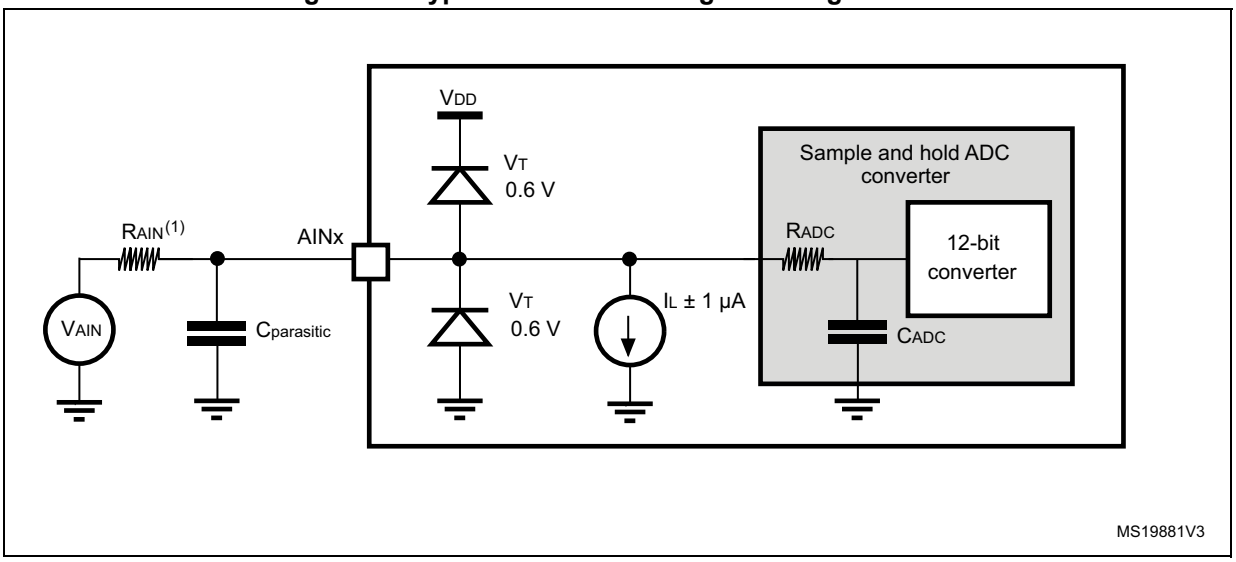
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

**Figure 48. ADC accuracy characteristics**




1. See also *Table 77*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. $E_T$ = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

**Figure 49. Typical connection diagram using the ADC**

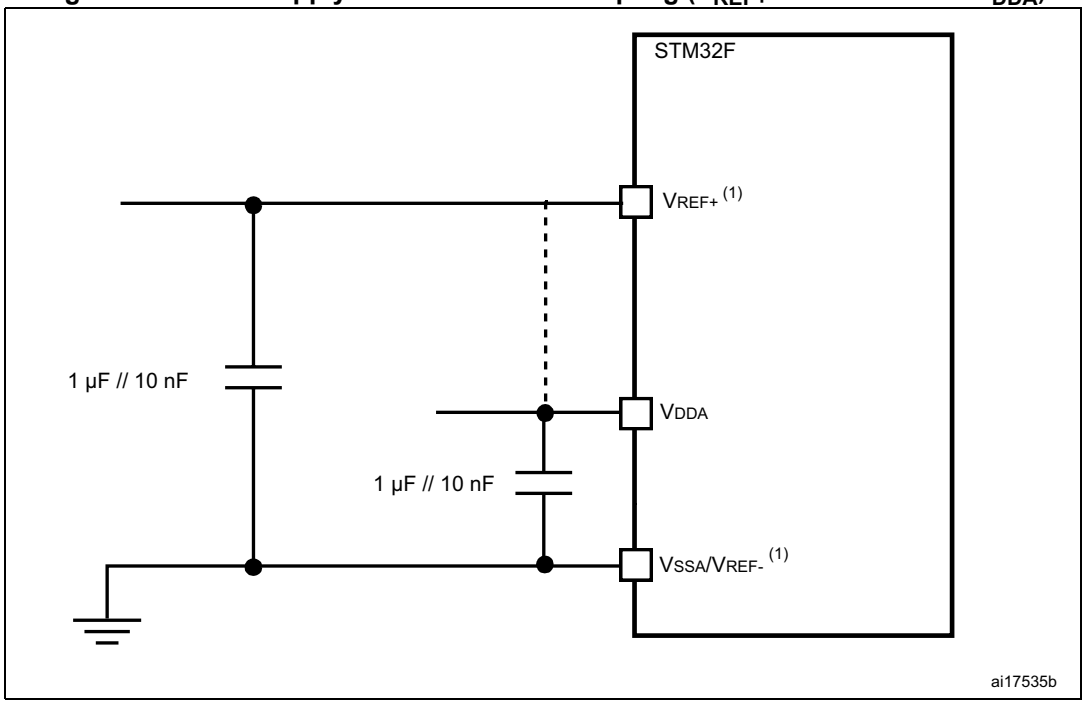



1. Refer to *Table 75* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### General PCB design guidelines

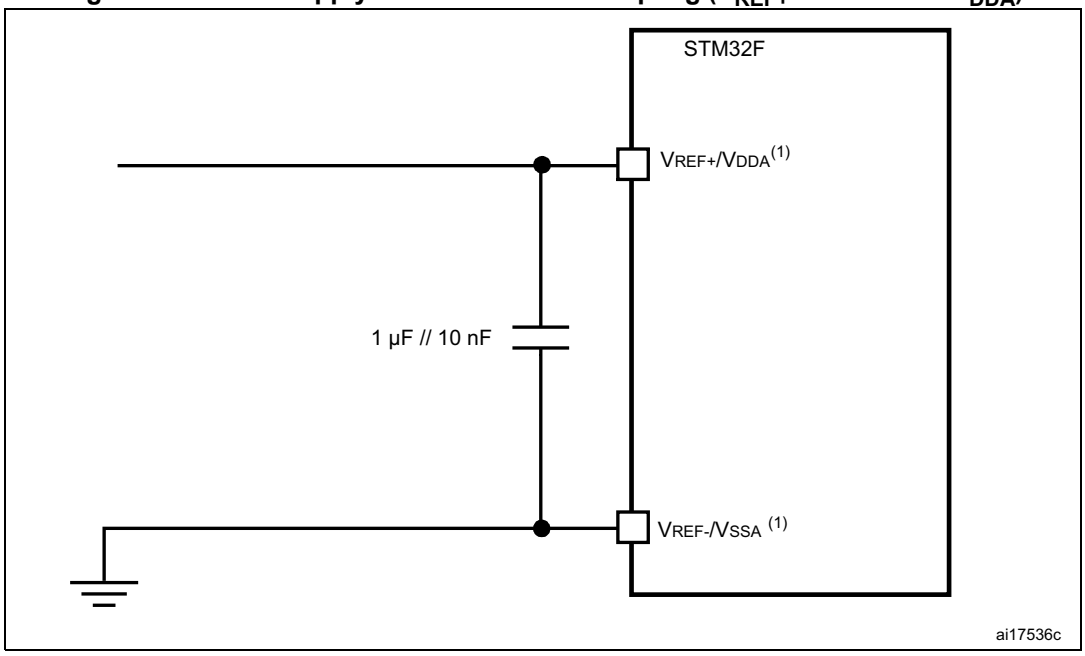
Power supply decoupling should be performed as shown in *Figure 50* or *Figure 51*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 50. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**




1. $V_{REF+}$ and $V_{REF-}$ inputs are both available on UFBGA100. $V_{REF+}$ is also available on LQFP100. When $V_{REF+}$ and $V_{REF-}$ are not available, they are internally connected to $V_{DDA}$ and $V_{SSA}$.

**Figure 51. Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$)**




1. $V_{REF+}$ and $V_{REF-}$ inputs are both available on UFBGA100. $V_{REF+}$ is also available on LQFP100. When $V_{REF+}$ and $V_{REF-}$ are not available, they are internally connected to $V_{DDA}$ and $V_{SSA}$.

## 6.3.21 Temperature sensor characteristics

**Table 81. Temperature sensor characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | - | 2.5 | - | mV/°C |
| $V_{25}$(1) | Voltage at 25 °C | - | 0.76 | - | V |
| $t_{START}$(2) | Startup time | - | 6 | 10 | µs |
| $T_{S_temp}$(2) | ADC sampling time when reading the temperature (1 °C accuracy) | 10 | - | - | µs |

1. Guaranteed by characterization results.
2. Guaranteed by design.

**Table 82. Temperature sensor calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3.3 V | 0x1FFF 7A2C - 0x1FFF 7A2D |
| TS_CAL2 | TS ADC raw data acquired at temperature of 110 °C, $V_{DDA}$= 3.3 V | 0x1FFF 7A2E - 0x1FFF 7A2F |

### 6.3.22 $V_{BAT}$ monitoring characteristics

**Table 83. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 50 | - | KΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 4 | - | |
| Er(1) | Error on Q | –1 | - | +1 | % |
| $T_{S_vbat}$(2)(2) | ADC sampling time when reading the $V_{BAT}$ 1 mV accuracy | 5 | - | - | µs |

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.23 Embedded reference voltage

The parameters given in *Table 84* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 84. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +125 °C | 1.18 | 1.21 | 1.24 | V |
| $T_{S_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | - | 10 | - | - | µs |
| $V_{RERINT_s}$(2) | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3V ± 10mV | - | 3 | 5 | mV |
| $T_{Coeff}$(2) | Temperature coefficient | - | - | 30 | 50 | ppm/°C |
| $t_{START}$(2) | Startup time | - | - | 6 | 10 | µs |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design

**Table 85. Internal reference voltage calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| $V_{REFIN_CAL}$ | Raw data acquired at temperature of 30 °C $V_{DDA}$ = 3.3 V | 0x1FFF 7A2A - 0x1FFF 7A2B |

### 6.3.24 DAC electrical characteristics

**Table 86. DAC characteristics**

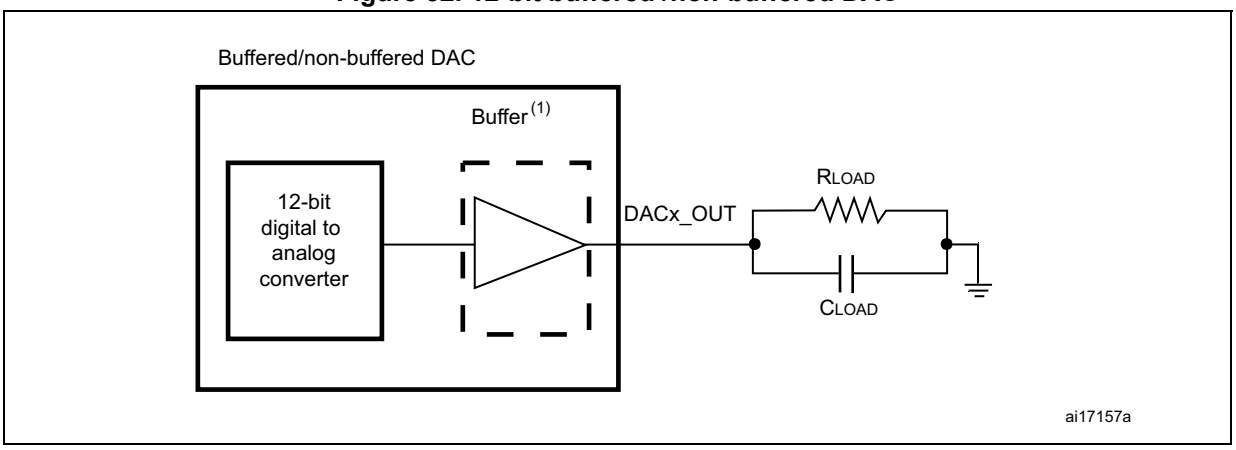
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.7(1) | - | 3.6 | V | |
| $V_{REF+}$ | Reference supply voltage | - | | 1.7(1) | - | 3.6 | V | $V_{REF+} \leq V_{DDA}$ |
| $V_{SSA}$ | Ground | - | | 0 | - | 0 | V | - |
| $R_{LOAD}$(2) | Resistive load | DAC output buffer ON | $R_{LOAD}$ connected to $V_{SSA}$ | 5 | - | - | kΩ | - |
| | | | $R_{LOAD}$ connected to $V_{DDA}$ | 25 | - | - | kΩ | - |
| $R_O$(2) | Impedance output with buffer OFF | - | | - | - | 15 | kΩ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 MΩ |
| $C_{LOAD}$(2) | Capacitive load | - | | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer ON | - | | 0.2 | - | - | V | It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+}$ = 3.6 V and (0x1C7) to (0xE38) at $V_{REF+}$ = 1.7 V |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer ON | - | | - | - | $V_{DDA}$ – 0.2 | V | |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer OFF | - | | - | 0.5 | - | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer OFF | - | | - | - | $V_{REF+}$ – 1LSB | V | |
| $I_{VREF+}$(4) | DAC DC $V_{REF}$ current consumption in quiescent mode (Standby mode) | - | | - | 170 | 240 | µA | With no load, worst code (0x800) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| | | - | | - | 50 | 75 | | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| $I_{DDA}$(4) | DAC DC VDDA current consumption in quiescent mode(3) | - | | - | 280 | 380 | µA | With no load, middle code (0x800) on the inputs |
| | | - | | - | 475 | 625 | µA | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |

**Table 86. DAC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|---|
| DNL(4) | Differential non linearity Difference between two consecutive code-1LSB) | - | - | - | ±0.5 | LSB | Given for the DAC in 10-bit configuration. |
| | | - | - | - | ±2 | LSB | Given for the DAC in 12-bit configuration. |
| INL(4) | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | - | - | - | ±1 | LSB | Given for the DAC in 10-bit configuration. |
| | | - | - | - | ±4 | LSB | Given for the DAC in 12-bit configuration. |
| Offset(4) | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$) | - | - | - | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | - | - | - | ±3 | LSB | Given for the DAC in 10-bit at $V_{REF+}$ = 3.6 V |
| | | - | - | - | ±12 | LSB | Given for the DAC in 12-bit at $V_{REF+}$ = 3.6 V |
| Gain error(4) | Gain error | - | - | - | ±0.5 | % | Given for the DAC in 12-bit configuration |
| $t_{SETTLING}$(4) | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB | - | - | 3 | 6 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| THD(4) | Total Harmonic Distortion Buffer ON | - | - | - | - | dB | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| Update rate(2) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | - | 1 | MS/s | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| $t_{WAKEUP}$(4) | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | - | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. |
| PSRR+ (2) | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement) | - | - | –67 | –40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. $V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

**Figure 52. 12-bit buffered /non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

### 6.3.25 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 87* for DFSDM are derived from tests performed under the ambient temperature, $f_{APB2}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 * $V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

**Table 87. DFSDM characteristics(1)**

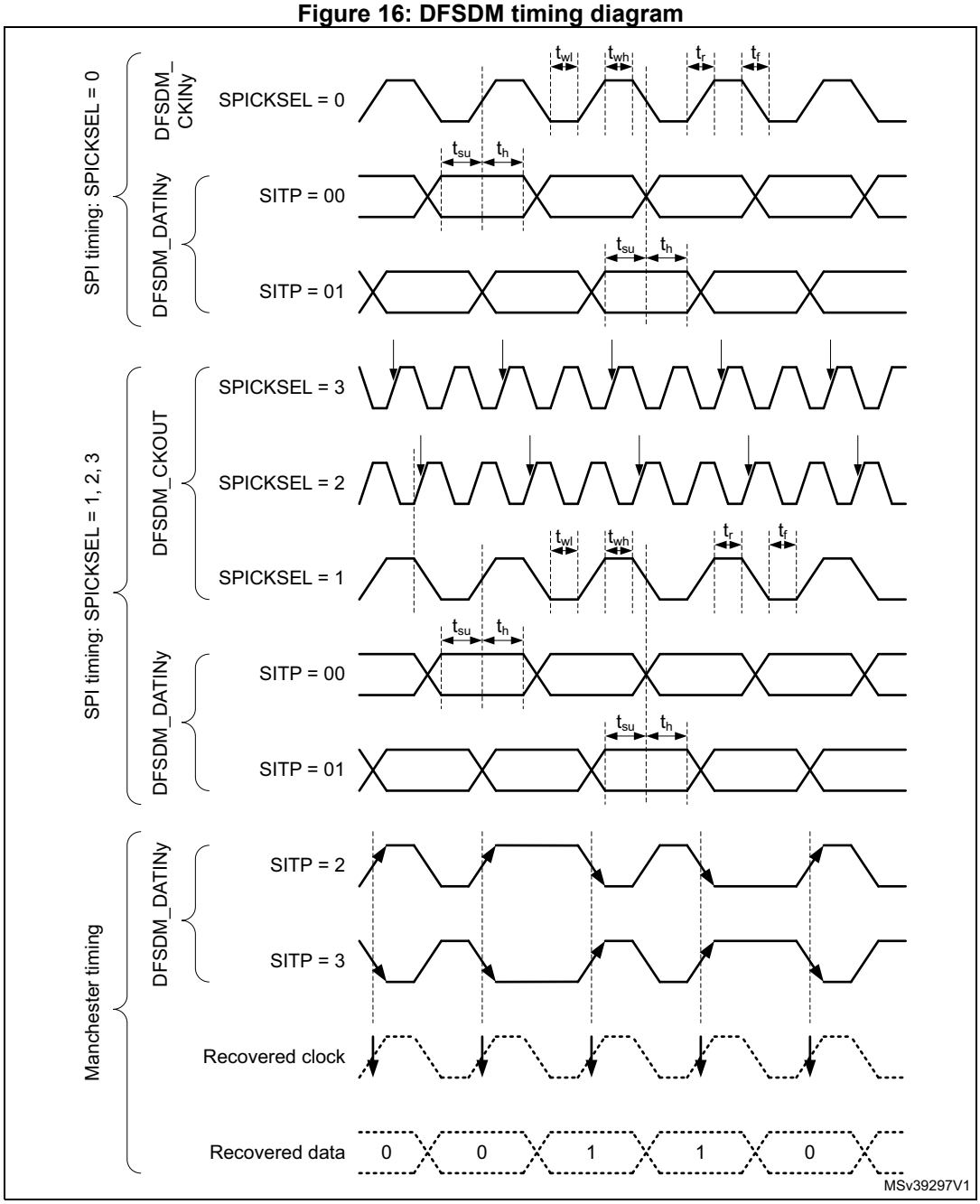
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{DFSDMCLK}$ | DFSDM clock | 1.71 < $V_{DD}$ < 3.6 V | - | - | $f_{SYSCLK}$ | MHz |
| $f_{CKIN}$ ($1/T_{CKIN}$) | Input clock frequency | SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0, 1.71 < $V_{DD}$ < 3.6 V | - | - | 20 ($f_{DFBDMCLK}$ / 4 | |
| | | SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0, 2.7 < $V_{DD}$ < 3.6 V | - | - | 20 ($f_{DFBDMCLK}$ / 4 | |
| | | SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] ≠ 0, 1.71 < $V_{DD}$ < 3.6 V | - | - | 20 ($f_{DFBDMCLK}$ / 4 | |
| | | SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] ≠ 0, 2.7 < $V_{DD}$ < 3.6 V | - | - | 20 ($f_{DFBDMCLK}$ / 4 | |
| $f_{CKOUT}$ | Output clock frequency | 1.71 < $V_{DD}$ < 3.6 V | - | - | 20 | |
| $DuCy_{CKOUT}$ | Output clock frequency duty cycle | 1.71 < $V_{DD}$ < 3.6 V | 45 | 50 | 55 | % |

**Table 87. DFSDM characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{wh(CKIN)}$ $t_{wl(CKIN)}$ | Input clock high and low time | SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0) 1.71 < $V_{DD}$ < 3.6 V | $t_{CKIN}$ / 2 - 0.5 | $t_{CKIN}$ / 2 | - | ns |
| $t_{su}$ | Data input setup time | SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0) 1.71 < $V_{DD}$ < 3.6 V | 3.5 | - | - | |
| $t_h$ | Data input hold time | SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0) 1.71 < $V_{DD}$ < 3.6 V | 2.5 | - | - | |
| $T_{Manchester}$ | Manchester data period (recovered clock period) | Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0) 1.71 < $V_{DD}$ < 3.6 V | (CKOUTDIV + 1) * $t_{DFBDMCLK}$ | - | (2 * CKOUTDIV ) * $t_{DFBDMCLK}$ | |

1. Data based on characterization results.

**Figure 16: DFSDM timing diagram**



## 6.3.26 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 88* to *Table 95* for the FSMC interface are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitance load C = 30 pF
- Measurement points are done at CMOS levels: $0.5.V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

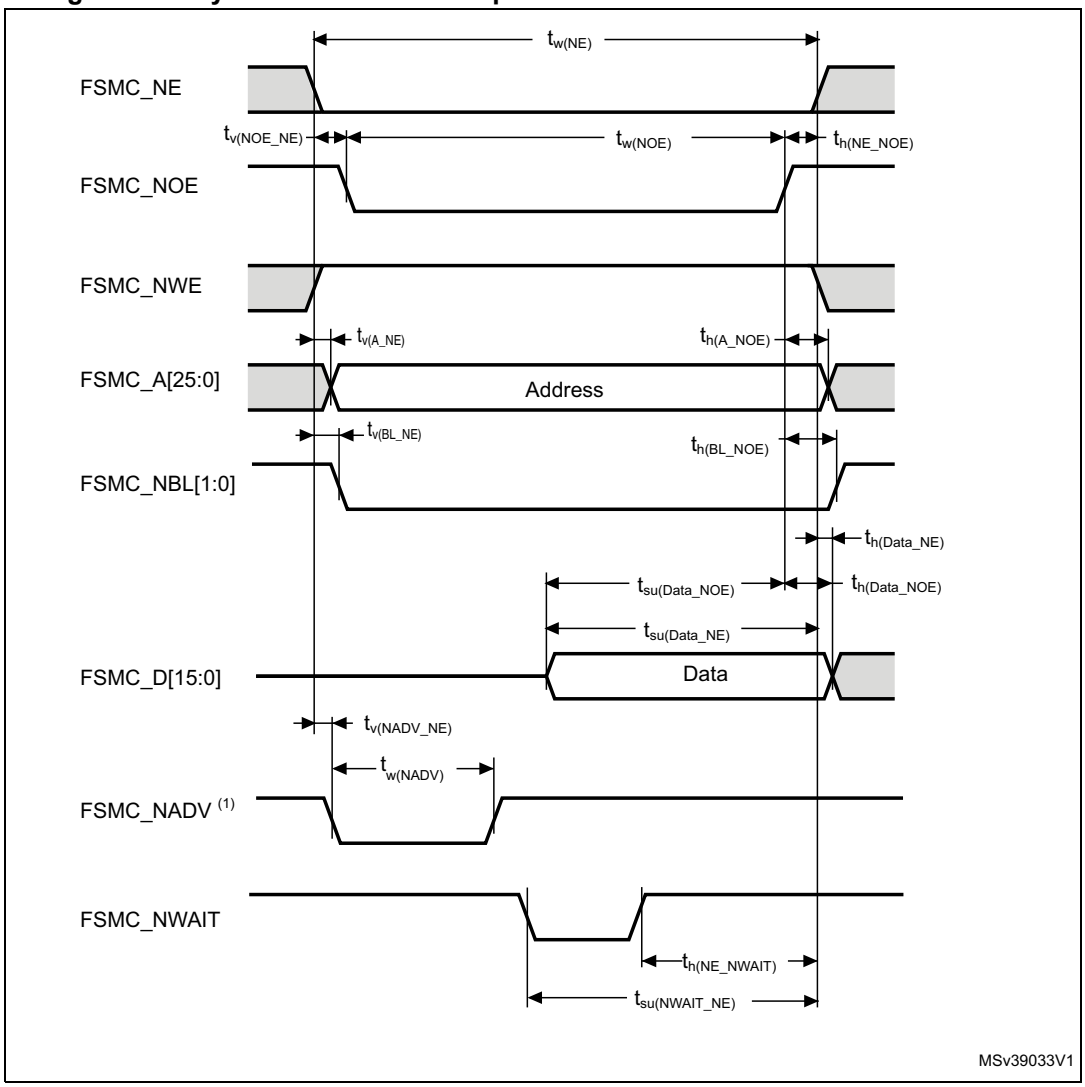
### Asynchronous waveforms and timings

*Figure 53* through *Figure 56* represent asynchronous waveforms and *Table 88* through *Table 95* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the $T_{HCLK}$ is the HCLK clock period.

**Figure 53. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**




1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

**Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $2 * t_{HCLK} - 1$ | $2 * t_{HCLK} + 1$ | ns |
| $t_{v(NOE_NE)}$ | FSMC_NEx low to FSMC_NOE low | 0 | 0.5 | |
| $t_{w(NOE)}$ | FSMC_NOE low time | $2 * t_{HCLK} - 1$ | $2 * t_{HCLK} + 1$ | |
| $t_{h(NE_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | 0 | - | |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0.5 | |
| $t_{h(A_NOE)}$ | Address hold time after FSMC_NOE high | 0 | - | |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | |
| $t_{h(BL_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | 0 | - | |
| $t_{su(Data_NE)}$ | Data to FSMC_NEx high setup time | $t_{HCLK} - 2$ | - | |
| $t_{su(Data_NOE)}$ | Data to FSMC_NOEx high setup time | $t_{HCLK} - 2$ | - | |
| $t_{h(Data_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | |
| $t_{h(Data_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FSMC_NADV low time | - | $t_{HCLK} + 1$ | |

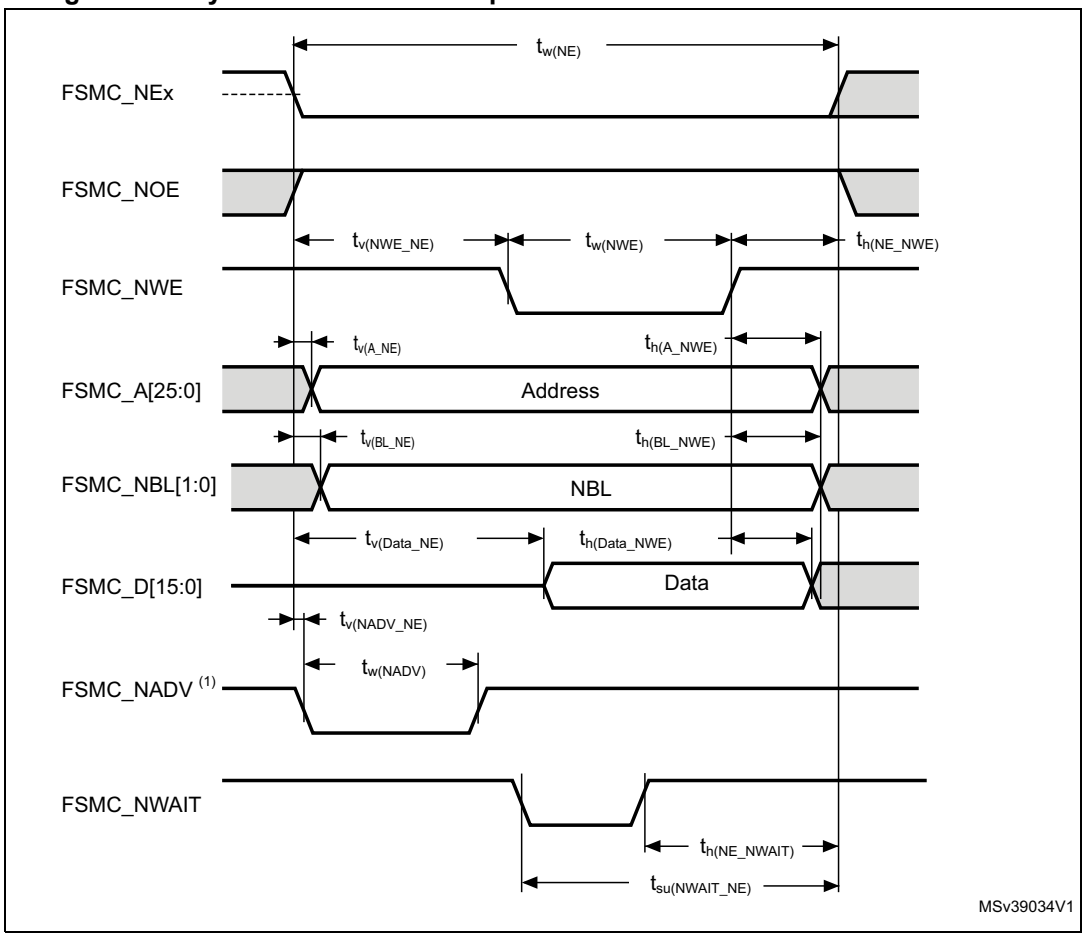
1. $C_L$ = 30 pF.
2. Based on characterization.

**Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $7 * t_{HCLK} + 1$ | $7 * t_{HCLK} + 1$ | ns |
| $t_{w(NOE)}$ | FSMC_NWE low time | $5 * t_{HCLK} - 1$ | $5 * t_{HCLK} + 1$ | |
| $t_{w(NWAIT)}$ | FSMC_NWAIT low time | $t_{HCLK} - 0.5$ | - | |
| $t_{su(NWAIT_NE)}$ | FSMC_NWAIT valid before FSMC_NEx high | $5 * t_{HCLK} + 1.5$ | - | |
| $t_{h(NE_NWAIT)}$ | FSMC_NEx hold time after FSMC_NWAIT invalid | $4 * t_{HCLK} + 1$ | - | |

1. $C_L$ = 30 pF.
2. Based on characterization.

**Figure 54. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**




1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

**Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | 3 * $t_{Hclk}$ - 1 | 3 * $t_{Hclk}$ - 1 | ns |
| $t_{v(NWE_NE)}$ | FSMC_NEx low to FSMC_NWE low | $t_{HCLK}$ - 1 | $t_{HCLK}$ + 0.5 | |
| $t_{w(NWE)}$ | FSMC_NWE low time | $t_{HCLK}$ - 1.5 | $t_{HCLK}$ + 0.5 | |
| $t_{h(NE_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $t_{HCLK}$ | - | |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | |
| $t_{h(A_NWE)}$ | Address hold time after FSMC_NWE high | $t_{HCLK}$ - 0.5 | - | |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | |
| $t_{h(BL_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $t_{HCLK}$ - 0.5 | - | |
| $t_{v(Data_NE)}$ | Data to FSMC_NEx low to Data valid | - | $t_{HCLK}$ + 2.5 | |
| $t_{h(Data_NWE)}$ | Data hold time after FSMC_NWE high | $t_{HCLK}$ | - | |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FSMC_NADV low time | - | $t_{HCLK}$ + 1 | |

1. $C_L$ = 30 pF.
2. Based on characterization.

**Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | 8 * $t_{HCLK}$ - 1 | 8 * $t_{HCLK}$ + 1 | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | 6 * $t_{HCLK}$ - 1.5 | 6 * $t_{HCLK}$ + 0.5 | |
| $t_{su(NWAIT_NE)}$ | FSMC_NWAIT valid before FSMC_NEx high | 6 * $t_{HCLK}$ - 1 | - | |
| $t_{h(NE_NWAIT)}$ | FSMC_NEx hold time after FSMC_NWAIT invalid | 4 * $t_{HCLK}$ + 2 | - | |

1. $C_L$ = 30 pF.
2. Based on characterization.

**Figure 55. Asynchronous multiplexed PSRAM/NOR read waveforms**

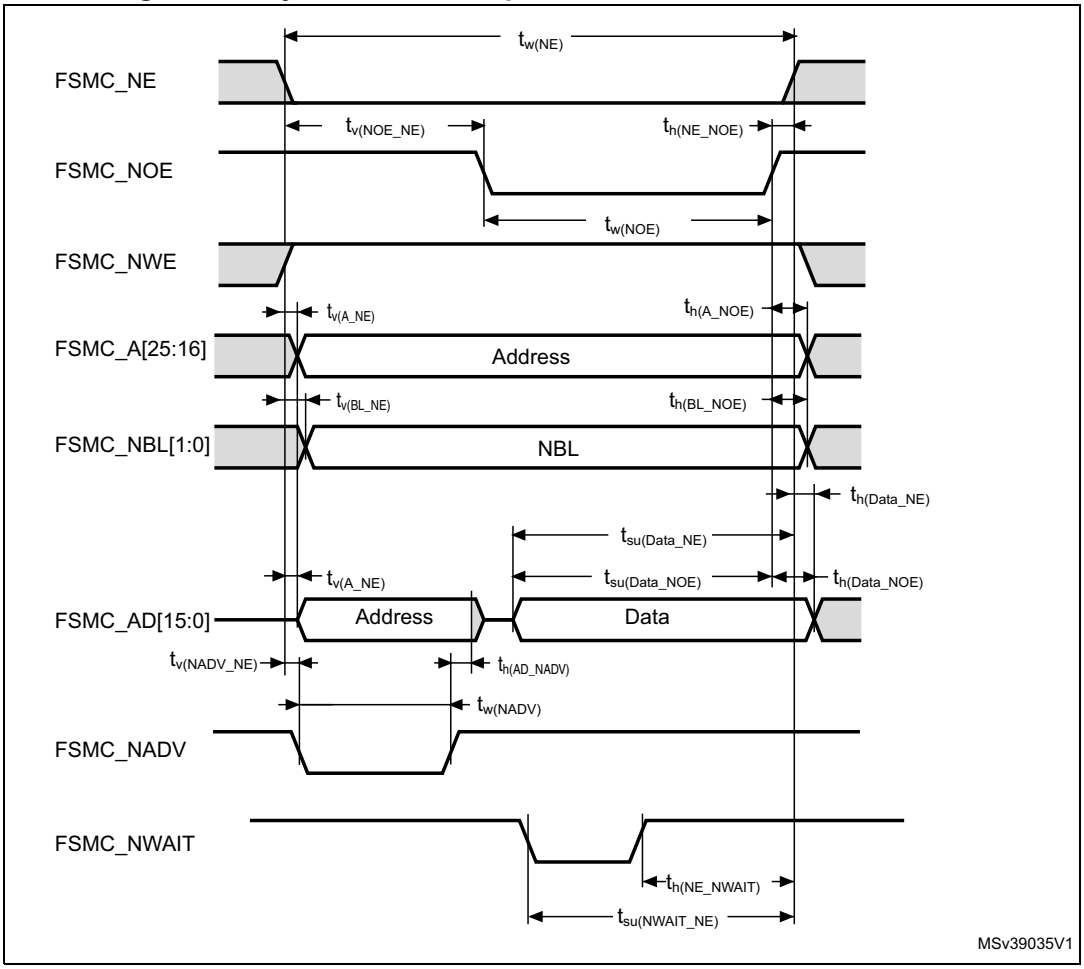


**Table 92. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $3 * t_{HCLK} - 1$ | $3 * t_{HCLK} + 1$ | ns |
| $t_{v(NOE_NE)}$ | FSMC_NEx low to FSMC_NOE low | $2 * t_{HCLK}$ | $2 * t_{HCLK} + 0.5$ | |
| $t_{w(NOE)}$ | FSMC_NOE low time | $t_{HCLK} - 1$ | $t_{HCLK} + 1$ | |
| $t_{h(NE_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | 0 | - | |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0.5 | |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | 0 | 0.5 | |
| $t_{w(NADV)}$ | FSMC_NADV low time | $t_{HCLK} - 0.5$ | $t_{HCLK} + 1$ | |
| $t_{h(AD_NADV)}$ | FSMC_AD(address) valid hold time after FSMC_NADV high) | $t_{HCLK} + 0.5$ | - | |
| $t_{h(A_NOE)}$ | Address hold time after FSMC_NOE high | $t_{HCLK} - 0.5$ | - | |
| $t_{h(BL_NOE)}$ | FSMC_BL time after FSMC_NOE high | 0 | - | |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | |
| $t_{su(Data_NE)}$ | Data to FSMC_NEx high setup time | $t_{HCLK} - 2$ | - | |
| $t_{su(Data_NOE)}$ | Data to FSMC_NOE high setup time | $t_{HCLK} - 2$ | - | |
| $t_{h(Data_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | |
| $t_{h(Data_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | |

1. $C_L$ = 30 pF.
2. Based on characterization.

**Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $8 * t_{HCLK} - 1$ | $8 * t_{HCLK} + 1$ | ns |
| $t_{w(NOE)}$ | FSMC_NWE low time | $5 * t_{HCLK} - 1.5$ | $5 * t_{HCLK} + 0.5$ | |
| $t_{su(NWAIT_NE)}$ | FSMC_NWAIT valid before FSMC_NEx high | $5 * t_{HCLK} + 1.5$ | - | |
| $t_{h(NE_NWAIT)}$ | FSMC_NEx hold time after FSMC_NWAIT invalid | $4 * t_{HCLK} + 1$ | - | |

1. $C_L$ = 30 pF.
2. Based on characterization.

**Figure 56. Asynchronous multiplexed PSRAM/NOR write waveforms**

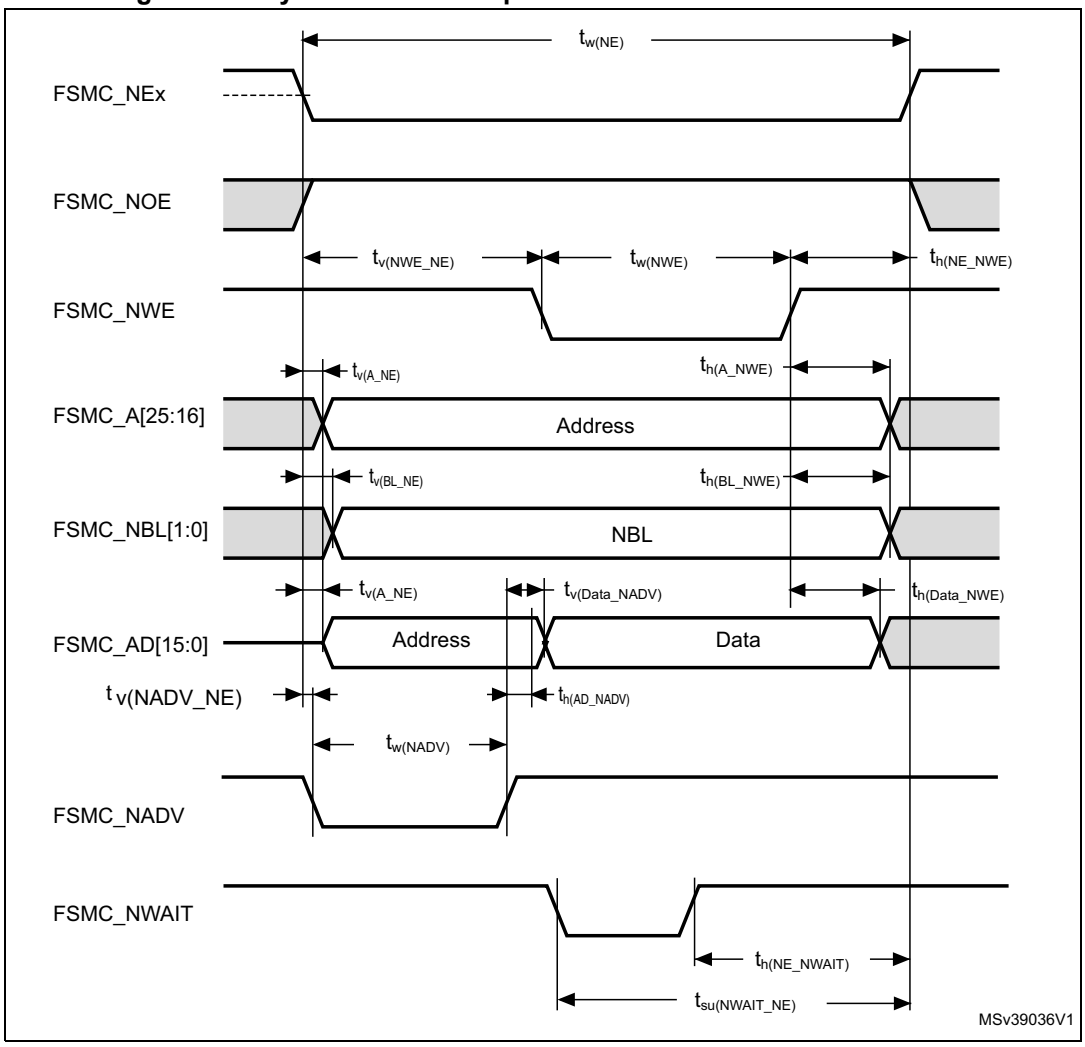


**Table 94. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $4 * T_{HCLK} - 1$ | $4 * T_{HCLK} + 1$ | ns |
| $t_{v(NWE_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK} - 1$ | $T_{HCLK} + 0.5$ | |
| $t_{w(NWE)}$ | FSMC_NWE low time | $2 * T_{HCLK} - 0.5$ | $2 * T_{HCLK} - 0.5$ | |
| $t_{h(NE_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $T_{HCLK} - 0.5$ | - | |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | 0 | 0.5 | |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK}$ | $T_{HCLK} + 1$ | |
| $t_{h(AD_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high) | $T_{HCLK} + 0.5$ | - | |
| $t_{h(A_NWE)}$ | Address hold time after FSMC_NWE high | $T_{HCLK} + 0.5$ | - | |
| $t_{h(BL_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $T_{HCLK} - 0.5$ | - | |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | |
| $t_{v(Data_NADV)}$ | FSMC_NADV high to Data valid | - | $T_{HCLK} + 2.5$ | |
| $t_{h(Data_NWE)}$ | Data hold time after FSMC_NWE high | $T_{HCLK}$ | - | |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

**Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $9 * T_{HCLK} - 1$ | $9 * T_{HCLK} + 1$ | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | $7 * T_{HCLK} - 0.5$ | $7 * T_{HCLK} + 0.5$ | |
| $t_{su(NWAIT_NE)}$ | FSMC_NWAIT valid before FSMC_NEx high | $6 * T_{HCLK} + 2$ | - | |
| $t_{h(NE_NWAIT)}$ | FSMC_NEx hold time after FSMC_NWAIT invalid | $4 * T_{HCLK} - 1$ | - | |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

### Synchronous waveforms and timings

*Figure 57* through *Figure 60* represent synchronous waveforms and *Table 96* through *Table 99* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F446 reference manual: RM0390)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the $T_{HCLK}$ is the HCLK clock period (with maximum FSMC_CLK = 90 MHz).

**Figure 57. Synchronous multiplexed NOR/PSRAM read timings**

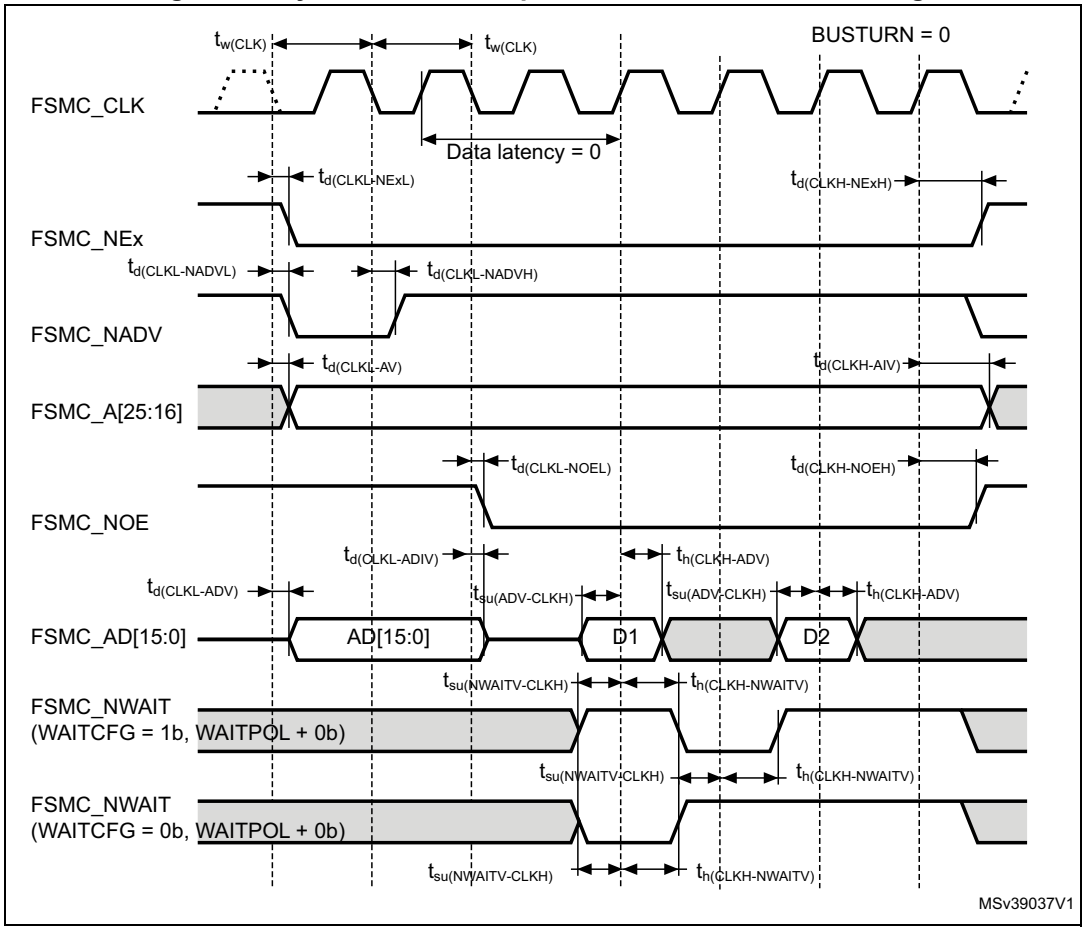


**Table 96. Synchronous multiplexed NOR/PSRAM read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | 2 * $T_{HCLK}$ - 0.5 | - | ns |
| $t_{d(CLKL-NExL)}$ | FSMC_CLK low to FSMC_NEx low (x=0..2) | - | 2 | |
| $t_{d(CLKH_NExH)}$ | FSMC_CLK high to FSMC_NEx high (x= 0…2) | $T_{HCLK}$ + 0.5 | - | |
| $t_{d(CLKL-NADVL)}$ | FSMC_CLK low to FSMC_NADV low | - | 1 | |
| $t_{d(CLKL-NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FSMC_CLK low to FSMC_Ax valid (x=16…25) | - | 2.5 | |
| $t_{d(CLKH-AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x=16…25) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NOEL)}$ | FSMC_CLK low to FSMC_NOE low | - | 1.5 | |
| $t_{d(CLKH-NOEH)}$ | FSMC_CLK high to FSMC_NOE high | $T_{HCLK}$ - 0.5 | - | |
| $t_{d(CLKL-ADV)}$ | FSMC_CLK low to FSMC_AD[15:0] valid | - | 3 | |
| $t_{d(CLKL-ADIV)}$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 0 | - | |
| $t_{su(ADV-CLKH)}$ | FSMC_A/D[15:0] valid data before FSMC_CLK high | 1.5 | - | |
| $t_{h(CLKH-ADV)}$ | FSMC_A/D[15:0] valid data after FSMC_CLK high | 3.5 | - | |
| $t_{su(NWAIT-CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | 2.5 | - | |
| $t_{h(CLKH-NWAIT)}$ | FSMC_NWAIT valid after FSMC_CLK high | 3.5 | - | |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

**Figure 58. Synchronous multiplexed PSRAM write timings**

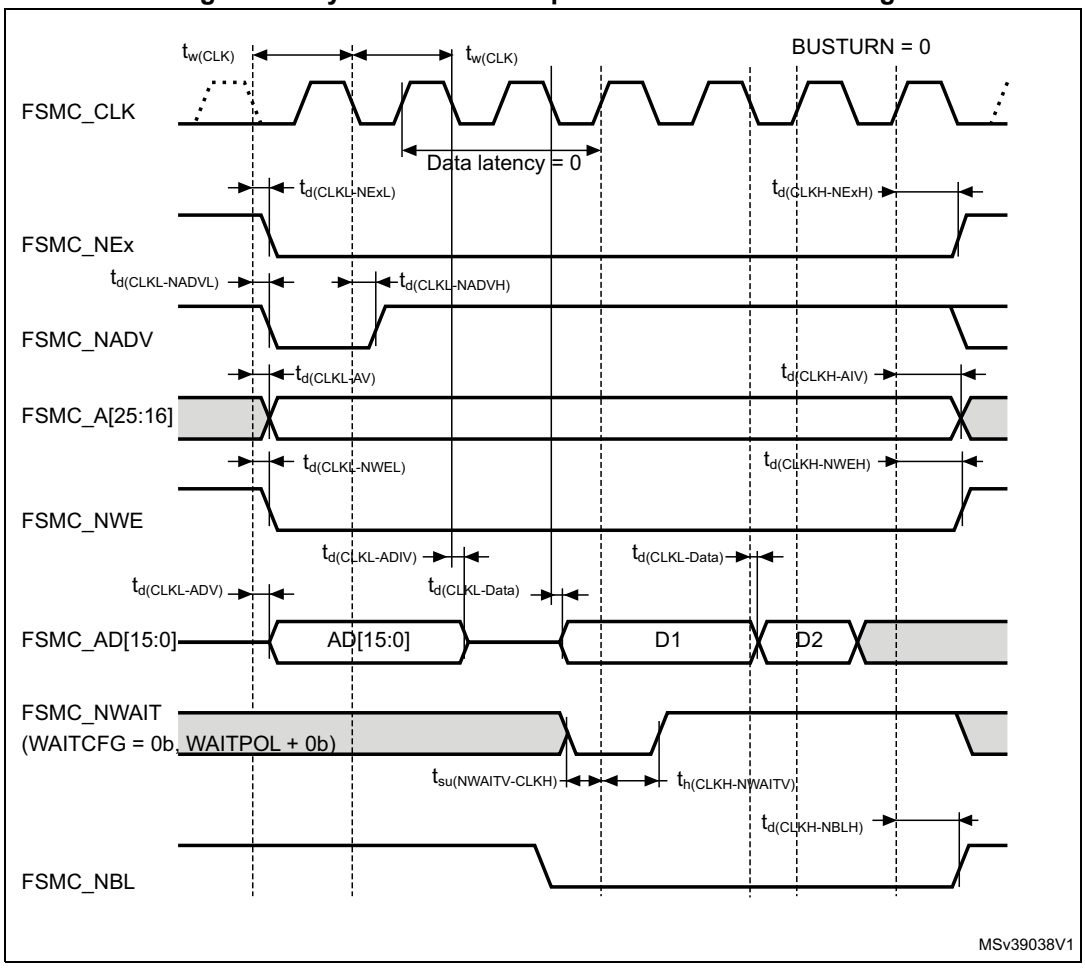


**Table 97. Synchronous multiplexed PSRAM write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period, $V_{DD}$ range= 2.7 to 3.6 V | 2 * $T_{HCLK}$ - 0.5 | - | ns |
| $t_{d(CLKL-NExL)}$ | FSMC_CLK low to FSMC_NEx low (x= 0...2) | - | 2 | |
| $t_{d(CLKH-NExH)}$ | FSMC_CLK high to FSMC_NEx high (x= 0…2) | $T_{HCLK}$ + 0.5 | - | |
| $t_{d(CLKL-NADVL)}$ | FSMC_CLK low to FSMC_NADV low | - | 1 | |
| $t_{d(CLKL-NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FSMC_CLK low to FSMC_Ax valid (x=16…25) | - | 2.5 | |
| $t_{d(CLKH-AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x=16…25) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NWEL)}$ | FSMC_CLK low to FSMC_NWE low | - | 1.5 | |
| $t_{(CLKH-NWEH)}$ | FSMC_CLK high to FSMC_NWE high | $T_{HCLK}$ + 0.5 | - | |
| $t_{d(CLKL-ADV)}$ | FSMC_CLK low to FSMC_AD[15:0] valid | - | 3 | |
| $t_{d(CLKL-ADIV)}$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 0 | - | |
| $t_{d(CLKL-DATA)}$ | FSMC_A/D[15:0] valid data after FSMC_CLK low | - | 4 | |
| $t_{d(CLKL-NBLL)}$ | FSMC_CLK low to FSMC_NBL low | 0 | 2 | |
| $t_{d(CLKH-NBLH)}$ | FSMC_CLK high to FSMC_NBL high | $T_{HCLK}$ + 0.5 | - | |
| $t_{su(NWAIT-CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FSMC_NWAIT valid after FSMC_CLK high | 3.5 | - | |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

**Figure 59. Synchronous non-multiplexed NOR/PSRAM read timings**

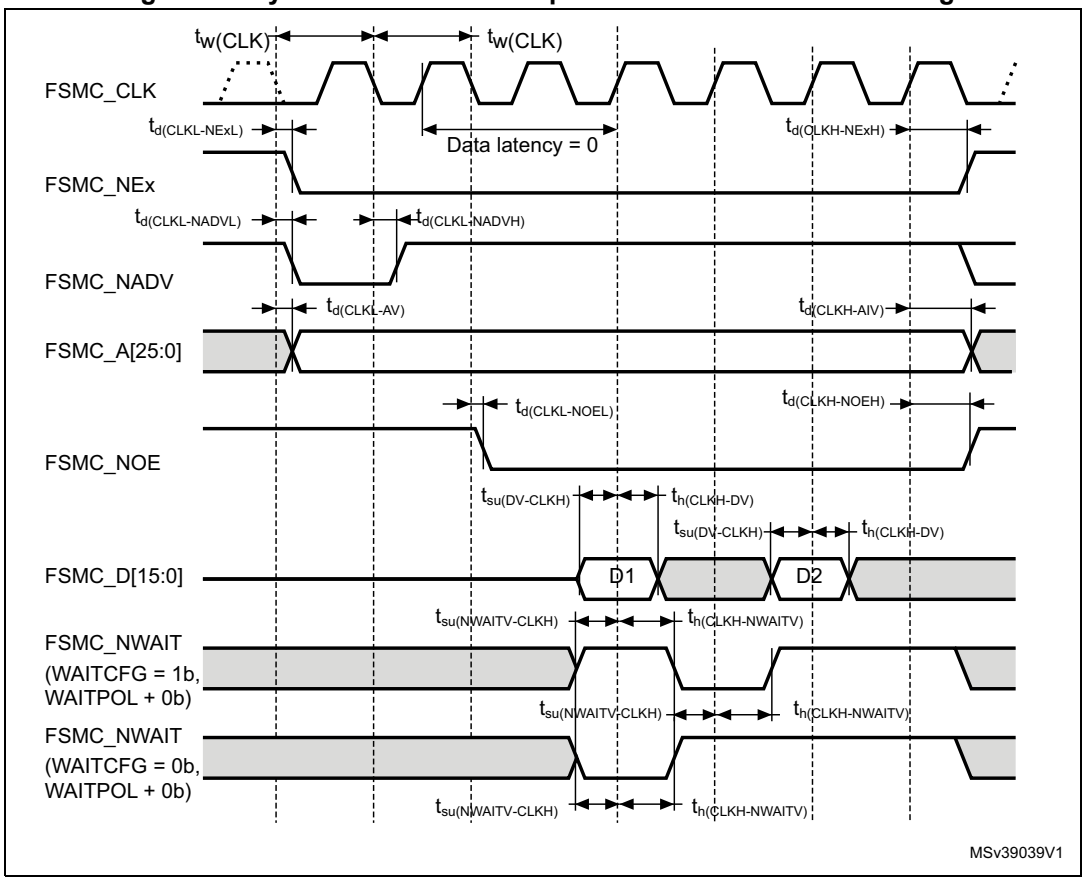



**Table 98. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | $2T_{HCLK} - 0.5$ | - | ns |
| $t_{(CLKL-NExL)}$ | FSMC_CLK low to FSMC_NEx low (x=0..2) | - | 2 | |
| $t_{d(CLKH-NExH)}$ | FSMC_CLK high to FSMC_NEx high (x= 0…2) | $T_{HCLK}$ +0.5 | - | |
| $t_{d(CLKL-NADVL)}$ | FSMC_CLK low to FSMC_NADV low | - | 0.5 | |
| $t_{d(CLKL-NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FSMC_CLK low to FSMC_Ax valid (x=16…25) | - | 2.5 | |
| $t_{d(CLKH-AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x=16…25) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NOEL)}$ | FSMC_CLK low to FSMC_NOE low | - | 1.5 | |
| $t_{d(CLKH-NOEH)}$ | FSMC_CLK high to FSMC_NOE high | $T_{HCLK}$ - 0.5 | - | |
| $t_{su(DV-CLKH)}$ | FSMC_D[15:0] valid data before FSMC_CLK high | 1.5 | - | |
| $t_{h(CLKH-DV)}$ | FSMC_D[15:0] valid data after FSMC_CLK high | 3.5 | - | |
| $t_{su(NWAIT-CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | 2.5 | - | |
| $t_{h(CLKH-NWAIT)}$ | FSMC_NWAIT valid after FSMC_CLK high | 3.5 | - | |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

**Figure 60. Synchronous non-multiplexed PSRAM write timings**

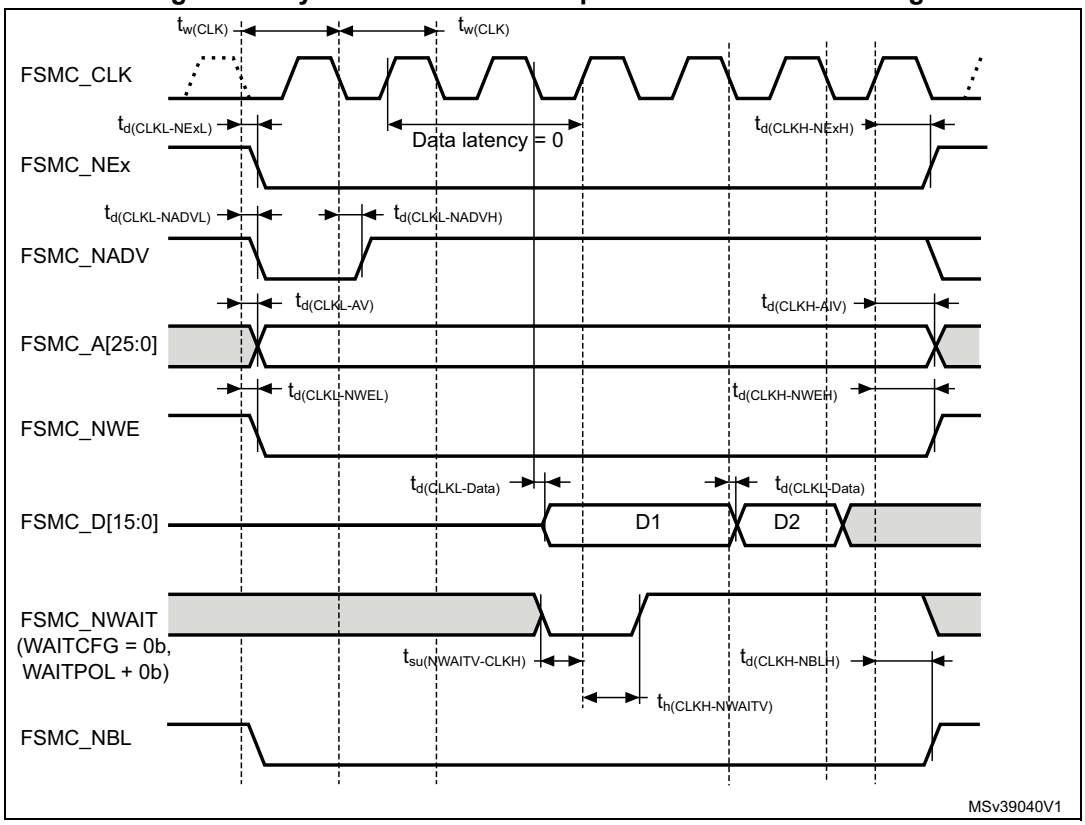



**Table 99. Synchronous non-multiplexed PSRAM write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | 2 * $T_{HCLK}$ - 0.5 | - | ns |
| $t_{d(CLKL-NExL)}$ | FSMC_CLK low to FSMC_NEx low (x=0..2) | - | 2 | |
| $t_{d(CLKH-NExH)}$ | FSMC_CLK high to FSMC_NEx high (x= 0…2) | $T_{HCLK}$ + 0.5 | - | |
| $t_{d(CLKL-NADVL)}$ | FSMC_CLK low to FSMC_NADV low | - | 0.5 | |
| $t_{d(CLKL-NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FSMC_CLK low to FSMC_Ax valid (x=16…25) | - | 2.5 | |
| $t_{d(CLKH-AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x=16…25) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NWEL)}$ | FSMC_CLK low to FSMC_NWE low | - | 1.5 | |
| $t_{d(CLKH-NWEH)}$ | FSMC_CLK high to FSMC_NWE high | $T_{HCLK}$ + 1 | - | |
| $t_{d(CLKL-Data)}$ | FSMC_D[15:0] valid data after FSMC_CLK low | - | 4 | |
| $t_{d(CLKL-NBLL)}$ | FSMC_CLK low to FSMC_NBL low | - | 2 | |
| $t_{d(CLKH-NBLH)}$ | FSMC_CLK high to FSMC_NBL high | $T_{HCLK}$ + 1 | - | |
| $t_{su(NWAIT-CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FSMC_NWAIT valid after FSMC_CLK high | 3.5 | - | |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

### 6.3.27 SD/SDIO MMC/eMMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 100* for the SDIO are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

**Figure 61. SDIO high-speed mode**

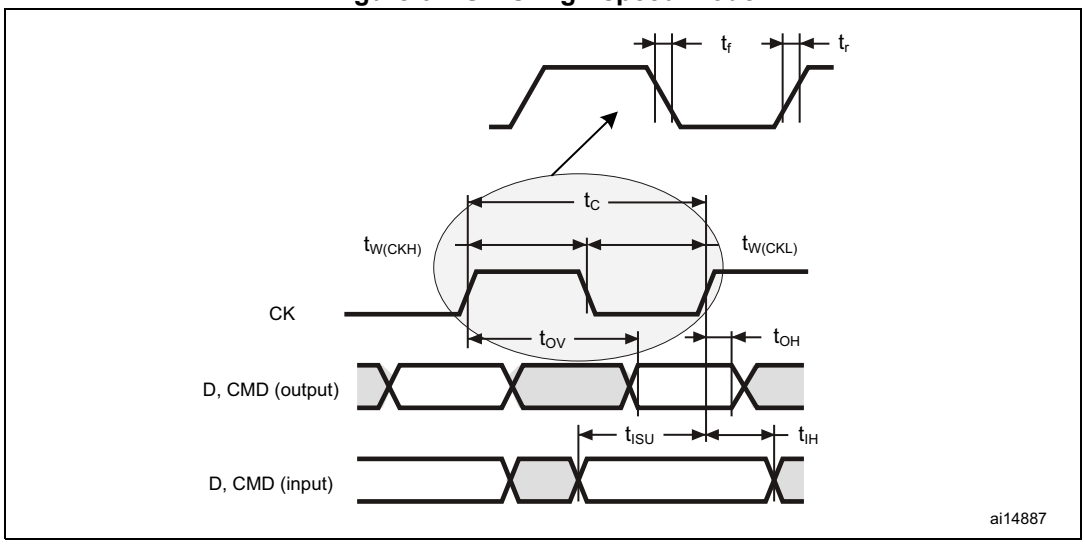



**Figure 62. SD default mode**

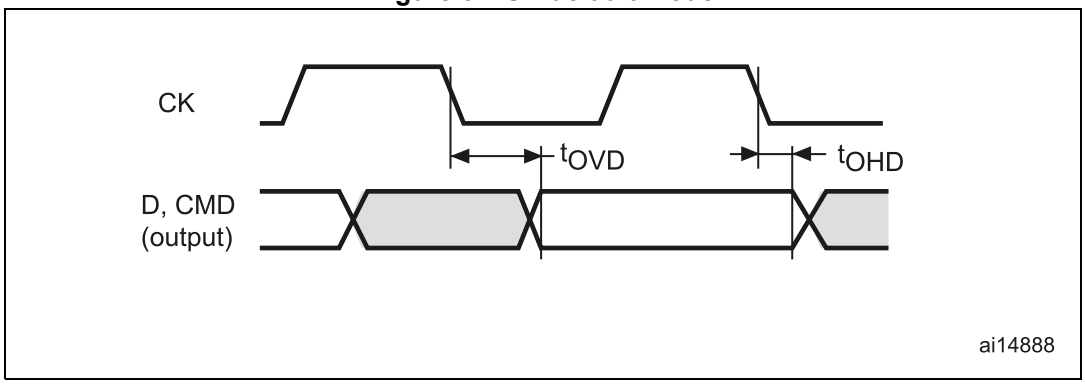


**Table 100. SD / MMC characteristics(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PP}$ | Clock frequency in data transfer mode | - | 0 | - | 50 | MHz |
| - | SDIO_CK/fPCLK2 frequency ratio | - | - | - | 8 / 3 | - |
| $t_{W(CKL)}$ | Clock low time | fpp =50MHz | 9.5 | 10.5 | - | ns |
| $t_{W(CKH)}$ | Clock high time | fpp =50MHz | 8.5 | 9.5 | - | |
| **CMD, D inputs (referenced to CK) in MMC and SD HS mode** | | | | | | |
| $t_{ISU}$ | Input setup time HS | fpp =50MHz | 5 | - | - | ns |
| $t_{IH}$ | Input hold time HS | fpp =50MHz | 1 | - | - | |
| **CMD, D outputs (referenced to CK) in MMC and SD HS mode** | | | | | | |
| $t_{OV}$ | Output valid time HS | fpp =50MHz | - | 12 | 13.5 | ns |
| $t_{OH}$ | Output hold time HS | fpp =50MHz | 10.5 | - | - | |
| **CMD, D inputs (referenced to CK) in SD default mode** | | | | | | |
| $t_{ISUD}$ | Input setup time SD | fpp =25MHz | 5 | - | - | ns |
| $t_{IHD}$ | Input hold time SD | fpp =25MHz | 1 | - | - | |
| **CMD, D outputs (referenced to CK) in SD default mode** | | | | | | |
| $t_{OVD}$ | Output valid default time SD | fpp =25 MHz | - | 2 | 3 | ns |
| $t_{OHD}$ | Output hold default time SD | fpp =25 MHz | 1 | - | - | |

1. Guaranteed by characterization results.
2. $V_{DD}$ = 2.7 to 3.6 V.

**Table 101. eMMC characteristics $V_{DD}$ = 1.7 V to 1.9 V(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PP}$ | Clock frequency in data transfer mode | - | 0 | - | 50 | MHz |
| - | SDIO_CK/fPCLK2 frequency ratio | - | - | - | 8 / 3 | - |
| $t_{W(CKL)}$ | Clock low time | fpp =50MHz | 9.5 | 10.5 | - | ns |
| $t_{W(CKH)}$ | Clock high time | fpp =50MHz | 8.5 | 9.5 | - | |
| **CMD, D inputs (referenced to CK) in eMMC mode** | | | | | | |
| $t_{ISU}$ | Input setup time HS | fpp =50MHz | 3 | - | - | ns |
| $t_{IH}$ | Input hold time HS | fpp =50MHz | 2.5 | - | - | |
| **CMD, D outputs (referenced to CK) in eMMC mode** | | | | | | |
| $t_{OV}$ | Output valid time HS | fpp =50MHz | - | 15 | 15.5 | ns |
| $t_{OH}$ | Output hold time HS | fpp =50MHz | 13 | - | - | |

1. Guaranteed by characterization results.
2. $C_{LOAD}$ = 20 pF.

### 6.3.28 RTC characteristics

**Table 102. RTC characteristics**

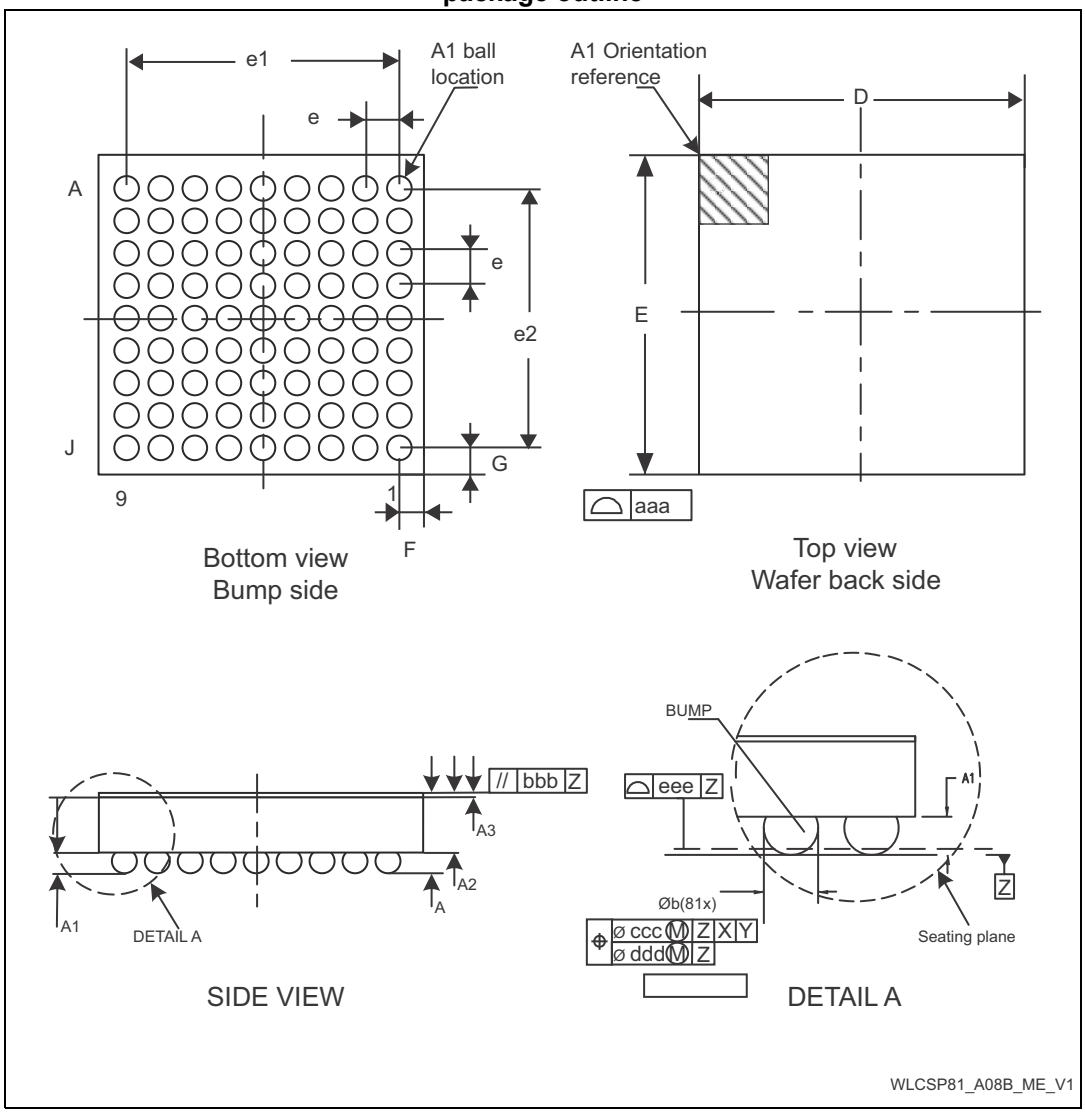
| Symbol | Parameter | Conditions | Min | Max |
|---|---|---|---|---|
| - | $f_{PCLK1}$/RTCCLK frequency ratio | Any read/write operation from/to an RTC register | 4 | - |

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.1 WLCSP81 package information

**Figure 63. WLCSP81 - 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package outline**




1. Drawing is not to scale.

**Table 103. WLCSP81 - 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | - | 0.175 | - | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| Ø b[3] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 4.004 | 4.039 | 4.074 | 0.1576 | 0.1590 | 0.1604 |
| E | 3.916 | 3.951 | 3.986 | 0.1542 | 0.1556 | 0.1569 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 3.200 | - | - | 0.1260 | - |
| e2 | - | 3.200 | - | - | 0.1260 | - |
| F | - | 0.4195 | - | - | 0.0165 | - |
| G | - | 0.3755 | - | - | 0.0148 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

**Figure 64. WLCSP81- 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package recommended footprint**

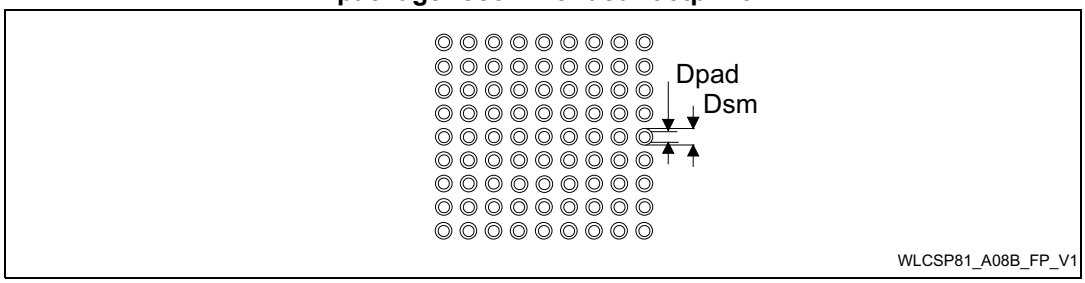



**Table 104. WLCSP81 recommended PCB design rules (0.4 mm pitch)**

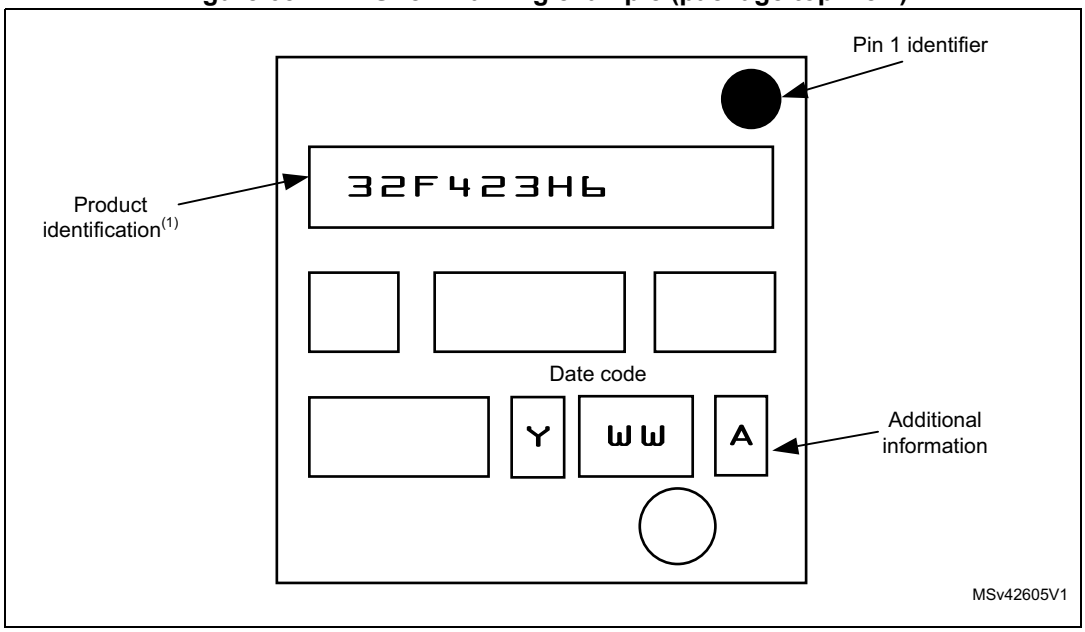
| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 mm |
| Dpad | 0.225 mm |
| Dsm | 0.290 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.250 mm |
| Stencil thickness | 0.100 mm |

### Device marking for WLCSP81

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

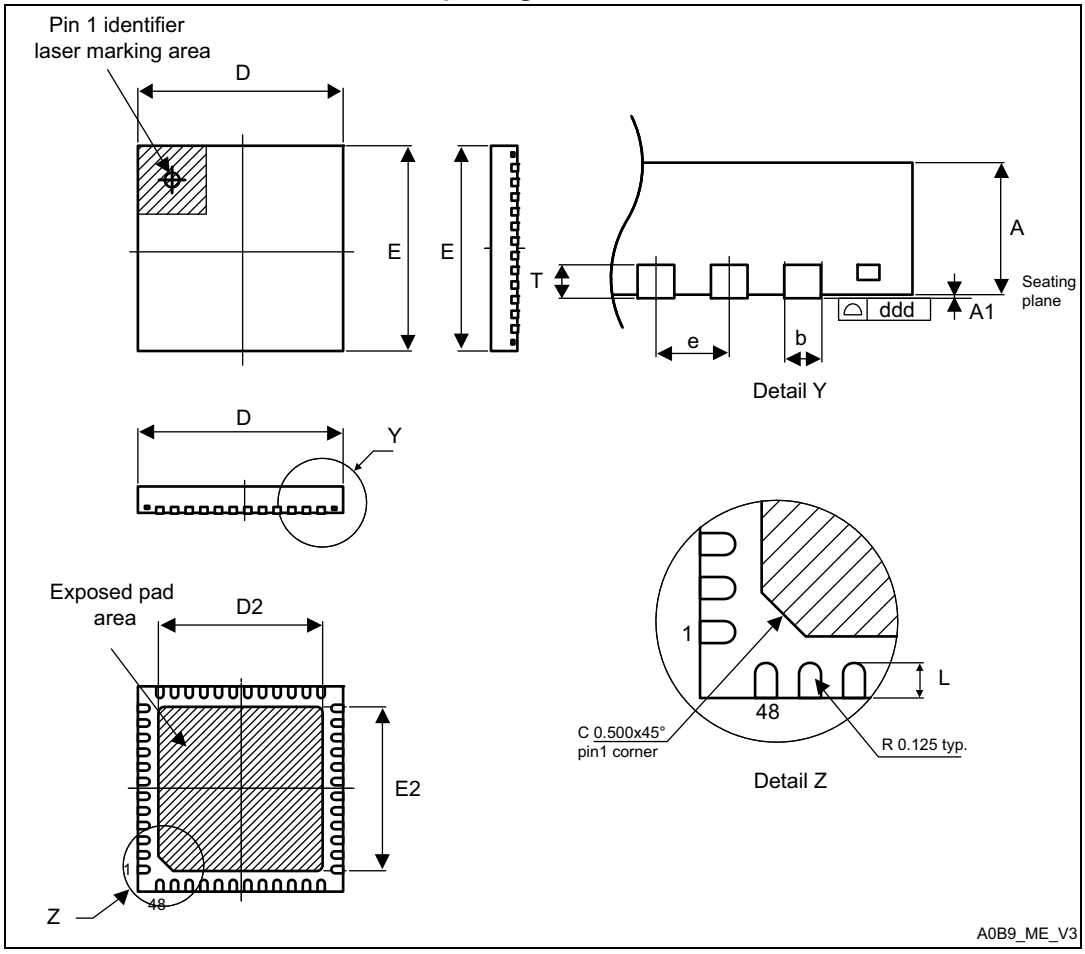
**Figure 65. WLCSP81 marking example (package top view)**




1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.2 UFQFPN48 package information

**Figure 66. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline**



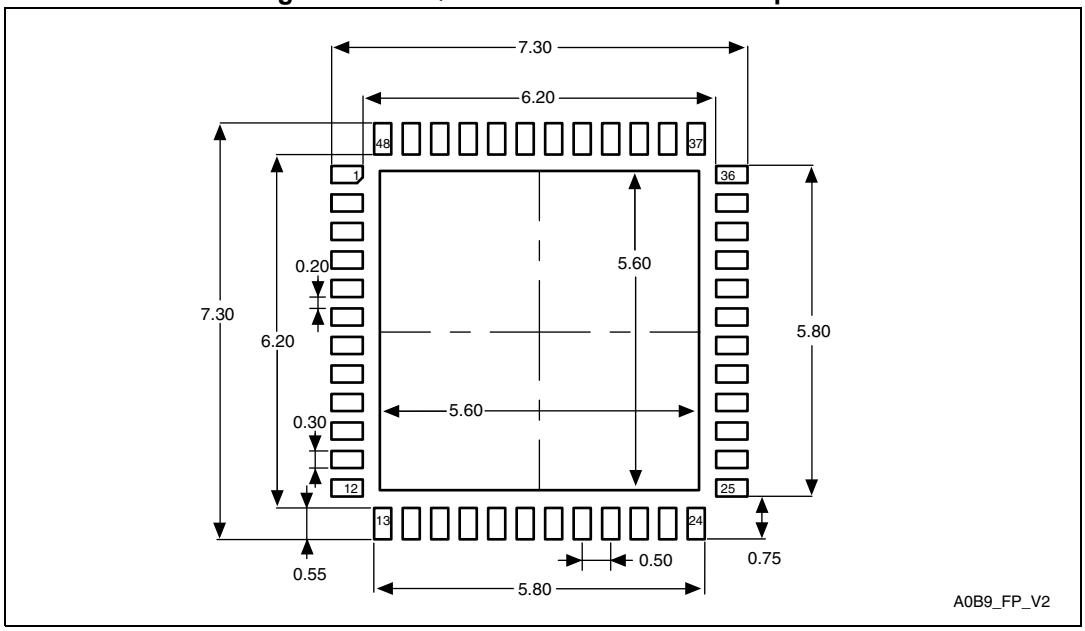

1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

**Table 105. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| D2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| E2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 67. UFQFPN48 recommended footprint**



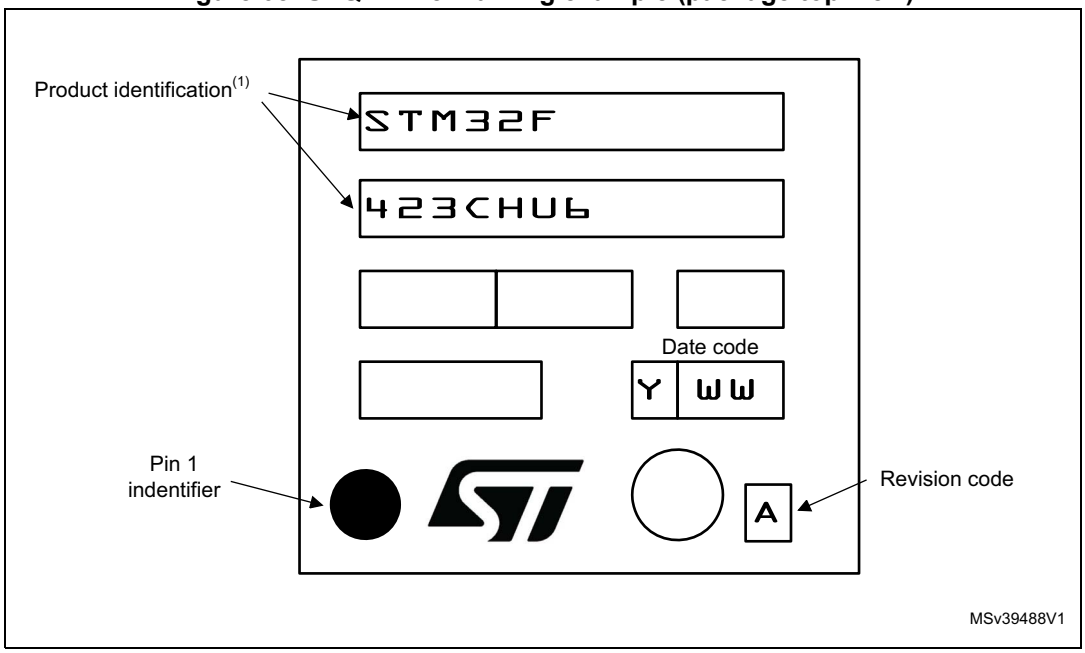

1. Dimensions are in millimeters.

### Device marking for UFQFPN48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

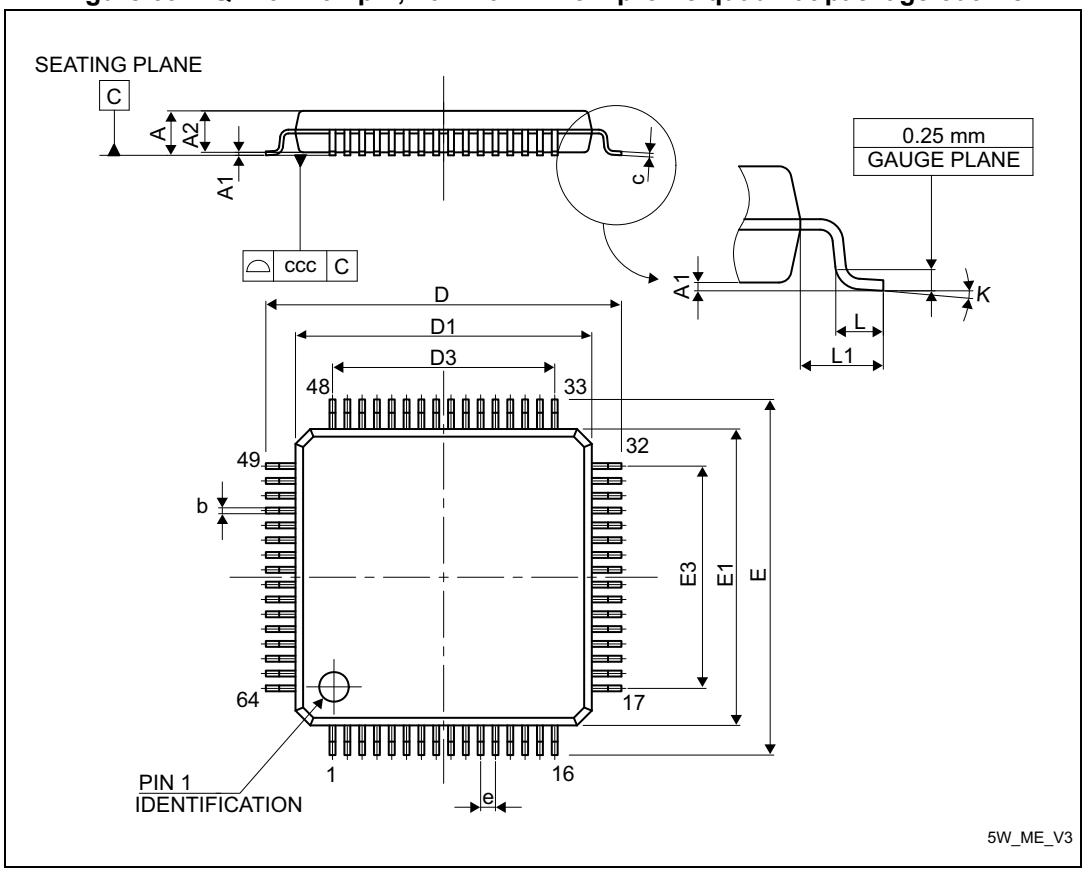
**Figure 68. UFQFPN48 marking example (package top view)**




1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.3 LQFP64 package information

**Figure 69. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline**



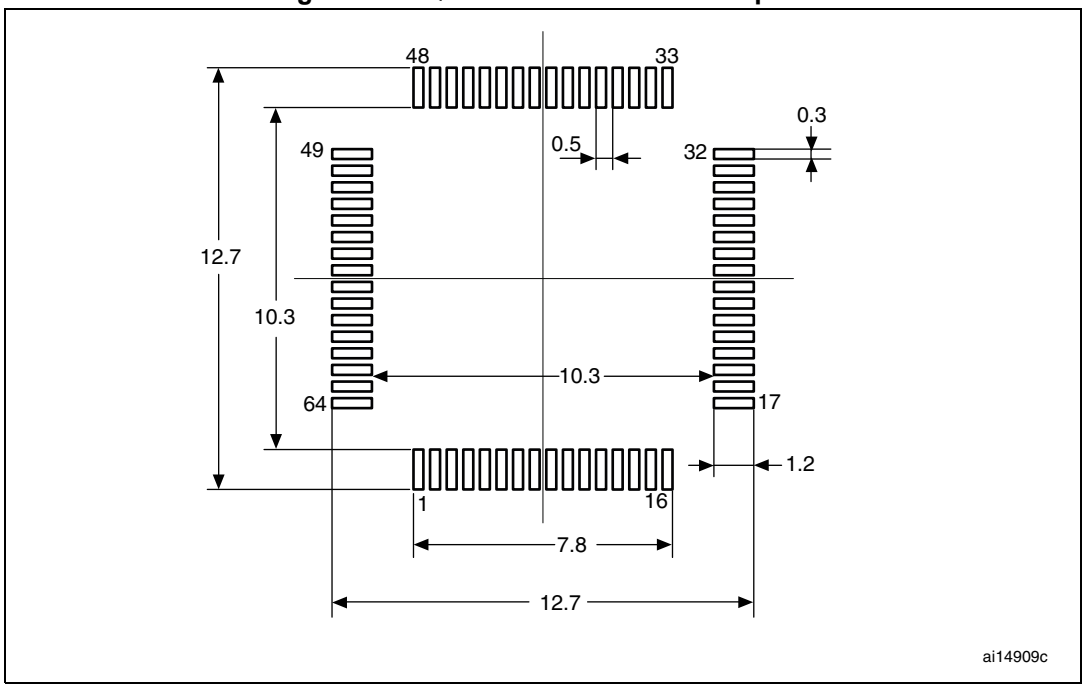

1. Drawing is not to scale.

**Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 70. LQFP64 recommended footprint**



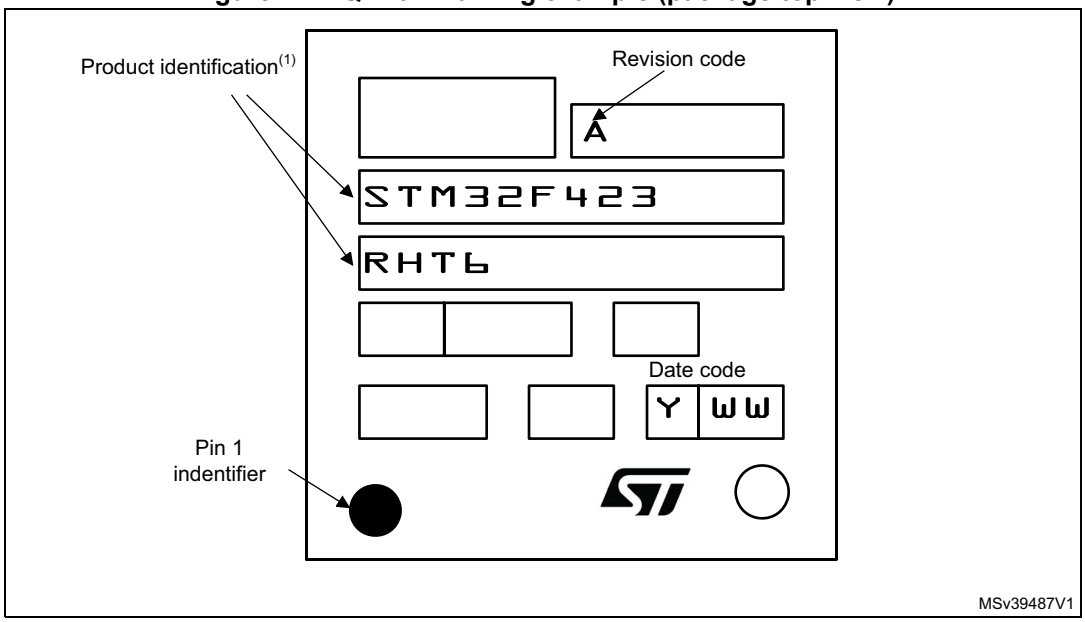

1. Dimensions are in millimeters.

### Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

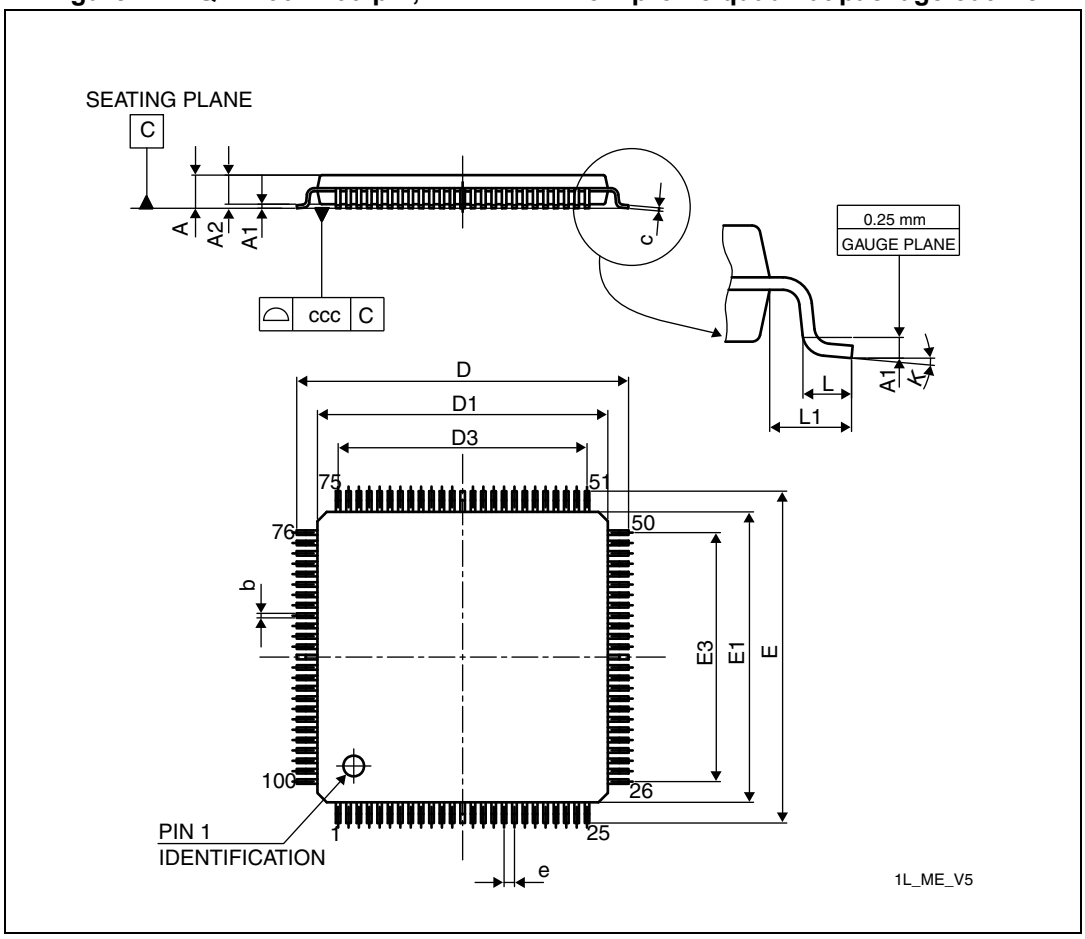
**Figure 71. LQFP64 marking example (package top view)**




1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.4 LQFP100 package information

**Figure 72. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline**




1. Drawing is not to scale. Dimensions are in millimeters.

**Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data**

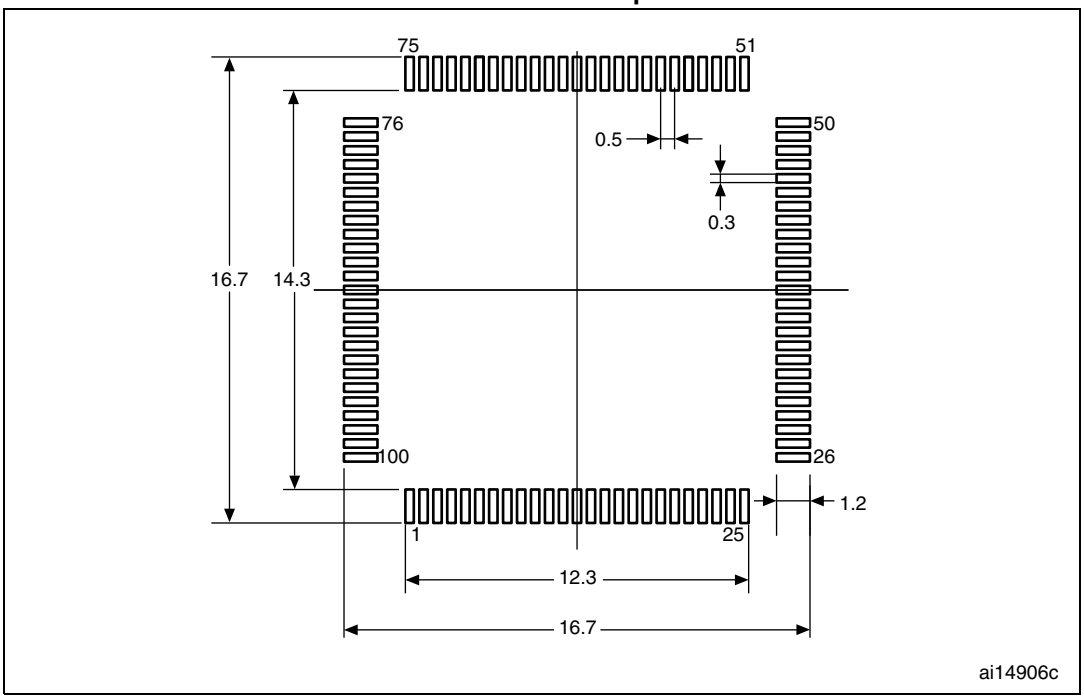
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.000 | - | - | 0.4724 | - |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |

**Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 73. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint**



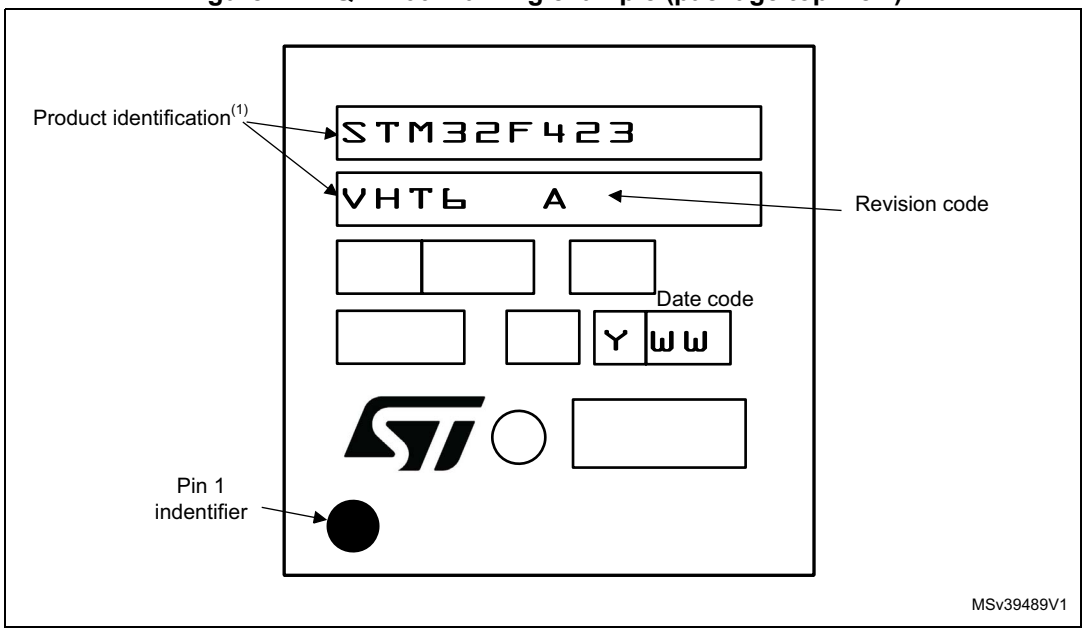

1. Dimensions are in millimeters.

### Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

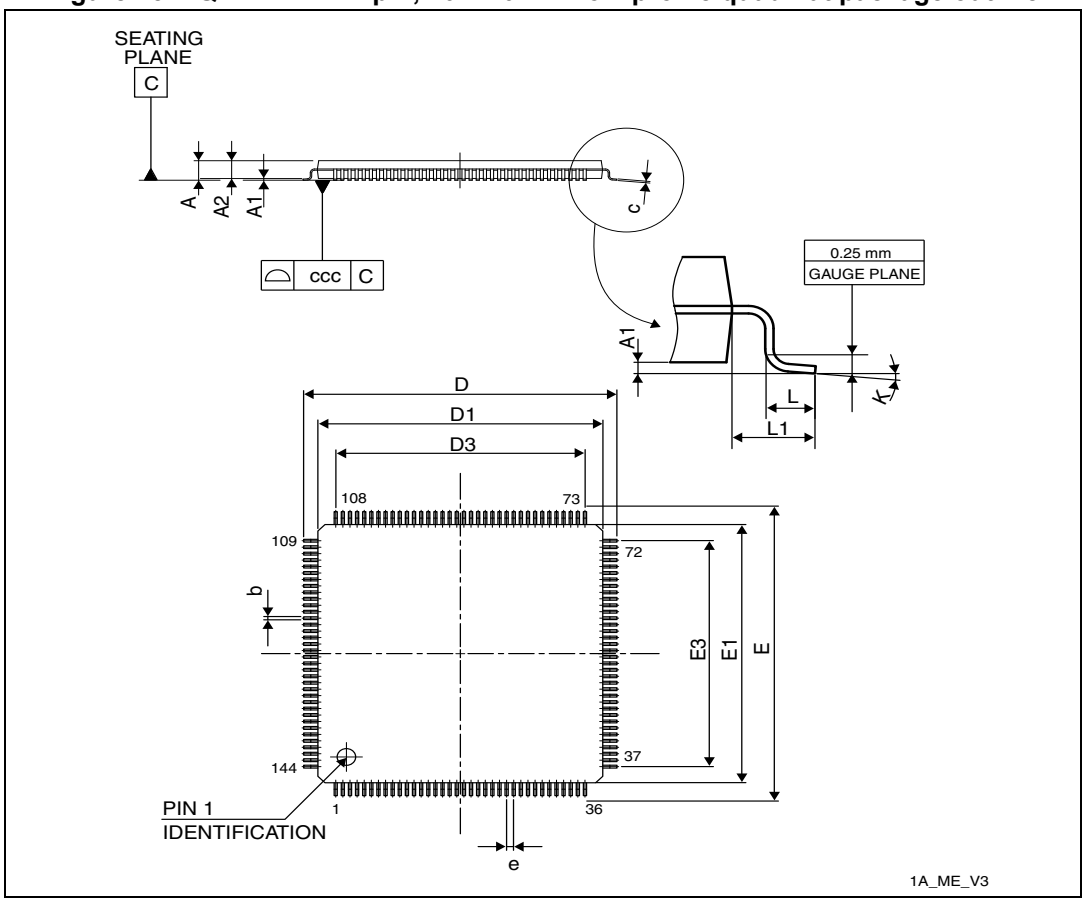
**Figure 74. LQFP100 marking example (package top view)**




1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.5 LQFP144 package information

**Figure 75. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline**



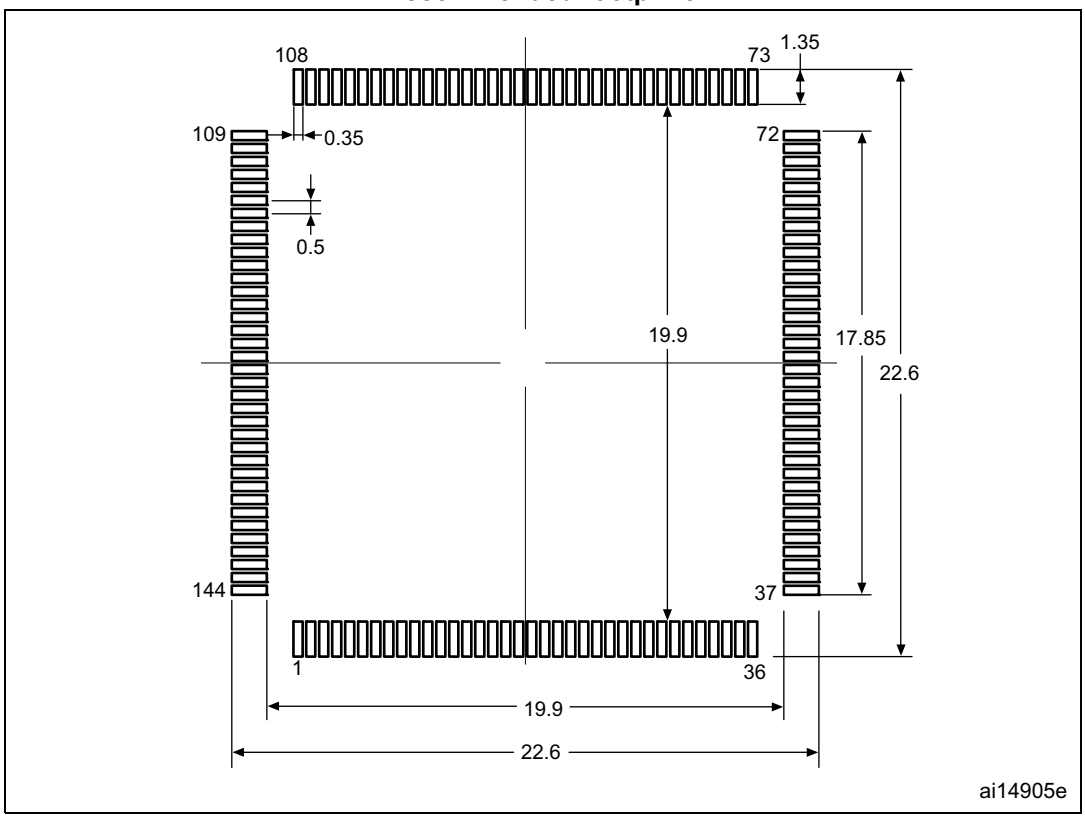

1. Drawing is not to scale.

**Table 108. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | - | 17.500 | - | - | 0.6890 | - |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | - | 17.500 | - | - | 0.6890 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 76. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint**



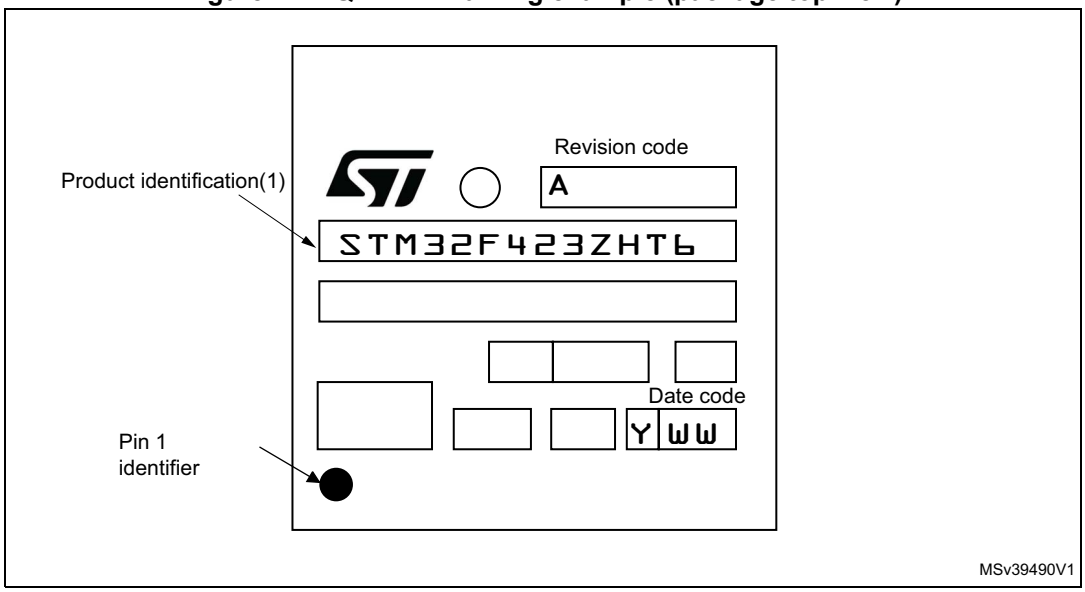

1. Dimensions are expressed in millimeters.

### Device marking for LQFP144

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

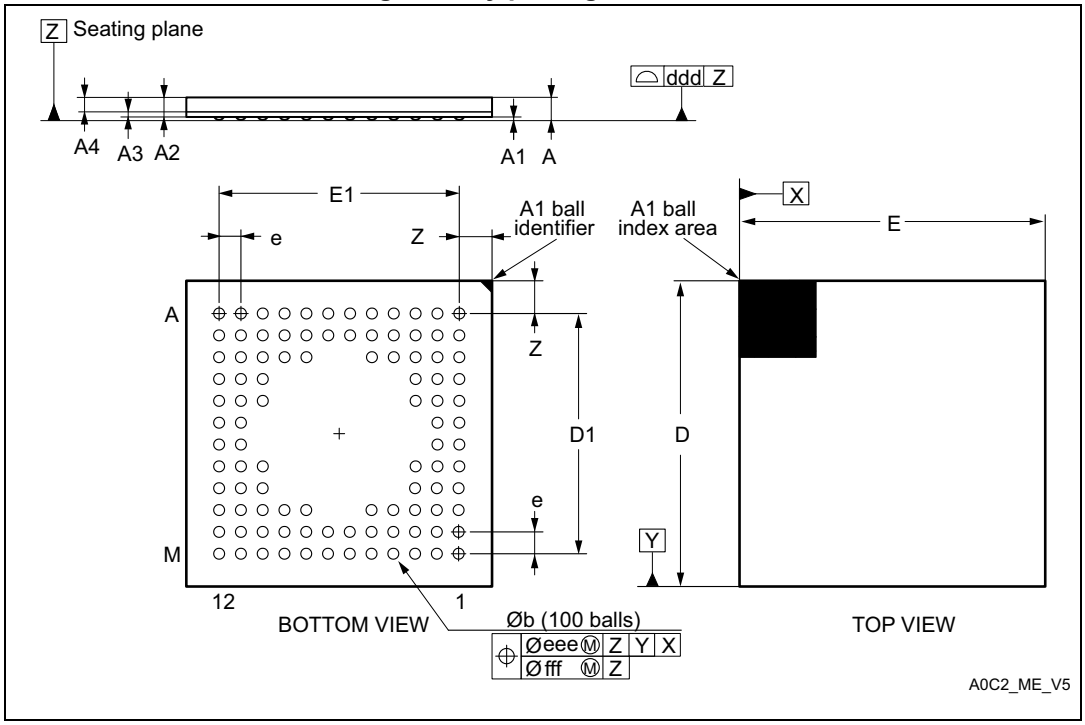
**Figure 77. LQFP144 marking example (package top view)**




1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.6 UFBGA100 package information

**Figure 78. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 109. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 0.600 | - | - | 0.0236 |
| A1 | - | - | 0.110 | - | - | 0.0043 |
| A2 | - | 0.450 | - | - | 0.0177 | - |
| A3 | - | 0.130 | - | - | 0.0051 | 0.0094 |
| A4 | - | 0.320 | - | - | 0.0126 | - |
| b | 0.240 | 0.290 | 0.340 | 0.0094 | 0.0114 | 0.0134 |
| D | 6.850 | 7.000 | 7.150 | 0.2697 | 0.2756 | 0.2815 |
| D1 | - | 5.500 | - | - | 0.2165 | - |
| E | 6.850 | 7.000 | 7.150 | 0.2697 | 0.2756 | 0.2815 |
| E1 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| Z | - | 0.750 | - | - | 0.0295 | - |

**Table 109. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| ddd | - | - | 0.080 | - | - | 0.0031 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 79. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint**

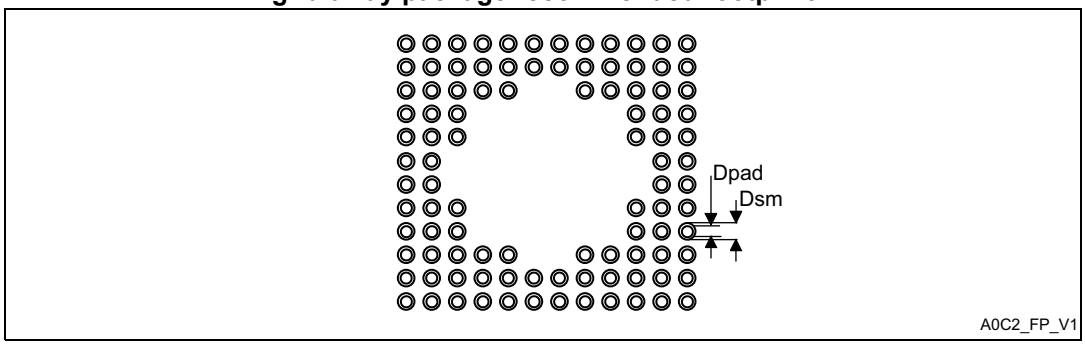



**Table 110. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)**

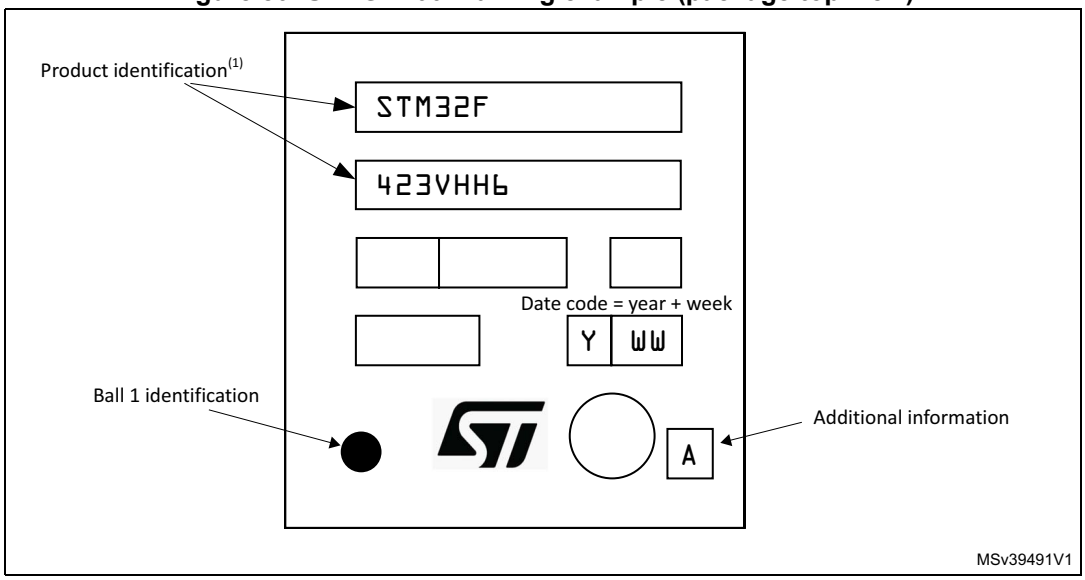
| Dimension | Recommended values |
|---|---|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |

### Device marking for UFBGA100

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

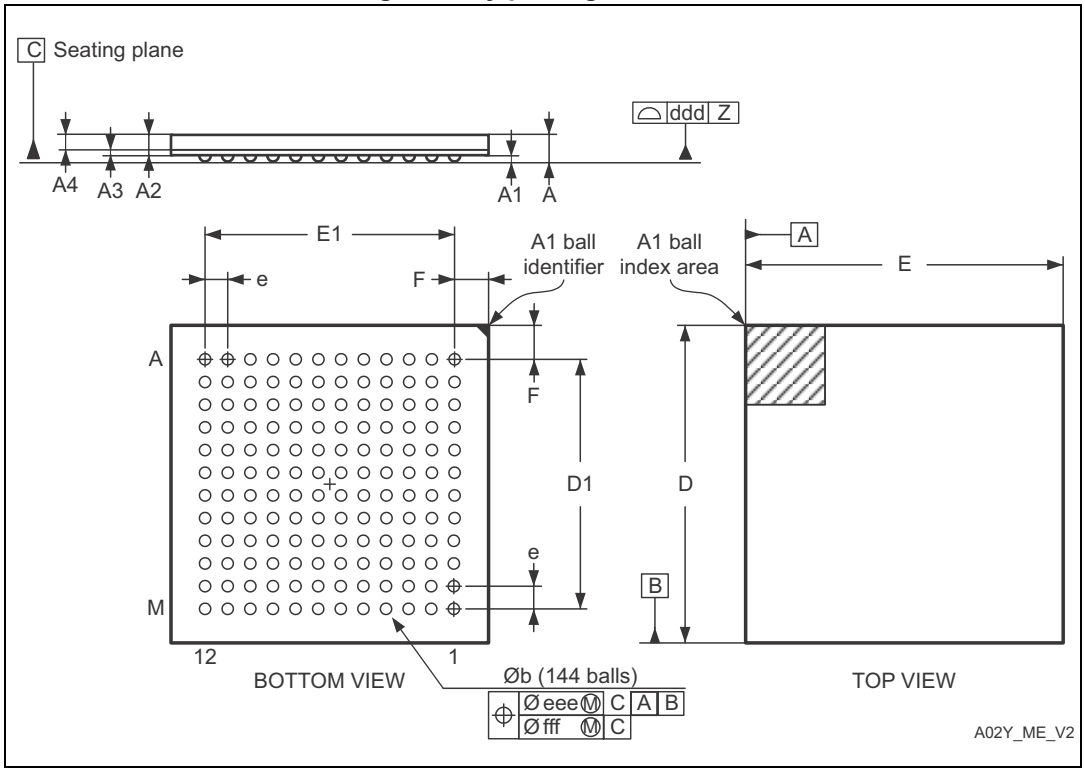
**Figure 80. UFBGA100 marking example (package top view)**




1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.7 UFBGA144 package information

**Figure 81. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 111. UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | - | 0.130 | - | - | 0.0051 | - |
| A4 | - | 0.320 | - | - | 0.0126 | - |
| b | 0.360 | 0.400 | 0.440 | 0.0091 | 0.0110 | 0.0130 |
| D | 9.950 | 10.000 | 10.050 | 0.2736 | 0.2756 | 0.2776 |
| D1 | 8.750 | 8.800 | 8.850 | 0.2343 | 0.2362 | 0.2382 |
| E | 9.950 | 10.000 | 10.050 | 0.2736 | 0.2756 | 0.2776 |
| E1 | 8.750 | 8.800 | 8.850 | 0.2343 | 0.2362 | 0.2382 |
| e | 0.750 | 0.800 | 0.850 | - | 0.0197 | - |

**Table 111. UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| F | 0.550 | 0.600 | 0.650 | 0.0177 | 0.0197 | 0.0217 |
| ddd | - | - | 0.080 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.080 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 82. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array recommended footprint**

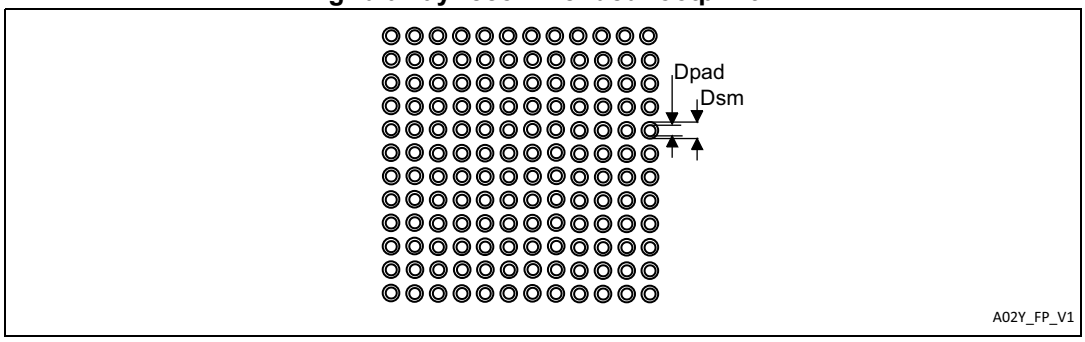



**Table 112. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.80 mm |
| Dpad | 0.400 mm |
| Dsm | 0.550 mm typ. (depends on the soldermask registration tolerance) |

*Note: Non solder mask defined (NSMD) pads are recommended.*

*4 to 6 mils solder paste screen printing process.*

*Stencil opening is 0.400 mm.*

*Stencil thickness is between 0.100 mm and 0.125 mm.*

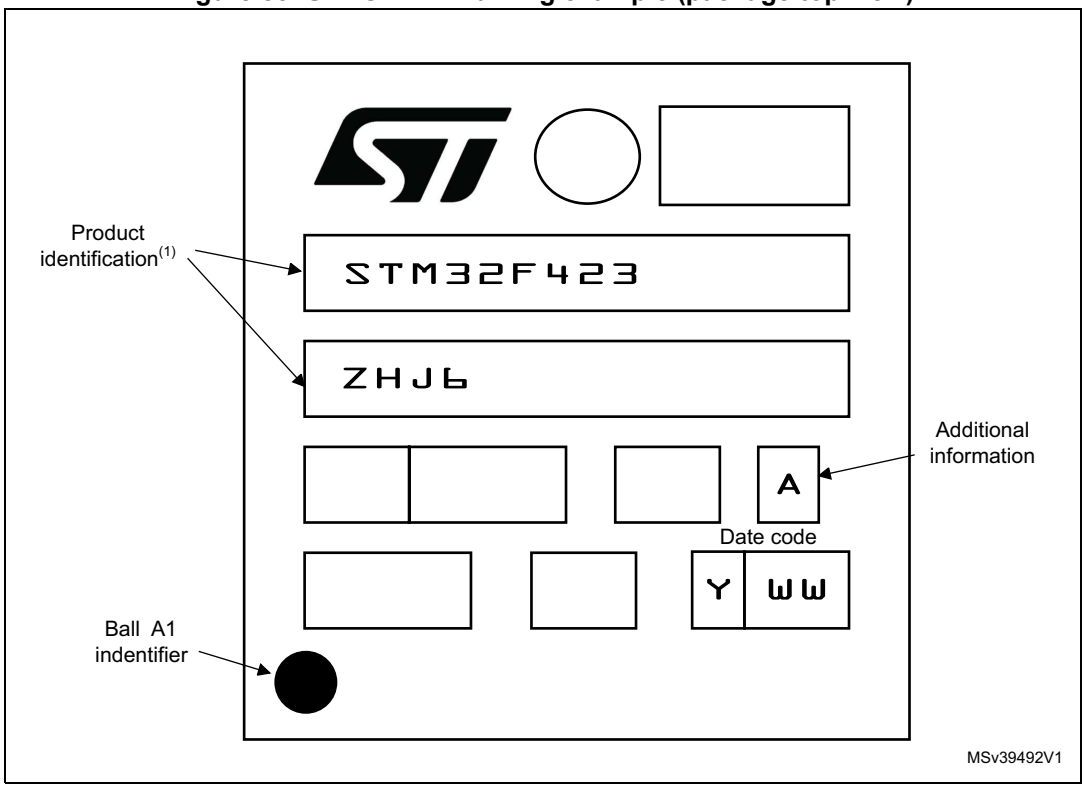
*Pad trace width is 0.120 mm.*

### Device marking for UFBGA144

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 83. UFBGA144 marking example (package top view)**




1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 17: General operating conditions*.

The maximum chip-junction temperature, $T_J$ max., in degrees Celsius, may be calculated using the following equation:

$T_J$ max = $T_A$ max + (PD max x $\Theta_{JA}$)

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- PD max is the sum of $P_{INT}$ max and $P_{I/O}$ max (PD max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 113. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP144 - 20 x 20 mm | 35 | °C/W |
| | **Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm | 43 | |
| | **Thermal resistance junction-ambient** LQFP64 - 10 x 10 mm | 47 | |
| | **Thermal resistance junction-ambient** UFBGA144 - 10 x 10 mm / 0.8 mm pitch | 48 | |
| | **Thermal resistance junction-ambient** UFBGA100 - 7 x 7 mm | 57 | |
| | **Thermal resistance junction-ambient** WLCSP81 - 4.039 x 3.951 mm | 39.7 | |
| | **Thermal resistance junction-ambient** UFQFPN48 - 7 x 7 mm | 32 | |

### 7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

# 8 Ordering information

**Table 114. Ordering information scheme**

Example: STM32 F 423 C H T 6 TR

**Device family**

STM32 = Arm®-based 32-bit microcontroller

**Product type**

F = General-purpose

Device subfamily

423 = 423 line with AES

Pin count

C = 48 pins

R = 64 pins

M = 81 pins

V = 100 pins

Z = 144 pins

**Flash memory size**

H = 1536 Kbytes of Flash memory

**Package**

H = UFBGA 7 x 7 mm

J = UFBGA 10 x 10 mm

T = LQFP

U = UFQFPN

Y = WLCSP

**Temperature range**

6 = Industrial temperature range, – 40 to 85 °C

3 = Industrial temperature range, – 40 to 125 °C

Packing

TR = tape and reel

No character = tray or tube

# Appendix A Recommendations when using the internal reset OFF

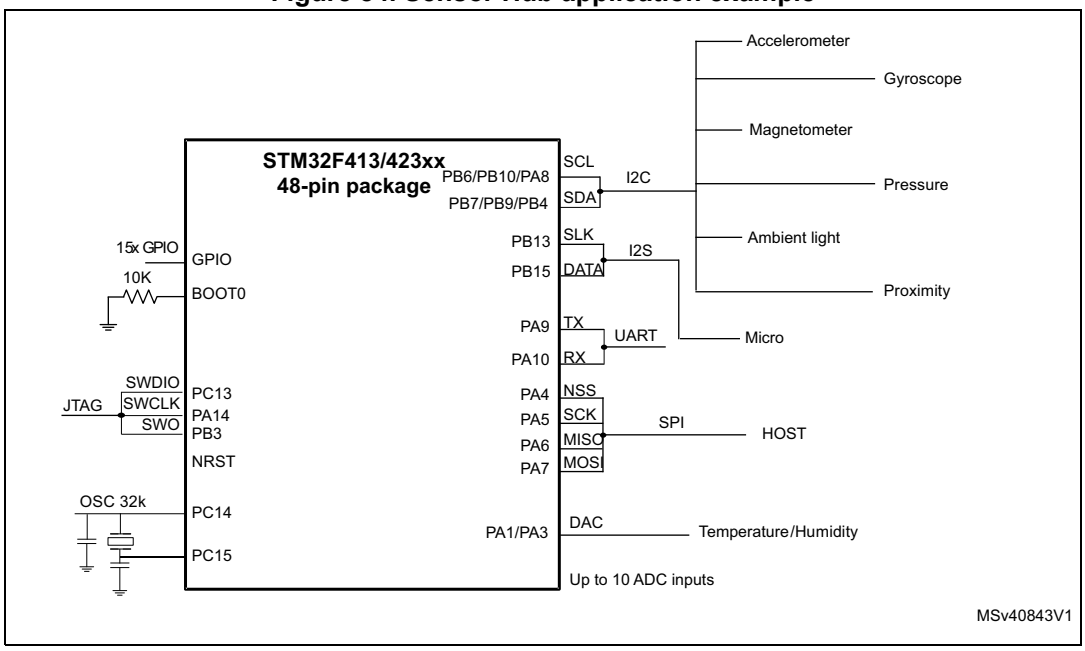
When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$ functionality is no more available and VBAT pin should be connected to $V_{DD}$.

# Appendix B Application block diagrams

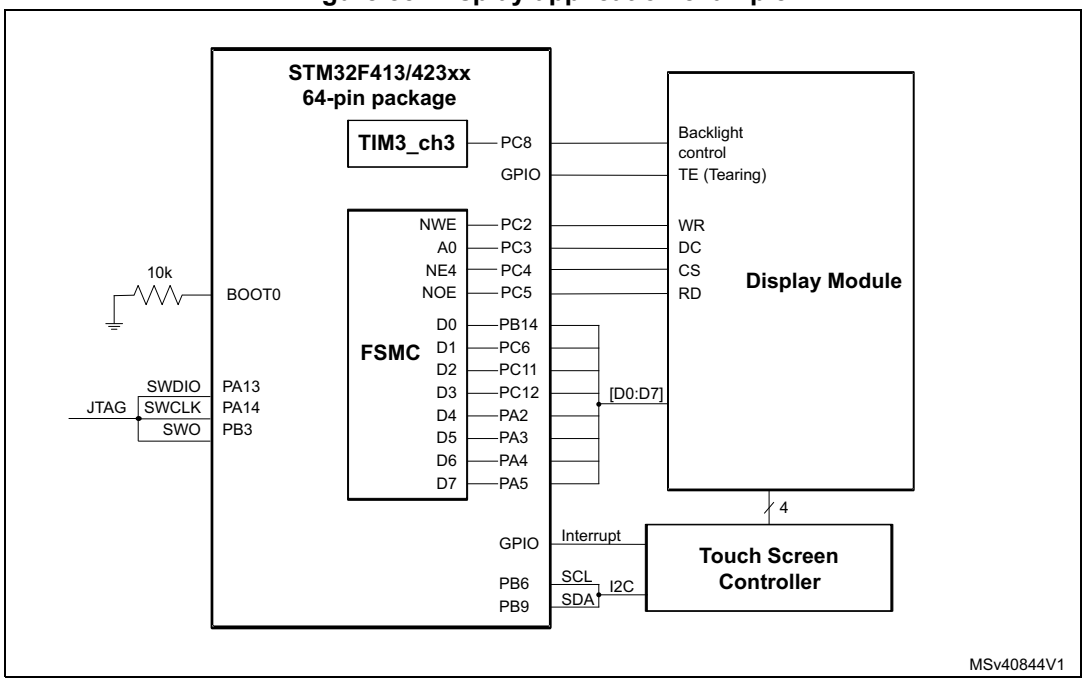
## B.1 Sensor Hub application example

**Figure 84. Sensor Hub application example**



## B.2 Display application example

**Figure 85. Display application example**

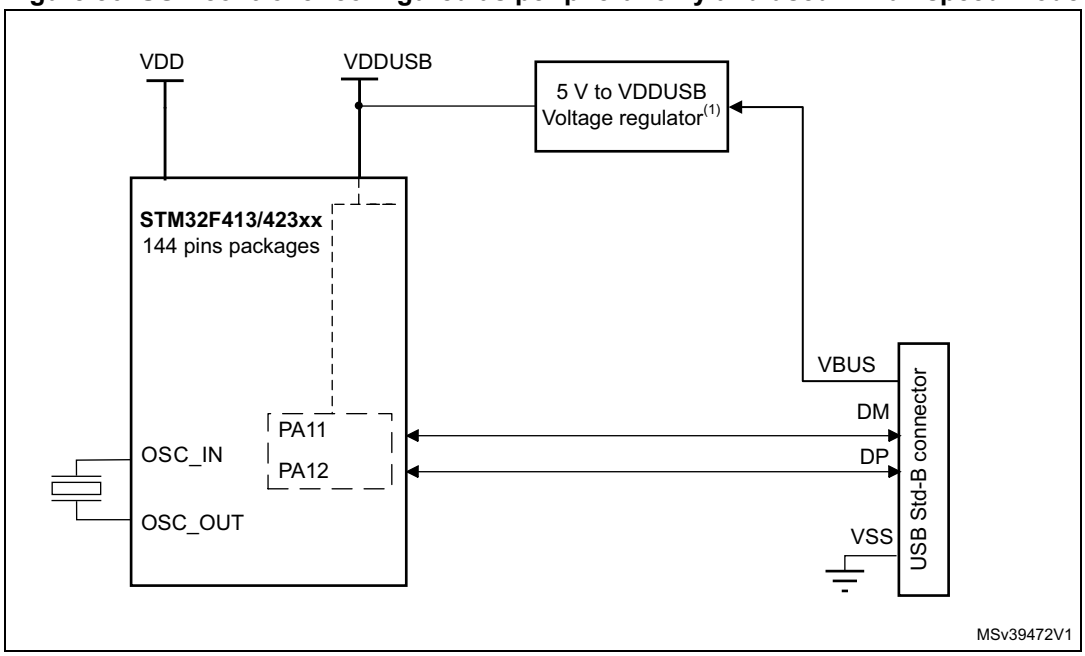



*Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.*

MSv40843

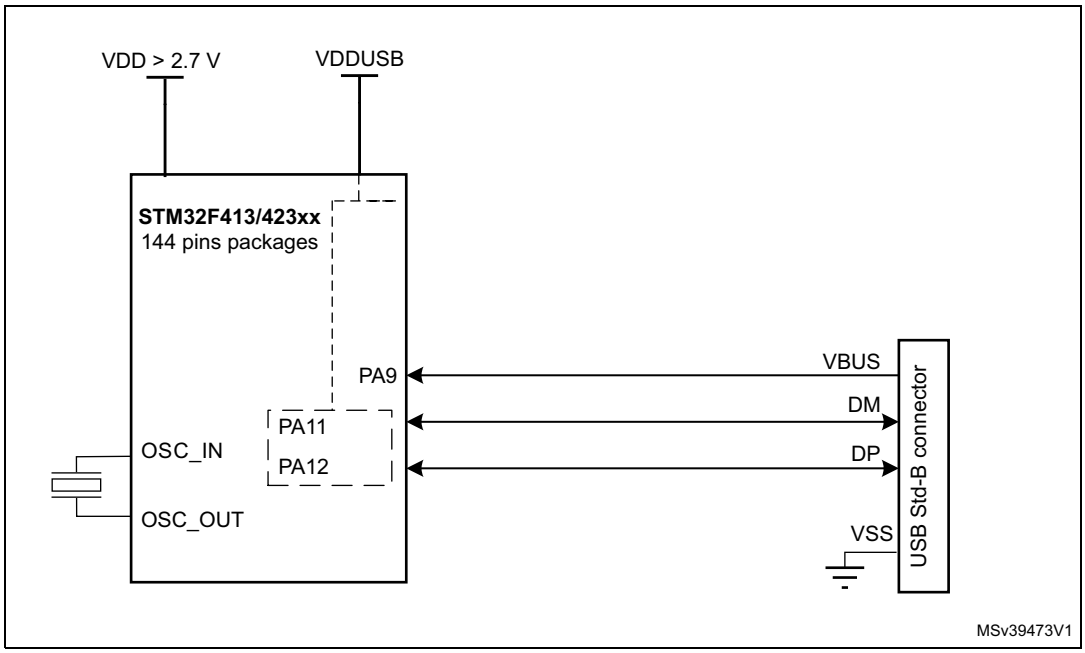
## B.3 USB OTG full speed (FS) interface solutions

**Figure 86. USB controller configured as peripheral-only and used in Full speed mode**



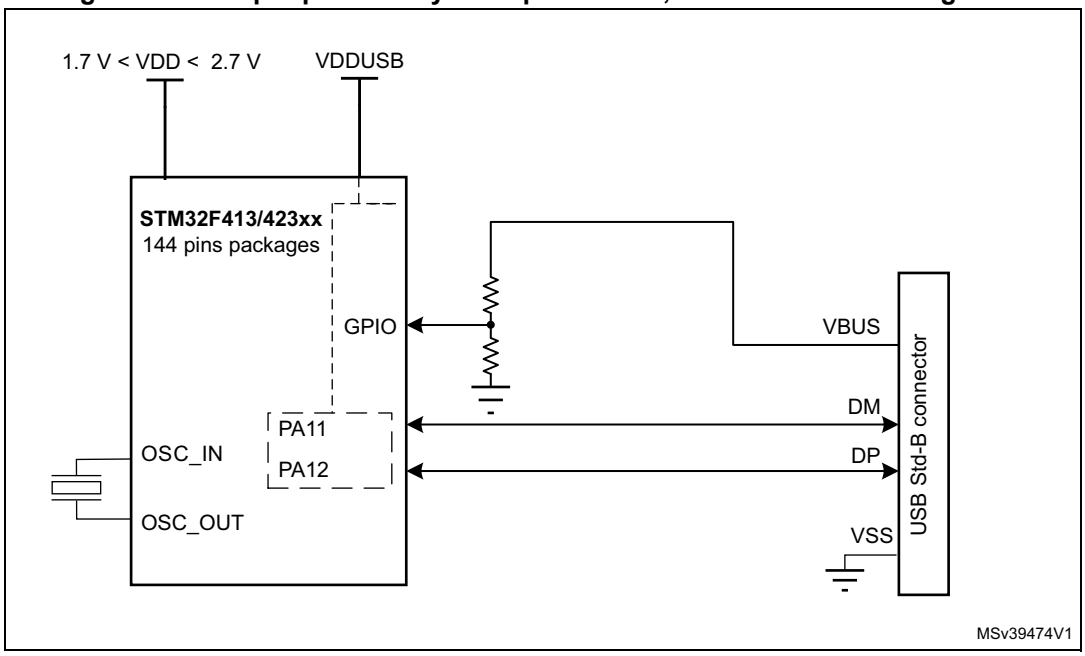

1. External voltage regulator only needed when building a $V_{BUS}$ powered device.

**Figure 87. USB peripheral-only Full speed mode with direct connection for VBUS sense**



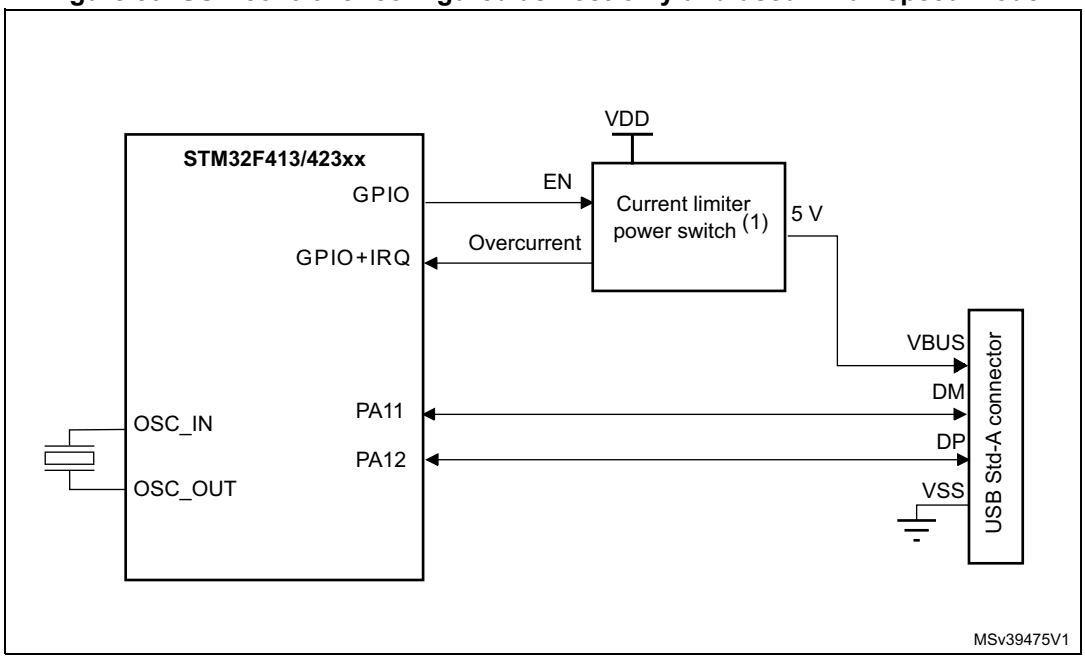

1. External voltage regulator only needed when building a $V_{BUS}$ powered device.

**Figure 88. USB peripheral-only Full speed mode, VBUS detection using GPIO**




1. External voltage regulator only needed when building a $V_{BUS}$ powered device.

**Figure 89. USB controller configured as host-only and used in full speed mode**




2. The current limiter is required only if the application has to support a $V_{BUS}$ powered device. A basic power switch can be used if 5 V are available on the application board.

# Revision history

**Table 115. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 02-Sep-2016 | 1 | Initial release. |
| 24-Oct-2016 | 2 | Updated *Figure 65: WLCSP81 marking example (package top view)* |
| 13-Dec-2016 | 3 | Updated:<br>– *Table 55: EMI characteristics for LQFP144*<br>– *Table 56: ESD absolute maximum ratings*<br>– *Table 70: QSPI dynamic characteristics in SDR mode*<br>– *Table 111: UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data*<br>– *Figure 81: UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline* |
| 12-Jan-2017 | 4 | Added:<br>– *Table 1: Device summary* |
| 07-Mar-2017 | 5 | Updated:<br>– *Table 2: STM32F423xH features and peripheral counts*<br>– *Table 12: STM32F423xH alternate functions*<br>Added:<br>– *Table 11: FSMC pin definition* |

**Table 115. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 19-Jun-2017 | 6 | Added:<br>– *Section 4.1: WLCSP81 pinout description*<br>– *Section 4.2: UFQFPN48 pinout description*<br>– *Section 4.3: LQFP64 pinout description*<br>– *Section 4.4: LQFP100 pinout description*<br>– *Section 4.5: LQFP144 pinout description*<br>– *Section 4.6: UFBGA100 pinout description*<br>– *Section 4.7: UFBGA144 pinout description*<br>– *Section 4.8: Pins definition*<br>– *Section 4.9: Alternate functions*<br>Updated:<br>– *Table 10: STM32F423xH pin definition*<br>– *Table 11: FSMC pin definition*<br>– *Figure 38: I2C bus AC waveforms and measurement circuit*<br>– *Figure 39: FMPI2C timing diagram and measurement circuit* |
| 15-Sep-2017 | 7 | Updated:<br>– *Section 3.29: Digital filter for sigma-delta modulators (DFSDM)*<br>– *Table 53: Flash memory endurance and data retention*<br>– *Table 59: I/O static characteristics*<br>– *Table 75: ADC characteristics* |

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