International
IOR Rectifier

Data Sheet No. PD60252 revA

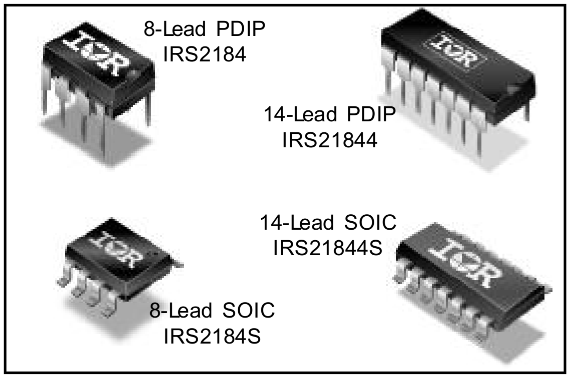
# IRS2184/IRS21844(S)PbF

# HALF-BRIDGE DRIVER

## Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4 A/1.8 A
- RoHS compliant

## Packages



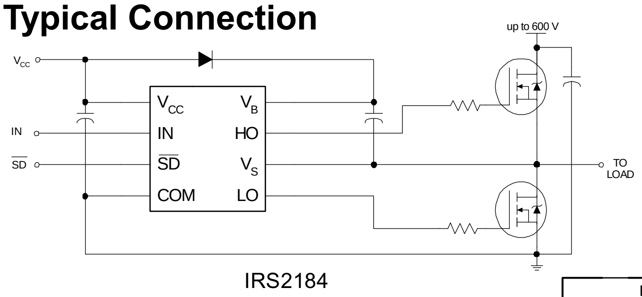

## Description

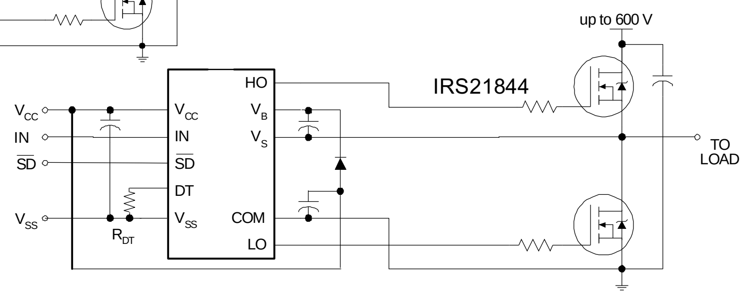
The IRS2184/IRS21844 are high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

### Feature Comparison

| Part | Input logic | Cross-conduction prevention logic | Deadtime (ns) | Ground Pins | $t_{on}/t_{off}$ (ns) |
|---|---|---|---|---|---|
| 2181 | HIN/LIN | no | none | COM | 180/220 |
| 21814 | | | | $V_{SS}$/COM | |
| 2183 | HIN/$\overline{LIN}$ | yes | Internal 400 | COM | 180/220 |
| 21834 | | | Program 400-5000 | $V_{SS}$/COM | |
| 2184 | IN/$\overline{SD}$ | yes | Internal 400 | COM | 680/270 |
| 21844 | | | Program 400-5000 | $V_{SS}$/COM | |

## Typical Connection




(Refer to Lead Assignments for correct configuration).These diagrams show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_B$ | High-side floating absolute voltage | | -0.3 | 620 (Note 1) | V |
| $V_S$ | High-side floating supply offset voltage | | $V_B$ - 20 | $V_B$ + 0.3 | |
| $V_{HO}$ | High-side floating output voltage | | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{CC}$ | Low-side and logic fixed supply voltage | | -0.3 | 20 (Note 1) | |
| $V_{LO}$ | Low-side output voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| DT | Programmable dead-time pin voltage (IRS21844 only) | | $V_{SS}$ - 0.3 | $V_{CC}$ + 0.3 | |
| $V_{IN}$ | Logic input voltage (IN & $\overline{SD}$) | | $V_{SS}$ - 0.3 | $V_{CC}$ + 0.3 | |
| $V_{SS}$ | Logic ground (IRS21844 only) | | $V_{CC}$ - 20 | $V_{CC}$ + 0.3 | |
| $dV_S/dt$ | Allowable offset supply voltage transient | | — | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \le$ +25 °C | (8-lead PDIP) | — | 1.0 | W |
| | | (8-lead SOIC) | — | 0.625 | |
| | | (14-lead PDIP) | — | 1.6 | |
| | | (14-lead SOIC) | — | 1.0 | |
| $Rth_{JA}$ | Thermal resistance, junction to ambient | (8-lead PDIP) | — | 125 | °C/W |
| | | (8-lead SOIC) | — | 200 | |
| | | (14-lead PDIP) | — | 75 | |
| | | (14-lead SOIC) | — | 120 | |
| $T_J$ | Junction temperature | | — | 150 | °C |
| $T_S$ | Storage temperature | | -50 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 300 | |

Note 1: All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The $V_S$ and $V_{SS}$ offset rating are tested with all supplies biased at a 15 V differential.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$ | High-side floating supply absolute voltage | $V_S$ + 10 | $V_S$ + 20 | |
| $V_S$ | High-side floating supply offset voltage | COM -8 (Note 2) | 600 | |
| $V_{St}$ | Transient high-side floating supply offset voltage | -50 (Note 3) | 600 | |
| $V_{HO}$ | High-side floating output voltage | $V_S$ | $V_B$ | |
| $V_{CC}$ | Low-side and logic fixed supply voltage | 10 | 20 | V |
| $V_{LO}$ | Low-side output voltage | 0 | $V_{CC}$ | |
| $V_{IN}$ | Logic input voltage (IN & $\overline{SD}$) | $V_{SS}$ | $V_{CC}$ | |
| DT | Programmable deadtime pin voltage (IRS21844 only) | $V_{SS}$ | $V_{CC}$ | |
| $V_{SS}$ | Logic ground (IRS21844 only) | -5 | 5 | |
| $T_A$ | Ambient temperature | -40 | 125 | °C |

**Note 2**: Logic operational for $V_S$ of -5 V to +600 V. Logic state held for $V_S$ of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
**Note 3:** Operational for transient negative VS of COM - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15 V, $V_{SS}$ = COM, $C_L$ = 1000 pF, $T_A$ = 25° C, DT = $V_{SS}$ unless otherwise specified.

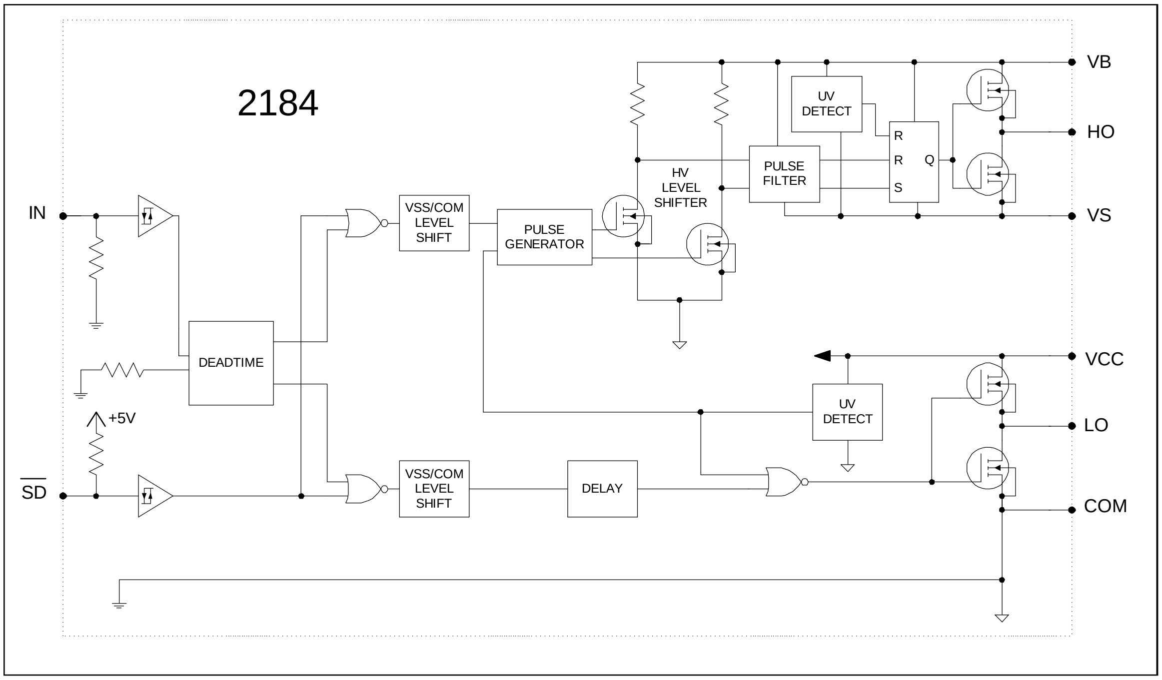
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | — | 680 | 900 | | $V_S$ = 0 V |
| $t_{off}$ | Turn-off propagation delay | — | 270 | 400 | | $V_S$ = 0 V or 600 V |
| $t_{sd}$ | Shut-down propagation delay | — | 180 | 270 | | |
| MTon | Delay matching, HS & LS turn-on | — | 0 | 90 | ns | |
| MToff | Delay matching, HS & LS turn-off | — | 0 | 40 | | |
| $t_r$ | Turn-on rise time | — | 40 | 60 | | $V_S$ = 0 V |
| $t_f$ | Turn-off fall time | — | 20 | 35 | | |
| DT | Deadtime: LO turn-off to HO turn-on($DT_{LO-HO}$) & | 280 | 400 | 520 | | $R_{DT}$= 0 Ω |
| | HO turn-off to LO turn-on ($DT_{HO-LO}$) | 4 | 5 | 6 | µs | $R_{DT}$ = 200 kΩ |
| MDT | Deadtime matching = $DT_{LO-HO}$ - $DT_{HO-LO}$ | — | 0 | 50 | ns | $R_{DT}$=0 Ω |
| | | — | 0 | 600 | | $R_{DT}$ = 200 kΩ |

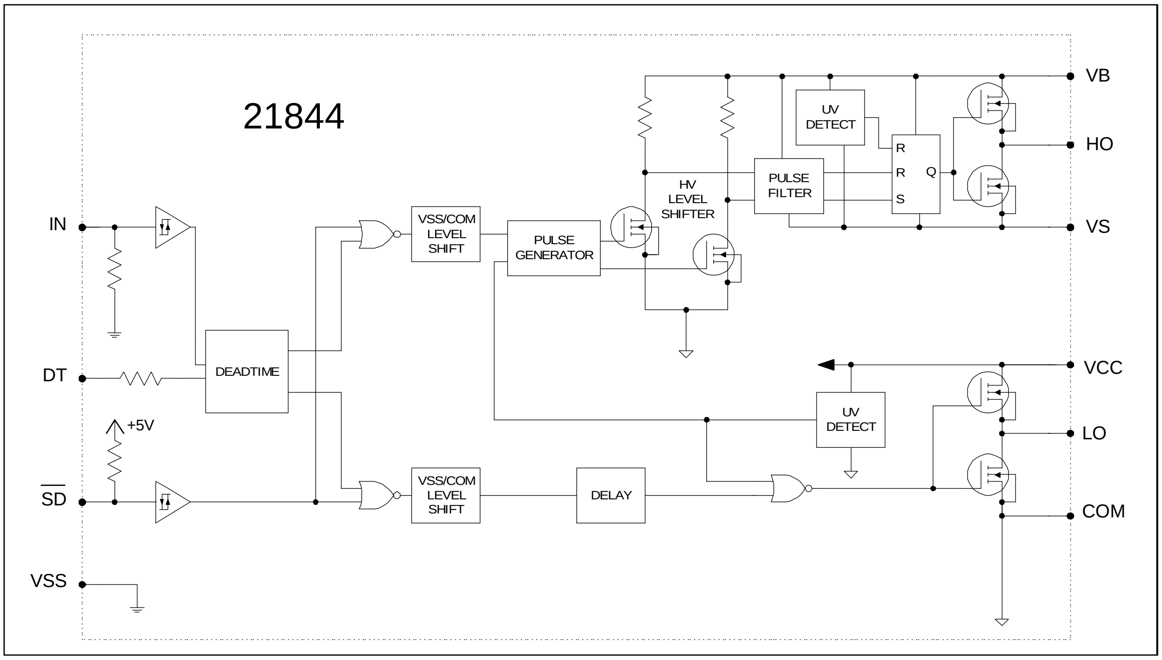
## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15 V, $V_{SS}$ = COM, DT= $V_{SS}$ and $T_A$ = 25 °C unless otherwise specified. The $V_{IL}$, $V_{IH}$, and $I_{IN}$ parameters are referenced to $V_{SS}$ /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The $V_O$, $I_O$, and $R_{on}$ parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic "1" input voltage for HO & logic "0" for LO | 2.5 | — | — | V | $V_{CC}$ = 10 V to 20 V |
| $V_{IL}$ | Logic "0" input voltage for HO & logic "1" for LO | — | — | 0.8 | V | $V_{CC}$ = 10 V to 20 V |
| $V_{SD,TH+}$ | $\overline{SD}$ input positive going threshold | 2.5 | — | — | V | $V_{CC}$ = 10 V to 20 V |
| $V_{SD,TH-}$ | $\overline{SD}$ input negative going threshold | — | — | 0.8 | V | $V_{CC}$ = 10 V to 20 V |
| $V_{OH}$ | High level output voltage, $V_{BIAS}$ - $V_O$ | — | — | 1.4 | V | $I_O$ = 0 A |
| $V_{OL}$ | Low level output voltage, $V_O$ | — | — | 0.2 | V | $I_O$ = 20 mA |
| $I_{LK}$ | Offset supply leakage current | — | — | 50 | µA | $V_B$ = $V_S$ = 600 V |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | 20 | 60 | 150 | µA | $V_{IN}$ = 0 V or 5 V |
| $I_{QCC}$ | Quiescent $V_{CC}$ supply current | 0.4 | 1.0 | 1.6 | mA | $V_{IN}$ = 0 V or 5 V |
| $I_{IN+}$ | Logic "1" input bias current | — | 25 | 60 | µA | IN = 5 V, $\overline{SD}$ = 0 V |
| $I_{IN-}$ | Logic "0" input bias current | — | — | 5.0 | µA | IN = 0 V, $\overline{SD}$ = 5 V |
| $V_{CCUV+}$<br>$V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold | 8.0 | 8.9 | 9.8 | V | |
| $V_{CCUV-}$<br>$V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold | 7.4 | 8.2 | 9.0 | V | |
| $V_{CCUVH}$<br>$V_{BSUVH}$ | Hysteresis | 0.3 | 0.7 | — | V | |
| $I_{O+}$ | Output high short circuit pulsed current | 1.4 | 1.9 | — | A | $V_O$ = 0 V,<br>PW ≤ 10 µs |
| $I_{O-}$ | Output low short circuit pulsed current | 1.8 | 2.3 | — | A | $V_O$ = 15 V,<br>PW ≤ 10 µs |

## Functional Block Diagrams

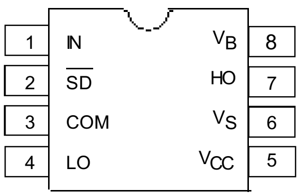


## Lead Definitions

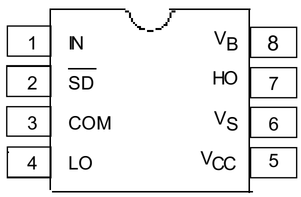
| Symbol | Description |
|---|---|
| IN | Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IRS2184 and VSS for IRS21844) |
| $\overline{\text{SD}}$ | Logic input for shutdown (referenced to COM for IRS2184 and VSS for IRS21844) |
| DT | Programmable deadtime lead, referenced to VSS. (IRS21844 only) |
| VSS | Logic ground (IRS21844 only) |
| $V_B$ | High-side floating supply |
| HO | High-side gate drive output |
| $V_S$ | High-side floating supply return |
| $V_{CC}$ | Low-side and logic fixed supply |
| LO | Low-side gate drive output |
| COM | Low-side return |

## Lead Assignments



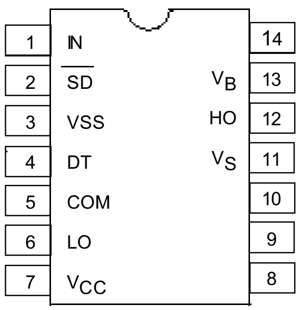
8-Lead PDIP

**IRS2184PbF**



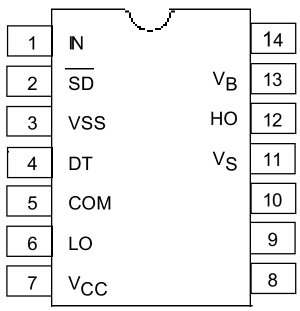
8-Lead SOIC

**IRS2184SPbF**



14-Lead PDIP

**IRS21844PbF**



14-Lead SOIC

**IRS21844SPbF**

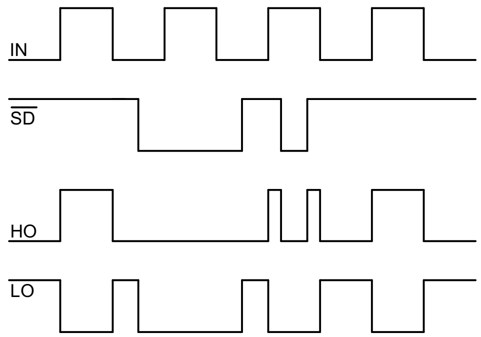



Figure 1. Input/Output Timing Diagram

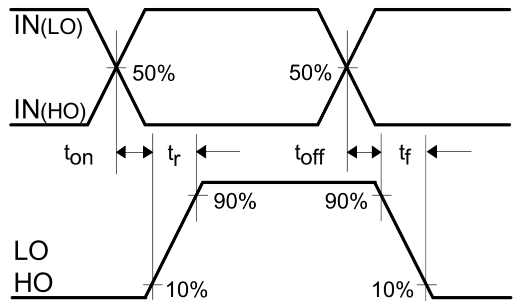



Figure 2. Switching Time Waveform Definitions

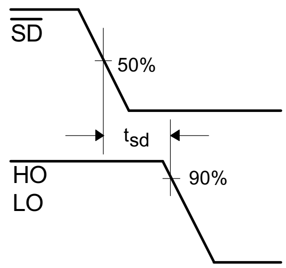



Figure 3. Shutdown Waveform Definitions

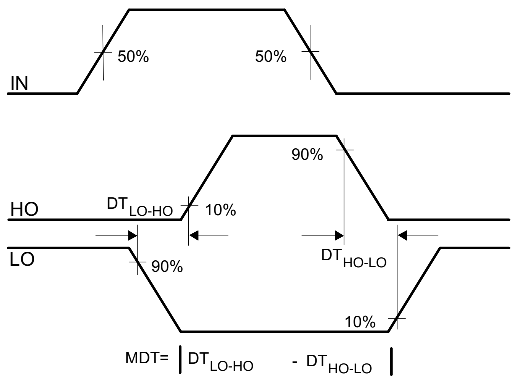



Figure 4. Deadtime Waveform Definitions

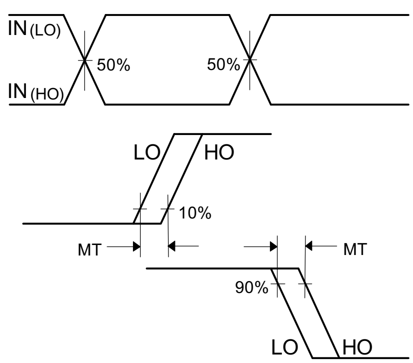



Figure 5. Delay Matching Waveform Definitions

### Tolerant to Negative $V_S$ Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical half bridge circuit is shown in Figure 6; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., Q1 in Figures 7 and 8) switches off, while the phase current is flowing to a load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node $V_{S1}$, swings from the positive DC bus voltage to the negative DC bus voltage.

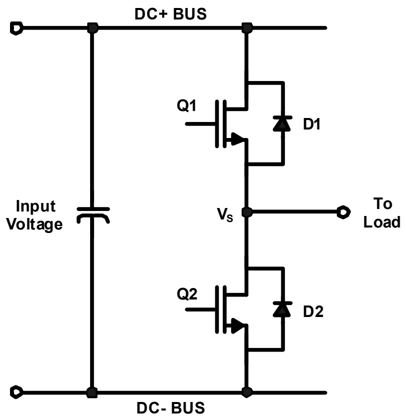



**Figure 6: Half Bridge Circuit**

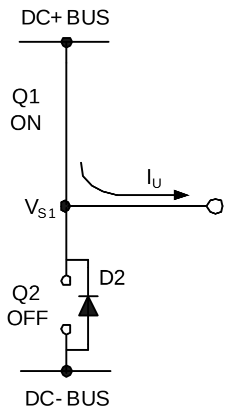



**Figure 7: Q1 conducting**

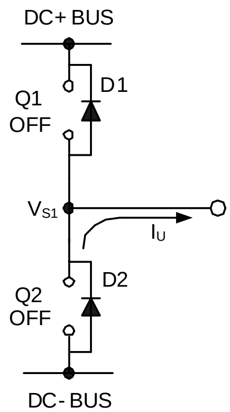



**Figure 8: D2 conducting**

Also when the phase current flows from the load back to the inverter (see Figures 9 and 10), and Q4 switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, $V_{S2}$, swings from the positive DC bus voltage to the negative DC bus voltage.

The circuit shown in Figure 11 depicts a half bridge circuit with parasitic elements shown; Figures 12 and 13 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in $L_C$ and $L_E$ for each switch. When the high-side switch is on, $V_{S1}$ is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current can momentarily flow in the low-side freewheeling diode due to the inductive load connected to $V_{S1,}$ for instance (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between $V_{S1}$ and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the $V_S$ pin).

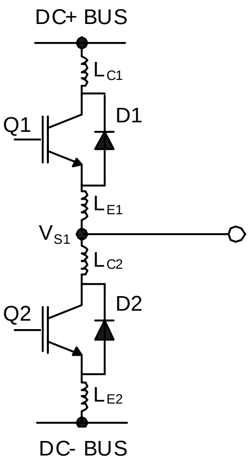



**Figure 9: Parasitic Elements**

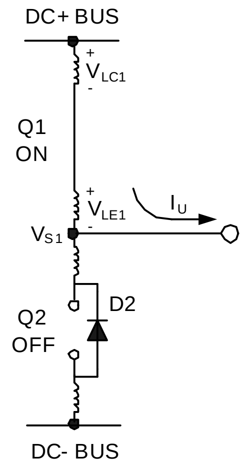



**Figure 10: $V_S$ positive**

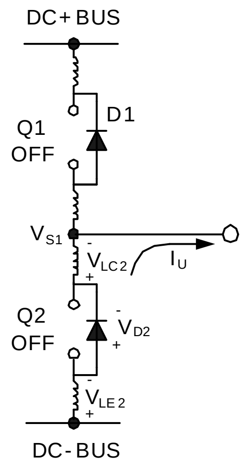



**Figure 11: $V_S$ negative**

In a typical power circuit, dV/dt is typically designed to be in the range of 1-5 V/ns. The negative $V_S$ transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the IRS2184(4)'s robustness can be seen in Figure 14, where there is represented the IRS2184(4) Safe Operating Area at $V_{BS}$=15V based on repetitive negative $V_S$ spikes. A negative $V_S$ transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.

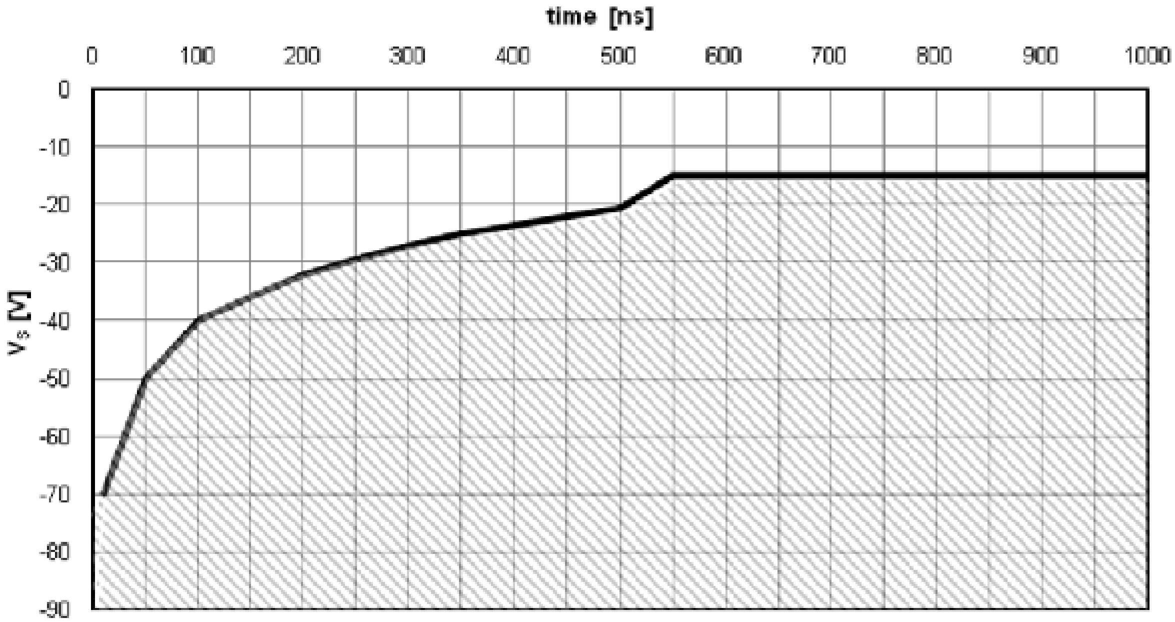



**Figure 12: Negative $V_S$ transient SOA for IRS2184 @ VBS=15V**

Even though the IRS2184(4) has been shown able to handle these large negative $V_S$ transient conditions, it is highly recommended that the circuit designer always limit the negative $V_S$ transients as much as possible by careful PCB layout and component use.

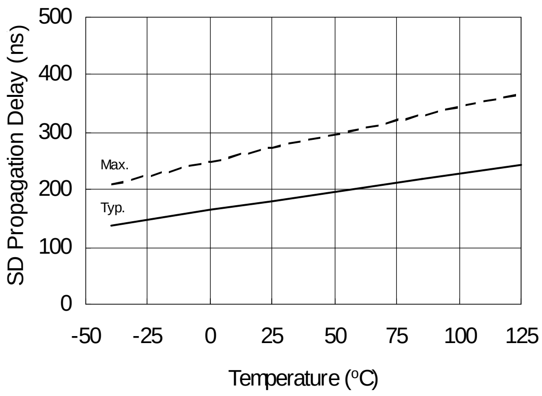



**Figure 13A. Turn-On Propagation Delay Time vs. Temperature**

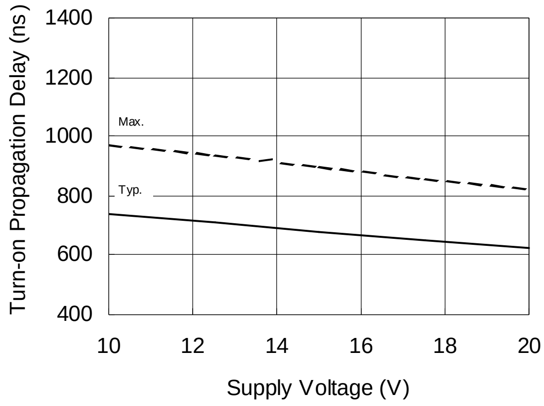



**Figure 13B. Turn-On Propagation Delay Time vs. Supply Voltage**

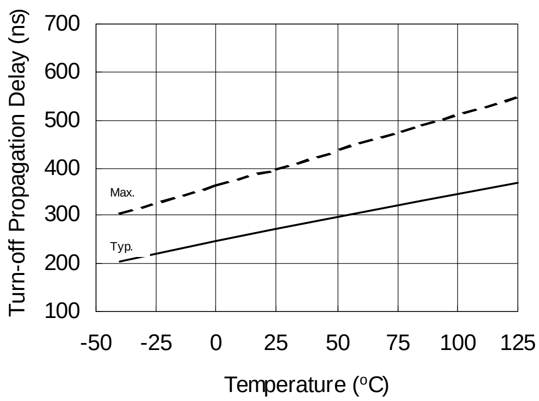



**Figure 14A. Turn-Off Propagation Delay Time vs. Temperature**

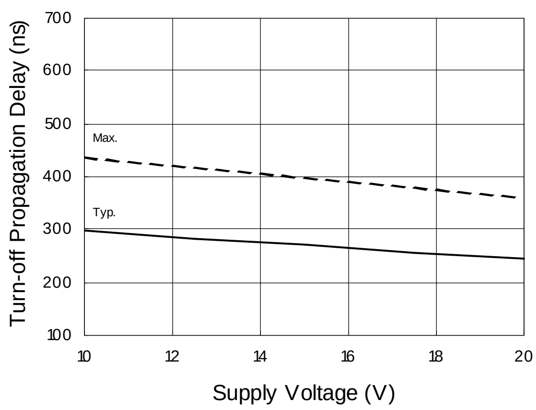



**Figure 14B. Turn-Off Propagation Delay Time vs. Supply Voltage**

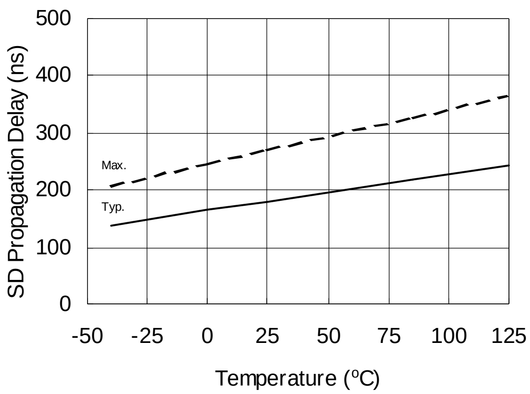



Figure 15A. SD Propagation Delay vs. Temperature

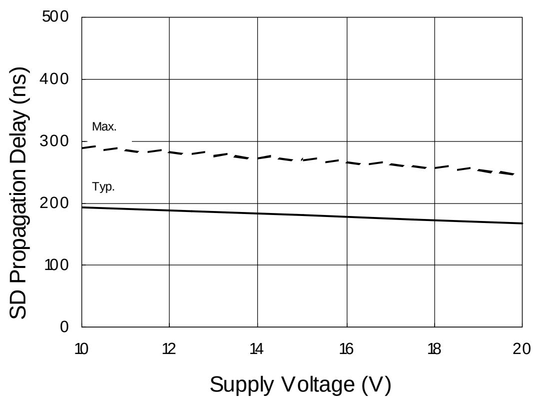



Figure 15B. SD Propagation Delay vs. Supply Voltage

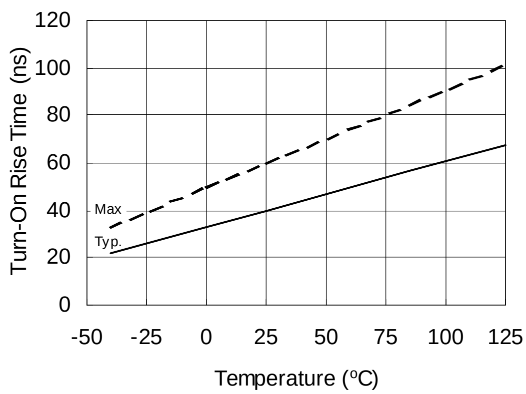



Figure 16A. Turn on Rise Time vs. Temperature

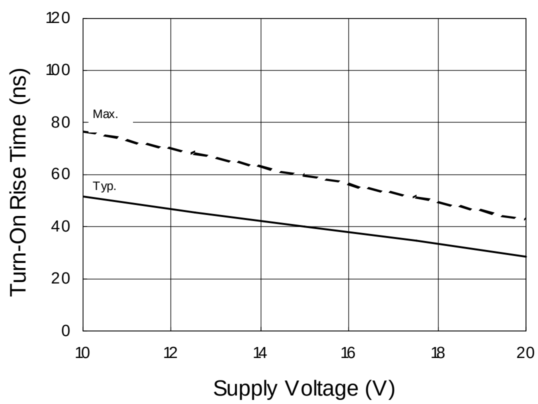



Figure 16B. Turn on Rise Time vs. Supply Voltage

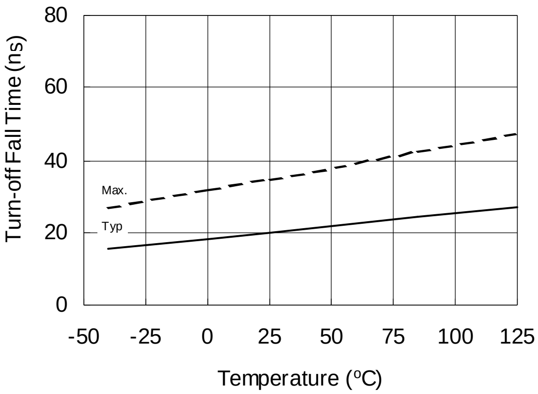



**Figure 17A. Turn-Off Fall Time vs. Temperature**

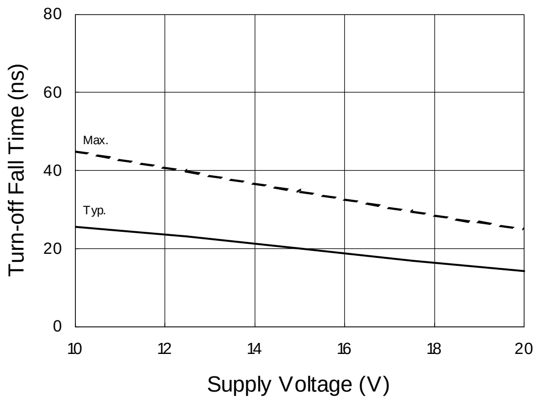



**Figure 17B. Turn-Off Fall Time vs. Supply Voltage**

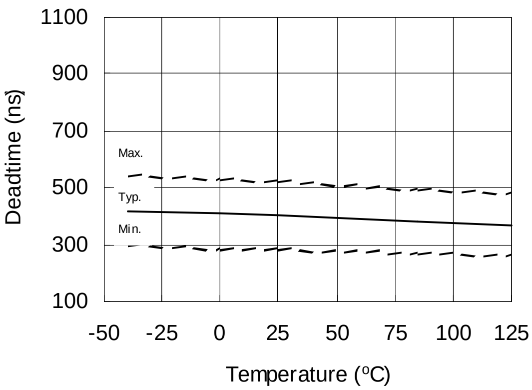



**Figure 18A. Deadtime vs. Temperature**

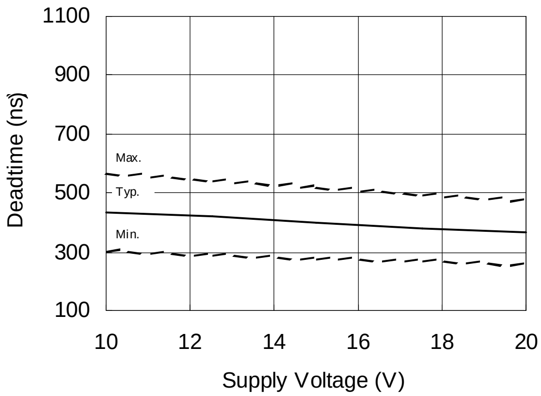



**Figure 18B. Deadtime vs. Supply Voltage**

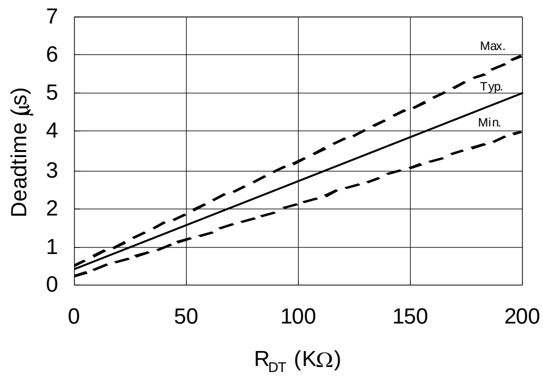



**Figure 18C. Deadtime vs. $R_{DT}$**

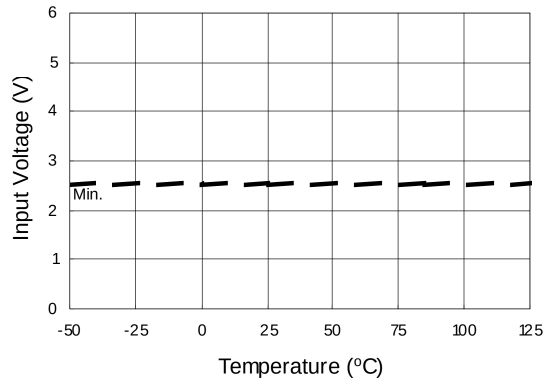



**Figure 19A. Logic "1" Input Voltage vs. Temperature**

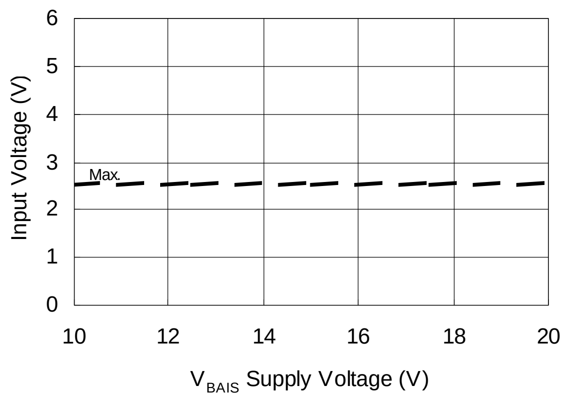



**Figure 19B. Logic "1" Input Voltage vs. Supply Voltage**

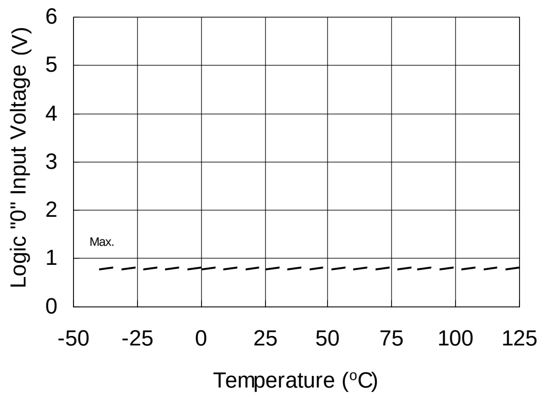



**Figure 20A. Logic "0" Input Voltage vs. Temperature**

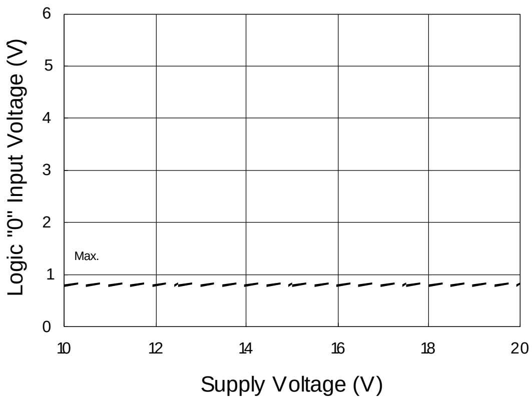



**Figure 20B. Logic "0" Input Voltage vs. Supply Voltage**

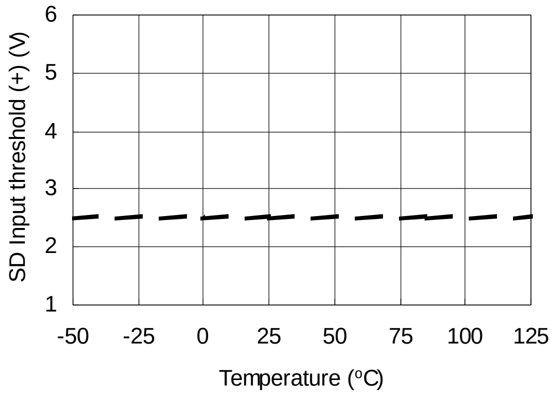



**Figure 21A. SD Input Positive Going Threshold (+) vs. Temperature**

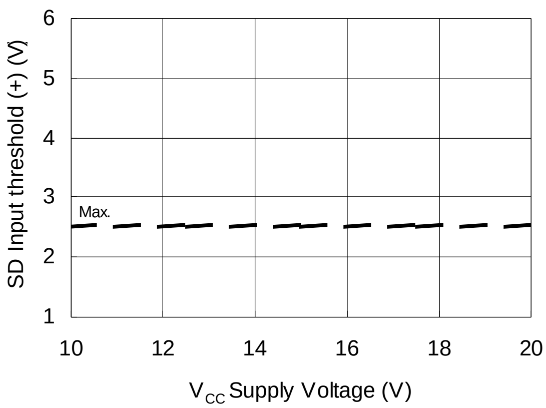



**Figure 21B. SD Input Positive Going Threshold (+) vs. Supply Voltage**

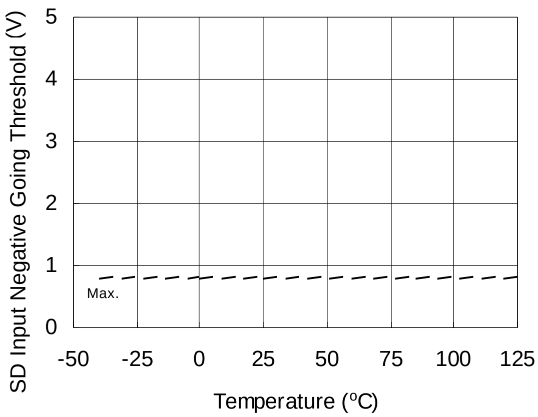



**Figure 22A. SD Input Negative Going Threshold vs. Temperature**

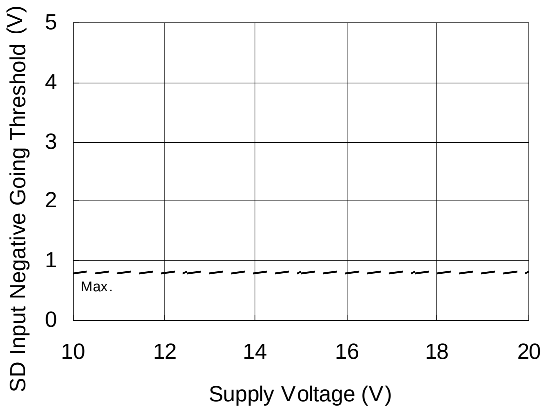



**Figure 22B. SD Input Negative Going Threshold vs. Supply Voltage**

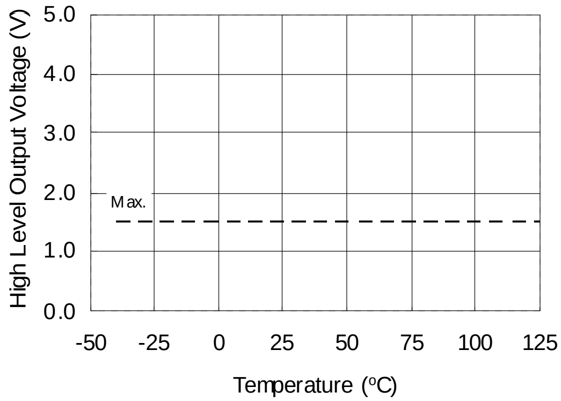



**Figure 23A. High Level Output Voltage vs. Temperature ($I_O$ = 0 mA)**

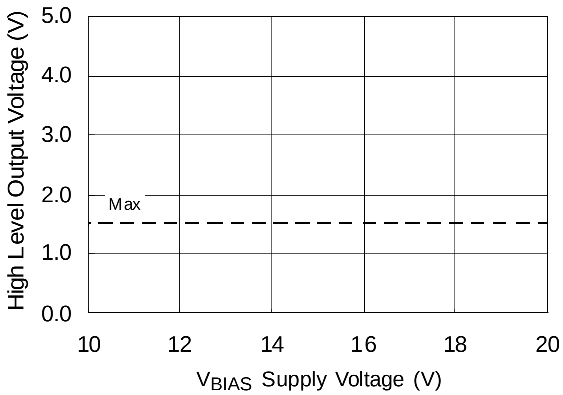



**Figure 23B. High Level Output Voltage vs. Supply Voltage ($I_O$ = 0 mA)**

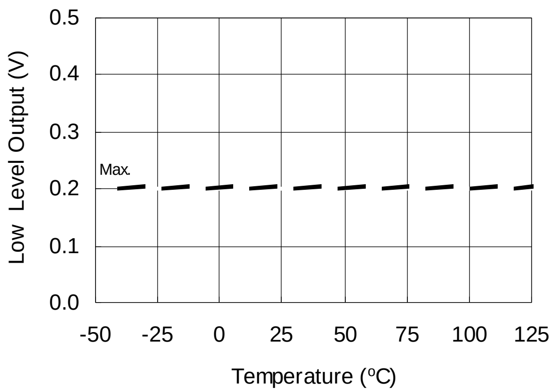



**Figure 24A. Low Level Output vs. Temperature**

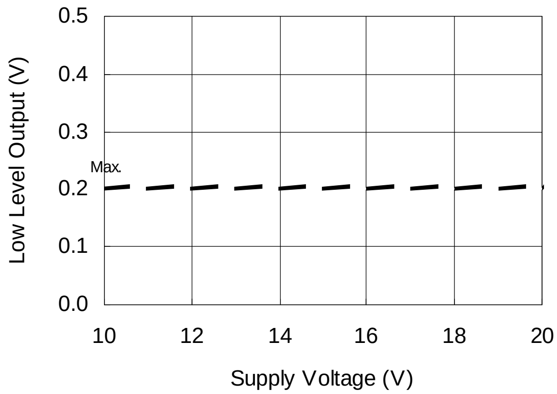



**Figure 24B. Low Level Output vs. Supply Voltage**

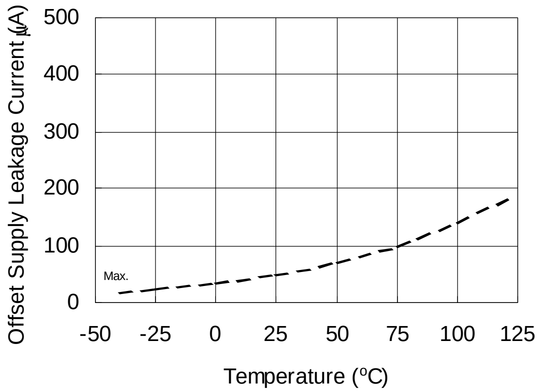



**Figure 25A. Offset Supply Leakage Current vs. Temperature**

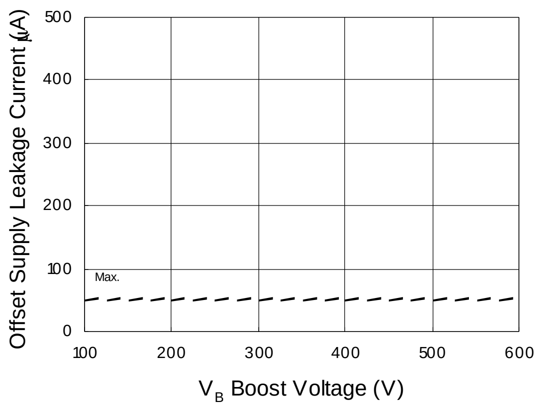



**Figure 25B. Offset Supply Leakage Current vs. $V_B$ Boost Voltage**

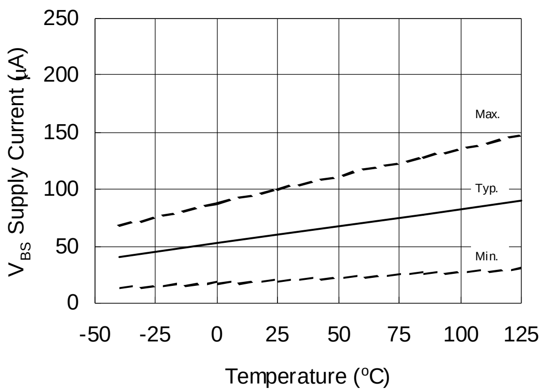



**Figure 26A. $V_{BS}$ Supply Current vs. Temperature**

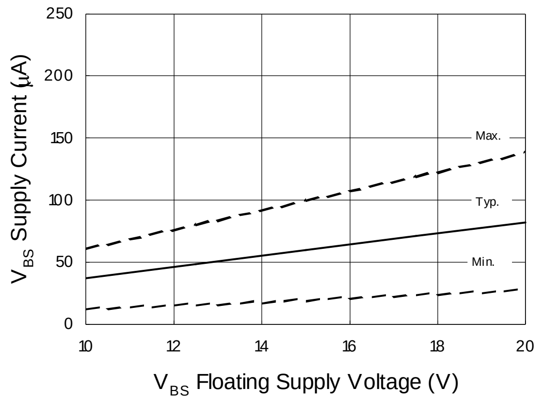



**Figure 26B. $V_{BS}$ Supply Current vs. $V_{BS}$ Supply Voltage**

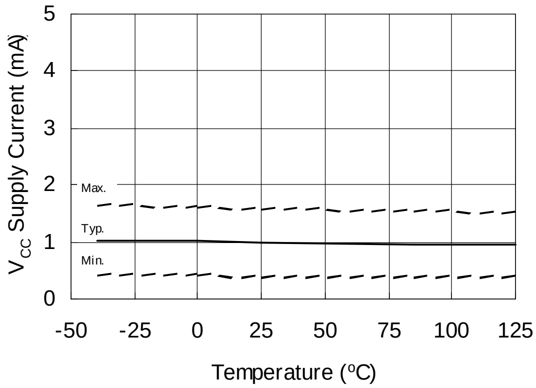



**Figure 27A. $V_{CC}$ Supply Current vs. Temperature**

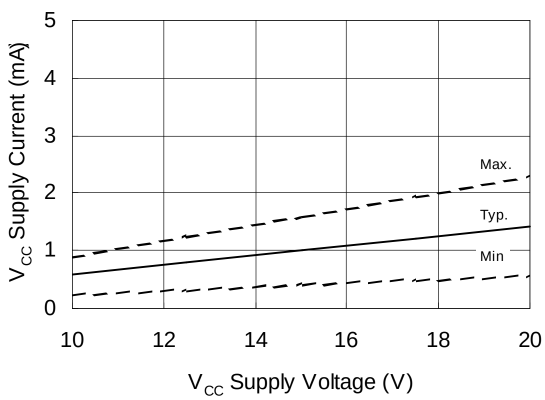



**Figure 27B. $V_{CC}$ Supply Current vs. $V_{CC}$ Supply Voltage**

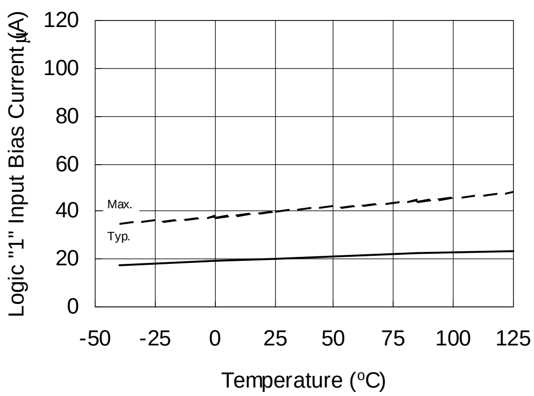



**Figure 28A. Logic "1" Input Bias Current vs. Temperature**

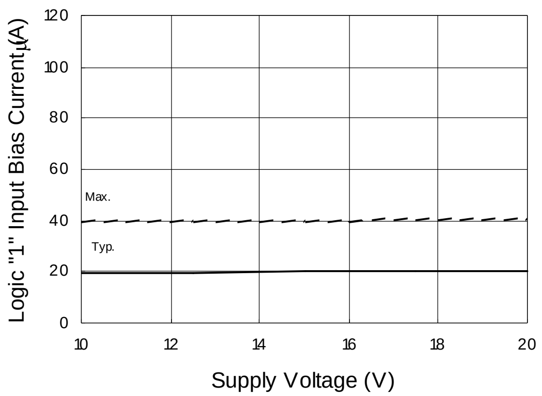



**Figure 28B. Logic "1" Input Bias Current vs. Supply Voltage**

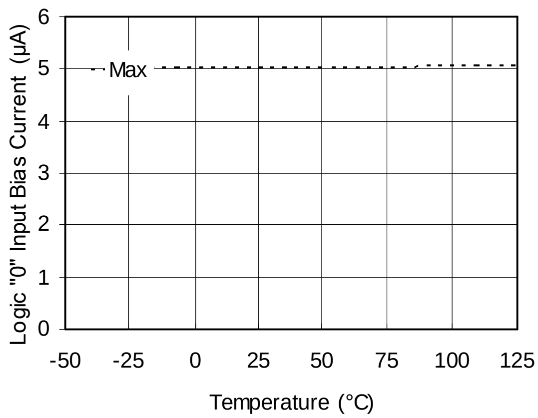



**Figure 29A. Logic "0" Input Bias Current vs. Temperature**

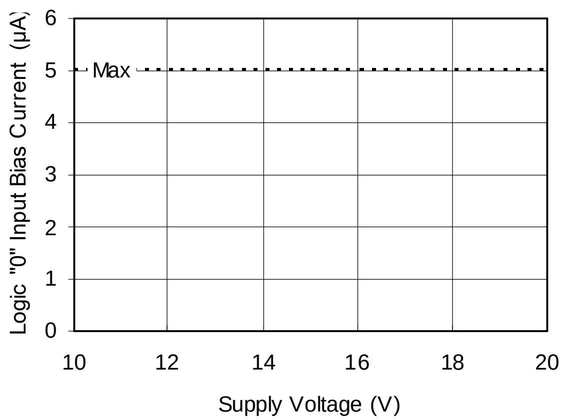



**Figure 29B. Logic "0" Input Bias Current vs. Supply Voltage**

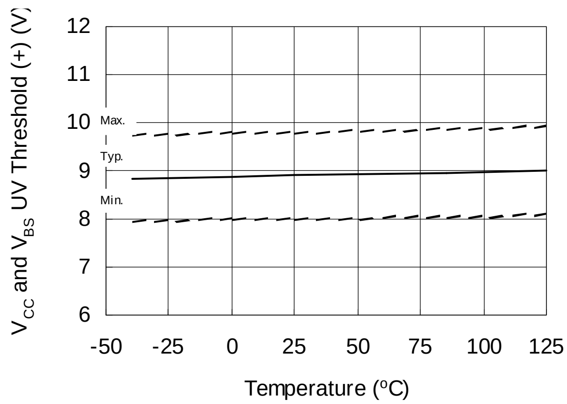



**Figure 30. $V_{CC}$ and $V_{BS}$ Undervoltage Threshold (+) vs. Temperature**

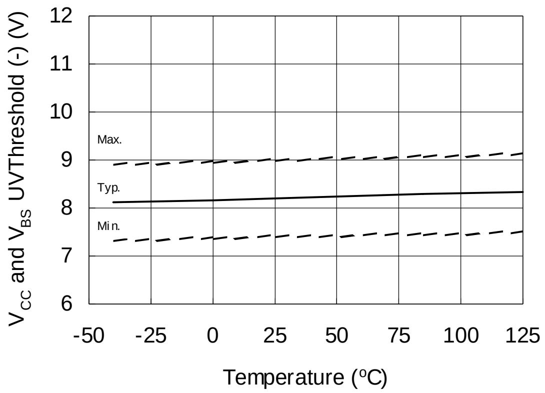



**Figure 31. $V_{CC}$ and $V_{BS}$ Undervoltage Threshold (-) vs. Temperature**

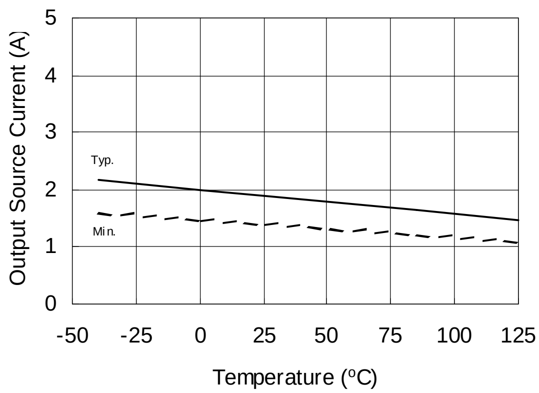



**Figure 32A. Output Source Current vs. Temperature**

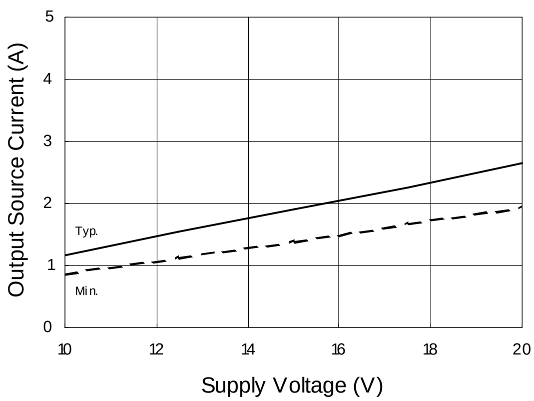



**Figure 32B. Output Source Current vs. Supply Voltage**

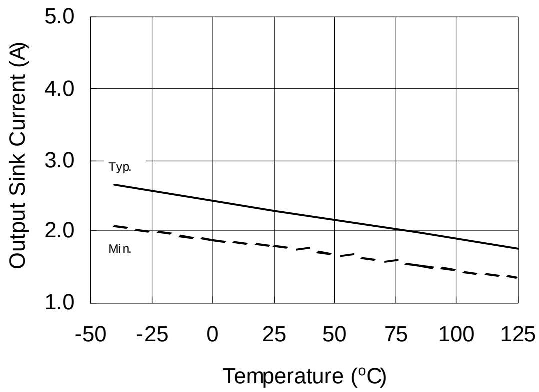



**Figure 33A. Output Sink Current vs. Temperature**

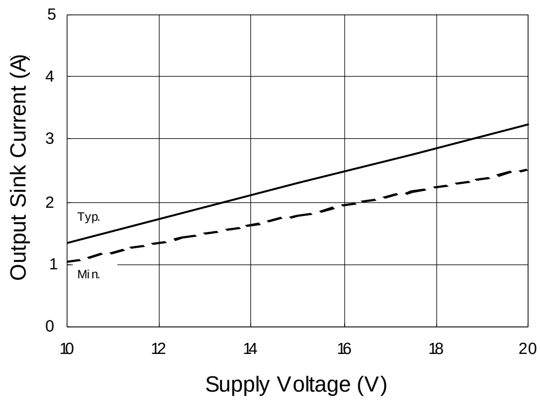



**Figure 33B. Output Sink Current vs. Supply Voltage**

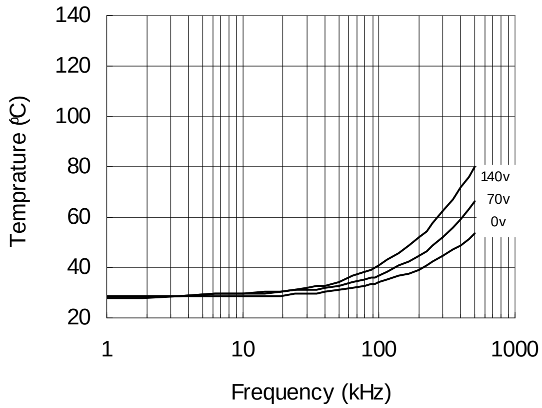



**Figure 34. IRS2184 vs. Frequency (IRFBC20), $R_{gate}$ = 33Ω, $V_{cc}$ = 15V**

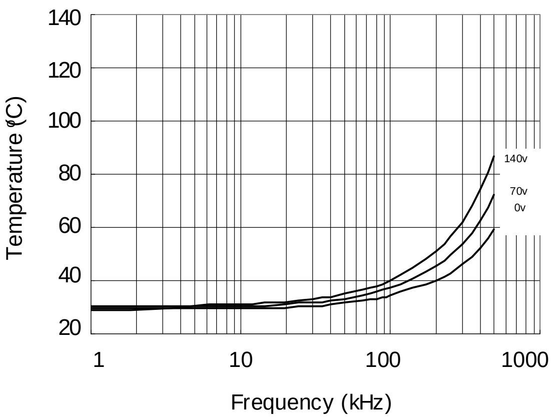



**Figure 35. IRS2184 vs. Frequency (IRFBC30), $R_{gate}$ = 22Ω, $V_{cc}$ = 15V**

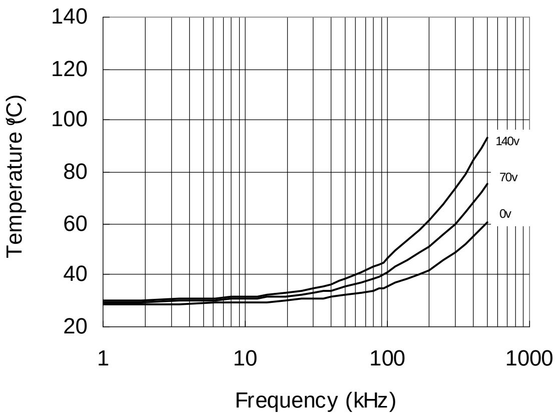



**Figure 36. IRS2184 vs. Frequency (IRFBC40), $R_{gate}$ = 15Ω, $V_{cc}$ = 15V**

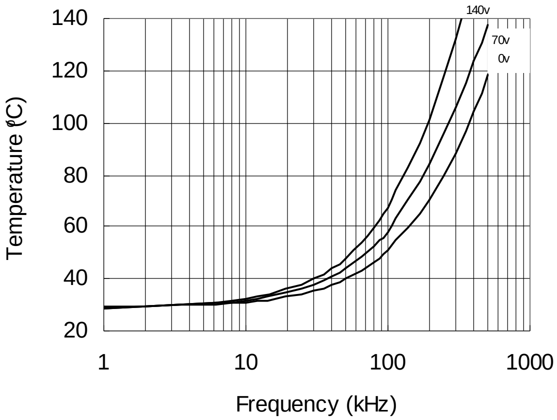



**Figure 37. IRS2184 vs. Frequency (IRFBC50), $R_{gate}$ = 10Ω, $V_{cc}$ = 15V**

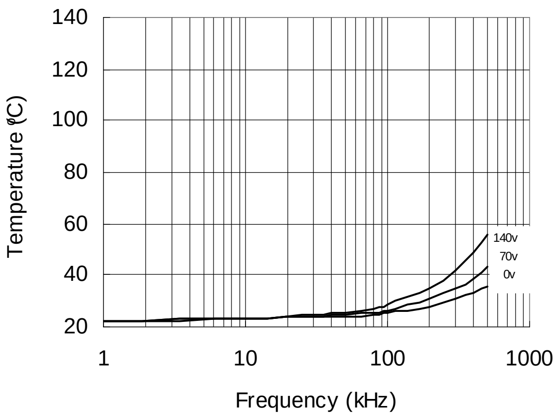



**Figure 38. IRS21844 vs. Frequency (IRFBC20), $R_{gate}$ = 33Ω, $V_{cc}$ = 15V**

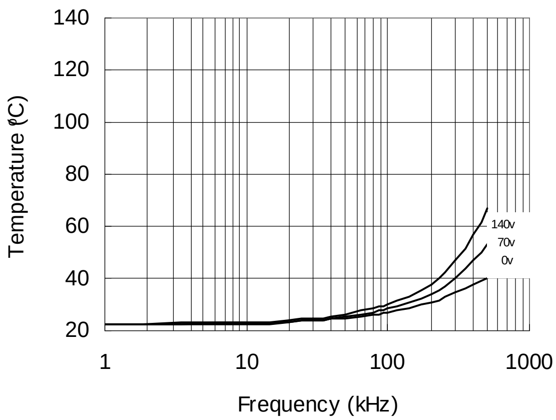



**Figure 39. IRS21844 vs. Frequency (IRFBC30), $R_{gate}$ = 22Ω, $V_{cc}$ = 15V**

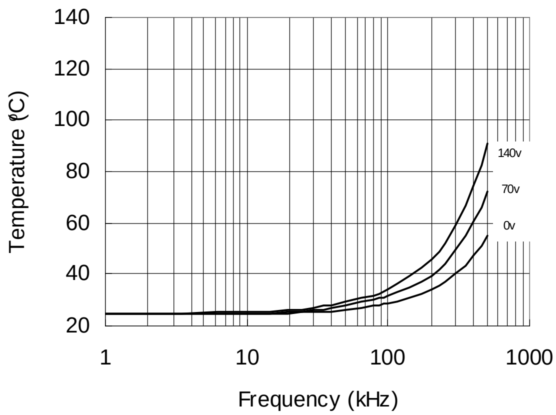



**Figure 40. IRS21844 vs. Frequency (IRFBC40), $R_{gate}$ = 15Ω, $V_{cc}$ = 15V**

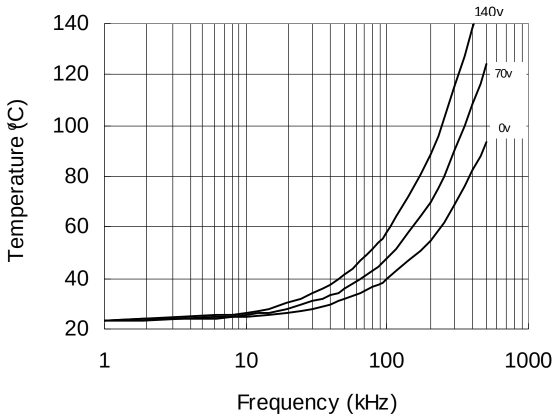



**Figure 41. IRS21844 vs. Frequency (IRFBC50), $R_{gate}$ = 10Ω, $V_{cc}$ = 15V**

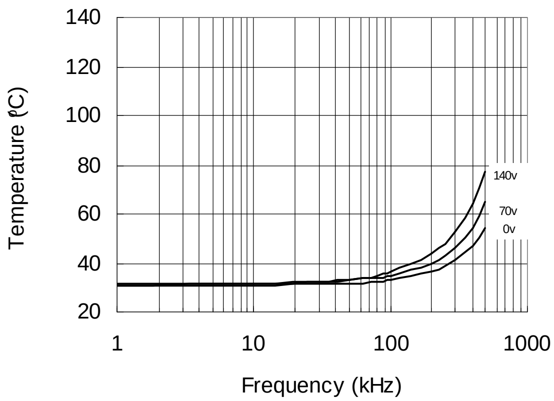



**Figure 42. IRS2184s vs. Frequency (IRFBC20), $R_{gate}$ = 33Ω, $V_{cc}$ = 15V**

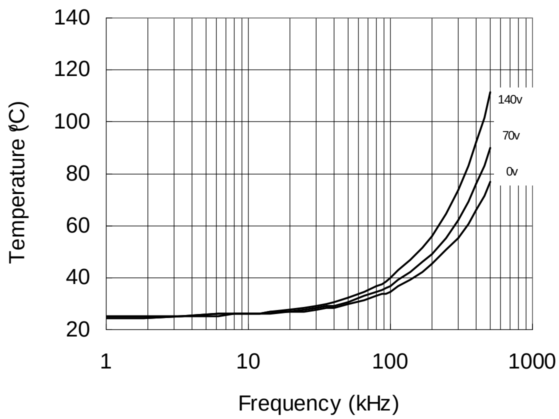



**Figure 43. IRS2184s vs. Frequency (IRFBC30), $R_{gate}$ = 22Ω, $V_{cc}$ = 15V**

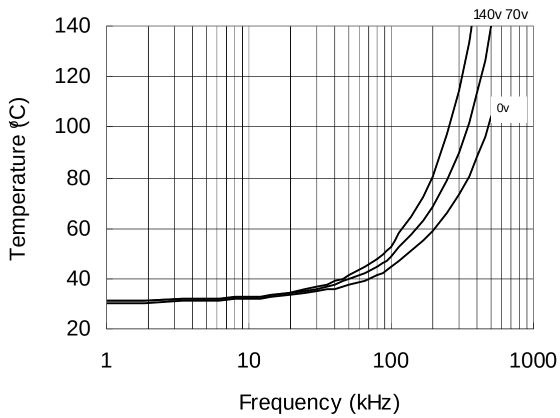



**Figure 44. IRS2184s vs. Frequency (IRFBC40), $R_{gate}$ = 15Ω, $V_{cc}$ = 15V**

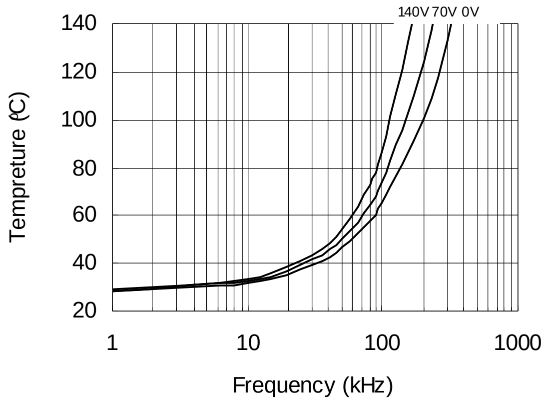



**Figure 45. IRS2184s vs. Frequency (IRFBC50), $R_{gate}$ = 10Ω, $V_{cc}$ = 15V**

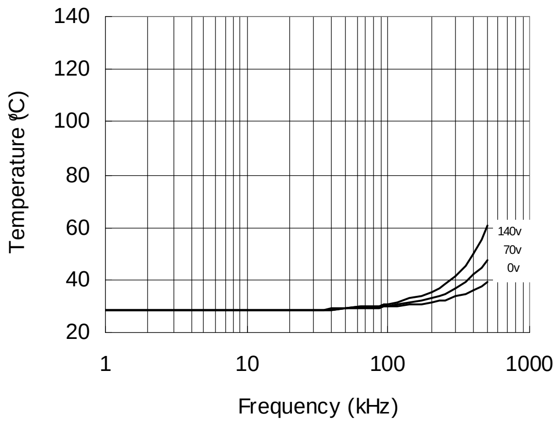



**Figure 46. IRS21844s vs. Frequency (IRFBC20), $R_{gate}$ = 33Ω, $V_{cc}$ = 15V**

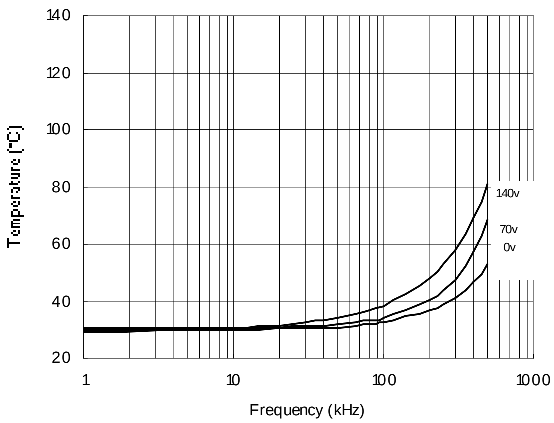



**Figure 47. IRS21844s vs. Frequency (IRFBC30), $R_{gate}$ = 22Ω, $V_{cc}$ = 15V**

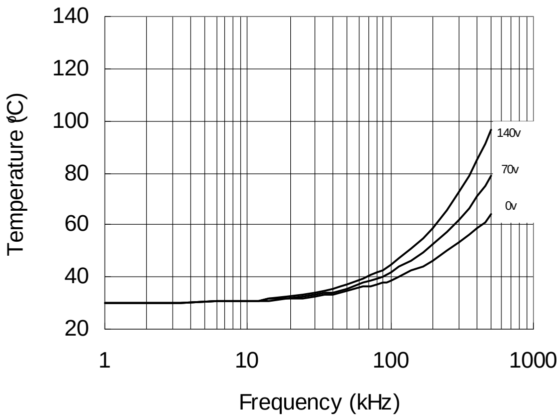



**Figure 48. IRS21844s vs. Frequency (IRFBC40), $R_{gate}$ = 15Ω, $V_{cc}$ = 15V**

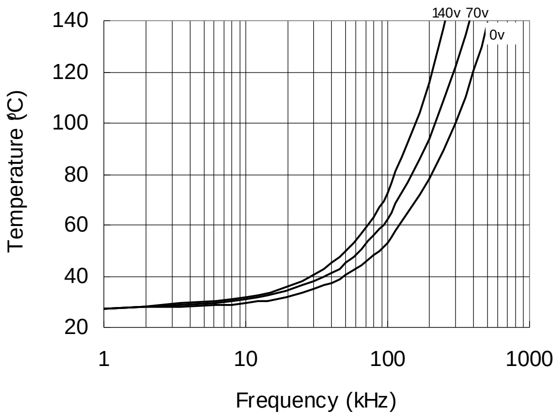
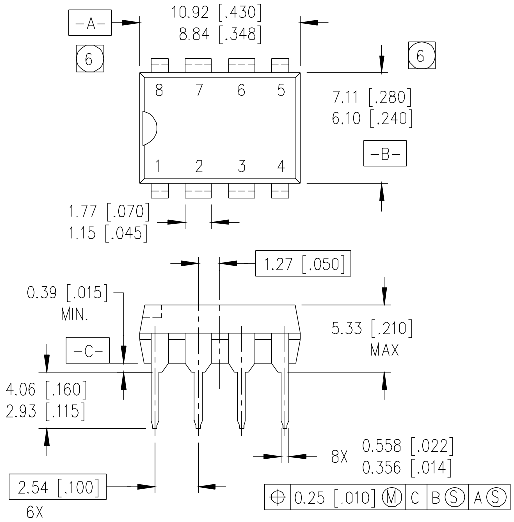
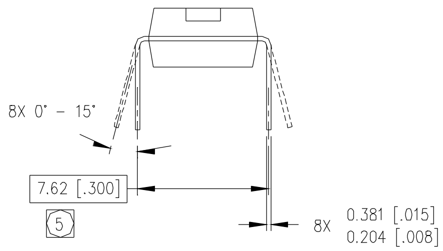



**Figure 49. IRS21844s vs. Frequency (IRFBC50), $R_{gate}$ = 10Ω, $V_{cc}$ = 15V**

## Cast Outlines

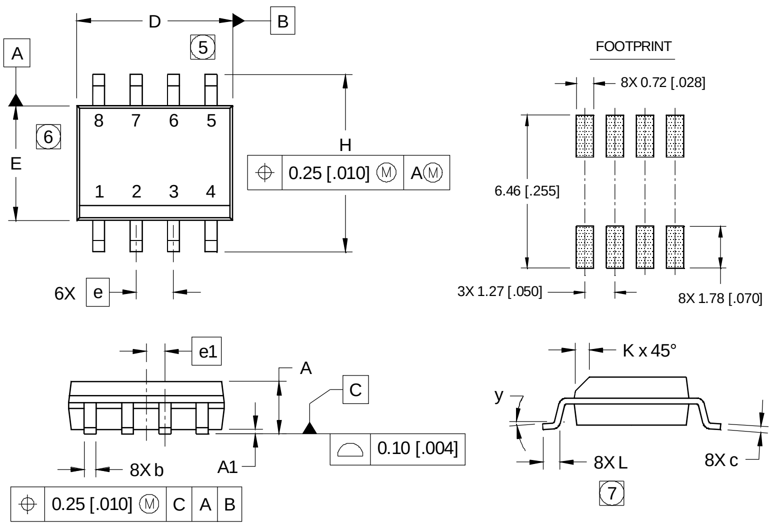



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].




**8-Lead PDIP**

01-6014
01-3003 01 (MS-001AB)

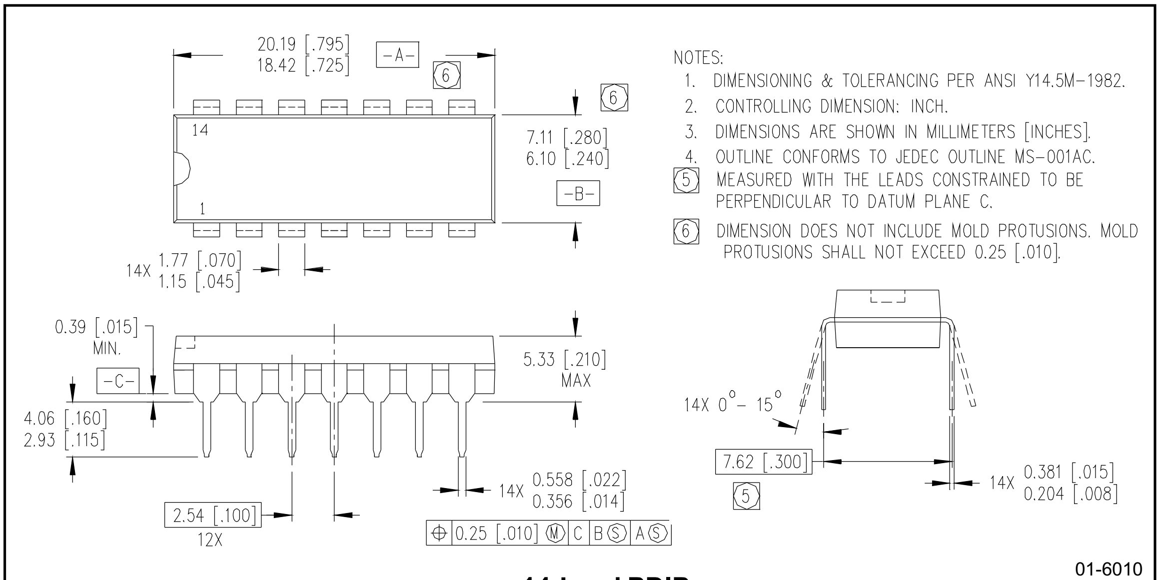



| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

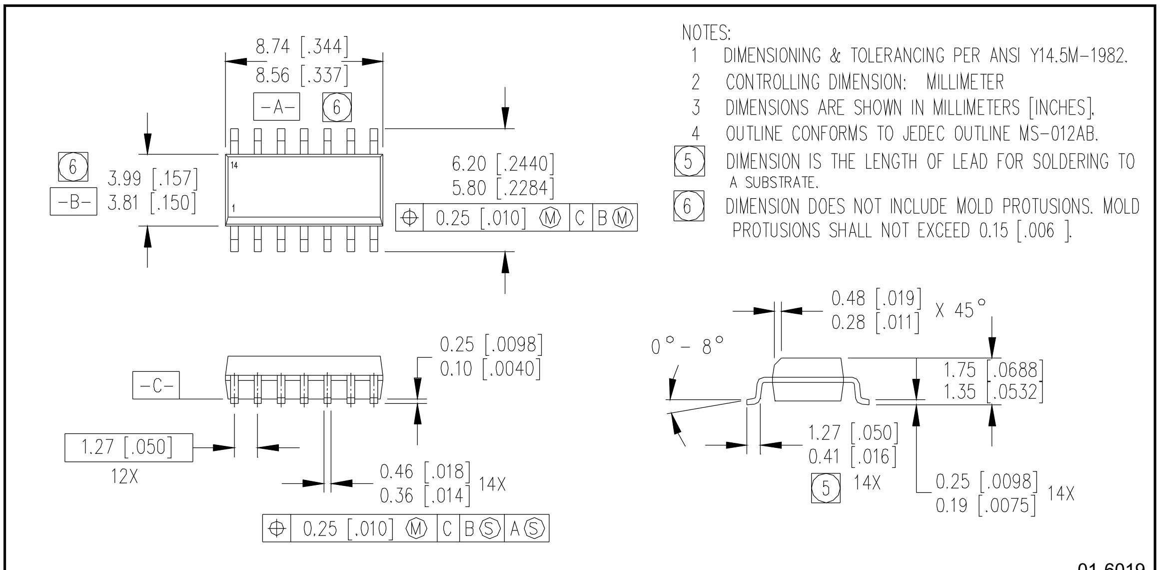
**8-Lead SOIC**

01-6027
01-0021 11 (MS-012AA)




**14-Lead PDIP**

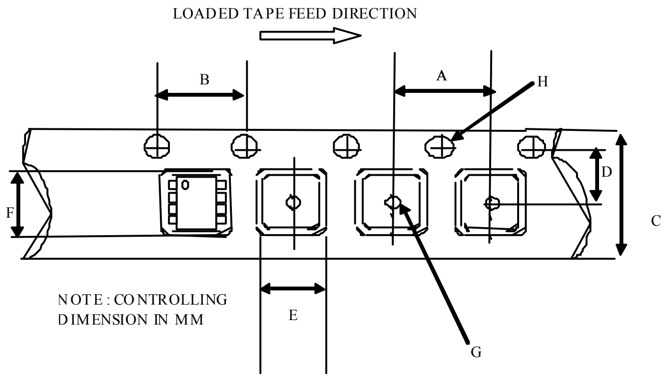
01-6010
01-3002 03 (MS-001AC)




**14-Lead SOIC (narrow body)**

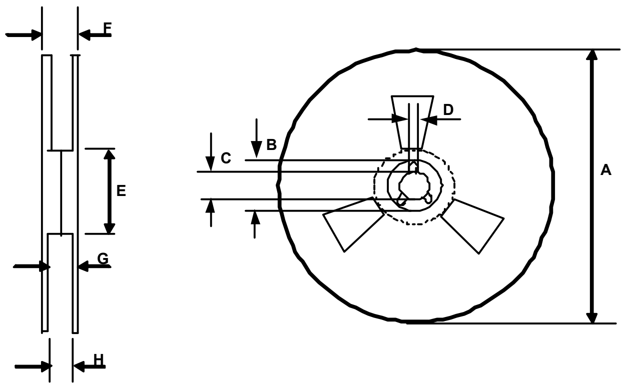
01-6019
01-3063 00 (MS-012AB)

## Tape & Reel
## 8-lead SOIC




CARRIER TAPE DIMENSION FOR 8SOICN

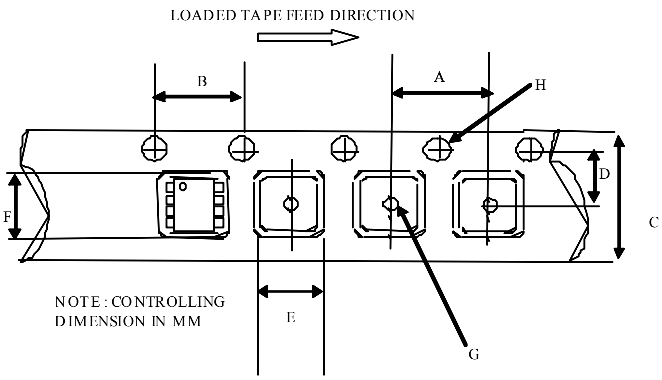
| | Metric | | Imperial | |
|---|---|---|---|---|
| Code | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |




REEL DIMENSIONS FOR 8SOICN

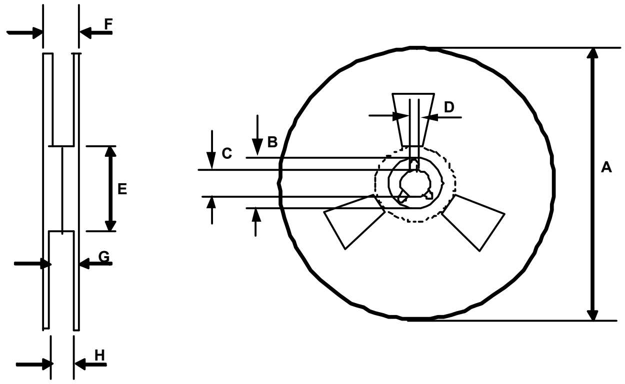
| | Metric | | Imperial | |
|---|---|---|---|---|
| Code | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

## Tape & Reel
## 14-lead SOIC




CARRIER TAPE DIMENSION FOR 14SOICN

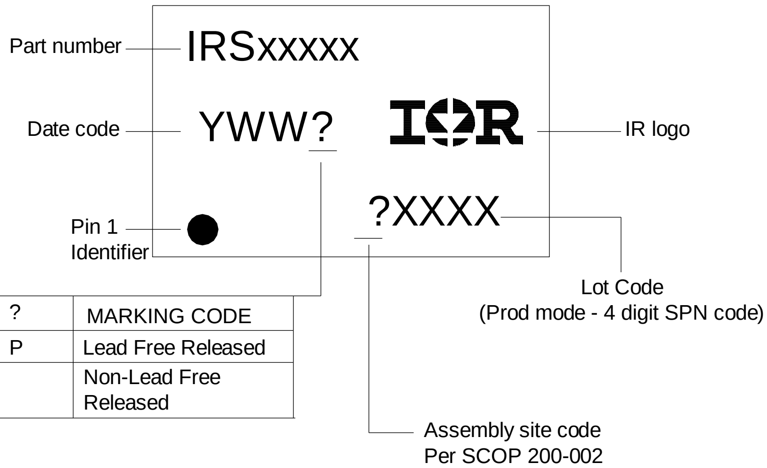
| Code | Metric | | Imperial | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 15.70 | 16.30 | 0.618 | 0.641 |
| D | 7.40 | 7.60 | 0.291 | 0.299 |
| E | 6.40 | 6.60 | 0.252 | 0.260 |
| F | 9.40 | 9.60 | 0.370 | 0.378 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |




REEL DIMENSIONS FOR 14SOICN

| Code | Metric | | Imperial | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 22.40 | n/a | 0.881 |
| G | 18.50 | 21.10 | 0.728 | 0.830 |
| H | 16.40 | 18.40 | 0.645 | 0.724 |

## LEADFREE PART MARKING INFORMATION




| ? | MARKING CODE |
|---|---|
| P | Lead Free Released |
| | Non-Lead Free Released |

## ORDER INFORMATION

8-Lead PDIP IRS2184PbF
8-Lead SOIC IRS2184SPbF
8-Lead SOIC Tape & Reel IRS2184STRPbF

14-Lead PDIP IR2S1844PbF
14-Lead SOIC IRS21844SPbF
14-Lead SOIC Tape & Reel IRS21844STRPbF

International
IOR Rectifier

SOIC8 &14 are MSL2 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

*Data and specifications subject to change without notice. 12/1/2006*

ООО "ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

*Мы предлагаем:*

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

*В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.*

*Конструкторский отдел помогает осуществить:*

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

*Тел: +7 (812) 336 43 04 (многоканальный)*
*Email: org@lifeelectronics.ru*

***www.lifeelectronics.ru***