2.5 MSPS, 24-Bit, 100 dB Sigma-Delta ADC with On-Chip Buffer

AD7760

FEATURES

- 120 dB dynamic range at 78 kHz output data rate
- 100 dB dynamic range at 2.5 MHz output data rate
- 112 dB SNR at 78 kHz output data rate
- 100 dB SNR at 2.5 MHz output data rate
- 2.5 MHz maximum fully filtered output word rate
- Programmable oversampling rate (8× to 256×)
- Fully differential modulator input
- On-chip differential amplifier for signal buffering
- Low-pass finite impulse response (FIR) filter with default or user-programmable coefficients
- Modulator output mode
- Overrange alert bit
- Digital offset and gain correction registers
- Filter bypass modes
- Low power and power-down modes
- Synchronization of multiple devices via $\overline{\text{SYNC}}$ pin

APPLICATIONS

- Data acquisition systems
- Vibration analysis
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

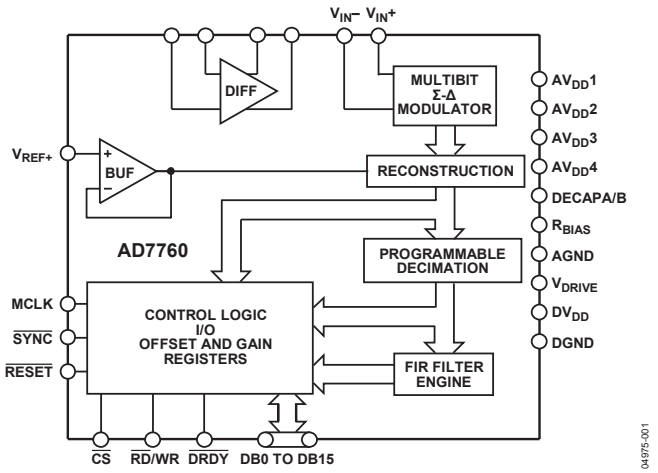

Figure 1.

GENERAL DESCRIPTION

The AD7760 is a high performance, 24-bit Σ-Δ analog-to-digital converter (ADC). It combines wide input bandwidth and high speed with the benefits of Σ-Δ conversion to achieve a performance of 100 dB SNR at 2.5 MSPS, making it ideal for high speed data acquisition. Wide dynamic range combined with significantly reduced antialiasing requirements simplify the design process. An integrated buffer to drive the reference, a differential amplifier for signal buffering and level shifting, an overrange flag, internal gain and offset registers, and a low-pass digital FIR filter make the AD7760 a compact, highly integrated data acquisition device requiring minimal peripheral component selection. In addition, the device offers programmable decimation rates, and the digital FIR filter can be adjusted if the default characteristics are not appropriate for the application. The AD7760 is ideal for applications demanding high SNR without a complex front-end signal processing design.

The differential input is sampled at up to 40 MSPS by an analog modulator. The modulator output is processed by a series of low-pass filters, with the final filter having default or user-programmable coefficients. The sample rate, filter corner frequencies, and output word rate are set by a combination of the external clock frequency and the configuration registers of the AD7760.

The reference voltage supplied to the AD7760 determines the analog input range. With a 4 V reference, the analog input range is ±3.2 V differential biased around a common mode of 2 V. This common-mode biasing can be achieved using the on-chip differential amplifier, further reducing the external signal conditioning requirements.

The AD7760 is available in an exposed paddle, 64-lead TQFP and is specified over the industrial temperature range from −40°C to +85°C.

Table 1. Related Devices

Part No.	Description
AD7762	24-bit, 625 kSPS, 109 dB, Σ-Δ parallel interface
AD7763	24-bit, 625 kSPS, 109 dB, Σ-Δ serial interface

Rev. A
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REVISION HISTORY

8/06—Rev. 0 to Rev. A

Updated Package Option ..... Universal
Change to Features 1
Changes to Specifications 4
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Changes to Terminology Section 11
Added Figure 36 Through Figure 39 17
Added Modulator Data Output Mode Section 19
Added Figure 41 Through Figure 47 19
Added Modulator Data Output Mode Interface Section 20
Changes to Reading Data Section 22
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Added Exposed Paddle Section 29
Change to Control Register 2—Address 0x0002 Section 33
Changes to Status Register (Read Only) Section 34

7/05—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD}1 = DV_{DD} = V_{DRIVE}$ = 2.5 V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4$ = 5 V, V_{REF+} = 4.096 V, MCLK amplitude = 5 V, T_A = 25°C, normal mode, using the on-chip amplifier with components as shown in Table 8, unless otherwise noted.[1]

Table 2.

Parameter	Test Conditions/Comments	Specification	Unit
DYNAMIC PERFORMANCE			
Decimate by 256	MCLK = 40 MHz, ODR = 78 kHz, f_{IN} = 1 kHz		
Dynamic Range	Modulator inputs shorted	119	dB min
		120.5	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dBFS	112	dB typ
	Input amplitude = −60 dBFS	59	dB typ
Spurious-Free Dynamic Range (SFDR)	Nonharmonic, input amplitude = −6 dBFS	126	dBc typ
	Input amplitude = −60 dBFS	77	dBc typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dBFS	−105	dB typ
	Input amplitude = −6 dBFS	−106	dB typ
	Input amplitude = −60 dBFS	−75	dB typ
Decimate by 32	MCLK = 40 MHz, ODR = 625 kHz, f_{IN} =100 kHz		
Dynamic Range	Modulator inputs shorted	108	dB min
		109.5	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dBFS	107	dB typ
Spurious-Free Dynamic Range (SFDR)	Nonharmonic, input amplitude = −6 dBFS	120	dBc typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dBFS	−105	dB typ
	Input amplitude = −6 dBFS	−106	dB typ
Decimate by 8	MCLK = 40 MHz, ODR = 2.5 MHz		
Dynamic Range	Modulator inputs shorted	99	dB min
		100.5	dB typ
Signal-to-Noise Ratio (SNR)[2]	f_{IN} = 1 kHz, input amplitude = −0.5 dBFS	100	dB typ
	f_{IN} = 100 kHz, input amplitude = −0.5 dBFS	99	dB typ
	f_{IN} = 1 MHz, input amplitude = −0.5 dBFS	98	dB typ
Spurious-Free Dynamic Range (SFDR)	Nonharmonic, f_{IN} = 100 kHz, input amplitude = −6 dBFS	120	dBc typ
	Nonharmonic, f_{IN} = 1 MHz, input amplitude = −6 dBFS	114	dBc typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dBFS, f_{IN} = 100 kHz	−103	dB typ
	Input amplitude = −6 dBFS, f_{IN} = 100 kHz	−102	dB typ
IMD Second Order	f_{IN} A = 989.95 kHz, f_{IN} B = 999.95 kHz	−115	dB typ
IMD Third Order	f_{IN} A = 989.95 kHz, f_{IN} B = 999.95 kHz	−89	dB typ
DC ACCURACY			
Resolution		24	Bits
Differential Nonlinearity	Guaranteed monotonic to 24 bits		
Integral Nonlinearity		0.00076	% typ
Zero Error		0.014	% typ
		0.02	% max
Gain Error		0.016	% typ
Zero Error Drift		0.00001	% FS/°C typ
Gain Error Drift		0.0002	% FS/°C typ
DIGITAL FILTER RESPONSE			
Decimate by 8			
Group Delay	MCLK = 40 MHz	12	µs typ
Decimate by 32			
Group Delay	MCLK = 40 MHz	47	µs typ
Decimate by 256			
Group Delay	MCLK = 40 MHz	358	µs typ

Parameter	Test Conditions/Comments	Specification	Unit
ANALOG INPUT			
Differential Input Voltage	$V_{IN}(+) - V_{IN}(-)$, V_{REF} = 2.5 V	±2	V p-p
	$V_{IN}(+) - V_{IN}(-)$, V_{REF} = 4.096 V	±3.25	V p-p
Input Capacitance	At internal buffer inputs	5	pF typ
	At modulator inputs	55	pF typ
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage	$V_{DD}3$ = 3.3 V ± 5%	+2.5	V max
	$V_{DD}3$ = 5 V ± 5%	+4.096	V max
V_{REF} Input DC Leakage Current		±6	µA max
V_{REF} Input Capacitance		5	pF max
POWER DISSIPATION			
Total Power Dissipation	Normal mode	958	mW max
	Low power mode	661	mW max
Standby Mode	Clock stopped	6.35	mW max
POWER REQUIREMENTS			
$AV_{DD}1$ (Modulator Supply)	±5%	+2.5	V
$AV_{DD}2$ (General Supply)	±5%	+5	V
$AV_{DD}3$ (Differential Amplifier Supply)		+3.15/+5.25	V min/max
$AV_{DD}4$ (Reference Buffer Supply)		+3.15/+5.25	V min/max
DV_{DD}	±5%	+2.5	V
V_{DRIVE}		+1.65/+2.7	V min/max
Normal Mode			
$AI_{DD}1$ (Modulator)		49/51	mA typ/max
$AI_{DD}2$ (General)[3]		40/42	mA typ/max
$AI_{DD}4$ (Reference Buffer)	$AV_{DD}4$ = 5 V	34/36	mA typ/max
Low Power Mode			
$AI_{DD}1$ (Modulator)		26/28	mA typ/max
$AI_{DD}2$ (General)[3]		20/23	mA typ/max
$AI_{DD}4$ (Reference Buffer)	$AV_{DD}4$ = 5 V	9/10	mA typ/max
$AI_{DD}3$ (Differential Amplifier)	$AV_{DD}3$ = 5 V, both modes	41/44	mA typ/max
DI_{DD}	Both modes	63/70	mA typ/max
DIGITAL I/O			
MCLK Input Amplitude[4]		5	V typ
Input Capacitance		7.3	pF typ
Input Leakage Current		±5	µA max
Three-State Leakage Current (D15:D0)		±5	µA max
V_{INH}		0.7 × V_{DRIVE}	V min
V_{INL}		0.3 × V_{DRIVE}	V max
V_{OH}[5]		1.5	V min
V_{OH}[6]		2.4	V typ
V_{OL}[4]		0.1	V max

[1] See the Terminology section.
[2] SNR specifications in decibels are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[3] Current scales with ICLK frequency. See the Typical Performance Characteristics section.
[4] Although the AD7760 can function with an MCLK amplitude of less than 5 V, this is the recommended amplitude to achieve the performance as stated.
[5] Tested using the minimum V_{DRIVE} voltage of 1.65 V with a 400 µA load current.
[6] Tested using V_{DRIVE} = 2.5 V with a 400 µA load current.

TIMING SPECIFICATIONS

$AV_{DD}1 = DV_{DD} = V_{DRIVE} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $T_A = 25°C$, normal mode, unless otherwise noted.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MCLK}	1	MHz min	Applied master clock frequency
	40	MHz max	
f_{ICLK}	500	kHz min	Internal modulator clock derived from MCLK
	20	MHz max	
t_1[1, 2]	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ pulse width
t_2	10	ns min	$\overline{DRDY}$ falling edge to $\overline{CS}$ falling edge
t_3	3	ns min	$\overline{RD}$/WR setup time to $\overline{CS}$ falling edge
t_4	$(0.5 \times t_{ICLK}) + 16$ ns	max	Data access time
t_5	t_{ICLK}	min	$\overline{CS}$ low read pulse width
t_6	t_{ICLK}	min	$\overline{CS}$ high pulse width between reads
t_7	3	ns min	$\overline{RD}$/WR hold time to $\overline{CS}$ rising edge
t_8	11	ns max	Bus relinquish time
t_9[2]	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ high period
t_{10}[2]	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ low period
t_{11}	$(0.5 \times t_{ICLK}) + 16$ ns	max	Data access time
t_{12}[3, 4]	23	ns min	Data valid prior to $\overline{DRDY}$ rising edge
t_{13}[3, 4]	19	ns min	Data valid after $\overline{DRDY}$ rising edge
t_{14}	11	ns max	Bus relinquish time
t_{15}	$4 \times t_{ICLK}$	min	$\overline{CS}$ low write pulse width
t_{16}	$4 \times t_{ICLK}$	min	$\overline{CS}$ high period between address and data
t_{17}	5	ns min	Data setup time
t_{18}	0	ns min	Data hold time
t_{19}[4, 5]	23	ns min	Data valid prior to MCLK falling edge while $\overline{DRDY}$ is logic low
t_{20}[4, 5]	19	ns min	Data valid after MCLK falling edge while $\overline{DRDY}$ is logic low

[1] $t_{ICLK} = 1/f_{ICLK}$.
[2] When ICLK = MCLK, $\overline{DRDY}$ pulse width depends on the mark-space ratio of applied MCLK.
[3] Valid when using the modulator output mode with $\overline{CDIV} = 1$.
[4] See the Modulator Data Output Mode section for timing diagrams.
[5] Valid when using the modulator output mode with $\overline{CDIV} = 0$.

TIMING DIAGRAMS

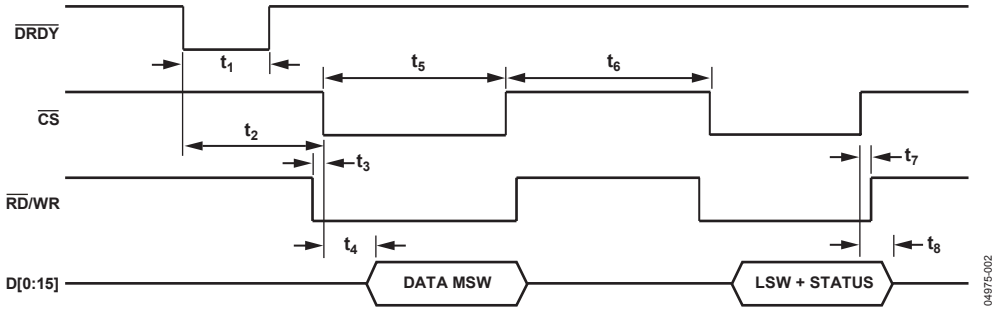

Figure 2. Filtered Output—Parallel Interface Timing Diagram

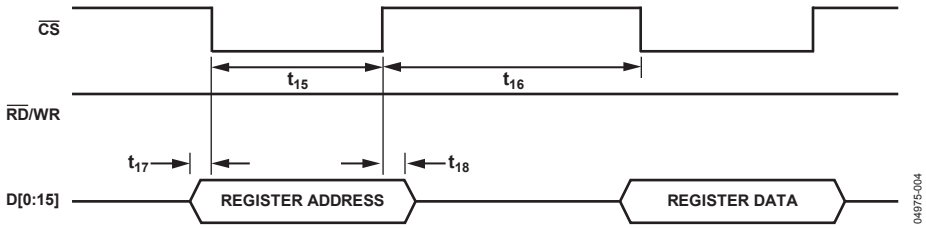

Figure 3. AD7760 Register Write

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameters	Rating
$AV_{DD}1$ to GND	−0.3 V to +3 V
$AV_{DD}2$:$AV_{DD}4$ to GND	−0.3 V to +6 V
DV_{DD} to GND	−0.3 V to +3 V
V_{DRIVE} to GND	−0.3 V to +3 V
V_{IN}+, V_{IN}− to GND[1]	−0.3 V to +6 V
$V_{IN}A$+, $V_{IN}A$− to GND[1]	−0.3 V to +6 V
Digital Input Voltage to GND[2]	−0.3 V to DV_{DD} + 0.3 V
MCLK to MCLKGND	−0.3 V to +6 V
V_{REF+} to GND[3]	−0.3 V to $AV_{DD}4$ + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies[4]	±10 mA
Operating Temperature Range	
Commercial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TQFP Exposed Paddle Package	
θ_{JA} Thermal Impedance	92.7°C/W
θ_{JC} Thermal Impedance	5.1°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	600 V

[1] Absolute maximum voltage for V_{IN}−, V_{IN}+ and V_{INA}−, V_{INA}+ is 6.0 V or $AV_{DD}3$ + 0.3 V, whichever is lower.
[2] Absolute maximum voltage on digital inputs is 3.0 V or DV_{DD} + 0.3 V, whichever is lower.
[3] Absolute maximum voltage on V_{REF+} input is 6.0 V or $AV_{DD}4$ + 0.3 V, whichever is lower.
[4] Transient currents of up to 200 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

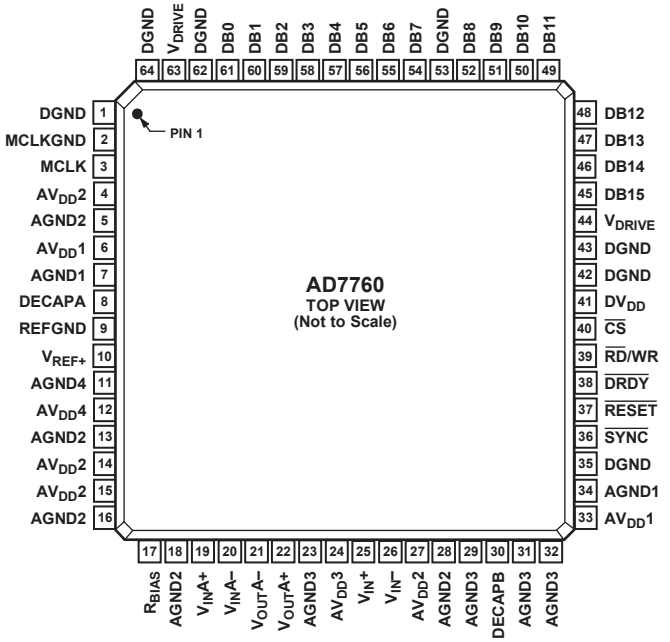

Figure 4. 64-Lead TQFP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
6, 33	$AV_{DD}1$	2.5 V Power Supply for Modulator. These pins should be decoupled to AGND1 (Pin 7 and Pin 34, respectively) with 100 nF and 10 µF capacitors on each pin. See the Decoupling and Layout Recommendations section for details.
4, 14, 15, 27	$AV_{DD}2$	5 V Power Supply. These pins should be decoupled to AGND2 (Pin 5 and Pin 13, with 100 nF capacitors on each of Pin 4, Pin 14, and Pin 15). Pin 27 should be connected to Pin 14 via a 15 nH inductor. See the Decoupling and Layout Recommendations section for details.
24	$AV_{DD}3$	3.3 V to 5 V Power Supply for Differential Amplifier. This pin should be decoupled to AGND3 (Pin 23) with a 100 nF capacitor. See the Decoupling and Layout Recommendations section for details.
12	$AV_{DD}4$	3.3 V to 5 V Power Supply for Reference Buffer. This pin should be decoupled to Pin 9 with a 10 nF capacitor in series with a 10 Ω resistor.
7, 34	AGND1	Power Supply Ground for Analog Circuitry Powered by $AV_{DD}1$.
5, 13, 16, 18, 28	AGND2	Power Supply Ground for Analog Circuitry Powered by $AV_{DD}2$.
23, 29, 31, 32	AGND3	Power Supply Ground for Analog Circuitry Powered by $AV_{DD}3$.
11	AGND4	Power Supply Ground for Analog Circuitry Powered by $AV_{DD}4$.
9	REFGND	Reference Ground. Ground connection for the reference voltage.
41	DV_{DD}	2.5 V Power Supply for Digital Circuitry and FIR Filter. This pin should be decoupled to DGND with a 100 nF capacitor.
44, 63	V_{DRIVE}	Logic Power Supply Input, 1.8 V to 2.5 V. The voltage supplied at these pins determines the operating voltage of the logic interface. Both of these pins must be connected together and tied to the same supply. Each pin should also be decoupled to DGND with a 100 nF capacitor.
1, 35, 42, 43, 53, 62, 64	DGND	Ground Reference for Digital Circuitry.
19	$V_{IN}A+$	Positive Input to Differential Amplifier.
20	$V_{IN}A–$	Negative Input to Differential Amplifier.
21	$V_{OUT}A–$	Negative Output from Differential Amplifier.
22	$V_{OUT}A+$	Positive Output from Differential Amplifier.
25	$V_{IN}+$	Positive Input to the Modulator.
26	$V_{IN}–$	Negative Input to the Modulator.
10	V_{REF+}	Reference Input. The input range of this pin is determined by the reference buffer supply voltage ($AV_{DD}4$). See the Reference Voltage Filtering section for more details.
8	DECAPA	Decoupling Pin. A 100 nF capacitor must be inserted between this pin and AGND.

Pin No.	Mnemonic	Description
30	DECAPB	Decoupling Pin. A 33 pF capacitor must be inserted between this pin and AGND3.
17	R_{BIAS}	Bias Current Setting Pin. A resistor must be inserted between this pin and AGND. For more details, see the Bias Resistor Selection section.
45 to 52, 54 to 61	DB15:DB8, DB7:DB0	16-Bit Bidirectional Data Bus. These are three-state pins that are controlled by the $\overline{CS}$ pin and the $\overline{RD}$/WR pin. The operating voltage for these pins is determined by the V_{DRIVE} voltage. See the Modulator Data Output Mode and AD7760 Interface sections for more details.
37	$\overline{RESET}$	A falling edge on this pin resets all internal digital circuitry and powers down the part. Holding this pin low keeps the AD7760 in a reset state.
3	MCLK	Master Clock Input. A low jitter, buffered digital clock must be applied to this pin. The output data rate depends on the frequency of this clock. See the Clocking the AD7760 section for more details.
2	MCLKGND	Master Clock Ground Sensing Pin.
36	$\overline{SYNC}$	Synchronization Input. A falling edge on this pin resets the internal filter. This can be used to synchronize multiple devices in a system. See the Synchronization section for more details.
39	$\overline{RD}$/WR	Read/Write Input. This pin, in conjunction with the chip select pin, is used to read and write data to and from the AD7760. If this pin is low when $\overline{CS}$ is low, a read takes place. If this pin is high when $\overline{CS}$ is low, a write occurs. See the Modulator Data Output Mode and AD7760 Interface sections for more details.
38	$\overline{DRDY}$	Data Ready Output. Each time new conversion data is available, an active low pulse, ½ ICLK period wide, is produced on this pin. See the Modulator Data Output Mode and AD7760 Interface sections for more details.
40	$\overline{CS}$	Chip Select Input. Used in conjunction with the $\overline{RD}$/WR pin to read and write data from and to the AD7760. See the Modulator Data Output Mode and AD7760 Interface sections for more details.

TERMINOLOGY

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7760, it is defined as

$$THD\,(\mathrm{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Nonharmonic Spurious-Free Dynamic Range (SFDR)
SFDR is the ratio of the rms signal amplitude to the rms value of the peak spurious spectral component, excluding harmonics.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for the dynamic range is expressed in decibels.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7760 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used.

In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Error
Zero error is the difference between the ideal midscale input voltage (when both inputs are shorted together) and the actual voltage producing the midscale output code.

Zero Error Drift
Zero error drift is the change in the actual zero error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

Gain Error
The first transition (from 100 … 000 to 100 … 001) should occur for an analog voltage ½ LSB above the nominal negative full scale. The last transition (from 011 … 110 to 011 … 111) should occur for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition, from the difference between the ideal levels.

Gain Error Drift
Gain error drift is the change in the actual gain error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

$AV_{DD}1 = DV_{DD} = V_{DRIVE} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF} = 4.096$ V, $T_A = 25°C$, normal mode, unless otherwise noted. All FFTs are generated from 65,536 samples using a 7-term Blackman-Harris window.

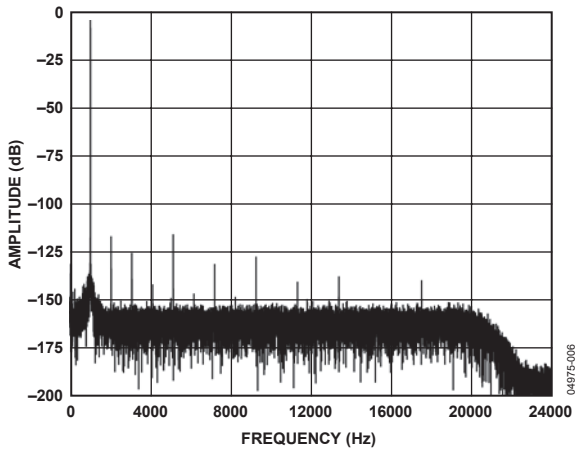

Figure 5. Normal Mode FFT, 1 kHz, −0.5 dB Input Tone, 256× Decimation

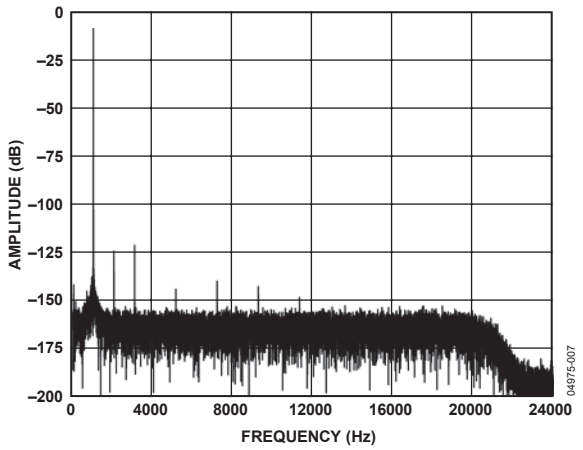

Figure 6. Normal Mode FFT, 1 kHz, −6 dB Input Tone, 256× Decimation

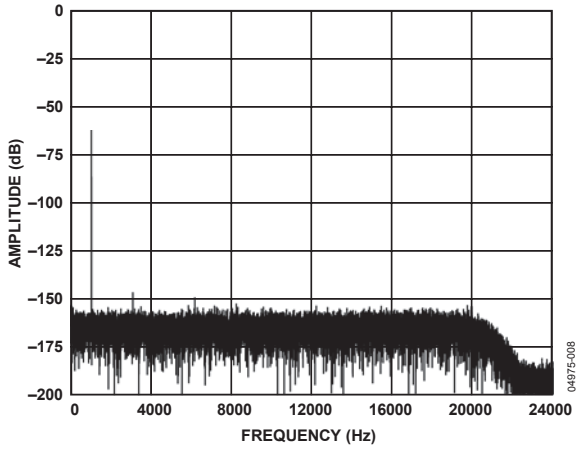

Figure 7. Normal Mode FFT, 1 kHz, −60 dB Input Tone, 256× Decimation

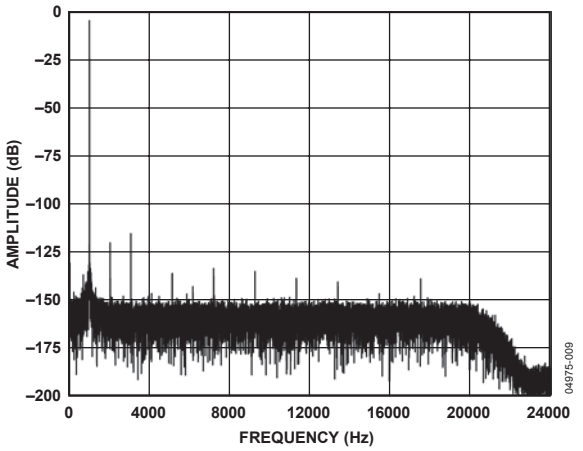

Figure 8. Low Power FFT, 1 kHz, −0.5 dB Input Tone, 256× Decimation

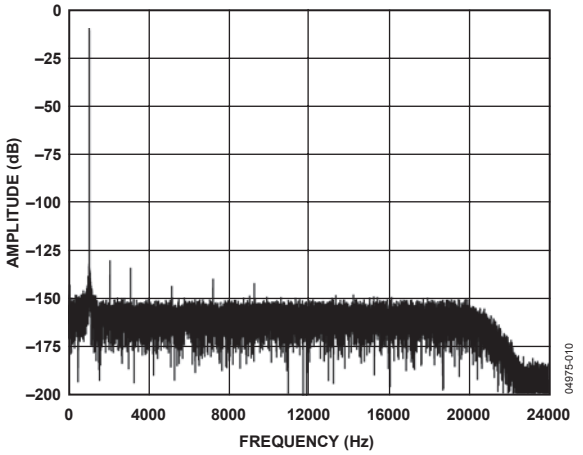

Figure 9. Low Power FFT, 1 kHz, −6 dB Input Tone, 256× Decimation

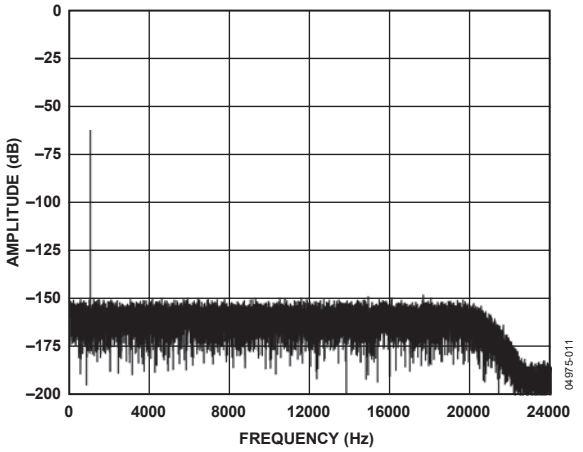

Figure 10. Low Power FFT, 1 kHz, −60 dB Input Tone, 256× Decimation

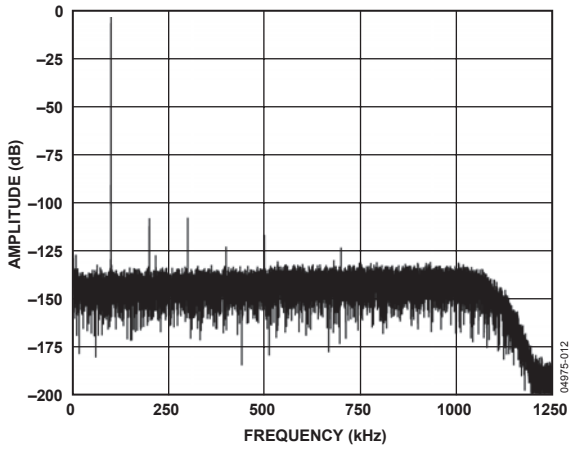

Figure 11. Normal Mode FFT, 100 kHz, −0.5 dB Input Tone, 8× Decimation

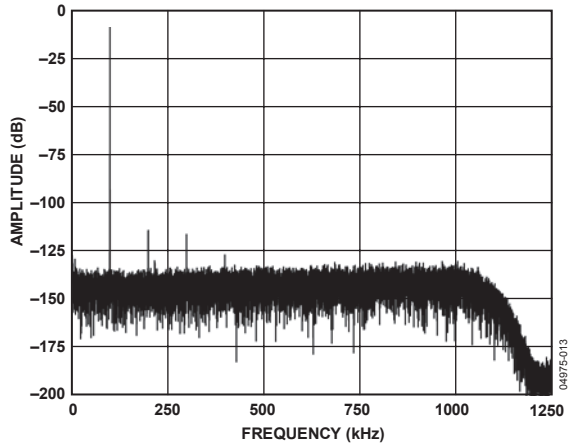

Figure 12. Normal Mode FFT, 100 kHz, −6 dB Input Tone, 8× Decimation

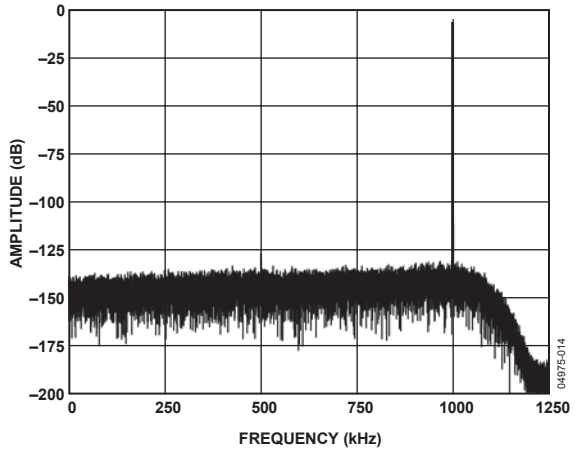

Figure 13. Normal Mode FFT, 1 MHz, −0.5 dB Input Tone, 8× Decimation

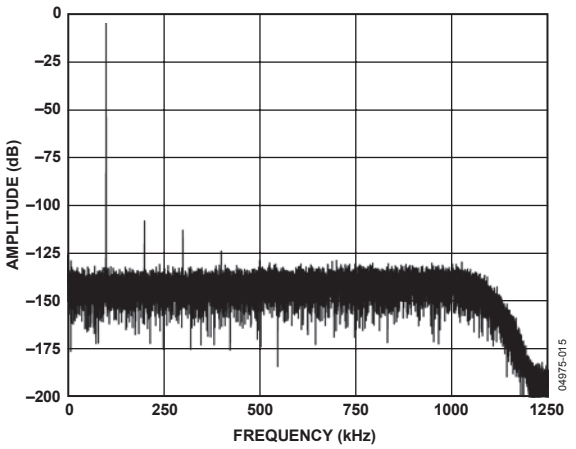

Figure 14. Low Power FFT, 100 kHz, −0.5 dB Input Tone, 8× Decimation

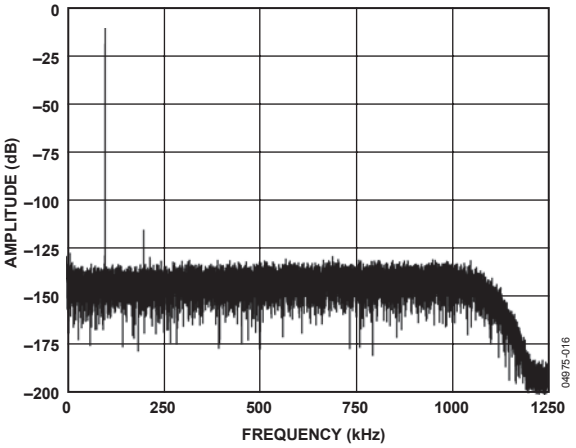

Figure 15. Low Power FFT, 100 kHz, −6 dB Input Tone, 8× Decimation

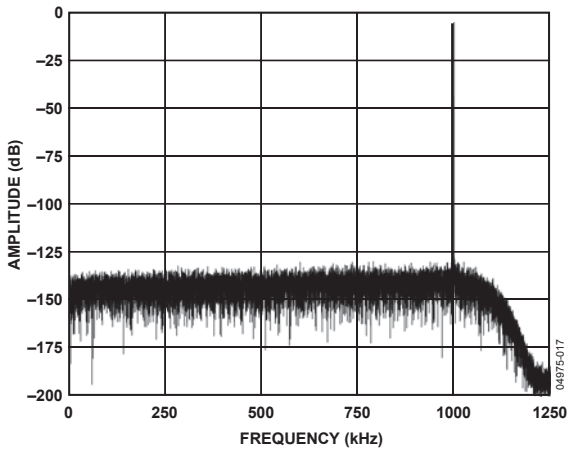

Figure 16. Low Power FFT, 1 MHz, −0.5 dB Input Tone, 8× Decimation

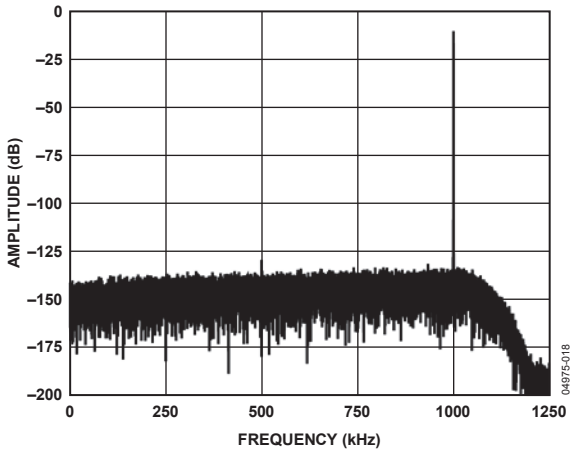

Figure 17. Normal Mode FFT, 1 MHz, –6 dB Input Tone, 8× Decimation

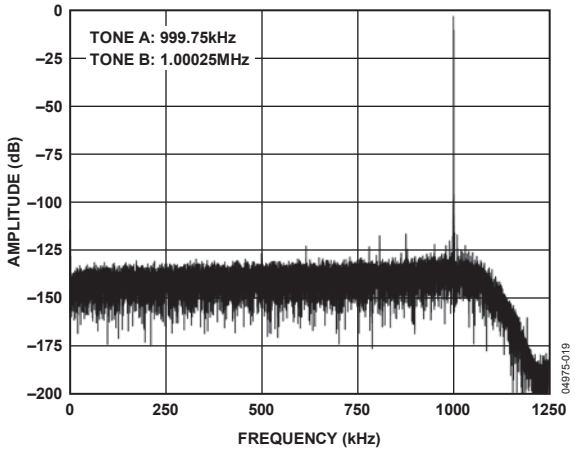

Figure 18. Normal Mode IMD, 1 MHz Center Frequency, 8× Decimation

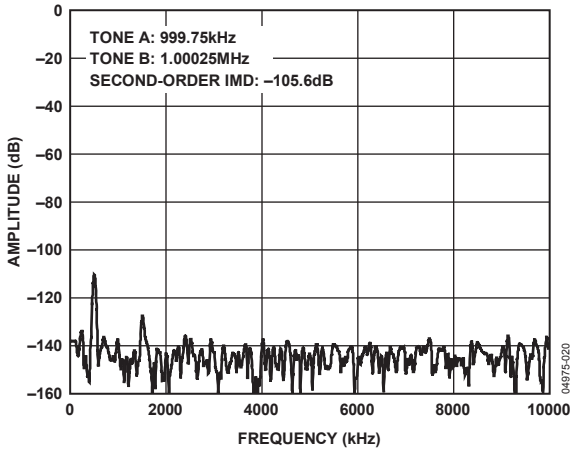

Figure 19. Normal Mode IMD, 1 MHz Center Frequency, 8× Decimation

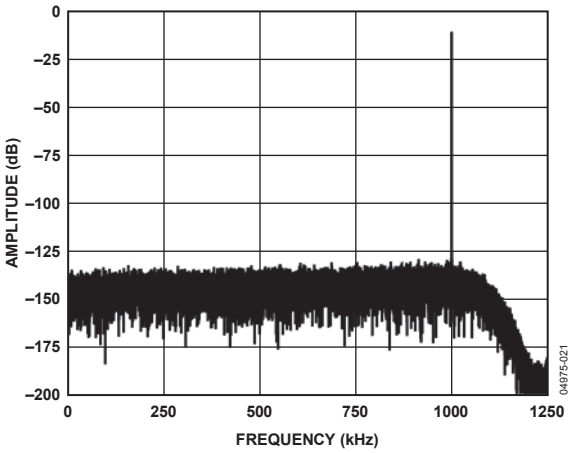

Figure 20. Low Power FFT, 1 MHz, –6 dB Input Tone, 8× Decimation

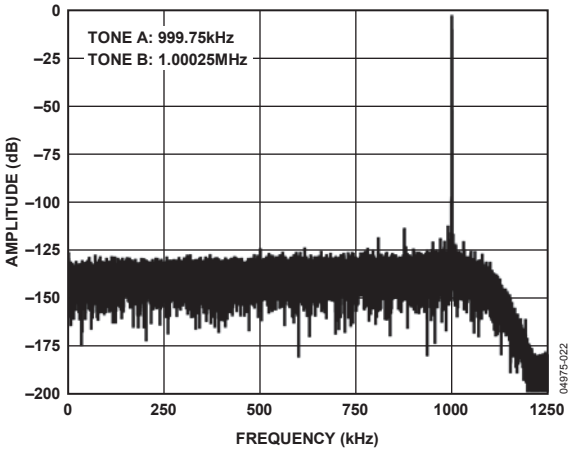

Figure 21. Low Power IMD, 1 MHz Center Frequency, 8× Decimation

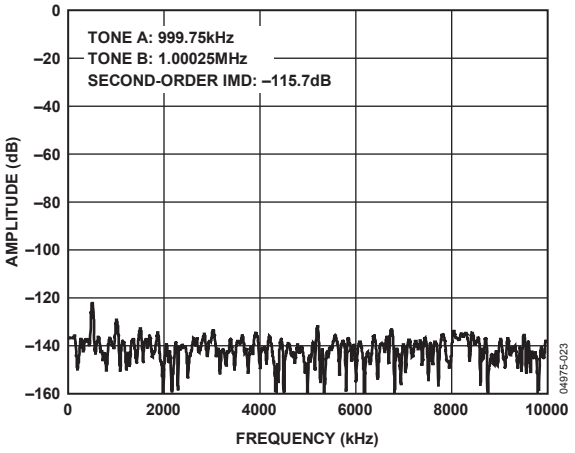

Figure 22. Low Power IMD, 1 MHz Center Frequency, 8× Decimation

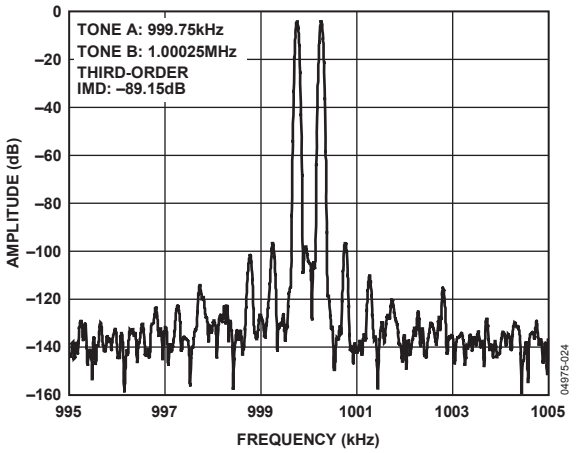

Figure 23. Normal Mode IMD, 1 MHz Center Frequency, 8× Decimation

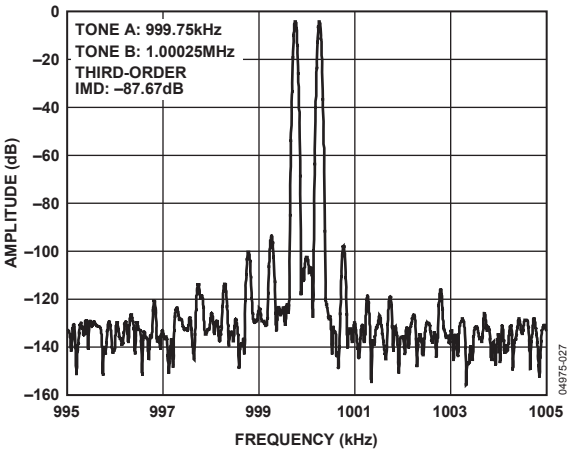

Figure 26. Normal Mode IMD, 1 MHz Center Frequency, 8× Decimation

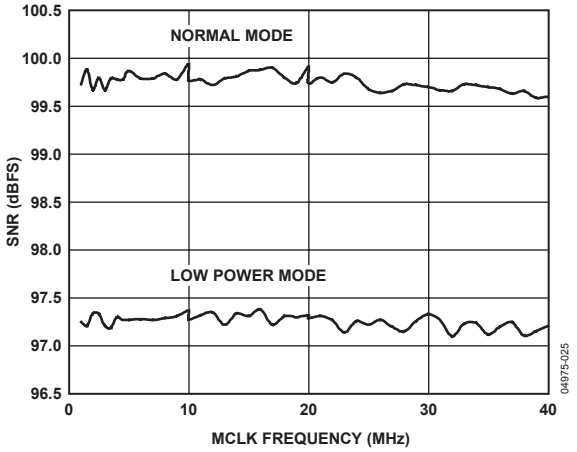

Figure 24. SNR vs. MCLK Frequency, 8× Decimation, −6 dB, 1 kHz Input Tone

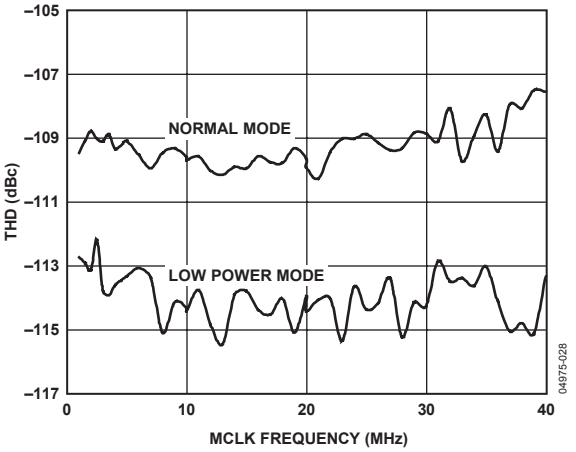

Figure 27. THD vs. MCLK Frequency, 8× Decimation, −6 dB, 1 kHz Input Tone

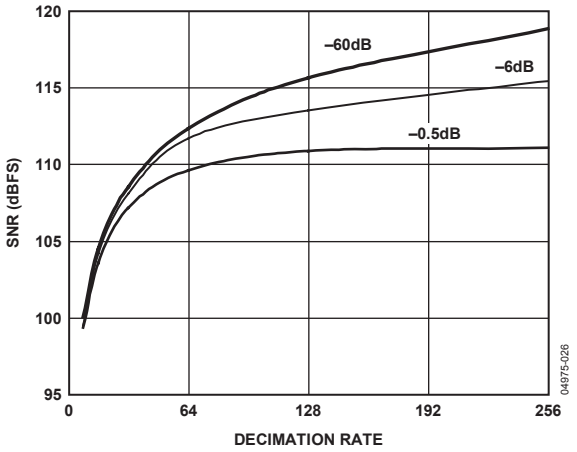

Figure 25. Normal Mode SNR vs. Decimation Rate, 1 kHz Input Tone

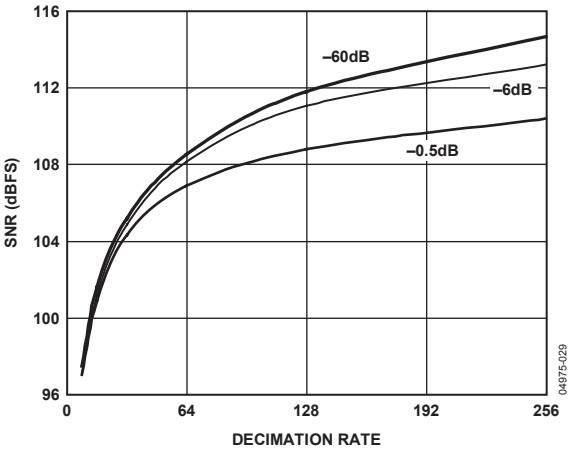

Figure 28. Low Power SNR vs. Decimation Rate, 1 kHz Input Tone

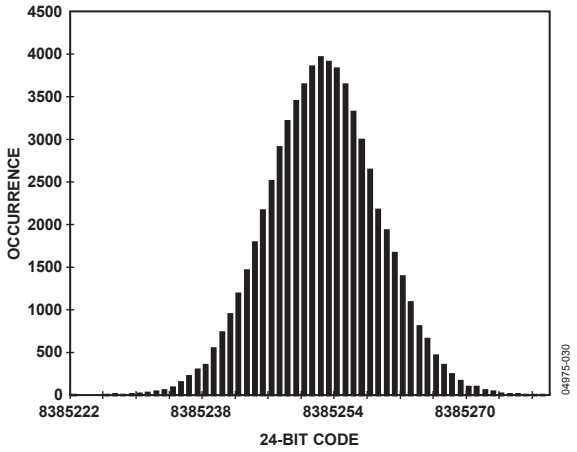

Figure 29. Normal Mode, 24-Bit Histogram, 256× Decimation

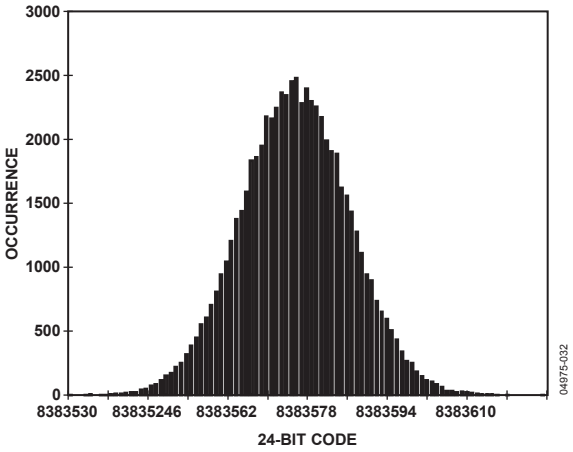

Figure 32. Low Power, 24-Bit Histogram, 256× Decimation

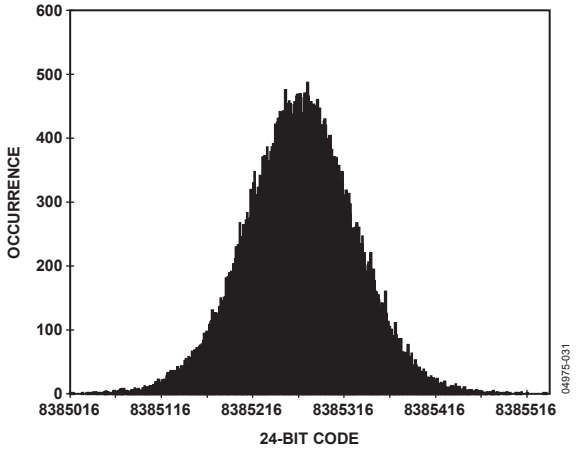

Figure 30. Normal Mode, 24-Bit Histogram, 8× Decimation

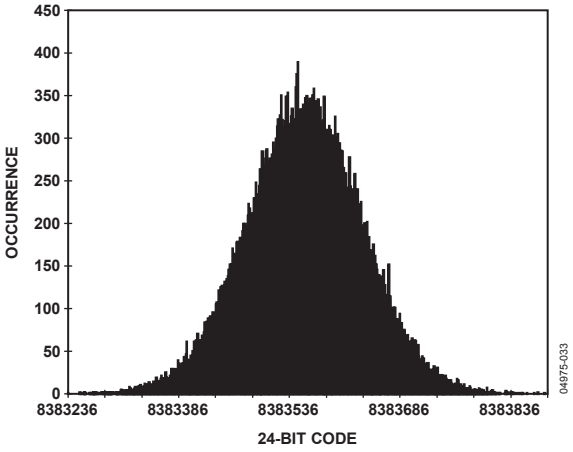

Figure 33. Low Power, 24-Bit Histogram, 8× Decimation

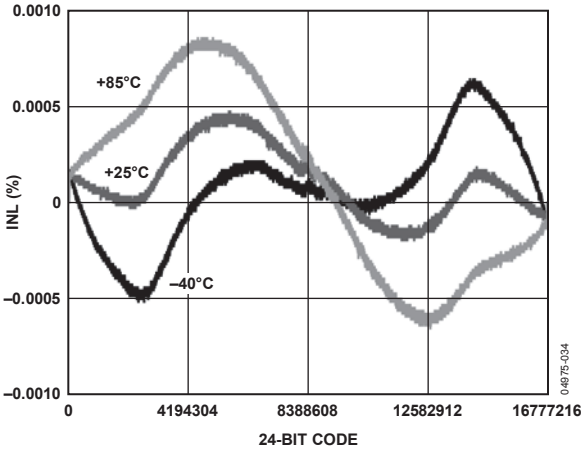

Figure 31. 24-Bit INL, Normal Mode

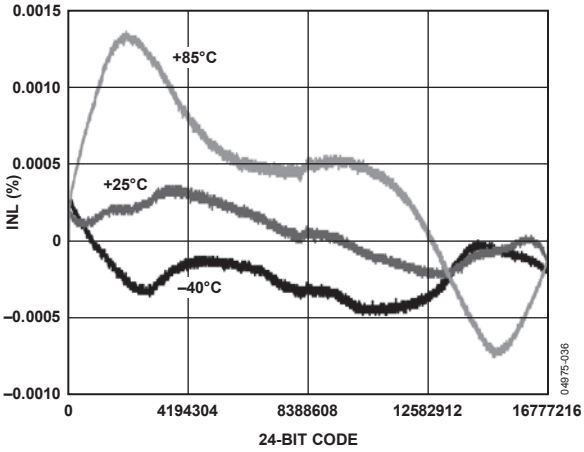

Figure 34. 24-Bit INL, Low Power Mode

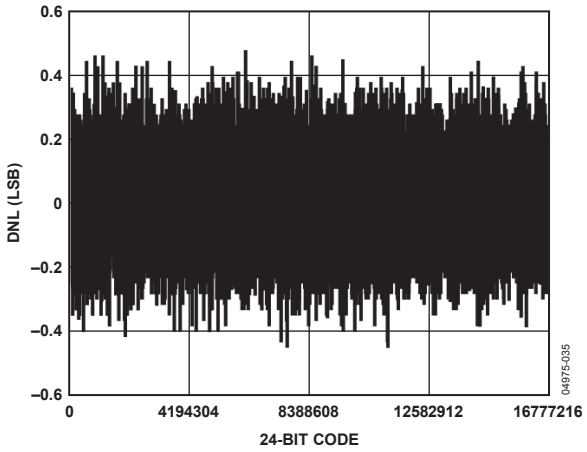

Figure 35. 24-Bit DNL

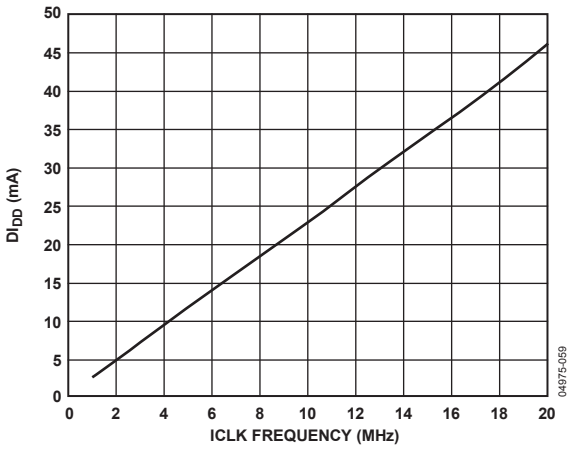

Figure 38. Decimate × 32, DI_{DD} vs. ICLK Frequency (DV_{DD} = 2.5 V)

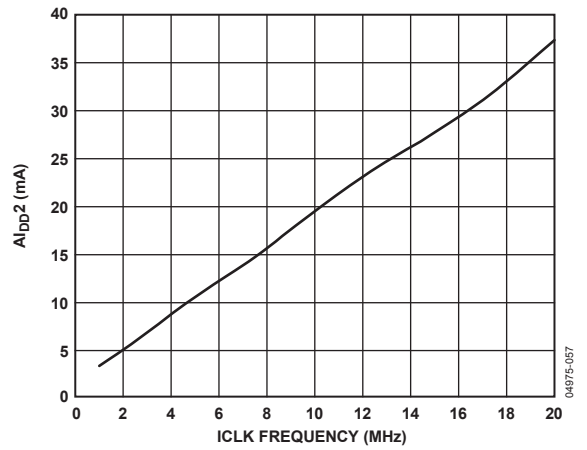

Figure 36. $AI_{DD}2$ vs. ICLK Frequency ($AV_{DD}2$ = 5 V)

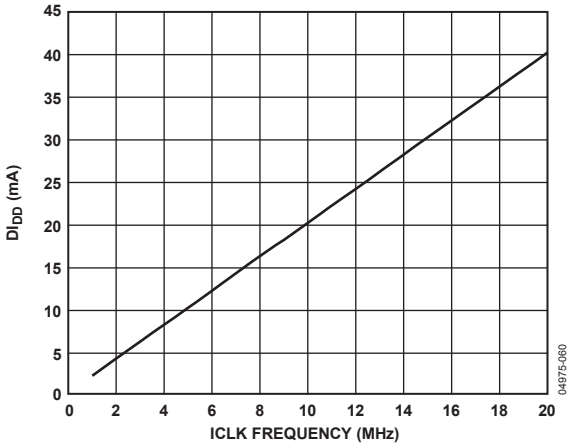

Figure 39. Decimate × 256, DI_{DD} vs. ICLK Frequency (DV_{DD} = 2.5 V)

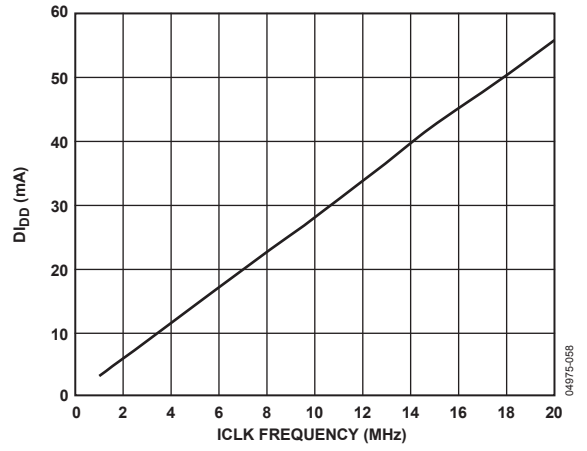

Figure 37. Decimate × 8, DI_{DD} vs. ICLK Frequency (DV_{DD} = 2.5 V)

THEORY OF OPERATION

The AD7760 employs a Σ-Δ conversion technique to convert the analog input into an equivalent digital word. The modulator samples the input waveform and outputs an equivalent digital word to the digital filter at a rate equal to ICLK.

By employing oversampling, the quantization noise is spread across a wide bandwidth from 0 to f_{ICLK}. This means that the noise energy contained in the signal band of interest is reduced (see Figure 40a). To further reduce the quantization noise in the signal band of interest, a high order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the signal band (see Figure 40b).

The digital filtering that follows the modulator removes the large out-of-band quantization noise (see Figure 40c) while also reducing the data rate from f_{ICLK} at the input of the filter to $f_{ICLK}/8$ or less at the output of the filter, depending on the decimation rate used.

Digital filtering has certain advantages over analog filtering: It does not introduce significant noise or distortion and can be made perfectly linear in terms of phase.

The AD7760 employs three FIR filters in series. By using different combinations of decimation ratios, filter selection, and bypassing, data can be obtained from the AD7760 at a large range of data rates. Multibit data from the modulator can be obtained at the ICLK rate (see Modulator Data Output Mode section). The first filter receives the data from the modulator at a maximum frequency of 20 MHz and decimates it by 4 to output the data at 5 MHz. The partially filtered data can be output at this stage. The second filter allows the decimation rate to be chosen from 2× to 32× or to be completely bypassed.

The third filter has a fixed decimation rate of 2×, is user programmable, and has a default configuration. It is described in detail in the Programmable FIR Filter section. This filter can also be bypassed.

Table 6 shows some characteristics of the default filter. The group delay of the filter is defined to be the delay to the center of the impulse response and is equal to the computation plus the filter delays. The delay until valid data is available (the DVALID status bit is set) is equal to twice the filter delay plus the computation delay.

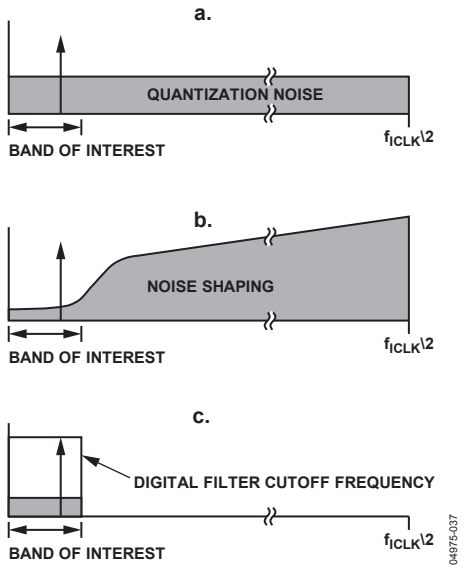

Figure 40. Σ-Δ ADC

Table 6. Configuration with Default Filter

ICLK Frequency	Filter 1	Filter 2	Filter 3	Data State	Computation Delay	Filter Delay	Pass-Band Bandwidth	Output Data Rate (ODR)
20 MHz	Bypassed	Bypassed	Bypassed	Unfiltered	0	0	10 MHz	20 MHz
20 MHz	4×	Bypassed	Bypassed	Partially filtered	0.325 µs	1.2 µs	1.35 MHz	5 MHz
20 MHz	4×	Bypassed	2×	Fully filtered	1.075 µs	10.8 µs	1 MHz	2.5 MHz
20 MHz	4×	2×	Bypassed	Partially filtered	1.35 µs	3.6 µs	562.5 kHz	2.5 MHz
20 MHz	4×	2×	2×	Fully filtered	1.625 µs	22.8 µs	500 kHz	1.25 MHz
20 MHz	4×	4×	Bypassed	Partially filtered	1.725 µs	6 µs	281.25 kHz	1.25 MHz
20 MHz	4×	4×	2×	Fully filtered	1.775 µs	44.4 µs	250 kHz	625 kHz
20 MHz	4×	8x	Bypassed	Partially filtered	2.6 µs	10.8 µs	140.625 kHz	625 kHz
20 MHz	4×	8×	2×	Fully filtered	2.25 µs	87.6 µs	125 kHz	312.5 kHz
20 MHz	4×	16×	Bypassed	Partially filtered	4.175 µs	20.4 µs	70.3125 kHz	312.5 kHz
20 MHz	4×	16×	2×	Fully filtered	3.1 µs	174 µs	62.5 kHz	156.25 kHz
20 MHz	4×	32×	Bypassed	Partially filtered	7.325 µs	39.6 µs	35.156 kHz	156.25 kHz
20 MHz	4×	32×	2×	Fully filtered	4.65 µs	346.8 µs	31.25 kHz	78.125 kHz
12.288 MHz	4×	8×	2×	Fully filtered	3.66 µs	142.6 µs	76.8 kHz	192 kHz
12.288 MHz	4×	16×	2×	Fully filtered	5.05 µs	283.2 µs	38.4 kHz	96 kHz
12.288 MHz	4×	32×	Bypassed	Partially filtered	11.92 µs	64.45 µs	21.6 kHz	96 kHz
12.288 MHz	4×	32×	2×	Fully filtered	7.57 µs	564.5 µs	19.2 kHz	48 kHz

MODULATOR DATA OUTPUT MODE

Operating the AD7760 in modulator output mode enables the output of data directly from the Σ-Δ modulator. This mode of operation bypasses the AD7760 on-board digital filtering capabilities, outputting data in its unfiltered form.

As discussed in the Theory of Operation section, the AD7760 operates using oversampling, which spreads quantization noise over a wide bandwidth. The decrease in the quantization noise energy in the resulting signal band is illustrated in Figure 40a. By coupling the use of oversampling with the use of a high order, multibit Σ-Δ modulator, the AD7760 further reduces the quantization noise in the signal band. Figure 41 is an FFT of unfiltered data output from the AD7760 when it is used in modulator output mode. This clearly demonstrates the shaping of the quantization noise performed by the AD7760's Σ-Δ modulator.

MODULATOR INPUTS

The maximum voltage input to each differential modulator input pin is 0.8 × 4.096 V ≈ 3.275 V (80% of V_{REF}), which must sit on a common mode of $V_{REF}/2$. This maximum differential input voltage is shown as the conditioned output of the AD7760's on-board differential amplifier in Figure 52 in the Driving the AD7760 section.

Further details on the signal conditioning implemented by the AD7760's on-board differential amplifier and the recommended external circuitry that accompanies it is described in the Driving the AD7760 section.

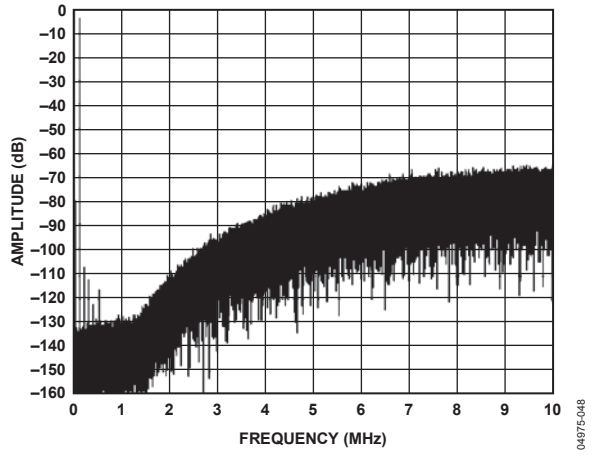

Figure 41. FFT of Data Output by the AD7760 in Modulator Output Mode

MODULATOR DATA OUTPUT SCALING

In modulator output mode, data is output in a 16-bit twos complement format on Pins D [15:0]; however, this data is scaled to 15 bits. The transfer function in Figure 42 shows the scaling involved for the 16 data bits output from Modulator Pins D[15:0] vs. the maximum differential voltage input allowed for the modulator inputs ($V_{IN}+$ and $V_{IN}-$).

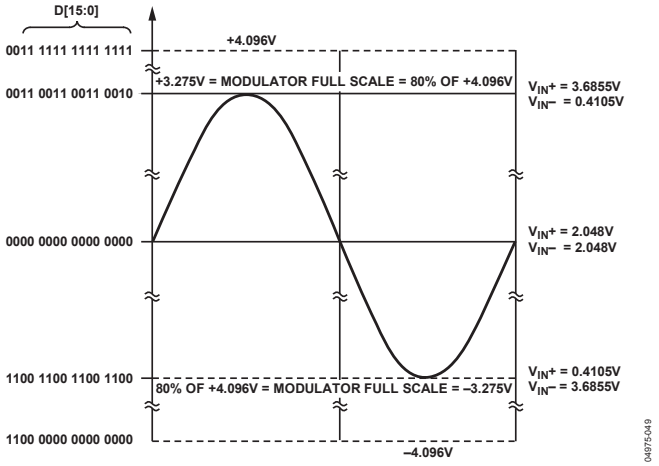

Figure 42. Modulator Output Data Scaling

As the nature of the modulator output is coarse relative to the fully filtered output of the AD7760 (due to the associated quantization noise of the modulator output), Bits D[3:0] of the modulator output are zero when operating in modulator data output mode. Thus, the data outputs for the calculations listed in Example 1 and Example 2 for inputs to the modulator pins $V_{IN}+$ and $V_{IN}-$ show Bits D[3:0] of the modulator output as zero.

Example 1

$V_{IN}+ = 3.5$ V

$V_{IN}- = 0.595$ V

Modulator Output Code = $([V_{IN}(+) - V_{IN}(-)]/4.096\text{ V}) \times 16384$

$= [(3.5\text{ V} - 0.595\text{ V})/4.096\text{ V}] \times 16384$

$= +11620$

Direct Scaling: [0010 1101 0110 0100]

Value Output on Data Output Pins D[15:0]:

D [15:0] = [0010 1101 0110 0000].

Example 2

$V_{IN}+ = 0.595$ V

$V_{IN}- = 3.5$ V

Modulator Output Code = $([V_{IN}(+) - V_{IN}(-)]/4.096\text{ V}) \times 16384$

$= [(0.595\text{ V} - 3.5\text{ V})/4.096\text{ V}] \times 16384$

$= -11620$

Direct Scaling: [1101 0010 1001 1100]

Value Output on Data Output Pins D[15:0]:

D [15:0] = [1101 0010 1001 0000].

MODULATOR DATA OUTPUT MODE INTERFACE

The AD7760 can be configured in modulator data output mode (bypassing the default decimation filtering) by writing 0 to each of the bits contained in Control Register 1: $\overline{\text{BYP F1}}$, $\overline{\text{BYP F3}}$, and DEC [2:0]. This will bypass all digital decimation filtering offered by the AD7760. See the AD7760 Registers section for further details.

When the AD7760 is operating in modulator data output mode, a different parallel interfacing scheme than that used for configurations, where the AD7760's data output is filtered is necessary.

The data output rate depends on the clock divider ratio that is used. When the $\overline{\text{CDIV}}$ bit in Control Register 2 is set to logic high, data is output at the MCLK frequency. If the $\overline{\text{CDIV}}$ bit is set to logic low, data is output at a frequency of MCLK/2. See the Clocking the AD7760 section.

CLOCK DIVIDE-BY-1 MODE ($\overline{\text{CDIV}}$ = 1)

When obtaining data from the AD7760 in modulator output mode, both the $\overline{\text{RD}}$/WR and $\overline{\text{CS}}$ lines must be held low. This brings the data bus out of its high impedance state. Figure 43 shows the timing diagram for reading data in the modulator data output mode when operating with $\overline{\text{CDIV}}$ = 1 (that is, ICLK = MCLK). A $\overline{\text{DRDY}}$ pulse is generated for each word. The data on each of the 16 data output pins, D [15:0], is valid on the rising edge of the $\overline{\text{DRDY}}$ pulse. The $\overline{\text{DRDY}}$ pulse can be used to latch the modulator data into a FIFO or as a DMA control signal. Shortly after the $\overline{\text{RD}}$/WR and $\overline{\text{CS}}$ lines return high, the AD7760 stops outputting data and the data bus returns to high impedance.

CLOCK DIVIDE-BY-2 MODE ($\overline{\text{CDIV}}$ = 0)

When operating in modulator output mode with $\overline{\text{CDIV}}$ = 0 (that is, ICLK = MCLK/2), the frequency of the $\overline{\text{DRDY}}$ signal created is half that of the MCLK frequency input to the device. The timing scheme that is used when $\overline{\text{CDIV}}$ = 0 depends on the number of MCLK cycles that occur between $\overline{\text{RESET}}$ and $\overline{\text{SYNC}}$. If the number of MCLK cycles (n) between the rising edge of $\overline{\text{RESET}}$ and the rising edge of $\overline{\text{SYNC}}$ (see Figure 44) is an even value, use the interface timing shown in Figure 43. If n is an odd value, use the interface timing shown in Figure 45.

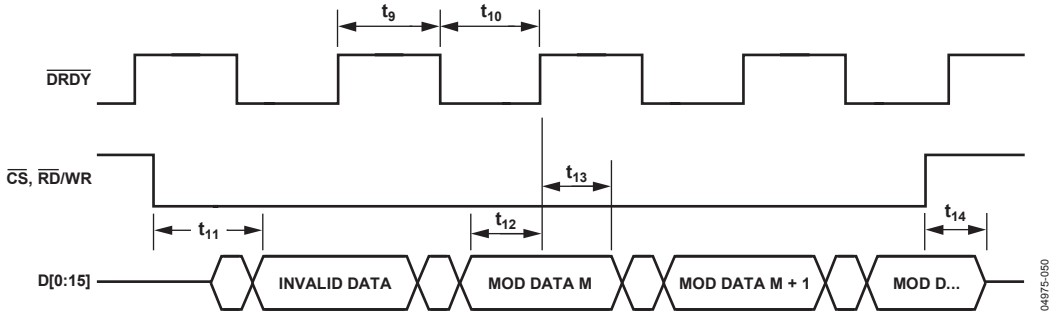

Figure 43. AD7760 Modulator Output Mode ($\overline{\text{CDIV}}$ = 1) and ($\overline{\text{CDIV}}$ = 0, n is even)

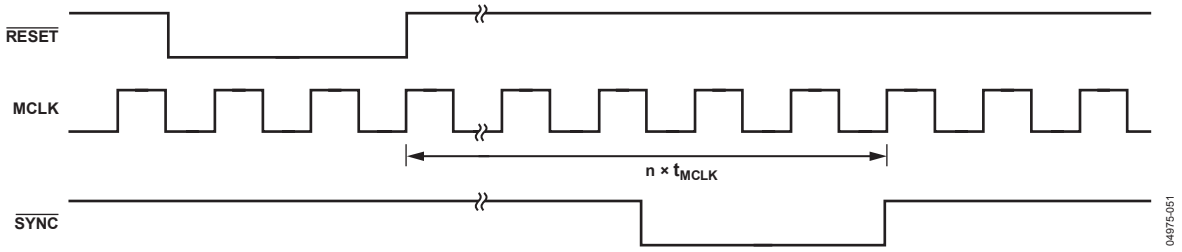

Figure 44. AD7760 Relative Timing Between $\overline{\text{RESET}}$ and $\overline{\text{SYNC}}$ in Modulator Output Mode $\overline{\text{CDIV}}$ = 0

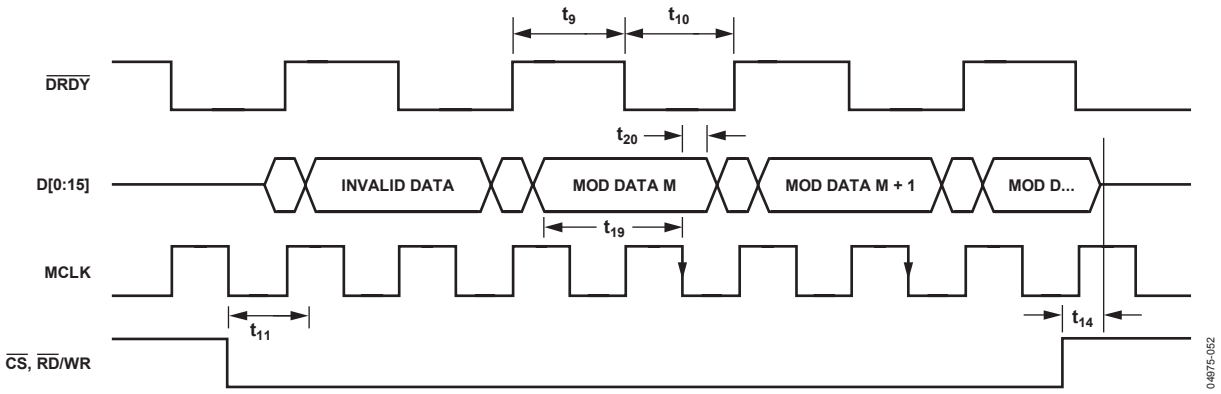

Figure 45. AD7760 Modulator Output Mode ($\overline{CDIV}$ = 0, n is odd)

In the case where n is an odd number of MCLK cycles, the modulator data output on Pins D [15:0] is output on the rising edge of $\overline{DRDY}$. In this case, the modulator data should be read on the falling edge of MCLK when $\overline{DRDY}$ is logic low. Figure 45 shows timing details to be used when reading the modulator output data where $\overline{CDIV}$ = 0 and there is an odd number of MCLK cycles between the rising edge of $\overline{RESET}$ and the rising edge of $\overline{SYNC}$. The edge of MCLK that should be used under these conditions is illustrated in Figure 45 by arrows on the MCLK falling edges in question.

USING THE AD7760 IN MODULATOR OUTPUT MODE

The following is the recommended sequence for powering up and using the AD7760:

1. Apply power.
2. Start the clock oscillator, applying MCLK.
3. Take $\overline{RESET}$ low for a minimum of one MCLK cycle.
4. Wait a minimum of two MCLK cycles after the rising edge of $\overline{RESET}$.
5. Write to Control Register 2 to power up the ADC and the differential amplifier as required. The correct clock divider ($\overline{CDIV}$) ratio should be programmed at this time.
6. Write to Control Register 1 to set the bypass filter bits, $\overline{BYP\ F1}$ and $\overline{BYP\ F3}$, and the decimation rate bits, DEC [2:0], to 0.
7. Wait a minimum of six MCLK cycles after the rising edge of $\overline{CS}$ has been released.
8. Take $\overline{SYNC}$ low for a minimum of four MCLK cycles, if required, to synchronize multiple parts.

Using this sequence results in an even number of MCLK cycles between the rising edge of $\overline{RESET}$ and the rising edge of $\overline{SYNC}$. Therefore, when using this sequence with $\overline{CDIV}$ = 0, the interface timing shown in Figure 43 should be implemented.

Note that whether the number of MCLK cycles between the rising edge of $\overline{RESET}$ and $\overline{SYNC}$ is odd or even is irrelevant when the AD7760 is operated with $\overline{CDIV}$ = 1.

When using the AD7760 in modulator output mode, the offset, gain, and overrange registers are not operational. The only registers that can be used are Control Register 1 and Control Register 2.

AD7760 INTERFACE

READING DATA

When the AD7760 is outputting data at a 5 MHz output data rate or less, the interface operates in a conventional mode, as shown in Figure 2, using a 16-bit bidirectional parallel interface. This interface is controlled by the $\overline{RD}$/WR and $\overline{CS}$ pins. The 24-bit conversion data is output in twos complement format. When a new conversion result is available, an active low pulse is output on the $\overline{DRDY}$ pin.

To read a conversion result from the AD7760, two 16-bit read operations are performed. The $\overline{DRDY}$ pulse indicates that a new conversion result is available. Both $\overline{RD}$/WR and $\overline{CS}$ go low to perform the first read operation. Shortly after both lines go low, the data bus becomes active and the 16 most significant bits (MSBs) of the conversion result are output. The $\overline{RD}$/WR and $\overline{CS}$ lines must return high for a full ICLK period before the second read is performed. This second read contains the eight least significant bits (LSBs) of the conversion result along with six status bits. These status bits are shown in Table 7. Descriptions of the other status bits are found in Table 17.

Table 7. Status Bits During Data Read

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DVALID	OVR	UFILT	LPWR	FILTOK	DLOK	0	0

Shortly after $\overline{RD}$/WR and $\overline{CS}$ return high, the data bus returns to a high impedance state. Both read operations must be completed before a new conversion result is available because the new result overwrites the contents of the output register. If a $\overline{DRDY}$ pulse occurs during a read operation, the data read is invalid.

READING STATUS AND OTHER REGISTERS

The AD7760 features a number of programmable registers. To read back the contents of these registers or the status register, the user must first write to the control register of the device, setting a bit that corresponds to the register to be read. The next read operation outputs the contents of the selected register instead of a conversion result. The AD7760 Registers section provides more information on the relevant bits in the control register.

SHARING THE PARALLEL BUS

By its nature, the high accuracy of the AD7760 makes it sensitive to external noise sources. These include digital activity on the parallel bus. For this reason, it is recommended that the AD7760 data lines be isolated from the system data bus by means of a latch or buffer to ensure all digital activity on the D0 to D15 pins is controlled by the AD7760.

If multiple synchronized AD7760 parts that share a properly distributed common MCLK signal exist in a system, these parts can share a common bus without being isolated from each other. This bus can then be isolated from the system bus by a single latch or buffer.

SYNCHRONIZATION

The $\overline{SYNC}$ input to the AD7760 provides a synchronization function that allows the user to begin gathering samples of the analog front-end input from a known point in time.

The $\overline{SYNC}$ function allows multiple AD7760s, operated from the same MCLK, $\overline{RESET}$, and $\overline{SYNC}$ signals, to be synchronized so that each ADC simultaneously updates its output register. The distribution of the signals that are common to each of the devices that are to be synchronized is extremely important in ensuring that the timing of each of the AD7760 devices is correct, that is, that each AD7760 device sees the same digital edges synchronously.

The $\overline{SYNC}$ signal is sensed on the falling edge of MCLK. On the first falling edge of MCLK after $\overline{SYNC}$ goes logic low, the digital filter sequencer is reset to 0. The filter is held in a reset state until a falling edge of the MCLK senses $\overline{SYNC}$ logic high. The $\overline{SYNC}$ signal must remain logic low for a minimum of four MCLK cycles. Figure 46 shows the recommended timing for the $\overline{SYNC}$ signal with respect to MCLK.

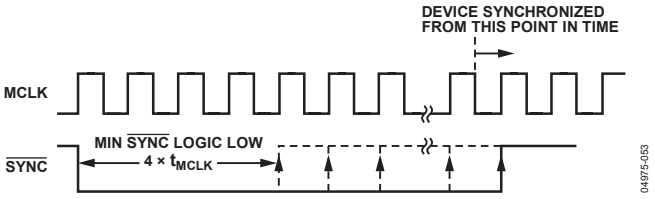

Figure 46. Recommended $\overline{SYNC}$ Timing

The rising edge of $\overline{SYNC}$ should be coincident with the rising edge of MCLK. Thus, the next falling edge of MCLK senses $\overline{SYNC}$ logic high and takes the filter out of its reset state. By applying this signal scheme to multiple ADCs using the same MCLK and $\overline{SYNC}$ signals, all of the devices will gather input samples synchronously.

Following a $\overline{SYNC}$ signal, the digital filter needs time to settle before valid data can be read from the AD7760. The DVALID status bit (D7 in Table 7) output with each conversion indicates when valid data is being output by the converter. The time from the rising edge of $\overline{SYNC}$ until the DVALID bit is asserted is dependent on the filter configuration used. See the Theory of Operation section and the values listed in Table 6 for details on calculating the time until DVALID is asserted.

WRITING TO THE AD7760

There are many features and parameters that the user can change by writing to the AD7760 device. See the Using the AD7760 section, which details the writing sequence needed to initialize the operation of the part.

The AD7760 has programmable registers that are 16 bits wide. This means that two write operations are required to program a register. The first write contains the register address, and the second write contains the register data. An exception is when a user-defined filter is being downloaded to the AD7760. This is described in detail in the Downloading a User-Defined Filter section. The AD7760 Registers section contains the register addresses and details.

Figure 3 shows a write operation to the AD7760. The $\overline{RD}$/WR line is held high while the $\overline{CS}$ line is brought low for a minimum of four ICLK periods. The register address is latched during this period. The $\overline{CS}$ line is brought high again for a minimum of four ICLK periods before the register data is put onto the data bus. If a read operation occurs between the writing of the register address and the register data, the register address is cleared and the next write must be the register address. This also provides a method to revert back to a known situation if the user forgets whether the next write is an address or data.

Generally, the AD7760 is written to and configured on power-up and very infrequently, if at all, after that. Following any write operation, the full group delay of the filter must elapse before valid data is output from the AD7760.

CLOCKING THE AD7760

The AD7760 requires an external low jitter clock source. This signal is applied to the MCLK pin, and the MCLKGND pin is used to sense the ground from the clock source. An internal clock signal (ICLK) is derived from the MCLK input signal. The ICLK controls all internal operations of the AD7760. The maximum ICLK frequency is 20 MHz, but due to an internal clock divider, a range of MCLK frequencies can be used. There are two ways to generate the ICLK:

$ICLK = MCLK$ ($\overline{CDIV} = 1$)

$ICLK = MCLK/2$ ($\overline{CDIV} = 0$)

These options are selected from the control register (see the AD7760 Registers section for more details). On power-up, the default is ICLK = MCLK/2 to ensure that the part can handle the maximum MCLK frequency of 40 MHz. For output data rates equal to those used in audio systems, a 12.288 MHz ICLK frequency can be used. As shown in Table 6, output data rates of 192 kHz, 96 kHz, and 48 kHz are achievable with this ICLK frequency. As mentioned previously, this ICLK frequency can be derived from different MCLK frequencies.

It is recommended that the MCLK signal applied to the AD7760 has a 50-50 mark-space ratio. When operating in clock divide-by-1 mode (that is, $\overline{CDIV} = 1$), using higher mark-space ratios reduces the maximum MCLK frequency that can be applied to the AD7760 yielding maximum performance. For example, using a mark-space ratio of 60-40 (with $\overline{CDIV} = 1$) reduces the maximum MCLK frequency that will yield the maximum INL and THD performance to 16 MHz.

BUFFERING THE MCLK SIGNAL

The MCLK signal for the AD7760 must be buffered before being input to the MCLK pin on the AD7760 device. This can be done simply by routing the MCLK signal to both inputs of an AND gate (see Figure 47).

The recommended buffer is the NC7SZ08M5, which is a two-input AND gate from Fairchild Semiconductor. Using the buffer with a supply voltage of 5 V is advised to achieve optimum performance from the AD7760.

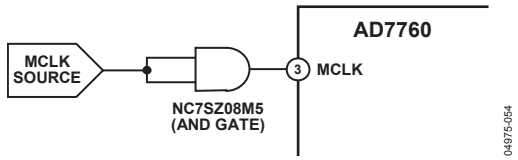

Figure 47. Buffering the MCLK Signal Using the NC7SZ08M5 AND Gate

MCLK JITTER REQUIREMENTS

The MCLK jitter requirements depend on a number of factors and are given by

$$t_{j(rms)} = \frac{\sqrt{OSR}}{2 \times \pi \times f_{IN} \times 10^{\frac{SNR\,(dB)}{20}}}$$

where:
OSR = oversampling ratio = f_{ICLK}/ODR.
f_{IN} = maximum input frequency.
$SNR(dB)$ = target SNR.

Example 1

This example can be taken from Table 6, where:
ODR = 2.5 MHz.
f_{ICLK} = 20 MHz.
f_{IN} (max) = 1 MHz.
SNR = 108 dB.

$$t_{j(rms)} = \frac{\sqrt{8}}{2 \times \pi \times 10^{6} \times 10^{5.4}} = 1.79 \text{ ps}$$

This is the maximum allowable clock jitter for a full-scale, 1 MHz input tone with the given ICLK and output data rate.

Example 2

Take a second example from Table 6, where:
ODR = 48 kHz.
f_{ICLK} = 12.288 MHz.
f_{IN} (max) = 19.2 kHz.
SNR = 120 dB.

$$t_{j(rms)} = \frac{\sqrt{256}}{2 \times \pi \times 19.2 \times 10^{3} \times 10^{6}} = 133 \text{ ps}$$

The input amplitude also has an effect on these jitter figures. For example, if the input level was 3 dB below full-scale, the allowable jitter would be increased by a factor of $\sqrt{2}$, increasing the first example to 2.53 ps rms. This happens when the maximum slew rate is decreased by a reduction in amplitude. Figure 48 and Figure 49 illustrate this point, showing the maximum slew rate of a sine wave of the same frequency but with different amplitudes.

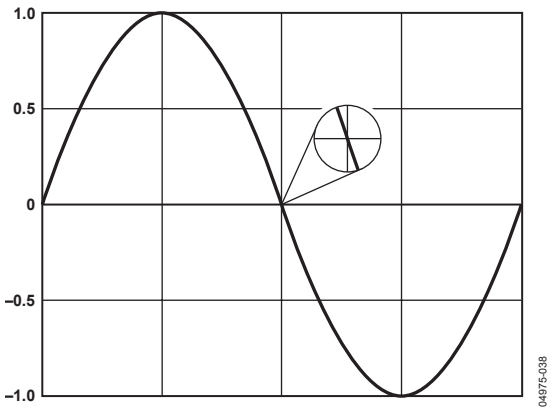

Figure 48. Maximum Slew Rate of Sine Wave with Amplitude of 2 V p-p

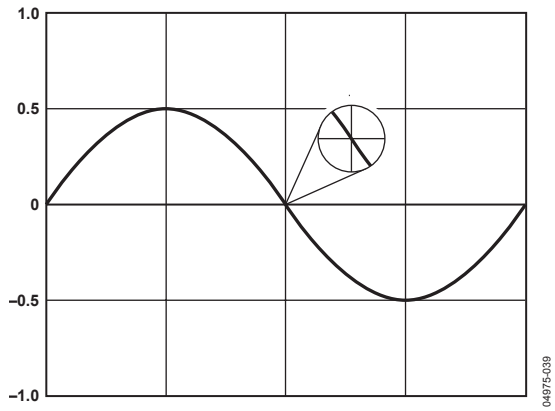

Figure 49. Maximum Slew Rate of Sine Wave (with the Same Frequency as in Figure 48) with Amplitude of 1 V p-p

DRIVING THE AD7760

The AD7760 has an on-chip differential amplifier that operates with a supply voltage ($AV_{DD}3$) within the 3.15 V to 5.25 V range. For a 4.096 V reference, the supply voltage must be 5 V.

To achieve the specified performance in normal mode, the differential amplifier should be configured as a first-order antialias filter, as shown in Figure 50. Any additional filtering should be carried out in previous stages using low noise, high performance op amps, such as the AD8021.

Suitable component values for the first-order filter are listed in Table 8. Using the values in the table as an example yields a 10 dB attenuation at the first alias point of 19 MHz.

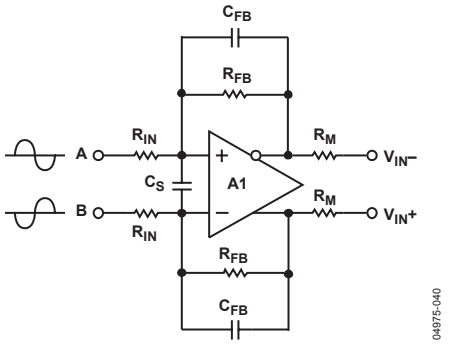

Figure 50. Differential Amplifier Configuration

Table 8. Normal Mode Component Values

V_{REF}	R_{IN}	R_{FB}	R_M	C_S	C_{FB}
4.096 V	1 kΩ	655 Ω	18 Ω	5.6 pF	33 pF

Figure 52 shows the signal conditioning that occurs using the circuit shown in Figure 50 with a ±2.5 V input signal biased around ground and the component values and conditions listed in Table 8. The differential amplifier always biases the output signal to sit on the optimum common mode of $V_{REF}/2$, in this case 2.048 V. The signal is also scaled to give the maximum allowable voltage swing with this reference value. This is calculated as 80% of V_{REF}, that is, 0.8 × 4.096 V ≈ 3.275 V p-p on each input.

With a 4.096 V reference, a 5 V supply must be provided to the reference buffer ($AV_{DD}4$). With a 2.5 V reference, a 3.3 V supply must be provided to $AV_{DD}4$.

Figure 51 shows the transfer function in terms of the 24-bit digital output codes (twos complement coding) of the AD7760 vs. the voltage signals V_A and V_B applied to the on-board differential amplifier A1, as shown in Figure 52.

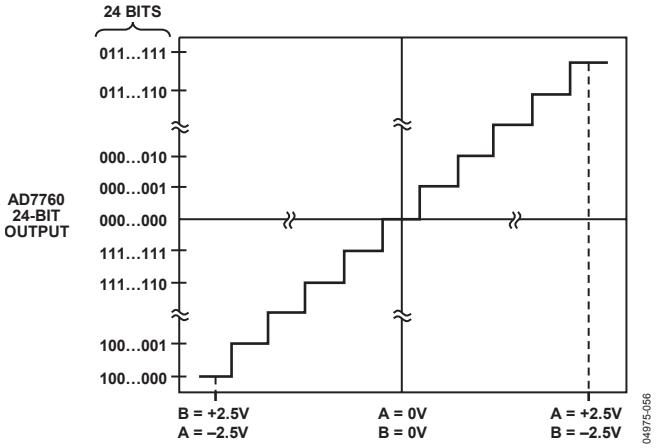

Figure 51. Transfer Function for the AD7760 Filtered Output Where V_A and V_B are Inputs to the On-Board Differential Amplifier A1

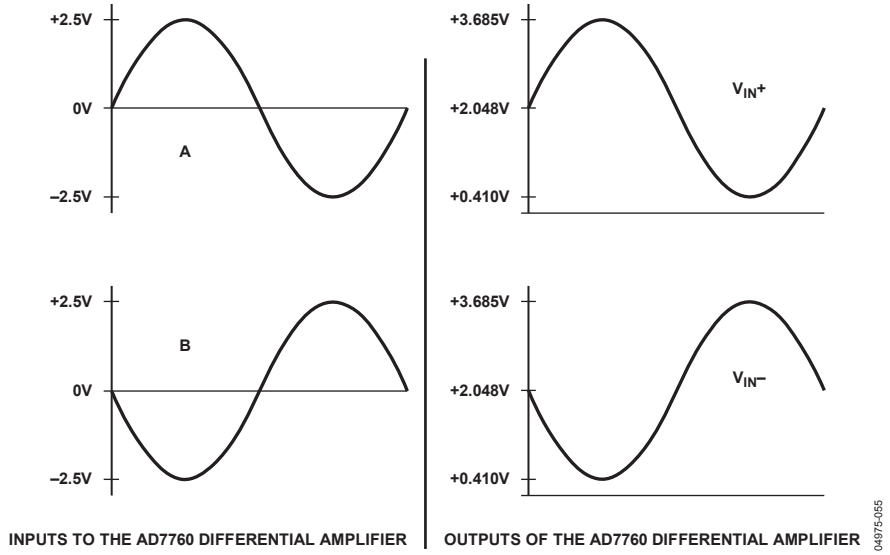

Figure 52. Differential Amplifier Signal Conditioning

To obtain maximum performance from the AD7760, it is advisable to drive the ADC with differential signals. Figure 53 shows how a bipolar, single-ended signal biased around ground can drive the AD7760 with the use of an external op amp, such as the AD8021.

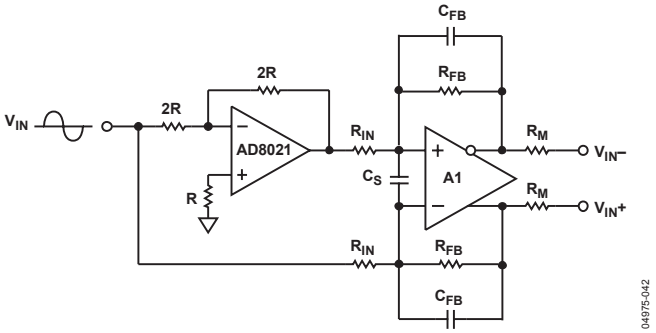

Figure 53. Single-Ended-to-Differential Conversion

The AD7760 employs a double-sampling front end, as shown in Figure 54. For simplicity, only the equivalent input circuit for $V_{IN}+$ is shown. The equivalent input circuitry for $V_{IN}-$ is the same.

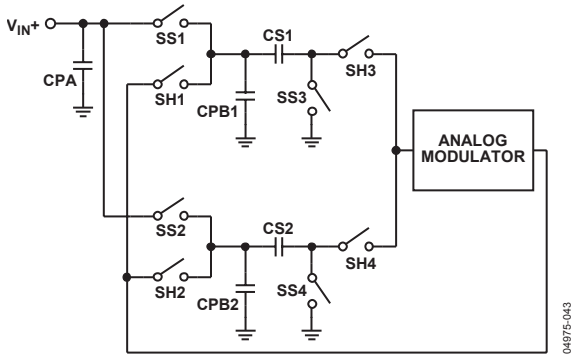

Figure 54. Equivalent Input Circuit

Sampling Switches SS1 and SS3 are driven by ICLK, whereas Sampling Switches SS2 and SS4 are driven by $\overline{\text{ICLK}}$. When ICLK is high, the analog input voltage is connected to CS1. On the falling edge of ICLK, the SS1 and SS3 switches open and the analog input is sampled on CS1. Similarly, when ICLK is low, the analog input voltage is connected to CS2. On the rising edge of ICLK, the SS2 and SS4 switches open and the analog input is sampled on CS2.

Capacitors CPA, CPB1, and CPB2 represent parasitic capacitances that include the junction capacitances associated with the MOS switches.

Table 9. Equivalent Component Values

Mode	CS1 (pF)	CS2 (pF)	CPA (pF)	CPB1/2 (pF)
Normal	51	51	12	20
Low Power	13	13	12	5

USING THE AD7760

The following is the recommended sequence for powering up and using the AD7760:

1. Apply power.
2. Start the clock oscillator, applying MCLK.
3. Take $\overline{\text{RESET}}$ low for a minimum of one MCLK cycle.
4. Wait a minimum of two MCLK cycles after $\overline{\text{RESET}}$ has been released.
5. Write to Control Register 2 to power up the ADC and the differential amplifier as required. The correct clock divider ($\overline{\text{CDIV}}$) ratio should be programmed at this time.
6. Write to Control Register 1 to set the output data rate.
7. Wait a minimum of five MCLK cycles after $\overline{\text{CS}}$ has been released.
8. Take $\overline{\text{SYNC}}$ low for a minimum of four MCLK cycles, if required, to synchronize multiple parts.

Data can then be read from the part using the default filter, offset, gain, and overrange threshold values. The conversion data read is not valid, however, until the group delay of the filter has elapsed. Once this has occurred, the DVALID bit read with the data LSW is set, indicating that the data is indeed valid.

The user can then download a different filter if required (see the Downloading a User-Defined Filter section). Values for gain, offset, and overrange threshold registers can be written or read at this stage.

DECOUPLING AND LAYOUT RECOMMENDATIONS

Due to the high performance nature of the AD7760, correct decoupling and layout techniques are required to obtain the performance as stated within this data sheet. Figure 55 shows a simplified connection diagram for the AD7760.

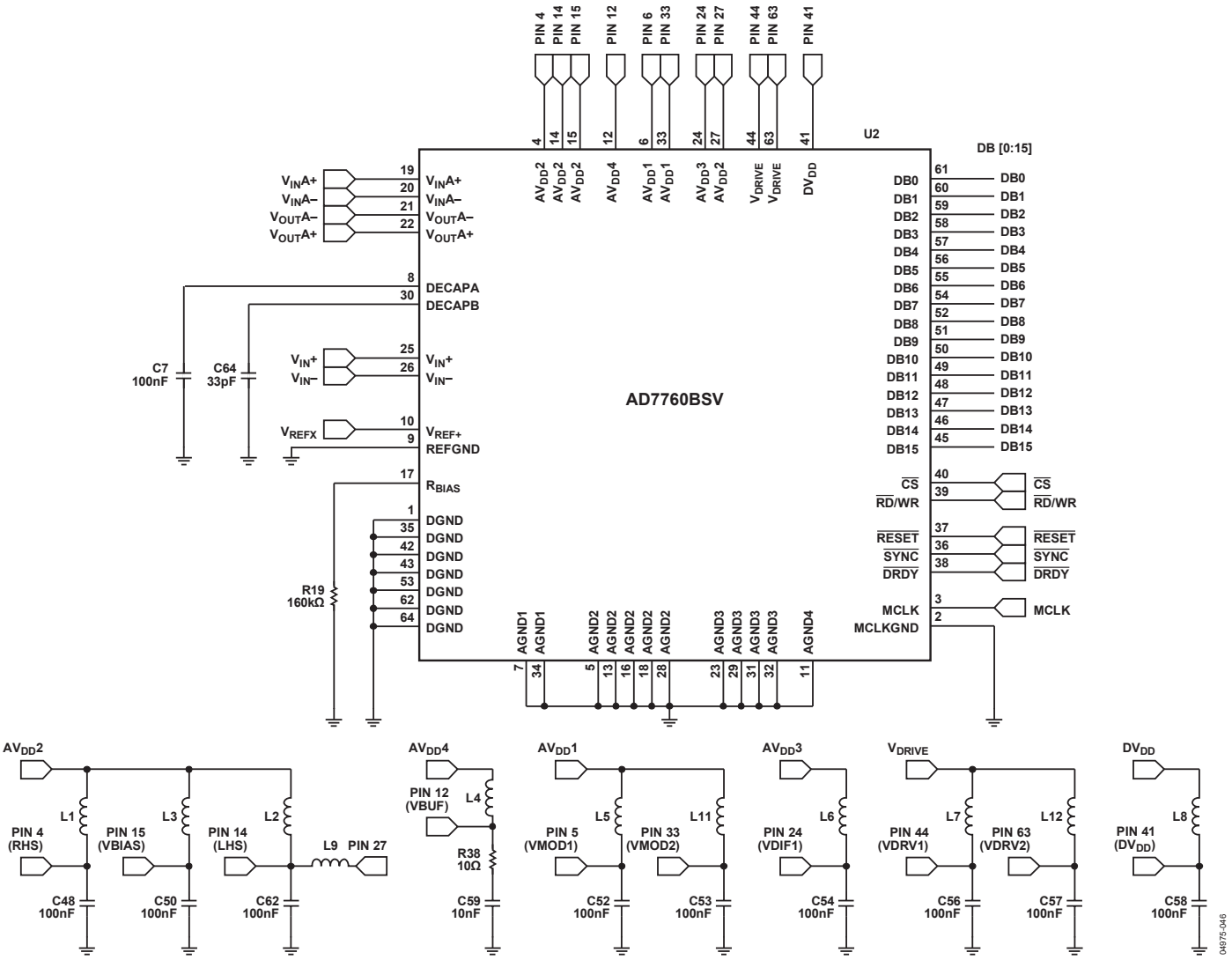

Figure 55. Simplified Connection Diagram

SUPPLY DECOUPLING

Every supply pin must be connected to the appropriate supply via a ferrite bead and decoupled to the correct ground pin with a 100 nF, 0603 case size, X7R dielectric capacitor. There are two exceptions to this:

- Pin 12 ($AV_{DD}4$) must have a 10 Ω resistor inserted between the pin and a 10 nF decoupling capacitor, which is connected to ground at Pin 9.
- Pin 27 ($AV_{DD}2$) does not require a separate decoupling capacitor or a direct connection to the supply, but instead is connected to Pin 14 via a 15 nH inductor.

ADDITIONAL DECOUPLING

There are two other decoupling pins on the AD7760—Pin 8 (DECAPA) and Pin 30 (DECAPB). Pin 8 should be decoupled with a 100 nF capacitor, and Pin 30 requires a 33 pF capacitor.

REFERENCE VOLTAGE FILTERING

A low noise reference source, such as the ADR431 (2.5 V) or ADR434 (4.096 V), is suitable for use with the AD7760. The reference voltage supplied to the AD7760 should be decoupled and filtered as shown in Figure 56.

The recommended scheme for the reference voltage supply is a 100 Ω series resistor connected to a 100 µF tantalum capacitor, followed by a series resistor of 10 Ω, and finally a 10 nF capacitor placed as close as possible to the V_{REF+} pin, decoupling this capacitor to the associated ground pin, Pin 11.

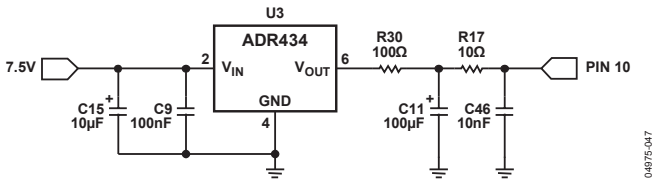

Figure 56. Reference Connection

DIFFERENTIAL AMPLIFIER COMPONENTS

The correct components for use around the on-chip differential amplifier are detailed in Table 8. Matching the components on both sides of the differential amplifier is important to minimize distortion of the signal applied to the amplifier. A tolerance of 0.1% or better is required for these components. Symmetrical routing of the tracks on both sides of the differential amplifier also assists in achieving the stated performance.

BIAS RESISTOR SELECTION

The AD7760 requires a resistor to be connected between the R_{BIAS} and AGND pins. The value of this resistor is dependent on the reference voltage being applied to the device. The resistor value should be selected to produce a current of 25 µA through the resistor to ground. For a 2.5 V reference voltage, the correct resistor value is 100 kΩ, and for a 4.096 V reference, the correct resistor value is 160 kΩ.

LAYOUT CONSIDERATIONS

While using the correct components is essential to achieve optimum performance, the correct layout is just as important. The AD7760 product page on the Analog Devices website contains the Gerber files for the AD7760 evaluation board. These files should be used as a reference when designing any system using the AD7760.

The location and orientation of some of the components mentioned in previous sections of this data sheet are critical, and particular attention must be paid to the components that are located close to the AD7760. Locating these components farther away from the device can have a direct impact on the achievable maximum performance.

The use of ground planes should also be carefully considered. To ensure that the return currents through the decoupling capacitors are flowing to the correct ground pin, the ground side of the capacitors should be as close as possible to the ground pin associated with that supply. A ground plane should not be relied on as the sole return path for decoupling capacitors because the return current path using ground planes is not easily predictable.

EXPOSED PADDLE

The AD7760 64-lead TQFP employs a 6 mm × 6 mm exposed paddle (see Figure 59). The paddle reduces the thermal resistance of the package by providing a path for heat energy to flow between the package and the PCB and, in turn, increases the heat transfer efficiency from the AD7760 package. Connecting the exposed paddle to the AGND plane of the PCB is essential in creating the conditions that allow the AD7760 package to perform to the highest specifications possible. The exposed paddle should not be connected directly to any of the ground pins on the AD7760 and should only be connected to the analog ground plane. Best practice is to use multiple vias connecting the exposed paddle to the AGND plane of the PCB.

PROGRAMMABLE FIR FILTER

As previously mentioned, the third FIR filter on the AD7760 is user programmable. The default coefficients that are loaded upon reset are given in Table 10, and the frequency responses are shown in Figure 57. The frequencies quoted in Figure 57 scale directly with the output data rate.

Table 10. Default Filter Coefficients

No.	Dec Value	Hex Value	No.	Dec Value	Hex Value
0	53656736	332BCA0	24	700847	AB1AF
1	25142688	17FA5A0	25	−70922	401150A
2	−4497814	444A196	26	−583959	408E917
3	−11935847	4B62067	27	−175934	402AF3E
4	−1313841	4140C31	28	388667	5EE3B
5	6976334	6A734E	29	294000	47C70
6	3268059	31DDDB	30	−183250	402CBD2
7	−3794610	439E6B2	31	−302597	4049E05
8	−3747402	4392E4A	32	16034	3EA2
9	1509849	1709D9	33	238315	3A2EB
10	3428088	344EF8	34	88266	158CA
11	80255	1397F	35	−143205	4022F65
12	−2672124	428C5FC	36	−128919	401F797
13	−1056628	4101F74	37	51794	CA52
14	1741563	1A92FB	38	121875	1DC13
15	1502200	16EBF8	39	16426	402A
16	−835960	40CC178	40	−90524	401619C
17	−1528400	4175250	41	−63899	400F99B
18	93626	16DBA	42	45234	B0B2
19	1269502	135EFE	43	114720	1C020
20	411245	6466D	44	102357	18FD5
21	−864038	40D2F26	45	52669	CDBD
22	−664622	40A242E	46	15559	3CC7
23	434489	6A139	47	1963	7AB

The default filter should be sufficient for most applications. It is a standard brick wall filter with a symmetrical impulse response. The default filter has a length of 96, is nonaliasing, and provides 120 dB of attenuation at Nyquist. This filter not only performs signal antialiasing, but also suppresses out-of-band quantization noise produced by the analog-to-digital conversion process. Any significant relaxation in the stop-band attenuation or transition bandwidth relative to the default filter can result in a failure to meet the SNR specifications.

The default filter characteristics scale with both the MCLK frequency applied and the decimation rate chosen by the user.

To create a filter, note the following:

- The filter must be an even, symmetrical FIR.
- The coefficients are in sign-and-magnitude format, with 26 magnitude bits and sign coded as positive = 0.
- The filter length must be between 12 taps and 96 taps in steps of 12.
- Because the filter is symmetrical, the number of coefficients that must be downloaded is half the filter length. The default filter coefficients exemplify this with only 48 coefficients listed for a 96-tap filter.
- Coefficients are written from the center of the impulse response (adjacent to the point of symmetry) outwards.
- The coefficients are scaled so that the in-band gain of the filter is equal to 134,217,726, with the coefficients rounded to the nearest integer. For a low-pass filter, this is the equivalent of having the coefficients summed arithmetically (including sign) to a +67,108,863 (0x3FF FFFF) positive value over the half-impulse-response coefficient set (a maximum of 48 coefficients). Any deviation from this introduces a gain error.

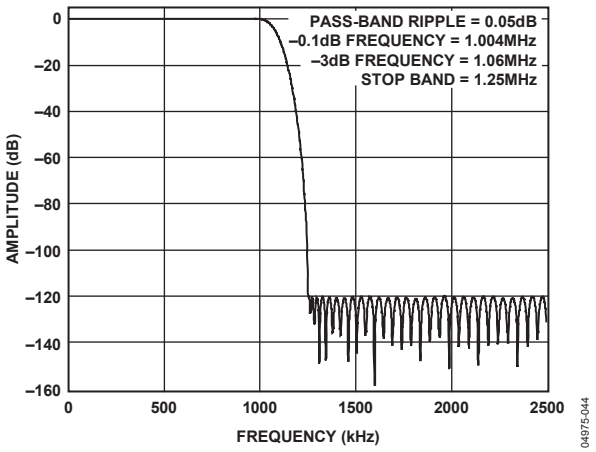

Figure 57. Default Filter Frequency Response (2.5 MHz ODR)

The procedure for downloading a user-defined filter is detailed in the Downloading a User-Defined Filter section.

DOWNLOADING A USER-DEFINED FILTER

As previously mentioned, the filter coefficients are 27 bits in length—one sign and 26 magnitude bits. Because the AD7760 has a 16-bit parallel bus, the coefficients are padded with 5 MSB 0s to generate a 32-bit word, split into two 16-bit words for downloading. The first 16-bit word for each coefficient becomes (00000, sign bit, Magnitude [25:16]), whereas the second word becomes (Magnitude [15:0]). To ensure that a filter is downloaded correctly, a checksum must also be generated and then downloaded following the final coefficient. The checksum is a 16-bit word generated by splitting each 32-bit word into four bytes and summing the bytes from all coefficients up to a maximum of 192 bytes (48 coefficients × four bytes). The same checksum is generated internally in the AD7760 and compared with the downloaded checksum. The DL_OK bit in the status register is set if these two checksums agree.

To download a user filter

1. Write to Control Register 1, setting the DL_FILT bit and the correct filter length bits corresponding to the length of the filter to be downloaded (see Table 11).
2. Write the first half of the current coefficient data (00000, sign bit, Magnitude [25:16]). The first coefficient to be written must be the one adjacent to the point of filter symmetry.
3. Write the second half of the current coefficient data (Magnitude [15:0]).
4. Repeat Step 2 and Step 3 for each coefficient.
5. Write the 16-bit checksum.
6. Use the following methods to verify that the filter coefficients are downloaded correctly:
    a. Read the status register, checking the DL_OK bit.
    b. Read data and observe the status of the DL_OK bit.

Note that because the user coefficients are stored in RAM, they are cleared after a $\overline{\text{RESET}}$ operation or a loss of power.

Table 11. Filter Length Values

FLEN [3:0]	Number of Coefficients	Filter Length
0000	Default	Default
0001	6	12
0011	12	24
0101	18	36
0111	24	48
1001	30	60
1011	36	72
1101	42	84
1111	48	96

EXAMPLE FILTER DOWNLOAD

The following is an example of downloading a short user-defined filter with 24 taps. The frequency response is shown in Figure 58.

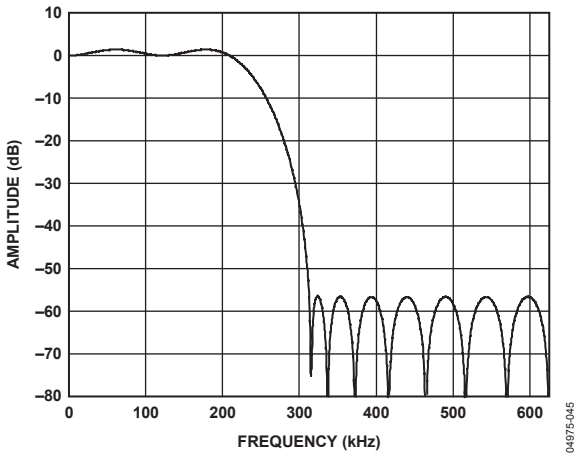

Figure 58. 24-Tap FIR Frequency Response

The coefficients for the filter are listed in Table 12 and are shown from the center of symmetry outwards. The raw coefficients were generated using a commercial filter design tool and were scaled appropriately so that their sum equals 67,108,863 (0x3FF FFFF).

Table 12. 24-Tap FIR Coefficients

Coefficient	Raw	Scaled
1	0.365481974	53188232
2	0.201339905	29300796
3	0.009636604	1402406
4	−0.075708848	−11017834
5	−0.042856209	−6236822
6	0.019944246	2902466
7	0.036437914	5302774
8	0.007592007	1104856
9	−0.021556583	−3137108
10	−0.024888355	−3621978
11	−0.012379538	−1801582
12	−0.001905756	−277343

Table 13 shows the hexadecimal values (in sign-and-magnitude format) that are downloaded to the AD7760 to realize this filter. The table is also split into the bytes that are summed to produce the checksum. The checksum generated from these coefficients is 0x0E6B.

Table 13. Filter Hexadecimal Values

	Word 1		Word 2	
Coefficient	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
1	03	2B	96	88
2	01	BF	18	3C
3	00	15	66	26
4	04	A8	1E	6A
5	04	5F	2A	96
6	00	2C	49	C2
7	00	50	E9	F6
8	00	10	DB	D8
9	04	2F	DE	54
10	04	37	44	5A
11	04	1B	7D	6E
12	04	04	3B	5F

Table 14 lists the 16-bit words the user would write to the AD7760 to set up the ADC and download this filter, assuming an output data rate of 1.25 MHz has been selected.

Table 14. Sequence of Write Instructions to Set Up Device and Download the Filter Example

Word	Description
0x0001	Address of Control Register 1.
0x8079	Control register data. DL filter: set filter length = 24, set output data rate = 1.25 MHz.
0x032B	First coefficient, Word 1.
0x9688	First coefficient, Word 2.
0x01BF	Second coefficient, Word 1.
0x183C	Second coefficient, Word 2.
…	Other coefficients.
0x0404	Twelfth (final) coefficient, Word 1.
0x3B5F	Final coefficient, Word 2.
0x0E6B	Checksum. Wait ($0.5 \times t_{ICLK} \times$ number of unused coefficients) for AD7760 to write 0s to the remaining unused coefficients.
0x0001	Address of control register.
0x0879	Control register data. Set read status and maintain filter length and decimation settings. Read contents of status register. Check Bit 7 (DL_OK) to determine if the filter was downloaded correctly.

AD7760 REGISTERS

The AD7760 has a number of user-programmable registers. The control registers are used to set the decimation rate, the filter configuration, the clock divider, and so on. There are also digital gain, offset, and overrange threshold registers. Writing to these registers involves writing the register address first, then a 16-bit data-word. Register addresses, details of individual bits, and default values are given in this section.

CONTROL REGISTER 1—ADDRESS 0x0001

Default Value 0x001A

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DL_ FILT	RD OVR	RD GAIN	RD OFF	RD STAT	0	SYNC	FLEN3	FLEN2	FLEN1	FLEN0	$\overline{\text{BYP F3}}$	$\overline{\text{BYP F1}}$	DEC2	DEC1	DEC0

Table 15. Bit Descriptions of Control Register 1

Bit	Mnemonic	Description
15	DL_FILT[1]	Download Filter. Before downloading a user-defined filter, this bit must be set. The filter length bits must also be set at this time. The write operations that follow are interpreted as the user coefficients for the FIR filter until all the coefficients and the checksum have been written.
14	RD OVR[1, 2]	Read Overrange. If this bit has been set, the next read operation outputs the contents of the overrange threshold register instead of a conversion result.
13	RD GAIN[1, 2]	Read Gain. If this bit has been set, the next read operation outputs the contents of the digital gain register.
12	RD OFF[1, 2]	Read Offset. If this bit has been set, the next read operation outputs the contents of the digital offset register.
11	RD STAT[1, 2]	Read Status. If this bit has been set, the next read operation outputs the contents of the status register.
10	0	0 must be written to this bit.
9	SYNC[1]	Synchronize. Setting this bit initiates an internal synchronization routine. Setting this bit simultaneously on multiple devices synchronizes all filters.
8 to 5	FLEN [3:0]	Filter Length Bits. These bits must be set when the DL_FILT bit is set before a user-defined filter is downloaded.
4	$\overline{\text{BYP F3}}$	Bypass Filter 3. If this bit is 0, Filter 3 (programmable FIR) is bypassed.
3	$\overline{\text{BYP F1}}$	Bypass Filter 1. If this bit is 0, Filter 1 is bypassed. This should only occur when the user requires unfiltered modulator data to be output.
2 to 0	DEC [2:0]	Decimation Rate. These bits set the decimation rate of Filter 2. All 0s implies that the filter is bypassed. A value of 1 corresponds to 2× decimation, a value of 2 corresponds to 4× decimation, and so on, up to the maximum value of 5, corresponding to 32× decimation.

[1] Bit 15 to Bit 9 are self-clearing bits.
[2] Only one of the bits from Bit 14 to Bit 11 can be set in any write operation because it determines the contents of the next read operation.

CONTROL REGISTER 2—ADDRESS 0x0002

Default Value After $\overline{\text{RESET}}$: 0x009B

Recommended register setting for power-up and normal operation using clock divide-by-2 ($\overline{\text{CDIV}}$ = 0) mode: 0x0002

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	$\overline{\text{CDIV}}$	0	PD	LPWR	1	D1PD

Table 16. Bit Descriptions of Control Register 2

Bit	Mnemonic	Description
5	$\overline{\text{CDIV}}$	Clock Divider Bit. This sets the divide ratio of the MCLK signal to produce the internal ICLK. Setting $\overline{\text{CDIV}}$ = 0 divides the MCLK by 2. If $\overline{\text{CDIV}}$ = 1, the ICLK frequency is equal to the MCLK.
3	PD	Power Down. Setting this bit powers down the AD7760, reducing the power consumption to 6.35 mW.
2	LPWR	Low Power. If this bit is set, the AD7760 is operating in a low power mode. The power consumption is reduced for a 6 dB reduction in noise performance.
1	1	Write 1 to this bit.
0	D1PD	Differential Amplifier Power Down. Setting this bit powers down the on-chip differential amplifier.

STATUS REGISTER (READ ONLY)

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PART 1	PART 0	DIE 2	DIE 1	DIE 0	0	LPWR	OVR	DL_OK	FILTOK	UFILT	$\overline{\text{BYP F3}}$	$\overline{\text{BYP F1}}$	DEC2	DEC1	DEC0

Table 17. Bit Descriptions of Status Register

Bit	Mnemonic	Comment
15, 14	PART [1:0]	Part Number. These bits are constant for the AD7760.
13 to 11	DIE [2:0]	Die Number. These bits reflect the current AD7760 die number for identification purposes within a system.
10	0	This bit is set to 0.
9	LPWR	Low Power. If the AD7760 is operating in low power mode, this bit is set to 1.
8	OVR	If the current analog input exceeds the current overrange threshold, this bit is set.
7	DL_OK	When downloading a user filter to the AD7760, a checksum is generated. This checksum is compared to the one downloaded following the coefficients. If these checksums agree, this bit is set.
6	FILTOK	When a user-defined filter is in use, a checksum is generated when the filter coefficients pass through the filter. This generated checksum is compared to the one downloaded. If they match, this bit is set.
5	UFILT	If a user-defined filter is in use, this bit is set.
4	$\overline{\text{BYP F3}}$	Bypass Filter 3. If Filter 3 is bypassed by setting the relevant bit in Control Register 1, this bit is also set.
3	$\overline{\text{BYP F1}}$	Bypass Filter 1. If Filter 1 is bypassed by setting the relevant bit in Control Register 1, this bit is also set.
2 to 0	DEC [2:0]	Decimation Rate. These bits correspond to the bits set in Control Register 1.

OFFSET REGISTER—ADDRESS 0x0003

Non-bit-mapped, Default Value 0x0000

The offset register uses twos complement notation and is scaled such that 0x7FFF (maximum positive value) and 0x8000 (maximum negative value) correspond to an offset of +0.78125% and −0.78125%, respectively. Offset correction is applied after any gain correction. Using the default gain value of 1.25 and assuming a reference voltage of 4.096 V, the offset correction range is approximately ±25 mV.

GAIN REGISTER—ADDRESS 0x0004

Non-bit-mapped, Default Value 0xA000

The gain register is scaled such that 0x8000 corresponds to a gain of 1.0. The default value of this register is 1.25 (0xA000). This results in a full-scale digital output when the input is at 80% of V_{REF}, tying in with the maximum analog input range of ±80% of V_{REF} p-p.

OVERRANGE REGISTER—ADDRESS 0x0005

Non-bit-mapped, Default Value 0xCCCC

The overrange register value is compared with the output of the first decimation filter to obtain an overload indication with minimum propagation delay. This is prior to any gain scaling or offset adjustment. The default value is 0xCCCC, which corresponds to 80% of V_{REF} (the maximum permitted analog input voltage). Assuming V_{REF} = 4.096 V, the bit is then set when the input voltage exceeds approximately 6.55 V p-p differential. Once the overrange bit is set, the DVALID bit in the status bits of the AD7760 ouptut is set to zero, providing another indication that an input overrange has occurred. Note that the overrange bit is set immediately if the analog input voltage exceeds 100% of V_{REF} for more than four consecutive samples at the modulator rate.

OUTLINE DIMENSIONS

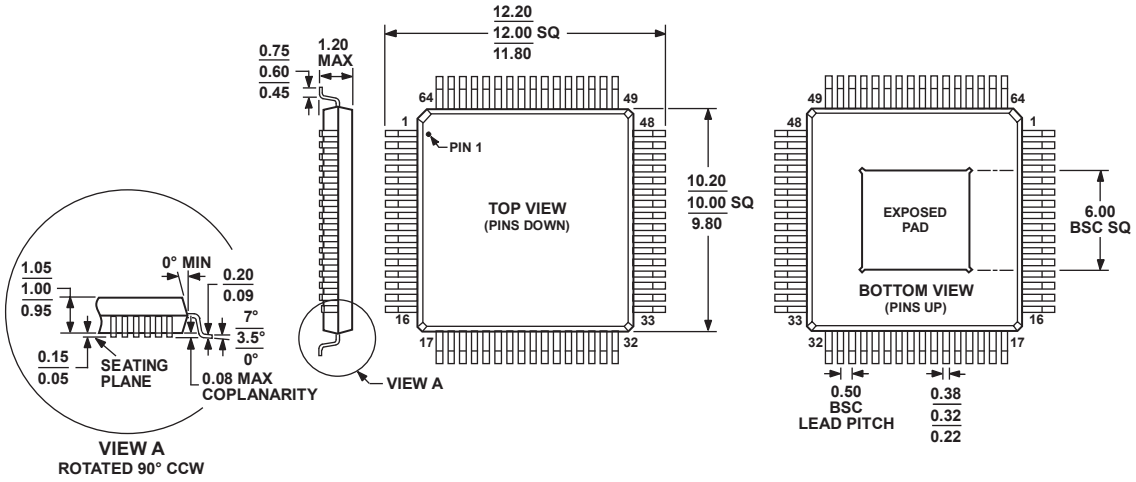

Figure 59. 64-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7760BSVZ[1]	−40°C to +85°C	64-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-64-2
AD7760BSVZ-REEL[1]	−40°C to +85°C	64-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-64-2
EVAL-AD7760EB		Evaluation Board	

[1] Z = Pb-free part.

NOTES

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